CdTe Nanowire Structures for Solar Cells

Thesis submitted in accordance with the requirements of the University of Liverpool for the degree of Doctor in Philosophy

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Abstract

This thesis investigates the growth and characterisation of CdTe and core-double shell ITO/CdS/CdTe nanowires (NWs), ITO/ZnO/CdS/CdTe/Mo thin-film solar cells and ITO/ZnO/CdS/CdTe(NW)/CdTe/Mo core-triple shell NW solar cells.

First, the generation of Au-catalysed CdTe NWs arrays on Mo foils is reported, with CdTe being deposited by close-space sublimation. NWs were up to 20 μm long, had diameters in the range 5 – 500 nm and densities in the range 10^6 – 10^7 cm^{-2}. A vapour-liquid-solid mechanism of NW growth, mediated by a Au-Te liquid catalyst, which accounts for the initial delay to NW nucleation (and the observed film growth) is postulated. By fitting a theoretical model of NW growth to experimental NW radius-time data, values for the sidewall diffusion length (2 μm) and sticking probability (0.61) were obtained. NW growth was also achieved on CdTe/Mo, with higher NW densities (10^8 cm^{-2}) achieved compared to growth directly on Mo. NW defects were evaluated by TEM and photoluminescence (PL). TEM analysis showed low-energy $\Sigma = 3$ grain boundaries present in the NWs, their incidence being dependent on the growth axis, which was either <110>, <111> or <112>. No high energy grain boundaries were observed. Their low-temperature PL spectra were dominated by excitonic emission with rarely observed above-gap emission also being recorded. PL also provided evidence of a deep level due to Au. UV-VIS-IR measurements showed that above-gap reflectance of NW arrays (~ 0.1%) was lower than for films of equivalent material (~ 10%).

Methods of coating the NWs with conformal CdS and ITO shells were explored, with RF sputtering proving most suitable. HRTEM imaging demonstrated that the CdS/CdTe interface was epitaxial, the quality of the core-shell interface being thought to be critical for NW solar cells. Low temperature PL spectra of CdS/CdTe NWs showed CdS luminescence typical of single-crystal material and also implied that interdiffusion at the core-shell interface occurred. Above-gap reflectance for core-double shell ITO/CdS/CdTe NWs was ~ 0.1%.

The fabrication procedures for thin-film CdTe devices on Mo foils were investigated so that understanding could be transferred to NW device fabrication. For thin-film devices, a peak efficiency of 8.0% was achieved upon incorporation of a double-anneal treatment process and a highly-resistive transparent ZnO layer. The main limitation to performance was the rectifying back contact, having a barrier height of $\phi_B = 0.51$ eV. Methods to improve the quality of the contact are suggested based on device modelling. Simulations comparing the operation of thin-film and NW solar cells predict that when minority carrier diffusion lengths are short (< 0.7 μm), J_{SC} enhancements can be achieved by adopting the NW device's radial junction configuration. For the full NW device, efficiencies of 2.5% were obtained.

Declaration

I declare that with the exception of those procedures listed below all the work presented in this thesis was carried out by the candidate. I also declare that none of this work has been previously submitted for any degree and that it is not being submitted for any other degree.

- Transmission electron microscopy, FIB-SEM images and one other SEM image (Fig 5.23b) presented in Chapters 5 -7 were taken/performed by Dr. Budhika Mendis, Mr. Leon Bowen and Dr. Aidan Taylor, GJ Russell Microscopy Facility, Durham University, Durham, UK.
- Modelling of nanowire growth (fits to experimental data presented in Figs 5.10 and 5.14) in Chapter 5 was carried out by Alexei Bolshakov and Vladimir Dubrovskii, St. Petersburg Academic University, St. Petersburg, Russia.
- XRD measurements included in Chapter 5 were performed by Dr. Jonathan Alaria, Department of Chemistry, University of Liverpool, Liverpool, UK.
- MOCVD growth of CdS and CdZnS, reported in Chapter 5, was performed by Dr. Giray Kartopu , Glyndwr University, St. Asaph, UK.
- CBD growth of CdS, reported in Chapter 5 and SIMS measurements, reported in Chapter 7, were performed by Dr. Guillaume Zoppi, Northumbria University, Newcastle, UK.
- Four-point probe resistivity measurement of an individual CdS/CdTe core-shell nanowire was perfomed by Dr. Alexander Walton, Department of Physics, Leeds University, Leeds, UK.

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*The candidate was based at Durham University for the period of October 2009 – March 2011 and then at the University of Liverpool for the period of March 2011 – July 2013.

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Chapter 1 : Introduction

With increasing acceptance of the anthropogenic impact on global climate trends comes the urgent call for a drastic reduction in greenhouse gas emissions. Attempts to place legally binding targets were first made in 1997 within the Kyoto Protocol, with the 192 involved parties (including the EU) moving into the second commitment period (2013-2020) this year, each with varying targets to reduce emissions. The concerns set out at Kyoto were echoed at the Copenhagen Summit, although no additional legally-binding targets were set.[1] Nevertheless, the overriding issue highlights the requirement for a significant increase in the use of renewable technologies for energy generation in place of the continued burning of fossil fuels. The need to diversify global energy generation is also an issue of sustainability and reliability of supply, with fossil fuel reserves depleting and global energy demand expected to increase by a third from 2010 to 2035.[2] However, currently only ~ 10% of the world's energy generation is produced by renewables[2], this figure being boosted primarily by hydroelectric power.

Of all renewable technologies, solar photovoltaics (PV) has the greatest potential to meet these growing energy demands, the amount of solar energy reaching the Earth being over 10,000 times the current energy consumption of man[3]. Indeed, covering an area the size of Scotland (78,000 km^2) with solar PV panels that are 20% efficient should satisfy the energy requirements of the whole of human society[4]. Moreover, during operation, solar panels generate no pollution - unlike some alternative renewable technologies such as biomass - and some manufacturers now give guarantees that they will produce at least 80% of their initial rated peak output after 25 years[5]. The solar PV industry has been growing rapidly – installed global capacity increased from ~ 2 GW in 2000 to ~ 56 GW in 2011[4] – and costs continue to fall as production levels and efficiencies increase. Reichelstein *et al.*[6] state that whilst utility PV installations are not yet cost competitive with fossil fuel power stations, cost parity has been achieved for commercial PV.

By far the most dominant PV technology until now has been based on crystalline silicon homo-junctions, this technology benefiting from the Si micro-electronics industry. Indeed, crystalline Si makes up ~ 90% of the PV industry, and laboratory scale research towards novel concepts to improve efficiency continue. However, since Si is an indirect band gap semiconductor it has a low absorption coefficient and therefore relatively thick Si wafers (> 100 μm) must be used to absorb the light. These wafers are expensive to produce due to the

growth, purification and slicing processes that are necessary. As a result, much interest has been shown to alternative technologies based on thin-films (2 - 10 μm) of highly absorbing direct band gap semiconductors, such as CdTe or copper indium gallium diselenide (CIGS), due to the lower material costs. CdTe in particular has a significant presence in the global PV industry owing to the success of First Solar, this company making up 9% of the installed PV capacity in 2011.[4]

CdTe has an optical band gap (1.5 eV) well matched to the solar spectrum and a high absorption coefficient, and polycrystalline CdTe films may be deposited stoichiometrically by simple deposition techniques. Moreover, the concerns about toxic Cd emissions that are voiced about CdTe PV may be unfounded given that it has been shown that upon taking into account the entire manufacturing processes of various energy generation technologies, coal, oil, nuclear and even Si-based PV all release more Cd than CdTe-based PV[7]. On the other hand, the best module and individual cell efficiencies of CdTe PV (16.1% and 19.6% respectively[8]) remain lower than Si (22.9% and 25.0%[8]) largely because the open-circuit voltages achieved in CdTe devices (the highest is 857 mV[8]) are well below the maximum value defined by the band gap. This discrepancy is thought to be due to the failure to achieve sufficiently high *p*-type doping densities in CdTe, and to excessive carrier recombination that is associated with the polycrystallinity of the material (see Chapter 2). Indeed, improving the open-circuit voltage (and therefore the efficiency) remains a primary objective of CdTe PV research, as does reducing the cost of manufacturing processes and the thickness of the active layer. The latter concern has been brought to the fore amid concerns of the availability of Te and its increasing price[9]. The slow improvement to the efficiencies of CdTe devices (the world record has increased by 3.8% in 20 years[8, 10]) and the failure to address the issue of reducing material usage has accompanied a lack of willingness to alter the basic design of the CdTe solar cell – the thin-film metal/CdTe/CdS/TCO/glass 'superstrate' design, where 'TCO' is transparent conducting oxide.

In this work, an entirely novel design is investigated, one that incorporates nanowires (NWs) and replaces the traditional planar *p-n* junction with an array of radial core-shell *p-n* junctions. It is based on the core-shell NW solar cells that have been researched for the Si system over the last decade (see Chapter 3), but as yet has only been rarely studied for the CdTe system. A schematic diagram of a cross section of a core-shell ITO/CdS/CdTe(NW)/CdTe/Mo NW solar cell is shown in Fig 1.1. It consists of a continuous film/NW CdTe structure grown on a Mo substrate and coated with shell layers of CdS and

indium tin oxide (ITO). Both planar and radial heterojunctions are formed at the CdTe/CdS interface.

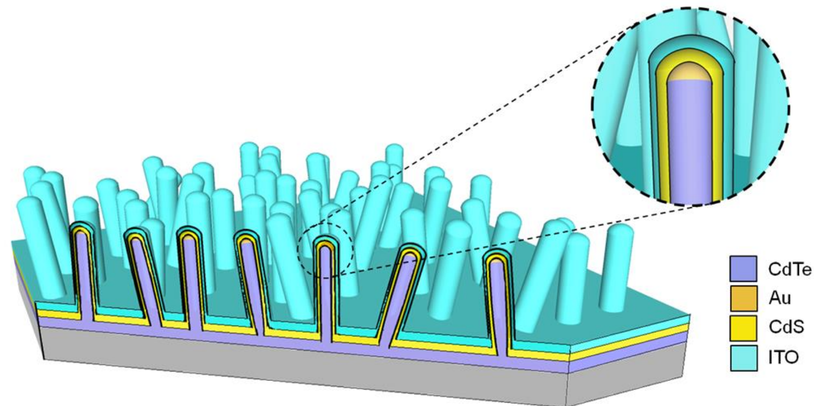

Fig 1.1: Schematic showing a cross-section of a core-shell ITO/CdS/CdTe(NW)/CdTe/metal nanowire solar cell.

The device design offers a number of potential advantages (see Chapters 3, 6 and 7). Firstly, the radial junction geometry orthogonalises the processes of light absorption and carrier collection and so these processes may be optimised separately by controlling the height and diameter of the CdTe NWs respectively. This could ultimately yield a reduction in bulk recombination in the CdTe and therefore increase open-circuit voltage and short-circuit current. Secondly, the absorption enhancements yielded by NW arrays may allow light to be absorbed using a smaller volume of CdTe than in traditional devices. Thirdly, replacing the glass superstrate with a lightweight metal substrate may yield reductions in the manufacture, transport and installation costs of CdTe devices, and enables roll-to-roll cell production.

The development of preliminary devices based on the design shown in Fig 1.1 is the ultimate objective of the work presented in this thesis, with particular focus on the growth of the separate components of the final structure and the characterisation of their physical properties. An overview of the structure of the thesis is as follows:

i. Chapter 2 includes a description of the underlying physics that govern the operation of PV devices that are based on semiconductor junctions. Some of the common PV technologies are reviewed, with particular emphasis given to CdTe PV;
ii. Chapter 3 reviews some of the key aspects of semiconductor NWs and their use in PV devices. First, a description of the various methods to fabricate NWs is given, with particular focus on the vapour-liquid-solid mechanism. Some of the configurations in which NWs may be incorporated into PV devices are explained. The properties of NWs are reviewed, as are the challenges associated with using

them in devices. Literature reviews of CdTe NW growth and NW solar cell fabrication are presented;

iii. Chapter 4 gives a description of the experimental and modelling techniques used;

iv. In Chapter 5, the growth of Au-catalysed CdTe NWs is reported (with a preliminary investigation into the generation of Au catalysts by annealing thin Au films being included in Appendix A). The growth mechanism of the NWs, both on Mo foils and CdTe films, is investigated. An evaluation of various deposition techniques for the coating of CdTe NWs with CdS and ITO shells is also reported;

v. Chapter 6 details an extensive characterisation of CdTe NWs, CdS/CdTe core-shell NWs and ITO/CdS/CdTe core-double shell NWs. The growth axis, planar defects and core-shell interface of the NWs are investigated by transmission electron microscopy, and point defects are evaluated using photoluminescence. UV-VIS spectrophotometry of NW arrays and electrical measurements of individual NWs are also presented;

vi. In Chapter 7, a preliminary study of the development of planar CdTe devices on Mo substrates is first reported, a baseline efficiency of 8.0% being yielded. Modelling of planar devices is also presented, demonstrating methods in which device performance may be improved. Simulations of the potential enhancements to device efficiency yielded by use of radial *p-n* junctions as opposed to a planar junction are then presented. Finally, experimental results of CdTe NW solar cells are reported, with a peak efficiency of 2.5% being obtained.

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Chapter 2 : Photovoltaic device physics and CdTe devices

2.1 Introduction

The photovoltaic (PV) effect can be simply described as the generation of a voltage in a material, or in a combination of two different materials in close contact, upon exposure to light. Subsequently, by connecting such photovoltaic material(s) in an electrical circuit, a photocurrent may be generated without the use of any external power supply. The photovoltaic effect was first observed by Adams and Day in 1876 in Se with two Pt contacts[1]. Notable milestones in the development of PV device technology include a device constructed from Se and Au which had a energy conversion efficiency of 1% in 1883[2] and a Si device constructed at Bell Laboratories in 1954 that had a 6% efficiency.[3]

In this Chapter the underlying physics behind the photovoltaic effect is described, and some of the leading PV technologies are reviewed, with particular focus on CdTe devices.

2.2 The photovoltaic effect

The processes that are fundamental for the conversion of light energy into electrical energy by the PV effect are[4]: a) The excitation of electron-hole pairs by photons; b) the separation of electrons and holes by an electric field; and c) their extraction to an external circuit.

2.2.1 Photo-generation of free carriers

Semiconductors are ideal materials to use as absorbing layers in PV devices since their optical energy gaps between their valence band maxima and conduction band minima are often comparable to the energies of photons in the solar spectrum (see Section 2.3.3).

In a direct band gap semiconductor, the valence band maximum, E_V, has the same wavevector, k, as the conduction band minimum, E_C.[5] A photon with energy $E_\gamma \geq E_g$, where E_g is the optical band gap and equal to $E_C - E_V$, incident on the material may excite an electron from the valence band into the conduction band, leaving a free hole in the valence band. Upon excitation, the excess kinetic energy of the charge carriers, equal to $E_\gamma - E_g$, is usually lost by thermalisation leaving only E_g of potential energy. Photons with $E_\gamma < E_g$ will not excite electrons and the material is said to be transparent to such photons of wavelength, $\lambda > hc/E_g$. In the case of an indirect band gap semiconductor, the valence band maximum is at a different k to the conduction band minimum and therefore since the momentum must be conserved in

optical transitions, an electron must be excited simultaneously by a photon together with either the absorption or emission of a phonon. Consequently, indirect gap materials (e.g. Si, Ge) have lower absorption coefficients than direct gap materials (e.g. CdTe, GaAs, InP).

2.2.2 Junction devices

The principal types of electrical junctions providing the field necessary for charge separation in PV devices are now described.

2.2.2.1 Homo-junction. Fig 2.1a shows a schematic diagram of the formation of a *p-n* homo-junction upon bringing together *p*- and *n*-type regions of the same semiconductor material and Fig 2.1b shows the equivalent electronic band structure representation, including band edges, Fermi levels, electron affinities, E_{ea}, and work functions, ψ.

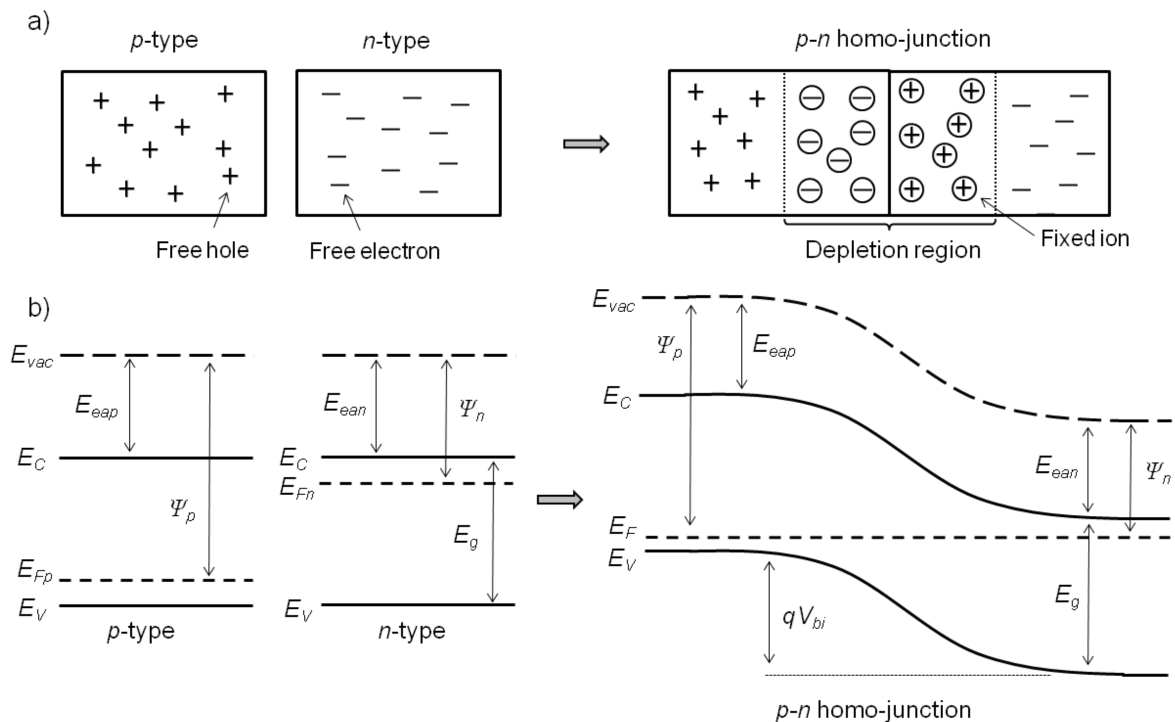

Fig 2.1: a) A schematic diagram and b) an electronic band structure representation of the formation of a homo-junction upon bringing together *p*- and *n*-type semiconductors.

Junction formation is described as follows: The initial concentration gradient of carriers causes electrons to diffuse from the *n*-type material to the *p*-type material, leaving uncompensated positively charged fixed ions in the *n*-type material near the interface, and holes to diffuse in the opposite direction, leaving negatively charged fixed ions in the *p*-type material. This creates a region of space charge called the ‘depletion region’ (as shown in Fig 2.1a). The potential difference established by these ions drives a ‘drift’ current in the opposite direction to the diffusion current. Equilibrium is reached when these two currents are equal.

The equilibration of the Fermi levels and the band-bending associated with junction formation is shown in the band diagram (Fig 2.1b). The built in voltage, V_{bi}, of the junction is determined from the difference between the *p*- and *n*-type work functions, i.e. $(\psi_p - \psi_n)/q$, where q is the electron charge. In Fig 2.1b, E_{eap} and E_{ean} are the electron affinities of the respective semiconductors, and E_{Fn} and E_{Fp} are the initial Fermi levels prior to junction formation.

Homo-junctions are commonly used in bulk Si PV devices: Typically a *p*-type Si wafer (doped *p*-type with e.g. boron) is grown, and a thin *n*-type layer is formed by diffusing *n*-type dopants (e.g. phosphorous) to a depth of a few hundred nms[4]. Homo-junctions are not suitable for materials with high absorption coefficients in which the majority of carriers are generated near the surface and are vulnerable to surface recombination.

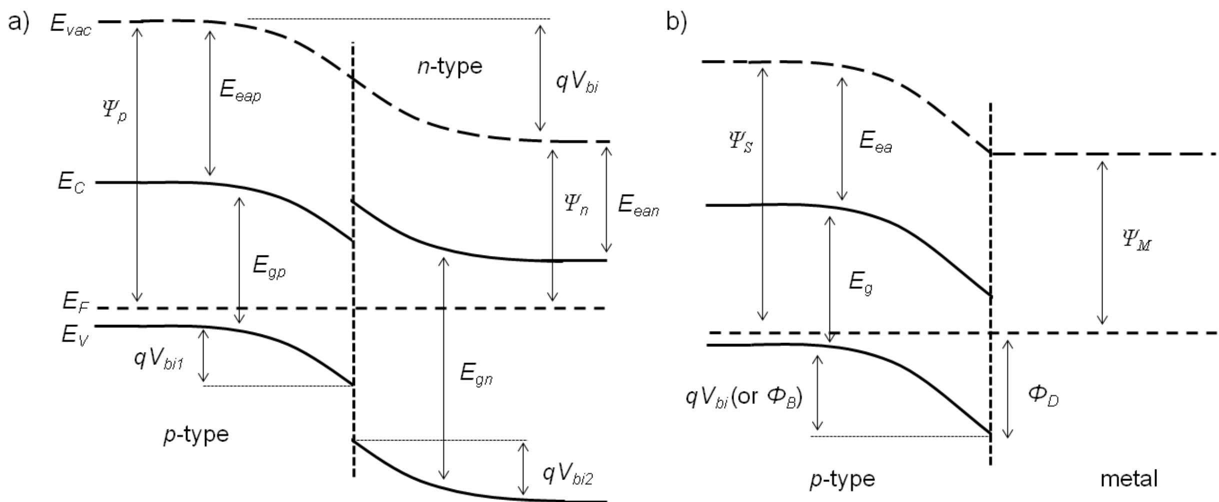

Fig 2.2: Electronic band structure representations of a) *p-n* hetero-junction and b) a Schottky junction between a *p*-type semiconductor and a metal.

2.2.2.2 Hetero-junction. For direct gap materials, to ensure the *p-n* junction is not close to a free surface or metal-semiconductor interface, hetero-junctions are used (the *n*- and *p*-type regions are of different materials). In this configuration, one of the layers (usually the *p*-type layer) is designated as the absorbing layer with a band-gap optimised to the incoming light, and the other (usually the *n*-type) is a 'window layer' that has a wide band-gap and enables light to enter the absorbing layer. However, unlike in homo-junctions, differences in E_g and E_{ea} can lead to 'spikes' in the conduction or valence bands, which may (detrimentally) act as potential barriers to carrier transport. Their sizes may be approximated by Anderson's rule[6], which is used to construct the hetero-junction band-diagram, i.e. $\Delta E_C = E_{eap} - E_{ean}$ and $\Delta E_V = (E_{eap} + E_{gp}) - (E_{ean} + E_{gn})$. The total built-in voltage is equal to $V_{bi} = V_{bi1} + V_{bi2}$, this also equal to $(\psi_p - \psi_n)/q$.[5]

2.2.2.3 Schottky junction. A potential difference may also be formed using a Schottky junction – a rectifying metal-semiconductor junction. A Schottky junction to a *p*-type material is formed if the work function of the metal, ψ_M, is smaller than that of the semiconductor, ψ_S, as shown in Fig 2.2b. As with homo- and hetero-junctions, when the two materials meet, carriers diffuse (in this case holes diffuse to the metal) and leave fixed ions (in this case negative ions left in the semiconductor) near the interface, until the Fermi levels are aligned and equilibrium is reached. The height of the hole barrier, qV_{bi} (or ϕ_B), that is created between the bulk and surface of the semiconductor is equal to the difference in metal and semiconductor work-functions, and can also be expressed as $\phi_B = \phi_D - (E_F - E_V)$, where $\phi_D = (E_{ea} + E_g) - \psi_M$ and is the difference between the semiconductor Fermi level at the metal interface and in the bulk. Equivalently, a Schottky junction to an *n*-type semiconductor is formed when $\psi_M > \psi_S$. Whilst solar cells using Schottky junctions alone may theoretically have efficiencies up to 18.5%[7], these junctions are more widely studied in the context of them being detrimental to solar cell performance when they exist at the back contact of homo- or hetero-junction solar cells (see Section 2.5).

2.2.3 Properties of p-n junctions

A number of properties of a *p-n* junction, such as the built-in voltage, the depletion region width and junction capacitance, are dependent on the extent to which the *n*- and *p*-type semiconductors are doped, i.e. on the donor and acceptor doping concentrations, N_D and N_A (Note that for doped semiconductors the concentration of free electrons is approximately equal to N_D and the concentration of holes approximately equal to N_A). The built in voltage of a hetero-junction may be defined as the sum of $(E_{Fn} - E_i)/q$ and $(E_i - E_{Fp})/q$ and therefore by the following equation[5];

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right) + \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) = \frac{kT}{q}\ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{2.1}$$

where k is Boltzmann's constant and T is the temperature. The depletion region width, W, may be derived by solving Poisson's equation, and for a hetero-junction is equal to;

$$W = \left[\frac{2\varepsilon_0(V_{bi} - V)(\varepsilon_n N_D + \varepsilon_p N_A)}{e\varepsilon_n N_A N_D}\right]^{\frac{1}{2}} \tag{2.2}$$

where ε_0 is the permittivity of free space, ε_n and ε_p are the relative permittivities of the *n*- and *p*-type materials and V is the applied voltage. Hence under forward bias, the depletion region

becomes narrower and under reverse bias, wider. In the case whereby $N_D >> N_A$, which is often true in CdTe/CdS devices (see Section 2.5), this is simplified to;

$$W = \left[\frac{2\varepsilon_0\varepsilon_p(V_{bi} - V)}{eN_A}\right]^{\frac{1}{2}} \tag{2.3}$$

and the depletion region only extends into the *p*-type material, i.e. it is one-sided. In this case, since the junction capacitance is given by $C = \varepsilon_p\varepsilon_0/W$, it is possible to determine N_A from the gradient of a plot of $1/C^2$ vs. V. For a full derivation of these formulae and more extensive descriptions of semiconductor device physics, the reader is referred to Refs. 4, 5 and 8.

2.3 Electrical characteristics of solar cells

This section describes the determination of PV device performance and explains the reasons for efficiency losses. Mechanisms of charge transport in a *p-n* junction are reviewed.

2.3.1 Equivalent circuit of a photovoltaic device

To determine the working parameters of a PV device, current-voltage (*J-V*) measurements are made both under illumination and in the dark. An ideal PV device in the dark is essentially a diode, through which flows a finite dark current, *J*, which may be expressed as a function of voltage using the Shockley diode equation[9, 10];

$$J = J_0\left(e^{qV/nkT} - 1\right) \tag{2.4}$$

where J_0 is the reverse saturation current, and n is the diode ideality factor. When illuminated, a photo-generated current, J_L, originating from the PV effect, is introduced:

$$J = J_0\left(e^{qV/nkT} - 1\right) - J_L \tag{2.5}$$

Fig 2.3a shows the equivalent circuit, with the photo-generated current in parallel with a diode. In reality, there are finite series, R_S, and shunt, R_{SH}, resistances (see Fig 2.3b), the latter accounting for short-circuit pathways through the device. Equation 2.5 must therefore be modified to include these parasitic resistances:

$$J = J_0\left(e^{(qV - JR_S)/nkT} - 1\right) + \frac{(V - JR_S)}{R_{SH}} - J_L \tag{2.6}$$

Evidently, the conditions required to regain the ‘ideal’ behaviour would be $R_S = 0$, and $R_{SH} = \infty$.

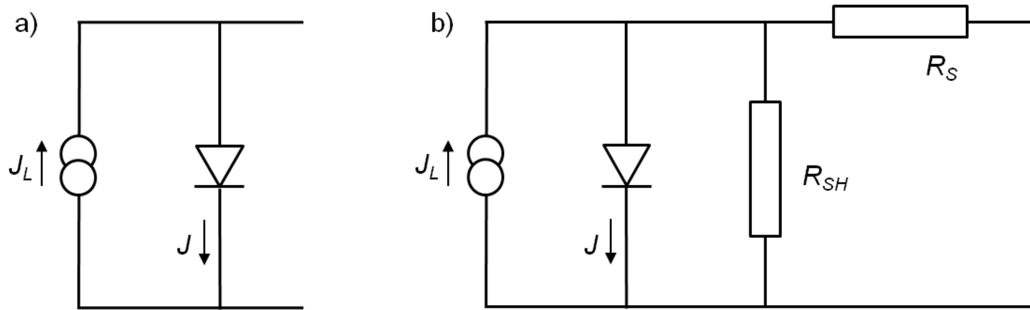

Fig 2.3: Equivalent circuits of a) an ideal photovoltaic device and b) a non-ideal device with finite series and shunt resistances.

2.3.2 J-V parameters of a device

Typical light and dark *J-V* curves are shown in Fig 2.4. Both demonstrate the rectifying characteristics of a diode, and the ‘light’ curve is shifted down the *y*-axis by J_L.

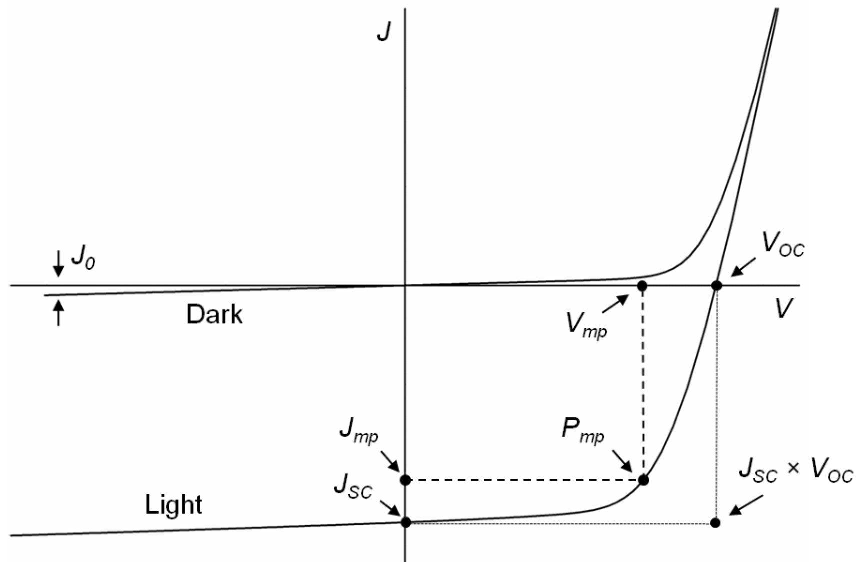

Fig 2.4: Typical *J-V* curves for a solar cell in the dark and under illumination.

The short-circuit current, J_{SC}, is taken from the *y*-axis intercept of the illuminated curve and is the current generated at $V = 0$. The open-circuit voltage, V_{OC}, is taken from the *x*-axis intercept of the illuminated curve and is the applied bias at which no net current flows through the device, i.e. at $J = 0$. Assuming ideal conditions (Equation 2.5), and setting $J = 0$, V_{OC} is expressed as

$$V_{OC} = \frac{nk_BT}{q} ln\left(\frac{J_L}{J_0} + 1\right) \tag{2.7}$$

The maximum power point, P_{mp} (indicated on Fig 2.4), of the *J-V* curve divided by the product of V_{OC} and J_{SC} gives the fill factor, *FF*, as follows:

$$FF = \frac{V_{mp}J_{mp}}{V_{OC}J_{SC}} \times 100\% = \frac{P_{mp}}{V_{OC}J_{SC}} \times 100\% \tag{2.8}$$

Since the efficiency, η, is simply the ratio P_{mp}/P_I, where P_I is the incident power, Equation 2.8 can be rearranged to yield an expression for η in terms of J_{SC}, V_{OC} and *FF*, this being;

$$\eta = \frac{V_{OC}J_{SC}FF}{P_I} \tag{2.9}$$

2.3.3 Fundamental losses in real devices

2.3.3.1 Shockley-Queisser Limit. From Equation 2.9, it is clear that V_{OC}, J_{SC} and *FF* should be maximised in order to obtain high η. In a single-junction device this involves choosing a semiconductor with an optical band gap well matched to the incident spectrum. It is normal to use the AM1.5 solar spectrum for device characterisation, this being shown in Fig 2.5a[11]. It is the spectrum of the sun modelled as a black-body emitting at a temperature of 5760K and attenuated by absorption in the Earth's atmosphere[4] (mainly by water and CO_2) at a lattitude of 42° - the incident spectrum is attenuated to a greater extent at higher latitudes since the optical depth of the atmosphere is greater. To maximise the obtainable J_{SC}, it may be considered wise to choose a semiconductor with a relatively narrow band gap, e.g. $E_g \sim 0.5$ eV, so that all wavelengths with $\lambda < 2500$ nm may be absorbed. However, *p-n* junctions fabricated from narrow band gap materials have low V_{bi} and therefore low V_{OC}. This can be understood by substituting the following expression[5] for n_i;

$$n_i^2 = N_C N_V e^{-E_g/kT} \tag{2.10}$$

where N_C and N_V are the effective densities of states in the conduction and valence bands respectively, into Equation 2.1 to yield an expression for V_{bi} in terms of E_g;

$$V_{bi} = \frac{E_g}{q} \ln\left(\frac{N_D N_A}{N_C N_V}\right) \tag{2.11}$$

On the other hand, if a *wide*-band gap material is chosen, V_{bi} and therefore V_{OC} can be higher, but a large proportion of the spectrum will not be absorbed and J_{SC} will be lower. Hence a compromise must be made, the maximum obtainable efficiency, η_{max}, as a function of E_g for the AM1.5 spectrum being shown in Fig 2.5b: η_{max} peaks at ~ 30% in the range

E_g = 1.1 - 1.5 eV and tails off towards lower and higher values of E_g. This curve was first calculated by Shockley and Quiesser[12] in 1961. All the common solar cell materials – Si, InP, GaAs and CdTe – have band gaps close to the maximum.

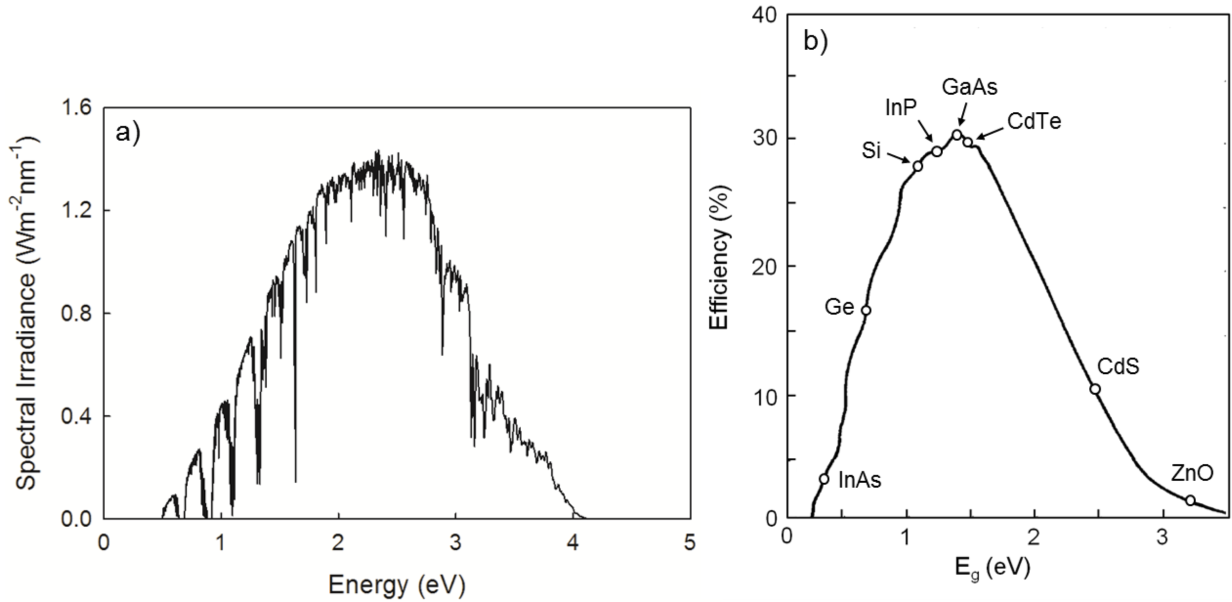

Fig 2.5: a) The AM1.5 solar spectrum, taken from the ASTM G173-03 standard[11]. b) Maximum efficiency of a single junction solar cell as a function of the optical band gap of the absorber layer. A number of intrinsic and compound semiconductor materials are marked on the graph.

This 'Shockley-Quiesser' limit can be exceeded however, by using more than one *p-n* junction. 'Multi-junction' devices comprise stacks of materials with different band-gaps to target different regions of the solar spectrum and therefore generate a high J_{SC}, and are designed so that their total V_{OC} is roughly the sum of the V_{OC}'s of the individual junctions[13]. For example, a InGaP/GaAs/InGaAs device has been reported to have η = 37.7%.[14]

2.3.3.2 Typical J_{SC} losses. Photons lost to reflection and absorption in non-active layers of a device do not contribute to the photo-current. Moreover, if $N_D >> N_A$ then carriers generated in the *n*-type window layer may not contribute. In such cases the depletion region exists entirely in the *p*-type region and minority carrier diffusion lengths are insufficient to transport holes to the depletion region. Losses may also occur when carriers are generated deep in the *p*-type layer[15] and for thin absorbers for which there are transmission losses[16].

2.3.3.3 Typical V_{OC} losses. According to Equation 2.1, V_{bi} and therefore V_{OC} can only be maximised relative to the optical band gap provided N_D and N_A are sufficiently high[17]. V_{OC} is also reduced by recombination current[17], which is typically higher in poly- than mono-

crystalline semiconductors since points defects related to impurities and dangling bonds at grain boundaries act as recombination centres.

2.3.3.4 Parasitic Resistances (R_S and R_{SH}). Contributions to R_S include; a) the intrinsic resistances of the *p*- and *n*-layers themselves, b) low conductivity in the transparent conducting oxide[17] and c) potential barriers to charge transport at grain boundaries, material interfaces and non-Ohmic contacts[18]. R_S is approximately the inverse of the gradient of the curve at the steepest section in forward bias. The effect of R_S on the *J-V* curve of a device is shown in Fig 2.6a; increased R_S is initially only detrimental to *FF*, but in extreme cases also to J_{SC}.

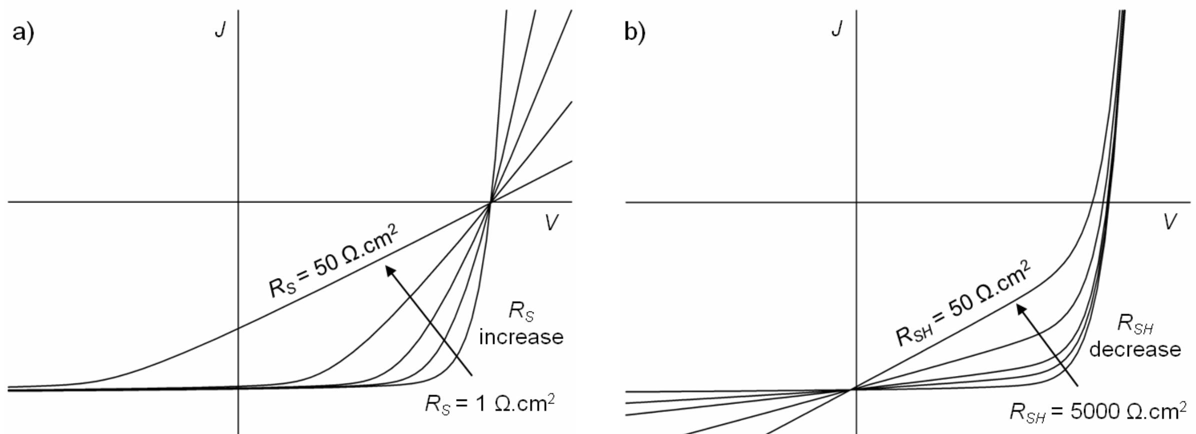

Fig 2.6: The detrimental effect of a) increasing R_S and b) decreasing R_{SH} on the shape of *J-V* curves in a solar cell, generated using SCAPS[19] (see Chapter 4 for a description of SCAPS).

Low R_{SH} indicates the presence of leakage pathways through a device, possible arising from pinholes[20]. R_{SH} is approximately the inverse of the gradient of the *J-V* curve in reverse bias. The effect of decreased R_{SH} on a *J-V* curve, as shown in Fig 2.6b, is initially to decrease *FF*, and in extreme cases, to decrease V_{OC}.

2.3.4 Carrier transport mechanisms

There are a number of possible mechanisms by which current may flow across *p-n* junctions as reviewed by Alturkestani[21]. Here, some of the more common mechanisms are reviewed, along with experimental methods for identifying them in a device.

2.3.4.1 Recombination in depletion region. In a *p-n* junction device, current is typically dominated by recombination processes or by generation and subsequent diffusion. Whilst recombination always takes place somewhere in the device, in the ideal case this occurs entirely in the quasi-neutral regions and not in the depletion region. Carrier transport in the depletion region is instead dominated by diffusion and in this case the ideality factor, $n = 1$.[5] In practice, recombination often also occurs in the depletion region[22].

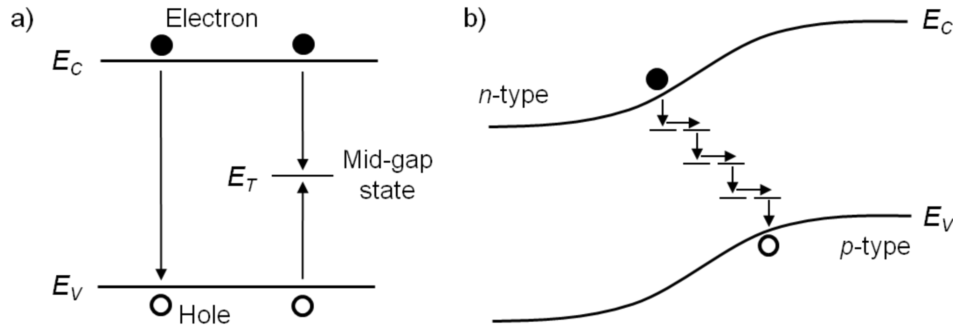

Fig 2.7: Schematic diagrams of some charge transport models, where E_T is the energy position of a mid-gap state: a) Recombination via band-to-band transitions or involving a mid-gap state, and b) multi-step tunnelling involving a number of localised states in the energy gap.

Possible recombination mechanisms include band-to-band recombination and trap-assisted Shockley-Read-Hall recombination[23, 24], as shown in Fig 2.7a. The latter process, involving the capture of both an electron and a hole at a trap state, is statistically most probable for traps situated in the middle of the band gap, i.e. at $E_T = E_g/2$, and in this case the value of n is 2. Therefore, physically n should always be between 1 and 2, and its value may be used to identify the extent to which charge transport in the depletion region is dominated by diffusion or recombination. By measuring a dark J-V curve, n may be determined from the slope of ln$J$ vs. V by approximating Equation 2.4 to be;

$$J = J_0\left(e^{qV/nkT} - 1\right) \approx J_0 e^{qV/nkT} \tag{2.12}$$

and assuming R_S and R_{SH} are negligible, this only being valid for a small section of the curve (typically for $0 \leq V \leq V_{OC}$). For a review of other methods of determining n, the reader is referred to Ref. 21. The intercept of ln$J$ vs. V is equal to ln(J_0) and for diffusion and recombination mechanisms J_0 is dependent on temperature according to;

$$J_0 = J_{00} e^{\Delta E/nkT} \tag{2.13}$$

where J_{00} is a constant and ΔE is the activation energy.

2.3.4.2 Multi-step tunnelling. Provided there is a sufficient distribution of traps throughout the band-gap, electrons may transport from the conduction band of the n-type material to the valence band of the p-type material via a number of steps in a staircase fashion: First electrons recombine with holes into states of lower energy, and then they tunnel into neighbouring states of equal energy, the process repeating until the electron recombines with a

hole in the valence band, as shown in Fig 2.7b. The dark *J-V* relationship of this mechanism is modelled by the following[25];

$$J = J_0 e^{AV} \tag{2.14}$$

where *A* is equal to the slope of ln*J* vs. *V*. There is no physical meaning to *n* for multi-step tunnelling, but its value (equal to *q/AkT*) can be used to identify a tunnelling mechanism: Since *A* is considered to be roughly independent of *T*, the multi-step tunnelling mechanism is inferred from an increase in *n* as *T* is reduced. The dependence of J_0 on *T* for tunnelling is given by;

$$J_0 = J_{00} e^{BT} \tag{2.15}$$

where *B* is a constant, this *T*-dependence differing to that of diffusion/recombination (Equation 2.13). *J-V-T* measurements are therefore highly useful for identifying which mechanisms operate in a device. The number of steps, *R*, involved in the tunnelling mechanism may be calculated from *A*, using the following equation (the approximation on the right hand side being for the case where $N_D >> N_A$)[26];

$$R = \frac{m_n \varepsilon_p}{N_A}\left(\frac{\pi}{4\hbar A}\right)^2 \left(1 + \frac{\varepsilon_p N_A}{\varepsilon_n N_D}\right)^2 \approx \frac{m_n \varepsilon_p}{N_A}\left(\frac{\pi}{4\hbar A}\right)^2 \tag{2.16}$$

where m_n is the electron effective mass, and $\hbar$ is the reduced Planck's constant.

2.4 Solar cell technologies

2.4.1 1st generation – Silicon wafer

Si has a band gap of 1.1 eV, which is well matched to the AM1.5 spectrum, but as it is an indirect-gap material its absorption coefficient is low and wafers approximately 300 – 500 μm thick are required to absorb light sufficiently[4]. As a result, long minority carrier diffusion lengths are required and therefore mono-crystalline wafers of high-purity should ideally be used. Mono-Si wafers are typically grown either by the 'Czochralski' or 'float zone' methods, during which they are *p*-doped with B. The junction is completed by diffusing an *n*-type dopant, most usually in the form of P. As yet, the best obtained efficiency is 25.0%[14]. Research has recently focused on light trapping techniques so that thinner wafers can be used, and on varying the contact morphology to limit shadowing. The main limitation of the technology is the cost of purification. Poly-Si devices are inevitably cheaper to manufacture,

but the increased recombination associated with the presence of grain boundaries reduces efficiency.

2.4.2 2nd generation – Thin-film

PV devices based on direct band gap materials may be constructed from films just a few microns thick due to their high absorption coefficients. The reduced material usage makes thin-film devices highly attractive in terms of their lower cost relative to Si. CdTe is currently the leading thin-film technology industrially, with First Solar being the world's largest PV manufacturer in 2009[27] and recently boasting record module efficiencies of 16.1% and laboratory-scale efficiencies of 18.7%[28]. Other successful thin-film technologies at the laboratory scale are copper indium gallium diselenide (CIGS) and amorphous-Si (a direct-gap phase of Si with a higher absorption coefficient than its crystalline counterpart), with their peak efficiencies currently at 19.6% and 10.1% respectively[14]. Recently, more effort has been made to develop thin film technologies based on cheap, abundant elements, such as copper zinc tin sulphide[29] (CZTS) or FeS_2.[30]

Although 'thin-film' is typically reserved to describe polycrystalline materials, epitaxial mono-crystalline GaAs devices also use absorber layers just a few microns thick, with efficiencies of 28.8% having been obtained. High purity GaAs is much more costly than Si[4].

2.4.3 3rd generation

3rd generation PV technologies are usually defined as those for which theoretically the Shockley-Queisser limit may be exceeded[31]. This includes multi-junction solar cells (whereby the band-gap of sections of the device is varied either by chemical content or quantum confinement effects) and hot carrier solar cells (whereby the usual energy loss associated with hot carrier relaxation via thermalisation is overcome by effective hot carrier collection). Solar cells that incorporate NWs (reviewed in Chapter 3) simply to reduce recombination loss or enhance light trapping may not exceed the Shockley-Queisser limit and should be considered as 2nd generation, whereas if the NWs exhibit hot carrier or confinement properties the cells may considered to be 3rd generation.

Dye sensitised solar cells and organic PV are sometimes referred to as 3rd generation, but as above this should only be the case for device configurations that can exceed the Shockley-Queisser limit. This has not yet been achieved for these technologies, although hot carrier extraction may be realised in dye sensitised cells via sub-picosecond charge-transfer processes[32].

2.5 CdTe device characteristics

2.5.1 CdTe material properties

2.5.1.1 Notable properties. CdTe is a direct band gap semiconductor with a high optical absorption coefficient (> 5×10^5 cm^{-1})[33] and its optical band gap of E_g = 1.45 eV at room temperature is well matched to the AM1.5 spectrum[34]. It usually adopts the zinc-blende form and only very rarely the wurtzite lattice type[35]. A representation of the zinc-blende crystal structure for CdTe (with lattice constant, *a*) is shown in Fig 2.8. This structure is formed by two intersecting face centred cubic sub-lattices (one for the Cd atoms and one for the Te atoms in this case), with one shifted ¼ of a unit cell along the <111> direction from the other (the co-ordinate system is shown in Fig 2.8). The structure has a stacking sequence AαBβCγAαBβCγ in the <111> direction, with A, B and C referring to lattice points of the Cd sub-lattice, and α, β and γ to the Te sub-lattice. The Cd-Te bond is highly polar, resulting in differing thermodynamic properties between the Cd-terminated (111)A planes and Te-terminated ($\bar{1}\bar{1}\bar{1}$)B planes, and strong coupling between electrons and the lattice. Like other zinc-blende semiconductors however, its optical properties are isotropic. CdTe is highly prone to twinning, particularly along {111} planes, owing to its low stacking fault energy of 9 - 10.1 mJ.m^{-2}.[36, 37]

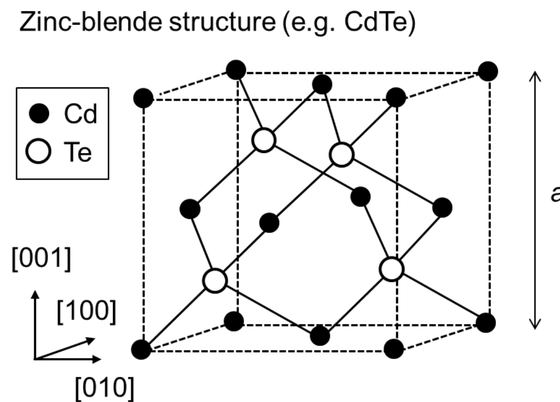

Fig 2.8: Unit cell of the cubic zinc-blende crystal structure. CdTe typically adopts this structure. The dashed lines define the unit cell boundaries and the solid lines represent Cd-Te bonds.

2.5.1.2 Doping. The conductivity type of CdTe is largely dependent on the concentration of Cd and Te vacancies and Te_{Cd} antisite donors, the Cd vacancy (V_{Cd}^{2-}) being a double acceptor and the Te vacancy (V_{Te}^{2+}) being a double donor. As-grown CdTe can be made strongly *n*-type but only weakly *p*-type due to compensation mechanisms associated with these defects[38]. Extrinsic substitutional dopants may be introduced, with acceptors being

selected from groups I and V (e.g. Au or As) and donors from groups III and VII (e.g. In or I). In this sense, Cl may be considered to be an *n*-type dopant in CdTe, but is universally used as a *p*-type dopant since it forms a single acceptor complex (V_{Cd}^{2-}-Cl_{Te}^{+}, called the *A*-centre) with the double acceptor V_{Cd}^{2-}.[39] Oxygen is thought to be an iso-electronic acceptor. Unintentional doping is also a consideration for solar grade CdTe[40] (99.999% pure), with typical impurities including Cu, Na, Li and Ag[41]. These detrimental impurities form levels in the band gap that may act as traps and recombination centres.

2.5.2 CdTe/CdS superstrate device configuration

The most common design for CdTe devices is that of the 'superstrate' configuration, shown in Fig 2.9, whereby a transparent front contact is first deposited onto a glass superstrate, followed by an *n*-type CdS window layer, a *p*-type CdTe absorbing layer, and a metallic back contact. The device is illuminated from the glass side. Features of each of the layers are now discussed.

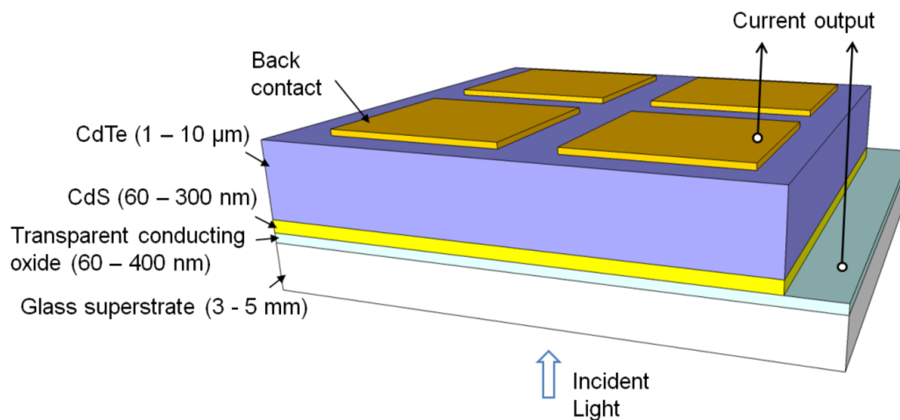

Fig 2.9: Structure of a typical research CdTe/CdS solar cell in the *superstrate* configuration.

2.5.2.1 Glass. The superstrate must be able to withstand temperatures at which subsequent film deposition and annealing stages are carried out and of course must be transparent to wavelengths that exist in the active region of the device. Whilst flexible, lightweight superstrates such as polyimide are attractive, they are less resistant to high temperatures than glass. Soda-lime glass is commercially the most common glass used since it is cheap, whereas fewer impurities exist in borosilicate glass.

2.5.2.2 Transparent front contact. The most common materials to be used for front contacts to solar cells are transparent conducting oxides (TCOs), such as SnO_2, Sn-doped In_2O_3 (ITO), Fl-doped SnO_2 (FTO) and Al-doped ZnO.[42] These materials have high transparency in the active region of the device (i.e. a wide band-gap) and low sheet resistance (< 10Ω/□). The high conductivities are due to degenerate doping, i.e. the Fermi level is above

the conduction band edge, which results in the material having a permanent population of carriers whilst maintaining a wide optical band gap. In this thesis ~ 200 nm thick ITO films were used as front contacts, ITO having been reported to have sheet resistances as low-as 2Ω/□ and an effective direct band gap of ~ 4 eV.[43] Moreover, ITO is *n*-type and may therefore form an Ohmic contact with the *n*-type CdS layer.

2.5.2.3 n-type CdS window layer. The CdS layer is typically highly *n*-type ($n \sim 10^{17}$ - 10^{19} cm^{-3}) as-grown and therefore the junction is one sided and located in the CdTe. Consequently, all carriers generated in the CdS are considered to be lost via recombination. However, since CdS has a much wider band gap (~ 2.4 eV)[44] than CdTe, it allows a significant proportion of the spectrum ($\lambda > 500$ nm) to pass, hence the term window layer. To further enhance transmission into the absorber layer the CdS layer may be grown very thin, i.e. < 80 nm, but problems can arise if the CdS is *too* thin as the presence of CdS pinholes can lead to the formation of weak CdTe/ITO diodes which are detrimental to V_{OC}.[45] To reduce window layer absorption loss, Cd(*x*)Zn(1-*x*)S can be used instead (where *x* is ~ 0.1) since it has a wider band gap than CdS, defined by Vegard's law[46]. Similarly, CdS grown in the presence of O_2 often exhibits a wider band gap, and this is attributed to quantum confinement effects associated with the nanocrystalline grain structure of CdS:O.[47] Since the electron affinity of CdS is comparable to that of CdTe, spikes in the conduction bands at the CdS/CdTe interface are small ($\Delta E_C \sim 0.2$ eV)[48]. Polycrystalline (wurtzite) CdS can be deposited by close-space sublimation (CSS), metal organic chemical vapour deposition (MOCVD), sputtering or chemical bath deposition (CBD), the latter two techniques providing excellent thickness uniformity.

A representation of the hexagonal wurtzite crystal structure (with lattice constants *c* and *a*) which CdS typically adopts, is shown in Fig 2.10. The structure consists of two overlapping close-packed hexagonal sub-lattices, one for the Cd atoms and one for the S atoms. Note that for description of hexagonal crystal structures, the four index labelling system is commonly used, i.e. ($h\ k\ i\ l$) where $i = -(h + k)$. The structure is highly polar in the [0001] direction (the *c*-axis), in which the stacking sequence is AαBβAαBβ, with A and B referring to lattice points of the Cd sub-lattice, and α and β to the Te sub-lattice. The (0001) plane has six-fold symmetry, and the co-ordinate system projected onto this plane, including the $(10\bar{1}0)$, $(01\bar{1}0)$ and $(1\bar{1}00)$ directions, is shown in Fig 2.10.

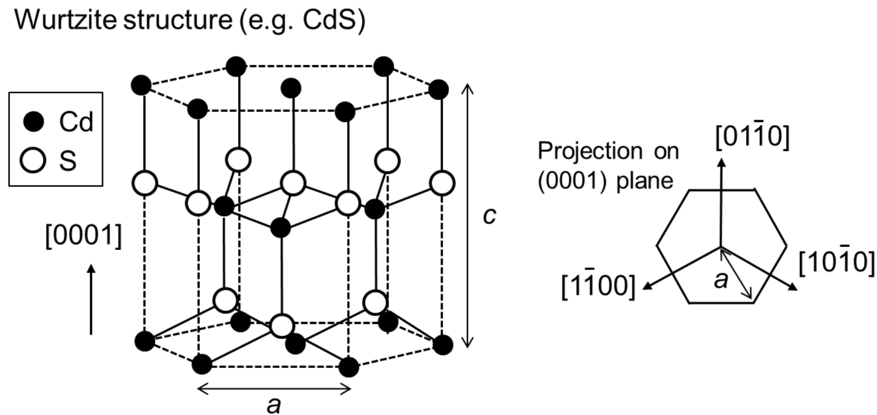

Fig 2.10: Unit cell of the hexagonal wurtzite crystal structure. CdS typically adopts this structure. The dashed lines define the unit cell boundaries and the solid lines represent Cd-S bonds. To the right is a projection of the (0001) plane showing the co-ordinate system used.

At the CdTe/CdS interface, there is a lattice mismatch of ~ 10% which leads to recombination (see Section 3.4.2). This may be alleviated by the formation of a thin alloy layer of $CdS_{1-x}Te_x$ upon inter-diffusion[49] of S and Te, which may be expected to increase V_{OC} and *FF*. Inter-diffusion may occur during subsequent high-temperature CdTe deposition, or post-growth annealing treatments[50]. On the other hand, since Te incorporation into CdS reduces the CdS band-gap[50], increased inter-diffusion can increase CdS absorption and consequently reduce J_{SC}.

2.5.2.4 p-type CdTe absorbing layer. Whilst 99.9% of above band-gap light can be absorbed by less than 2 μm of CdTe, it is common to use layers ~ 2 – 10 μm thick to reduce the incidence of pinholes and shunting pathways. Polycrystalline CdTe layers can be deposited by CSS[51], sputtering[52], electro-deposition[53], or MOCVD[46]. The grain size and grain boundary density in the films are considered to be highly influential on device performance[54] since grain boundaries are thought to increase: a) recombination due to impurity segregation; b) series resistance due to potential barriers created by upward band bending at the boundary[55]; and c) shunting. The *p*-type doping densities of as-grown CdTe are usually insufficient to yield high-efficiency devices, and it is common to dope with Cl, either by deposition of $CdCl_2$, or in some cases CuCl. Doping of the CdTe layer must be: a) sufficiently high so to ensure high V_{OC} and low R_S; and b) sufficiently uniform so to prevent the formation of homo-junctions within the layer.

An energy band diagram for a typical CdTe solar cell is shown in Fig 2.11, along with carrier density profiles of electrons, *n*, and holes, *p*. The data was generated using SCAPS having assumed an Ohmic back contact between the metal and CdTe and layer thicknesses of

2 μm for the CdTe and 200 nm for the CdS. A small conduction band offset is present at the CdS/CdTe interface.

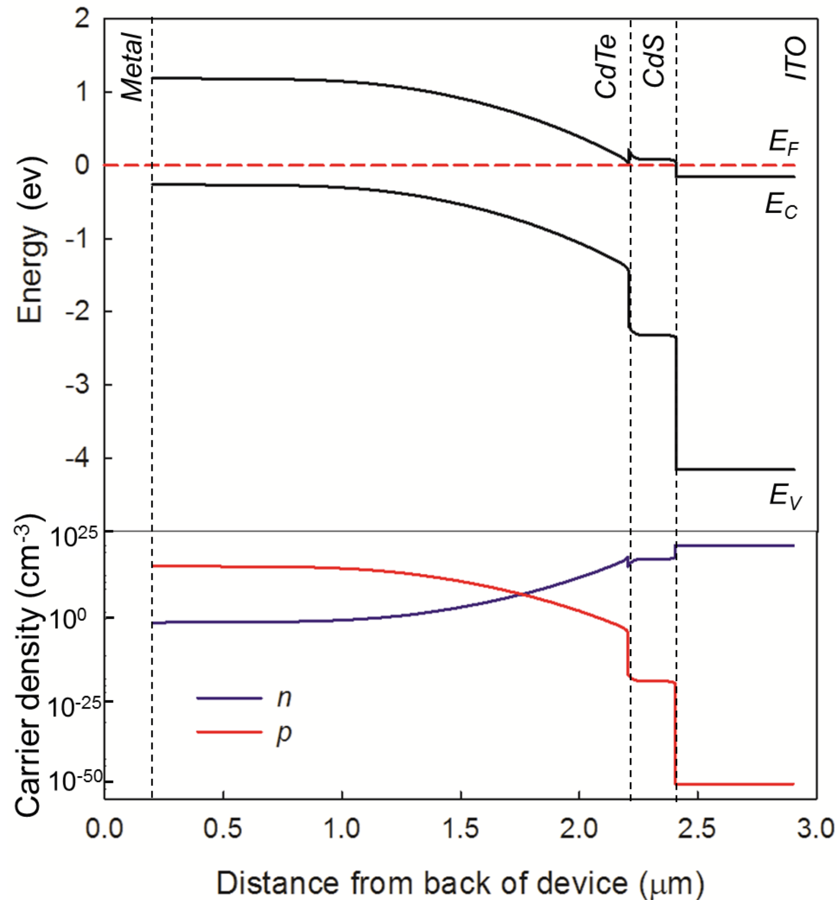

Fig 2.11: Top: Energy band diagram of a metal/CdTe/CdS/ITO solar cell assuming an Ohmic contact at the metal/CdTe interface. Bottom: Carrier density profiles (for electrons, *n*, and holes, *p*) through the device. The data was generated using SCAPS[19].

2.5.2.5 Back contact. As *p*-CdTe has a work function (ψ > 5.7 eV) that is higher than most metals, owing to its high electron affinity (E_{ea} ~ 4.4 eV)[33], a particular challenge of CdTe device fabrication is the successful formation of an Ohmic back contact. Au is one of the more promising metal contacts to be used, but its work function, reported in the range 4.8 – 5.4 eV, remains insufficient.[56, 57]

A Schottky back contact to a PV device results in band-bending in the opposite direction to the main junction, as shown in Fig 2.12a, provided the two depletion regions do not overlap[58]. The effect of this on the *J-V* response is to cause 'rollover' in forward bias, increasing the R_S and reducing *FF*, as shown in Fig 2.12b. In order to achieve a quasi-Ohmic contact to CdTe, the back surface can be made highly *p*-type, which has the effect of making the barrier thinner and encouraging tunnelling. This is achieved either by generating a Te-rich

layer at the back surface prior to contacting - by etching out the Cd with nitric-phosphoric acid[59] or bromine-methanol solution[60] - or by p^+ doping with Cu-containing materials. The incorporation of Cu into CdTe solar cells can lead to performance degradation over time however[61].

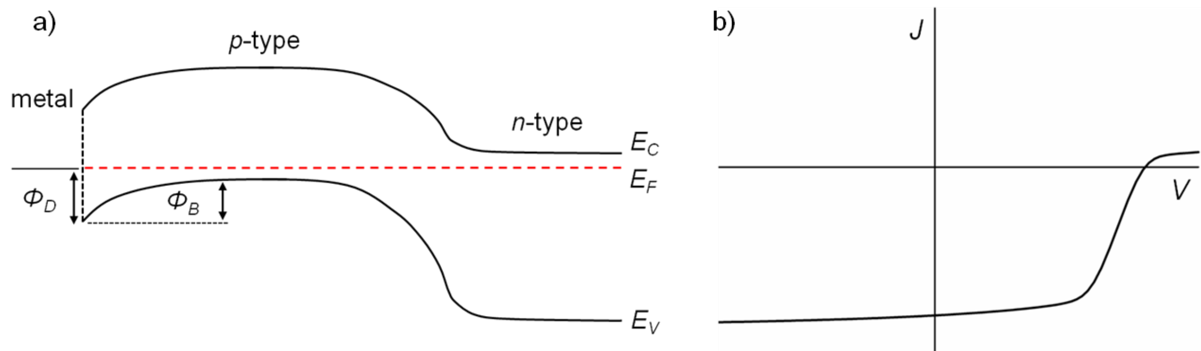

Fig 2.12: a) Energy band diagram of a hetero-junction solar cell with a Schottky back contact. b) 'Rollover' effect that the poor back contact has on the *J-V* curve.

2.5.2.6 $CdCl_2$ doping. It has been universally found that the performance of as-grown CdTe solar cells is significantly enhanced upon post-growth treatment with Cl. It is thought to have a number of effects, these being: a) *p*-type doping of the CdTe layer[62]; b) promotion of grain growth[63, 64] and recrystallisation (both in CdS[65] and CdTe[64] layers), resulting in the as-desired reduction in grain boundary density; and c) increased inter-diffusion of S and Te at the CdTe/CdS interface[62, 64], resulting in passivation of surface defects. These effects lead to increases in V_{OC} and *FF*.[65] Cl-activation can be achieved either by deposition of $CdCl_2$ (by evaporation[66] or by solution dipping[67]) onto the CdTe back surface and subsequent annealing in air, or in-situ by depositing CdTe in the presence of Cl-containing gases[68]. Some of the beneficial effects induced by Cl-activation, such as grain growth and recrystallisation, can be achieved to some extent simply by annealing in air at temperatures exceeding ~ 450°C[69].

2.5.2.7 High-resistive transparent layer. In some cases, a thin (~ 50 nm) highly resistive transparent (HRT) layer is placed between the CdS and TCO. Such a layer is thought to reduce the detrimental impact of CdS pinholes by preventing the formation of weak TCO/CdTe diodes. As a result, the CdS layer may be grown thinner whilst maintaining high V_{OC}. This HRT layer may also limit diffusion of unwanted impurities from the glass or TCO to the junction region[70]. Materials used for HRT layers in CdTe solar cells include ZnO[71], Zn_2SnO_4[72] and SnO_2[73].

2.5.3 High efficiency CdTe/CdS devices

In the early 90s, the University of South Florida reported a series of significant enhancements to the world-record CdTe device efficiency, peaking at 15.8% in 1993.[74] A key aspect of these devices was the optimisation of the inter-diffusion at the CdTe/CdS interface by varying the CdTe deposition temperature. Significant improvements to this were not realised until 2004, with Wu reporting a 16.5% efficiency device[75]. Wu used a $CdSnO_4$ TCO which demonstrated very low electrical resistivity (~ 1.5×10^{-4} Ω.cm), a Zn_2SnO_4 HRT layer and an oxygenated CdS window layer with a wider band-gap (2.5 – 3.1 eV) than CdS to improve transmission into the CdTe. Wu also commented on the importance of optimising the inter-diffusion. A series of advances have been made in recent years however: First Solar reported a 17.3% device in 2011[76], and General Electric reported 18.3% earlier this year. Then, First Solar reached 18.7%[28] and General Electric broke the record again with 19.6%[77]. The exact experimental details for fabrication of these recent standout devices have not been reported, but the quantum efficiency curves demonstrate enhanced short wavelength responses which indicates very high transmittance through the window layer[14]. Additionally, the world record device has a *FF* as high as 80%, a significant gain over that recorded by Wu (75%), presumably owing to enhancements to TCO conductivity.

2.5.4 The future of CdTe solar cell research

With reported J_{SC} values approaching the theoretical limit for CdTe devices, the performance parameter identified for improvement is that of V_{OC}, the highest reported (857 mV) is significantly lower than the optical band gap. The present limitation to V_{OC} is thought to lie in the inability to achieve sufficiently high *p*-type carrier densities in the CdTe layer, presumably due to self-compensation. Focus should be directed towards generating a deeper fundamental understanding of point defects and doping in CdTe.

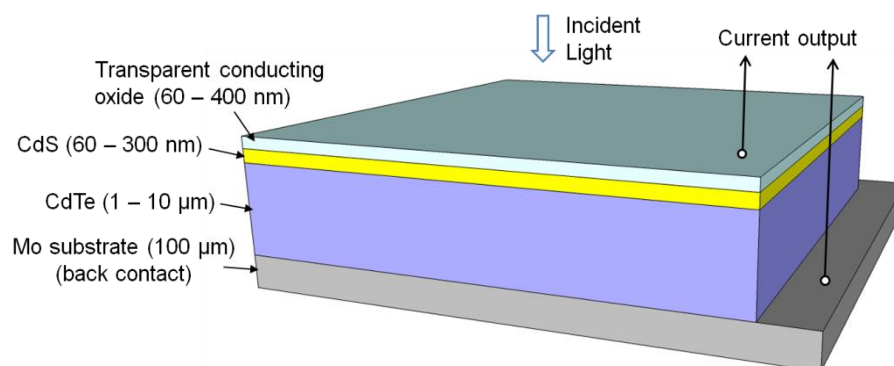

Fig 2.13: Structure of a typical CdTe/CdS solar cell in the *substrate* configuration.

Alternative device designs are under investigation, especially the ‘substrate configuration’ on metal foils, as shown in Fig 2.13. The substrate configuration offers two significant advantages: a) The stages of CdTe doping and CdTe/CdS junction formation may be optimised independently; and b) the replacement of heavy glass superstrates with lightweight, low cost, flexible metal substrates may reduce manufacture, transport and installation costs and enable roll-to-roll cell production. However, the formation of an Ohmic back contact – in this case between the CdTe and metal substrate – has thus far proved more challenging than for superstrate devices. This is because the selected substrate should ideally have a thermal expansion coefficient matching that of CdTe so that delamination and film cracking does not occur and the most suitable metal in this regard, Mo, has a low work function (4.36 – 4.95 eV)[78] relative to CdTe. Consequently the performance of substrate devices lags somewhat behind those of superstrate cells, the best efficiencies[79-85] having been achieved through inclusion of a buffer layer between the Mo back contact and CdTe in order to achieve a quasi-Ohmic contact, as listed in Table 2.1. Note that the 13.6 % Kranz[79], 11.3 % Gretener[80] and 11.0 % Dhere[81] devices were grown on Mo/glass substrates and therefore cannot be considered to be truly flexible (or lightweight). In this regard, the standout device is Kranz’s 11.5 % device on Mo foil. Kranz emphasised the importance of controlling Cu-doping of the CdTe layer on the device performance.

Table 2.1: Efficiency of CdTe devices grown in substrate configuration on Mo substrates. The ‘buffer layer’ referred to is situated between Mo and CdTe for all devices.

Reference	***Best Efficiency***	***Comments***
Kranz *et al.*, 2013 [79]	a. 13.6 % (Mo/glass substrate) b. 11.5 % (Mo foil substrate)	Te/MoO_3 buffer layer + Cu doping
Gretener *et al.*, 2012 [80]	11.3 % (Mo/glass substrate)	Cu/Te/MoO_3 buffer layer
Dhere *et al.*, 2012 [81]	11.0 % (Mo/glass substrate)	Cu_xTe buffer layer
Matulionis *et al.*, 2001 [82]	7.8 %	ZnTe:N buffer layer
Drayton *et al.*, 2005 [83]	6.5 %	RF sputtered CdTe + unnamed buffer
Hodges *et al.*, 2009 [84]	6.0 %	ZnTe buffer layer
Singh *et al.*, 2003 [85]	6.0 %	CuTe buffer layer

In the coming years, substrate based devices should be the focus of significant research in order to reduce the cost of CdTe PV and widen the scope for their implementation. The growth of devices directly onto metal substrates enables them to be integrated onto vehicle panelling for instance. The development of substrate CdTe devices on Mo foils is therefore

investigated in this thesis along with optimisation of the fabrication procedure, this work being presented in Sections 7.2 and 7.3. It is demonstrated that competitive efficiencies (> 11 %) may be achievable for these devices in this laboratory. The main goal of this investigation however was to set a baseline to which the more novel device designs – those based on CdTe NW structures that serve as the primary focus of this thesis (see below) – may be compared. This was necessary since the NW devices were also designed in the substrate configuration as opposed to the more familiar superstrate configuration (to ensure that the core section of the core-shell structures was the CdTe absorber layer).

Indeed, the use of novel designs for CdTe devices, such as the NW device described in Chapter 1, may yield performance enhancements that are not achievable using the traditional planar design and so the development of such devices should play a key part of future CdTe research. The advantages of using NWs in solar cells are described in detail in Chapter 3 but the key points are summarised as follows: a) a textured absorber layer may yield light trapping and anti-reflective effects that enable lower volumes of absorbing material to be used; b) core-shell radial *p-n* junctions may be more efficient than the planar counterparts in collecting minority carriers and so diffusion losses to J_{SC} and V_{OC} may be limited; and c) NWs grown by bottom-up methods typically are of high crystal quality. However, current research towards NW PV is in its infancy (particularly in the case of CdTe) and therefore significant work should be done to develop the growth procedures of CdTe nanostructures, to characterise their physical properties so that the feasibility of using them in PV devices can be determined, and to demonstrate that working devices can be made to serve as a proof of concept. Accordingly, these issues are the main focus of this thesis.

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Chapter 3 : Semiconductor nanowires and their use in photovoltaics

3.1 Introduction

In this Chapter, the growth and physical properties of semiconductor nanowires (NWs) and their use in photovoltaic (PV) devices is reviewed. It is considered necessary to review these topics given the investigations documented in this thesis; NW growth and characterisation in Chapters 5 and 6 respectively, and NW solar cell development in Chapter 7. Generally, a nanowire may be defined as a structure with a diameter at the nano-scale, but having an unconstrained length. Three diameter-scales are relevant: a) A *quantum* wire has a diameter, D, comparable to the given material's exciton Bohr radius (typically a few nms) and therefore experiences quantum confinement in two dimensions; b) a *nano*wire has a diameter of tens or hundreds of nms (i.e. 10 nm $< D <$ 1 μm); and c) a *micro*wire with 1 μm $< D <$ 10 μm.

All have been researched for their use in opto-electronic devices[1-10] since some of their physical properties differ to those of bulk materials, and their morphology opens up a wide array of device designs. Most obviously, quantum confinement effects may be realised in quantum wires, but even for nanowires and microwires, the light trapping properties, mobility enhancements and surface effects associated with these structures present significant opportunities. Work presented in this thesis involves the use of wire structures with $D \sim 50$ – 500 nm therefore the majority of this Chapter focuses on *nano*wires as defined above.

First, in Section 3.2, methods of fabricating semiconductor NWs are presented, with particular focus on the vapour-liquid-solid mechanism. Methods of incorporating NWs into solar cells are described in Section 3.3, the use of NWs having the potential to yield enhancements at every stage of solar cell operation – i.e. light absorption and carrier generation, separation and collection[2]. The challenges faced in developing these devices are discussed in Section 3.4 and literature reviews of CdTe NW growth and NW solar cell fabrication are given in Sections 3.5 and 3.6 respectively. This review is necessarily selective and for more extensive reviews the reader is referred to Refs 11-13.

3.2 Nanowire fabrication methods and growth features

3.2.1 Top-down vs. bottom-up approaches

The experimental methods used to fabricate NWs can largely be divided into two categories, 'top-down' methods and 'bottom-up' methods. Top-down methods involve etching structures from a larger piece of material in a subtractive fashion[14] via optical[15] or electron-beam lithography[16], selective etching[17] or focussed ion beam (FIB) milling[18]. Bottom-up methods describe those whereby NWs are grown additively from their subcomponents, examples being metal-catalysed NW growth (see Sections 3.22 - 3.25), the self-assembly of NWs from nanoparticles[19], or the patterned growth of NWs within prior defined membranes[20, 21].

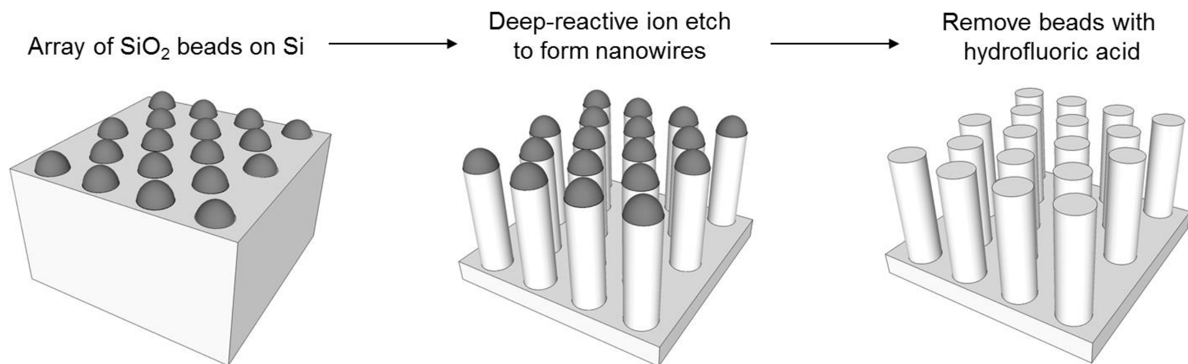

Fig 3.1: Schematic of one 'top-down' approach of forming a Si nanowire array, see text.

A top-down process is shown in Fig 3.1, reported by Garnett *et al*.[22] Here, a Si wafer is dip-coated in a solution of SiO_2 beads (a few hundred nms in diameter), which self-assemble into a hexagonal array at the surface. This self-assembly process gives the highest packing density, i.e. the hexagonal structure[23]. In this structure, the nearest neighbour distances are all equal, defined by a balance between attractive (e.g. van der Waals) and repulsive forces. This patterned structure is then selectively reactive ion etched to define the NW array. The bead diameter and etch time control the NW diameter and length respectively. Hydrofluoric acid is then used to remove the beads from the NW tips.

Alternative top-down methods such as FIB milling may be slower[24] but offer different levels of control. All top-down methods are limited by the fact that the resulting material quality of the final structure is only as good as the original material, whereas bottom-up grown NWs may have superior material quality (see Section 3.3.3). In this work, the bottom-up vapour-liquid-solid mechanism was used for NW growth, and this is discussed in the next section.

3.2.2 Vapour-liquid-solid mechanism

In 1964, Wagner and Ellis[25] demonstrated the growth of Si 'whiskers' upon vapour deposition of Si onto a Au droplet covered Si substrate. It was observed that each whisker (or indeed each NW) had a Au droplet at its tip following growth and its diameter (as small as ~ 100 nm) was equal to that of its droplet. They explained that this selective, highly directional seeded-growth was governed by the vapour-liquid-solid (VLS) mechanism - having a *solid* substrate and eventual NW, a *liquid* droplet acting as a growth catalyst, and a *vapour* flux providing the growth material. This method is now in widespread use for NW growth.

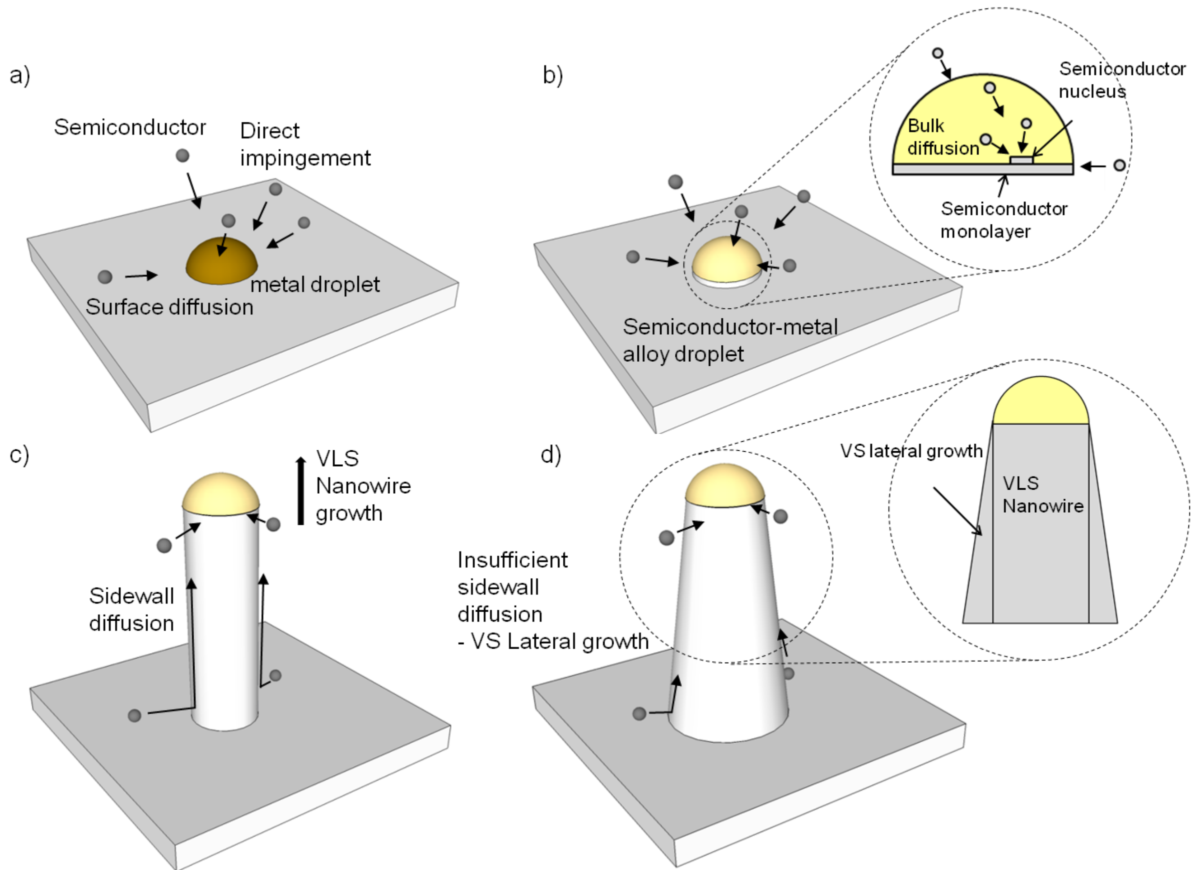

Fig 3.2: Stages of VLS growth: a) Semiconductor deposition onto substrate coated with metal nano-droplets and incorporation of semiconductor into droplets, b) formation of semiconductor-metal liquid alloy, its subsequent saturation, and precipitation of semiconductor to initiate VLS growth (inset: diffusion of material through droplet), c) continued VLS growth. d) If material impinges on sidewalls, VS lateral growth occurs.

3.2.2.1. Basic VLS processes. The main stages of VLS growth of a NW are shown in Fig 3.2a – c and now described in the context of the Au-Si system. A Au droplet (or catalyst) lies on a Si substrate which is heated to a temperature exceeding the Au-Si eutectic temperature (363°C)[26] so that a liquid Au-Si alloy may form. A flux of Si vapour is then directed towards the substrate and adatoms arrive at the droplet either by: a) direct impingement; or b) surface

diffusion following arrival at the bare substrate (Fig 3.2a). The droplet is a preferred site for incorporation since it has a larger accommodation coefficient than the bare substrate as it consists of many atomic steps[27]. The droplet becomes saturated and Si precipitates out at the interface between the droplet and substrate, i.e. the liquid/solid interface (Fig 3.2b), initiating NW growth. Diffusivity of Si through the droplet to the liquid/solid interface is high since the droplet is liquid, and NW growth proceeds at this interface in a layer-by-layer fashion (Fig 3.2b inset), lifting the Au-Si droplet upwards so that it always remains at the NW tip. This process continues upon continued exposure to Si vapour (Fig 3.2c), and since the growth front is at the liquid-solid interface, the NW diameter is equal to that of the interface.

3.2.2.2 Lateral growth. In some cases, at later stages of NW growth, adatoms arriving on the substrate or on the NW sidewalls may be incorporated onto the sidewalls via a standard vapour-solid (VS) growth mechanism, this occurring once the NW length exceeds surface diffusion lengths and adatoms are no longer able to reach the droplet. As a result, the diameter of the NW becomes greater than that of the liquid/solid interface, particular towards the base of the NW[28].

3.2.2.3. 'Nanowire root' and 'cooling neck'. Whilst the schematic in Fig 3.2c shows a NW with a constant radius from substrate to droplet, VLS-grown NWs often have a shape like that shown in Fig 3.3a, with a tapered base (even in the case of no lateral growth) and tip, owing to the non-steady state mechanics at the initial and final stages of growth. An example of the tapered base, or 'root', is shown in the inset of Fig 3.3a[29]. (This is the standard case, for a discussion of other NW shapes achieved by VLS growth, the reader is referred to Ref. [30]). The root and neck features are now described.

Before NW growth initiates, the droplet may be modelled as a spherical cap (Fig 3.3b) with a contact angle, θ, defined by Young's equation[31]:

$$\gamma_{SV} = \gamma_{LV} \cos\theta + \gamma_{SL} \tag{3.1}$$

where γ_{SV}, γ_{SL} and γ_{LV} are the substrate-vapour, substrate-liquid and liquid-vapour surface energies respectively. However, as reported by Schmidt *et al.*[29, 32], this contact angle changes during the initial phase of NW growth (Fig 3.3c) to account for the presence of the NW sidewall and is expressed as;

$$\gamma_{LV} \cos\theta = \gamma_{WV} \cos\alpha - \gamma_{SL} \tag{3.2}$$

where γ_{WV} is the sidewall-vapour surface energy and α is the angle of inclination of the NW flank, equal to 0° prior to NW growth and then increasing to 90° for steady-state NW growth.

As α increases during this initial stage, θ increases, resulting in a reduction of the liquid-solid interfacial area and a tapering of the NW until equilibrium and steady-state growth is reached. Note that for droplets with a diameter of just a few nm's, a line tension term is included in Equations 3.1 and 3.2, its magnitude influencing the extent of the root[29]. For instance a large line tension results in a large amount of tapering. Line tension is ignored for larger droplets, but a root should still exist.

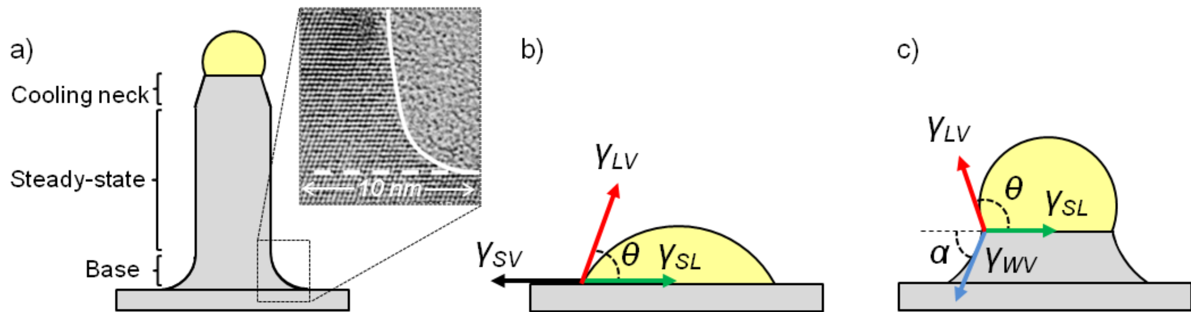

Fig 3.3: a) Typical NW shape including a tapered base, or 'root', and tapered cooling neck (inset: image taken from Ref. 29. b) and c) development of droplet and wire shape in the initial phases of NW growth, resulting in the formation of NW root.

Steady-state VLS NW growth ceases when vapour deposition is terminated, where upon the liquid droplet is saturated with residual semiconductor material (Fig 3.4a). Upon cooling, the solubility is reduced, and this residual material begins to precipitate out at the liquid-solid interface. This reduces the volume of the droplet and the liquid-solid interfacial area so the final stage of growth is tapered[33], as shown in Fig 3.4b. (The contact angle between the droplet and NW will also change as the droplet composition changes). After cool-down there is therefore a 'cooling neck' and only traces of semiconductor remain in the droplet (Fig 3.4c).

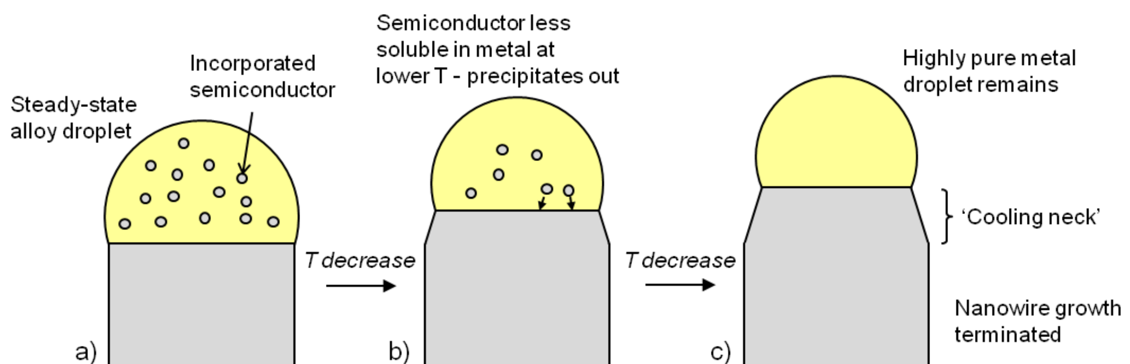

Fig 3.4: Formation of a 'cooling neck' and purification of the droplet upon cool-down, see text.

3.2.2.3. Material requirements for VLS growth. Firstly, the minimum requirement for VLS growth is for the droplet to be a liquid alloy at the growth temperature, this being dependent on the temperature-composition phase diagram of the materials. For Au-catalysed Si NW growth on a Si wafer supersaturation is achieved readily since both the substrate and the vapour contribute to the concentration of Si in the catalyst. In other cases however if the substrate and wire are of different materials there may be a longer nucleation delay while supersaturation is achieved from the vapour alone. In such a case (e.g. Au-catalysed growth of CdTe on Mo), the model describing the initial stages of NW growth is expected to be more complex.

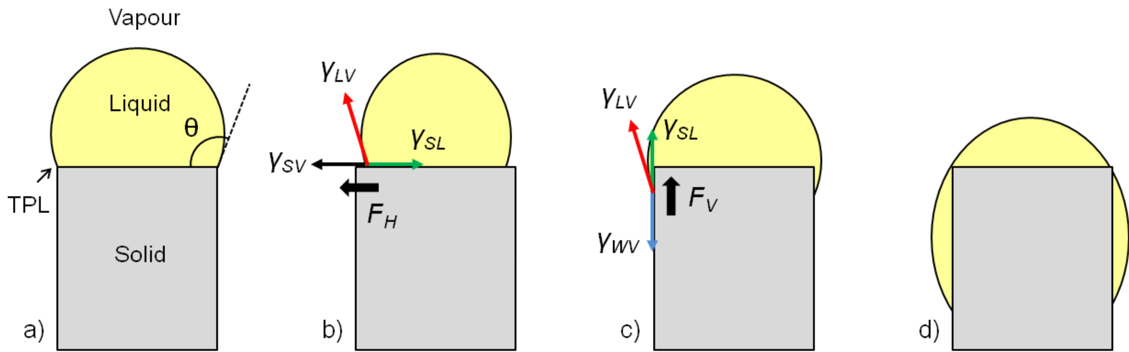

Fig 3.5: Droplet-NW interface for standard VLS growth involving surface energies in cases of a) steady state, b) horizontal droplet shift and c) vertical droplet shift. d) Non-standard VLS growth whereby droplet wets the nanowire sidewalls due to excessive vertical droplet shift[34].

Secondly, the droplet must be stable, this being determined by the balance of surface energies. In 'standard' steady-state NW growth the triple-phase line (TPL) between vapour, liquid and solid phases, as indicated in Fig 3.5a, is stable and is shifted upwards upon completion of each NW monolayer. Due to environmental perturbations however, the TPL can experience random shifts horizontally (Fig 3.5b) or vertically (Fig 3.5c) and a force is required in order to return the TPL to the steady-state position, this force being provided as long as certain surface energy inequalities are met[34]. In the horizontal case, a force, F_H, will return the TPL to its steady-state position provided

$$\gamma_{SV} > \gamma_{LV} \cos\theta + \gamma_{SL} \tag{3.3}$$

which is *always* the case if one considers the following: The left hand side of the inequality is equal to the right hand side (RHS) prior to NW growth according to the model of a spherical cap on a surface (Equation 3.1) and during NW growth the RHS becomes smaller since θ becomes greater (Fig 3.3b and c) – even more so in the case of a horizontal shift of the

droplet. In the vertical case, a force F_V, will return the TPL to its steady-state position provided

$$\gamma_{WV} < \gamma_{LV} \sin\theta + \gamma_{SL} \tag{3.4}$$

which is the same as the Nebol'sin—Shchetinin inequality for standard VLS growth[34, 35]. If Equation 3.4 is not satisfied, the droplet slides downwards and wets the sidewall resulting either in a modified mode of VLS growth[34] or droplet perforation and termination of NW growth. A separate phenomenon is that of droplet migration: Hannon *et al.*[36] observed that some droplets gradually migrated from one NW to a neighbouring NW, resulting in the diameter of some NW's decreasing over time and that of others increasing over time.

Further material properties desirable for VLS growth are: a) the solubility of the metal component in the liquid eutectic is greater than in the solid wire (i.e. the segregation coefficient for the metal component in the semiconductor, $k < 1$); and b) the vapour pressure of the metal component must be smaller than that of the liquid eutectic so that the droplet does not evaporate or shrink in volume.

3.2.2.4 Growth rate (length and diameter). In order to understand the relationships between NW length, l, radius, R, and growth time, t, during VLS growth, one should consider the possible adatom processes involved (see Fig 3.6), these being: 1) Direct adsorption on droplet surface; 2) desorption from droplet; 3) adsorption to sidewall and diffusion to droplet; 4) desorption from sidewall; 5) substrate-to-sidewall diffusion; 6) substrate-to-droplet diffusion via sidewall; and 7) nucleation on substrate.

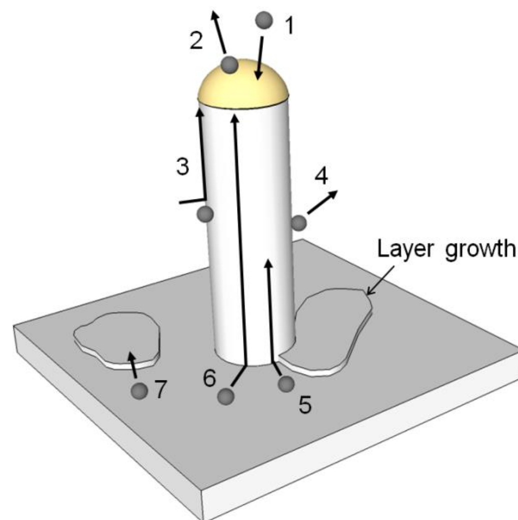

Fig 3.6: Possible adatom processes during VLS NW growth, modified from Ref. 37, see text.

For cases whereby the main contribution to NW growth is direct adsorption, NWs of greater diameter have greater elongation rates, dl/dt, owing to the increased adsorption

associated with the increased capture area. This is the assumption made by the Givargizov-Chernov[38] theory, which also takes into account the Gibbs-Thomson effect; since smaller particles have greater curvature they have a higher vapour pressure which opposes the adsorption of adatoms.

Alternatively, for cases whereby the main contributions to NW growth are those of adatoms diffusing to the droplet from the substrate and sidewalls, NWs of *smaller* diameter have greater elongation rates. For GaAs NWs, Dubrovskii demonstrated that the adsorption-induced regime occurs for $D < 50$ nm, and the diffusion-induced regime for D > 50 nm[39]. Indeed, Dubrovskii *et al.* have published a series of pioneering articles focussed on quantifying d*l*/d*t*, d*R*/d*t* and d*l*/d*R* for the case of diffusion-induced[40-42] NW growth and also for more general cases that take into account *all* the kinetic processes[43] indicated in Fig 3.6 as well as the Gibbs-Thomson effect[37, 39, 44]. For a diffusion-induced model[41], d*l*/d*t* is given by;

$$\frac{3\sqrt{3}R^2}{2\Omega}\frac{\mathrm{d}l}{\mathrm{d}t} = \frac{3\sqrt{3}R^2}{2}C_0 J_f - 6RD_f\left(\frac{\mathrm{d}n_a}{\mathrm{d}z}\right)_{z=l} \tag{3.5}$$

where C_0 is a coefficient accounting for the droplet shape, adsorption and desorption at the droplet and film growth on the substrate, J_f is the vapour deposition flux, Ω is the elementary volume in the NW, n_a is the adatom concentration on the sidewalls, z is the coordinate along the NW axis and D_f is the diffusion coefficient. With $n_a(z)$ obeying the form $D_f \mathrm{d}^2 n_a(z))/\mathrm{d}z^2 + \chi J_f - n_a(z)/\tau = 0$ (where χJ_f is the adsorption from the vapour flux and τ is the effective adatom lifetime accounting for desorption and incorporation) and the boundary conditions of $n_a(z = 0) = n_s$ (i.e. the adatom concentration on the substrate) and $n_a(z = l) = n_l$ being used, the solution to $n_a(z)$ may be yielded and subsequently substituted into Equation 3.5 to obtain;

$$\frac{\mathrm{d}l}{\mathrm{d}t} = C_0 V + \frac{4\chi V\lambda}{\sqrt{3}R}\frac{\left(1 - n_l/n_f\right)[\cosh(l/\lambda) - 1] + (n_s - n_l)/n_f}{\sinh(l/\lambda)} \tag{3.6}$$

where $n_f = \chi\tau J_f$ is the effective adatom activity on the sidewalls, $V = J_f\Omega$ is the equivalent deposition rate and $\lambda = \sqrt{D_f\tau}$ is the diffusion length.

This model may also account for the lateral extension of a NW, this becoming more significant as l increases beyond λ. The radial growth may be expressed by the following expression;

$$\frac{dR}{dt} = \frac{2\chi V}{\sqrt{3}}\frac{\tau}{\tau_{inc}}\left[1 + \frac{(\cosh(L/\lambda) - 1)}{(L/\lambda)\sinh(L/\lambda)}\left(\frac{n_s + n_l}{n_f} - 2\right)\right] \tag{3.7}$$

The model assumes that *R* is constant along the NW length, however it is often observed that lateral growth occurs to a greater extent at the base of NWs resulting in the tapered morphology shown in Fig 3.2d. The model also assumes a hexahedral NW shape.

3.2.3 Catalyst generation

Various techniques are available to generate arrays of metal nanodots on substrates (used as the droplets in VLS growth) including drop casting[45, 46] or spin-coating[47, 48] of nanodot colloidal solutions and various lithographic techniques[49, 50]. In this work, thin metal films were de-wetted by annealing, this method being used widely for VLS catalyst fabrication[36, 40, 51-59]. In Appendix A, a short description of the dewetting mechanism is given in Section A.2, and an experimental study of Au nanodot formation on Si and Mo substrates is presented in Sections A.3 – A.5.

3.2.4 Alternative bottom-up growth mechanisms for NWs

3.2.4.1 Solution-liquid-solid. One variant of the VLS mechanism is the *solution*-liquid-solid (SLS) mechanism, which follows the same principle as VLS growth, i.e. droplet alloy formation, droplet saturation and NW precipitation, but the reactions take place at catalysts suspended in solution, the semiconductor material being delivered in the form of dissolved molecular precursors[60].

3.2.4.2 Vapour-solid-solid. NWs may also be grown from the vapour phase via the vapour-*solid*-solid mechanism (VSS), whereby the catalyst remains solid throughout (hence the term 'droplet' is not used here) and incoming material reaches the catalyst-solid interface via solid diffusion through the catalyst[61]. VSS growth may occur when growth is carried out at temperatures at which no liquid alloy may form. Owing to the diffusivity of impurities through a solid phase being lower than through a liquid phase, the growth rates of VSS NWs are typically an order of magnitude lower than for VLS[62]. Other characteristics of VSS growth are: a) the catalyst has a faceted shape and a low aspect ratio[63]; and b) after cool down, major levels of semiconductor material (typically exceeding ~ 10%) remain in the catalyst[64]. There has been some controversy over the phase of the catalyst in this mechanism, Noor[65] proposing that it exists as a quasi-solid (or quasi-liquid) and that material is delivered to the catalyst-solid interface through semi-molten pores.

Other bottom-up methods include catalyst-free vapour-solid NW growth[66] – thought to be crystallographically driven[67] – and screw-dislocation driven NW growth[68].

3.2.5 Nanowire growth directions and cross-sectional shape

3.2.5.1 NW growth axis: NWs typically grow in a crystallographic direction that minimises the total free energy, this being dominated by the surface energy of the interface between the metal droplet and the semiconductor[69]. This is usually a low-index direction, such as <100>, <110>, <111> or <112>. For zinc-blende semiconductors, the polar <111>A and <$\bar{1}\bar{1}\bar{1}$>B directions are most common. NWs with a wurtzite structure are often found to grow along the <0001> direction[70].

The most obvious way of controlling the angle of inclination between NW and substrate is by choice of substrate orientation. For instance, on a <$\bar{1}\bar{1}\bar{1}$>B substrate, there are 4 available out of plane <111> directions in which zinc-blende NWs may grow; the <$\bar{1}\bar{1}\bar{1}$>B direction perpendicular to the substrate and three other <111> directions at an angle of 19.5° (Fig 3.7a). Fig 3.7b shows a plan view of this case, the azimuthal angle between the non-vertical <111> NWs being 120°. Of course, NWs growing from a <$\bar{1}\bar{1}\bar{1}$>B substrate may also adopt non-<111> growth directions. The surface treatment, initial catalyst condition and NW diameter are all known to affect the growth direction[69].

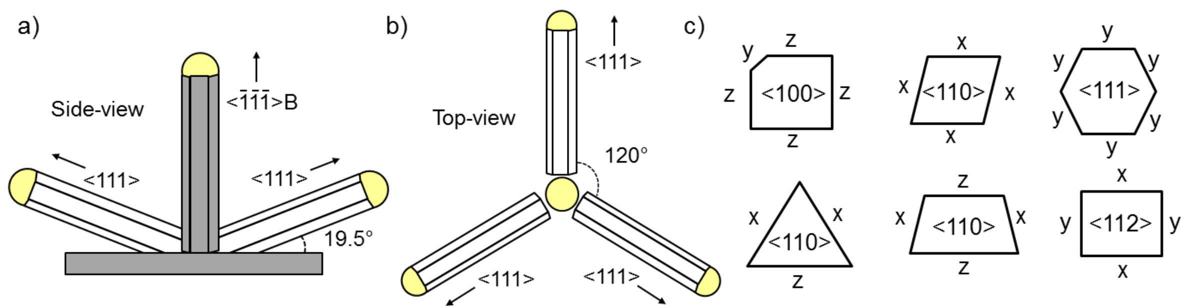

Fig 3.7: a) Side-view and b) plan-view of zinc-blende NWs with <$\bar{1}\bar{1}\bar{1}$>B (grey) and other <111> (white) growth directions, on a <$\bar{1}\bar{1}\bar{1}$>B oriented substrate. c) Some possible cross-sectional geometries for zinc-blende NWs having different growth axes (as labelled inside the shape), enclosed by the low index planes x = {111}, y = {110} and z = {100}, adapted from Ref. 71. The NWs depicted in a) and b) have the hexagonal cross section of <111> NWs that is depicted in the top-right of c).

3.2.5.1 Cross sectional shape: The growth axis of a NW influences its cross-sectional shape since its sidewalls are terminated on low-index crystallographic planes that are parallel to the growth axis (for non-tapered mono-crystalline NWs). Fig 3.7c shows some of the allowed shapes for zinc-blende NWs of differing growth directions. The NW ultimately adopts the shape that minimizes both the surface energy of the sidewalls and the surface-to-volume ratio.

In crystal growth the 'Wulff construction' is used to predict crystal habit. Wulff[72] stated that the perpendicular distance, h_i, from the centre of mass of a crystal to the ith face of the crystal is proportional to the surface energy, γ_i, of that face. Based on this, Herring[73] proposed that to predict a crystal's geometry, one must first construct a polar plot of the surface energy as a function of crystal orientation, this plot being denoted $\gamma(\hat{n})$. Then, one must draw lines from the origin to the points on the $\gamma(\hat{n})$ plot in all directions, and then draw planes perpendicular to each line at the points of intersection with the $\gamma(\hat{n})$ plot, the end result being the 'Wulff construction' whereby the inner envelope of the planes defines the equilibrium shape of the crystal. See Chapter 6 for Wulff constructions of CdTe NWs.

3.3 Nanowire solar cell concepts and features

In this section, some NW-based solar cell concepts are described and the advantages and challenges associated with them are discussed with reference to CdTe solar cells.

3.3.1 Nanowire device configurations

Fig 3.8 shows some examples of configurations in which NWs may be used in a PV device.

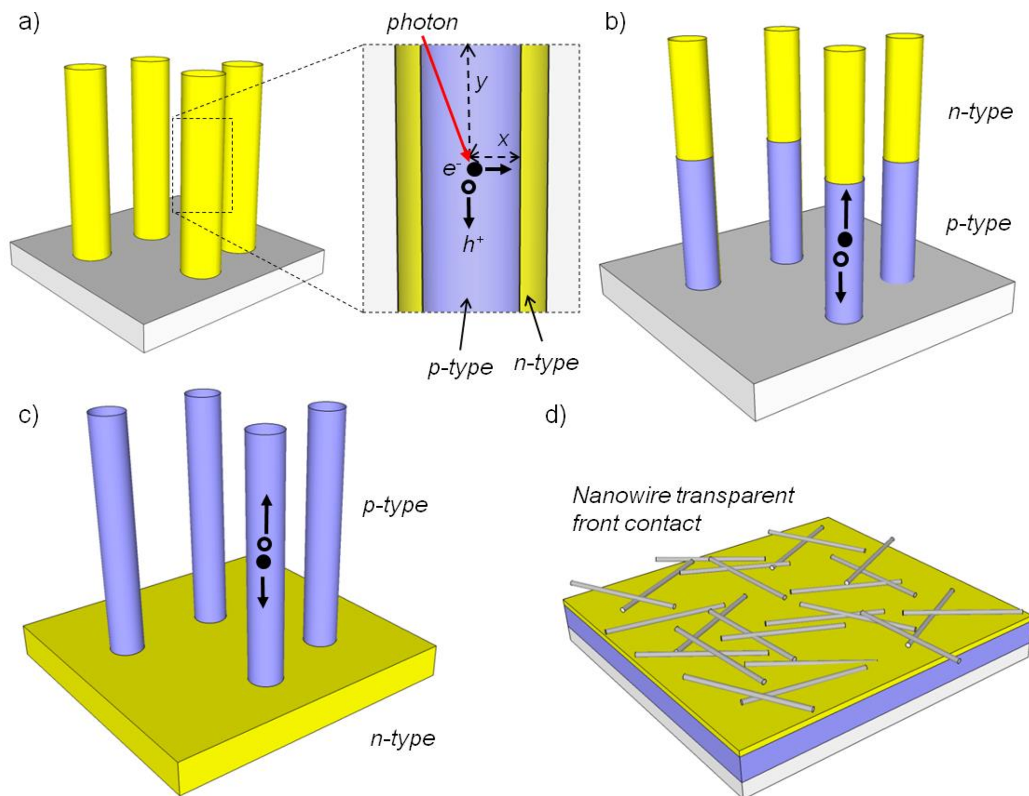

Fig 3.8: Various NW solar cells using a) radial *p-n* junctions, b) axial *p-n* junctions and c) NW-substrate *p-n* junctions. d) Interconnected metal NW network used as a transparent front contact on a traditional planar device.

In particular, the 'core-shell radial *p-n* junction solar cell' (Fig 3.8a) has recently been the focus of much research[74-84] since it may yield PV performance enhancements.

Radial *p-n* junctions have been formed by depositing an *n*-type (*p*-type) shell layer onto a *p*-type (*n*-type) NW array[79, 80], or by diffusing an *n*-type (*p*-type) dopant into the surface of *p*-type (*n*-type) NWs[78]. Devices based on axial *p-n* junctions[85] (Fig 3.8b) or on *p-n* junctions formed between the NWs and the substrate[86] (Fig 3.8c) do not benefit from the concept of absorption/collection orthogonolisation, but may take advantage of absorption enhancements yielded by the NW arrays and the improved crystal quality of the NWs (see Sections 3.3.2 and 3.3.3). Finally, there has recently been interest in the use of interconnected metal NW networks as transparent front contacts[87] (Fig 3.8d) – the spaces between the NWs providing suitable transmittance and the NWs themselves being highly conductive.The geometry orthogonalises the processes of light absorption and carrier collection allowing them to be optimised individually by tailoring the NW height and diameter[82]. In traditional planar devices, either a compromise has to be made between these two processes, or high quality material enabling sufficiently long minority carrier diffusion lengths must be used. This is particular relevant to poor absorbers such as Si[76].

3.3.2 Optical absorption

The optical properties of NW arrays are highly dependent on the NW diameter, length, density, orientation, uniformity and periodicity. Nevertheless, absorption enhancements relative to traditional films are regularly reported, either by quenching transmission (light trapping) or reflection.

Light-trapping effects resulting from the textured nature of NW arrays are inevitably highly beneficial for solar cells, particularly for materials with low absorption coefficients such as Si. For ideally textured surfaces, the theoretical maximum[88] enhancement factor (EF) to the effective path length of a photon is $2n_{ref}^2$ (where n_{ref} is the refractive index and the enhancement is due to total internal reflection). However, Garnett *et al.*[22] demonstrated factors (EF ~ 73) exceeding this in Si NW solar cells ($2n_{ref}^2$ ~ 25 in Si) with NW diameters of 490 nm, resulting in J_{SC} enhancements relative to thin-film devices. At larger diameter scales, Kelzenberg[89] *et al.* demonstrated that the absorbance of thin-films and of Si micro-wire arrays (D ~ 1 – 2 μm) were comparable when the total wire array volume was just 1/100th that of the film's. In this case however, the optical response was highly anisotropic owing to the verticality of the NWs, the absorption being significantly reduced when the light was incident normal to the substrate (parallel to wire axis). NWs with random orientations are expected to be superior in absorbing a wider range of incident angles.

In terms of reducing reflectance, as well as the obvious quenching associated with the roughness of NW arrays, a more sophisticated method may be used: By varying the NW diameter along their length, their effective refractive index will also vary accordingly, resulting in a graded index from air-to-NW, which quenches reflectance[90].

NWs present a multitude of other interesting optical properties: For example, NWs with sub-wavelength diameters may act as waveguides owing to the high refractive index difference between the NWs and their surrounding medium, leading to them also being suitable for lasing applications. Quantum-size effects are briefly discussed in Section 3.3.5.

In the case of CdTe it may be presumed that light trapping is less of a concern than for Si, owing to CdTe's already high absorption coefficient. However, the reduction of material usage in CdTe devices remains desirable[91, 92] owing to the scarcity and high cost of Te.

3.3.3 Carrier collection

Semiconductor material of lower quality (i.e. with lower minority carrier diffusion length, L) may be used in radial junction NW devices as opposed to in planar devices since in the former case minority carriers are generated much closer to the depletion region. This was proven theoretically by Kayes *et al.*[76], who calculated that whereas in a planar Si device J_{SC} drops from 35 mA/cm^2 to 4 mA/cm^2 as L is reduced from 100 μm to 100 nm, in a Si NW device J_{SC} remains > 40 mA/cm^2 through the same range of L. Indeed, J_{SC} was also shown to be roughly independent of L in CdTe/CdS radial junction devices[75].

Nevertheless, VLS grown NWs are typically of *high* crystal quality, the layer-by-layer growth mechanism yielding monocrystalline structures with no random high-energy grain boundaries, as often reflected in the NWs' highly structured photoluminescence spectra[93-95]. This is expected to lower bulk recombination, since random grain boundaries are known to be sinks for impurity segregation, and therefore improve carrier collection even in axial junction and NW-substrate junction devices.

On the other hand, since NWs have a high surface-to-volume ratio, carrier collection can be plagued by surface recombination or interface defects[2] as discussed in Section 3.4.2.

3.3.4 Strain relaxation

In the case of heteroepitaxial growth onto lattice mismatched substrates, misfit and threading dislocations may form due to strain and in some cases there is surface roughening and island-formation. However, in the case of NW growth, this strain can be more effectively relieved owing to the extra degree of freedom at the free NW sidewalls[96]. Biermanns *et al.*[97] report that strain accommodation in NW growth is achieved through the formation of misfit

dislocations immediately at the beginning of growth. As a result, threading dislocations do not form[98], or alternatively they grow out immediately at sidewalls. This should enable the development of solar cells of high quality material from layer sequences that would traditionally be unobtainable. In some cases, fully coherent NW growth is reported for highly mismatched systems, such as InAs on Si, this system having a lattice mismatch of 11.6%[99]. However, there exists a critical radius below which dislocation-free NW growth can be achieved (26 nm for the InAs/Si system), and this decreases with increasing mismatch[99].

The extra degree of freedom provided by the NW sidewalls also enables more efficient strain relaxation during subsequent shell growth, with Kavanagh *et al.*[98] demonstrating that strain relaxation was more quickly achieved (also via the formation of misfit dislocations) in core-shell InAs/GaAs heteronanowires as opposed to axial heteronanowires.

3.3.5 Confinement effects in quantum wires

In the case of *quantum* wires, quantum confinement effects occur due to the spatial confinement of the exciton wavefunction in two dimensions[100]. One particular quantum effect that may be relevant to solar cells is the size-dependence of a materials' optical band gap. Typically, the 'particle in a box' model using effective mass approximations is used to understand this behaviour[101]. Here, the exciton dispersion relation includes a size-dependent kinetic energy term (not the case in bulk unconfined systems): In the strong confinement regime the energy levels of free electrons and free holes are inversely proportional to the square of the size of the confining dimension, therefore the effective optical band-gap increases with decreasing size. This tunability of the band-gap of quantum structures makes them ideal candidates for use in multi-junction solar cells[102], however currently quantum *dots* are favoured over quantum wires for this purpose[103], presumably owing to their stronger confinement effects[104].

Other potentially beneficial confinement effects for solar cells include: a) improved absorption in indirect band gap solar cells due to the effective creation of a direct gap via folding of energy bands in *k*-space[105]; b) reduction of electron-phonon coupling[106] which may reduce the thermalisation of hot carriers and enable their collection; and c) multiple-exciton generation[107].

3.4 Challenges for core-shell nanowire solar cells

In this section, the issues related to the design and characterisation of radial junction core-shell NW devices and the fundamental limitations to their efficiency are discussed.

3.4.1 Optimisation of device architecture

Whereas in thin-film solar cells significant effort is made to optimise film thickness to maximise device efficiency[108], for NW solar cells the complexity is greater: NW radius, length, spacing, shape and orientation must all ultimately be optimised. For example, in the case of NW spacing, if it is too large then optical absorption may be limited by transmission losses[89], although these may be reduced by using light scattering nanoparticles (Fig 3.9a). If NWs are spaced too close together on the other hand, it can prove challenging to effectively coat NW arrays with conformal shell layers.

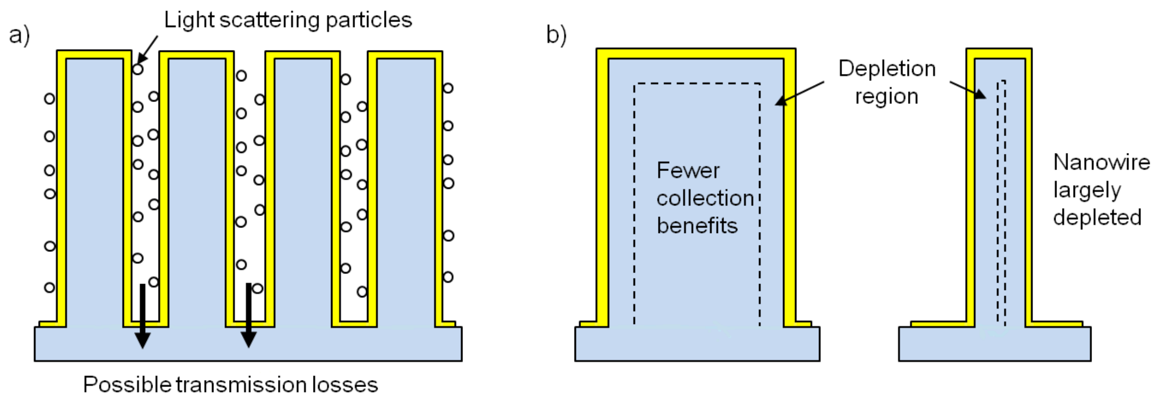

Fig 3.9: a) Vertical core-shell NWs may be coated in light scattering nanoparticles in order to reduce transmission losses. b) In order to maximise the carrier collection benefits of the radial geometry of the *p-n* junction, the NW core diameter must be optimised.

In the case of NW radius, if it is too wide then the collection benefits of radial junctions are lost, and if it is too narrow then the overlapping radial depletion regions would lead to the entire NW being depleted of carriers (Fig 3.9b). The optimum radius is expected to be comparable to the minority carrier diffusion length[109]. An investigation of the effect of NW dimensions on device efficiency is reported in Chapter 7.

3.4.2 Interface states

One of the principal loss mechanisms in heterojunction solar cells is recombination at interface states in the band gap[110]. This contributes to the reverse saturation current density, J_0, which reduces V_{OC}. Interface recombination, and therefore J_0, is expected to increase with increased junction surface area[111].

First, a distinction is made between *surface* states and *interface* states. Surface states arise upon termination of a single material, whereas interface states arise at the interface of two different materials. Nevertheless, they both have localised wavefunctions (at the surface or interface) that correspond to solutions to the one-dimensional Schrödinger equation that arise

when there is disruption to the periodic potential[112], these solutions existing within the forbidden band gap in both cases. For surface states, this disruption to the potential is in the form of an abrupt step from a periodic function in the bulk to the vacuum level outside, and for interface states, the periodicity of the potential is simply different on either side of the interface. These states also arise due to the existence of dangling bonds[112]. Furthermore, interface induced gap states may arise from the tailing off of electron wavefunctions from one material into the band-gap of the other material when there is a conduction (or valence) band off-set (Fig 3.10)[112]. For heterojunctions, it is interface states and interface recombination that are relevant.

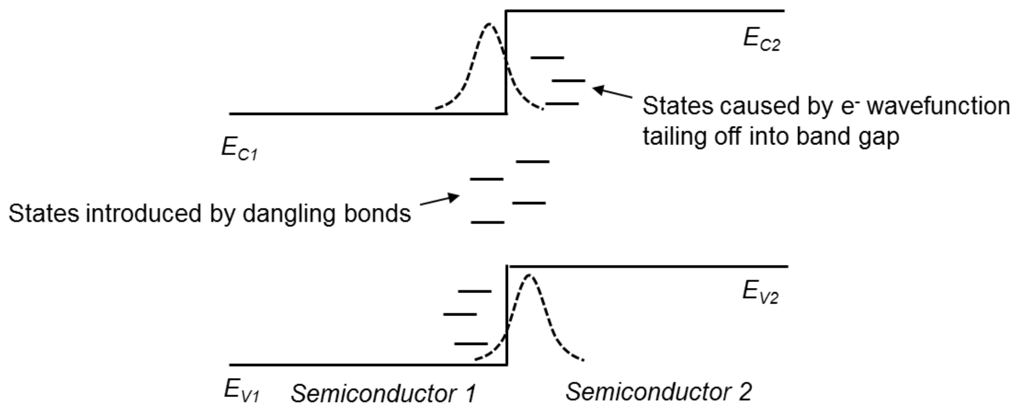

Fig 3.10: a) Band-diagram of an abrupt hetero-interface demonstrating the origin of interface induced gap-states.

An estimate of the V_{OC} reduction caused by an increase in junction surface area can be made by assuming that J_0 scales *linearly* with junction area[113] and neglecting any changes to the bulk recombination rate. For a planar device, if J_0 is taken to be 1×10^{-12} mA.cm^{-2} and J_L to be 27 mA.cm^{-2} (i.e. close to the best reported J_{SC} for CdTe solar cells) then according to Equation 2.7, V_{OC} ~ 800 meV. For NW devices with cylindrical NW's 10 μm long, having a diameter of 200 nm and being spaced 200 nm apart, $J_0 \sim 4 \times 10^{-11}$ mA.cm^{-2}, i.e. 40 times greater than in the planar case, and V_{OC} ~ 710 meV. (This V_{OC} loss may however be counteracted by reductions in bulk recombination).

In an attempt to reduce interface recombination in radial junction solar cells, a thin intrinsic layer may be inserted between the *n*- and *p*-type materials to passivate the interface states[114]. For the CdS/CdTe system, Kapadia *et al.*[75] calculated that V_{OC} may be affected by increased interfacial recombination velocity, S_i, but notably, in the range of experimentally determined values of S_i at the CdS/CdTe interface, this effect is minimal.

3.4.3 Impurities from catalysed NW growth

Although the metal droplets may be removed from the NW tips after growth[115], these catalysts may introduce deleterious impurities into the NWs themselves. For example, Au in Si introduces deep recombination centres that are detrimental to solar cell performance. Indeed, Oh *et al.*[116] identified Au within Au-catalysed Si NWs using *Z*-contrast transmission electron microscopy (TEM) imaging. Consequently, efforts have been made to self-catalyse VLS growth using one of the NW's constituent elements as the droplet (e.g. Ga for GaAs NWs)[117, 118].

3.4.4 Characterisation

Measuring the physical properties of NWs and the performance of full NW devices can be a challenge in itself, either owing to the non-uniformity of NW arrays, contacting difficulties, or the requirement to distinguish the contribution of the NWs themselves from any additional structures present (such as an underlying seed layer). However, several strategies are helpful, including: a) optical characterisation of NWs that have been mechanically removed onto substrates[119] or into solutions; b) electrical contacting of mechanically removed individual NWs using moveable probes[120]; and c) deposition of electrical contacts onto NWs using a focussed ion beam[121].

3.5 CdTe nanowire literature review

Previous reports of CdTe NW growth are now summarised, with comments made on the suitability of the techniques used for the development of the CdTe NW core-shell solar cell that is proposed in Chapter 1. There are more than 110 reports of CdTe NW growth and this review is therefore restricted to those having the greatest relevance to PV devices, structures and methods. From a top-down perspective, CdTe NWs have been successfully manufactured from thin-films via etching[122] and lithographic[123] procedures. In the former case, the luminescence spectrum of the nanostructures was the same as that of the original film, implying the material quality is, as expected, highly comparable.

Bottom-up approaches are more regularly reported however, such as the deposition of material into either polycarbonate membranes[124, 125] or anodic alumina membranes[126-130] to template NW growth. Here, the material is typically delivered via electro-deposition. Other frequently reported bottom-up methods include the self-assembly of NWs from CdTe NPs[19, 131-134] – this process having also been studied theoretically for the CdTe system[135] – and the SLS technique[136, 137]. However, these solution-based methods typically result in a suspension

of NWs in solution rather than an array of NWs intact with a substrate, so they may not be suitable for the purpose of developing the NW solar cell described in Chapter 1. One exception is that reported by Sung *et al.*[138], whereby Bi-catalysed CdTe NWs were SLS-grown on glass substrates, although in this case a number of the NWs collapsed and the procedure produces a significant volume of unwanted planar material alongside the NWs.

The VLS approach to CdTe NW growth has also been successfully employed, with Bi[139], Au-Ga[140] and Bi_2Te_3[141] being used as catalysts, and molecular beam epitaxy[140, 142], pulsed laser deposition[143] and close-space sublimation[141] being used to deliver vapour-phase CdTe. In this work, a CSS-based VLS growth method is used (see Chapter 5), the only previous report being that of Ruiz *et al.*[141], although in that case the NWs were not uniformly intact with a substrate in a way that may be desirable for integration into a device.

In terms of producing uniform structures intact on a substrate, the most promising works are those reported by Utama *et al.*[144], who demonstrate self-catalysed VLS growth on muscovite (mica), and Wang *et al.*[145], who grew self-catalysed NWs onto ITO substrates. However, muscovite is insulating and ITO is typically used as a front contact in PV devices. At the present time, the production of well oriented upstanding CdTe NWs on a conductive substrate that is a suitable contact, using a scalable process has not been reported.

With regards the structural properties of CdTe NWs reported in the literature, it is common for the NWs to adopt the zinc-blende (ZB) phase[124, 132, 145, 146] and a <111> growth axis[145, 147], although wurtzite (WZ) CdTe NWs have occasionally been reported[143]. Luo *et al.*[148] demonstrated the ability to control whether self-catalysed 'NWs' were ZB or WZ by changing the growth temperature during sputter deposition. However, the structures grown may more accurately be described as columnar grains that are common for sputtered films, as opposed to individual NWs. VLS-grown CdTe NWs are monocrystalline, whereas those formed by etching, lithography or self-assembly are usually polycrystalline. CdTe *quantum* wires exhibit high absorption coefficients[137] and high luminescent quantum yields[149], and at larger scales (D ~ 50 - 100 nm), Kum *et al.*[124] report that the conductivity of CdTe NWs can be increased by five order of magnitudes through a combination of annealing and increasing the Te content.

3.6 Nanowire solar cell literature review

3.6.1 Silicon

As is typical for opto-electronic device research, early progress in the field of NW solar cells was largely made in Si devices, with the group of Prof. Harry Atwater at the California Institute of Technology publishing a number of pioneering articles in the last decade. First, the benefits of the radial junction concept were quantified in a theoretical study by Kayes *et al.*[76], who predicted the dependence of performance parameters on device dimensions and minority carrier diffusion lengths (L). The model used solves the diffusion/drift equations for minority carriers, the current continuity equations, and Poisson's equation in the geometry of interest. It was demonstrated that J_{SC} was independent of L for the radial junction devices and that efficiencies exceeding 20% were obtainable. Subsequently, Kelzenberg *et al.*[77] experimentally obtained efficiencies of 9% for single microwire core-shell Si devices, and Putnam *et al.*[78] obtained 7.9% for microwire array devices. In the latter case, the volume of Si used was equivalent to 4 μm thick planar films, i.e. significantly less than traditional bulk-Si devices. Note that these are microwire devices (D ~ 1 – 2 μm) rather than NW devices. Since then, a number of groups have broken the 10% efficiency threshold[150, 151], Ghargi *et al.*[152] reporting 12% efficient devices using particularly low quality Si.

Notably, it has been shown that radial junction device performance may be enhanced by optimizing NW/microwire density[115] and passivating surfaces using amorphous-Si coatings[77].

3.6.2 III-V

The highest efficiency NW array solar cells so far reported were fabricated from InP NWs, although in this case axial *p-i-n* junctions were used[153]. Efficiencies of 13.8% were achieved, with J_{SC} values (24.6 mA.cm^{-2}) reaching 83% of the best reported planar J_{SC} despite the fact that the NWs only covered 12% of the substrate surface. This was believed to be made possible by light trapping effects. Moreover, the V_{OC} (906 mV) of this device exceeds that achieved by planar devices despite having a surface-to-volume ratio 30 times greater. Another notable report accounts a GaAs radial *p-i-n* junction single NW device that achieved a very high J_{SC} value (180 mA.cm^{-2}), contributing to an efficiency (η ~ 40%) exceeding the Shockley Quiesser limit[154]. This was attributed to the enhanced absorption coefficient of the structure.

3.6.3 II-VI

Fan *et al.*[74] report the development of a radial junction CdTe/CdS device. CdS NWs were grown within an anodic alumina membrane which was then partially etched to expose the

NWs before a thin CdTe film was deposited to complete the radial junction array - the remaining alumina membrane is intended to block shunting pathways. The structure was completed with a Au/Cu bilayer contact, through which the device is illuminated. A peak efficiency of 6% was achieved, and notably, the efficiency increased as the exposed NW length was increased, this highlighting the importance of the radial junction. However, the insulating alumina in-fill reduces the area of the *p-n* junction available for illumination, and the metal contact through which the device is illuminated has only 50% transmittance. Moreover, the device is back-illuminated and so will incur significant recombination losses (since the majority of carriers will be generated far from the depletion region). Nevertheless, Fan's work remains the best example of a NW based device for the CdTe/CdS system. It was followed by a theoretical study by Kapadia *et al.*[75] claiming that efficiencies exceeding 20% are obtainable for the design. Other significant reports for II-VI systems include a 1%-efficient device based on CdTe NWs encapsulated in poly (3-octylthiophene)[155], a 3.53% ZnO/CdS core-shell NW device[80] and a device that includes ZnO nanocones embedded into a CdTe film[156].

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Chapter 4 : Experimental Methods

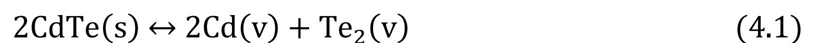
4.1 Introduction

This chapter presents an overview of the experimental methods used to grow and characterise all the samples studied in this thesis. It is in three Sections. Section 4.2 describes all of the thin-film and nanowire (NW) growth methods. Section 4.3 describes structural, chemical and optical characterisation methods used for the structures grown - where appropriate there are summaries of the methods used for interpretation of the data. Finally, Section 4.4 explains the device modelling, device fabrication, and the methods to characterise devices and to determine their performance. Unless otherwise stated, the equipment described was based at the University of Liverpool.

4.2 Thin film and nanowire growth techniques

4.2.1 Close-space sublimation

Close-space sublimation (CSS) is a form of physical vapour deposition (PVD) and was used in this work to deposit CdTe NWs and CdTe thin films. Whilst evaporation of CdTe can prove challenging and costly due to the material's high melting point (1092°C), direct sublimation can be achieved at temperatures as low as 500 – 600°C, owing to CdTe having a sufficiently high vapour pressure (0.1 Torr at 600°C). However, to achieve suitable deposition rates for thin-film growth (> 1μm/min) using sublimation, it is desirable to place the target substrate in close proximity (typically a few mm) to the source material so as to ensure efficient transfer of material from the source to the substrate. In the sublimation process, upon heating, CdTe dissociates into elemental vapours which then recombine at the substrate surface, as follows;



$$2\mathrm{CdTe(s)} \leftrightarrow 2\mathrm{Cd(v)} + \mathrm{Te_2(v)} \quad (4.1)$$

Other materials that have high melting points, such as CdS, may be deposited using CSS, provided they have a sufficiently high vapour pressure at the temperatures used. A schematic diagram of the system used, custom built by Electro-Gas Systems Ltd., is shown in Fig 4.1.

In this system, powdered CdTe source material (bought from Alfa Aesar, 5N pure) is placed in a source tray, above which the substrate is held - face down, 5 mm from the source. The source tray, substrate holder and chamber are constructed from high purity quartz, so to

limit the introduction of impurities. Two external heating elements are used, one situated below the source, and one situated above the substrate. These heaters are on rollers and are removable. They are separately controlled, although their heating cannot be completely decoupled due to their close proximity - the diameter of the chamber is ~ 110 mm.

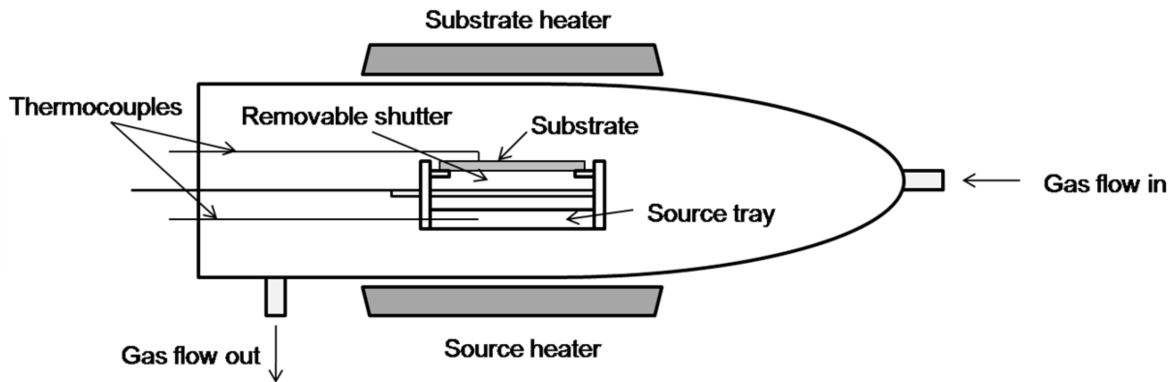


Fig 4.1: Schematic diagram of the close space sublimation chamber used in this work

Nevertheless, a sufficient temperature gradient from source to substrate can be achieved to promote sublimation transfer. Thermocouples are used to monitor the source and substrate temperatures, T_{source} and T_{sub}. A removable shutter could be used to start and stop growth. Since for T_{source} > 500°C the growth rate could be as high as 5 μm/min. The use of the shutter was sometimes necessary for the accurate control of layer thickness.

The growth tube may be pumped to ~ 10^{-1} Torr using a scroll pump although most growth runs in this work were conducted under either N_2, O_2, H_2, or N_2/O_2 or N_2/H_2 mixtures. These gases could be introduced to the growth chamber as a static fill in the pressure range 1 – 700 Torr, or as a flow of up to 100 sccm (standard cm^3 min^{-1}).

This equipment provides a wide parameter space for growth via control of T_{source}, T_{sub}, gas pressure and mixture and deposition time. These variables are known to have a significant effect on the deposition rate and grain structure of generated thin-films. For instance, Major *et al.*[1] demonstrated that grain size in CSS-grown CdTe increased linearly with N_2 pressure, the grain size having a profound effect on the performance of CdTe solar cells. The exact growth conditions used in this work are included in the relevant results chapters.

4.2.2 Radio frequency magnetron sputtering

Sputtering can be used to deposit a wide range of dielectrics, metals and semiconductors. Sputter deposition involves the ejection of material upon bombardment of a source ‘target’ with an ionised gas (i.e. a plasma), and the subsequent transfer of the ejected material onto a substrate. For the plasma, typically a non-reactive gas such as Ar is used, which is ionised and

accelerated by a DC or RF potential, the former for conducting and the latter for resistive materials. The ejection process occurs as a result of the momentum transfer between the impinging ions and the atoms of the target being bombarded. The transfer of material from source to substrate is a ballistic process as the pressures within the sputtering chamber are typically just a few mTorr. For magnetron sputtering, an arrangement of permanent magnets is situated behind the target to confine the plasma at the target surface, so as to enhance sputter rates. For more in-depth explanations of the principles of sputter deposition, the reader is referred to Refs 2-4.

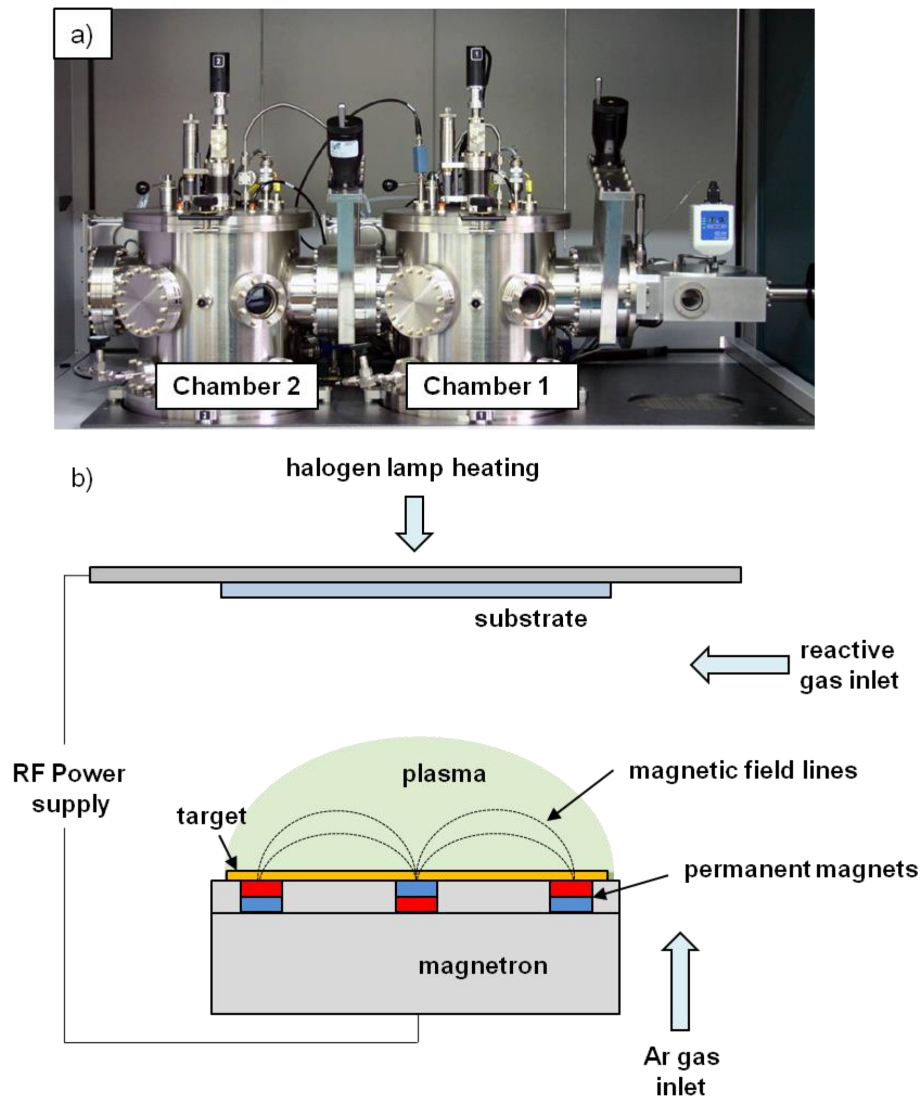


Fig 4.2: a) Photograph of the AJA Orion Phase II-J dual chamber system. b) Schematic diagram of the sputtering set-up inside each chamber.

In this work, RF magnetron sputtering was used to deposit thin films and NW coatings of CdS, ZnO and In_2O_3:Sn (ITO). Fig 4.2a shows a photo of the sputtering system used here, an AJA Orion Phase II-J dual chamber kit. Fig 4.2b shows a schematic diagram of a single

magnetron/substrate configuration within each chamber, although each chamber may accommodate multiple magnetrons. A brief description of the deposition process in this system from a single target is now given. For further details, the reader is referred to the PhD thesis by Treharne[5].

The chamber is pumped to high vacuum (~ 10^{-6} – 10^{-7} Torr) and Ar is introduced at pressures of 1 – 20 mTorr. The AJA system uses the 'sputter up' configuration and the substrate is heated by halogen lamps to up to 800°C. The target is rotated during growth to improve uniformity; this is necessary as the targets are not placed centrally. Reactive gases may also be introduced during growth: In Chapter 7, the use of CdS:O films, generated by sputtering CdS in the presence of O_2, is presented (CdS:O has a wider band-gap than CdS - see Chapter 7 - and therefore may be more suitable as a window layer). Deposition rates are typically of the order ~ 10 nm/min, and sputter generated films commonly consist of grains < 50 nm in diameter.

For sputter deposition variation of the growth conditions is well-known to influence both the growth rate and properties of the films. While there are some general trends – i.e. increasing the RF power and decreasing the gas pressure both have the effect of increasing the growth rate – the details may be system dependent. The reader is referred to Ref. 5 for a specific report of the electrical and optical properties of ITO, ZnO, SnO_2, CdS and CdTe prepared in this particular sputtering system.

4.2.3 Chemical bath deposition

Chemical bath deposition (CBD) is achieved via the precipitation of a solid phase from a solution onto a substrate following chemical reactions. The substrate is immersed in the aqueous solution that contains the precursors. CBD is a convenient and low cost technique conducted at relatively low temperatures (< 100°C), and is often used to grow the window layers for thin-film solar cells[6]. Grain sizes are typically small (< 50 nm) therefore the films can be grown relatively thin (< 100 nm) whilst maintaining high levels of surface coverage. For the case of CdS, CBD is achieved by the thermal decomposition of aqueous thiourea ($SC(NH_2)_2$) in the presence of Cd^{2+} (aq).[7]

In this work, CBD was used to coat CdTe NWs with a CdS shell layer. A solution of 318.2g H_2O + 31.8g NH_4OH was prepared, which was put into a reaction vessel and heated to 67°C by a water bath. 0.1456g of $CdSO_4$ was then added to the vessel. NW samples on substrates were then suspended in the vessel and 0.333g of thiourea was added to initiate the reaction. A nitrogen 'bubbler' was put in place in the vessel and used intermittently during the reaction (once a minute) to displace any gas bubbles that may accumulate on the substrate

surface. Following deposition, samples were removed and rinsed in DI water. Using this method, layers of ~ 100 nm were deposited after 20 minutes of reaction time. In this work, CBD was carried out at Northumbria University.

4.2.4 Metal-organic chemical vapour deposition

In metal organic vapour deposition (MOCVD), organometallic precursors are thermally decomposed over a heated substrate, normally in the presence of hydrogen, often at atmospheric pressure. A polycrystalline deposit forms on the substrate (MOCVD) or in the case of a single crystal substrate, an epilayer may form (metal organic vapour phase epitaxy, or MOVPE). Dopants may be introduced in organometallic or gaseous form and the method is capable of high levels of materials control. High performance CdTe solar cells have been generated by MOCVD at the University of Glyndwr[8], where MOCVD was carried out in this work.

A schematic diagram of the system used here is shown in Fig 4.3. In this work, CdZnS and CdS shell layers were deposited onto CdTe NWs. The precursors used were dimethylcadmium (DMCd), ditertiarybutylsulphide (DtBS) and diethylzinc (DEZn). H_2 was used as the carrier gas, controlled using mass flow controllers. Reactions took place with the substrate held at 360°C for 15 – 20 mins; heating being provided by an RF heater. Film thickness was monitored and controlled in-situ by a triple wavelength laser reflectometer.

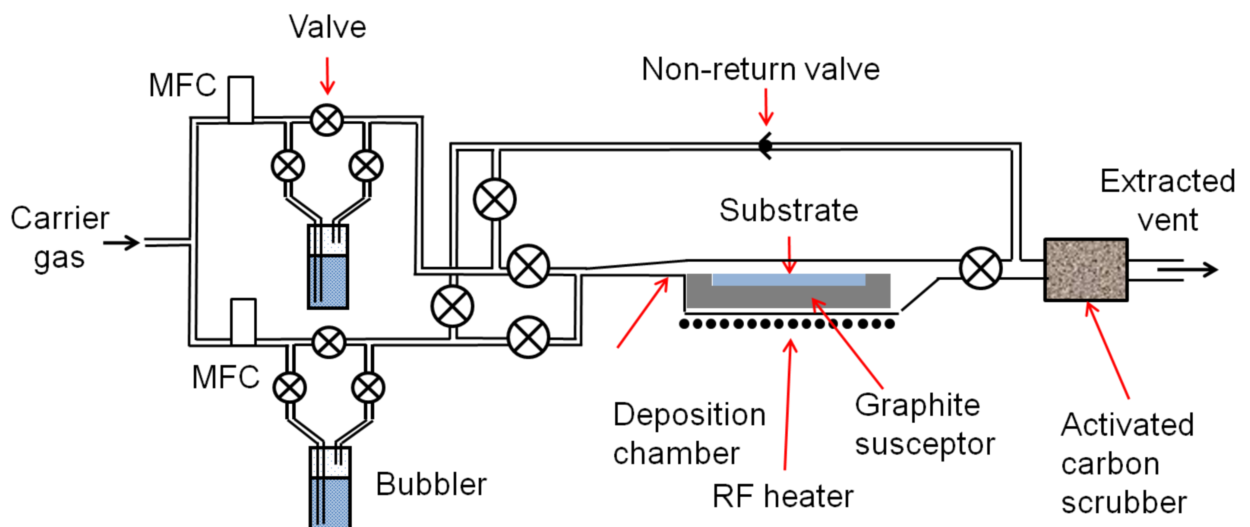


Fig 4.3: Schematic diagram of the metal-organic chemical vapour deposition system.

4.2.5 Thermal evaporation

Thermal evaporation is a common PVD technique to deposit thin films and involves the vaporisation of a source from liquid phase upon heating under vacuum. In this work, Au and $CdCl_2$ were deposited using thermal evaporation, in separate systems. For Au, a UNIVEX 300

evaporator, having a base pressure of 10^{-4} Torr and a quartz crystal thickness monitor was used. For fine control of layer thickness, the growth could be lowered to 5 nm/min. Patterned growth could be achieved by placing substrates in contact with a shadow mask. Au of 99.99% purity was obtained from Advent.

$CdCl_2$ was evaporated in a custom built diffusion pumped system operating at 10^{-5} Torr. The $CdCl_2$ was of 99.99% purity and was from Aldrich Ltd. In CdTe device fabrication, doping with $CdCl_2$ is achieved by evaporation of a layer onto the CdTe surface followed by annealing [9] - in this work the annealing step was carried out in a tube furnace.

4.3 Characterisation techniques for grown films and nanostructures

Here, structural, chemical, electrical and optical characterisation techniques are described.

4.3.1 Thin-film profilometry

Thin film profilometry is used to measure the thickness of a grown film by scanning a stylus across a step profile in the film. The change in height of the stylus is measured via deflection of a laser which is incident on the back of the stylus assembly. In this work, an AMBIOS XP-Plus Stylus Profiler was used. The resolution of this instrument is limited to ~ 20 - 30 nm. Step profiles in the films were created either by mechanical scribing (for CdTe), swabbing with HCl (for CdS) or masking during deposition (ZnO and ITO).

4.3.2 Scanning electron microscopy

The scanning electron microscope (SEM) is in widespread use for the imaging and analysis of solids in materials science. In modern instruments a focussed nanoscale (~ 5 nm) electron beam is used to excite secondary electrons, backscattered electrons, X-rays and cathodoluminescence from the sample. Each of these signals may be recorded using a dedicated detector as reviewed by Goldstein[10]. To produce an image, the beam is raster scanned over the sample, and the detected signal is combined with the beam position. The majority of work in this thesis uses the secondary electron and back-scattered electron imaging modes. Secondary electrons are ejected from the specimen atoms by inelastic scattering interactions with beam electrons, and are detected by an Everhart-Thornley detector which is situated to one side above the sample. The shadowing effects caused by the detector placement and sample roughness results in images with topographic contrast. Back-scattered electrons are beam electrons that are elastically scattered by atoms in the specimen. Images generated in this mode exhibit compositional contrast since electrons are scattered more strongly by heavier atoms[10].

To gain a detailed understanding of the spatial origin of a given signal the generation volume resulting from the electron-beam specimen interaction can be modelled by Monte-Carlo means. In this work 'CASINO 3.1' software was used for the modelling[11], which makes a projection of electron trajectories following scattering collisions within a bulk sample upon irradiation with a Gaussian shaped electron beam. Two SEMs were used here; a Hitachi SU-70 field emission gun (FEG) SEM (at Durham University) and a Jeol JSM 7100F SEM. The reader is referred to Ref. 12 for a review of the prospects for electron microscopy characterisation of thin-film solar cells.

4.3.3 Transmission electron microscopy

Transmission electron microscopes (TEM) have wide applications in materials science and metallurgy in the evaluation of both crystal defects and man-made structures. They make use of the wave nature of electrons in the energy range ~ 100 – 400 keV, although some instruments use electron guns providing other energies. Samples must be very thin (< 200 nm) as image formation is based on transmission and diffraction of the incident electrons. In conventional 'two-beam' imaging, the specimen is oriented to favour just one strong Bragg reflection as well as the direct beam; bright- and dark-field images are formed using the direct and scattered beams respectively. Defects in samples can be revealed by diffraction contrast. Diffraction patterns that provide information about the phase, orientation and lattice constant of a crystal can be viewed in the back focal plane of the objective lens[13].

In high resolution instruments multiple beams are allowed to contribute to the image intensity and the phase contrast that results forms an image having resolution comparable to that of a semiconductor crystal lattice. In recent years the high quality of electron optics available has allowed imaging with nano-scale electron probes in scanning transmission electron microscopy (STEM) mode to generate atomic resolution images. This is particularly useful for compositional imaging (Z contrast) when combined with an annular detector in high angle annular dark field (HAADF) microscopy. TEMs are also often fitted with energy dispersive X-ray analysis (EDX) and electron energy loss spectrometers (EELS) for elemental analysis and mapping. The reader is referred to Refs 13 and 14 for fuller descriptions. In this work, a Jeol 2100 FEG TEM was used at Durham University.

4.3.4 Focussed ion beam microscopy and processing

A focussed ion beam (FIB) microscope uses a focussed beam of Ga^+ ions to sputter or mill away material, and can also deposit material using a organometallic vapour injection system. Its applications range from circuit modification and repair[15] to microstructural analysis or

even nanostructure patterning[16] and growth[17]. FIBs typically accommodate SEM capability, and can image in secondary electron or secondary ion modes. In this work, a FEI Helios NanoLab 600 was used (at Durham University) for milling and imaging smooth cross sections of NW arrays, individual core-shell NWs and thin-film solar cells. Prior to milling, a protective layer of Pt was deposited onto samples to ensure uniform polishing. Fig 4.4a shows a typical 'trench' that is initially created to reveal a cross section, and Fig 4.4b is an example of a secondary electron image of a cross section of a CdTe solar cell, taken from Ref. 18.

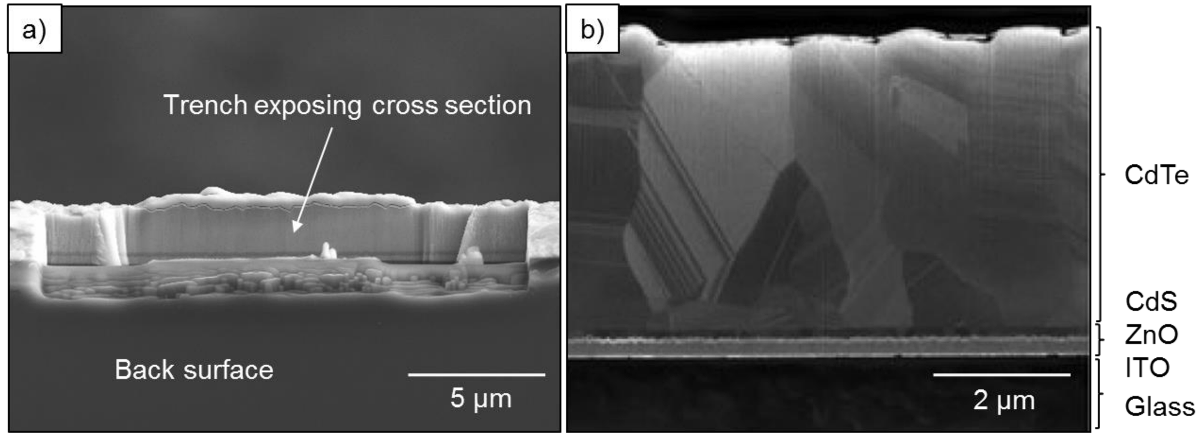


Fig 4.4: a) A trench created by FIB milling reveals a smooth cross section of a sample. b) A secondary electron image of a CdTe solar cell, demonstrating clear crystallographic contrast[18].

4.3.5 X-ray diffraction

X-ray diffraction (XRD) measurements were used to determine the crystal orientation and lattice parameters of CdTe films and CdTe NWs. The Bragg-Brentano geometry[19] was used as shown in Fig 4.5. X-rays are incident on a sample at an angle θ to the sample surface, and the intensity of diffracted X-rays is measured by an X-ray detector. As the sample is rotated by θ, the detector is rotated through 2θ, and the measured intensity is then plotted as a function of 2θ. X-rays diffract from crystal planes parallel to the sample surface when the incident angle θ satisfies Bragg's law;

$$\lambda = 2d_{hkl} \sin\theta \tag{4.2}$$

for which λ is the wavelength of the X-rays and d_{hkl} is the lattice spacing. Peaks in diffraction intensity at certain 2θ values are therefore characteristic of certain planes of Miller indices *hkl*. By determining d_{hkl} from θ, the lattice parameter, a, can also be calculated (for cubic materials), using the equation;

$$d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \tag{4.3}$$

Samples in which the grains are preferentially oriented will produce an XRD spectrum that is dominated by one peak, whereas randomly oriented samples will produce multiple peaks. This level of orientation may be quantified using the Harris method[20]. Here, a quantity called the texture coefficient, C_{hkl}, may be calculated for a given set of planes $\{hkl\}$, using the equation;

$$C_{hkl} = \frac{\frac{I_{hkl}}{I_{r,hkl}}}{1/n_p \sum_{n_p=1}^{n_p} \frac{I_{hkl}}{I_{r,hkl}}} \tag{4.4}$$

where I_{hkl} is the measured intensity of the diffraction peak for the given *hkl* plane, n_p is the number of diffraction peaks being considered, and $I_{r,hkl}$ is the intensity for the same plane but in a randomly oriented sample – in this work $I_{r,hkl}$ values for CdTe were taken from the ASTM index (set 15, card 770). The standard deviation, σ, of these C_{hkl} values is a measure of how preferentially oriented the sample is, and is calculated using the equation:

$$\sigma = \sqrt{\sum 1/n_p \, (C_{hkl} - 1)^2} \tag{4.5}$$

In this work, a Panalytical XPert Pro MRD XRD system was used with a Cu X-ray source.

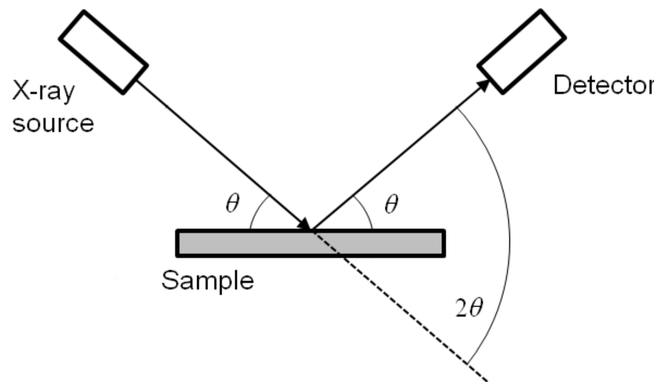


Fig 4.5: Schematic of the Bragg-Brentano (θ-2θ) set-up for X-ray diffraction measurements.

4.3.6 Energy dispersive X-ray analysis

X-ray compositional microanalysis was used in both the SEM and TEM work in this thesis. The principle is the identification of elements from their characteristic X-ray emission[10] (upon excitation with an electron beam) as described by Moseley's law which relates the emission frequency, ν, to the atomic number, Z, using two constants, C and σ:

$$\sqrt{\nu} = C(Z - \sigma) \tag{4.6}$$

Where necessary, the generation volume was quantified in order to interpret the spatial origin of an X-ray signal using Monte-Carlo modelling, as discussed in Section 4.3.2.

4.3.7 Secondary ion mass spectrometry

Secondary ion mass spectrometry (SIMS) is a destructive technique used to determine the composition of a sample. It is highly sensitive, with detection limits down to parts per billion. A beam of primary ions, having energies of several keV, is fired at the sample and secondary ions ejected by sputtering are analysed by a mass spectrometer[21]. In this work a quadrupole mass spectrometer was used, having a mass resolution ($m/\Delta m$) of ~ 100 – 500.[22] The reader is referred to Ref. 23 for a general review of mass spectrometry including the 'dynamic' or 'profiling' SIMS used in this work.

Here, a O^{2+} ion gun (Hidden Analytical) was used to sputter the sample, using a beam energy of 5 keV and beam current of 600 nA , with the sample chamber held at < 10^{-6} Torr (Thermo Scientific). The measurements were carried out at Northumbria University.

4.3.8 Nanoprobe STM/SEM

The Nanoprobe is a purpose built system for conducting electrical measurements of individual nanostructures. It comprises four individual scanning tunnelling microscopes (STMs) and a high resolution LEO Gemini FEG-SEM. The STM tips can be guided to a nanostructure to form non-destructible contacts, enabling two and four-point probe current-voltage measurements on NWs, or van der Pauw sheet resistance measurements[24] on nanosheets (e.g. graphene). Liquid He cooling allows measurements to be taken from 25 - 450K. The system is part of the Leeds EPSRC Nanoscience and Nanotechnology Research Equipment Facility at The University of Leeds. Ref. 25 gives an overview of STM operation.

4.3.9 Photoluminescence spectroscopy

Photoluminescence (PL) is an optical characterisation technique widely used for semiconductors. Electrons in a sample are excited by photons from a monochromatic light source, and the subsequent emission of photons is associated with a decay from a higher to a lower energy state. The variety of possible radiative transitions which give rise to PL spectral features is described in Section 4.3.9.1. The excitation intensity-dependent and temperature-dependent behaviour of the different types of radiative transitions are explained in Sections 4.3.9.2 and 4.3.9.3 respectively – these behavioural characteristics are often used to investigate the origin of spectral features.

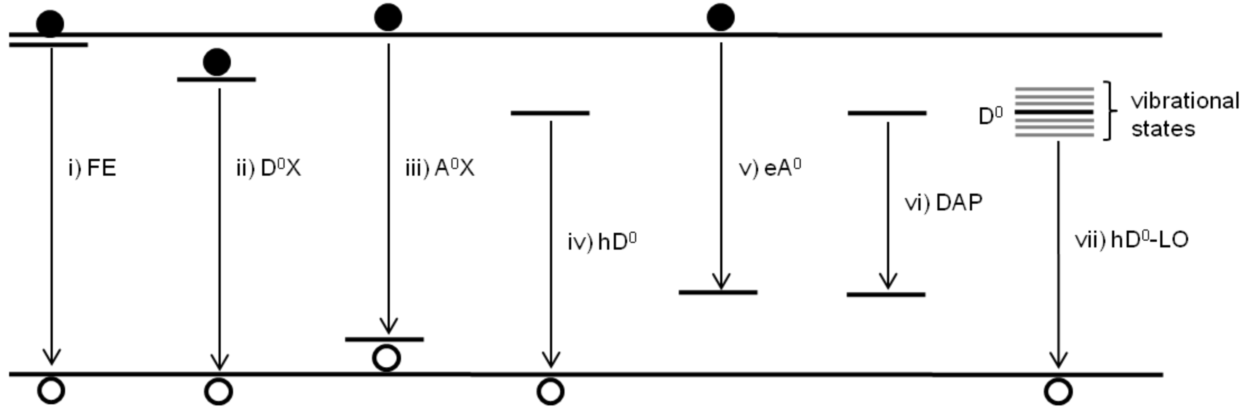


Fig 4.6: Possible radiative transitions in a semiconductor following absorption of a photon, giving rise to photoluminescence emission. CB and VB refer to conduction and valence bands respectively. Other symbols are explained in the text.

4.3.9.1 Possible radiative transitions: The energy of the emitted light, upon excitation, corresponds to the energy difference between the excited and ground states, and is therefore characteristic of the participating levels[26]. As well as band-to-band transitions, i.e. a decay from the conduction band edge to valence band edge, there are a number of other possible transitions as illustrated in Fig 4.6. Upon photon absorption, electron-hole pairs (excitons) can form – these are typically only stable at low temperatures, for which kT is lower than the exciton binding energy. Radiative emission arises from the recombination of free excitons (Fig 4.6i) and excitons bound to donor (ii) or acceptor states (iii). Alternatively, photon absorption can generate free carriers, which may decay via free-to-bound transitions, such as a free hole decaying to a neutral donor level (iv) or a free electron to a neutral acceptor (v). There may also be donor-acceptor pair (DAP) recombination (vi). Additionally, both Stokes and anti-Stokes processes can occur for each of these transitions (vii), via either the emission or absorption of a phonon: this may involve either longitudinal-optical (LO), transverse-optical (TO), or transverse-acoustic (TA) phonons.

Transitions that involve the absorption or emission of a phonon produce spectral peaks that are termed 'phonon-replicas' and are spectrally shifted from the 'zero-phonon' transition by an energy equivalent to the energy of the involved phonon. Intense phonon replicas are indicative of strong coupling between electrons and the lattice, this being defined by the Huang-Rhys coupling parameter, S, which is calculated using the relation

$$I_0 - I_N = e^{-S} \frac{S^N}{N!} \quad (4.7)$$

where I_0 is the intensity of the zero-line peak, and I_N is the intensity of the Nth phonon replica.

As the energy of PL emission is characteristic of certain donor and acceptor levels within a given material, the presence of these levels, and associated impurities, may be inferred from the spectra. However, considering all the possible transitions which have been described (including phonon related), it is noted that analysis of PL spectra must be treated with caution. Indeed, in order to identify overlapping peaks, analysis of their temperature- and excitation intensity-dependent behaviour is often necessary; this being reviewed in Sections 4.3.9.2 and 4.3.9.3.

PL spectroscopy ultimately serves to *qualitatively* identify point defect population; PL spectra dominated by exciton-related emission (also known as 'near band-edge' PL) is indicative of a highly pure sample for example[26]. Moreover, as the spectral resolution of PL spectra is enhanced for single crystal samples, with respect to polycrystalline samples, it can provide microstructural information. It is also used to quantitatively determine a samples' luminescent efficiency.

In this work, the 514 nm and 488 nm lines of an Argon laser (spot size, d = 1 mm, and excitation intensity, $L_{ex} \sim 10^1 - 10^3$ mA/cm^2) were used to excite samples held in a He cryostat at $T = 4 - 200$ K. The beam was highly linearly polarised in the vertical by use of a Brewster window, although with the beam being reflected by four mirrors there will be some degradation of the polarisation, and was incident on the samples at an angle of 20° to the normal. Low-pass filters were used to exclude the laser light. A collecting lens focussed the luminescence into a Bentham TM300 monochromator. Low resolution spectra were obtained by selecting the 150 line/mm grating, and higher resolution spectra with a 1200 line/mm grating. Detection was carried out on a 1024 pixel EG&G 1453C silicon diode array, cooled to -20°C. These measurements were carried out at Durham University.

4.3.9.2 Excitation intensity dependence of PL emission: The relation between the PL intensity and the excitation intensity L_{ex}, $I \propto L_{ex}^{k}$ often holds for PL experiments, with the value of k being a useful diagnostic tool for identifying the origin of transitions. By using basic rate equations that describe the different radiative transitions and the L_{ex}-dependence of the concentrations of excitons [X], electrons [e], holes, [h], acceptors, [N_{A0}], and donors [N_{D0}], Schmidt[27] calculated the expected k-values associated with excitonic transitions and free-to-bound transitions, these being $k > 1$ and $k \sim 0.5 - 1$ respectively. Here, the author summarises the approach used by Schmidt in Table 4.1. This is also extended here to include the k dependence for DAP transitions.

The power law dependence is estimated for two separate cases; that of free carrier formation (where $[e] \propto L_{ex}$ and $[h] \propto L_{ex}$) and that of direct exciton formation (where $[e] \propto L_{ex}^{0.5}$

and $[h] \propto L_{ex}^{0.5}$). The k-values derived from these two separate cases define the upper and lower boundaries of the real value of k for constant $[N_{A0}]$ and $[N_{D0}]$. However, one should also consider the effects of donor and acceptor saturation (i.e. $[N_{A0}]$ and $[N_{D0}]$ are reduced), screening, and exciton collision, all of which result in I saturating at high L_{ex}. As DAP transitions are dependent on both $[N_{A0}]$ and $[N_{D0}]$, they tend to saturate at lower L_{ex}, resulting in them typically having lower k-values (< 0.5) than free-to-bound transitions.

Table 4.1: Calculation of k-values for various radiative transitions in cases of i) free carrier formation and ii) direct exciton formation.

	Free excitons	***Bound excitons***	***Free-to-bound***	***DAP***
Generally, I_{PL} proportional to..	$[X] \alpha [e].[h]$	$[X] \alpha [e].[h].[N_{A0}] \alpha [e].[h]$	$[e].[N_{A0}] \alpha [e]$	$[e].[N_{A0}].[N_{D0}] \alpha [e]$
For free carrier formation, I_{PL} proportional to..	$L_{ex}.L_{ex}$	$L_{ex}.L_{ex}$	L_{ex}	L_{ex}
k for free carrier	*2*	*2*	*1*	*1*
For direct X formation, I_{PL} proportional to..	$L_{ex}^{0.5}.L_{ex}^{0.5}$	$L_{ex}^{0.5}.L_{ex}^{0.5}$	$L_{ex}^{0.5}$	$L_{ex}^{0.5}$
k for direct X	*1*	*1*	*0.5*	*0.5*
k range in reality	*1 - 2*	*1 - 2*	*0.5 - 1*	*0.5 - 1*

The excitation intensity dependence of peak *position* is useful in identifying DAP transitions. These peaks are blue-shifted as L_{ex} increases since the energy of emitted photons is dependent on the Coulomb potential, which is inversely proportional to the spatial separation of donors and acceptors: Increased excitation intensity gives an increased photo-excited carrier concentration leading to increased free carrier screening so that the more closely spaced DA pairs dominate.[26]

4.3.9.3 Temperature dependence of PL emission: The intensity, full-width half maximum and spectral position of peaks in PL spectra may all be influenced by the temperature at which measurements are carried out. Some of the general trends are now discussed. The shift in peak position can largely be attributed to the temperature-dependence of the optical band-gap, although DAP transitions may be identified by a blue-shift as temperature is increased[28]. PL *intensity* is typically quenched as the temperature is increased due to the presence of competing thermally activated non-radiative transitions involving non-radiative recombination centres, or Auger emission[29]. The extent of quenching varies depending on the type of

transition, although it is particularly pronounced for excitonic PL since at temperatures for which kT exceeds the exciton binding energy, excitons may dissociate.

An Arrhenius plot of PL intensity can be fitted with a theoretical decay model to obtain thermal activation energies associated with the quenching process. For example, as a bound exciton can be assumed to have two possible routes of dissociation, it can be modelled with an expression of the form;

$$I = \frac{I_0}{1 + \alpha_1 \exp(-E_1/k_B T) + \alpha_2 \exp(-E_2/k_B T)} \tag{4.8}$$

where I_0 is the zero temperature intensity, α_1 and α_2 are constants, and E_1 and E_2 are the thermal activation energies[30]. An expression of this form may also be used to fit the decay of DAP transitions. In this work, the temperature dependence of PL spectra were measured by varying the temperature of the cryostat from 4 – 200K. The decay of bound-exciton and DAP transitions were analysed using the above methodology.

4.3.10 Time-resolved photoluminescence

Time resolved PL involves the measurement of PL intensity following excitation by a laser pulse, as a function of time after the pulse event, within a narrow spectral range (~ 20 – 100 nm). This enables measurements of the PL decay of spectral features, and therefore the determination of the lifetime of excitons (of the order of picoseconds in polycrystalline films, or tens of nanoseconds in semiconductor quantum dots[31]) and free carriers. Either mono- or multi-exponential decays are observed, which relate to a decay from an excited state to the ground state, or to a decay via multiple excited states to the ground state, respectively.

In this work, initially PL spectra were generated, using an Edinburgh Instruments FLS 90 spectrofluorometer, equipped with an R928 photomultiplier tube (PMT). Excitation was provided by the 440 nm line of a Xe lamp. For lifetime measurements, a PicoQuant PDL 800-B pulsed diode laser (406 nm line, pulse width of 65 ps, repetition rate of 20 MHz) was used. The emitted photons were then collected and analysed by a Hamamatsu PMT (H5738P-01) and a Time Harp 200 time-correlated photon counting card (emission wavelength could be selected using a monochromator). Samples were held at 4 – 20K in a cryostat, cooled by continuous He flow. These measurements were carried out at Utrecht University, The Netherlands.

4.3.11 Spectrophotometry

Specular transmission and reflectance, and diffuse reflectance measurements of individual films, nanostructures and full devices were carried out using a Shimadzu SolidSpec-3700

spectrophotometer in the range λ = 165 – 2600 nm. The optical band-gap, E_G, of a film can be determined from a plot of $(\alpha h\nu)^2 - h\nu$, where α is the absorption coefficient that is calculated from experimental transmittance curves using the Beer-Lambert law [32], and $h\nu$ is the photon energy. These plots typically display a linear region indicating the onset of absorption, and the band-gap is equal to the *x*-axis intercept of the linear fit. This method is based on Stern's equation[33], which relates the absorption coefficient, photon energy, and band gap energy;

$$\alpha = \frac{\left[\xi(h\nu - E_G)^{\varsigma/2}\right]}{h\nu} \tag{4.9}$$

where ξ is a constant and ς = 1 for direct transitions. Note that the physically correct method is to plot α^2 - $h\nu$ (i.e. the $h\nu$ denominator in Equation 4.9 should not be included[34]), but plotting $(\alpha h\nu)^2$ - $h\nu$ is the widely used method since it makes identification of the linear region more clear, without affecting the accuracy of the measured E_G value.

4.4 Solar cell modelling, fabrication and characterisation

4.4.1 Modelling of solar cells

The SCAPS software, designed by Burgelman *et al.*[35], can be used to numerically model the operation of thin-film solar cells. In this work, SCAPS v.3.2.00 was used to model CdTe solar cells; the reader is referred to Ref. 35 for a brief description of an older version of the program. The program operates in one-dimension, dividing the entire stack of a solar cell into N_i intervals. At each interval, three unknowns are calculated from non-linear equations, these being; i) the electrostatic potential, ϕ_i, from the Poisson equation, and ii) the electron and hole concentrations, n_i and p_i, from their respective continuity equations. Alternatively, the quasi-Fermi energy levels for electrons and holes, E_{Fni} and E_{Fni} respectively, may be calculated. The model accounts for the incorporation of multiple separate layers, interfacial discontinuities in the band line-ups and also for carrier recombination. It generates *I*-*V* curves, capacitance-voltage (*C*-*V*) characteristics, spectral response and band diagrams.

The user interface allows insertion of new layers and the assignment of their physical properties (optical band gap, densities of states, carrier mobilities, doping levels etc.). The user can also input the type and concentration of defects in the bulk of individual layers and at interfaces. Relevant simulations may then be carried out either in dark, or under illumination (using a spectrum of the user's choice – in this work the AM1.5 spectrum was used).

4.4.2 Device architecture and scribing

In this work, two device types were investigated; CdTe thin-film and CdTe NW devices. Both were grown on Mo substrates, and comprised ITO/CdS/CdTe/Mo, with the primary difference being that for the NW device the CdTe film was replaced with a CdTe NW/CdTe film bi-layer (see Chapter 1). For both types, ZnO was also included in between the ITO and CdS layers for some devices. Growth on metal substrates is known as the 'substrate' configuration, which differs from the more common 'superstrate' configuration of metal/CdTe/CdS/ITO/glass.

To prepare the devices for electrical characterisation measurements, the grown structures were mechanically scribed into individual cells (see Fig 4.7). For contacting, Au probes were placed directly on an exposed section of Mo (the back contact) and on the ITO (the front contact) of the individual cells. The Au probe placed on the ITO resulted in some shadowing of the device for measurements under illumination, but this was accounted for when the cell area was defined.

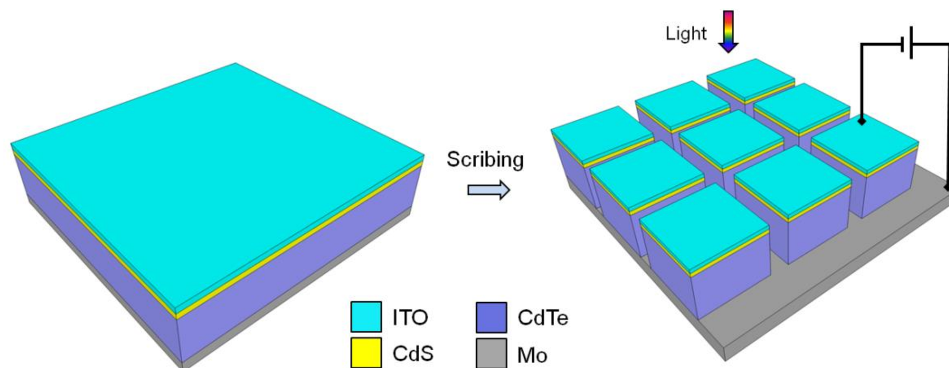


Fig 4.7: Contacting procedure for CdTe solar cells that have been grown in the substrate configuration. The same procedure was applied to NW CdTe cells.

4.4.3 Current-voltage measurements of performance

Current density-voltage (*J*-*V*) measurements of solar cells, under-illumination, were used to generate the key performance parameters of devices – efficiency, η, fill factor, *FF*, short-circuit current, J_{sc}, and open-circuit voltage, V_{oc}. Analysis of *J*-*V* curves and the methods of extracting these parameters, as well as R_S and R_{SH} are explained in Section 2.3. For *J*-*V* curves exhibiting significant rollover, R_S was determined from sections of the curve unaffected by rollover, typically at biases just below V_{OC}.

Here, samples were placed under an Oriel 81160 solar simulator which generates AM 1.5 illumination with a total intensity of 100 mW/cm^2. It was calibrated with a GaAs reference cell – which has an optical band gap (~ 1.42 eV at 300K)[36] that is well matched to that of

CdTe. The front and back contacts of solar cells were connected to a Keithley 2400 source meter, which provided biasing and measurement of current. Typically, *J-V* measurements were performed at room temperature using a bias range of -1 to +1V. Automation of *J-V* measurements was provided via a LabView interface.[37]

4.4.4 Current-voltage-temperature measurements

Temperature dependent *J-V* measurements (*J-V-T*) were carried out with the same source meter and software as above, but with the sample being held in the dark in a CTI closed cycle He cryostat. Temperatures in the range 200 – 350 K were explored. *J-V-T* measurements in the dark were performed to yield information on charge transport mechanisms, according to Equations 2.12 – 2.16 discussed in Section 2.3.

J-V-T measurements were also used to determine the height of the back contact barrier, ϕ_B, according to the Bätzner[38] method, whereby the total R_S is assumed to be equal to;

$$R_S = R_{\Omega 0} + \frac{\partial R_{\Omega 0}}{\partial T} T + \frac{C_x}{T^2} \exp(\frac{\phi_B}{kT}) \tag{4.10}$$

where the first two terms are the Ohmic resistance and its temperature coefficient, the final term is the thermionic emission component and C_x is a constant. The barrier height was calculated by determining R_S at various T and fitting the data to Equation 4.10. This method is only valid provided the main junction and back contact depletion regions do not overlap.

4.4.5 External quantum efficiency

External quantum efficiency (*EQE*) is the ratio of the number of charge carriers generated by a solar cell to the number of incident photons. For *EQE* measurements, monochromatic light is incident on a solar cell, its wavelength, λ, varied over a range that covers the active region of the cell (i.e. $\lambda <$ the optical band-gap of the absorber layer), and the measured *EQE* is plotted as a function of λ. Any *EQE* value < 100% represents either optical or electrical losses. A review of the features of the *EQE* response of CdTe/CdS devices is given in Ref. 39.

In this work, a purpose built Bentham PVE300 *EQE* system was used, which has a spectral range of 300 – 1100 nm, is fully automated through a USB interface, and controlled by Benwin+ software. The system uses a chopped monochromatic probe, assembled from a TMc300, 300 mm focal length monochromator and a dual xenon/quartz halogen light source. It also allows testing to be carried out under light biasing at 100 mW/cm^2 to simulate working conditions. The solar cell output is coupled by a transformer, which passes only the optically chopped signal, which is amplified and passed to the lock-in amplifier.

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Chapter 5 : Growth of Au-catalysed CdTe nanowires and core-shell structures

5.1 Introduction

This chapter explores the growth characteristics of CdTe nanowires (NWs) and core-shell CdS/CdTe hetero-nanowires. Au nanodots were used to catalyse CdTe NW growth by the vapour-liquid-solid (VLS) mechanism on Mo foil and on polycrystalline CdTe films, with vapour phase CdTe being delivered by close-space sublimation (CSS). Sulphide-based shell layers (CdS, $Cd_{0.9}Zn_{0.1}S$) were deposited onto these NWs by RF sputtering, chemical bath deposition (CBD) and metal-organic chemical vapour deposition (MOCVD). Finally, generation of core-double shell ITO/CdS/CdTe hetero-nanowires is presented, with the ITO layer being sputter-deposited. This CdTe NW and core-shell growth forms the basis of the development of radial *p-n* junction solar cells which is presented in Chapter 7.

Au is often used as the catalyst for vapour-liquid-solid (VLS) grown Si[1-5] and III-V[6-10] NWs, as discussed in Chapter 3, and here it was identified as suitable for the CdTe system due to the relatively low melting temperatures of both the Au-Cd[11] and Au-Te[12] binary systems, as shown in the temperature-composition (*T-x*) binary phase diagrams in Fig 5.1. According to these diagrams, at 520°C (a typical substrate temperature achieved in close-space sublimation), upon the incorporation of ~ 64 at. % of Cd or ~ 50 at. % of Te into Au, liquid droplets may form: The presence of liquid droplets is necessary for VLS growth to proceed.

In Section 5.2 the generation of Au nanodots on conductive Mo foils, necessary for VLS growth, by thermal annealing of Au films is reported - see Appendix A for a full investigation of the effects of annealing conditions on nanodot size and distribution. VLS CdTe NW growth on Mo substrates is then presented in Section 5.3, with NW lengths of up to 20 µm, diameters in the range 5 - 500 nm, and array densities of 10^6 – 10^7 cm^{-2} having been achieved. A mechanism of NW growth based on the gradual incorporation of Te into the Au nanodots, droplet saturation, and CdTe precipitation is postulated. The proposed mechanism is consistent with the additional observation of thin-film growth prior to NW nucleation; the formation of this film being untypical of VLS growth. As discussed in Chapter 3, the performance of NW-based solar cells is highly dependent on NW dimensions. Consequently, efforts to control CdTe NW dimensions and the extent of NW and film growth, by the manipulation of growth temperature and pressure, are also presented in Section 5.3.

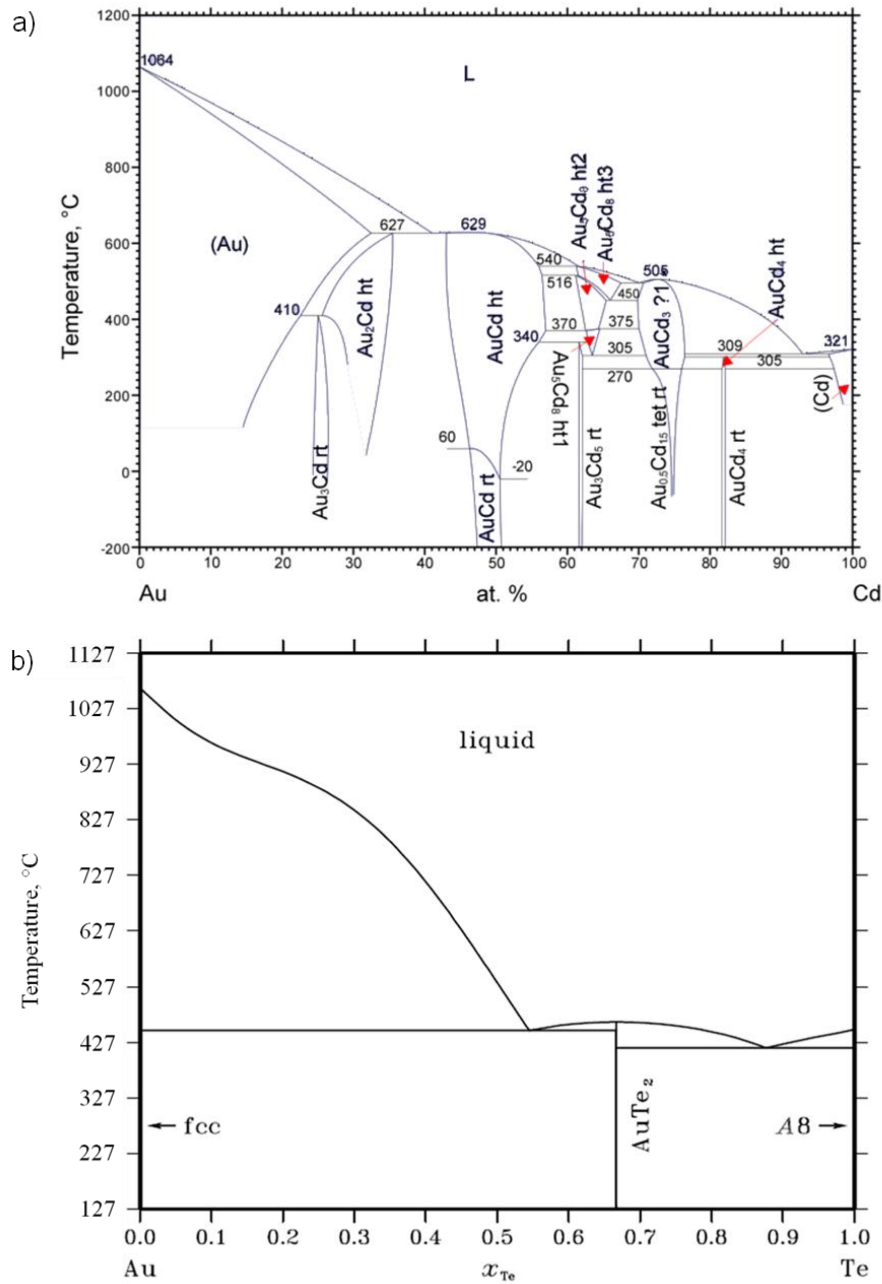

Fig 5.1: Binary phase diagrams of a) Au-Cd[11] and b) Au-Te[12]. Both systems have liquid phases at temperatures < 500°C.

As the desired architecture of the CdTe NW solar cell requires an electrically continuous absorber layer, NWs were also grown on polycrystalline CdTe films, generated by RF sputtering, as reported in Section 5.4. For CdTe it is shown that this yields more immediate NW nucleation and higher NW density ($10^7 – 10^8$ cm^{-2}) than for growth directly on Mo. This is considered to be because the necessary saturation of Au droplets with semiconductor material is achieved more readily.

Finally, in Section 5.5 the next stage in the development of radial *p-n* junctions is presented – the coating of CdTe NWs with sulphide based (CdS, CdZnS) shell layers. The

ability of RF sputtering, CBD and MOCVD to give uniform coatings without damaging the NWs was evaluated. Ultimately, RF sputtering was considered the most suitable in this regard, and therefore was also used to deposit an ITO coating onto CdS/CdTe core-shell NWs.

5.2 Au nanodot arrays

The formation of arrays of Au nanodots by thermal annealing of thin Au films is reviewed in Appendix A, Section A.2 and a preliminary investigation of annealing Au films on Si and Mo substrates is reported in Sections A.3 – A.5. These studies provided considerable insight into the conditions that generate nanodots which have morphologies and sizes appropriate for their use in VLS NW growth. Based on these insights, the basic procedure used for nanodot generation in all NW growth experiments reported in this thesis is described here.

5.2.1 Experimental procedure

15 mm x 15 mm substrates were cut from 100 μm thick Mo foil. They were cleaned ultrasonically and rinsed with de-ionised water, and dried with a N_2 gun. Following deposition of a 5 nm thick Au film by thermal evaporation, samples were transferred into the CSS chamber (described in Section 4.2.1). Both upper and lower heaters of the system were used to achieve a uniform heat distribution for annealing. The Au films were annealed at 360°C, under a static N_2 pressure of 100 Torr, for 30 mins. Plan view SEM images of each sample were recorded in the secondary electron imaging mode. The average diameter and density of Au was measured using the *Image Tool*^{TM} image analysis software.

5.2.2 Generation of nanodot arrays on Mo

Fig 5.2 shows an SEM image of Au nanodot array on Mo, achieved by the experimental procedure described above. Here the average diameter of the nanodots is 34 ± 4 nm and the density is $(3 \pm 1) \times 10^9$ cm^{-2}.

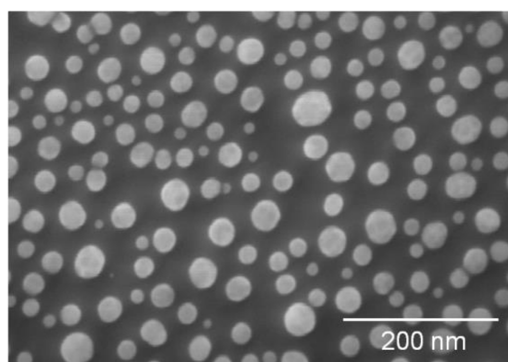

Fig 5.2: Plan view SEM image of Au nanodot array on Mo foil resulting from annealing a 5 nm thick Au film under 100 Torr of nitrogen at 360°C for 30 mins.

5.2.3 Discussion

The annealing conditions used here are suitable for the generation of high density Au nanodots arrays on conductive Mo substrates. For all subsequent NW growth experiments reported in this thesis, the annealing temperature and time are kept constant at 360°C and 30 mins respectively, but the N_2 pressure is varied (See Section 5.3).

5.3 CdTe nanowires on Mo substrates

This Section presents the first demonstration of CdTe NW growth on Mo substrates. The effects of the growth conditions on NW dimensions and morphology are reported. Chemical analysis of the wires and their catalysts is described and discussed with reference to the NW growth mechanisms reviewed in Chapter 3.

5.3.1 Experimental procedure

The general procedure used to generate CdTe NWs was as follows: 15 mm x 15 mm substrates, cut from 100 μm thick Mo foil (99.9% purity), were cleaned ultrasonically with de-ionized water and blow dried using N_2. Au films (~ 4 nm) were thermally evaporated onto the substrates, which were annealed in-situ in the chamber of the CSS kit at 360°C, for 30 minutes under 10 - 100 Torr of nitrogen to form arrays of nanodots. A shutter was used at this stage to prevent any sublimed CdTe arriving at the substrate. The temperatures of substrate and source were then raised to 520°C and 550°C respectively and the shutter removed for 30 minutes to allow CdTe sublimation transport, followed by rapid cooling (achieved by turning off the heater and sliding it away from the growth tube).

Although this was the basic procedure used for the growth of all CdTe NWs in Chapter 5, the exact values of the growth conditions were varied in order to gain insights towards the growth mechanism of the NWs, as presented in the following Sections: i) 5.3.3 – deposition time, t, was varied in the range 5 sec – 60 mins, ii) 5.3.4.1 – N_2 pressure, P, was varied in the range 10 – 100 Torr and iii) 5.3.4.2 – substrate temperature, T_{sub}, was varied in the range 490 – 550°C and source temperature, T_{source}, in the range 520 - 600°C. (Whilst for all NW growth experiments the temperature and time of the annealing stage were 360°C and 30 mins, the pressure was equal to that reported for the growth stage, as it was preferred not to abruptly change the pressure during the process since this is known to induce NW kinking[13]).

Secondary electron SEM images were recorded for all samples and microanalysis achieved by energy dispersive X-ray analysis (EDX) in the same instrument. Monte Carlo simulations of electron trajectories were generated using the CASINO 3.1 code (see Section

4.3.2). For these, a Gaussian shaped beam, of diameter, d = 1 nm and energy, E = 8 keV, was incident on the modelled specimen, and the subsequent trajectory of 1000 electrons were simulated. Bright-field TEM images and high-angle annular dark-field images – taken using the TEM operating in scanning mode (STEM) - were also recorded for some samples, with chemical analysis provided by electron energy loss spectroscopy (EELS) and EDX.

5.3.2 Nanowire morphology and chemical analysis

Fig 5.3a shows a CdTe NW array, generated using T_{sub} = 520°C, T_{source} = 550°C, P = 25 Torr and t = 30 mins. An example of an individual NW is shown in Fig 5.3b – it has a diameter of ~ 250 nm that is constant along its axis (see Section 5.3.5.2 for a discussion as to why this diameter is larger than the initial nanodot diameter), a length, l, of ~ 10 µm (determined from a lower magnification image) and a spherical droplet at the tip (confirmed below to be the Au catalyst). Its growth axis is not perpendicular to the substrate.

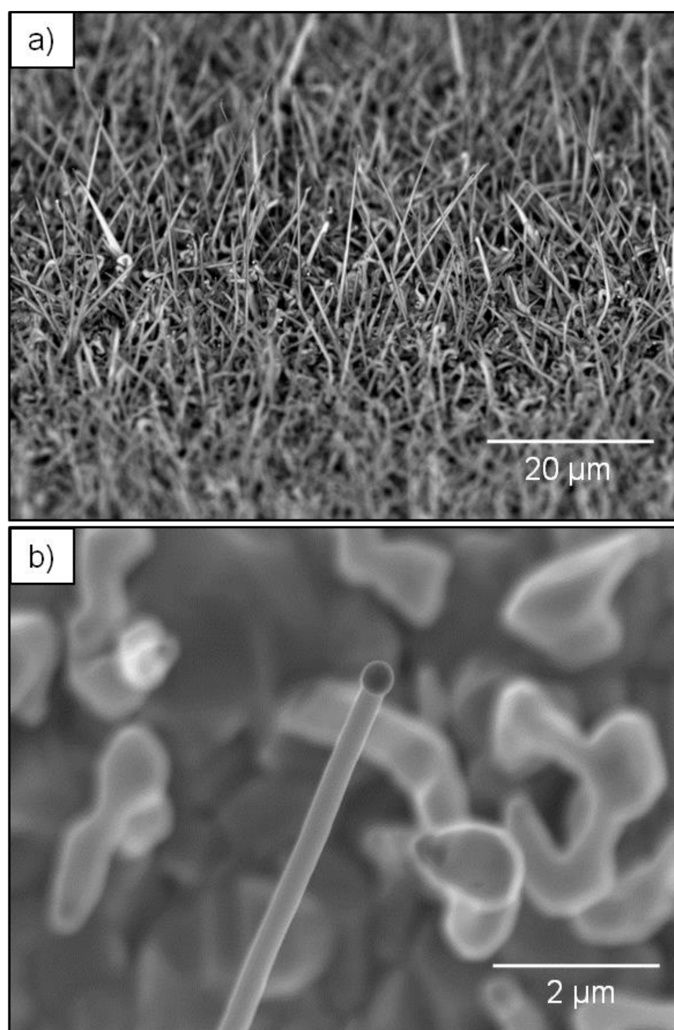

Fig 5.3: a) Secondary electron SEM image of a CdTe NW array grown by subliming CdTe at 550°C for 30 mins under 25 Torr nitrogen onto a Au-nanodot covered Mo substrate held at 520°C. b) Image of an individual NW with a spherical droplet present at the tip.

A distribution of NW lengths and diameters was obtained, with some exceeding 20 μm in length and having diameters in the range 50 - 500 nm. The distribution of NW diameters is considered to be governed by the distribution of the Au catalyst drop diameters. Fig 5.4 shows the relationship between NW length and diameter for approximately 70 NWs; typically, the thinner NWs grew to greater lengths than the thicker NWs. The orientation of NWs with respect to the substrate appears to be random (see Section 5.4). The NW density (in the range $10^6 – 10^7$ cm^{-3}, estimated from an average of measurements taken at different regions of the substrate) is roughly two orders of magnitude lower than the initial density of Au dots (~ 10^9 cm^{-3}, inferred from results from Section 5.2 for annealing Au films at 360°C). A rough semi-continuous thin film (~ 500 nm thick, confirmed to be CdTe by EDX) was also observed, at the base of the NWs and this is described in more detail in Section 5.3.3.

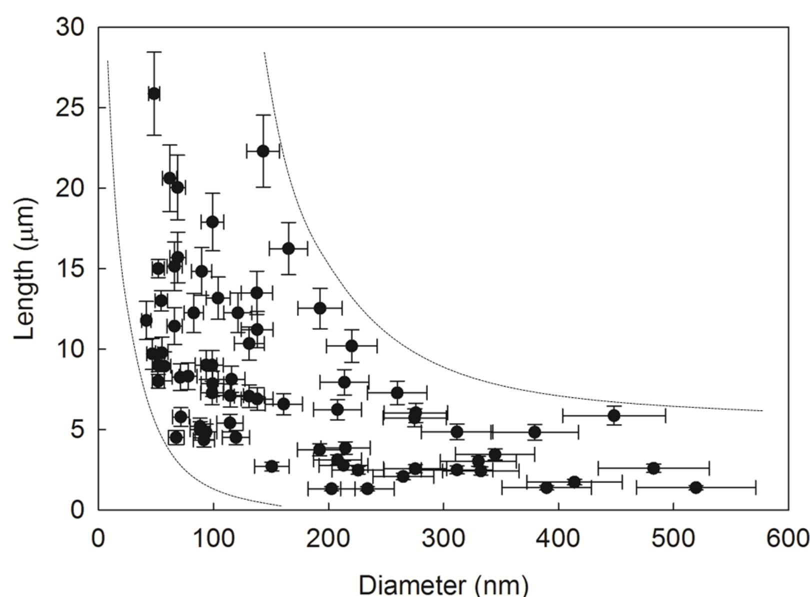

Fig 5.4: The relationship between nanowire length and diameter, measured directly from SEM micrographs for ~ 70 nanowires. Typically, the thinner NWs grew to greater lengths than the thicker NWs.

SEM/EDX microanalysis was used to determine the composition of both the stem and tip of a typical NW. A spectrum taken from the stem of a NW (Fig 5.5a) clearly shows Cd and Te Lα1 peaks but no Au, whereas a spectrum taken from the droplet (Fig 5.5b) is dominated by a Au peak. Fig 5.5c shows EDX mapping of the Au Lα1 peak overlaid with the accompanying secondary electron image, and Fig 5.5d is a TEM image demonstrating the highly abrupt interface between catalyst and the NW (in-depth TEM analysis is provided in Chapter 6). While both the EDX spectrum and mapping indicate that the droplet is at least Au-rich, it is not clear from these experiments whether it is pure Au or else contains Cd and Te (peaks for

all three elements are present in Fig 5.5b). It remains possible that the apparent presence of both Cd and Te in the droplet is due to a measurement artefact such as beam spreading or the excitation of a signal from a nearby wire.

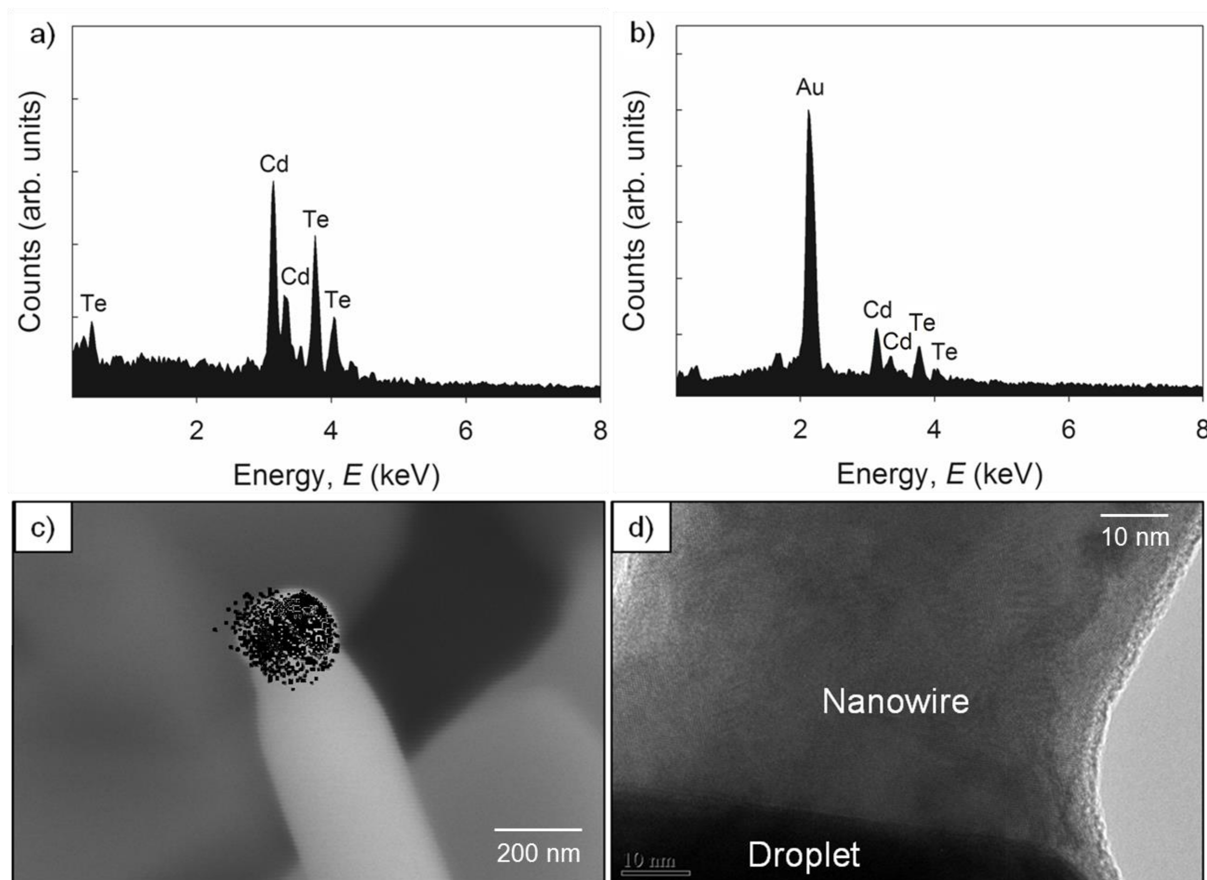

Fig 5.5: Energy dispersive X-ray diffraction (EDX) taken from a) NW stem and b) droplet at the NW tip. c) EDX mapping of the Au Lα1 peak overlaid on a secondary electron image of the NW tip. d) TEM image demonstrating the highly abrupt interface between droplet and NW.

For a more reliable chemical analysis, NWs were mechanically removed onto a Si substrate, and a number of EDX spectra were taken to investigate the spatial distribution of the elements. Fig 5.6a shows a representative example of such a NW and the analysis points. Fig 5.6c shows the corresponding atomic % of Au, Cd and Te at these points, with scan 1 being taken from the droplet, and scan 9 being taken from the furthest-most point from the droplet. Likewise, the data shown in Fig 5.6d corresponds to the higher magnification image shown in Fig 5.6b. The uncertainty assigned to the composition values was $\sqrt{\boldsymbol{n_c}}$ where $\boldsymbol{n_c}$ is the number of counts. The following comments refer to the higher resolution data in Fig 5.6d.

At the centre of the droplet, the composition is 100.0 % Au, although it must be noted that the sensitivity of EDX is limited to 100 ppm. Towards the edge of the droplet however, both

Cd and Te are detected (scans 2 and 3, Fig 5.6d). Moreover, Au was detected as a major impurity in the upper 50 nm of the CdTe NW stem itself (scans 5 and 6, Fig 5.6d). These observations may be real or may be the result of artefacts, either due to: a) the orientation of the NW on the Si – in this plane of view, the Au droplet is obscuring part of the NW itself; or b) beam spreading.

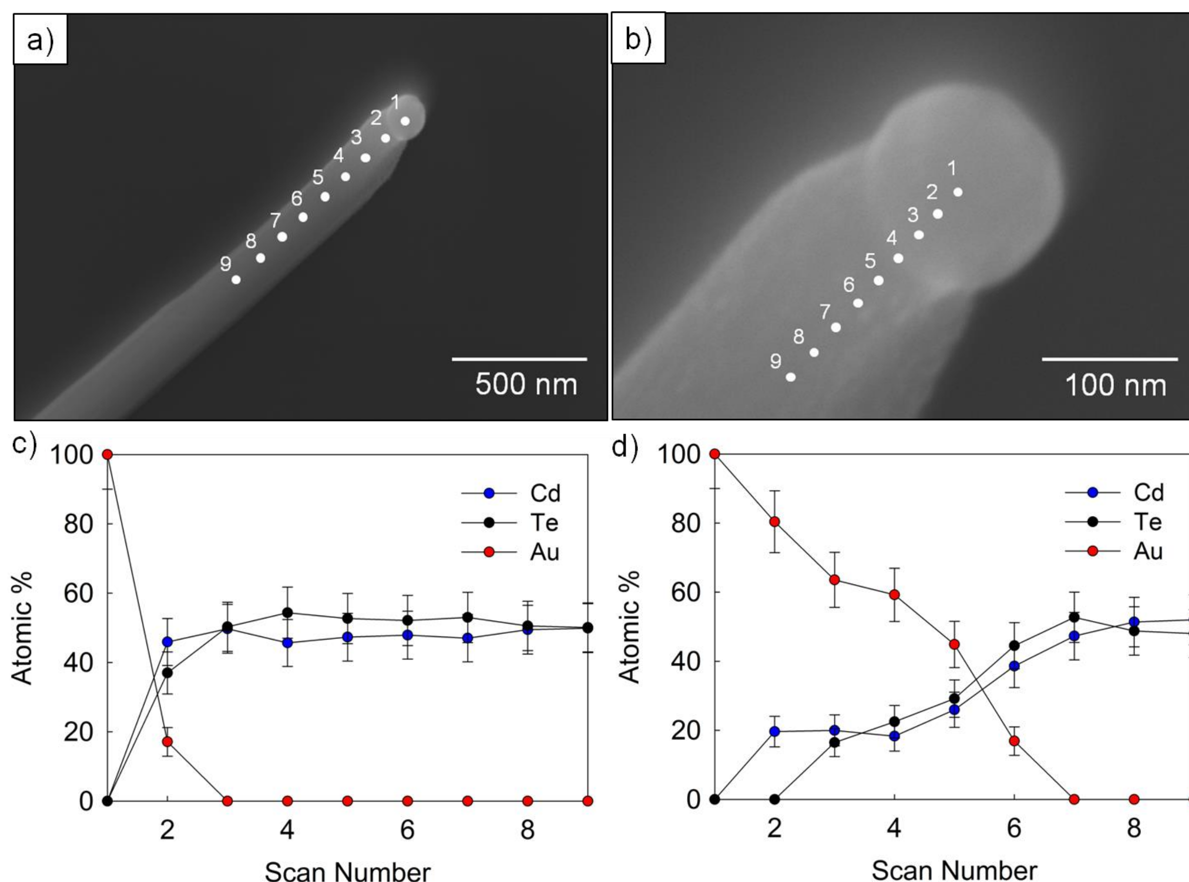

Fig 5.6: EDX was taken at various points along a NW to determine the spatial variation of the atomic % of Au, Cd and Te. This was first done at low-magnification in the SEM (a), with the corresponding composition plot shown in c. Similarly, the plot in d) corresponds to the higher magnification image in b).

In order to evaluate the influence of beam spreading, the electron trajectories in a CdTe NW (diameter ~ 100 nm) lying on a Si substrate upon irradiation with an 8 kV beam, were modelled using a Monte Carlo method. From Fig 5.7 it is clear that a large proportion of X-rays were emitted from a generation volume of radius as large as ~ 75 nm. Ultimately, while beam spreading and the angle of the interface are evidently significant on the scale of the analysis intervals in Fig 5.6b, scan 1 indicates that at least the tip of the droplets comprises Au alone.

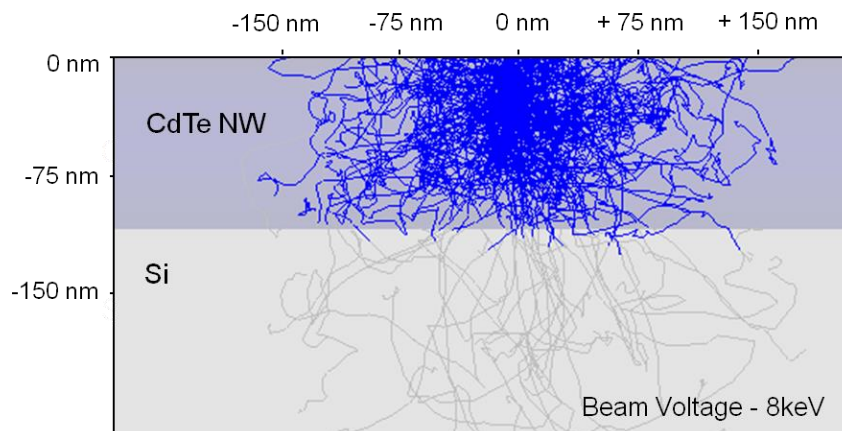

Fig 5.7: Monte Carlo simulation of the electron trajectories in a CdTe NW lying on a Si substrate irradiated by an 8kV electron beam.

5.3.3 Effect of deposition time on nanowire morphology

5.3.3.1 Time dependence of NW length and observation of film growth: Fig 5.8a - c show structures generated for different CdTe sublimation times in the range 5 secs – 40 mins.

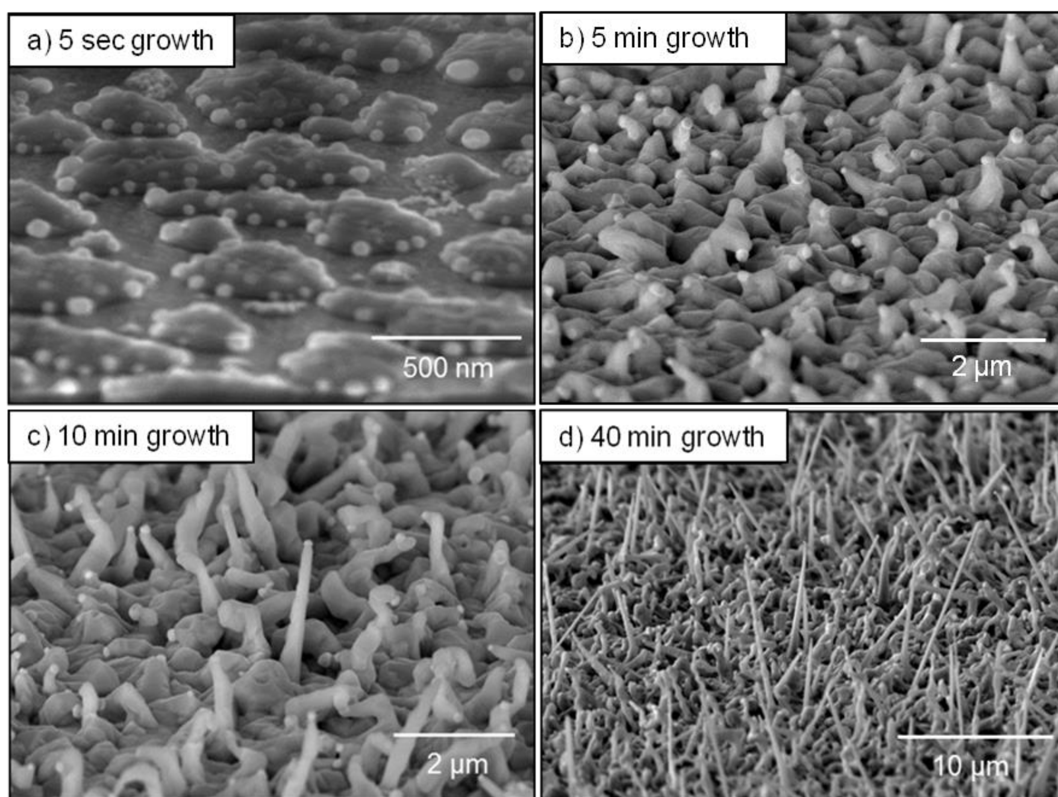

Fig 5.8: Structures generated after subliming CdTe for 5 secs – 40 mins, under P = 25 Torr nitrogen, using source and substrate temperatures of 550°C and 520°C respectively. a) After 5s of deposition, islands of deposit develop adjacent to the Au nanodots. b) After 5 mins, a film of CdTe covers the entire substrate and NW growth has initiated. After c) 10 mins and d) 40 mins NW growth becomes more widespread and NW lengths are greater.

For these samples growth was carried out under 25 Torr N_2, at T_{source} = 550°C and T_{sub} = 520°C. Fig 5.8a shows that after just 5 sec of deposition, islands of material (confirmed to be CdTe by EDX) accumulated adjacent to the Au droplets, and no NW growth is observed.

After 5 minutes of deposition, a film of CdTe covered the substrate, and NW growth had initiated with the NWs apparently nucleating from the film itself. At the longer growth times of 10 and 40 mins (Fig 5.8c and d) there is more widespread growth of longer NWs, the NWs being typically ~ 3 μm in the former and ~ 15 μm in the latter.

As the formation of a thin continuous film after 5 mins of growth was somewhat unexpected, chemical analysis was used to investigate the interface between this film and the Mo substrate. Fig 5.9 shows a high angle annular dark-field image, taken using the TEM in scanning mode (STEM). In this image, there appears to be three distinct regions of contrast, these being determined by EDX and EELS to be; CdTe at the top of the image, Mo at the bottom, and a ~ 50 nm layer of a $CdMoO_x$ phase in between. The spots of bright contrast in the $CdMoO_x$ phase are Au, evidently buried underneath the thin film.

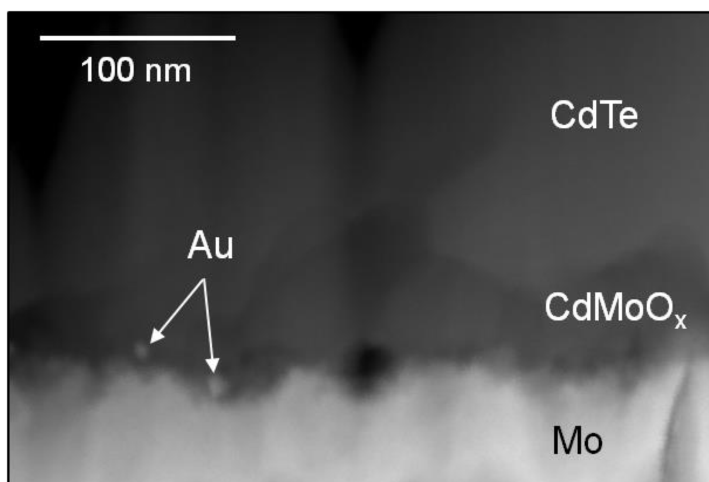

Fig 5.9: High angle annular dark-field TEM image of the interface between the Mo substrate and the thin film that forms during the initial phases of CdTe deposition. Between the CdTe and Mo, a thin layer (50 nm) of $CdMoO_x$ exists. Buried Au droplets are also seen.

Fig 5.10 shows the time dependencies of both NW lengths and radii with each data point being the average from 50 NWs in three separate locations. Initially (0 – 10 minutes) the formation of a continuous film dominated the growth and the average NW growth rate was just 0.16 μm/min. This increased to a maximum of 0.52 μm/min (between 20 - 30 minutes) once steady-state NW growth had become established. The red-line shows a theoretical fit to the data, which is described in Section 5.3.3.3.

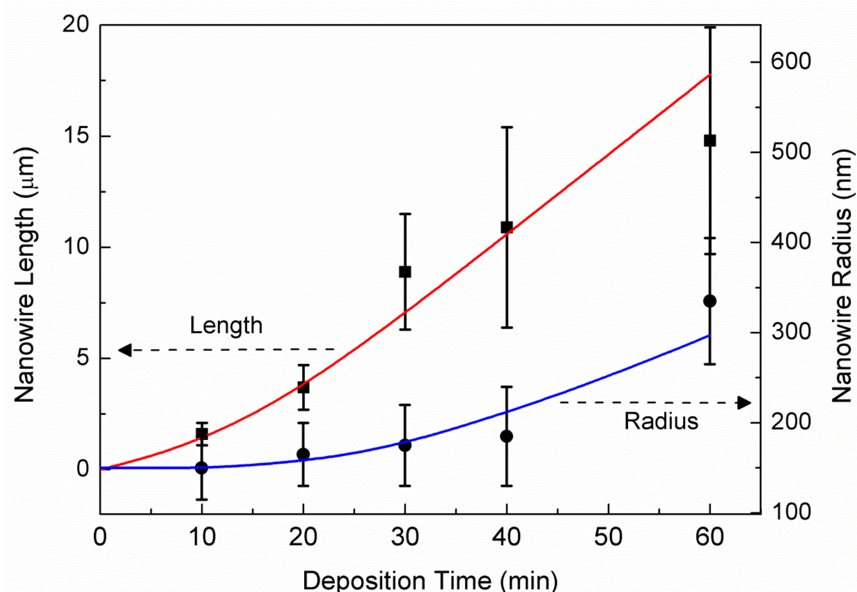

Fig 5.10: Dependence of NW length and radius on deposition time. The red and blue lines are the theoretical dependence calculated using a diffusion-induced kinetic model of VLS NW growth.

5.3.3.2: NW radius-time dependence: The time dependence of NW radii shown in Fig 5.10 was obtained by measuring the average of the base, middle and top radii for 50 NWs per data point. The average radius was constant (~ 175 nm) for 40 minutes of growth, and then increases after 60 minutes (~ 325 nm). As shown in Fig 5.11, many of the NWs were tapered, this being particularly visible for the longer growth times used. The NW in the centre of the image for example has a tip radius of < 100 nm and a base radius of > 500 nm.

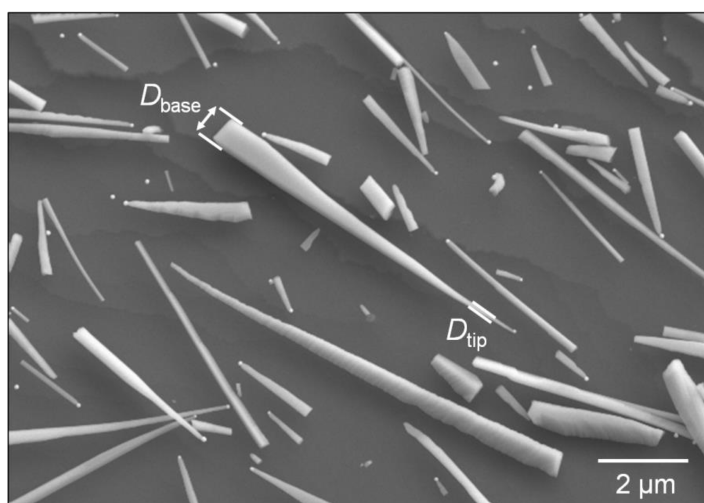

Fig 5.11: NWs (grown for 60 minutes) that have been removed from their substrate by pressing onto Si wafers. Some of the NWs show significant tapering from base to tip.

5.3.3.3: Fitting of time-dependence data with a theoretical model of VLS growth. The time dependence of both the lengths and radii of the NWs was fitted to the model of growth

developed by Dubrovskii *et al.*[14, 15] and described in Section 3.2.2.4 (Equations 3.6 and 3.7), which takes into account both the elongation and the simultaneous lateral extension of the NWs. In order to allow this, supply of vapour to the growth surfaces was modelled by solving Fick's law for the case of close space sublimation transport. Details of the modelling outcomes are reported in Ref. 16 and are discussed in Section 5.3.5.

5.3.4 Effect of deposition pressure and temperature on nanowire morphology

5.3.4.1 Pressure dependence. Fig 5.12a-d shows the effect that changing the nitrogen pressure (under which CdTe was sublimed) has on the morphology of the generated structures in the range 10 – 150 Torr at T_{source} = 550°C, T_{sub} = 520°C for 30 minutes. As the pressure was decreased a change from two-dimensional films to one-dimensional NWs was observed. For example, Fig 5.12a and b show rough but essentially two-dimensional films grown under 150 and 100 Torr of N_2 respectively; some of the original Au droplets remain visible on top of the film, but their density is much lower than before growth – this suggests either droplet evaporation, coalescence or burial. On the other hand Fig 5.12c and d shows that NW growth is encouraged by reducing the pressure to 25 and 10 Torr respectively; NW growth was most extensive for P = 10 Torr.

5.3.4.2 Temperature dependence. Results of subliming CdTe at source temperatures, T_{source} = 500 - 600°C, with the substrate held at T_{sub} = 490 - 540°C under 25 Torr of nitrogen for 30 minutes are presented in Fig 5.13 and 5.14 . Fig 5.13a – c show the effect that T_{source} (varied from 530 - 570°C) has on the morphology of generated structures, for a given T_{sub} (520°C) while Fig 5.13d shows a NW array grown using T_{source} = 600°C and T_{sub} = 550°C. The dependence of NW length on T_{source} is presented in Fig 5.14 for three different values of T_{sub} (490°C, 520°C and 550°C). Increasing T_{source} whilst keeping T_{sub} constant, led to the formation of denser arrays of longer NWs (Fig 5.13-c): For T_{source} = 530°C, the average NW length was 2 ± 0.3 μm, whilst for T_{source} = 570°C, it was 12 ± 1 μm. This trend is consistent for all values of T_{sub} (Fig 5.14). The experimental data was fitted with the diffusion-induced model of VLS NW growth discussed in Section 5.3.3.3, and once again there is a good agreement between experimental and theoretical data. By using a higher substrate temperature, T_{sub} = 550°C, NWs grew to greater lengths – some exceeding 30 μm when T_{source} = 600°C – and greater aspect ratios than for lower T_{sub} but the NW density was lower (Fig 5.13d). Successful NW growth was achieved here using substrate temperatures in the range 490 – 550°C, but not outside these limits.

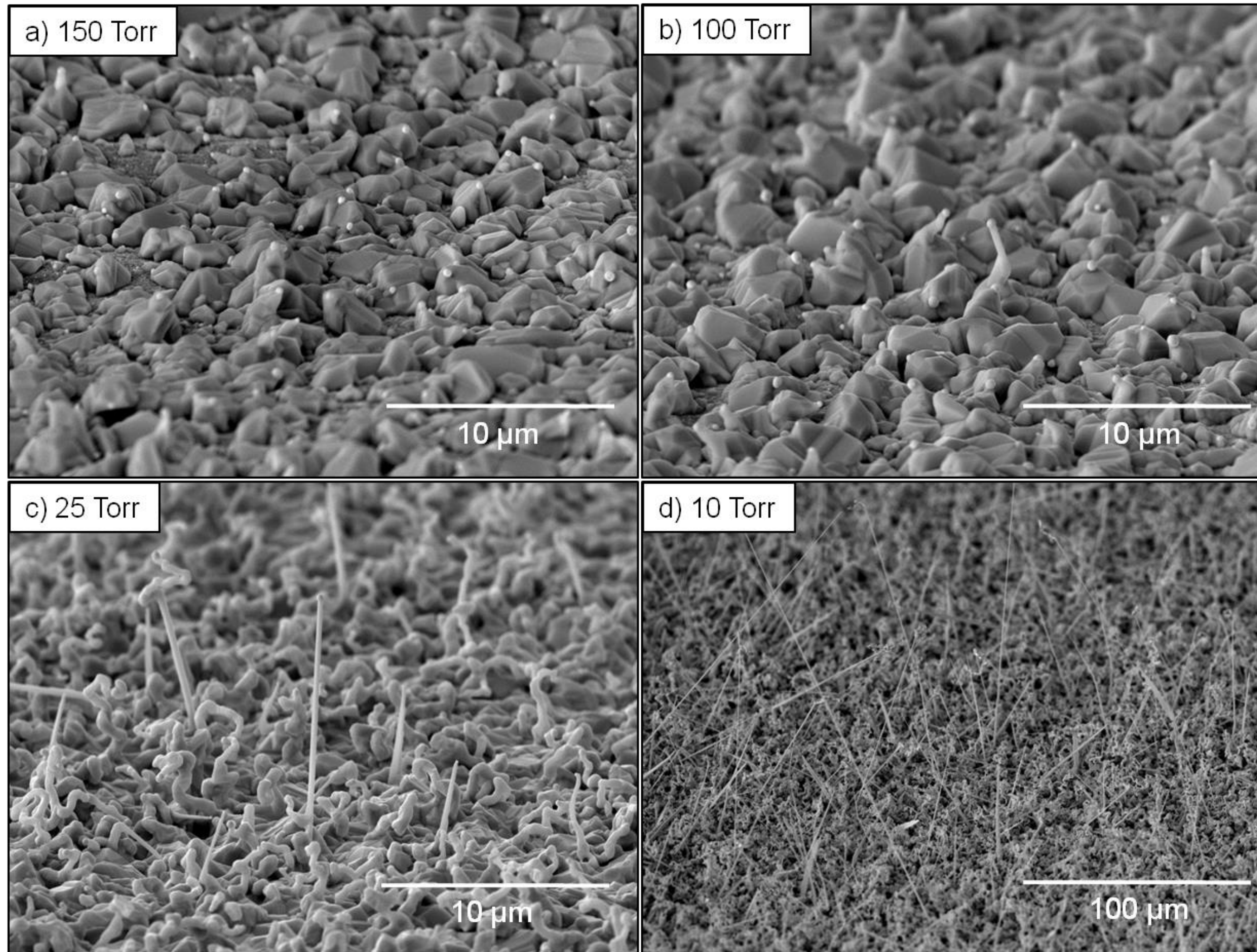

Fig 5.12: SEM images at 20° tilt of CdTe film/NW structures grown under a) 150 Torr, b) 100 Torr, c) 25 Torr and d) 10 Torr of N_2 for 30 minutes at T_{source} = 550°C, T_{sub} = 520

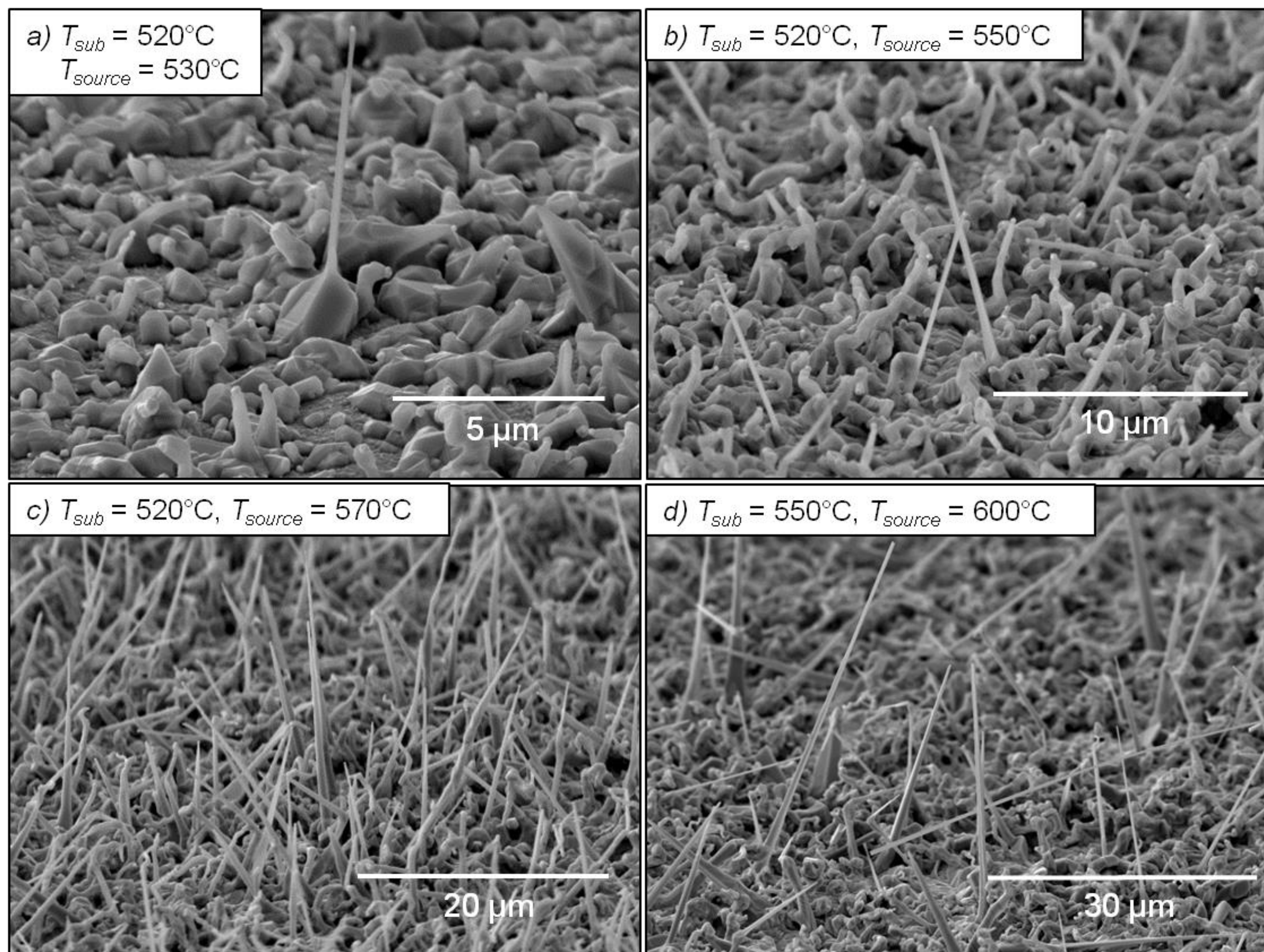

Fig 5.13: SEM images at 20° tilt of CdTe film/NW structures grown at different substrate temperatures, T_{sub}, and source temperatures, T_{source}. For all samples, the N_2 pressure and growth time were kept constant at 25 Torr and 30 minutes respectively.

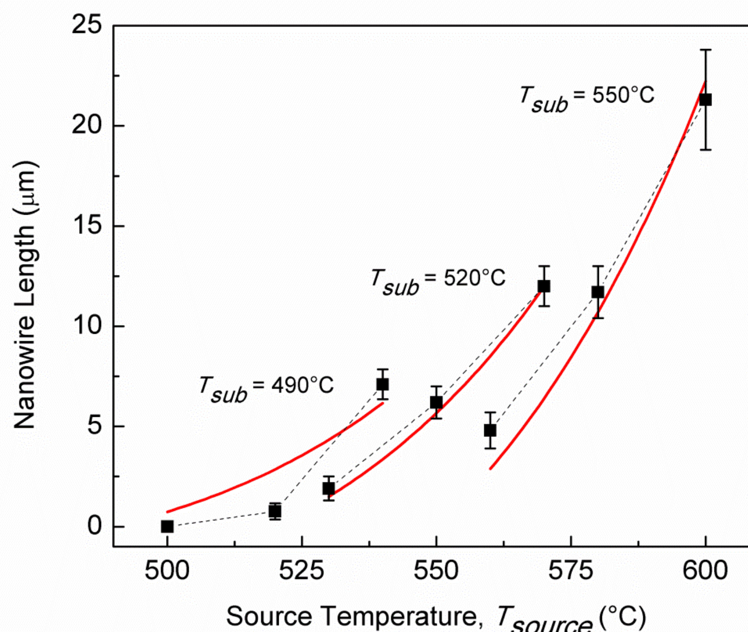

Fig 5.14: Experimental dependences of average CdTe NW length on the source temperature, T_{source} (500 - 600°C), at three different substrate temperatures, T_{sub} (490 - 550°C), obtained after 30 min of growth at P = 25 Torr (symbols). The theoretical fits (red-lines) were obtained using the diffusion-induced model of VLS NW growth.

5.3.5 Discussion of nanowire growth mechanism and morphological dependence on growth conditions

The mechanisms of CdTe NW growth are now discussed. Firstly, the evidence for the VLS mechanism itself is evaluated, followed by a more detailed discussion of the growth of the Au-CdTe system on Mo. Finally, the relationship between the morphologies of the structures and the growth conditions are explained with reference to the growth model.

5.3.5.1 Evidence for VLS mechanism. The observation of spherical droplets at the tips of NWs (Fig 5.3) is frequently used as confirmation that NW growth proceeded by the VLS mechanism[17-22]. However, this does not rule out the vapour-solid-solid (VSS) mechanism[23]. To discern between the two, one can analyse the composition of the droplet. For VSS grown NWs, major levels of semiconductor material (typically exceeding ~ 10 %) remain throughout the catalyst upon cool down[24], as the catalyst actually exists as a metal-semiconductor solid compound both during and after growth[25]. For VLS growth, typically only traces of semiconductor remain – the majority precipitates out, leaving a predominantly pure metal catalyst[26-28]. In this work SEM microanalysis showed that while the centre of a Au droplet was 100% Au, analyses from points close to the Au/NW interface (on both sides) showed major impurity levels of either CdTe in the Au or vice versa (see Fig 5.6d). However, these results

were influenced by the relative size of the generation volume (75 nm) and from the sample having inclined interfaces. Hence the significant finding is that the analysis point that was not subject to such sampling errors (scan 1, Fig 5.6d) indicates that the Au droplet is likely to be 100% Au: This is evidence that NWs grew by the VLS mechanism. Moreover, the droplets have a high aspect ratio and rounded shape whereas droplets on VSS NWs have a low aspect ratio and are faceted[29] and growth rates here are an order or magnitude greater than those typically observed for VSS growth[25, 30].

For VLS growth, semiconductor material may arrive at the catalyst either by direct adsorption or by surface diffusion of adatoms from the substrate (see Section 3.2.2). To identify which is the major contribution here, one must consider the relationship between NW length and NW diameter. Here, the thinner NWs grew to greater lengths (Fig 5.4) indicating that the diffusion of adatoms was the dominant contribution, as observed by Dubrovskii *et al*.[31] An adsorption-limited regime would have been inferred had the *thicker* NWs grown to greater lengths[32].

A significant observation for all NW arrays presented in this Section, that is atypical for VLS growth, is the presence of a semi-continuous thin-film of CdTe at the base of the NWs. Vapour-solid growth directly on the substrate is considered to be unfavourable in the model of VLS growth because the liquid surface of the catalyst has a larger accommodation coefficient[33] than the substrate. From time-dependent growth experiments (Fig 5.8), it was determined that this film grows prior to NWs, and that the NWs nucleate from the film itself. Indeed, there is a delay of NW growth.

5.3.5.2 A postulated mechanism for Au catalysed VLS growth of CdTe on Mo. Given that the VLS NW growth has the unusual feature of being preceded by the growth of a layer, the NW growth in this system is deemed to be atypical. In this section the evidence for the growth mechanism is collected and a mechanism consistent with it is postulated. The model must account for the following:-

1. The initial formation of NWs being suppressed in favour of the formation of a CdTe film.

2. Eventual VLS NW growth, which requires the formation of a liquid catalyst droplet.

With regard to condition 1 it is clear that one or both of the preconditions for VLS growth is/are not satisfied, these being: a) the presence of a liquid droplet; and b) its supersaturation with semiconductor material. Indeed, evidence from the melting points and solubilities of the materials involved indicates that at the growth temperature (520°C) there is initially no liquid phase present:

i) At the growth temperature Au, Mo, CdTe are all solid.[34, 35] Melting point suppression is not significant for Au for the sizes of particles in this work.

ii) The formation of Au-Mo and CdTe-Au compositions will not lead directly to liquid phases at 520°C[34, 35] - Mo has low solubility in Au (< 1%)[36] and the eutectic comprising Au-CdTe has a melting point in excess of 800°C.[35]

iii) Eutectics in the systems Au-Cd and Au-Te have melting points < 520° (the growth temperature), but they exist on the high Cd or Te sides of the phase diagram (see Fig 5.1a and b), therefore they would not be expected to form during the initial stages of growth.

With regard to condition 2, it is viable that the eventual formation of either Au-Cd or Au-Te liquid alloys accounts for the VLS NW growth observed here. Indeed, such binary liquid alloys have been demonstrated to be suitable catalysts for NW growth within other ternary systems, with Xian *et al.*[37] reporting the growth of GaAs NWs using Ga-Au droplets and Yazawa *et al.*[38] and Park *et al.* [39] each reporting In-Au catalysed InAs NWs. Moreover, considering that the eutectics are Te- and Cd-rich, a delay in liquid formation would be expected. Dhalluin[1] reported similar delays to NW growth, similarly attributing them to insufficient saturation.

For direct evidence as to which of Au-Cd or Au-Te is responsible for catalysing NW growth, in-situ EDX analysis of the droplet would be necessary. Ex-situ post-growth analysis of the droplet is insufficient since upon cool-down it is pure Au following precipitation of the remaining semiconductor material. Nevertheless, the likelihood of the formation of such binary compounds can be speculated based on the known information:

i) For $Au_{1-x}Te_x$ to be liquid at 520°C, x must exceed 0.5, whereas for $Au_{1-x}Cd_x$, x must exceed 0.65 (see Fig 5.1a and b).

ii) The Gibbs free energy, ΔG, of $AuTe_2$ at 520°C is – 13.7 kJ.mol^{-1}, whilst for AuCd it is ~ -17 kJ.mol^{-1} (the value being expected to be lower for $x > 0.5$).[40, 41]

Hence, whilst less Te must be incorporated than Cd for the droplet to become liquid, and whilst liquid phases of Au-Te exist at lower temperatures than for Au-Cd, on free energy grounds, one might expect a Au-Cd phase to form. However, a significant result was that presented in Fig 5.9, which shows a $CdMoO_x$ phase exists at the interface between the CdTe film and the Mo substrate, as confirmed by EDX and EELS. Evidently, there exists a residual MoO_x phase on the substrate prior to growth, with which Cd atoms mix to form a ternary phase. The author acknowledges the possibility that this phase may form late on in the growth process, but its existence implies the phase is thermodynamically stable therefore one expects that it forms immediately upon arrival of sublimed Cd and Te, especially considering that the

substrate temperature is already at a maximum at the onset of deposition. Indeed, in free energy terms, $CdMoO_4$ (ΔG = – 790 kJ/mol^{-1} at 520°C, extrapolated from data acquired in the range 714 - 760°C) is potentially more stable than CdTe (ΔG = - 138 kJ/mol^{-1} at 520°C).[42, 43] Hence, one could expect that during the initial stages of deposition, $CdMoO_4$ is formed on the substrate, leaving Te to diffuse to the Au droplet. A tentative model of growth that takes into account the evidence above is now postulated.

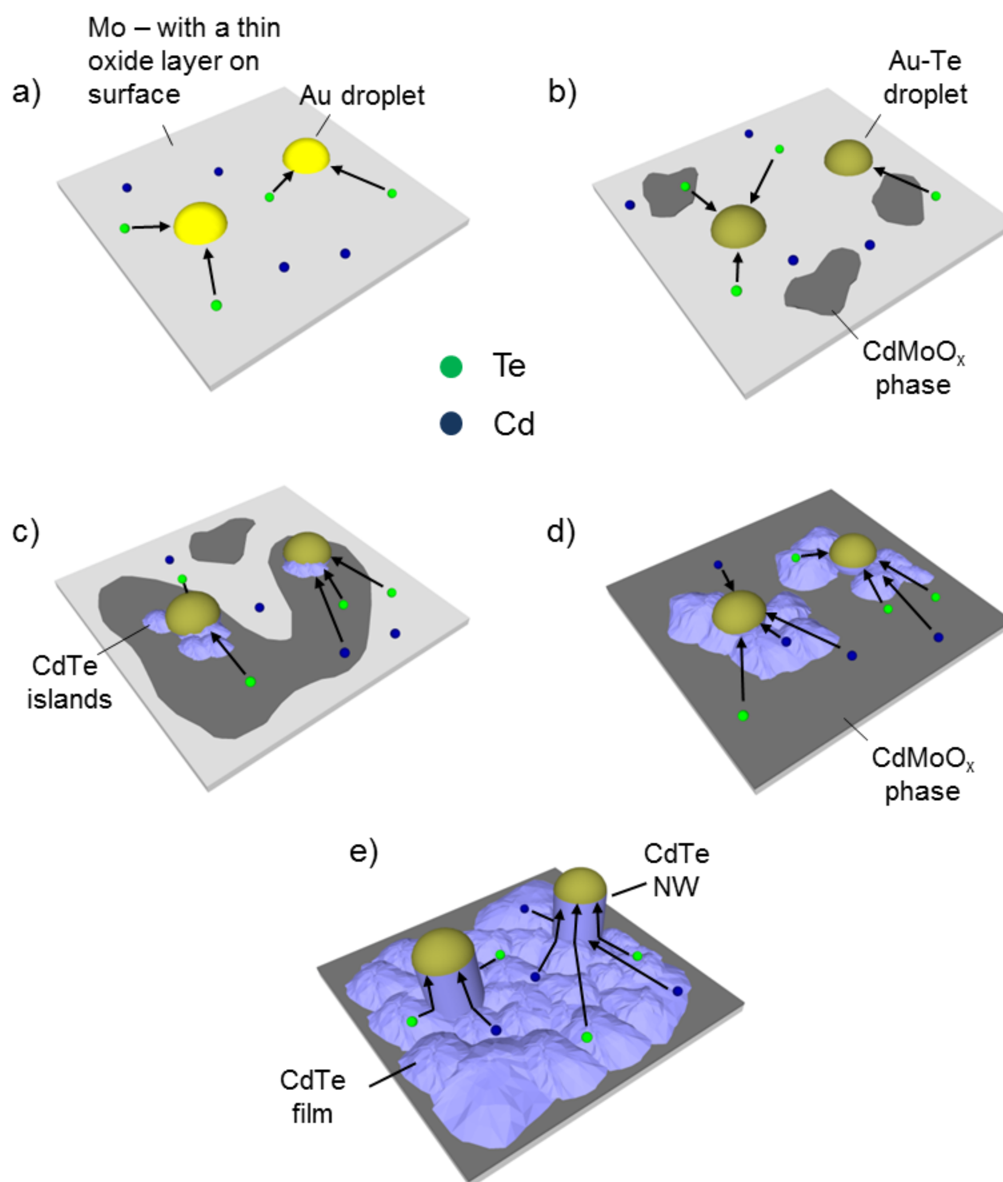

Fig 5.15: Postulated growth mechanism of CdTe NWs on Mo substrate. a) Arrival of Cd and Te adatoms: Te diffuses to droplet, Cd binds to MoO_x surface. b) $CdMoO_x$ islands grow and Au-Te liquid alloy droplets form. c) $CdMoO_x$ islands reach droplet and nucleation of CdTe occurs at the triple line. d) $CdMoO_x$ film is complete, CdTe islands grow and eventually coalesce, and VLS growth begins. e) CdTe thin film is complete and VLS NW growth becomes energetically favourable.

Step 1(Fig 5.15a): On arrival of Cd and Te adatoms at the Mo substrate, Cd atoms bind to the native MoO_x that exists on the substrate surface, forming $CdMoO_x$ and leaving Te free to migrate and dissolve in the Au particle.

Step 2 (Fig 5.15b): The $CdMoO_x$ islands grow across the substrate, and Te continues to diffuse to the droplets.

Step 3 (Fig 5.15c): As soon as $CdMoO_x$ islands reach a Au-Te droplet, the triple line (the interface between vapour, droplet and substrate) provides an ideal site for Cd and Te atoms to bind and nucleate CdTe islands (such islands, adjacent to the droplets, are observed in Fig 5.8a). Continued incorporation of Te into the Au droplets results in them becoming liquid.

Step 4 (Fig 5.15d): When the residual MoO_x layer is exhausted, $CdMoO_x$ formation stops, enabling Cd to diffuse to the CdTe islands or the droplets. The droplets are saturated with Te, which is a necessary condition for VLS growth. As soon as any Cd atoms diffuse into a Au-Te droplet, they bind with Te atoms and precipitate CdTe species at the liquid-solid interface, as per VLS growth. Consequently, NWs begin to develop alongside vapour-solid (VS) CdTe film growth.

Step 5 (Fig 5.15e): Neighbouring CdTe islands coalesce and eventually form an entire film, with liquid Au-Te droplets on. Surface diffusion rates of Cd and Te adatoms are now equal, and the system is now ideal for VLS growth: Diffusion of adatoms to the droplet is energetically favourable as the liquid surface of the droplet has a greater accommodation coefficient than the solid substrate [33]. Consequently, VLS growth dominates and steady state NW growth proceeds (leading to the film/wire morphologies observed in Fig 5.8b-d).

Ultimately, the length-time dependence presented in Subsection 5.3.3.1 is accounted for by the gradual incorporation of semiconductor material into the droplet and delayed formation of a liquid catalyst. The discrepancy between NW density (the highest achieved in the results presented in this Section being $10^6 – 10^7$ cm^{-3}) and estimated initial Au nanodot density ($10^8 – 10^9$ cm^{-3}) is to some extent a result of droplets being buried by the film during the early stages of deposition, an example of this being shown in Fig 5.9. Moreover, continued Au nanodot coalescence may occur during the period whereby the temperature is raised from the annealing temperature to the growth temperature - this typically takes ~ 2-3 mins (this also explains why the Au droplets catalysing NW growth are larger than those initially formed upon annealing of Au films).

5.3.5.3 Modelling outcomes and dependence of NW morphology on pressure and temperature. The agreement between the experimental data of NW length-time dependence and a theoretical model for diffusion-induced VLS growth is further evidence that the VLS

mechanism is responsible. The theoretical fits to the experimental data for elongation rate, dl/dt, and radial growth rate (see below), dR/dt, were given by Equations 3.6 and 3.7 respectively[14, 15]. To solve these equations in this case, values for the CdTe flux, J, from source to substrate were calculated using a model, developed by Dubrovskii[16], based on Fick's law, $J = -D_v(x)dN(x)/dx$, where D_v is the diffusion coefficient in the vapour and N is the vapour concentration at distance x from the source.

The radius-time dependence was also studied (Section 5.3.3.2). Whilst initially, the average NW radius remained constant for the first 40 mins of growth, thereafter, it increased with time (Fig 5.10); the increase was greatest at the bases of the NWs and they were tapered. Hannon *et al.* [44] attributed the tapering of Si NWs to a gradual reduction of catalyst size - via incorporation of catalyst material into the NW itself, evaporation of catalyst material or migration of catalyst. Here, the tapering is instead attributed to lateral growth[45] that occurs when the NW length exceeds surface diffusion lengths, and adatoms are unable to reach the catalyst. Indeed, the theoretical model of dR/dt, which takes into account the elongation *and* simultaneous lateral extension of NWs, agrees well with the experimental data (Fig 5.10). Useful kinetic parameters could be extracted from fitting the data in this case: The diffusion length of adatoms on NW sidewalls, λ, was 2 μm and the probability that adatoms stick to the sidewalls, τ_{inc}, was 0.61. Both of these values are consistent with the high extent of lateral growth that is frequently observed.

The pressure dependence of NW/film morphology - i.e. NW growth was only achieved at sufficiently low N_2 pressures (< 25 Torr) - may be explained as follows: for VLS growth to proceed, it is necessary for the droplets to be saturated with dissolved material. Such conditions are achieved when the flux of incoming material exceeds that of loss from the droplet (due to wire formation and re-evaporation). The rate of arrival of Cd and Te species at the catalyst tip is influenced by the pressure of N_2 which acts as a buffer gas. Indeed, in the model of CdTe NW growth[46], the diffusion flux, J, is inversely proportional to the pressure of the buffer gas, P. Under relatively high pressures of N_2 (e.g. 150 Torr), the arrival rate of semiconductor species is insufficient to saturate the droplet, and the conditions for VLS growth are not achieved. Even at long growth times planar growth dominates. Nevertheless for lower pressures (e.g. 25 or 10 Torr) VLS growth proceeds, as shown in Fig 5.12c and d.

The NW length increase with source temperature may be directly attributed to the associated increase in deposition flux, this being proportional to the difference between the vapour pressures at the source and substrate temperatures[16]. To explain the effect of T_{sub} on NW morphology (Section 5.3.4.2) one must consider the thermally activated nature of surface

diffusion. NW densities were lower when deposited at higher T_{sub} since at higher temperatures adatoms may diffuse to existing NWs rather than nucleate new NWs. Moreover, NWs of greater length and aspect ratio were yielded at higher T_{sub}, because lateral growth may be delayed at higher temperatures, as adatoms are able to diffuse up sidewalls of longer NWs.

Successful NW growth could not be achieved using substrate temperatures outside the 490 – 550°C range. The Au-Cd and Au-Te phase diagrams shows that at lower temperatures the Au droplets must incorporate even more semiconductor material for liquid catalyst to form: Evidently, when $T_{sub} < 490$°C in these experiments, this does not occur. On the other hand, at higher T_{sub}, it is necessary to use a higher T_{source} in order to effect transport. In these experiments $T_{source} > 600$°C caused very high deposition rates (> 1 µm/min for planar films) limiting control over structure morphology.

5.4 CdTe nanowires on polycrystalline CdTe films

Given that growth of CdTe NWs on Mo required the presence of a deposit of CdTe, in this Section growth directly onto a pre-deposited continuous CdTe film was investigated. This was achieved by forming Au catalyst droplets on a continuous sputtered CdTe film, e.g. CdTe/Mo, CdTe/ITO/glass or CdTe/glass (Section 5.4.2). The structure of the NWs was investigated by X-Ray diffraction (XRD) in Section 5.4.3 and results are discussed in Section 5.4.4.

5.4.1 Experimental procedure

The procedure for NW generation was as follows: 15 mm x 15 mm substrates were cut from 3 mm thick soda-lime glass and 100 µm thick Mo foil, and cleaned with isopropyl alcohol and DI-water. On some of the glass substrates, 200 nm thick In_2O_3:Sn (ITO) films were deposited by RF sputtering under 1 mTorr of Ar at 60 W, with the substrates held at 400°C. On Mo, glass and ITO/glass substrates, 1 µm thick CdTe films were RF sputtered under 10 mTorr of Ar at 70 W with the substrates held at 200°C. Au was evaporated to a thickness of 5 nm and then annealed at 360°C under 10 - 25 Torr of nitrogen for 30 mins – in-situ in the CSS chamber. CdTe was then sublimed at 550 - 570°C, under 10 - 25 Torr of nitrogen for 5 secs – 60 mins with the substrates held at 520°C.

For XRD analysis, three samples were prepared, these being: i) a 1 µm CdTe film on glass; ii) a Au/CdTe/glass stack annealed under 25 Torr of nitrogen at 360°C for 30 mins, and at 520°C for 1 min – this being intended to replicate the condition of the surface upon which NWs are grown (CdTe and Au films were grown by the same procedure as prior to NW generation); and iii) a NW array grown on CdTe/glass for 20 mins using T_{source} = 570°C and P

= 25 Torr. XRD measurements were carried out in the Bregg-Brentano geometry, texture coefficients and the degree of preferred orientation were calculated using the Harris method, and lattice parameters were calculated from (111) peaks using Bragg's law. (See Chapter 4 for a description of the Bragg-Brentano geometry and Harris method).

SEM images were recorded in secondary electron mode, with cross-sectional SEM images being prepared using the FIB-milling method (see Section 4.3.4). For the remainder of this thesis, growth of NWs from a pre-deposited CdTe film will be referred to as 'metamorphic growth', a term that is already used by the III-V community[47].

5.4.2 Results of nanowire growth on CdTe/Mo and CdTe/ITO/glass substrates

Secondary electron and backscattered electron images of a NW array grown on a CdTe/Mo substrate under 10 Torr of nitrogen, for 20 minutes at T_{sub} = 520°C using T_{source} = 570°C are shown in Fig 5.16a and b respectively. Fig 5.16c is an SEM image showing the result of subliming CdTe for 5 secs.

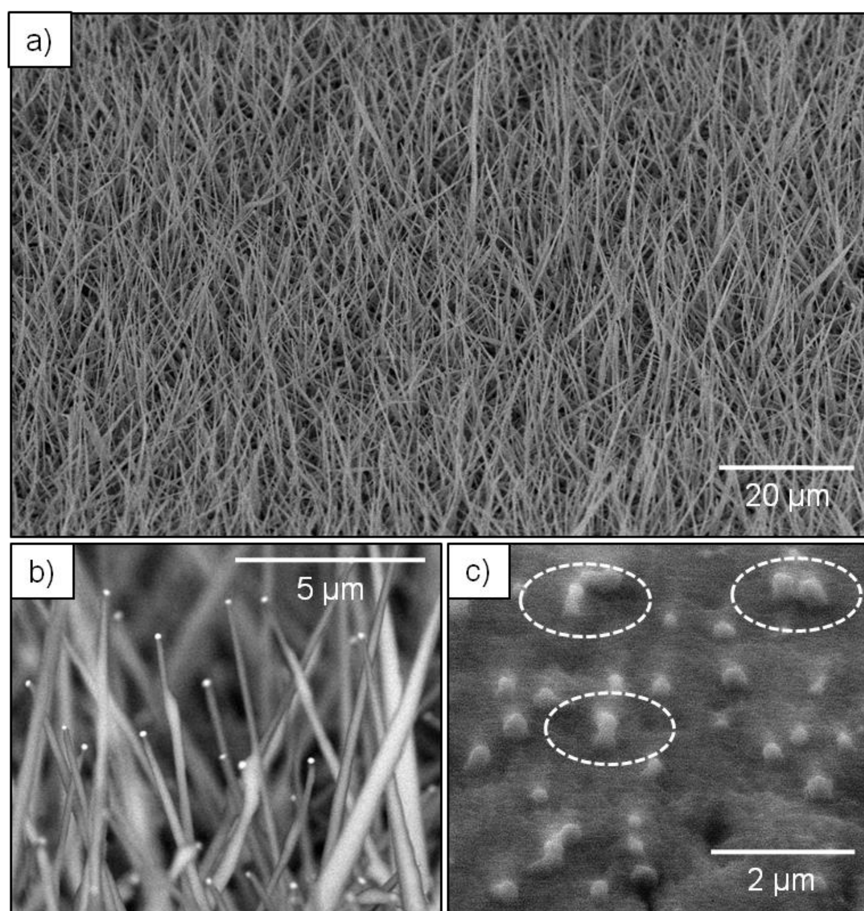

Fig 5.16: a) Secondary electron image and b) back-scattered electron image of a NW array grown on a CdTe/Mo film, i.e. by the metamorphic approach. NWs were grown at T_{sub} = 520°C and T_{source} = 570°C under 25 Torr of N_2 for 20 minutes. c) Secondary electron image of a sample grown for just 5 secs, with cases of immediate NW nucleation circled.

A plot of NW length as a function of deposition time, for NW arrays grown on CdTe/Mo substrates under 25 Torr of nitrogen, using T_{source} = 550°C is shown in Fig 5.17 - the data for NW arrays grown directly on Mo (taken from Fig 5.10) is included for comparison. Fig 5.18a shows a FIB-milled cross-sectional SEM image of a section of a NW array grown on a CdTe/ITO/glass substrate. Fig 5.18b is an enlarged view of the area highlighted in Fig 5.18a, showing a droplet buried within a CdTe film underneath the NWs, and Fig 5.18c shows the edge of a sputtered CdTe film, representative of those onto which NWs were grown.

As seen in Fig 5.16, NW arrays were successfully generated using the metamorphic approach, this representative example having been grown on a CdTe/Mo substrate. The NWs are similar to those grown directly on Mo; radii range from 50 – 500 nm, catalysts are present at their tips, there is an apparent random distribution of NW orientation, and some NWs taper from base to tip. The longest NWs exceed 20 μm in length. The catalysts were confirmed to be Au by EDX, and are clearly visible with bright contrast in the back-scattered image (Fig 5.16b). Some NWs contain kinks along their axis, i.e. the growth direction in which they propagate abruptly changes, this being investigated in greater detail later.

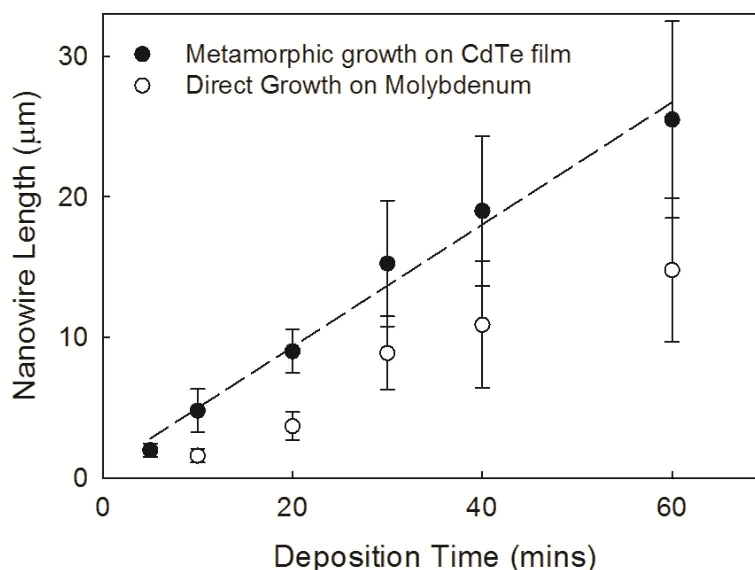

Fig 5.17: NW length as a function of sublimation time for growth on CdTe/Mo substrates (solid circles) and directly on Mo (open circles). Deposition was carried out under 25 Torr of nitrogen using T_{source} = 550°C, with the substrates held at 520°C. The dashed line shows a linear fit to the data.

Significantly however, the NW density (10^7 - 10^8 cm^{-2}, estimated from an average of measurements taken at different regions of the substrate) is at least an order of magnitude greater than the highest achieved for growth directly on Mo (10^6 – 10^7cm^{-2}). Moreover, NW nucleation was achieved more readily on CdTe/Mo substrates; Fig 5.16c shows that some Au

droplets (circled) nucleate CdTe NW growth after just 5 secs of deposition. Indeed, the plot of NW length as a function of time (Fig 5.17) implies there is no delay to NW growth when using this metamorphic approach. The length-time dependence is linear throughout the range 0 - 60 mins. After 10 minutes, the average NW length on a CdTe/Mo substrate was 4.8 ± 1.6 μm, whereas on Mo substrates it was just 1.6 ± 0.5 μm. From the linear fit, a constant growth rate of 0.45 ± 0.05 μm/min was determined for metamorphic growth.

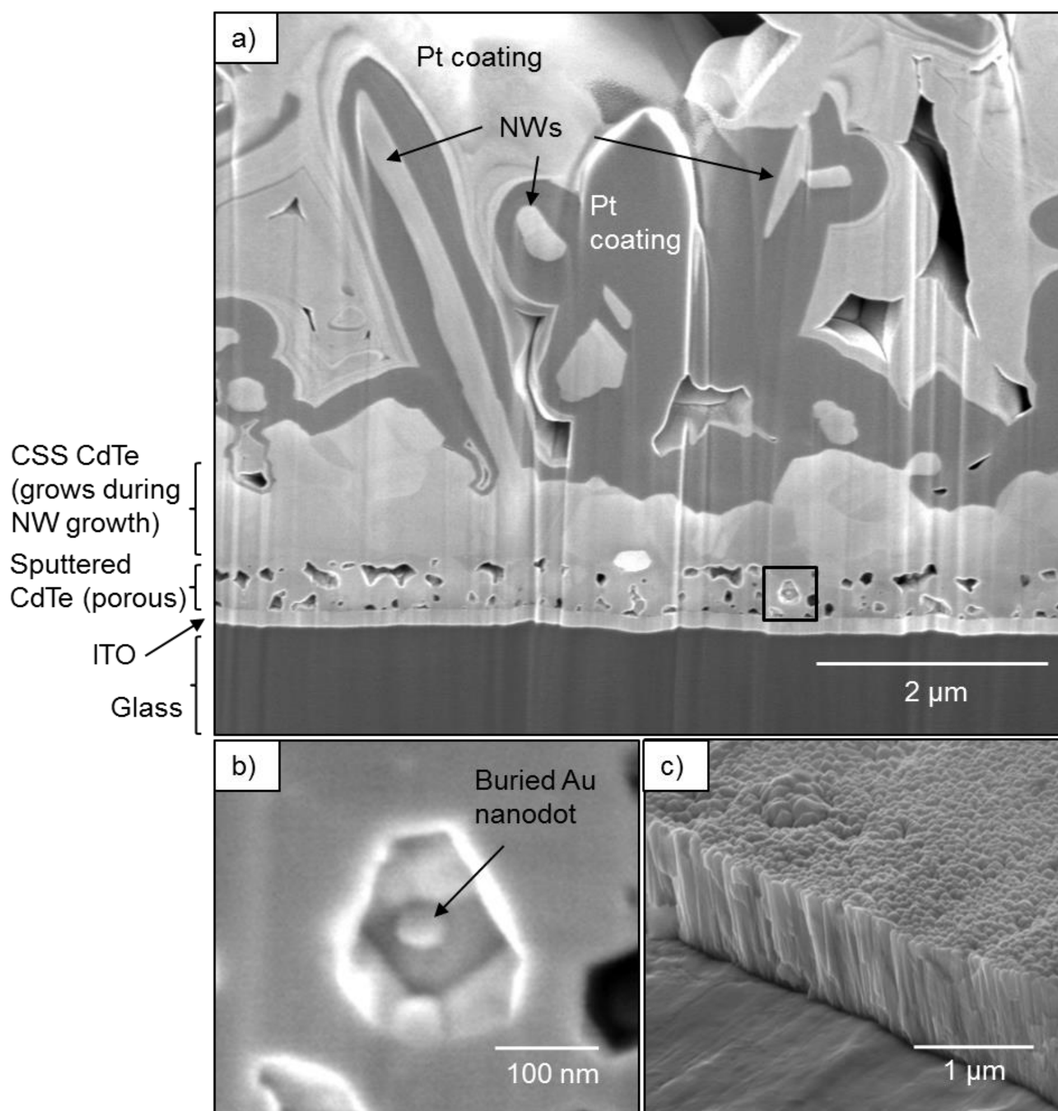

Fig 5.18: a) FIB-milled cross-section of CdTe NWs deposited on a CdTe/ITO/glass substrate. The area of dark contrast surrounding the NW is a layer of protective Pt, deposited as part of the milling process. See the text for a detailed description of the features. b) An expanded view of the region highlighted in a) that shows a Au droplet buried underneath planar CdTe. c) An SEM image of an as-grown sputtered CdTe film, which consists of densely packed pillar-like grains.

NW growth was also successfully achieved on both CdTe/glass and CdTe/ITO/glass substrates. The features observed in the cross-sectional image of a representative example of a NW array grown on CdTe/ITO/glass (Fig 5.18a) are now described. The region of dark contrast at the bottom of the image is the glass substrate, and above this, there is a 200 nm film of ITO. The porous region is the ~ 1μm thick sputtered CdTe film. On top of the sputtered CdTe, there lies both planar sublimed CdTe, and CdTe NWs. In this cross-sectional plane, a large proportion of one NW is observed (including the base), as are sections of other NWs (labelled) which do not lie in the cross-sectional plane. Around the NWs, the region of dark contrast is the Pt coating, deposited prior to FIB-milling as a protective layer. The region of lighter contrast at the top of the image is the free surface of this Pt. Close examination of the base of the complete NW reveals that it nucleates from the sputtered CdTe film, and not the sublimed CdTe material, this being determined from the crystallographic contrast.

Within some of the visible pores in the sputtered CdTe film lie droplets of material (confirmed to be Au by EDX), as seen in Fig 5.18. These pores are not observed in as-grown sputtered CdTe films (Fig 5.18c), which consist of densely packed columnar grains < 50 nm in diameter.

5.4.3 Investigation of nanowire growth orientation

The XRD spectra for an as-grown CdTe/glass stack, an annealed Au/CdTe/glass stack and a NW array grown on Au/CdTe/glass are shown in Fig 5.19; the texture coefficients and degrees of preferred orientation are listed in Table 5.1 and the lattice parameters in Table 5.2.

First, the XRD spectra are described. For all samples, (111) is the most dominant orientation, but the *degree* of preferred orientation varies between samples. Both of the CdTe film samples (before and after annealing) are highly (111) oriented. (There are weak peaks from (220) and (511), the latter being the twin orientation to (111)). In contrast, the orientation of the CdTe NW sample is more random, with increases of the (220), (311), (400), (331) and (422) planes being observed, accompanied with a decrease in the (111) peak and the degree of preferred orientation: The texture coefficient of the (111) peak was 4.58, 4.88 and 2.74 for films a, b and the NWs respectively, whilst the degree of preferred orientation was 1.53, 1.66 and 0.85 (Table 5.1).

The lattice parameters for the as-grown CdTe film, annealed CdTe film and the NW array, calculated from using the position of the (111) peak, are listed in Table 5.2. Because of the lack of peaks, a Nelson-Riley plot was not possible. The lattice parameter of the CdTe film and annealed film (6.50 ± 0.20 Å and 6.51 ± 0.02 Å respectively) are greater than the reported bulk value (6.482 Å), whereas that of the NWs (6.481 ± 0.02 Å) agrees with the bulk value[48].

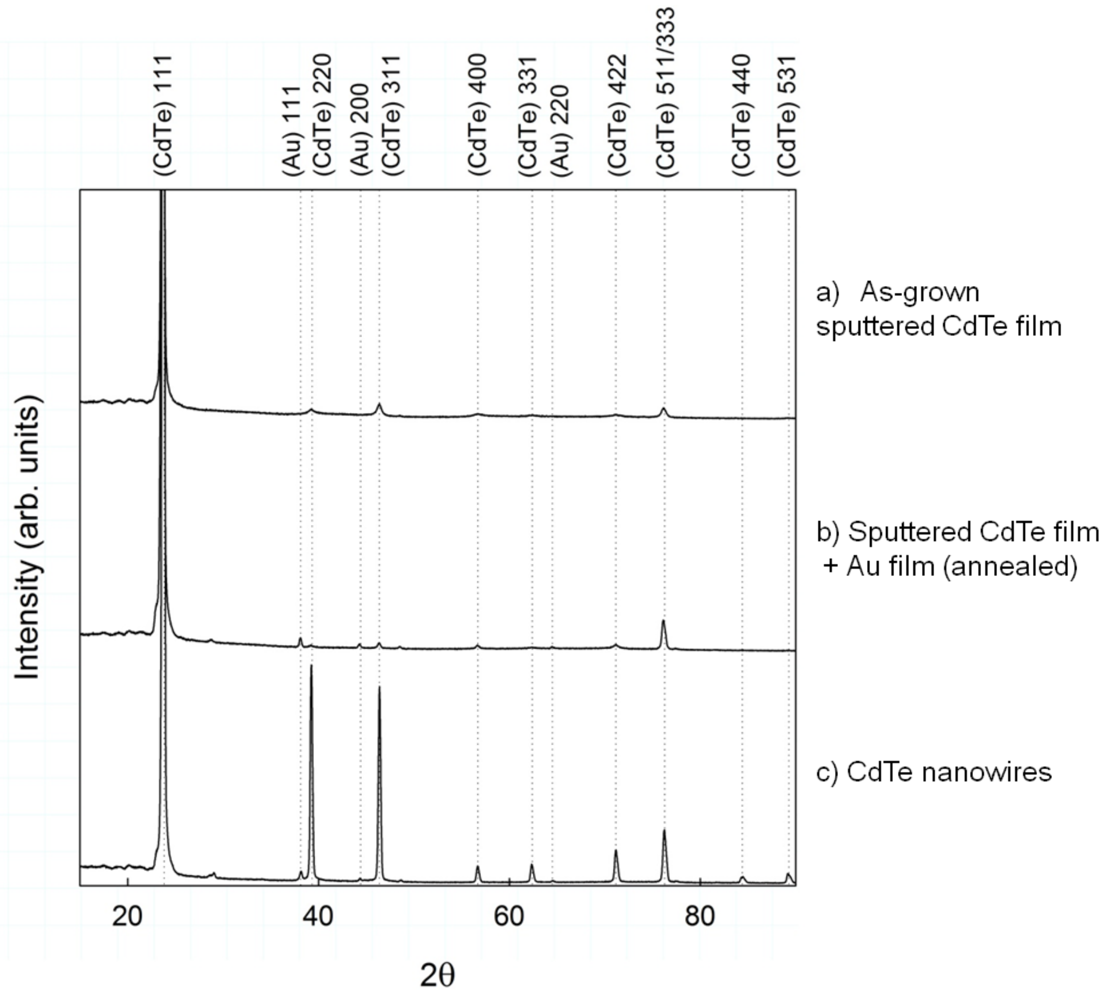

Fig 5.19: XRD spectra of a) as-grown sputtered CdTe film, b) a stack of 5 nm Au/sputtered CdTe annealed at 360°C for 30 mins and then at 500°C for 1 minute, and c) CdTe NWs.

Table 5.1: Texture coefficients, C_{hkl}, and degree of preferred orientation, σ, at various stages of NW generation.

Sample	C_{111}	C_{220}	C_{311}	C_{400}	C_{331}	C_{422}	C_{511}	σ
CdTe film	4.58	0.07	0.21	0.40	0.23	0.25	1.19	***1.53***
CdTe film + Au (annealed)	4.88	0.02	0.05	0.21	0.10	0.13	1.22	***1.66***
CdTe NWs	2.74	0.47	0.85	0.50	0.28	0.45	1.79	***0.85***

Table 5.2: Lattice parameters, calculated from the position of the (111) peak for CdTe film, annealed film and CdTe NWs. Bulk value taken from Ref. 48.

Sample	**(111) Pos. (2*θ*)**	***a*** **(Å)**
CdTe film	23.69	6.50 ± 0.02
CdTe film + Au (annealed)	23.67	6.51 ± 0.02
CdTe NWs	23.76	6.48 ± 0.02
Bulk Value		6.482

Fig 5.20 shows NWs that have been mechanically removed onto a Si substrate. The highlighted NW has a distinct kink along its length, with an angle of 111° indicating an abrupt change of growth direction. This kinking behaviour is commonly observed in all NW samples.

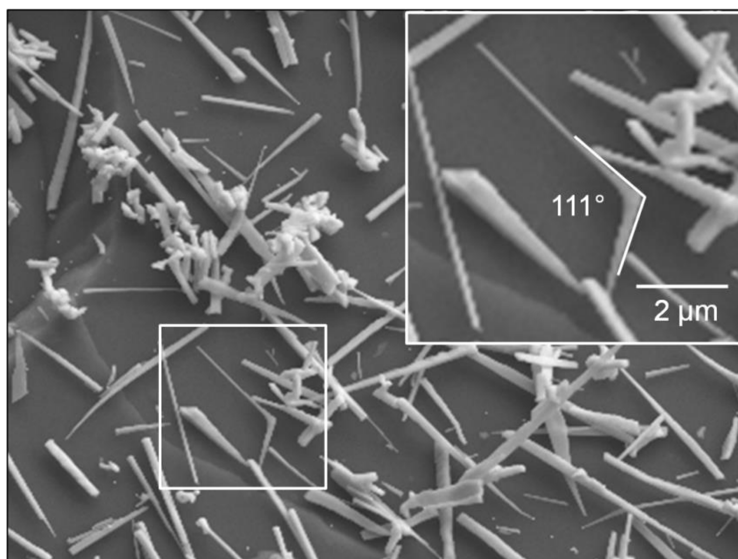

Fig 5.20: NWs mechanically removed onto a Si substrate. Inset: An enlarged view of the highlighted NW shows it kinks with an inner radius angle of 111°.

5.4.4 Discussion of growth mechanism for metamorphic growth and of nanowire orientation

First, the mechanism of NW growth on polycrystalline CdTe films is discussed in order to explain the differences relative to growth directly on Mo. Second, the non-vertical and apparently random orientation of NWs with respect to the substrate is discussed with reference to the XRD data. Finally, in light of the results, the advantages of metamorphic growth, with reference to the development of NW solar cells, are evaluated.

5.4.4.1: Growth mechanism: NW growth on CdTe/Mo, compared to directly on Mo substrates (Section 5.3), differed in that: a) the NW density increased by ×10; and b) that

growth proceeded without delay (< 5s compared to > 5 mins). This behaviour may be attributed to the more ready formation of liquid droplets. Regardless of whether Au-Cd or Au-Te is responsible for NW growth, the liquid phase is more readily achieved for Au droplets that lie on CdTe films than for Au droplets on Mo, since the former can absorb semiconductor material from both the vapour *and* the underlying film, whereas the latter may only absorb material from the vapour (in both cases, 'material from the vapour' includes atoms arriving directly at the droplet and adatoms that have been deposited onto the substrate and subsequently diffused to the droplet).'

This also accounts for the increased NW density: Solid droplets may be buried by CdTe film growth and do not nucleate NWs, therefore the more ready acquisition of liquid droplets should result in a lower proportion of them being buried. However, Fig 5.18b shows that even for metamorphic growth, some droplet burial occurs, as there is still some planar CdTe growth. The NW density achieved (10^7 – 10^8 cm^{-2}) therefore falls short of the density of catalyst droplets (10^8 – $10^9 cm^{-2}$) achieved by annealing 5 nm Au films at 360°C – due to droplet burial and possibly due to continued droplet coalescence.

5.4.4.2 NW orientation and lattice parameter: The results presented in Subsection 5.4.3 are now discussed in terms of explaining the apparent random orientation of NWs, which was observed for all cases of NW growth presented in this Chapter.

The reduced degree of preferred orientation - determined from XRD spectra (Fig 5.19 and Table 5.1) - observed for NW arrays, relative to the substrates upon which they were grown, implies either that: a) the NW growth on the substrate is not epitaxial; or b) the underlying substrate of the NW array sample has undergone recrystallisation prior to NW growth, and has templated epitaxial growth of NWs in a variety of crystallographic directions. Firstly, the postulation that growth is non-epitaxial is discussed. If the CdTe substrate remained (111) oriented, and NWs grew epitaxially, then NWs could legitimately still have grown in non <111> directions; a [112] wire would be inclined to the substrate normal by 33°66' for example. However, as the θ-2θ arrangement only detects reflections from planes that are parallel to the surface, then the reflection detected from a [112] NW would *still* be from its (111) planes that remain parallel to the substrate surface. The resultant XRD spectra in this case would match that of the substrate, i.e. be highly oriented, which it does not, hence the implication that growth is non-epitaxial.

Secondly, the suggestion that the sputtered CdTe film undergoes recrystallisation prior to NW growth is discussed. As the texture coefficient of the (111) plane, C_{111}, and the degree of preferred orientation, σ, of the annealed CdTe film (at 360°C for 30 mins and 520°C for 1

minute) were comparable to the as-grown film (grown at 200°C), it can be assumed that recrystallisation had not taken place at the point immediately prior to CdTe sublimation. However, it may have occurred during CSS deposition, with the substrate held at 520°C for 20 minutes; although this would only affect any NWs that nucleate later within the deposition period. It is important to note that X-rays could in principle sample both the NWs and the underlying film however. In contrast to these results, Moutinho *et al.* report recrystallisation of RF sputtered CdTe upon annealing at 400°C for 30 minutes – inferred from AFM and XRD data[49]. However, Moutinho's films were grown at a lower temperature than these, and annealing was carried out in air rather than nitrogen. Moreover, Moutinho's annealing included $CdCl_2$; Cl being known to accelerate microstructural changes in CdTe. Indeed, without the use of $CdCl_2$-activation, higher annealing temperatures (500°C) are typically required to induce recrystallisation, as shown by Paudel *et al.*[50].

Evidently, these XRD results cannot unambiguously distinguish between the two postulates. Nevertheless, the presence of voids in the sputtered layer of an equivalent NW sample, shown in Fig 5.18a, could be indicative of recrystallisation. Moreover, the lattice parameter, calculated from (111) peak positions, is smaller for the NW sample, and more comparable to the bulk value, than for the two film samples. Depending on whether the main contribution to the XRD data was from the NWs or the film, this may imply either: a) recrystallisation of the underlying film (only after high temperature sublimation) or merely that the film undergoes strain relaxation; or b) the NWs have a smaller lattice parameter compared to the films. Indeed the lattice parameter of the films is higher than the accepted bulk value, which indicates they are under compressive stress, whereas NWs possess additional degrees of freedom compared to thin films, due to a high surface to volume ratio, which enables them to relieve stress more effectively, as described in Section 3.3.3.

Kinking of the NWs, as shown in Fig 5.20, also makes a minor contribution to the distribution of observed orientations. The example shown has an external angle of 111°, which is comparable to the angle of 109° expected for a $\Sigma = 3$ twin involving the [111] and $[1\bar{1}1]$ directions (where Σ is the 'Friedel index', defined as the ratio of the number of lattice sites in either of two adjacent grains to the number of coincidence sites for the two interpenetrating lattices). In some cases, NWs kinked so that they would propagate back down towards the substrate, which could be explained by a change from a [111] to a $[\bar{1}\bar{1}1]$ growth direction.

5.4.4.3 Advantages of metamorphic growth for the design of NW solar cells. There are numerous advantages of using the metamorphic approach of growing CdTe NWs for PV devices. Firstly, it results in the formation of a continuous absorber layer consisting of a thin

film and NWs, which provides electrical continuity and prevents short circuiting in the device. Whilst depositing directly on Mo also forms a film, it is discontinuous and there is poor thickness control. Secondly, the metamorphic approach yields an immediate nucleation of NWs (i.e. more reliable control over NW length) and an enhancement in the NW density.

This approach can be replicated on other substrates other than Mo, as demonstrated on CdTe/glass and CdTe/ITO/glass (Fig 5.18a). As the NWs nucleate from the CdTe film, the only requirement for the substrate is that CdTe films can be grown uniformly on them and that they adhere to them. This is extremely significant with regards device fabrication as it enables the selection of a variety of conductive substrates, and subsequent optimisation of the back contact of a device, without the need to re-optimise NW growth conditions. Even highly complex thin film stacks, designed to create an Ohmic back contact, or electron back reflectors, may be integrated between the substrate and the CdTe film, provided they do not subsequently degrade at the NW growth temperatures (500 – 550°C).

However, NW density is still not fully optimised with this approach (i.e. not all Au nanodots catalyse NW growth), and additional VS planar growth still occurs. Nevertheless, the metamorphic approach was used for NW generation in the remainder of this work: a) growth of core-shell heterostructures (Section 5.5); b) NW and core-shell characterisation (Chapter 6); and c) fabrication of NW solar cells (Section 7.5).

5.5 Core-shell hetero-nanowire growth

In this Section, the generation of core-shell CdS/CdTe and $Cd_{0.9}Zn_{0.1}S$/CdTe hetero-nanowires on CdTe/Mo substrates is reported - $Cd_{0.9}Zn_{0.1}S$ has a wider band gap than CdS and its use in full devices may reduce window layer absorption loss. Three different techniques - CBD, MOCVD and RF sputtering – were used to deposit the sulphide coatings onto CdTe NW arrays. The suitability of each of the deposition techniques for generating conformal shells is evaluated. Moreover, the formation of core-double shell ITO/CdS/CdTe hetero-nanowires on CdTe/Mo substrates is also presented, with the ITO layer being sputter-deposited. Completion of the desired ITO/CdS/CdTe(NW)/CdTe/Mo solar cell architecture, described in Chapter 1, was therefore demonstrated, enabling the devices to be fabricated that are reported in Chapter 7.

5.5.1 Experimental procedure

CdTe NWs were grown by the metamorphic approach, as described in Section 5.4, i.e. on 1 μm CdTe films on Mo using T_{source} = 570°C, T_{sub} = 520°C, under a nitrogen pressure of 10 Torr, for 10 minutes. The growth conditions of the sulphide coatings were:

i. CdS by CBD: Solution growth of CdS was carried out at 67°C for 20 mins, and samples were then rinsed in DI water (see Section 4.2.3 for the CBD recipe).

ii. $Cd_{0.9}Zn_{0.1}S$ by MOCVD: Growth was conducted with the substrate held at 360°C for 15 – 30 mins. The precursors employed were dimethylcadmium (DMCd), ditertiarybutylsulphide (DtBS) and diethylzinc (DEZn). See Section 4.2.4 for a more detailed description of MOCVD growth.

iii. CdS by MOCVD: The same process as above was used, but without the diethylzinc precursor.

iv. CdS and ITO by RF Sputtering: CdS deposition took place for 120 mins in an Ar pressure of 5 mTorr, with the substrate held at 200°C, using an RF power of 60 W. ITO was then sputtered from a target with 5% SnO_2 using 70 W RF power and 1 mTorr of Ar, with the substrate at 250°C, for 150 minutes.

The results were evaluated by SEM and TEM. For TEM, NWs were mechanically removed onto Cu grids. Cross-sectional SEM images of individual core-shell NWs were obtained by removing NWs onto a Si substrate, coating them with a protective layer of Pt and then FIB-milling.

5.5.2 CBD growth of CdS shell

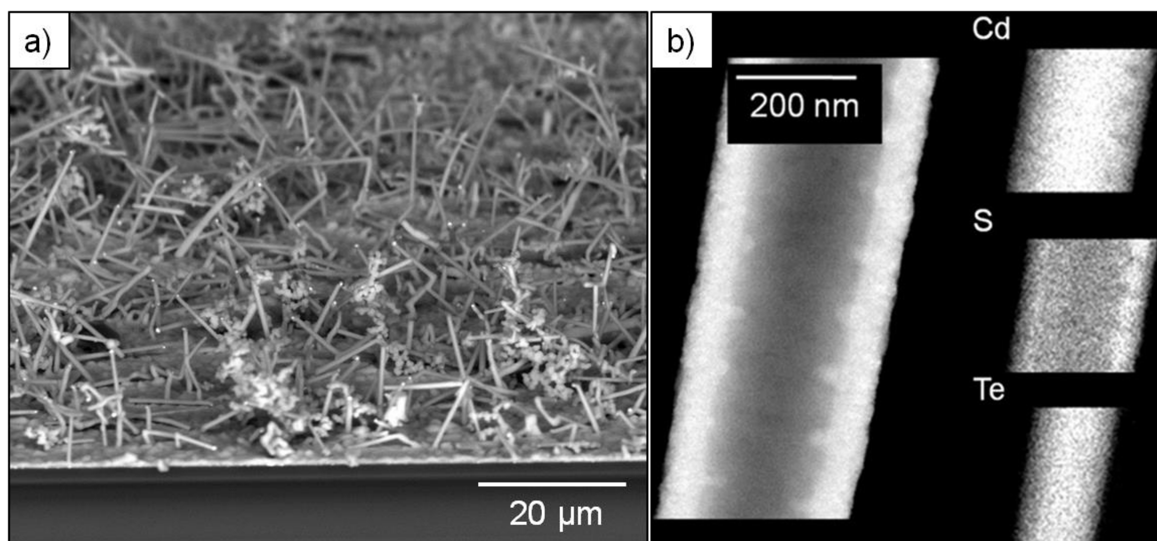

Fig 5.21: a) Secondary electron image of collapsed NWs following CBD-CdS process. b) Dark-field TEM image of a single core-shell CdS(CBD)/CdTe nanowire and EDX mapping of its constituent elements.

A secondary electron SEM image of a NW array on a CdTe/Mo substrate after CBD deposition of CdS is shown in Fig 5.21a , and a dark field TEM image of an individual core-

shell CdS/CdTe NW, accompanied with EDX elemental mapping of the constituent elements, is shown in Fig 5.21b. Whilst the TEM analysis confirms that a highly uniform CdS shell of ~ 40 nm was generated, it is evident that the solution growth caused both widespread damage to the NWs, collapsing many of them onto the substrate, and the deposition of unwanted agglomerates of CdS nanocrystals between them.

5.5.3 MOCVD growth of CdZnS and CdS shells

Fig 5.22a and b show representative examples of CdZnS/CdTe NWs onto CdTe NWs following MOCVD growth for 15 and 30 minutes respectively. The generated structures are dendritic, with rows of 'secondary NWs' growing from the CdTe NW, perpendicular to its axis. A high-resolution TEM of these is shown in Fig 5.22c with a fast Fourier transform shown inset. Representative examples of NWs coated with CdS by MOCVD, and subsequently removed onto a Si substrate are shown in Fig 5.22d.

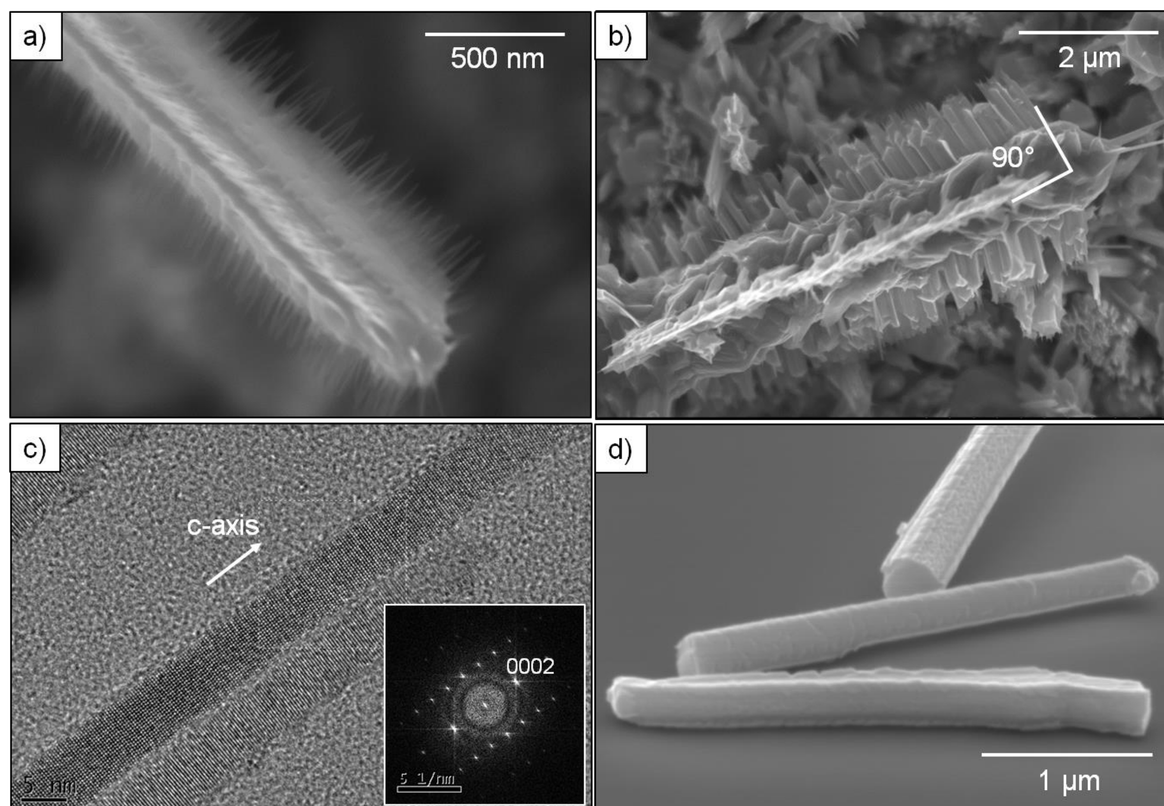

Fig 5.22: SEM images of NWs coated with CdZnS by MOCVD for a) 15 mins and b) 30 mins show the dendritic morphology of the shell layer, i.e. a second generation of NWs are generated, growing perpendicular to the primary CdTe NW axis. c) An HRTEM image of the secondary NWs with fast Fourier transform inset. d) SEM image of CdTe NWs coated with CdS by MOCVD, that have been removed onto a Si substrate. No secondary NWs were formed, but the coating is nevertheless non-uniform.

First, the CdZnS/CdTe NWs are described. There was no observable damage inflicted to the CdTe NWs, but the generated coatings are highly non-uniform. Whilst there exists a thin polycrystalline shell wholly around the NW (this being most clear in Fig 5.22b), the larger extent of the deposit grows as a second generation of NWs, propagating at 90° from the primary NW axis. These secondary NWs appear to be constrained to certain axes themselves, presumably crystallographically patterned by the faceted sidewalls of the primary NW. This is more evident on the NW shown in Fig 5.22b, for which the deposition time (30 mins) was twice as long as the NWs shown in Fig 5.22a. Moreover, the secondary NWs are more pillar-like after a longer period of growth, i.e. their diameter is greater. The number of secondary NW growth axes observed varied from wire to wire; in some cases there were 3 rows of secondary NWs, in other cases there were 4 or 6.

TEM analysis of the secondary NWs shows that they are single crystal, of wurtzite phase, and grow along the c-axis (Fig 5.22c, fast Fourier transform inset). The separation of lattice fringes perpendicular to growth is 3.2 ± 0.1 Å, and parallel to growth is 3.2 ± 0.1 Å, corresponding to the (0002) and ($10\bar{1}0$) planes. From these, lattice constants were calculated as c = 6.4 ± 0.2 Å and a = 3.7 ± 0.1 Å, these values being similar to those reported for bulk wurtzite ZnS; c = 6.26 Å and a = 3.82 Å (see JCPS card, No 89-2942). Wurtzite CdTe and CdS on the other hand have much higher lattice constants and so it is inferred that these structures are ZnS – this being supported by the observation that secondary NWs did not grow when the diethylzinc precursor was removed (see below). Although a low Zn:Cd ratio was used (1:9), these secondary NWs only constitute a small volume of the deposited shell. No catalysts particles were present at the tips of any of the secondary NWs analysed.

Secondly, the CdS/CdTe NWs are described. Without the use of diethylzinc precursor in the deposition process, no secondary NWs were formed, and a non-continuous coating of CdS was found on the CdTe NWs. This anisotropic growth is displayed in Fig 5.22d (NWs here were mechanically removed onto Si), most evidently for the top and bottom NWs shown, for which the shell appears to be thickest on their top and bottom edges.

5.5.4 RF sputtering of CdS and ITO shells

Fig 5.23 shows the results of sputter-depositing CdS and both CdS *and* ITO layers onto CdTe NW arrays grown on CdTe/Mo substrates. Fig 5.23a shows an array of NWs and Fig 5.23b shows the tip of an individual NW following sputter deposition of CdS. Images of FIB milled cross sections, of core-double shell ITO/CdS/CdTe NWs are shown in Fig 5.23c and d.

Following sputter coating of CdS the NW arrays remained intact (Fig 5.23a). Moreover, the NWs were completely coated with CdS, both radially around the NW and longitudinally

along the NW axis – no visibly bare regions were observed. However, there was some evidence of shadowing occurring, as towards the base of some tilted NWs, the thickness of the shell on the underside of the NW appeared to be thinner than on the top side. Sputter deposition of ITO also coated the NWs completely. Elemental contrast in the cross-sectional images of the core-double shell structures show that the core and shell regions are well defined. Fig 5.23c shows an example of a NW coated uniformly; the CdTe core is ~ 200 nm in diameter, and the CdS and ITO shells are ~ 200 nm and ~ 100 nm thick respectively. However, the uniformity of the shells was inconsistent, as shown in Fig 5.23d. Here, the CdS and ITO shells are much thicker on one side of the NWs than the other.

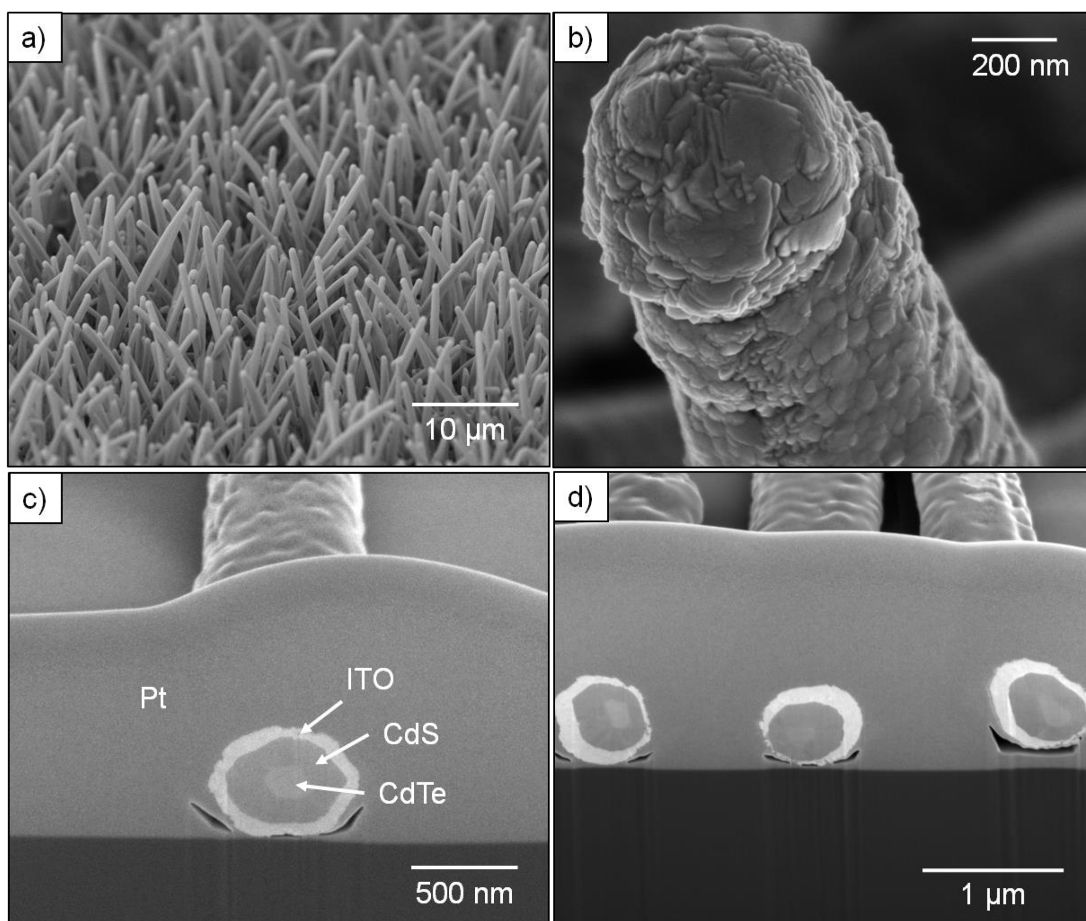

Fig 5.23: SEM images of core-shell structures generated by sputtering of CdS and ITO/CdS onto CdTe NWs. a) and b) CdS coated CdTe NWs. The CdS layer is rough and covers both the NW and catalyst tip (b). c) and d) Sputtered double-shells of ITO and CdS on CdTe NWs. The shell structures were frequently non-uniform. The images are of FIB-milled cross-sections, with the NWs having been held in place on a Si substrate by Pt.

5.5.5 Discussion

The suitability of each of the deposition methods for the generation of shell coatings is now discussed, as are the details of some of the structures observed.

CBD is considered to be unsuitable for shell growth due to the damage the process inflicted on the NW arrays, despite its ability to generate highly uniform coatings.

MOCVD is also considered to be unsuitable due to the highly non-uniform growth of both CdZnS and CdS. The dendritic morphology of the CdZnS growth is undesirable within the context of the NW solar cell (described in Chapter 1), and whilst CdS deposition did not yield dendritic growth, it failed to completely coat the CdTe NWs, leaving bare regions – this would result in shunts in a solar cell.

Nevertheless, the nature of the secondary NWs, observed for CdZnS growth, is now discussed. Most notably, the removal of the Zn from the growth procedure quenched secondary NW growth, which implies that Zn may be responsible for their nucleation. Indeed, the hexagonal lattice constants of these structures, obtained from TEM analysis, agreed with reported values for ZnS. Although ZnS typically adopts the zinc-blende phase at low temperature, wurtzite phase ZnS NWs have indeed previously been grown at just 180°C by hydrothermal synthesis - growing preferentially along the c-axis, catalyst free [51]. They have also been VLS-grown by pulsed laser vaporization at 950°C using Au catalysts [52]. Here, the absence of catalysts at the secondary NW tips suggests the VLS mechanism was not responsible.

It is likely that the secondary NW growth was crystallographically driven, as they are arranged in a number of distinct rows around the NW circumference – either 3, 4 or 6 rows. As the primary CdTe NWs adopt different growth directions, then they will have different cross-sectional shapes; this being investigated in greater detail in Chapter 6. A <112> NW for example could have a rectangular cross-section, defined by two {110} facets and two {111} facets. Accordingly, this would provide four separate growth directions, which are perpendicular to the primary NW growth axis, for secondary NWs to adopt. Indeed, in Fig 5.22b there appears to be 4 definite rows of secondary NWs, each rotated around the primary NW by 90° with respect to its neighbor, and so we assume the primary wires' axis is <112>. NWs growing in a <111> direction on the other hand may have a hexagonal cross-section, with 6 sidewall facets from which secondary NWs could grow. The more pillar-like morphology of these structures, obtained after a longer growth time (Fig 5.22b) is attributed to lateral growth.

Sputter deposition is considered to be the most suitable method for the generation of shell layers, as it did not disrupt the NWs themselves, and resulted in the complete coating of the CdTe NWs with CdS, although in some cases the coatings were thicker on one side of the NWs than the other. The non-uniformity is attributed to shadowing effects, this being

supported by the observation that the side of the NWs on which the layers were thickest is the same for both CdS and ITO layers. A further benefit to sputter deposition is that the CdS and ITO layers can be deposited sequentially without breaking vacuum in the system used here.

5.6 Conclusions

In this Chapter, all the necessary processes required to generate core-double-shell ITO/CdS/CdTe NW structures, suitable for solar cell architectures, have been demonstrated.

First, the generation of Au nanodots on Mo foils was demonstrated, by annealing 5 nm thick Au films at 360°C in 100 Torr N_2 for 30 minutes. This was the basic process used for preparing Au catalysts for NW growth experiments in this Chapter. Nanodot diameters of 34 ± 4 nm and densities of $(3 \pm 1) \times 10^9$ cm^{-3} were achieved.

Au-catalysed CdTe NW growth was demonstrated directly on Mo foil (Section 5.3), using close-space sublimation as the source of deposition flux. NWs, of radii in the range 50 – 500 nm and of lengths up to 20 μm, were grown at a substrate temperature of 500°C. The presence of a semi-continuous film at the base of the NWs was also observed. Pure Au droplets were present at the NW tips, which implied a VLS mechanism was responsible for NW growth. The high aspect ratio of the catalysts, and their rounded surfaces, and the fast growth rates of the NWs also supported a VLS mechanism. As the NW length was inversely proportional to the radius, it was concluded that the main contribution to VLS growth was the diffusion of adatoms from the substrate to the catalyst, as opposed to direct adsorption.

At the growth temperature, liquid phases of both Au-Te and Au-Cd are achievable, provided sufficient molar ratios of Te or Cd are present. Accordingly, VLS growth can be attributed to the eventual formation of either of these phases (although the limited evidence acquired implies a Au-Te phase is responsible), through incorporation of semiconductor by the Au droplets. During the period of incorporation, the droplets remained solid, accounting for the initial delay to NW growth. NW growth then initiated once they became liquid (allowed by the eventual sufficient incorporation of Te or Cd).

Section 5.3 continued with a demonstration of the influence of growth conditions on NW growth. The morphology of the generated structures was highly influenced by the N_2 pressure. NW growth was absent when using high pressures as the deposition flux was insufficient to saturate the droplets, whereas, at low pressures, NW growth proceeded. The temperature dependence of NW growth was also investigated, with an increase in NW length with source temperature, and a decrease of NW density with increased substrate temperature being observed. The experimental data agreed well with a kinetic model for VLS NW growth, which

also gave a good fit to the time dependence of the NW length and radius. NW radius was constant for 40 minutes and then increased due to lateral growth, with the radius at the base increasing more than at the tip, resulting in some NWs having a tapered morphology. The observed lateral growth is consistent with some of the fitting parameters that were extracted from the model; a sidewall diffusion length of 2 μm and a sidewall sticking probability of 0.61.

NW growth was also achieved on CdTe/Mo, CdTe/glass and CdTe/ITO/glass substrates (Section 5.4). The array densities were greater than those directly grown on Mo substrates ($10^7 – 10^8$ cm^{-2} compared to $10^6 – 10^7$ cm^{-2}), and NW growth initiated immediately without delay. These improvements were accounted for by the more ready acquisition of saturated liquid droplets, i.e. the Au droplets could acquire semiconductor material from both the vapour *and* the substrate.

NWs were not vertically aligned, but were inclined at a variety of angles, as large as 90° to the substrate normal. XRD measurements confirmed that the NW arrays were less preferentially crystallographically oriented than both as-grown and annealed substrates. It is likely that NW growth was non-epitaxial and that recrystallisation of the underlying film occurred during NW growth, this being supported by the existence of pores in the film, as shown in Fig 5.18a. A consideration of this, and the effects of stereology, account for the apparent randomness of the angle of NW inclination. A detailed evaluation of NW growth direction is later reported in Chapter 6.

Finally, methods of coating the NWs – CBD, MOCVD and RF sputtering – with sulphide shells, to form radial *p-n* junction heteronanowires, were evaluated in Section 5.5. Whereas CBD generated highly uniform shell coatings of CdS, the method caused the collapse of a large proportion of the NWs. On the other hand, MOCVD caused no mechanical disruption to the NWs, but the shell coatings of both CdS and CdZnS were highly non-uniform; CdZnS deposition generated complex, dendritic structures. RF sputtering however was considered to be more suitable, as it did not collapse the NWs, and generated conformal coatings. The only undesirable feature was the slight variation of shell thickness around the NW, attributed to shadowing effects. An ITO layer was subsequently sputtered resulting in the generation of ITO/CdS/CdTe core-double shell NWs.

Ultimately, methods to generate CdTe NW arrays, to control the NW length, radius and array density, and to do this on pre-deposited sputtered CdTe films – which may provide electrical continuity in a full device - have been presented. The basis of the NW cell design was completed by sputtering the window layer and front contact. These structures are

optically, structurally and electrically characterised in Chapter 6 and their solar cell characteristics are interrogated in Chapter 7.

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Chapter 6 : Structural, optical and electrical characterisation of CdTe and CdS/CdTe nanowires

6.1 Introduction

Having reported the growth of CdTe nanowires (NWs) and CdS/CdTe core-shell NWs, their characterisation is now presented. This is essential for understanding the potential of these structures for use in photovoltaic (PV) devices.

In Sections 6.2 and 6.3, the microstructural and point defects in CdTe NWs are evaluated using TEM analysis and photoluminescence (PL) spectroscopy. Both microstructural and point defects have profound effects on the conversion efficiencies of PV devices. For example, in the case of grain boundaries, recombination loss – leading to reductions in the open circuit voltage and short circuit current – is very significant[1]. Moreover, point defects are responsible for the shallow levels that (beneficially) control the conductivity type of semiconductors and also for the compensating and deep level behaviour that is deleterious to solar cell performance. These considerations are known to be important for CdTe devices[2, 3]. Here, it is demonstrated that these CdTe NWs have point defect and microstructural defect content that is very different from that of polycrystalline thin films, and is of a quality similar to that of single crystals. The effect of post-growth annealing treatments on the populations of defects in CdTe NWs is also investigated, using annealing conditions similar to those that have been used to improve the performance of polycrystalline thin-film CdTe solar cells[4, 5].

TEM and PL analysis of CdS/CdTe core-shell heterostructures is reported in Section 6.2 and 6.4 respectively; the CdS/CdTe interface is shown to be epitaxial, and there is evidence of S and Te inter-diffusion at the interface.

One of the main benefits cited for the use of NWs in PV devices is their potential to trap light more effectively, particularly at long wavelengths[6, 7]. Accordingly, an evaluation of the reflectance and transmittance of both CdTe NW arrays and ITO/CdS/CdTe core-shell heterostructures is reported in Section 6.5, along with those for planar CdTe and ITO/CdS/CdTe films for comparison. Section 6.5 also includes resistivity measurements of individual NWs using the 4-point probe technique.

6.2 Microstructure of CdTe nanowires and ITO/CdS/CdTe nanowires

In this Section, the microstructure of as-grown NWs, annealed NWs and core-double shell ITO/CdS/CdTe NWs are evaluated by TEM. In particular, the growth directions of the NWs, the incidence of planar defects within the NWs, their morphologies and the CdS/CdTe interface structure are described.

6.2.1 Experimental procedure

Au-catalysed CdTe NWs were sublimation grown by the vapour-liquid-solid (VLS) mechanism on CdTe/glass substrates, with the CdTe film having been RF sputtered as described in Section 5.4.1. Growth was carried out using a CSS source temperature of 570°C, under 10 Torr of nitrogen for 15 mins, with the substrate held at 520°C. 50% of the NW arrays were then annealed in-situ in the CSS chamber, at 400°C for 30 minutes under 100 Torr of nitrogen. For the core-double shell structures presented in Section 6.2.3, CdS and ITO shells were sputter grown onto as-grown CdTe NWs, the exact growth conditions being reported in Section 5.5.1.

As-grown and annealed CdTe NWs were mechanically removed onto Cu TEM grids. TEM analysis of ten as-grown NWs and ten annealed NWs was performed, with bright-field TEM images and HRTEM images being acquired.

Cross-sections of ITO/CdS/CdTe core-double shell NWs were prepared for TEM analysis by the FIB lift out technique[8]: Prior to any exposure to the Ga^{+} ion beam, the area of interest was coated with a 1 μm Pt layer, and the accelerating voltage of the ion beam was stepped down during sample thinning to 2 kV so to limit the depth to which Ga is implanted in the sample. Both bright field STEM images and HRTEM images were acquired for cross-sections.

6.2.2 TEM analysis of CdTe nanowires

It was found that the microstructure of CdTe NWs was determined only by their growth axis, with annealing having no effect on the extended defects – this will be discussed further in Section 6.2.4. The microstructural trends are therefore now described with reference to the growth axis only. NWs having one of three growth axes, but no others, were observed, these being <110> (20%), <111> (50%) and <112> (30%), with typical examples for each of these shown in Figs 6.1 – 6.3 respectively.

Those growing in the <110> direction (Fig 6.1a) were all defect free (Fig 6.1b), there being no evidence of any planar defects. The NW shown has one smooth side-wall, on the left-hand side, and one tapered sidewall, on the right-hand side. The tapering occurs abruptly

rather than gradually, presumably defined by crystallographic facets. This is not representative of all NWs growing in <110> directions, as some had smooth sidewalls on both sides and constant radii along their entire axis.

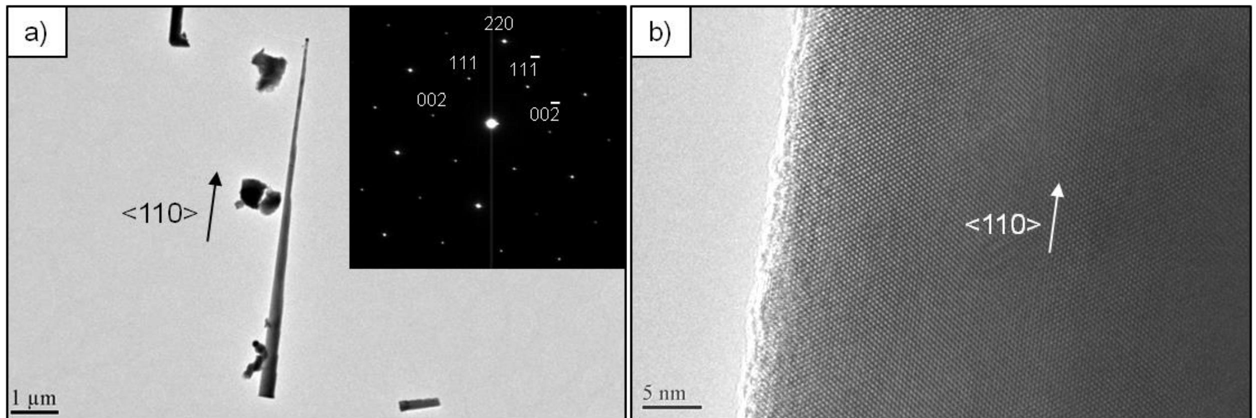

Fig 6.1: a) Bright-field TEM image of a CdTe NW growing in a <110> direction, with diffraction pattern inset. b) HRTEM image of the same NW showing it is a clean single crystal with no planar defects.

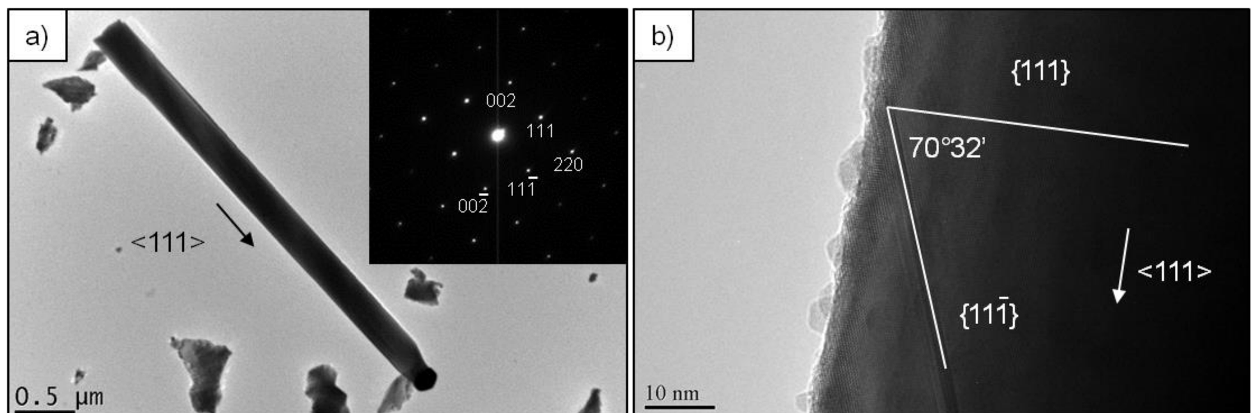

Fig 6.2: a) Bright-field TEM image of a CdTe NW growing in a <111> direction, with diffraction pattern inset. This NW is single crystal and free of any planar defects. b) HRTEM image of a different NW, also growing in a <111> direction, showing a stacking fault along a {111} plane.

About 10% of those wires growing with the <111> direction were also defect free (Fig 6.2a), whereas most contained stacking faults inclined at an angle of 70°32’ to the growth axis, i.e. on a set of {11$\bar{1}$} planes, as shown in Fig 6.2b. Some <111> NWs were tapered on one side, but this behaviour was less frequent than for <110> or <112> (see below) NWs.

The highest density of planar faults was seen in those wires growing along the <112> axis (Fig 6.3a), this direction containing a set of {111} planes that extend along the full length of the wires. Stacking faults and low-energy $\Sigma = 3$ twins were observed on these {111} planes, as shown in Fig 6.3b and c. While the twinning and stacking faults often occurred randomly,

there was sometimes periodic behaviour. The periodicity of the regular structure was consistent with a 4H polytype, that is the stacking sequence AαBβAαCγAαBβAαCγ. A diffraction pattern taken from a region of another NW exhibiting such periodic twinning is shown in Fig 6.3d. It consists of three sets of spots, two of which correspond to the zinc-blende structures of the twin and matrix elements, and the other to the hexagonal 4H polytype associated with the periodic twinning (as labelled).

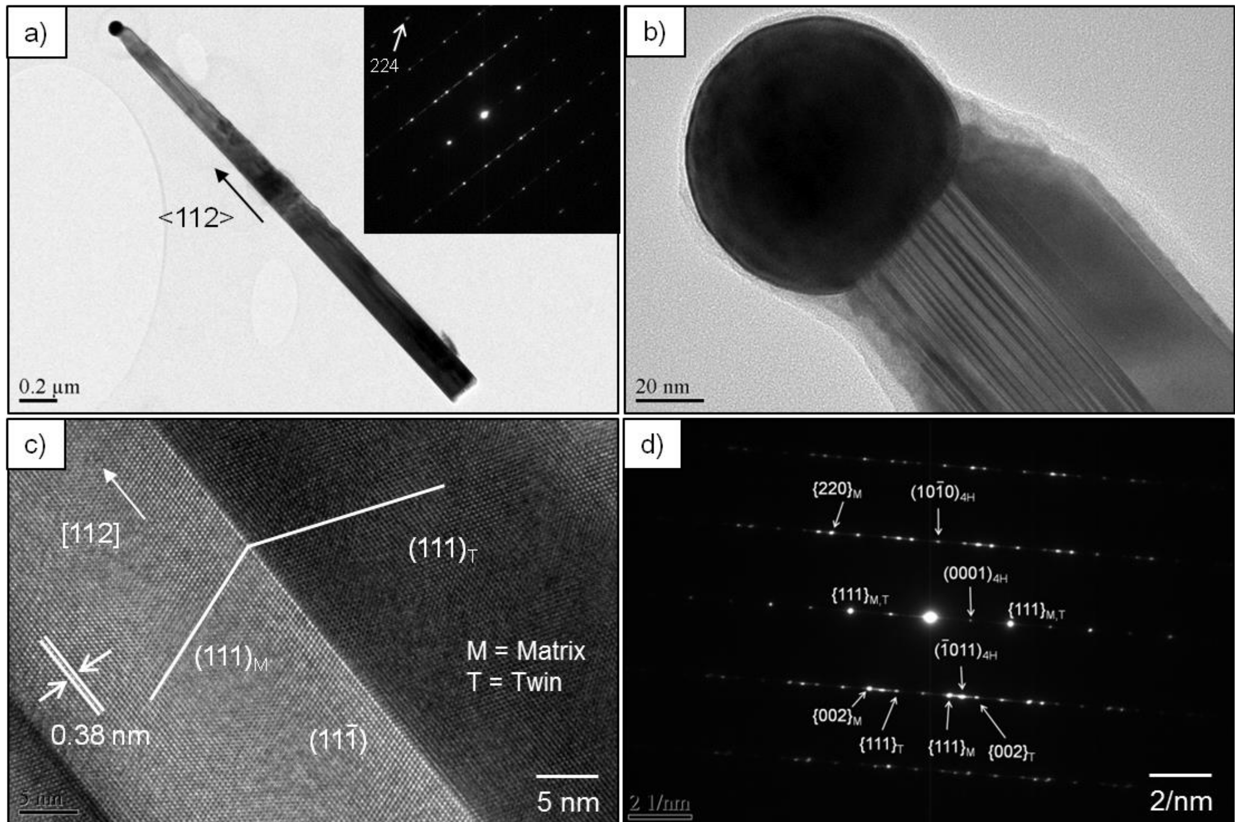

Fig 6.3: a) Bright-field TEM image of a CdTe NW growing in a <112> direction, with diffraction pattern inset and b) an enlarged image of the NW tip which shows the catalyst, and a high density of lengthwise twins in the NW. c) HRTEM image taken from the same NW of a $\Sigma = 3$ twin, lying in a $\{11\bar{1}\}$ plane, which is parallel to a <112> growth direction. d) Indexed diffraction pattern of a separate NW, also growing in a <112> direction, see text.

Fig 6.4 shows the effect the growth orientation has on the NW-droplet interface. Whilst NWs growing in the <111> direction have a smooth NW-droplet interface lying on a {111} plane (Fig 6.4a), those growing in a <112> direction have a staggered NW-droplet interface as a result of the high density of lengthwise twins and stacking faults (Fig 6.4b). In Fig 6.4b, the regions of dark contrast are zinc-blende regions, for which the NW-droplet interface lies along a {111} plane, whilst the regions of light contrast are 4H polytype, for which the interface

may lie along, for example, a $(10\bar{1}0)_{4H}$ plane. These regions of ZB or 4H are just ~ 1 nm wide in some cases.

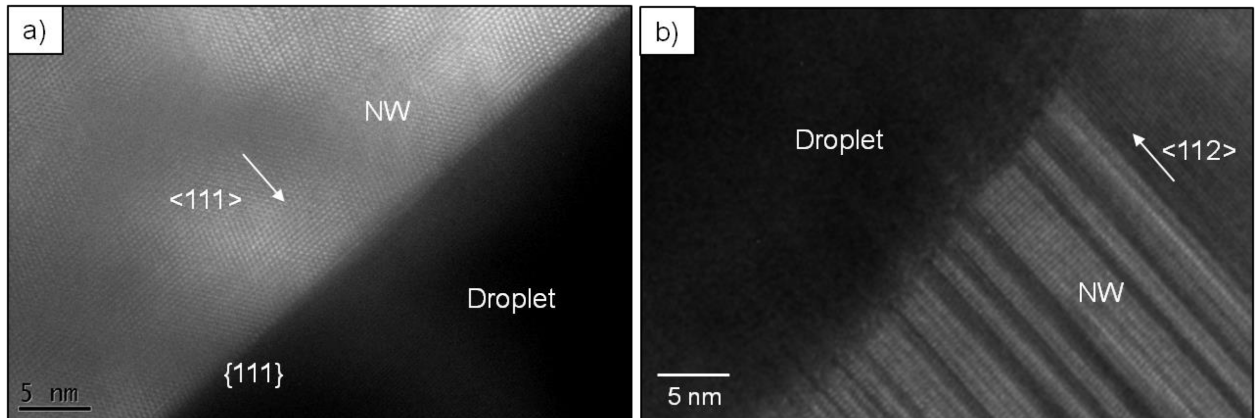

Fig 6.4: a) The NW-droplet interface for a NW growing in a <111> direction is smooth, lying on {111} plane. b) For a NW growing in a <112> direction, lengthwise twins cause the interface to be staggered.

6.2.3 TEM analysis of ITO/CdS/CdTe core-double shell nanowires

From analysis of cross-sectional STEM images of ITO/CdTe/CdS core-double shell heterostructures, it was found that CdTe NWs can adopt both hexagonal and rectangular cross-sectional geometries, examples of these being shown in Fig 6.5a and b respectively. Since only five NWs were analysed, other geometries are likely to exist however (see Section 3.2.5).

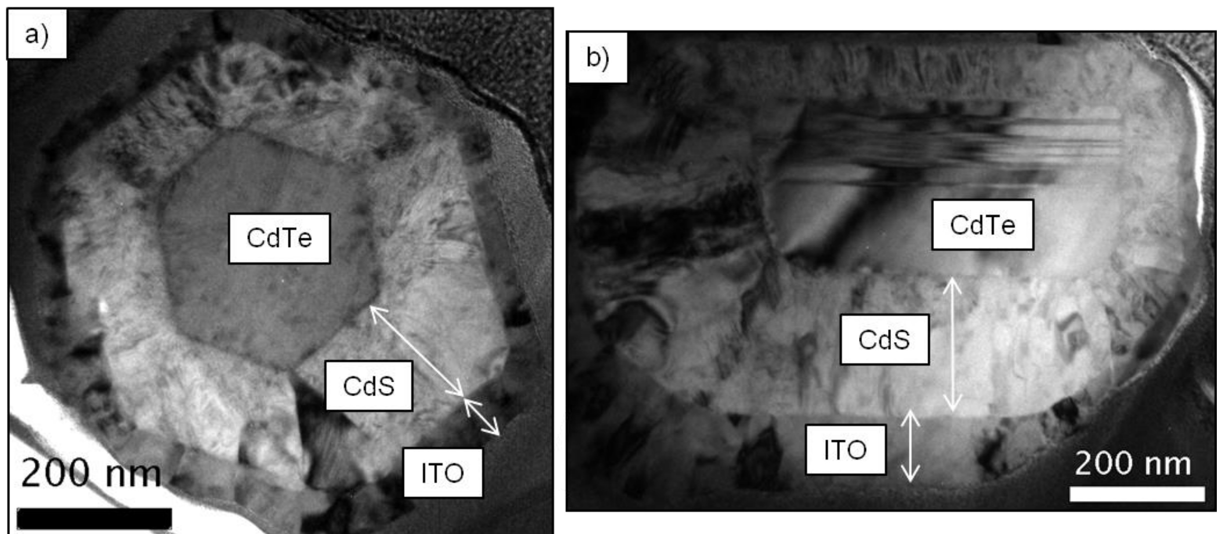

Fig 6.5: a) Cross sectional bright-field STEM images of ITO/CdTe/CdS core-double shell NWs with a) <111> growth axis and a hexagonal geometry and b) <112> growth axis and a rectangular geometry.

The NW of hexagonal cross-section (Fig 6.5a) has a <111> growth axis, as determined from the FFT (not shown). In this example, the CdS shell has a relatively uniform thickness, ranging from a minimum of ~ 150 nm to a maximum of ~ 200 nm, and the ITO shell has a thickness of 35 – 60 nm. This was not always the case, as some NWs had highly non-uniform coatings, with a CdS thickness range as wide as 70 – 250 nm. The CdS shell in Fig 6.5a is largely single crystal, although at the vertices between two sidewalls, at the bottom of the image, a separate grain has nucleated. Both CdS and ITO shells adopt the hexagonal geometry of the CdTe core. No planar defects were observed in any of the cross sections of <111> NWs.

The NW of rectangular cross-section shown in Fig 6.5b has a <112> growth axis, as determined from the FFT (not shown). Its geometry is somewhat irregular in that the lower two corners of the rectangle are rounded. The CdS is largely single crystal but for a separate grain that has nucleated from one of the rounded corners. In this example, the non-uniformity of shell thickness around the NW is clearly shown. A high density of twins are observed in the CdTe core, this being consistent with images of <112> NWs shown in Fig 6.3.

The geometry of these NWs can be explained using Wulff constructions, which predict the equilibrium shape of a crystal based on energy minimisation arguments (See Chapter 3). Fig 6.6a shows the surface energy plot, $\boldsymbol{\gamma}(\hat{\boldsymbol{n}})$, for a CdTe NW with a <111> growth axis. Here, only low index crystallographic planes that are perpendicular to <111> are considered, these being six {110} planes and six {112} planes. According to calculations made by Berding[9], the {110} planes are the lowest energy planes in CdTe ($\boldsymbol{\gamma}_{\mathbf{110}}$ = 0.18 J/m^2). No data could be found for the {112} planes, but Iwanaga[10] states that $\boldsymbol{\gamma}_{\mathbf{112}}$ is expected to be much higher than $\boldsymbol{\gamma}_{\mathbf{110}}$ in zinc-blende semiconductors. The Wulff construction, based on this $\boldsymbol{\gamma}(\hat{\boldsymbol{n}})$ plot is shown in Fig 6.6b, predicting that NWs with <111> growth axis are bounded by six <110> facets, this consistent with the geometry shown in Fig 6.5a.

For <112> NWs, the only low-index planes perpendicular to the growth axis are two {111} planes, e.g. the Cd-terminated (111)A plane and Te-terminated $(\bar{1}\,\bar{1}\,\bar{1})$B plane, and two {110} planes. The Wulff construction for NWs with a <112> growth axis, overlayed with the $\boldsymbol{\gamma}(\hat{\boldsymbol{n}})$ plot is shown in Fig 6.6c. Whilst the inequality $\boldsymbol{\gamma}_{\mathbf{110}} < \boldsymbol{\gamma}_{\mathbf{111B}} < \boldsymbol{\gamma}_{\mathbf{111A}}$ was used for this plot, no specific $\boldsymbol{\gamma}$ data was found for the (111)A and $(\bar{1}\,\bar{1}\,\bar{1})$B planes, only for the general {111} planes. However, the assumption that the $(\bar{1}\,\bar{1}\,\bar{1})$B plane is lower in energy than the (111)A was considered to be valid given that this is typically the case for polar III-V and II-VI semiconductors[11]. For all other orientations, $\boldsymbol{\gamma}$ was assumed to be very large. The Wulff construction predicts the rectangular shape for <112> NWs, tapering in the [111]A

direction. The two {110} faces are predicted to be wider than the {111} faces whereas experimentally the opposite is the case (Fig 6.5b), the {111} faces having been identified in Fig 6.5b as those parallel to the twins. Fig 6.6d shows 3D schematic diagrams of <111> and <112> NWs based on these models.

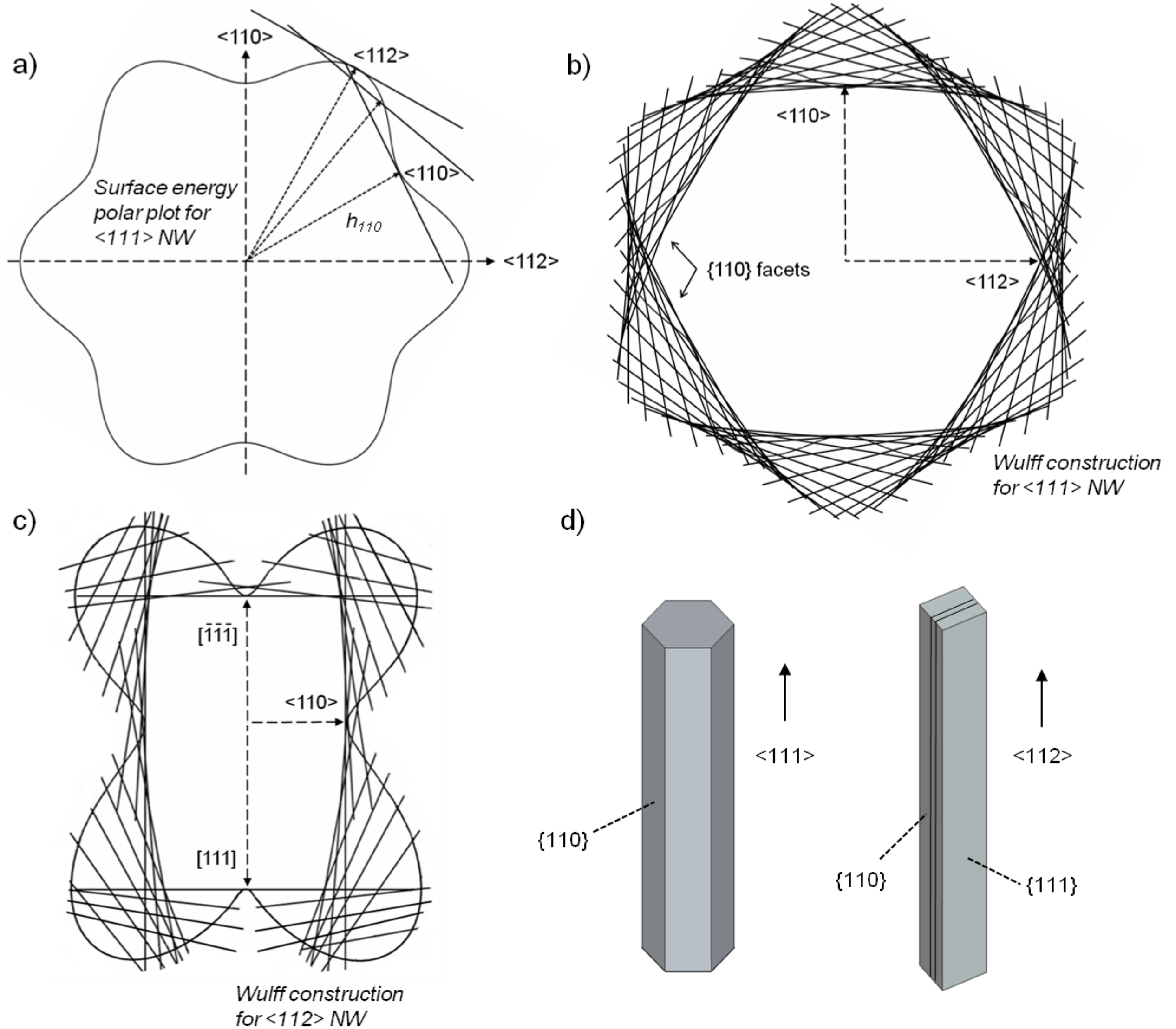

Fig 6.6 a) Polar plot of surface energy as a function of crystallographic orientation for a NW with <111> growth axis. b) Wulff construction for a <111> NW. c) Wulff construction for a <112> NW overlayed with the polar plot of surface energy. D) Three-dimensional schematic diagrams of <111> and <112> NWs.

Fig 6.7 shows a HRTEM image of the interface between the CdTe core and the CdS shell, taken from the ITO/CdS/CdTe core-double shell structure shown in Fig 6.5a. The interface lies on one of the six {110} CdTe facets. The FFTs taken from both CdS (inset, left hand side) and CdTe (inset, right hand side) regions have equivalent six-fold symmetry and are well aligned, implying an epitaxial relationship.

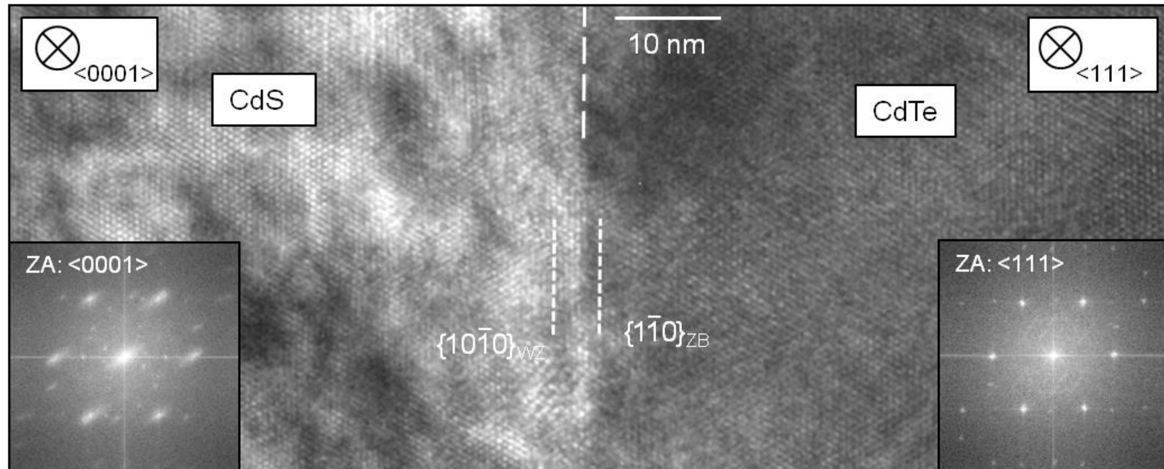

Fig 6.7: A HRTEM image of the interface between the CdS and the CdTe core for the core-double shell NW shown in Fig 6.5. An epitaxial relationship is implied from the alignment of the FFTs taken on either side of the interface.

6.2.4 Discussion

6.2.4.1 NW growth directions and planar defects. The observation that NWs grew in three families of crystallographic directions - <110>, <111> and <112> - goes some way to explaining the non-verticality and apparent randomness of CdTe NW orientation, as reported in Chapter 5. In general, NWs grow in crystallographic directions that minimise the total free energy, which is typically dominated by the surface free energy between the semiconductor and liquid catalyst[12]. These tend to be low-index growth directions, i.e. <001>, <110>, <111> and <112>.

The presence of twins, stacking faults and polytypes in the CdTe NWs is not unexpected, as the stacking fault energy of CdTe is relatively low (reported in the range 9 – 10.1 mJ/m^2)[13, 14], compared to, for example, Ag or Ni with stacking fault energies of 22 and 250 mJ/m^2 respectively[15]. In this work twins in CdTe NWs were *only* observed on {111} planes. This resulted in te highest density of twins being found in NWs growing in <112> directions (Fig 6.3), as there is a set of {111} planes lying parallel to the growth axis and so twins persist along the entire NW length. Lengthwise twins having equivalent crystallography have similarly been observed in, for example, Ag[16] and Si[17, 18] NWs. For NWs growing in <111> directions, stacking faults and twins are not parallel to the growth axis and so intersect NW sidewalls and grow out (Fig 6.2), hence they are not often observed in cross sections (Fig 6.5a). Twins may form either by growth or deformation processes[19]. Growth twins (or stacking faults) may form on {111} planes when the ABCABC stacking sequence is interrupted by adatoms arriving on top of an A plane adopting a C-site instead of a B-site. Wang *et al.*[16] propose a mechanism whereby this is induced by the presence of impurities

'forcing' adatoms onto C-sites, whilst Zhou *et al.*[20] show that in some cases the binding energy difference for adatoms occupying B-sites or C-sites is very small, and so the presence of impurities is not necessary to induce frequent growth twinning. Lengthwise twins have alternatively been attributed to the coalescence of nuclei that possess different <111> orientations[16].

6.2.4.2 Impact of planar defects on electrical properties of NWs. The planar defects observed here in CdTe NWs may be thought to be undesirable considering the detrimental impact of grain boundaries in PV devices: Electron-hole recombination, which acts to reduce open-circuit voltage (V_{OC}) and short circuit current (J_{SC})[1], is typically enhanced at grain boundaries as they act as sinks for impurity segregation[21] and in any case may have wrong bonds. Even when such boundaries are passivated to electrical recombination[22], they may nevertheless contribute to the series resistance of the devices that acts to reduce their fill factor, as has been shown for CdTe solar cells[23]. However, the electrical activity of grain boundaries depends on their crystallographic make up[24]: Whilst high-energy twin boundaries and random grain boundaries are considered to be electrically active in zinc-blende semiconductors, low-energy pure $\Sigma = 3$ coherent twin boundaries, such as those found in these NWs, are mostly inactive. This is particularly the case in CdTe and other sphalerite semiconductors as these low-energy planar defects do not disrupt bonding significantly. (The extent of recombination in these NWs is investigated in Section 6.3, using PL spectroscopy).

A further consideration is that although the diameters of these NWs are not on the quantum-scale, the extent of lengthwise twinning in <112> oriented NWs may yield quantum confinement effects, through the formation of ZB/4H/ZB/4H/ZB (where ZB is zinc-blende and 4H is 4H-polytype) superlattices. Indeed, upon close examination of Fig 6.4b, it is clear that some of the ZB and 4H regions are just a few nms in diameter. However, to the author's knowledge, the positions of the conduction and valence band edges of 4H-polytype CdTe are not known, therefore the superlattice *type* of ZB/4H/ZB/4H/ZB is also unknown. Nevertheless, subtle electrical effects due to these planar defects cannot be ruled out.

Post-growth annealing of the NWs at 400°C in a nitrogen environment for 30 mins had no observable effect on the NW microstructure. Indeed, the post-growth annealing processes applied to CdTe PV devices generally causes grain growth rather than reducing the incidence of low-energy twin boundaries. Terheggen *et al.*[25] demonstrate that upon Cl-activated annealing (at 430°C) of polycrystalline CdTe/CdS solar cells, there was significant recrystallisation of the CdTe, but a large density of twins existed both before and after annealing. Moreover, by using higher annealing temperatures (530 – 630°C) and longer

annealing times (up to 8 hours) than here, Consonni *et al.*[26] actually *increased* twin density through the formation of annealing twins in polycrystalline CdTe.

The observed hexagonal cross-sectional geometry of CdTe NWs with a <111> growth axis (Fig 6.5a) was consistent with that predicted by a Wulff construction (Fig 6.6b). For CdTe γ_{110} is much lower than γ_{111} and so the six perpendicular {110} facets should be highly stable. In many other semiconductors (GaAs, InP, Si) $\gamma_{111}$is lower than γ_{110} and for the case of InP, NWs have been observed to grow with inclined sidewalls alternating between (111)A and $(\bar{1}\bar{1}\bar{1})$B orientations, resulting in the formation of twinned axial superlattices[27]. The Wulff construction of NWs having a <112> growth axis (Fig 6.6c) predicted them to possess a rectangular geometry bound by two {111} facets and two {110} facets, as observed experimentally (Fig 6.5b). However, whilst the {111} sidewalls were experimentally observed to be wider than the {110} sidewalls, the Wulff construction predicted the opposite to be the case since the γ values used for the construction defined $\gamma_{110} < \gamma_{111}$. This may imply that the γ values used are inaccurate. Moreover, whilst two of the corners were observed to be rounded in the STEM image, the Wulff construction only accounted for a slight tapering of the rectangular geometry towards the [111]A sidewall. Evidently, a complete data set of γ as a function of orientation is required for a more accurate representation. It should also be noted that NW geometry is not just defined by the surface energies, but also by a minimisation of the surface-to-volume ratio[28].

The reader is referred to Ref. 12 (or Section 3.2.5) for a general review of the control of NW growth directions, and its impact on NW geometry. Depending on the system, <111> and <110> oriented NWs may adopt a number of possible geometries, whereas <112> oriented NWs can *only* be rectangular. In the general case, <112> NWs may have a practical advantage, despite the higher occurrence of twinning, as their geometry is controlled, whereas those of <110> and <111> NWs are not, NW geometry being known to influence their optical and electronic properties in some cases[29].

The apparently asymmetrical abrupt tapering of NWs (along the growth axis) as described for all NWs, has also been observed by Schwarz *et al.*[30] in Si NWs. The behaviour is thought to be driven by the instability of some of the sidewall facets that are perpendicular to the liquid-solid interface: Tapering can occur by the introduction of discrete 'jogs' – possibly upon small fluctuations of growth conditions, or upon loss of Au - and its asymmetrical nature is thought only to be an artefact of stereological projection. The behaviour was less frequent for <111> NWs than <110> and <112> NWs, presumably since <111> NWs can only have {110} sidewalls, whereas others may have {110}, {111} or {100} sidewalls.

6.2.4.3 Epitaxial CdS/CdTe interface. HRTEM imaging demonstrated the heteroepitaxial interface between the CdTe NW core and CdS shell (Fig 6.7). Here, the six-fold symmetry observed in the FFT of the CdTe is typical for a zinc-blende lattice aligned along a $\langle 111\rangle$ zone-axis with six equivalent $\langle 1\bar{1}0\rangle$ directions lying in the cross section plane. Indeed, this NW has a $\langle 111\rangle$ growth axis and six $\{1\bar{1}0\}$ sidewall facets (Fig 6.5c). In the CdS, the beam direction is $\langle 0001\rangle$, this being inferred from the FFT which has six-fold symmetry due to the six equivalent $\langle 10\bar{1}0\rangle$ directions lying in the cross section plane. The epitaxial relationship can therefore be defined as $\{10\bar{1}0\}\langle 0001\rangle$CdS//$\{1\bar{1}0\}\langle 111\rangle$CdTe, these planes having a lattice mismatch of ~ 20%. The blurring of the spots in the CdS FFT implies there exists a high level of strain which is expected for such a high mismatch. NWs have an extra degree of freedom relative to planar films in which to relieve mismatch-induced strain: In this case, it is likely that the nucleation of a separate grain at the vertices of two facets, as seen in the bottom of Fig 6.5a, helps to relieve this strain.

An epitaxial CdS/CdTe interface may be highly desirable in the context of PV devices, as it is likely to result in lower densities of interface states: Surface recombination at interface states, to some extent attributable to dangling bonds at lattice mismatched heterointerfaces, is detrimental to V_{OC}. Kosyachenko *et al.*[31] calculated a significant gain in internal quantum efficiency could be achieved in CdS/CdTe solar cells if surface recombination velocity was reduced, particularly for CdTe doping densities of ~ 10^{14}cm^{-3} (a value which is typical for real devices). Limitation of surface recombination velocity is of particular relevance to NW solar cells, due to their high surface-to-volume ratio.

6.3 Photoluminescence of CdTe nanowires

PL spectroscopy was used to evaluate point defects in CdTe NWs. In Section 6.3.2, spectral PL data of CdTe NWs, and of CdTe films for comparison, is presented. Assignment of the spectral features to radiative transitions involving particularly energy states, and hence the inference of the presence of particular impurities in the NWs, was made with reference to literature data and by observing the features' behavioural characteristics. The effect of annealing CdTe NWs in different environments on the relative intensities of these features is also presented (Section 6.3.3). Radiative lifetimes of excitons in CdTe NWs were determined using time-resolved PL (Section 6.3.5).

6.3.1 Experimental procedure

CdTe NW arrays were grown on CdTe/ITO substrates by the metamorphic technique (see Section 5.4) using source material from Alfa Aesar (5N pure). The NW arrays were subsequently annealed on their substrates for 30 minutes in the following environments: a) as-grown control; b)100 Torr N_2 at 400°C; c) air at 400°C; d)10 Torr O_2 + 90 Torr N_2 400°C; e) 100 Torr N_2 at 500°C; and f) 10 Torr H_2 + 90 Torr N_2 at 400°C. These annealing conditions were chosen as they are similar to those that have been used to improve the microstructure of CdTe in thin-film solar cells[4, 5]. For spectral data reported in Section 6.3.2, low temperature PL spectra were excited using the 514 nm line of an argon ion laser (spot size, d = 1 mm, excitation intensities of 30 – 1500 mW/cm^2). The beam was incident at an angle of 20° to the normal, with the samples being held at 4 - 200K in a closed-cycle He cryostat. PL spectra were recorded from a CdTe thin-film substrate, from the NW arrays on their substrates and from NWs that had been removed by pressing the samples onto clean Si (111) wafers, the latter being most informative (see Section 6.3.2). Secondary electron images were recorded for isolated as-grown and annealed NWs.

For time-resolved PL measurements, CdTe NWs were generated using the same procedure as above, but from different source material (bought from Sigma Aldrich, 5N pure). The NW arrays were annealed at 400°C in 100 Torr N_2 for 30 mins and removed onto Si wafers. Initially, spectral data was generated by exciting with the 440 nm line of a Xe lamp, and then for lifetime measurements the 406 nm line of a pulsed diode laser was used (pulse width of 65 ps, repetition rate of 20 MHz), with samples held at 4 – 20K.

6.3.2 Photoluminescence spectra of as-grown nanowires

6.3.2.1 Photoluminescence from CdTe control films and NW arrays on their substrates:

Fig 6.8 shows a comparison between the PL from: a) a control film of polycrystalline CdTe; b) an array of NWs on their substrate; and c) a group of NWs that have been isolated by removing them from their substrate onto a clean Si wafer. Si does not luminesce in the region measured here.

The spectra from both the films and the NW arrays on their films differ greatly from those from the isolated NWs: The former both comprise a broad donor-acceptor-pair (DAP) luminescence band (~1.35 – 1.5 eV) having no fine structure, and little or no near-edge emission, whereas the latter contain both near-edge peaks (~1.5 - 1.6 eV) and donor-acceptor-pair (DAP) peaks (~1.35 – 1.5 eV) that show fine structure.

It may be inferred that for the case of NWs on a polycrystalline CdTe layer, the layer dominates the PL emission. Hence, for the purposes of this work, the removal of the wires

from their substrates clearly gives spectra that are unique to the wires, and which give the opportunity for the further spectral analysis (presented in Section 6.3.2.2) and line identification (discussed in the Section 6.3.6).

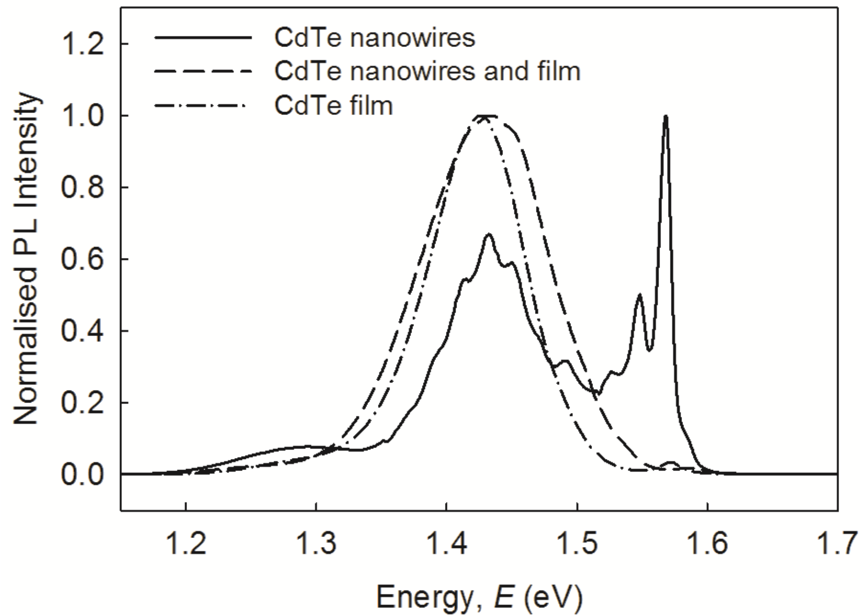

Fig 6.8: Comparison of PL spectra (4K) from CdTe: a) dash/dotted line – control film of sputtered CdTe, b) dashed line – NW array on a polycrystalline CdTe film, and c) NWs that had been isolated by removal from their substrate onto a clean Si wafer. The latter shows strong excitonic emission and fine structure in the peaks that is discussed in the text.

6.3.2.2 Photoluminescence of isolated nanowires (as-grown samples): The spectra of the isolated NWs are now described in more detail, with reference to Fig 6.8 and a high-resolution spectrum of the near-edge region, shown in the inset of Fig 6.9. Fig 6.9 also shows the relation between the PL intensity, I, and the incident light, L_{ex}, for three of the peaks observed in the spectra, at 1.569, 1.548 and 1.432 eV. The relationship $I \propto L_{ex}^{k}$ often holds for PL experiments, with the value of k being a useful diagnostic tool for identifying the origin of transitions, as discussed in Chapter 4. Discussion of the origin of each of the peaks is deferred to Section 6.3.6, but nevertheless, this is summarised in Table 6.1. Assignments were proposed with reference to both the studies presented here, and those in the literature.

The spectrum of the as-grown NWs consists of three main energy regions: a) the excitonic region with peak energies greater than 1.5 eV; b) the donor-acceptor pair (DAP) series with peak energies in the range 1.35 – 1.5 eV; and c) the deep-level region with peak energies lower than 1.35 eV. Firstly, in the excitonic region, the most intense lines were at 1.589, 1.569 and 1.548 eV (Fig 6.9 inset), which are separated by the LO phonon energy (20 – 21 meV). The lines at 1.569 and 1.548 eV have k-values of 1.27 and 1.13 respectively (Fig 6.9). (No

change to the spectral positions of these peaks was observed as L_{ex} was increased). Assuming that these lines are optical phonon replicas of the 1.589 eV line, the Huang-Rhys electron-phonon coupling parameter was estimated at S = 2.0 using the Poisson distribution, although the fit of the peak intensity series to the Poisson envelope was not good, with the first phonon replica being more, and the higher orders less intense than expected. The 1.548 eV line has low-energy shoulders at 1.539 and 1.529 eV.

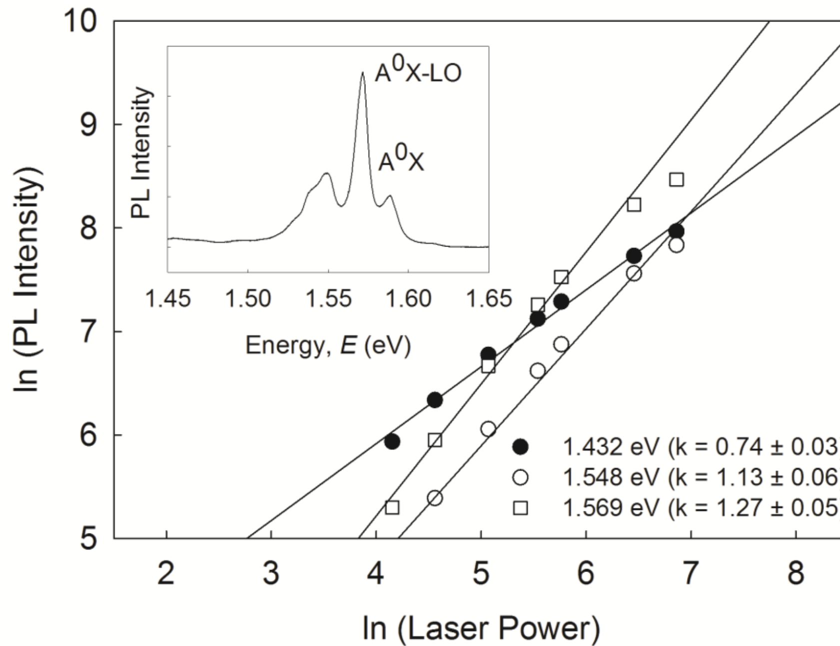

Fig 6.9: *ln-ln* plot of PL intensity against laser power (the laser power was measured in mW/cm^2) for the 1.569 eV, 1.548 eV (inset) and 1.432 eV (not shown) features of the PL spectra for mechanically removed as grown NWs. The intensity of PL emission, I was related to the laser power by $\propto L_{ex}^{k}$. Values of $k > 1$ are consistent with excitonic emission, as was seen for the peaks labelled A^0X and A^0X-LO. The peak at 1.432 eV is part of the DAP series; see Section 6.3.6 for a discussion of peak assignments.

Secondly, the 1.35 – 1.5 eV region is considered. There is a series of seven peaks and shoulders here, with the highest energy line centred at 1.491 eV. The features are separated by ~ 20 meV, i.e. by the LO phonon energy. The most intense peak is that at 1.432 eV, its $I - L_{ex}$ relationship shown in Fig 6.9. The exponent values for the first five lines in the series are roughly equal, in the range k = 0.73 – 0.76, and assuming the peaks are phonon-related, an S-value of 2.5 was estimated, with the fit of peak intensity to the Poisson envelope being very good. As L was increased from 60 – 2000 mW.cm^{-2}, a blue-shift of these peaks (~ 6 meV) was observed. Finally, a broad and weak peak on the low-energy side of the spectrum is observed. In the de-convolution of the spectrum, this was modelled as a single peak at 1.287 eV, with k = 0.5.

Table 6.1: Photoluminescence bands excited from CdTe nanowires in this work and their assignments. See Fig 6.8 and Fig 6.11, and text in Section 6.3.6.

Region	Energy (eV)	*k*	Notes	Assignment	Origin
Near Edge	1.614		Above-gap emission seen in only a few samples	FE or A^0X with anti-Stokes process	Ag, Cu or Na
	1.589		Strong line S = 1.8 (for A^0X series)	A^0X	Ag, Cu or Na
	1.569	1.27	Strong line	A^0X – 1LO (+ unassigned feature)	Ag, Cu or Na
	1.548	1.13	Weaker line. Lower k value than normal for excitonic, but > 1, not eA^0	A^0X – 2LO	Ag, Cu or Na
	1.539	-	Weak shoulder of 1.548 eV peak	Not assigned	
	1.529	-	Weak shoulder of 1.548 eV peak	A^0X – 3LO ?	Ag, Cu or Na
DAP region	1.491	0.76	S = 2.5 (for DAP series)	DAP	
	1.472	0.75		DAP – 1LO	
	1.452	0.77		DAP – 2LO	
	1.432	0.74	Strongest peak in series	DAP – 3LO	
	1.412	0.73		DAP – 4LO	
	1.392	-		DAP – 5LO	
	1.372	-		DAP – 6LO	
Deep region	1.287	0.5	Weak and broad	DAP	Au

6.3.3 Post-growth annealing of nanowires

The results of annealing the wires on both the PL spectra and morphology of the wires as revealed by SEM are shown in Fig 6.10.

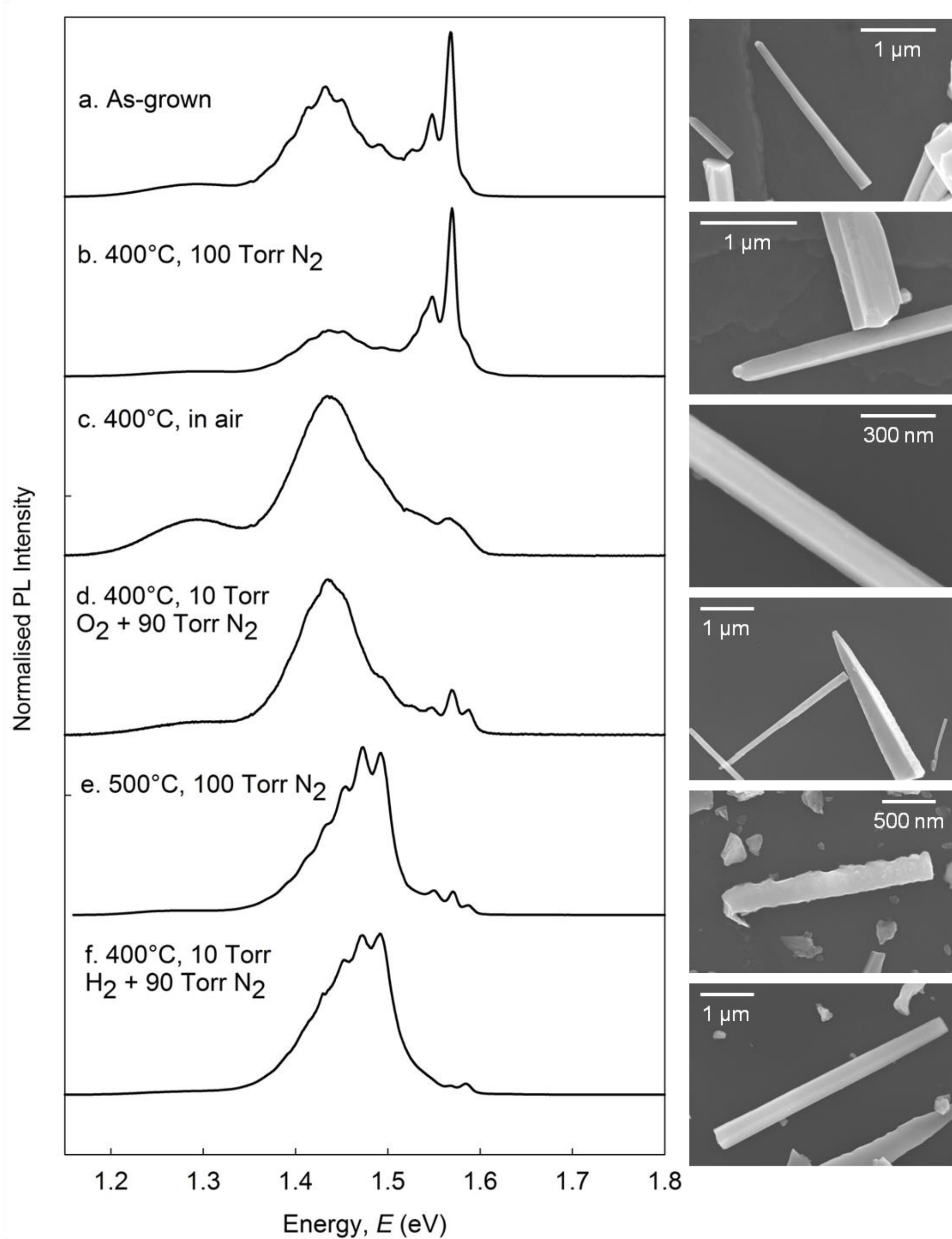

Fig 6.10: Normalised PL spectra of (a) As-grown NWs and NWs annealed in (b) 100 Torr N_2 at 400°C (c) air at 400°C, (d) 10 Torr O_2 + 90 Torr N_2 at 400°C, (e) 100 Torr N_2 at 500°C and (f) 10 Torr H_2 + 90 Torr N_2 at 400°C. For all samples, NWs were mechanically removed onto Si substrates with the spectra being recorded under ~ 60 mW/cm^2 of illumination at 4K. SEM images for each sample are shown to the right of the spectra.

Since the number of NWs sampled by the laser beam was not controlled (although typically of the order 10^7 cm^{-2}), the intensity of each spectrum was normalised by equalising

the heights of the highest peaks from spectrum to spectrum, with the relative heights being used for comparative study. The samples are now discussed in three groups, assigned by the character of their PL spectra.

6.3.3.1 As-grown and annealed in 100 Torr N_2 at 400°C (samples A and B): Fig 6.10 shows that the effect of annealing under nitrogen at moderate temperatures was to increase the relative intensity of excitonic over DAP emission. This is shown more clearly in Fig 6.11a whereby the spectra for as-grown and annealed are directly compared. The higher-resolution spectrum of the annealed NWs shown in Fig 6.11b, recorded using the 1200 line/mm diffraction grating instead of the 150 line/mm grating, reveals a new but weak peak that is introduced by annealing, at 1.614 eV – an energy exceeding that of the CdTe band-gap at 4K (1.605 eV). The Huang-Rhys coupling parameter for the series of peaks at 1.589, 1.569 and 1.548 eV was calculated to be S = 1.8, i.e. similar to that for as-grown NWs.

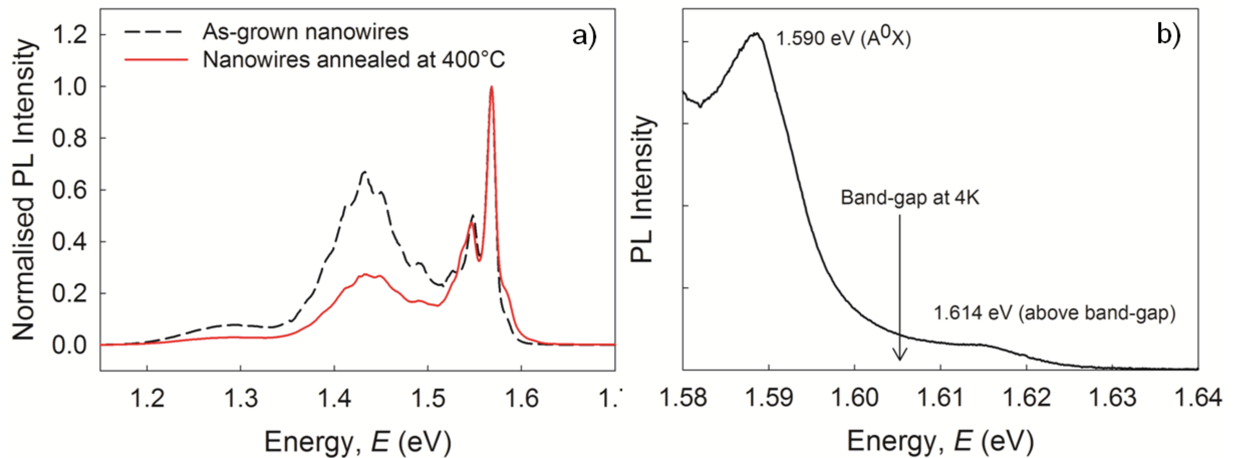

Fig 6.11: a) PL spectrum of NWs after annealing at 400°C under 100 Torr of nitrogen for 30 minutes (solid red line), normalised to the highest intensity peak at 1.569 eV, along with the as-grown spectrum (dashed black line) for comparison. b) Higher-resolution spectrum of the high-energy region showing above-gap luminescence for the annealed NWs.

6.3.3.2 Annealing in the presence of oxygen (samples C and D): Annealing in the presence of oxygen acts to quench the near-edge emission and so the DAP luminescence dominates the normalised spectra (Fig 6.10c and d). Moreover, the structure of both the near-edge and DAP emission is degraded, with the identity of individual peaks and the appearance of individual phonon replica peaks being lost. Furthermore, the air annealed sample shows a new minor peak at 1.523 eV, and its SEM image shows visible surface change.

6.3.3.3 Reducing and high temperature annealing conditions (samples E and F): Annealing at 500°C under N_2 or at 400°C under H_2/N_2 further quenches the near-edge

luminescence and enhances the DAP emission (Fig 6.10e and f). Moreover, the DAP emission changes in character, with the strongest emission now being from the first (1.492 eV) or second line (1.472 eV) in the series rather than the fourth (1.432 eV). Indeed, the Huang-Rhys coupling parameter is reduced to $S = 0.7$ from its value of 2.5 in the as-grown samples. The exponents k for the zero-line and the first two phonon replicas of the DAP series in sample E (annealed at 500°C) are in the range 0.82 – 0.84, as shown in Fig 6.12. For both samples E and F, roughening of the sidewalls was observed for most of the NWs in SEM.

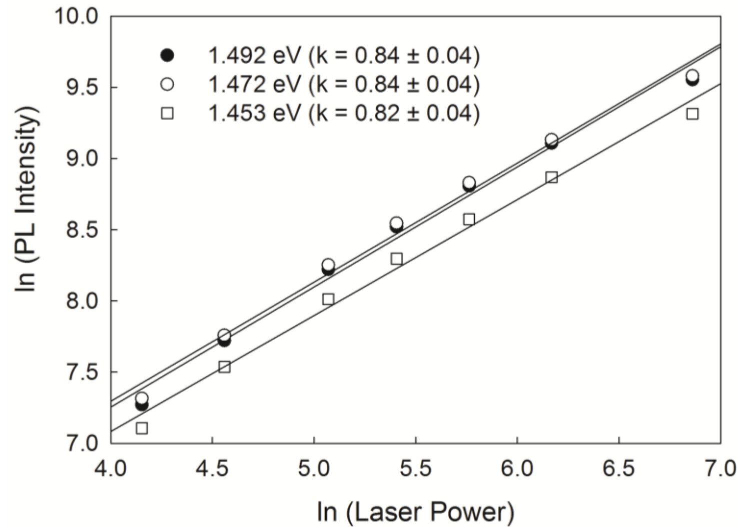

Fig 6.12: Laser excitation intensity dependence of the PL intensity for three features within the low-energy defect band region (1.4 – 1.5 eV) for sample E – NWs annealed in 100 Torr N_2 at 500°C.

6.3.4 Temperature dependence of photoluminescence spectra

Fig 6.13a shows the PL spectra obtained at different temperatures, in the range 7 - 200K for the NWs annealed at 400°C under 100 Torr N_2 for 30 minutes (sample B). It is shown that across the whole spectrum, the PL intensity decreases with increasing temperature. This thermal quenching is more pronounced for the high-energy excitonic region, i.e. > 1.5 eV, than for the DAP region, i.e. the broad-band from 1.35 – 1.50 eV. Arrhenius plots of the three excitonic features at 1.589, 1.569 and 1.548 eV, and of the broad DAP band centred at 1.440 eV – the fine-structure of this band being lost at high temperature – are shown in Fig 6.13b, clearly highlighting that the DAP band exhibits a slower decay. These plots are fit with, a theoretical expression that simulates the presence of two thermal activation processes (Equation 4.8, Chapter 4). The thermal activation energies of the quenching process, E_1 and E_2, used to obtain the best fit to the experimental data with this expression, are listed in Table 6.2.

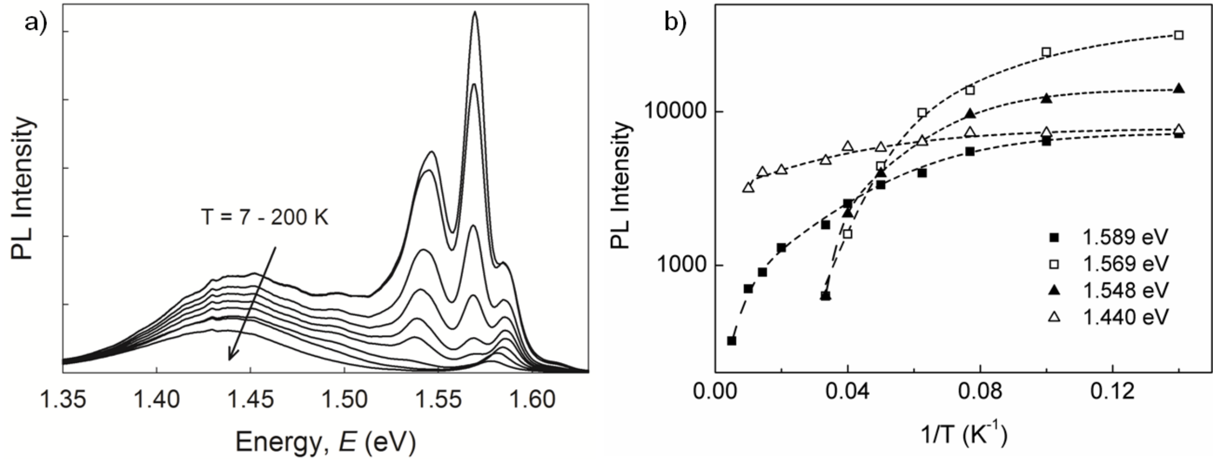

Fig 6.13: a) PL spectra of NWs annealed at 400°C under 100 Torr N_2 for 30 minutes, taken at increasing temperatures in the range 7 – 200K. b) Arrhenius plots of the intensities of four of the main peaks in the PL spectra, centred at 1.589 (solid squares), 1.569 (empty squares), 1.548 (solid triangles) and 1.440 eV (empty triangles). These plots are fit with a model (Equation 4.8, Chapter 4) used to obtain thermal activation energies (see Table 6.2) associated with the quenching of PL.

Table 6.2: Activation energies, E_1 and E_2, of the low temperature and high temperature quenching processes, extracted from analysis of the temperature-dependence of PL of sample B (NWs annealed at 400°C in 100 Torr N_2) using models described in the text.

Peak (eV)	E_1 (meV)	E_2 (meV)
1.589	3.9 ± 0.1	25 ± 6
1.569	3.0 ± 0.4	12 ± 2
1.548	5.2 ± 0.4	34 ± 2
1.440	2.8 ± 0.5	160 ± 10

At low temperatures, the spectra are dominated by the peak at 1.569 eV, it being significantly stronger than the 1.589 eV peak. On the contrary, at higher temperature the 1.569 eV peak is the strongest (not considering the DAP band in this case) - the exact value of its spectral position is gradually red-shifted with temperature due to the temperature-dependence of the optical band-gap. Assuming these features are phonon-related (see Table 6.1 and the text in Section 6.3.6), this can be described as a reduction in the Huang-Rhys coupling parameter with increased temperature, from 1.8 ± 0.1 at 7K to 0.35 ± 0.1 at 30K (Fig 6.14).

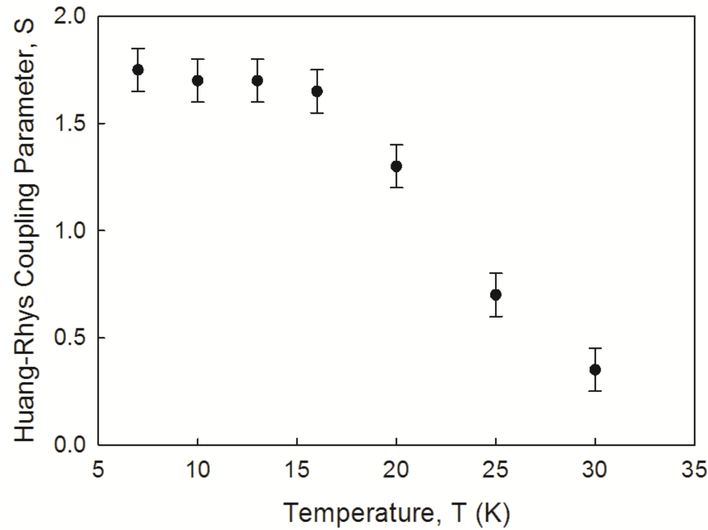

Fig 6.14: Temperature-dependence of the Huang-Rhys coupling parameter, *S*, associated with the near band-edge excitonic series, i.e. the peaks at 1.589, 1.569 and 1.548 eV, for sample B (NWs annealed at 400°C in 100 Torr N_2.

6.3.5 Time-resolved photoluminescence

PL spectra and decay curves of CdTe NWs, which had been grown using a different source of CdTe than all other NWs analysed in this Section, are shown in Fig 6.15.

Fig 6.15a shows the near-band edge region (1.50 – 1.60 eV) of the PL spectrum (at 5K) of these NWs. The spectral resolution is inferior compared to that presented in Fig 6.9, and the spectral positions of the features observed are different. Nevertheless, three main peaks were identified for decay measurements, at 1.598, 1.576 and 1.555 eV, these decay curves being shown in Fig 6.15b – d respectively (at both 5 and 20K). The origins of these peaks are discussed in Section 6.3.6.

Whereas the highest energy peak, at 1.598 eV, was fitted with a bi-exponential decay, the two peaks at 1.576 and 1.555 eV were fitted with mono-exponential decays; the decay constants obtained from these fits, at 5K and 20K are listed in Table 6.4. The decay constant associated with the slow component of the decay of the 1.598 eV peak (2.72 ± 0.03 ns at 4K) is comparable to the single decay constants of the other two features, i.e. in the range 2 – 3 ns. For all peaks, the decay constants are shorter at 20K than at 5K.

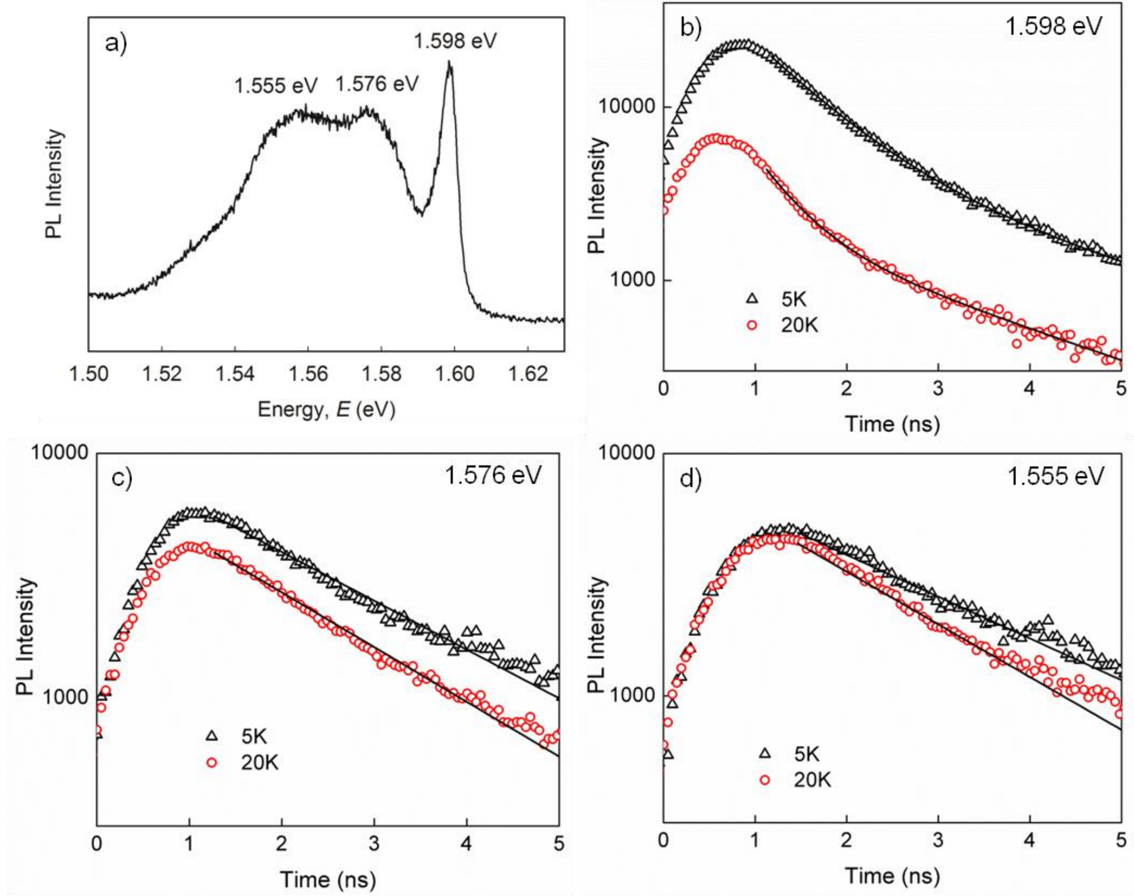

Fig 6.15: a) PL spectra of CdTe NWs annealed at 400°C in 100 Torr for 30 mins. These NWs were grown from a different CdTe source than those analysed in Sections 6.3.2 - 6.3.4 and have slightly different spectral features. PL decay curves for the b) 1.598, c) 1.576 and d) 1.555 eV peaks at 5 and 20K are also shown.

Table 6.3: Decay constants obtained from the PL decay curves of peaks at 1.589, 1.576 and 1.555 eV, for NWs annealed at 400°C under 100 Torr N_2 for 30 mins.

Peak (eV)	τ at 5K (ns)	τ at 20K (ns)
1.598	0.76 ± 0.03 (τ_{fast})	0.44 ± 0.02 (τ_{fast})
	2.72 ± 0.03 (τ_{slow})	2.25 ± 0.20 (τ_{slow})
1.576	2.10 ± 0.10	1.94 ± 0.03
1.555	2.32 ± 0.20	2.00 ± 0.10

6.3.6 Discussion

The origins of the peaks and their behaviour are now discussed. First, it is noted that the ratio of near band-edge, i.e. exciton related, PL emission to DAP emission is often used as a measure of the ‘quality’ of CdTe, this being influenced both by microstructure and the populations of point defects participating in the transitions[32]. In this sense, the PL spectra of

isolated NWs are far superior to those of the polycrystalline CdTe films and the NW arrays on films, as the former exhibits stronger excitonic emission (Fig 6.8). Moreover, the fine structure observed in the spectra of the isolated NWs is typical of PL from single-crystal materials. The reduced DAP recombination is considered to be beneficial for solar cells. For the case of the NWs arrays on films, it may be inferred that the layer dominates the PL emission, considering the similarity of the spectrum to that of the CdTe film alone. The presence of the NWs in this configuration merely contributes to inhomogenous broadening of the spectra due to a range of NW diameters.

6.3.6.1 Assignment of peaks in spectra of isolated as-grown NWs: The origin of the peaks in the PL spectra of isolated CdTe NWs (Fig 6.8 and 6.9), as summarised in Table 6.1 are now discussed. Since the NWs might be expected to be contaminated by the Au catalyst (and possibly its minor impurities) special consideration has been given to the contributions to the luminescence from Au, Cu, Ag and Na, with the relevant literature reports being shown in Table 6.4.

Firstly, the excitonic region with peak energies greater than 1.5 eV: Here, the most intense lines were at 1.589, 1.569 and 1.548 eV. Peaks at these energies are reported to be associated with excitons bound to neutral acceptors, A^0X, and their phonon replicas. Indeed, these lines are separated by the LO phonon energy (20 – 21 meV), and for the case of the 1.569 and 1.548 eV lines, the exponents k extracted from $\ln I - \ln L_{ex}$ plots were 1.27 and 1.13 respectively (Fig 6.9) – excitons having exponents of $k > 1$ (see Section 4.3.9 and Ref. 33). The lack of any observable L_{ex}-dependence of these peaks' spectral positions is as expected for defect-bound excitons. It is noticeable that the most intense line in this phonon replica series is the first phonon replica (A^0X-1LO) peak at 1.569 eV, and while this is uncommon there are reports of it for CdTe[34], ZnO[35-37] and GaN[38]. The intensities of phonon replica peaks is normally attributed to the strength of the electron-phonon coupling arising from the Frölich potential, and this is usually strong for CdTe. Indeed, for these peaks the Huang-Rhys coupling parameter was estimated as $S = 2.0$. Although the fit of the peak intensity series to the Poisson envelope was not good, as there is no such discrepancy for the DAP phonon replica series, it is concluded that the luminescence is not perturbed from the bulk on account of the presence of surface defects, as has been postulated elsewhere[36, 37]. Instead it is speculated that the poor fit is attributable to an overlap of the A^0X-1LO peak with an unidentified emission line, and the fact that the (combined) line does not have a pure Gaussian shape supports this possibility.

Magnea's review[39] indentifies the following principal bound exciton PL line energies (recorded at 1.8K): Ag^0X - 1.58848, Cu^0X 1.58956, Na^0X – 1.58916 and Au^0X – 1.57606 eV. It is clear from this that the Au^0X line is absent from the NW spectra whereas it is reported as present for diffused[40] and implanted[41] samples. There was also no match to the positions of Au^0X phonon replica lines. However, the luminescence is consistent with A^0X emission from either Ag, Cu or Na which may be present from impurities in the Au (Ag 80, Cu 20 ppm) or from the glass (Na). Since these lines lie within 0.00112 eV of one another and within 0.0006 eV of the peaks measured here, this experiment cannot distinguish between them. Therefore, the line at 1.589 eV has been assigned to be A^0X (A being possibly Ag, Cu or Na), and the 1.569 and 1.548 eV lines as its phonon replicas (as shown in Table 6.1). From the levels of Ag and Cu in the Au, and the fact that Na would have to diffuse from the glass, the most likely acceptor is considered to be Ag followed by Cu and then Na. Given the lack of near edge Au luminescence, matches to other Au-related lines were also looked for in this region, these being the series of three lines assigned to the neutral complex Au_{Cd} – Au_i by Molva[40], as shown in Table 6.4, and having energies 1.57210, 1.53850 and 1.52668 eV. However, there is no match to the first (1.57210 eV), and it is considered unlikely that the second two (1.53850 and 1.52668 eV) were hidden under the lines at 1.539 and 1.529 eV for the following reasons: a) Molva reports that the three complex lines *only* appear alongside the Au^0X line, which is missing here; and b) Molva reports that all three complex lines appear together, but the first is clearly missing from our spectra. Overall, there is no evidence of Au related near-edge emission from these samples, although deeper emission is reported below. The reader is referred to Section 6.3.6.2 for a discussion of the above-gap emission seen in some of the heat-treated samples. Later, in Section 6.3.6.4 some evidence of Au-related near-edge emission in separate samples, grown from a different CdTe source, is discussed.

The series of peaks in the DAP region (1.35 – 1.5 eV) is widely seen in CdTe. Here, the 1.492 eV peak is assigned to be the DAP zero-phonon line, with the lower energy peaks being its phonon replicas: The *k* values of the first five lines (in the range 0.73 – 0.76) are comparable, and typical for DAP emission, and their energy separation (19 - 20 meV) is close to the LO phonon energy. The measured coupling parameter, $S = 2.5$, is typical for the *A*-centre [Cl_{Te}-V_{Cd}] in CdTe, although in these samples there were no intentionally introduced halogens. Moreover, the blue shift of this band (~ 6 meV), observed upon increasing the excitation intensity in the range 60 – 2000 mW/cm^2, is expected for DAP transitions, since the energy of emitted photons is dependent on the Coulomb potential, which is inversely proportional to the spatial separation of donors and acceptors: Increased excitation intensity

gives an increased photo-excited carrier concentration leading to increased free carrier screening so that the more closely spaced DA pairs dominate. However, since the DAP spectra from CdTe is usually at very similar energies, even for material doped with a wide range of impurities, it is only possible to infer its origin from knowledge of the impurity content of the particular samples. Hence the participating acceptor is inferred to be Ag, Cu or Na in order of decreasing probability (as discussed above).

Table 6.4: Literature reports of photoluminescence lines due to Au, Cu and Na. Values marked * are the positions of phonon replica lines estimated using an LO phonon energy of 21.2 meV[39], and are not shown in the spectra in the references given. They are included for comparison with the lines observed in this work.

(Au) Molva [40] (eV)	**(Au) Hamman [41] (eV)**	**(Au) de Nobel [42] (eV)**	**(Cu) Hamman [41] (eV)**	**(Cu) Magnea [39] (eV)**	**(Ag) Magnea [39] (eV)**	**(Na) Magnea [39] (eV)**
1.57606 Au^0X	1.5761 Au^0X		1.5896 Cu^0X	1.58956 Cu^0X	1.58848 Ag^0X	1.58916 Na^0X
1.55486 Au^0X – 1LO				1.56836 Cu^0X – 1LO	1.56728* Ag^0X-1LO	1.56796 Na^0X-1LO
1.53366 Au^0X – 2LO				1.54716* Cu^0X – 2LO	1.54608* Ag^0X-2LO	1.54676* Na^0X-2LO
1.57210 ‘C_1^{Au}’ Au_{Cd} – Au_i neutral				1.52596* Cu^0X – 3LO	1.52488* Ag^0X-3LO	1.52556* Na^0X-3LO
1.53850 ‘C_2^{Au}’ Au_{Cd} – Au_i neutral				1.50476* Cu^0X – 4LO	1.50368* Ag^0X-4LO	1.50436* Na^0X-4LO
1.52688 ‘C_3^{Au}’ Au_{Cd} – Au_i neutral						
DAP series of 6 peaks centred at 1.28	DAP series centred at 1.267	1.287				

The weak broad peak on the low energy side of the spectrum in Fig 6.8, at 1.287 eV is now discussed: It has a *k* value of 0.5, which is consistent with DAP emission. This peak is also consistent with reports of Au-related DAP luminescence: Molva recorded a phonon replica series for CdTe:Au with the peak of the envelope being in the range 1.275 – 1.284 eV; Hamann’s implanted sample had a broad peak at 1.267 eV and de Nobel’s[42] work at 77K had a peak at 1.27 eV. The possibility that this line is oxygen related is also considered (since

results presented later involve air annealing). However, since the deep oxygen emission is generally at a lower energy, as shown by Vatavu[43] for example, the 1.287 eV emission is assigned to Au.

6.3.6.2 Post-growth annealing of NWs: The increase in the relative intensity of the excitonic emission upon annealing at 400°C under 100 Torr N_2 (Fig 6.11) presumably results from the reduction in concentration of one of the (electrically active) centres that participates in the DAP transition. This can be considered to be a beneficial impact in the context of the NWs potential use in PV devices.

The above band-gap emission at 1.614 eV, introduced upon annealing, is unusual and has only been observed previously on rare occasions. The origins of above-gap emission from CdTe are discussed by Tkachuk[44] and include phonon absorption (LO, transverse optical (TO) and transverse acoustic), excitonic and indirect transitions – a variety of such processes are possible. Tkachuk specifically attributes emission at 1.614 eV to an anti-stokes process involving the free exciton and a TO phonon. Lee *et al.* observed luminescence centred at 1.615 eV (comparable to 1.614 eV in this work) at 4.9K for as-grown *p*-type CdTe, and attributed it to an anti-Stokes process involving an acceptor-bound exciton[45]. As free exciton emission is not seen in this sample – at 1.598 eV – the latter is considered to be more probable. For material with strong electron-phonon coupling, as is the case here, a large number of phonons are emitted via the Stokes process making phonons available for absorption even at such low temperatures. Indeed, the coupling parameter of the A^0X series, S = 1.8, is consistent with this.

Particularly for the samples annealed in oxygen, the fine structure in the spectra was degraded, and as this effect was greatest for the sample annealed in the greater partial pressure of oxygen (sample C), one may speculate it is an effect of oxidation. Annealing in reducing or high temperature conditions changed the character of the DAP emission. The reduction in the coupling parameter S, from 2.5 in the as-grown samples, to 0.7 indicates much reduced electron-phonon coupling. The k values of the 1.492, 1.472 and 1.452 lines (in the range 0.82 - 0.84) indicate the transitions remain of DAP type however. There is some evidence in the literature that weak phonon coupling is a signature of transitions associated with extended defects or surfaces. Emission at 1.49 eV for example, has been linked to surfaces[46, 47] although not without controversy[48]. Nevertheless, of all the samples A-F examined, only E and F showed visible signs of surface degradation in the SEM.

6.3.6.3 Temperature-dependence of photoluminescence: The quenching of the PL across the entire spectra with increased temperature is typically attributed to the thermal activation of

non-radiative transitions. The observation that excitonic emission is quenched to a greater extent than DAP emission is understandable, considering that at temperatures for which kT exceeds the exciton binding energy, excitons may dissociate. Good fits to the Arrhenius plots of the 1.589, 1.569, 1.548 and 1.440 eV peaks obtained using a model described by Equation 4.8 (see Chapter 4) support the assignments given to these peaks in Table 6.1, as the model is said to be appropriate for transitions involving bound-excitons (the three higher energy peaks) or DAP recombination. In the case of bound-excitons, the model assumes there are two routes of dissociation, hence E_1 corresponds to the exciton binding energy and E_2 to the impurity binding energy[49] – the values estimated from the fit for the three excitonic peaks are in the range 3.0 – 5.2 meV for E_1 and 12 – 34 meV for E_2. These values do not differ greatly from those measured in polycrystalline CdTe by Halliday *et al.*[50] for the A^0X transition (E_1 ~ 3 meV, E_2 ~ 25 meV). For the case of the DAP peak, the estimated values for E_1 (2.8 ± 0.5 meV) and E_2 (160 ± 10 meV) correspond to the binding energies of the shallow donor and deep acceptor respectively. With a CdTe band-gap of 1.605 eV at 4K, the value for the acceptor level is consistent with the broad DAP peak being positioned in the range 1.35 – 1.5 eV. Castaldini *et al.*[51] identified three deep acceptor levels in CdTe:Cl, with activation energies of 120, 140 and 160 meV, with the level at 140 meV being the only one observed in undoped CdTe. Whilst the DAP peak exhibits all the characteristics of the *A*-centre, it remains unresolved as to which impurity, *X*, is involved in forming the V_{Cd}-X_{Te} complex.

The reduction in strength of the Huang-Rhys electron-phonon coupling parameter, *S*, as sample temperature was increased (Fig 6.14) may be considered to be unusual given that higher phonon densities would be expected at higher temperature. On the other hand, the exciton concentration is reduced at higher temperatures due to their thermal dissociation. Zhao *et al.*[52] report that for highly polar semiconductors, 'hot excitons' can be formed which have varying kinetic energy, upon which *S* is dependent. Zhao states that if *S* is calculated by the integration of PL spectra, as here, then the observed dependence of *S* on sample temperature is an artefact associated with the kinetic energy dependence of *S*. Wijnen *et al.*[53] also observed a reduction of electron-phonon coupling with increased temperature, in CdSe quantum dots. Although the NWs investigated here do not have diameters comparable to quantum-scales, quantum confinement effects cannot be completely dismissed due to the possible presence of superlattice quantum wells in some of the highly twinned NWs, as discussed in Section 6.2.

6.3.6.4 Time-resolved photoluminescence measurements: The PL spectrum of NWs used for time-resolved experiments (Section 6.3.5) differed from all those presented in Section 6.3.2 – 6.3.4, the three main peaks in the excitonic region being at 1.598, 1.576 and 1.555 eV.

This may be attributed to the fact that a different CdTe source was used during NW growth, or that a shorter PL excitation wavelength was used (440 nm rather than 514 nm) which may have induced resonant effects - these measurements having been taken using the apparatus at Utrecht University rather than Durham University (see Chapter 4). The highest energy peak was observed at an energy typically associated with the free exciton, FE (1.598 eV)[54, 55]. The 1.576 eV peak exists at an energy that Molva[40] and Hamann[41] ascribed to the as yet unseen Au^0X transition. However this peak is both broadened and superimposed on a broad high intensity background. Positive identification would therefore require further high resolution PL investigation. Assignment of the peak at 1.555 eV has similar uncertainties. Nevertheless, they are likely to be bound-excitons, A^0X or D^0X (bound to a neutral donor), considering their spectral position (see Table 6.4), with the impurity involved being unidentified. The decay curve of the highest energy peak is notably different than the other two – whereas the decays of the 1.576 and 1.555 eV peaks are fit well with a mono-exponential expression, the 1.598 eV peak decays bi-exponentially. The bi-exponential decay shape suggests that the 1.598 eV peak is in fact a convolution of two smaller peaks, e.g. the FE and a bound-exciton, with the fast decay component attributed to the FE, and the slow component to the bound-exciton. Indeed the slower decay component of the 1.598 eV peak has a decay constant comparable to the decay constants of the 1.576 and 1.555 eV peaks (at both 4 and 20K), these two features being assigned to bound excitons. Moreover, the FE is rarely observed to be so intense in itself in CdTe and the feature has a non-Gaussian shape with a shoulder on the low energy side. Nevertheless, exciton lifetimes measured here (> 2 ns) are comparable to some of the longest ever measured for (non-quantum scale) CdTe[56]. This, coupled with the high ratio of excitonic to DAP emission observed for most samples suggests that the NWs may be highly suitable for PV applications.

6.4 Photoluminescence of core-shell CdS/CdTe nanowires

Low-temperature PL spectra generated from as-grown and annealed CdS/CdTe core-shell NWs are presented in this Section. PL spectra of CdS/CdTe structures are complex, but often have three distinct regions: a) near band-edge CdS luminescence (at 2.4 – 2.6 eV); b) CdTe luminescence (at 1.2 -1.6 eV); and c) an intermediate region (at 1.6 – 2.4 eV), in which luminescence can be assigned to deep-levels in CdS or to CdS_xTe_{1-x} inter-diffused layers. As inter-diffusion of S and Te is highly influential on the performance of CdS/CdTe solar cells[57], particular attention is paid to the intermediate region of the spectra upon discussing the results.

6.4.1 Experimental procedure

Au-catalysed CdTe NWs were grown on CdTe/glass substrates, (see Section 5.4) onto which CdS shell layers were sputter-grown at 200°C, with the shells being ~ 200 nm thick. Both as-grown and annealed (at 400°C, under 100 Torr N_2 for 30 mins) core-shell NWs were analysed by PL spectroscopy, with the NWs being mechanically removed onto Si substrates for measurements. Spectra were excited using the 457 nm line of a linearly polarised argon ion laser (excitation intensities of 30 – 1500 mW/cm^2), with the beam incident at 20° to the normal and the samples held at 4K in a closed-cycle He cryostat.

6.4.2 Results

A comparison of the PL spectra of as-grown and annealed CdS/CdTe core-shell NWs is shown in Fig 6.16a (spectra having been corrected for unidentified background signal). Both spectra have a number of sharp features in the region 2.4 – 2.6 eV, which are typical of the CdS near-band edge region (CdS band-gap being 2.578 eV at 4K). A broad structured band also exists in both spectra from 1.4 – 2.2 eV, which consists of overlapping peaks and shoulders and will be referred to as the ‘intermediate band’. In the spectra of the as-grown NWs, some sharp features, overlapping with this broad band, are observed at 1.5 – 1.6 eV and 1.4 – 1.5 eV.

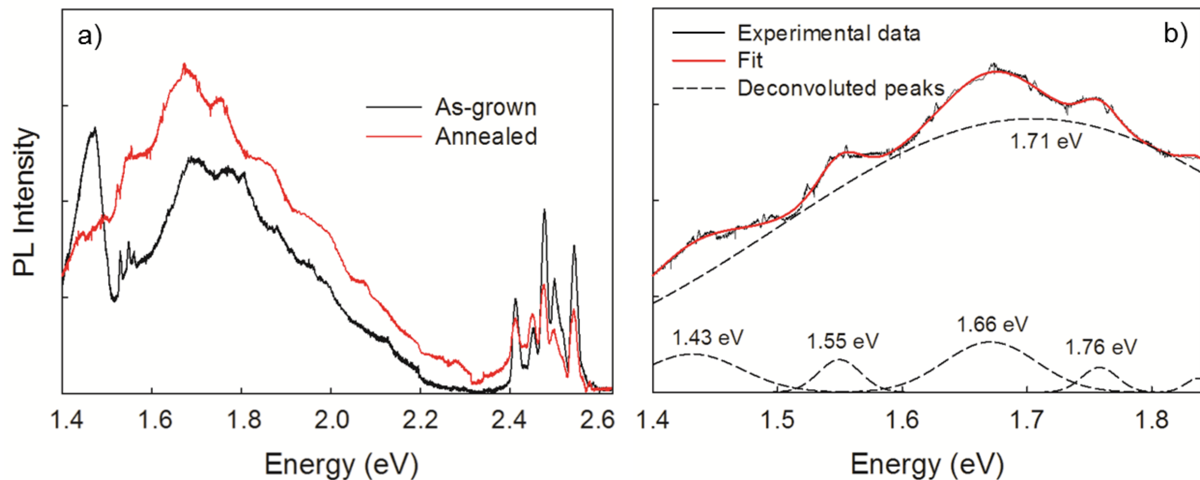

Fig 6.16: a) Comparison of PL spectra excited from as-grown (black line) and annealed (red line) isolated CdS/CdTe core-shell NWs. Annealing was carried out at 400C under 100 Torr N_2. b) Deconvolution of the intermediate PL band of the annealed sample – black line shows experimental data, dashed lines are the deconvoluted peaks and the red line is the fit generated from the deconvolution.

Gaussian deconvolutions (carried out using the *Fityk* software) of these spectra are shown in Fig 6.16b, 6.17 and 6.18. Such deconvolutions must be treated with caution however given that good fits are obtainable simply by the inclusion of more Gaussian peaks. Nevertheless, Fig 6.16b shows a deconvolution of the intermediate band from the spectra of the annealed NWs and Fig 6.17 and Fig 6.18 show deconvolutions of the entire spectra of the as-grown and annealed NWs respectively. The spectra are now described in more detail with reference to these.

In the CdS near-band edge region of the as-grown core-shell NWs (Fig 6.17), sharp peaks are observed at 2.543, 2.501, 2.479, 2.453 and 2.401 eV, and shoulders at 2.555 and 2.519 eV. From I - L_{ex} measurements, exponent values, k, for the 2.555 and 2.543 eV features were determined to be 1.04 and 1.10 respectively. Loss of spectral resolution made this analysis difficult for the other features. The intermediate region has a broad background peak centred at 1.72 eV, which overlaps with a series of peaks of similar intensity at 2.11, 1.98, 1.87, 1.77, 1.67 and 1.55 eV. The blue peaks are coloured so because they exist at energies previously assigned to transitions in bare CdTe NWs (see Section 6.3); sharp near-band edge CdTe peaks in the 1.53 – 1.59 eV region, and a DAP peak at 1.47 eV.

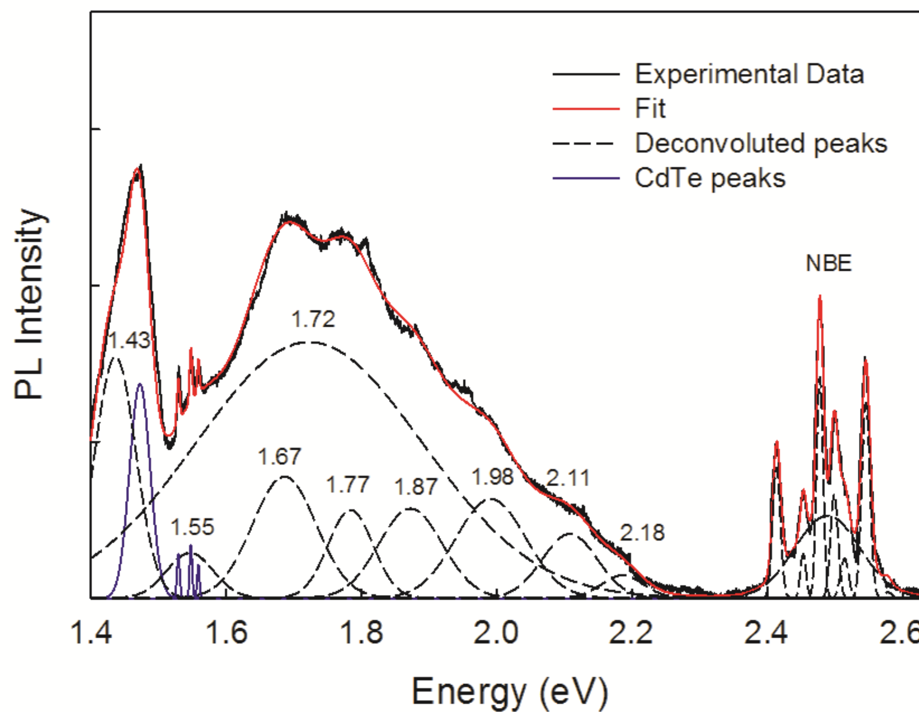

Fig 6.17: Deconvolution of PL spectra excited from as-grown CdS/CdTe core-shell NWs - black line shows experimental data, dashed lines are the deconvoluted peaks, blue lines are deconvoluted peaks assigned to CdTe emission and the red line is the fit generated from the deconvolution.

In the spectra of the annealed core-shell NWs (Fig 6.18), the CdS near-band edge features are still observed but are lower in intensity. A good fit to the intermediate band of the annealed NWs (Fig 6.16b) could be obtained by using peaks at similar energies as for the as-grown core-shell NWs, i.e. at 2.11, 1.98, 1.87, 1.76, 1.66 and 1.55 eV overlapped with a broad 1.71 eV peak. The broad peak is notably more intense than for the as-grown core-shell NWs.

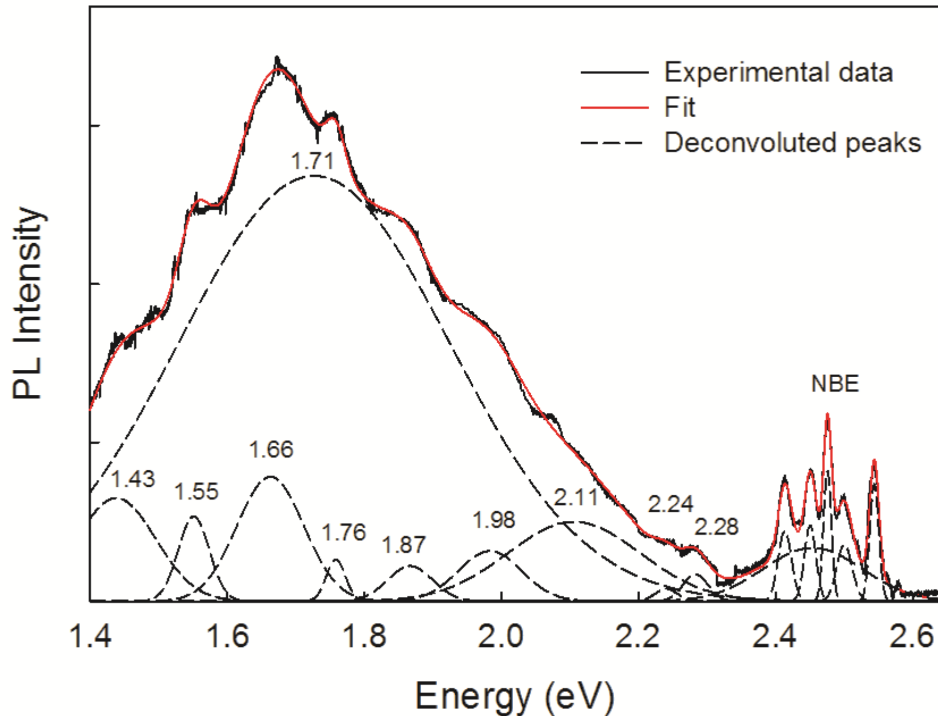

Fig 6.18: Deconvolution of PL spectra excited from CdS/CdTe core-shell NWs annealed at 400°C - black line shows experimental data, dashed lines are the deconvoluted peaks, and the red line is the fit generated from the deconvolution.

Moreover, upon annealing the features assigned to CdTe are no longer observed, but for a broad-band in the DAP region, and a new CdS feature is observed at 2.24 eV.

Assignments of each of these features to types of transitions are summarised in Table 6.5, having been made with reference to literature data (the reference being noted in the final column), these being discussed below.

Table 6.5: Photoluminescence bands excited from as-grown CdS/CdTe nanowires in this work and their assignments. See Figs 6.16 – 6.18 and text in Section 6.4.3. The references used for each assignment are included in the final column.

Energy (eV)	k	Shape + Comments	Assignment	Ref. for assignment
CdS NBE				
2.555	1.04	Shoulder	FE(A)	[59-61]
2.543	1.10	Sharp Peak	D^0X	[59, 62, 63]
2.519		Shoulder	FE(A)-1LO or hD^0	[64]
2.501		Sharp Peak	D^0X-1LO or hD^0	[64]
2.479		Sharp Peak	FE(A)-2LO or hD^0	[64]
2.453		Sharp Peak	'Y-band' – excitons localised at dislocations?	[65]
2.414		Sharp Peak	DAP involving V_S^{2-}	[66]
Intermediate				
2.24		Shoulder (appeared after anneal)	hD^0 involving Cd_i or V_S^{2-}	[67]
2.12		Shoulder	DAP transition involving Cd_i and V_{Cd}	[68, 71]
1.4 – 2.2		Broad band with 5 – 6 shoulders	'Red-band' consisting of peaks at 1.43, 1.55, 1.66 , 1.76, 1.87 and 1.98 eV attributable to transitions of electrons trapped at surface states to valence band + 1.71 eV broad band associated with Te impurities and/or V_S^{2-}	[67], [68, 69, 70]
CdTe				
1.53 – 1.59		Sharp peaks (disappeared after anneal)	NBE CdTe	See Section 6.3
1.47		Broad peak (disappeared after anneal)	CdTe DAP band	See Section 6.3

6.4.3 Discussion

First, the near-band edge CdS luminescence is discussed. Imada *et al.*[58] state that, due to spin-orbit coupling, the valence band-edge in wurtzite CdS splits into three separate sub-bands, which allows three different free-exciton transitions, namely FE(A), FE(B) and FE(C). Imada calculated that the FE(A) transition is at 2.555 eV, and it has been estimated experimentally at 2.551 and 2.553 eV by PL[59, 60], and at 2.554 eV by absorption[61] measurements. The small shoulder observed here at 2.555 eV on the high energy side of the 2.543 peak is therefore assigned to the FE(A). The exponent values of k = 1.04 for this feature is consistent with it being excitonic in nature – the observation of luminescence attributable to a free exciton only being common for single crystal CdS. The sharp intense peak at 2.543 eV is assigned to a donor-bound exciton, D^0X, according to literature values from Jeong (2.545 eV)[59], Yu (2.546 eV)[62] and Lovergine[63] (2.544 eV), its exact position depending on which donor impurity is involved. In Yu's work, the exciton was bound to a F or Cl impurity, although whilst CdS has been sputtered in the presence of CHF_3 in the equipment used here in previous work, no such F-containing gases were used in these growth experiments. The peak also has a k-value (1.10) consistent with it being excitonic.

The assignment of the features at 2.519, 2.501 and 2.479 eV are not clear: they may be phonon replicas of the FE(A) and D^0X peaks – the LO phonon energy in CdS is 37 meV, and the 2.519 peak is separated by 36 meV from the FE(A). Ekimov *et al.*[64] attribute luminescence in this region to transitions involving a free hole and the donor (hD^0). Peaks observed at 2.453 and 2.414 eV have previously been attributed to the Y-band[65] – excitons localised at dislocations – and to DAP luminescence[66] involving V_S^{-2} respectively.

Secondly, the intermediate band has been deconvoluted into a series of bands at 2.11, 1.98, 1.87, 1.77, 1.67 and 1.55, and a broad band at 1.72 eV (shown in Fig 6.17 and 6.18, but more clearly in Fig 6.16b). Although deconvolution of spectra of low-resolution must be treated with caution, this model is supported by previous work: Abken *et al.*[67] labelled this region as the 'infra-red/red band', and observed each of these peaks, (each within 10 meV of the peaks observed here, and each of comparable FWHM) in CBD grown CdS, assigning them (not including the peak at 2.12 eV) to the radiative decay of electrons trapped in surface states to the valence band – this may be expected to be significant for NWs that have a high surface-to-volume ratio. The broad feature similar to the one at 1.72 eV has been observed by Cuthbert[68] (1.72 eV), Vuylsteke[69] (1.73 eV) and Gemain[70] (1.65 eV), with the former assigning it to DAP luminescence involving Te doping of CdS – an increase in its intensity was observed with

increased Te doping - and the others assigning it to DAP luminescence involving V_S^{-2}. The FWHM observed here (0.47 eV) is highly comparable to that observed by Cuthbert (0.44 eV) for this peak. The peak at 2.12 eV has previously been associated with DAP transitions involving Cd_i-V_{Cd} complexes formed during S re-evaporation[67, 71].

In the range 1.53 – 1.59 eV, three peaks were observed, which are likely to be attributable to CdTe luminescence, as discussed in Section 6.3, as is the broad DAP band at 1.47 eV – their spectral positions being consistent with those listed in Table 6.1.

A number of differences are observed between the PL spectra of as-grown core-shell NWs and those annealed at 400°C. Upon annealing: a) the intensity of the near band edge CdS luminescence was reduced; b) the CdTe luminescence was much less intense and could not be resolved upon deconvolution; c) the intermediate band increased in intensity, particularly the 1.72 eV peak which is related to Te doping of S and/or S vacancies; and d) a new peak at 2.24 eV was observed, similar 'green-yellow' luminescence being associated with Cd interstitials and/or S loss[67]. The reduction of CdS near-band edge luminescence and the enhancement of features related to S vacancies implies the loss of S upon annealing, either to the atmosphere via re-evaporation, or by diffusion into the CdTe core. Moreover, the quenching of CdTe emission and enhancement of CdS:Te related emission would imply the diffusion of Te into CdS. It is therefore postulated that annealing promotes inter-diffusion of S and Te at the CdS/CdTe interface in these core-shell NWs, despite the lower density of grain boundaries present – inter-diffusion is typically most prominent at grain boundaries[72].

6.5 Spectrophometry and nanoprobe measurements

In this section, further optical and electrical characterisation of CdTe NWs and core-shell CdS/CdTe NWs is presented, by reflectance, transmittance and four-point probe measurements. The reflectance and transmittance measurements of NWs are compared with those of thin films.

6.5.1 Experimental procedure

For reflectance measurements, four samples were grown: 1) a CdTe NW array; 2) a CSS-CdTe thin film; 3) an ITO/CdS/CdTe core-double shell NW array; and 4) an ITO/CdS/CSS-CdTe planar stack, all of which were on sputtered-CdTe/glass. The CdTe NWs were grown as described in Chapter 5, and ITO and CdS shells were sputtered at room temperature and 200°C respectively. For the planar samples, the same growth conditions were used (T_{source} = 570°C, T_{sub} = 520°C, P = 10 Torr of N_2, t = 15 mins for CdTe growth) but the Au deposition

step was omitted. For transmittance measurements, an additional control sample of sputtered-CdTe/glass was also prepared.

Reflectance data shown in Section 6.5.2 represents the combined specular and diffuse reflectance of samples, taken using an integrating sphere in a Shimadzu SolidSpec-3700 spectrophotometer. Direct transmittance measurements were taken in the same system. All optical measurements of NWs were taken with the NWs remaining on their substrates.

For 4-point probe measurements, both CdTe NWs and core-shell CdS/CdTe NWs (grown as above, but without deposition of the ITO) were mechanically removed onto Au-grid covered Si substrates. Current-voltage measurements were carried out in the Nanoprobe (see Chapter 4) in a bias range of -1V to +1V.

6.5.2 Spectrophotometry of nanowires and planar film

Combined spectral and diffuse reflectance measurements of a planar CdTe film and a CdTe NW array are shown in Fig 6.19a, and of a planar ITO/CdS/CdTe stack and a core-double shell ITO/CdS/CdTe NW array in Fig 6.19b. The CdTe NWs show a significant decrease in reflectivity relative to the CdTe film, with both the above- and below-gap regions showing reductions by factors of 100 and 10 respectively. A similar trend is observed for the ITO/CdS/CdTe NW and planar structures.

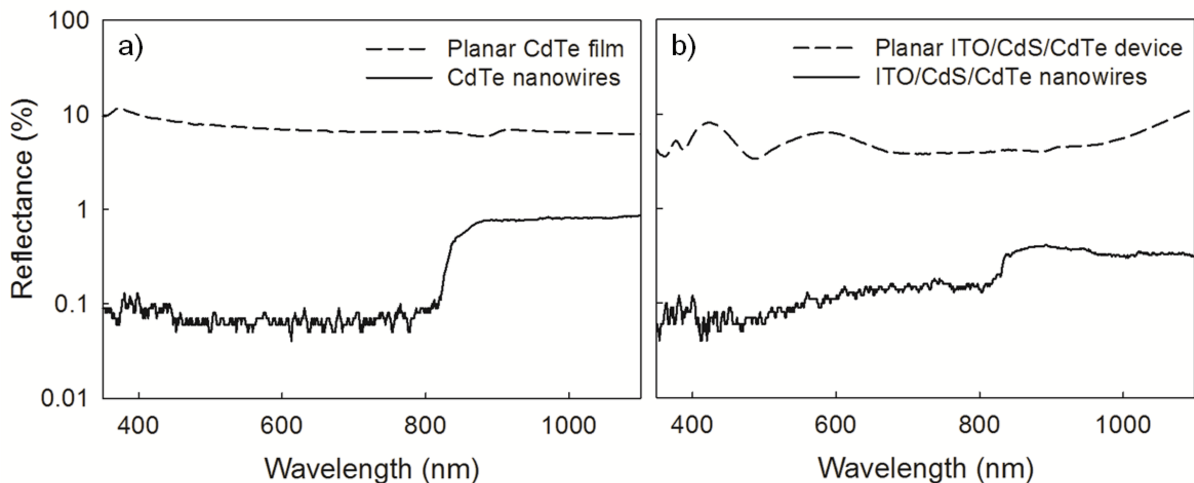

Fig 6.19: Log plots of integrated reflectance data taken from a) a planar CdTe film (dashed line) and a CdTe NW array (solid line) and b) planar ITO/CdS/CdTe stack (dashed line) and a core-double shell ITO/CdS/CdTe NW array (solid line).

The transmittance of a sputtered-CdTe film, a CSS-CdTe/sputtered-CdTe bi-layer and CdTe NWs/sputtered-CdTe is shown in Fig 6.20a. In the above-gap region, interference fringes are observed for the sputtered-CdTe and NW samples. Of the three samples, the NW

array shows the lowest transmittance, T, in both above- and below-gap regions, T being as low as $\sim 0.2\%$ in the range 400 – 600 nm. The band-gap is determined for NW/sputtered-CdTe and CSS-CdTe/sputtered-CdTe samples from the intercept of $(\alpha h\upsilon)^2 - h\upsilon$ plots. The results were $E_G = 1.48 \pm 0.01$ eV for the planar film and $E_G = 1.47 \pm 0.01$ eV for the NW array.

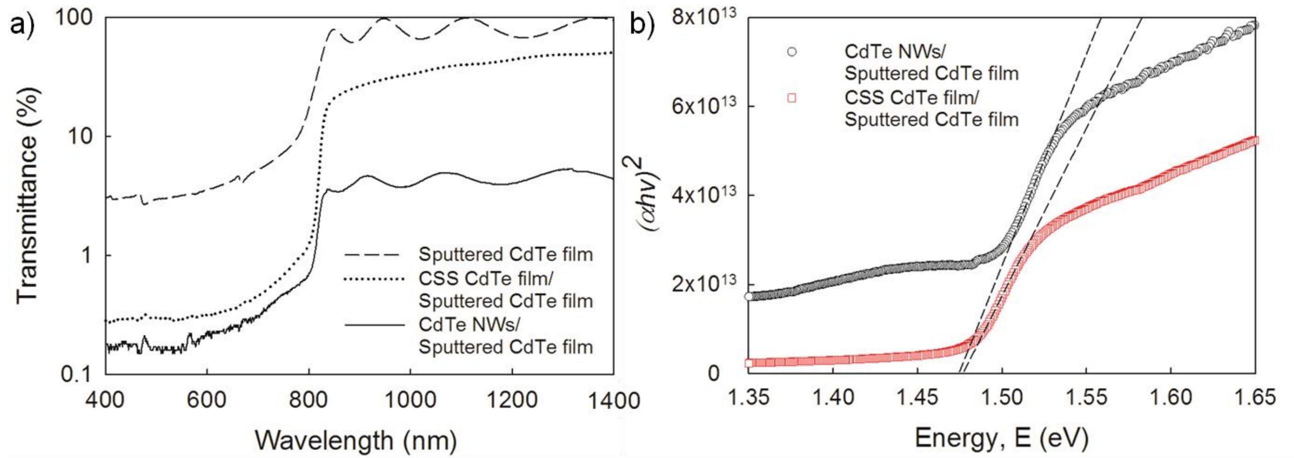

Fig 6.20: a) Direct transmittance of sputtered-CdTe film (dashed line), CSS-CdTe/sputtered-CdTe bi-layer (dotted line) and CdTe NWs/sputtered-CdTe (solid line). b) $(\boldsymbol{\alpha h\upsilon})^{\mathbf{2}} - \boldsymbol{h\upsilon}$ plots for CdTe NWs/sputtered-CdTe (black circles) and CSS-CdTe/sputtered-CdTe (red squares)

6.5.3 Resistivity measurements of nanowires

An example of the four-contact arrangement made to an individual CdS/CdTe core-shell NW using tungsten STM tips is shown in the secondary electron image in Figure 6.21a. Figure 6.21b shows the linear current-voltage response acquired from the NW.

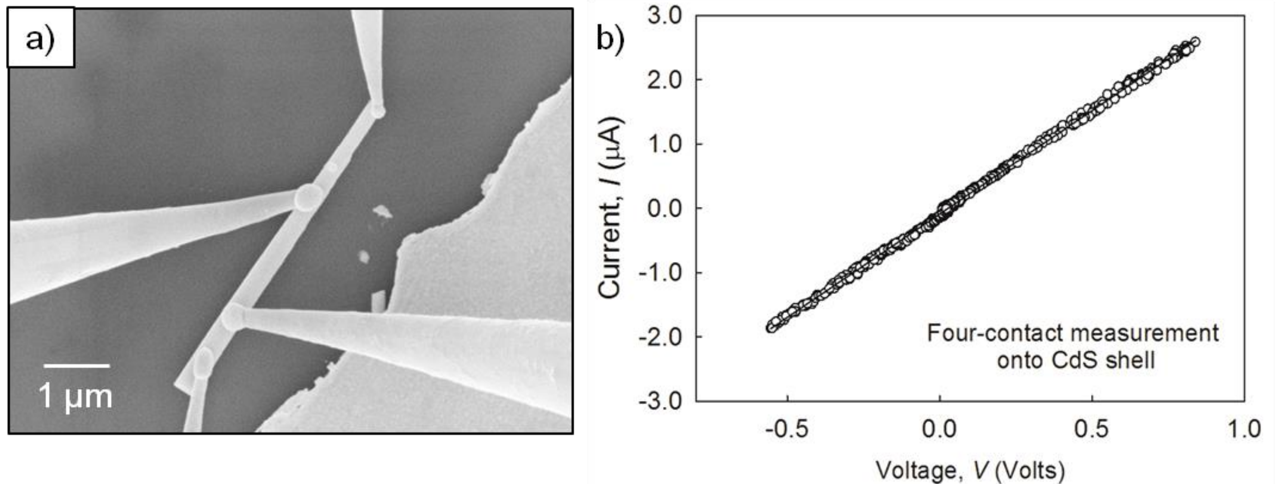

Figure 6.21: a) Secondary electron image showing tungsten STM tips contacting a CdS/CdTe core-shell NW in the four-contact arrangement. b) Current-voltage response of the core-shell NW.

As CdS is typically more conductive than undoped CdTe, it is assumed that this measurement is dominated by the response from the CdS – all the contacts are made directly to the outer CdS shell. The resistivity of the CdS shell, assuming it is a 6 μm long nanotube with 200 nm thick tube walls, was calculated to be $\rho = 0.7 \pm 0.4$ Ω.cm.

Measurements of bare CdTe NWs were unsuccessful as the measured current was too low, even at biases of up to 10V.

6.5.4 Discussion

The reflectance and transmittance measurements suggest that NW arrays have the ability to absorb light more efficiently than planar films of equivalent volumetric material. A reduction from ~ 10% reflectance for planar films, to ~ 0.1% for NWs throughout the above-gap region is a significant improvement. Additionally, lower transmittance was measured for the NW/sputtered-CdTe sample than for the CSS-CdTe/sputtered-CdTe sample (also of equivalent CdTe volume). Indeed, the reduced transmittance through the NW sample is equivalent to that which would be expected had the CSS-film been grown thicker. This may imply that scattering of photons by the NW array increases the path length, and therefore the absorption, of photons within the CdTe – this would translate to enhancements to J_{SC} in solar cells. However, it is noted that these measurements only account for direct transmittance.

The band-gaps determined from the $(\alpha h\upsilon)^2 - h\upsilon$ plots for the CSS-CdTe/sputtered-CdTe bilayer (1.48 ± 0.01 eV) and the NW/sputtered-CdTe sample (1.47 ± 0.01 eV) were identical within error bounds. In the former case, the band gaps of the CSS-CdTe and sputtered-CdTe are not expected to differ. In the latter case, the measurement cannot accurately distinguish the band gap of the NWs themselves from that of the film since the absorption onset should be dominated by the lowest band gap. Nevertheless, quantum confinement-induced band gap widening in the NWs is not expected given their size. Transmittance measurements of isolated NWs that had been mechanically removed onto glass substrates were also inconclusive since the generated NW densities were too low.

The inability to successfully measure the resistivity of bare CdTe NWs (owing to the current being lower than that measurable by the system) may imply their resistivity is particularly high, exceeding that of as-grown CdTe films. However, the same measurement failure occurred when measuring planar CdTe films, hence it is presumed that the resistivity is caused by Schottky barriers between the tungsten STM tips and the CdTe. Indeed, to form an Ohmic contact with CdTe, a metal with a work function comparable to, or higher than, that of CdTe (~ 5.7 – 5.9 eV) is required, whereas the work function of tungsten (4.54 – 4.91 eV) is

too low[73]. Nevertheless, a successful measurement of the CdS resistivity was made, the value of $\rho = 0.7 \pm 0.4\ \Omega$.cm being comparable to that achieved by Romeo *et al.*[74] for CdS films sputtered at 200°C (~ 1 Ω.cm). The assumption that this measurement is representative of the CdS shell only and not the CdTe core (i.e. the current flows predominantly through the CdS) is considered to be reasonable given that as-grown CdTe resistivities are typically a few orders of magnitude larger than this.

6.6 Conclusions

In this Chapter, the physical properties of isolated CdTe NWs and CdS/CdTe core-shell NWs, and of NW arrays intact on their substrates have been investigated, and compared to those of planar films.

First, the microstructure of the CdTe NWs was evaluated by TEM (Section 6.2), it being shown to be dependent on their growth axes. Extended defects in the wires comprise stacking faults, polytypes and twins only. Annealing did not influence their incidence or type, and they were determined solely by the orientations of the wires. Since they were grown on polycrystalline films, the wires adopted neither a single growth axis nor a fixed tilt angle with respect to the substrate. Three growth axes dominated and these were <110> at 20% incidence with no planar faults, <111> at 50% incidence with inclined planar faults and <112> at 30% incidence with the highest density of planar faults and lying within the growth axis. For CdTe and other sphalerite semiconductors, these planar defects do not disrupt bonding significantly, and have very little intrinsic electrical activity in pure samples. The recombination activity of these defects is correspondingly low and it may therefore be said that they are not likely to interfere with PV performance in these materials.

The growth axes also affected the cross-sectional geometry of the NWs, with a <111> NW adopting a hexagonal shape, and a <112> NW adopting a rectangular shape – a NW's shape is thought to have an impact on its optical and electrical behaviour[29]. Sputter deposited CdS shells were observed to grow epitaxially onto the CdTe NWs. An epitaxial CdS/CdTe interface is considered to be desirable for PV applications, owing to the reduction of recombination that is associated with reducing the density of lattice-mismatch induced surface states.

In Section 6.3, PL spectroscopy of CdTe NWs, used to evaluate the point defects present within, was presented. Low temperature photoluminescence of the wires showed that they have strong near-band edge features and weak DAP luminescence that is characteristic of

single crystal CdTe, rather than the degraded spectra that are normally associated with polycrystalline films. Moreover, annealing under nitrogen at 400°C acts to further improve the crystal quality; that is the relative strength of the near edge compared to DAP emission lines. For the annealed samples, the rarely observed above-gap luminescence was observed, this being attributed to anti-Stokes emission with the participation of an exciton. Such emission is associated with materials having high electron-phonon coupling, which is the case for CdTe. This is supported by the observation of particularly strong phonon coupling to the (A^0X) transition. The dominance of the near-edge emission indicates that the as-grown and annealed wires have sufficiently high optoelectronic quality to make them potentially superior to thin films for PV applications.

Perhaps surprisingly, the spectra did not reveal any exciton band luminescence that could be attributed to the presence of Au (from the catalyst) in the CdTe. Certainly the published accounts of Au acceptor bound exciton luminescence from CdTe:Au show strong lines in positions that could not be confused with the ones observed in this work at the resolution of our experiment. Instead, there were lines that might be attributed to either Ag^0X, Cu^0X or Na^0X, these lines being so close in energy as to be indistinguishable from one another in our experiment.

Annealing of the wires, either at higher temperatures under inert gas (e.g. 500°C under nitrogen) or at lower temperatures under oxidizing or reducing environments caused the degradation of the luminescence by the quenching of the excitonic emission and the dominance of the DAP luminescence. This implies the creation of new populations of point defects that would be deleterious to minority carrier device operation. Such treatments are therefore unlikely to be of value in solar cell device processing.

By fitting the temperature dependence of the PL intensity of excitonic and DAP transitions to a model that accounts for the thermal quenching of PL, values for the binding energies of bound-excitons to their impurity, of the excitons themselves, and of donor and acceptor levels were estimated, these being comparable to those found in the literature. On the contrary, exciton lifetimes, determined from time-resolved PL measurements, are some of the longest ever seen in CdTe material that is not on the quantum-scale.

PL spectroscopy of CdS/CdTe core-shell NWs was also carried out, as presented in Section 6.4. Strong near-band edge CdS luminescence was observed, as is only seen for single-crystal material, along with CdTe luminescence and an intermediate band associated both with deep-levels in CdS and with S vacancies and Te doping of CdS. Upon annealing, the near-band edge CdS luminescence and the CdTe luminescence was quenched, whilst the

intermediate band was enhanced. These results imply there was an extent of S and Te inter-diffusion at the CdS/CdTe interface, which is promoted by annealing at 400°C.

UV-VIS spectrophotometry of NWs demonstrated their optical properties are favourable compared to thin films for PV applications. Both bare NWs and core-shell NWs demonstrated significant reflectance and transmittance reductions in comparison to their planar counterparts of equivalent volumetric material. Transmittance measurements failed to accurately determine the optical band-gap of the CdTe NWs.

Whilst resistivity measurements of individual CdTe NWs by the four-point probe method were unsuccessful, due to the inability to effectively make Ohmic contacts between the CdTe and the STM tips, the resistivity of the CdS shell was determined by this method to be $\rho = 0.7 \pm 0.4$ Ω.cm, this being comparable to literature values of sputtered CdS thin-films.

Overall, in this Chapter it has been demonstrated that the NWs grown here possess a number of properties that are desirable for PV applications, these being: a) an absence of high-energy electrically active grain boundaries; b) a reduced point defect density relative to thin films; c) exciton lifetimes comparable to high quality monocrystalline CdTe; and d) reduced transmittance and reflectance compared to thin films. Moreover, sputter-deposited CdS shells were observed to grow epitaxially on CdTe NWs, and there is evidence that upon thermal annealing, intermixing of S and Te was promoted, these features potentially being beneficial for PV devices as they may result in a lower density of interface states at CdS/CdTe junctions, although this is subject to further investigation.

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Chapter 7 : CdTe solar cells based on nanowire and planar absorber layers on Mo substrates

7.1 Introduction

In this Chapter the growth, characterisation and modelling of CdTe thin-film and nanowire solar cells on Mo substrates is reported.

Firstly, the procedures for fabricating thin-film CdTe devices in the 'substrate' configuration, i.e. ITO/ZnO/CdS/CdTe/Mo, are presented in Section 7.2. This was a necessary step in the development of CdTe NW devices, since the two device types are topographically equivalent and the performance of substrate devices achieved here acts as a suitable baseline to which NW devices are subsequently compared. Here both the optimisation of performance and in-depth characterisation are reported, with emphasis on the Cl-doping stage and characterisation by FIB-SEM, *EQE* and temperature-dependent *J-V* measurements. A peak efficiency of 8.01% for ITO/ZnO/CdS/CdTe/Mo substrate devices was obtained. Device modelling is presented in Section 7.3 with methods to improve efficiency beyond 8% being suggested.

Secondly, this Chapter centres on the investigation of NW devices. In Section 7.4, calculations of the performance enhancements achievable for CdTe solar cells with the use of radial rather than planar *p-n* junctions are presented. The results provide insights as to what the suitable NW dimensions may be for CdTe NW devices. The growth of ITO/CdS/CdTe NWs devices on CdTe/Mo and their photovoltaic (PV) performance is presented in Section 7.5. The effect of various post-growth treatment processes, and of NW dimensions and underlying film thickness, on the NW device efficiency is reported. A peak efficiency of 2.49% was obtained.

7.2 Growth and characterisation of CdTe planar solar cells on Mo

In this Section, the growth and characterisation of thin-film ITO/ZnO/CdS/CdTe/Mo solar cells is presented, with the effect of varying the post-growth treatment of these devices on their performance being of particular interest. CdTe planar cells in the superstrate configuration, having the layer sequence Au/CdTe/CdS/ZnO/ITO, were also grown for comparison.

7.2.1 Experimental

7.2.1.1 Deposition conditions for growing ITO/CdS/CdTe/Mo substrate devices. 50 mm x 50 mm Mo foil substrates (Advent, 3N pure) were cleaned ultrasonically in de-ionised water and dried with a N_2 air gun. CdTe films were CSS-deposited, with a powdered source (Alfa Aesar, 5N pure) heated to 605°C and the substrate held at 530°C, by a two stage process; firstly, under a static pressure of 25 Torr N_2 for 2 - 10 minutes, and then under medium vacuum (10^{-1} Torr) for 1 minute. This generated films of thickness 1.8 – 10 µm. The CdS window layers were RF sputtered under 5 mTorr Ar for 30 mins, using a target power of P = 60W, with the substrate held at 200°C. The ITO front contact layer was also deposited by sputtering, under 1 mTorr Ar for 120 min, using a target power of P = 70W and with the substrate at 350°C. Whilst this completed the basic layer structure, some samples included additional layers. For instance, in some samples CdS/CdS:O bilayers were used as an alternative to CdS for the window layer: In this case CdS was first sputtered for 5 mins in pure Ar and then for 1 hour in a partial pressure of 3% O_2. Moreover, for some samples, an intrinsic ZnO film was included between the CdS and ITO layers, this also grown by sputtering, at room temperature, under 1 mTorr Ar for 20 mins, using a target power of P = 100W. The 50 mm x 50 mm samples were then quartered into 25 mm x 25 mm pieces.

Preliminary studies indicated that the standard $CdCl_2$ annealing process used for superstrate devices (typically a 20 – 30 minute anneal of the CdS/CdTe stack at 420°C following $CdCl_2$ evaporation) was ineffective for substrate cell activation. Hence, in order to optimise the device processing, four different $CdCl_2$ post-growth treatments were attempted, these being summarised in Table 7.1 and now described:

Treatment A) After CdS deposition, 200 nm $CdCl_2$ was evaporated and the structures were annealed in air at 420°C for 30 mins, with ITO being subsequently deposited, and no further treatment being applied.

Treatment B) $CdCl_2$ deposition and annealing conditions were identical to treatment A but were applied *prior* to CdS and ITO deposition, i.e. only the CdTe layer was treated.

Treatment C) As treatment B (i.e. after CdTe deposition) but with the addition of a *second* annealing step after ITO deposition, in air at 480 - 580°C air for 30 mins, with no additional $CdCl_2$ deposition.

Treatment D) No $CdCl_2$ deposition and just a single annealing step, after ITO deposition, in air at 480 - 560°C for 30 mins.

For clarity, for the remainder of this Section, the temperature of the $CdCl_2$ annealing step after CdTe or CdS deposition is denoted T_{CdCl2}, and the temperature of the annealing step after

ITO deposition is denoted T_{anneal}. After layer growth and annealing, samples were mechanically scribed into 2.5 mm x 2.5 mm individual devices. Device performance parameters quoted in Table 7.3 are from individual devices, whereas those plotted in Fig 7.4 are averages taken from a sample (each with up to 16 individual devices).

Table 7.1: Annealing processes applied to substrate solar cells. Each annealing step was carried out in air for 30 mins, see text.

	After CdTe dep.	*After CdS dep.*	*After ITO dep.*
A	-	200 nm $CdCl_2$ T_{CdCl2} = 420°C	-
B	200 nm $CdCl_2$ T_{CdCl2} = 420°C	-	-
C	200 nm $CdCl_2$ T_{CdCl2} = 420°C	-	T_{anneal} = 480 - 580°C
D	-	-	T_{anneal} = 480 - 580°C

7.2.1.2 Deposition conditions for growing Au/CdTe/CdS/ZnO/ITO superstrate devices: Low iron soda-lime glass superstrates (Pilkington Opti-WhiteTM), 100 mm x 100 mm x 3 mm in size, were cleaned by DI water and dried with a N_2 air gun. ITO, ZnO and then CdS films were RF sputtered using the same conditions as for the substrate devices. The 100 mm x 100 mm plates were then quartered and CdTe was CSS-deposited, using the same growth conditions as for substrate devices. 200 nm $CdCl_2$ was evaporated onto the CdTe surface, and the samples were annealed at 400°C in air for 30 minutes. These were then subjected to a 10 sec nitric-phosphoric acid etch, before an array of 5 mm x 5 mm gold back contacts were deposited by thermal evaporation to complete the devices.

7.2.1.3 Characterisation. *J-V* measurements were carried out under AM1.5 illumination using an Oriel solar simulator and *J-V-T* measurements were conducted in the dark, in the temperature range 200 – 350K. *EQE* data was collected using a Bentham PVE 300 EQE system with white light bias. For SIMS analysis, a O^{2+} ion gun (Hiden Analytical) was used to sputter the sample (using a beam energy of 5 keV) and secondary ions were analysed by a quadrupole detector. Secondary electron SEM images of device cross sections were recorded, the cross sections having been prepared by the FIB-milling method (see Chapter 4).

7.2.2 The impact of the $CdCl_2$ activation step

Fig 7.1 shows the *J-V* curves of the best performing devices obtained from each of the post-growth treatments A – D, the shapes of the curves being representative of each respective

sample set. Table 7.2 shows the PV performance parameters of these 'best devices'. All devices described in this comparison had a CdTe thickness, $X = 4 \pm 0.5$ µm and did not include a ZnO layer. Those subject to treatments C and D used $T_{anneal} = 560$°C.

All devices subject to post-growth treatment A, i.e. annealing after CdS deposition and with no further annealing, performed very poorly, the majority of contacts were short-circuits and the remainder typically had $\eta < 0.5\%$ due to low FF (< 35%), J_{SC} (< 7.5 mA.cm^{-2}) and V_{OC} (< 300 mV). The best-device from this sample set had $\eta = 0.62\%$, limited by a series resistance ($R_S = 18.9$ Ω.cm^2) that is considerably greater than that of high efficiency CdTe/CdS devices, and an extraordinarily low R_{SH} (75 Ω.cm^2).

Likewise, devices subject to post-growth treatment B, i.e. annealing after CdTe deposition and with no further annealing, performed poorly, with the highest efficiency achieved being $\eta = 1.96\%$. Nevertheless, relative to treatment A, these devices had improved V_{OC} (in the range 200 – 400 mV), and J_{SC} (5 – 15 mA.cm^{-2}), but FF remained low (< 35%). Indeed, although treatment B yielded higher R_{SH} (434 Ω.cm^2 for the best device, ~ 400 Ω.cm^2 being typical for the sample set) it remains much lower than that of high efficiency devices, and R_S is too high (16.2 Ω cm^2 for the best device, ~ 20 Ω.cm^2 being typical for the sample set).

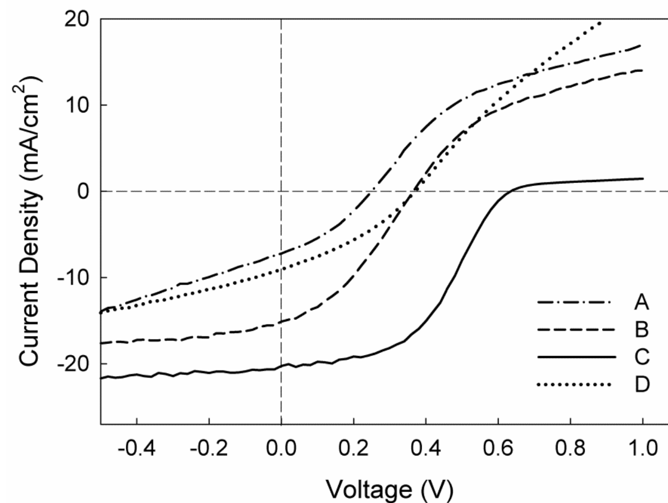

Fig 7.1: *J-V* curves of the best performing substrate devices obtained from each of the post-growth treatments A, B, C and D. See Table 7.1 and the text in Section 7.2.1 for a description of these treatments, and Table 7.2 for the associated solar cell performance parameters.

Post-growth treatment C yielded significant performance enhancements, with $\eta = 6.05\%$ being achieved for $T_{anneal} = 560$°C. This was principally a result of enhancements to V_{OC} (from 365 mV for treatment B to 635 mV for treatment C) and FF (from 35.5% to 47.1%). For

treatment C, R_S (12.3 Ω.cm^2) was lower than for either treatments A or B, and R_{SH} (563 Ω.cm^2) was higher.

Table 7.2: A comparison of the best performance parameters of substrate devices subjected to different post-growth annealing processes (see Table 1 and text).

Treatment	*η* (%)	J_{SC} (mA/cm^2)	V_{OC} (mV)	*FF* (%)	R_S (Ω.cm^2)	R_{SH} (Ω.cm^2)
A	0.62	7.22	251	34.1	18.9	75
B	1.96	15.1	365	35.5	16.2	434
C (T_{anneal} = 560°C)	6.05	20.2	635	47.1	12.3	563
D (T_{anneal} = 560°C)	1.14	9.06	367	34.2	20.4	111

All devices subjected to treatment D (with no prior Cl-doping) had efficiencies, $\eta < 1.2\%$, primarily due to low V_{OC} (< 370 mV) and J_{SC} (< 9 mA.cm^{-2}). Notably, the R_S of the best device (20.4 Ω.cm^2) from this sample set was higher than that of treatments A, B and C.

Regardless of the post-growth treatment, the *J*-*V* curves of all devices demonstrated significant roll-over in the first quadrant (Fig 7.1), this being indicative of a rectifying back contact[1] (see Sections 7.2.4 and 7.3).

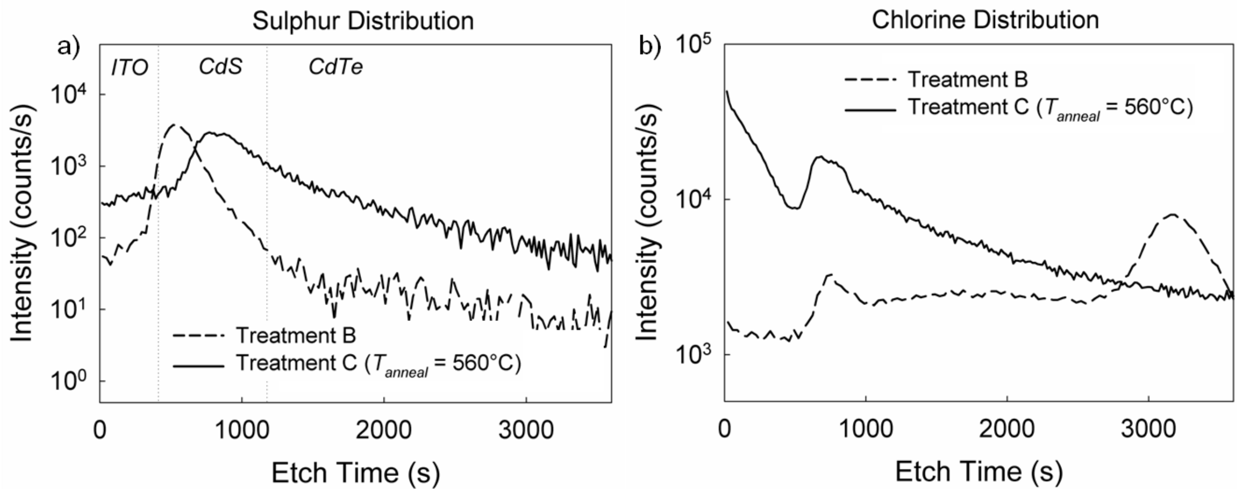

Fig 7.2: SIMS depth-profiles of a) S and b) Cl concentrations in a device subject to treatment B (once-annealed) and a device subject to treatment C (twice annealed, T_{anneal} = 560°C). The left edge of the plots represents the front surface of the cell, i.e. the ITO surface.

As the double-annealing process (treatment C) was the most effective treatment, the effect of the second annealing stage was investigated by SIMS profiling. Depth profiles of S and Cl concentrations are shown in Fig 7.2a and b respectively for the devices B and C from Table

7.2. The left edge of the plots represents the front surface of the devices, i.e. the ITO surface. The actual depth that correlates to the etch time during the SIMS measurement is not quoted, but the depth of the CdS layer is inferred from the S peak of the B-treated device. It is clear from Fig 7.2a that one of the effects of the second annealing stage is to increase S diffusion into the CdTe layer, giving a less abrupt CdTe/CdS interface. There is also a distinct difference in the Cl-profiles of the two devices. In the device subject to just one annealing stage (B), there is an excess of Cl deep in the CdTe layer, towards the CdTe/Mo interface. In the device subject to two annealing stages (C), the deep Cl peak is not seen but there is a higher Cl concentration in the CdS layer and throughout the remainder of the CdTe, presumably having diffused from deep in the CdTe following the second-annealing stage.

7.2.3 Inclusion of ZnO layer and EQE of best device

Fig 7.3a shows a comparison of the performance of cells with and without a ZnO layer, processed using treatment C (at T_{anneal} = 560°C) from Table 7.2.

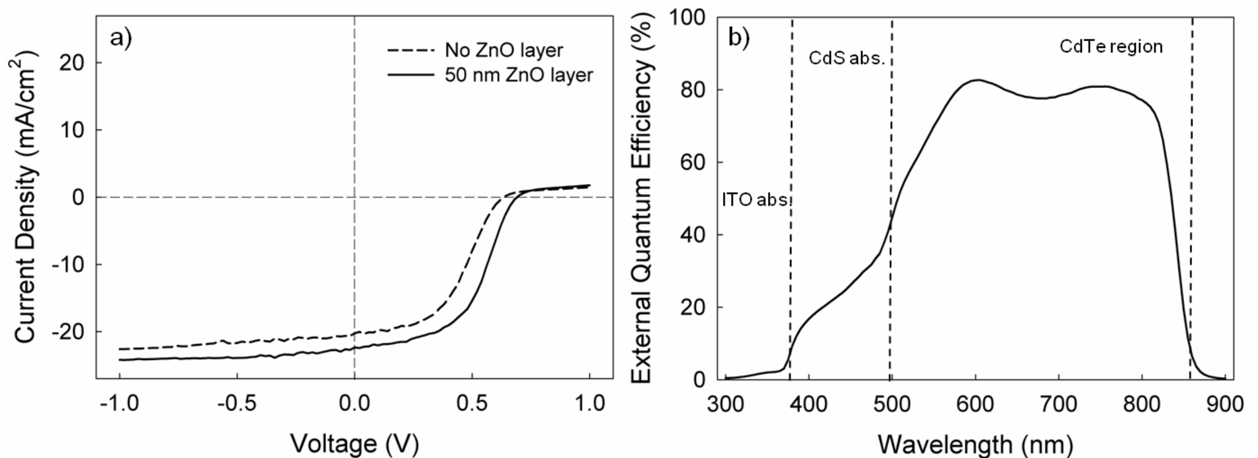

Fig 7.3: a) *J-V* curves of devices subject to treatment C at T_{anneal} = 560°C with and without the inclusion of a ZnO layer. b) *EQE* response of the device (η = 8.01%) for which the ZnO layer was included.

The ZnO layer increases the efficiency from 6.05 to 8.01% by increasing J_{SC} (from 20.2 mA.cm^{-2} to 22.4 mA.cm^{-2}), V_{OC} (from 635 mV to 690 mV) and *FF* (from 47.1% to 51.9%). Notably R_{SH} is significantly greater upon inclusion of the ZnO layer, from 563 Ω.cm^2 to 881 Ω.cm^2. This device had the best efficiency achieved in these experiments.

Fig 7.3b shows the *EQE* response measured from this device for which the main features are now described. A relatively flat response is observed in the spectral region 600 – 860 nm, peaking at ~ 80% - the drop at ~ 860 nm being at the CdTe band-edge. There are significant losses in the above-gap region of the CdS (i.e. ≤ 500 nm) and a further reduction in *EQE* for

λ < 400 nm associated with absorption by the ZnO. Note also the gradual decrease in *EQE* in the 500 – 550 nm wavelength region, presumably associated to absorption in alloyed $CdS_{1-y}Te_y$ for which the band-gap is lower than CdS.

7.2.4 Comparison with superstrate CdTe solar cell

Fig 7.4 shows the *J-V* curve of the best performing ITO/ZnO/CdS/CdTe/Mo substrate device (η = 8.01%) compared with that of an equivalent superstrate device (η = 11.9%), having the configuration Au/CdTe/CdS/ZnO/ITO/glass. The growth conditions and times of each of the layers were the same for both devices so their thicknesses are assumed to be similar. The post-growth treatments (see Section 7.2.2) used the same amount of $CdCl_2$ and differed by only 20°C. The performance parameters of each of these devices are shown in Table 7.3.

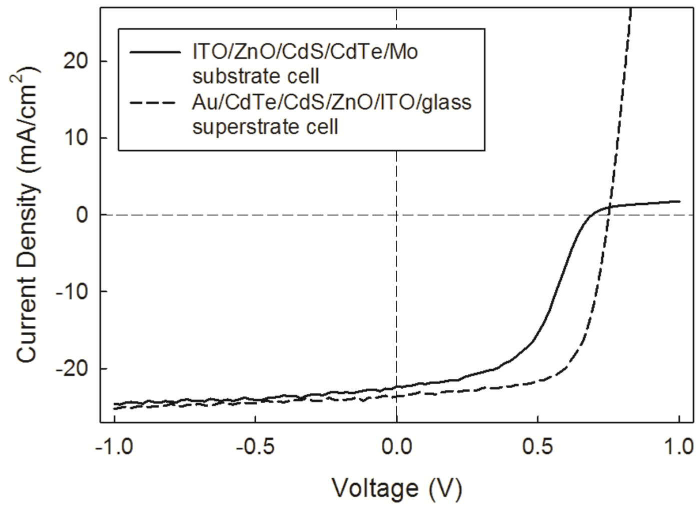

Fig 7.4: *J-V* curve of a 'superstrate' Au/CdTe/CdS/ZnO/ITO/glass device, compared with that of the best performing substrate device.

Table 7.3: PV performance parameters for the best performing substrate device and for a superstrate device.

Device	**η (%)**	**J_{SC} (mA/cm²)**	**V_{OC} (mV)**	***FF* (%)**	**R_S (Ω.cm²)**	**R_{SH} (Ω.cm²)**
Substrate cell	8.01	22.4	690	51.9	9.89	881
Superstrate cell	11.9	23.6	740	68.2	2.88	665

Whilst the J_{SC} values are relatively comparable, the superstrate device has a much higher V_{OC} and *FF* than the substrate device, these being 740 mV compared to 690 mV and 68.2% compared to 51.9% respectively. As a result, the superstrate device has an efficiency more

than 3% higher than the substrate device. It is immediately evident from the *J-V* curves that the quality of the back contact is the main difference between these two devices, the superstrate device not exhibiting any of the rollover which limits the substrate device. Indeed, the superstrate device has a much lower R_S (2.88 Ω.cm^2) than the substrate device (9.89 Ω.cm^2).

7.2.5 Use of CdS/CdS:O bi-layer in substrate geometry devices

In this Section, the effect of replacing the CdS window layer of a substrate device with a CdS:O/CdS bilayer is presented. This step was attempted with the aim of reducing absorption in the window layer, preliminary results having demonstrated that CdS:O has a wider optical band-gap than CdS (see Section 7.2.8). The thicknesses of the CdS:O and CdS films within the bilayer were estimated to be 200 nm and 40 nm respectively from known growth rates. The device also included a ZnO layer between CdS and ITO and was subject to treatment C at T_{anneal} = 560°C. Fig 7.5 shows its *EQE* response, compared with that of the best performing device from Section 7.2.3, which had the normal CdS window layer, but was otherwise identical.

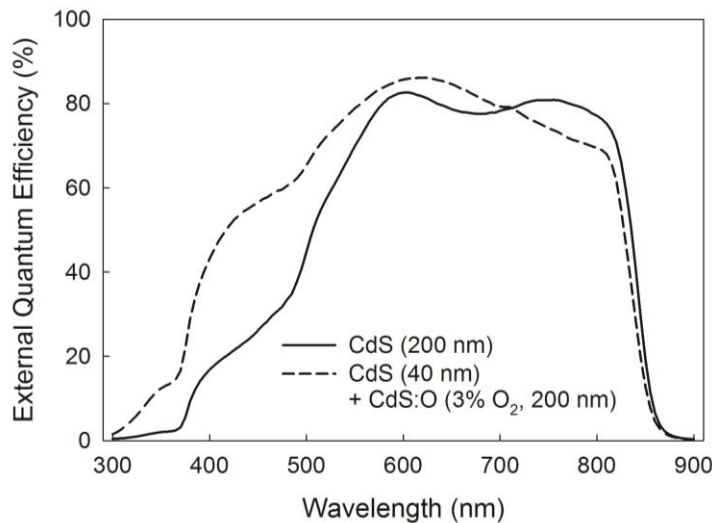

Fig 7.5: *EQE* response of an ITO/ZnO/CdS:O/CdS/CdTe/Mo device and an ITO/ZnO/CdS/CdTe/Mo device, each having been subject to treatment C at T_{anneal} = 560°C. The performance parameters are shown in Table 7.4.

It is clear from Fig 7.5 that the effect of replacing the single CdS layer with the bilayer is to significantly enhance the blue-response of the device, the *EQE* increasing from 20 – 30% in the 400 – 500 nm region to almost 60%. There are some losses in the bilayer device at long wavelengths however, particularly in the 720 – 820 nm range. Nevertheless, a higher J_{SC} was achieved in the bilayer device than in the single window layer device, 24.6 mA.cm^{-2} compared

to 22.4 mA.cm^{-2}. Overall however the efficiency of the bilayer device (η = 7.05%), remains lower than the original device due to it having poorer V_{OC} and FF. Preliminary results of devices for which only a single CdS:O layer was used (with no CdS) had even lower V_{OC} (< 400 mV).

Table 7.4: PV performance parameters for two substrate devices with different window layers, these being; a) a single CdS layer, and b) a CdS:O/CdS bilayer.

Window Layer	η (%)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	R_S (Ω.cm^2)	R_{SH} (Ω.cm^2)
CdS (200 nm)	8.01	22.4	690	51.9	9.89	881
CdS (40 nm) + CdS:O (200 nm)	7.05	24.6	605	47.4	10.3	741

7.2.6 Effect of CdTe thickness and second annealing temperature on substrate devices

The effect of varying both the annealing temperature, T_{anneal}, in the range 540 - 580°C and the CdTe thickness, X, in the range 1.8 – 10 µm was evaluated for a series of devices having 50 nm of ZnO and being processed using treatment C. The average performance parameters as a function of X and T_{anneal}, are plotted in Fig 7.6 and typical J-V curves for devices having different X, each annealed at T_{anneal} = 580°C, are shown in Fig 7.7.

Regardless of annealing temperature the optimum CdTe thickness was X = 3 – 6 µm, the average efficiency being ~ 4% in this range for T_{anneal} = 580°C. The thickness-dependency of efficiency closely follows that of J_{SC}, which peaks at 18.9 ± 2.1 mA.cm^{-2} with an absorber thickness of 3.4 µm, also for T_{anneal} = 580°C.

The graphs in Fig 7.6 show considerable spread with for example the 1.8 µm thick sample annealed at T_{anneal} = 580°C having $\eta_{avg.}$ = 1.7 ± 1.6%. Nevertheless there are some overall trends: a) The thinnest devices had low efficiency due to low V_{OC} (< 300 mV) despite having some of the highest FF; and b) the thickest devices maintained high V_{OC} (> 500 mV) but lost efficiency due to reduced FF and J_{SC} values. The low FF of the thicker devices may be attributed to higher R_S given that for devices annealed at T_{anneal} = 580°C, R_S increased with X, the values calculated from the J-V curves being 8.1 Ω.cm^2 (X = 1.8 µm), 14.1 Ω.cm^2 (X = 3.4 µm), 14.8 Ω.cm^2 (X = 6.1 µm) and 22.3 Ω.cm^2 (X = 10.0 µm). Notably, the R_S for the devices with X = 10 µm annealed at 580°C was comparable to that of the thinner devices (X = 3 – 6 µm) that were annealed at 540°C. Another observation of note was that the J-V curves of the thinnest devices (X = 1.8 µm) did not exhibit the strong rollover that was typical for the thicker devices (X = 3.4 – 10 µm).

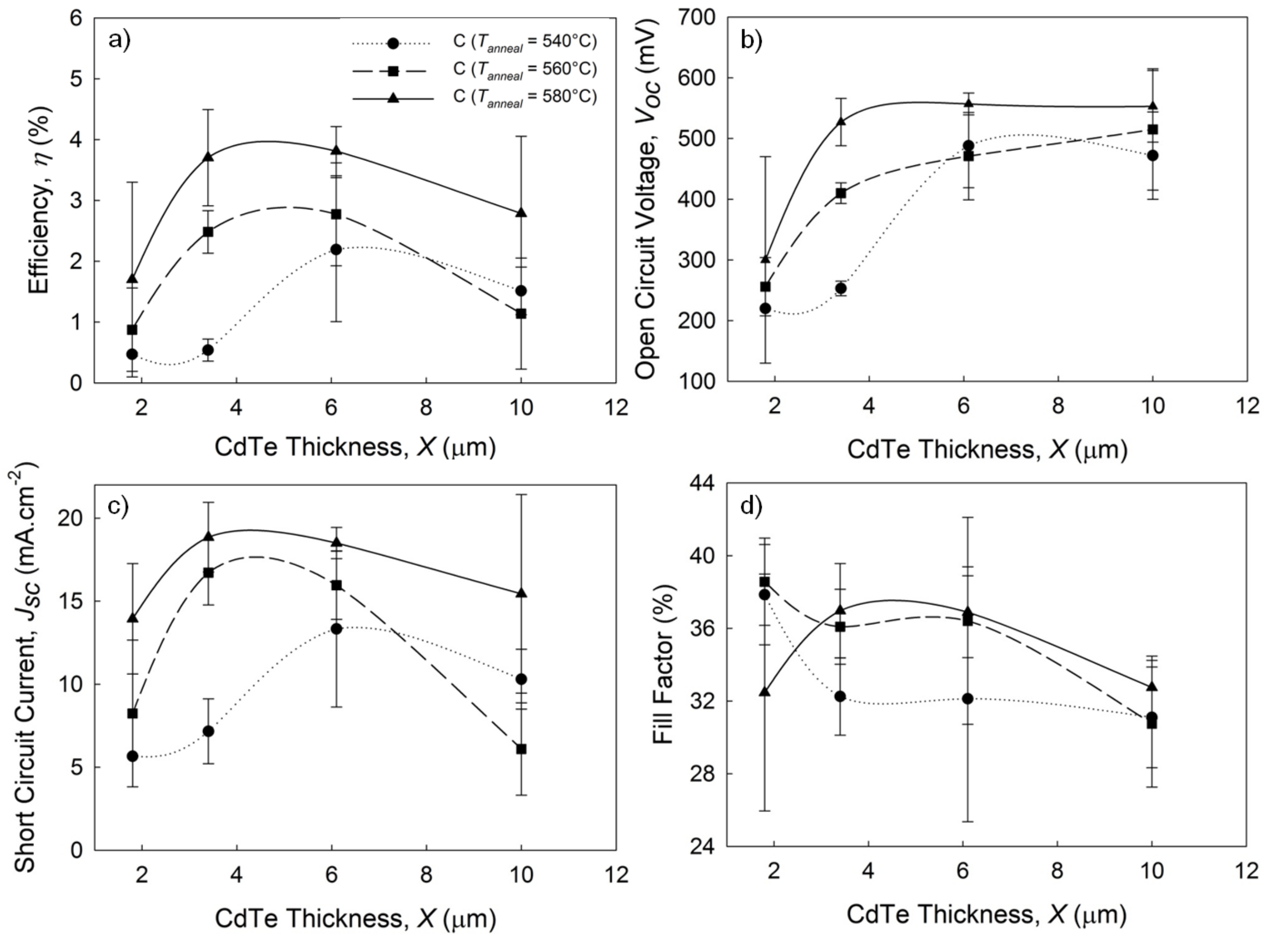

Fig 7.6: a) Dependence of a) η, b) V_{OC}, c) J_{SC} and d) FF as a function of CdTe thickness for a range of annealing temperatures (T_{anneal} = 540 – 580°C). Lines added as a guide to the eye.

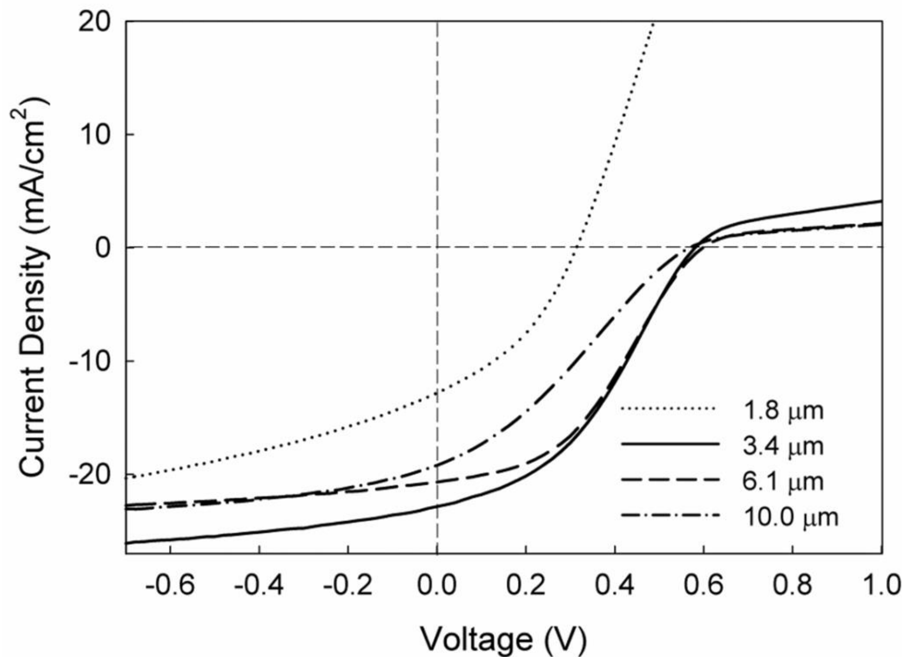

Fig 7.7: Typical J-V curves for devices subject to treatment C (T_{anneal} = 580°C), with different CdTe thickness (X = 1.8 – 10 μm).

Overall though the most significant finding was that annealing in the range 540 - 580°C gave increased device performance with higher temperature. However trials at 600°C and above caused very significant device degradation.

7.2.7 Further characterisation of substrate devices

7.2.7.1 FIB-SEM. A secondary electron image of a FIB-milled ITO/ZnO/CdS/CdTe/Mo device cross section is shown in Fig 7.8a, and a higher magnification image of the layers at the device front surface is shown in Fig 7.8b. This device had been subject to treatment C, and had η = 5.3%. The grains in the CdTe layer extend the entire thickness of the film (X ~ 1.6 - 1.9 μm), are up to ~ 4 μm wide and are twinned. Twin density is remarkably lower than has been reported elsewhere however[2].

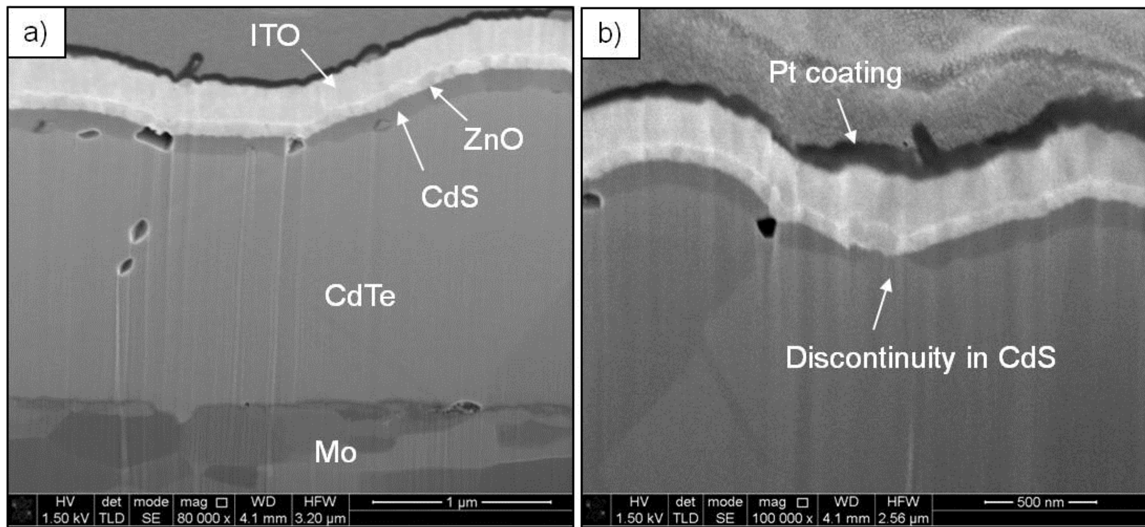

Fig 7.8: Secondary electron images of a FIB-milled ITO/ZnO/CdS/CdTe/Mo device cross-section. The device was subject to treatment C with T_{anneal} = 580°C, and had efficiency of 5.3%.

Estimates for the thickness of the CdS, ZnO and ITO layers from these images are 120 ± 10 nm, 90 ± 10 nm and 200 ± 10 nm respectively. The estimate of 120 nm for the CdS is much less than the 200 nm predicted from growth rates, and it is likely that inter-diffusion has taken place. Numerous voids exist within the device; in the bulk of the CdTe, at the CdTe/CdS interface, and some extending the entire thickness of the CdS film. Discontinuities in the CdS layer occasionally result in the ZnO coming into contact with the CdTe (Fig 7.8b), although for the most part this was not the case. The CdTe/CdS interface is much rougher in the case of these substrate cells than would typically be observed in superstrate cells.[3]

7.2.7.2 J-V-T. Temperature dependent *J-V* measurements were used to determine the back contact barrier height, ϕ_B, of a ITO/ZnO/CdS/CdTe/Mo device (X ~ 6 μm, subject to

treatment C and having $\eta = 5.5\%$), and to investigate the electrical current transport mechanisms that operate at its main junction. To determine ϕ_B, the method of Bätzner[4] was used (see Section 4.4). Fig 7.9 shows R_S as a function of temperature, R_S having been calculated from the slopes of dark *J-V* curves in forward bias. By fitting Equation 4.10 to this data, a barrier height of $\phi_B = 0.51$ eV was extracted.

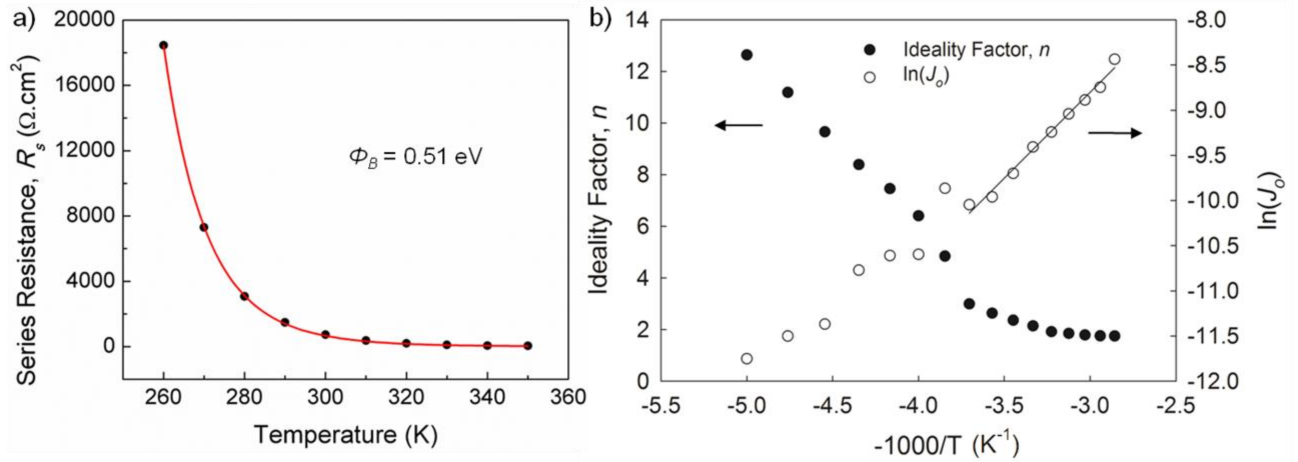

Fig 7.9: The temperature dependence of R_S, used to determine the back contact barrier height, Φ_B. b) Temperature dependence of the ideality factor, *n*, and the saturation current, J_0. This data was taken from a device subject to treatment C ($T_{anneal} = 580°C$), having a CdTe thickness of $X \sim 6$ µm and for which $\eta = 5.5\%$. A good fit to the relationship $\ln(J_0) \propto -1/T$ was obtained in the range $T = 270 – 350$ K.

Identification of which transport mechanisms operate within a device can be inferred from the temperature dependence of *n* and J_0 (see Section 2.3), this being shown for the substrate device in Fig 7.9b. Here, *n* and J_0 were determined from the slope and intercept respectively of dark $\ln(J) – V$ plots at each temperature, from sections of the curves for which rollover had not yet begun. Both *n-T* and J_0-*T* plots indicate that there are two distinct temperature regions in which the transport behaviour is different. In the range 270 - 350K, $n \sim 2$ and J_0 follows the dependence $\ln(J_0) \propto -1/T$, both of these characteristics being indicative of recombination in the depletion region of the device, at traps located near the middle of the band-gap. At temperatures below 270K, *n* increases as *T* decreases, this being indicative of a regime dominated by multi-step tunnelling of electrons through the depletion region via a distribution of localised states.

For temperatures at which the tunnelling mechanism dominates, the number of tunnelling steps, *R*, involved in the process may be calculated from the value of *A* ($= q/nkT$), as described in Section 2.3, using Equation 2.16. For this calculation, values for the permittivity, ε, and the effective electron mass, m_n, of CdTe were taken as 10.5 ε_0 and 0.1 m_e respectively (estimated

for this temperature range from data in Ref. 5). A value for the *p*-type doping density, N_A, of CdTe was estimated to be ~ 2×10^{15} cm^{-3} for this device using preliminary capacitance-voltage measurements (see Section 2.2.3 for an explanation of how N_A may be determined). From the data, a value of $R = 5720 \pm 1310$ steps was determined, the average having been calculated from measurements at a number of temperatures in the range 210 – 260 K. This value is an order of magnitude greater than that found for superstrate CdS/CdTe solar cells[6, 7].

7.2.8 Discussion of substrate device experimental results

7.2.8.1 Impact of post-growth treatments and the inclusion of a ZnO layer on device performance. The relative success of the various post-growth treatment procedures, in terms of yielding the highest PV performance, may be discussed in terms of the known effects of both Cl-containing and Cl-free treatments. The effects of $CdCl_2$ treatment are: a) *p*-doping of the CdTe; b) recrystallization of both CdS and CdTe; and c) the promotion of inter-diffusion[8] of CdTe and CdS, which may (beneficially) reduce the density of interface states. Recrystallisation and inter-diffusion may also be realised using Cl-free treatments provided that higher annealing temperatures are used (> 450°C)[9].

In terms of increasing PV performance, these effects are usually beneficial if controlled to an appropriate level. However, *over*treatment with $CdCl_2$ is considered to be detrimental to the CdS by either: a) opening intergranular short circuit paths during the densification that may accompany recrystallization; or b) local pinholing in the CdS caused by complete consumption of the CdS by the inter-diffusion process[10].

Post-growth treatment A yielded low-efficiency devices with low R_{SH} and V_{OC} and frequent shunting. Since this was the only process in which the CdS was directly $CdCl_2$ treated, it is presumed that the detrimental effects of overtreatment are responsible. Indeed, Singh *et al.*[10] report that excessive inter-diffusion occurs for similarly treated substrate devices. It may also indicate that the process fails to sufficiently *p*-dope the CdTe.

Treatment B, in which only the CdTe is $CdCl_2$ treated, does not suffer from such serious shunts and its higher V_{OC} indicates that CdS pinhole density is reduced and/or that the process is more effective in *p*-type doping the CdTe.

Treatment C gave the highest device performance and this may be assumed to be due to introducing both the required *p*-doping (during the first $CdCl_2$ treatment) and inter-diffusion (during the Cl-free second treatment) but without direct $CdCl_2$ treatment of the bare CdS that could lead to deleterious effects. SIMS analysis supports the attribution of performance increase (notably V_{OC}) to inter-diffusion, since the second annealing stage correlated with an

increase in S concentration in the CdTe. It also correlated with an increase in Cl concentration in the CdS and CdTe bulk, which may be responsible for an enhancement of the junction.

Treatment D on the other hand yielded low efficiency devices despite its final Cl-free annealing stage possibly enhancing inter-diffusion, presumably since the absence of the initial $CdCl_2$ treatment resulted in the CdTe being insufficiently doped. These results imply that both annealing stages are necessary for substrate devices. Kranz *et al.*[11] achieved the best reported CdTe substrate device on Mo foil (11.5 %) by using a similar double-annealing process, but having used Cl-doping during *both* stages.

The inclusion of a ZnO layer in devices subject to treatment C yielded the best efficiency of the entire sample set (η = 8.01%), also having the highest V_{OC} (690 mV) and R_{SH} (881 $\Omega.cm^2$) reported here. It is thought that the detrimental impact of shunting pathways and weak CdTe/ITO diodes, caused by overtreatment of the CdS (or merely CdS deposition non-uniformities), is lessened by the inclusion of the ZnO. Non-uniformities of CdS thickness may always be more of a concern for substrate cells than for superstrate cells because CdS is deposited onto a rough CdTe film rather than a relatively smooth ITO film.

7.2.8.2 Back contact. The *J-V* curves of almost all substrate devices reported here demonstrated significant rollover, this characteristic implying that the back contact is severely rectifying[1] (see Section 2.5). This is to be expected since the work function of Mo (~ 4.36 – 4.95 eV)[12] is much lower than that of CdTe (~ 5.7 eV, dependent on N_A). However, it must be noted the barrier height is not only dependent on the difference in work functions, but also on interface states[13]. The back contact barrier height was determined here to be 0.51 eV by *J-V-T* measurements which may be considered high given that any barrier height exceeding 0.3 eV is thought to be detrimental to PV performance[14]. (The device used for this measurement was deemed to be sufficiently electronically thick - X = 6.1 μm - for Bätzner's method to be valid). Niemegeers[1] reports that the presence of the barrier reduces the *FF* as it plays the role of a series resistance, but disregards its effect on V_{OC} or J_{SC} except for extremely high barrier heights. This is consistent with the findings of Demtsu[15] who used a two-diode model (consisting of the main junction diode and the back contact diode in opposite directions) to simulate the effect of barrier heights in the range 0.5 – 0.6 eV. The effect of the back-contact on device performance parameters for these devices is explored in more detail in Section 7.3.

7.2.8.3 Comparison with superstrate devices. The *J-V* curve of a superstrate device demonstrated no rollover, achieving a higher efficiency (η = 11.9%) than the substrate devices through enhanced *FF* (68.2%) and V_{OC} (740 mV). For the superstrate device, a nitric-

phosphoric acid etch was applied in order to generate a Te-rich back surface[16] to help improve the contact, and its Au back contact has a higher work function (~ 5.1 – 5.47 eV)[12] than Mo.

Furthermore, only one annealing stage was required to achieve a high-efficiency superstrate device. It is generally understood that CdTe doping, recrystallisation and inter-diffusion are *all* achieved during this single annealing stage for superstrate devices. In this case Cl-doping was applied from the back surface of the CdTe layer therefore its effects on the main junction and the CdS layer were more gradual than in the case of direct treatment of the CdS layer in substrate devices (treatment A). Consequently, the detrimental effects of overtreatment were not observed. Whilst in this context, it may be perceived that superstrate cells have an advantage (in terms of simplifying the treatment process), it must be noted that optimisation of the Cl-activation of superstrate cells has developed over a number of decades of research. Indeed, the two-stage annealing process of the substrate devices may be more desirable since it allows the doping and junction formation stages to be optimised separately.

7.2.8.4 EQE of substrate device and use of CdS:O/CdS bilayer. The measurement highlighted significant collection losses in the blue region of the incident spectrum ($EQE <$ 30% at wavelengths < 500 nm) indicating absorption in the CdS layer (optical band-gap ~ 500 nm): Carriers generated in the CdS window layer typically do not contribute to the photocurrent because the depletion region in CdS/CdTe solar cells is heavily one-sided and almost entirely exists in the CdTe layer. Blue-losses are a shortcoming relative to the best performing devices in the industry, a high-efficiency superstrate CdTe device recently developed by General Electric[17] having EQE ~ 95% at 400 nm and ~ 50% at 350 nm. However, the use of a CdS:O/CdS bilayer improved the blue-response here, resulting in an increase of J_{SC} by ~ 2 mA/cm^2. The enhancement can be attributed to the thinner CdS layer (~ 40 nm) and to the CdS:O having a wider optical band-gap. The use of an oxygenated CdS window layer to reduce window layer absorption in CdTe solar cells was first reported by Wu[18], who later demonstrated that CdS:O has a nanocrystalline structure and that its grain size decreases with increasing O content, which results in the higher optical band-gap by quantum confinement[19]. Despite the increase in J_{SC} observed here, V_{OC} and FF was lower for the bilayer devices than for the single CdS layer devices. Indeed, the drop in V_{OC} and FF was even more significant for preliminary devices that included just a single CdS:O layer. Wu, who used just a single CdS:O layer as opposed to a bilayer, reports that another effect of using CdS:O is to suppress Te diffusion and the formation of a $CdTe_xS_{1-x}$ alloy. In that case, the effect was said to be beneficial as the alloy has a low optical band gap and can (detrimentally) increase window layer absorption, but as suppression of inter-diffusion can also be detrimental

to junction formation, this may explain the V_{OC} losses observed here for devices that included CdS:O. Further investigations, such as chemical profiling and XRD measurements, are necessary to confirm this postulation however.

7.2.8.5 Effect of CdTe thickness on device performance. The main findings from the investigations presented in Section 7.2.6 were: a) the optimum thickness for the absorber layer of substrate devices was $X = 3 – 6$ µm; b) devices with thinner absorber layers suffered from low V_{OC} (< 300 mV); c) devices with thicker absorber layers suffered from low *FF*; and d) there was a wide distribution of performances for each thickness. Deterioration of V_{OC} as CdTe thickness is reduced has similarly been reported by Clayton[20] *et al.*, who attributed it to the presence of micro-shorts due to incomplete coverage of the CdTe layer. However, in that case, these effects were only observed for CdTe thicknesses of 1 µm or less. Moreover, Clayton observed a corresponding drop in *FF* with CdTe thickness due to reduced R_{SH}, which was not consistently observed here. The low V_{OC} observed for the thinnest devices ($X = 1.8$ µm) here may instead be caused by the rectifying back contact: Whilst Demtsu states that back contact barrier heights of $\phi_B = 0.5 – 0.6$ eV are not detrimental to V_{OC}, the two-diode model is only valid provided the depletion regions of the main junction and of the back contact are independent and do not interact[15]. For thin devices, this will not be the case, with the effect of V_{OC} being lowered and the device being a *p/i/n* structure[13]. The observation that the *J-V* curves of these thinnest devices do not show any rollover is consistent with Demtsu's simplified two-diode model no longer being valid.

The reduction in *FF* with increased *X* was caused by an increase in R_S as a function of *X*, this being most likely due to either: a) the intrinsic resistance of the CdTe itself; or b) the existence of grain boundaries perpendicular to current flow in thicker CdTe films. Indeed, FIB-SEM imaging showed that CdTe grains extend the entire thickness of the film when $X = 1.8$ um, but the thicker films were not characterised. Nevertheless, the observation that R_S of devices with $X = 10$ µm annealed at $T_{anneal} = 580$°C was comparable to those with X = 3 – 6 µm annealed at $T_{anneal} = 540$°C does imply that for optimal treatment of thicker films, a higher annealing temperature is required. Devices with thicker CdTe layers also had lower J_{SC}, this presumably being a consequence of their higher R_S.

The wide distribution of performances measured here, observed for each thickness, is not uncommon for CdTe solar cells, and may be attributable to thickness non-uniformities – typically more of a problem for CSS-deposited CdTe films than sputtered films – non-uniformities in grain size, doping and shunting behaviour associated with the films' polycrystallinity[21], and/or variations in $CdCl_2$ treatment[22].

7.2.8.6 Transport mechanism in substrate devices. The identification of two distinct temperature regions in which charge transport is governed by different mechanisms (recombination in the depletion region at high T and tunnelling at lower T) has similarly been reported for fully sputtered CdTe/CdS devices, Treharne[22] observing the change between the two regimes at ~ 250 K. Here, this 'turning point' was identified at ~ 270 K. In contrast, Alturkestani[6], Al-Allak[7] and Gaewdang[23] each report a multi-step tunnelling mechanism at *all* temperatures (typically ~ 200 – 300 K). Significantly, the number of tunnelling steps, R, calculated here for the multi-step tunnelling process was an order of magnitude greater than that calculated by Alturkestani[6] and Al-Allak[7], which may imply a higher interfacial defect density is present in the devices reported here. Although, the value given here was an average taken in the range $T = 210 – 260$ K, whereas in the case of Alturkestani, the value given was taken at room temperature, at which thermally activated de-trapping may be more prominent.

7.3 Modelling of CdTe planar solar cells

The results in the previous Section indicate that the principal limitation to efficiencies of substrates devices was that of a non-Ohmic back contact. Indeed, the highest efficiencies reported for substrate devices have all been achieved by inclusion of a buffer layer between CdTe and metal substrate in order to generate a quasi-Ohmic contact (see Section 2.6). In this Section, modelling of CdTe substrate cells is reported, this being used to: a) investigate the attainable efficiencies upon acquisition of an Ohmic contact for devices reported here; and b) evaluate the impact of a variety of buffer layers, having different electrical properties, on the back contact barrier height and on device performance.

7.3.1 Methodology

Device modelling was carried out using the SCAPS simulation tool.[24]

7.3.1.1 Replication of J-V data. Firstly, the experimental *J-V* curve of the best performing substrate device ($\eta = 8.01\%$) was replicated by SCAPS. This was achieved by uploading an 'ideal baseline' CdTe device model ($\eta = 16.4\%$) developed by Gloeckler[25] *et al.*, with the configuration metal/CdTe/CdS/ITO, and then modifying it to represent devices reported here by including: a) A back contact with a work function to represent Mo (5.25 eV), generating a large Schottky barrier; b) a maximum CdTe doping density of $N_A = 2 \times 10^{15}/\text{cm}^3$; c) reduced N_A in the CdTe layer towards the back contact due to the depletion of holes affected by the Schottky barrier; and d) increased R_S, comparable to devices reported here (10 $\Omega.\text{cm}^2$). Moreover, a more accurate value for the CdTe electron affinity (4.5 eV) was used[26].

All other physical properties were kept the same as that reported by Gloeckler, e.g. for CdTe; optical band-gap, $E_G = 1.5$ eV, effective densities of states, $N_C = 2.2 \times 10^{18}$/cm^3 and $N_V = 1.8 \times 10^{19}$/cm^3, and electron and hole mobilities, $\mu_e = 320$ cm^2/Vs and $\mu_h = 40$ cm^2/Vs. The thicknesses of the layers were CdTe(4 μm)/CdS(200 nm)/ITO(200 nm). *J-V* curves were simulated under AM1.5 illumination in the bias range – 1 to +1 V for the device, and this was repeated once the option for 'Ohmic contact' was selected, which generates an Ohmic contact regardless of the properties of metal and CdTe.

7.3.1.2 Inclusion of buffer layers between metal contact and CdTe. A 500 nm thick layer was inserted between the CdTe and the back contact. All of its properties were kept the same as that of CdTe, other than E_{ea} and N_A. By varying E_{ea}, but keeping E_G constant, the effect of introducing a buffer layer with a different work function, ψ, to CdTe could be investigated. *J-V* curves under illumination and electronic band diagrams (at zero bias in the dark) of the back contact/buffer layer/CdTe interfaces were simulated upon inclusion of buffer layers with varying combinations of E_{ea} and N_A.

7.3.2 Effect of generating an Ohmic back contact on device performance

Fig 7.10 shows the experimental *J-V* curve for the best performing device, taken from Fig 7.3, the simulated *J-V* curve that represents this device, and a simulated curve of the device with an Ohmic contact.

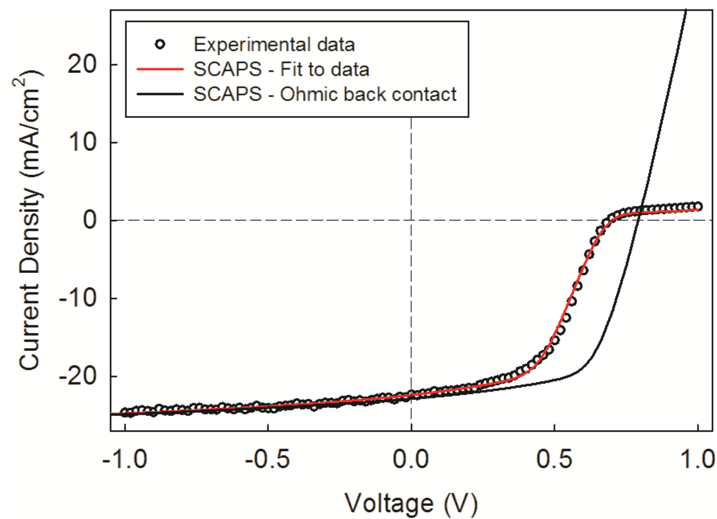

Fig 7.10: *J-V* data for highest efficiency (η = 8.01 %) substrate cell overlapped with modelled *J-V* data from SCAPS software ($\eta = 8.02$ %). By inclusion of an Ohmic back contact in the model, the predicted performance was improved to 11.3%.

A good agreement between the experimentally determined performance parameters ($\eta = 8.01$%, $J_{SC} = 22.4$ mA/cm^2, $V_{OC} = 690$ mV, $FF = 51.9$%) and the simulated parameters

(η = 8.02%, J_{SC} = 22.4 mA/cm^2, V_{OC} = 694 mV, FF = 51.6%) was achieved. Upon acquisition of an Ohmic contact, the simulation suggests these may be increased to η = 11.3%, J_{SC} = 22.9 mA/cm^2, V_{OC} = 792 mV and FF = 62.3%, with the curve showing no rollover.

7.3.3 Formation of quasi-Ohmic back contact using buffer layer

Fig 7.11a shows the simulated electronic band-diagram at the back contact of the substrate device and Fig 7.11b – c show the band diagrams upon inclusion of various buffer layers between the CdTe and Mo. The PV performance parameters simulated for each of these cases are listed in Table 7.5.

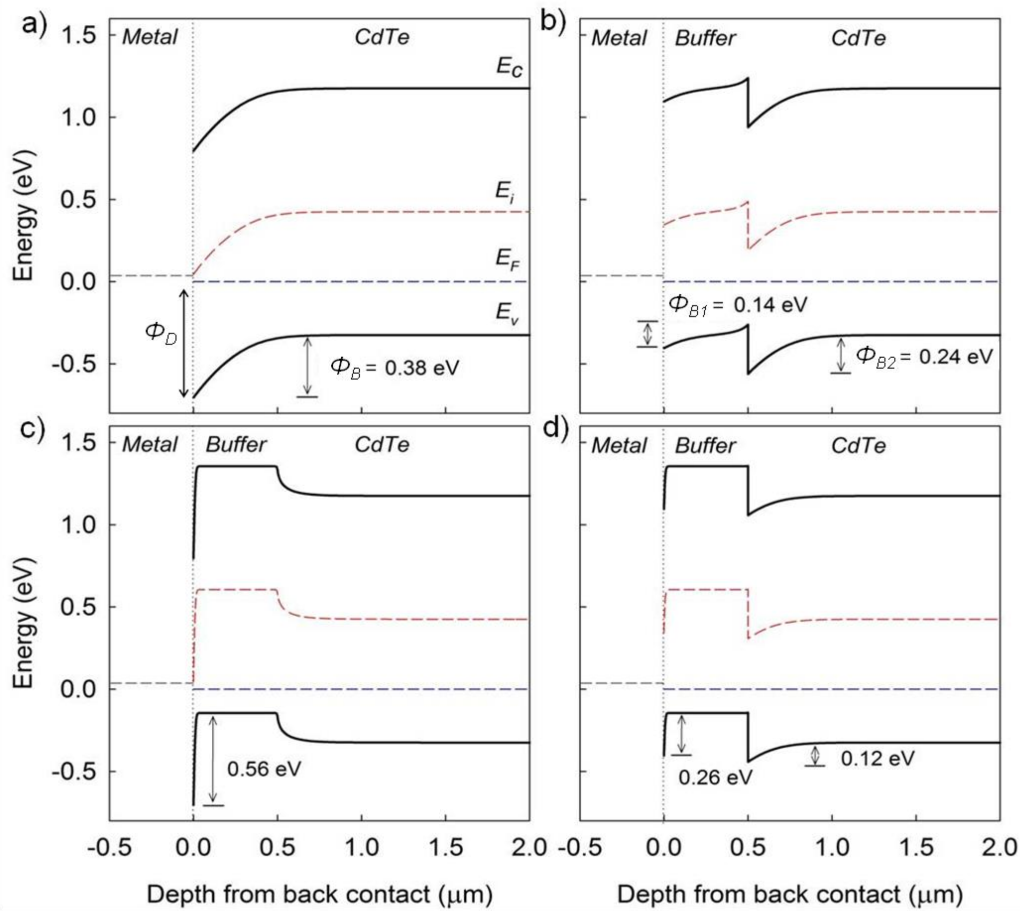

Fig 7.11: Electronic band diagrams (at zero bias in the dark) generated using SCAPS focussing on the back contact region showing the effect of the inclusion of various buffer layers placed between CdTe and Mo: a) No buffer layer, b) buffer layer with lower E_{ea} (4.2 eV) than CdTe, c) highly doped layer (N_A = 10^{18} cm^{-3}) and d) highly doped layer that also has E_{ea} = 4.2 eV.

It can be observed that a significant hole barrier, of height 0.38 eV, exists for the device with no buffer layer. It should be noted that this value represents the difference between metal and semiconductor work functions, and can be expressed as $\phi_B = \phi_D - (E_F - E_V)$ whereas ϕ_D

is the difference between the metal work function and CdTe valence band edge. Whilst the barrier height determined experimentally (ϕ_B= 0.51 eV) exceeds this value, the experimental value was calculated using R_S values taken from the forward bias sections of *J*-*V* curves, whereas these band-diagrams were simulated at zero bias. The use of a buffer layer that has a lower E_{ea} (4.2 eV) than CdTe but has otherwise the same physical properties has an immediate effect on the barrier, ϕ_B: It is divided into two smaller barriers (Fig 7.11b), one at the metal/buffer layer interface, ϕ_{B1} = 0.14 eV, and one at the buffer layer/CdTe interface, ϕ_{B2} = 0.24 eV. This has the effect of increasing the efficiency to η = 10.61% via enhancements to V_{OC} (791 mV) and *FF* (59.9%).

By using a buffer layer that is highly *p*-doped (N_A = 10^{18} cm^{-3}) but otherwise has the same properties of CdTe, the metal/buffer layer barrier height is increased to ϕ_{B1} = 0.56 eV but the band bending extends < 20 nm into the CdTe, and there is no barrier at the buffer layer/CdTe interface (Fig 7.11c). This results in the efficiency increasing to η = 9.65%. By including a buffer layer that has E_{ea} = 4.2 eV *and* is highly doped (N_A = 10^{18} cm^{-3}) an efficiency matching that obtainable upon acquisition of an Ohmic contact (η = 11.3%) is achieved. In this case, there exist two barriers (Fig 7.11d), one small barrier at the buffer layer/CdTe interface (ϕ_{B2} = 0.12 eV) and one thin barrier at the metal/buffer layer interface (ϕ_{B1} = 0.26 eV).

Table 7.5: Performance parameters of substrate configuration devices simulated by SCAPS upon inclusion of various buffer layers between CdTe and Mo.

Buffer layer properties	*W* (μm)	η (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	*FF* (%)
No buffer	-	8.02	694	22.4	51.6
Electron Affinity = 4.2 eV	500 nm	10.61	791	22.4	59.9
Highly *p*-doped (10^{18} m^{-3})	500 nm	9.65	772	22.3	56.1
Electron Affinity = 4.2 eV & highly *p*-doped	500 nm	11.32	794	22.5	63.4

7.3.4 Discussion of substrate device modelling

Results presented in Section 7.3.2 demonstrate that significant performance enhancements (from η = 8.02% to 11.3%) maybe achievable by use of an Ohmic contact to the substrate devices that were reported in Section 7.2. Evidently, the efficiency shortcoming of these

devices relative to the best reported on Mo foil by Kranz (η = 11.5%) may be largely attributed to the poor back contact.

7.3.4.1 Back contact's effect on V_{OC}. As a poor back contact is generally considered only to be detrimental to *FF* and not to V_{OC}[1, 15], it is unexpected that these results imply V_{OC} can be increased by 100 mV upon elimination of the rectifying contact. Whereas for the case of thin absorber layers (*X* = 1.8 µm) the Schottky barrier's effect on V_{OC} was explained by a break-down of the two-diode model (due to overlapping depletion regions), in this case the two-diode model is assumed to be valid given that: a) heavy rollover was observed; b) the CdTe thickness was ~ 4 µm; and c) the simulated band-diagrams showed the depletion regions to be independent. However, Burgelman[27] reports that V_{OC} *can* be effected by the back contact in the two-diode model if either ϕ_B is sufficiently high (~ 0.6 eV), or if N_A towards the back surface of the CdTe layer is sufficiently low (10^{13} - 10^{14} cm^{-3}). This is consistent with the author's following interpretation: V_{OC} is affected by rollover if rollover begins at $V < V_{OC}$, which occurs for *J-V* curves that saturate at extremely low current in the first quadrant (e.g. < 2 mA/cm^2 for the η = 8.01% device). This occurs when the back contact saturation current, J_{b0}, is sufficiently low, and J_{b0} is known to decrease with increasing ϕ_B, and decreasing hole concentration, *p* ($\approx N_A$), at the CdTe back surface[15]. Indeed, to successfully replicate the experimental *J-V* curve with the SCAPS simulation, a lower N_A near the CdTe back surface (than in the bulk) had to be included in the device model. The depletion of holes at the back surface is, by definition, always the case when non-Ohmic contacts are made to *p*-type materials, but the non-uniformity of N_A in the CdTe may be exacerbated by insufficient Cl-doping. If the Cl-doping is indeed non-uniform and if this is detrimental to V_{OC}, then clearly the post-growth treatment of these devices remains unoptimised. This is subject to further research.

7.3.4.2 Impact of using buffer layers. Results presented in Section 7.3.3 have shown that an effective Ohmic contact can be achieved through selection of a buffer layer with appropriate physical properties. Materials that have E_{ea} such that their work function, ψ, exists between the values of the metal and CdTe ($\psi_{metal} < \psi < \psi_{CdTe}$) may be used to divide the hole barrier, ϕ_B, into two smaller barriers ϕ_{B1} and ϕ_{B2}, ultimately increasing both V_{OC} and *FF*. Presumably the total thermionic promotion of carriers across these two barriers is greater than across the original larger barrier. Alternatively, inclusion of a highly *p*-doped buffer layer has the effect of reducing the width of the barrier, this also improving device efficiency, presumably by allowing carriers to tunnel through the barrier. Indeed, this approach is used for the formation of Ohmic contacts to superstrate CdTe devices: The CdTe back surface is

chemically etched to generate a Te-rich surface making it highly p-type. However, for substrate cells, etching of the back surface is not possible. The most effective buffer layer was that which had an optimal E_{ea} and was heavily p-doped, allowing a tunnelling current at the metal/buffer layer interface and a barrier of insignificant height at the buffer layer/CdTe interface. Fahrenbruch[13] has reviewed similar methods to those proposed here, citing Cu_xTe, Sb_2Te_3 and ZnTe:N as potential materials with sufficiently high N_A (~ 10^{21}, ~ 10^{20} and ~ 10^{18} cm^{-3} respectively) but did not mention materials with $\psi_{metal} < \psi < \psi_{CdTe}$. Cu_xTe[28] and ZnTe:N[29] have been used for buffer layers in substrate devices and Romeo *et al.*[30] achieved η = 15.8% for superstrate devices upon using Sb_2Te_3 back contacts.

7.4 Carrier collection enhancements in nanowire solar cells

The remainder of this Chapter is focussed on NW based solar cells. First, in this Section, calculations of the potential efficiency gains achievable by the adoption of radial *p-n* junctions, in favour of a single planar junction, are presented. By determining the depth profile of carrier generation in CdTe, J_{SC}, V_{OC} *and* η values are estimated for planar devices and for NW devices, the impact of the depletion region width and the minority carrier diffusion length being considered.

7.4.1 Methodology

7.4.1.1 Outline of model. The model calculates the depth profiles of photo-generated carriers in CdTe structures using data for the transmittance of above-gap light as a function of CdTe thickness. Then, assuming the CdTe structures are part of a full CdS/CdTe device (where the interface is assumed to be positioned at the CdTe surface) carriers are assumed to be collected, and to contribute to J_{SC}, provided they are generated at a distance C from the CdTe surface (*p-n* junction interface) that is less than the sum of the depletion region width, W, and minority carrier diffusion length, L. Note that CdS absorption loss is not considered in this model, i.e. the CdS is assumed to be a perfect window layer with 100% transmission. The model was applied to devices based on one-dimensional planar CdTe layers, and two-dimensional CdTe NW arrays for various L and W, the principal impact of using NW arrays being to reduce C.

7.4.1.2 Short-circuit Current. First, the transmittance of light, T, as a function of CdTe thickness, X, was determined. To do this, the absorption coefficient, α, of CdTe at each wavelength, λ, was determined from the transmittance spectrum of a 1 μm thick sputtered

CdTe film on glass (sputtering parameters; $P = 70$W, $p = 1$ mTorr, $T = 250$°C, $t = 1$ hour), using a form of the Beer-Lambert law;

$$\alpha(\lambda) = \frac{-1}{X}\ln\left(\frac{T(\lambda)}{T_0}\right) \tag{7.1}$$

where T_0 is the initial transmittance. For determination of $\alpha(\lambda)$, T_0 was not taken as 1, but as $T_0(\lambda) = 1 - R(\lambda)$, where R is the total specular and diffuse reflectance of the sputtered film (~ 0.1 for above band-gap wavelengths). Using the obtained values of $\alpha(\lambda)$, $T(\lambda)$ was calculated as a function of X, in the range 0 – 3 µm, for each λ in the range 375 – 850 nm. For these transmittance depth profiles, $T_0(\lambda) = 1 - R(\lambda)$ was taken using sample specific values for $R(\lambda)$, this being different for thin-film and NW samples (see the end of Section 7.4.1.2 for the values of variables used in the model). The transmittance depth profiles were then used to calculate: a) the depth profiles of photo-generated carriers that are successfully collected, $G_{n,coll}$, in thin-film and NW devices; and b) the total J_{SC} for each device type as a function of L and W using the following procedures:

1. The CdTe layers were divided into lamellae in the z-direction (in the same plane as the incoming wavefront) each of thickness, $t = 0.005$ µm, as shown in Fig 7.12.

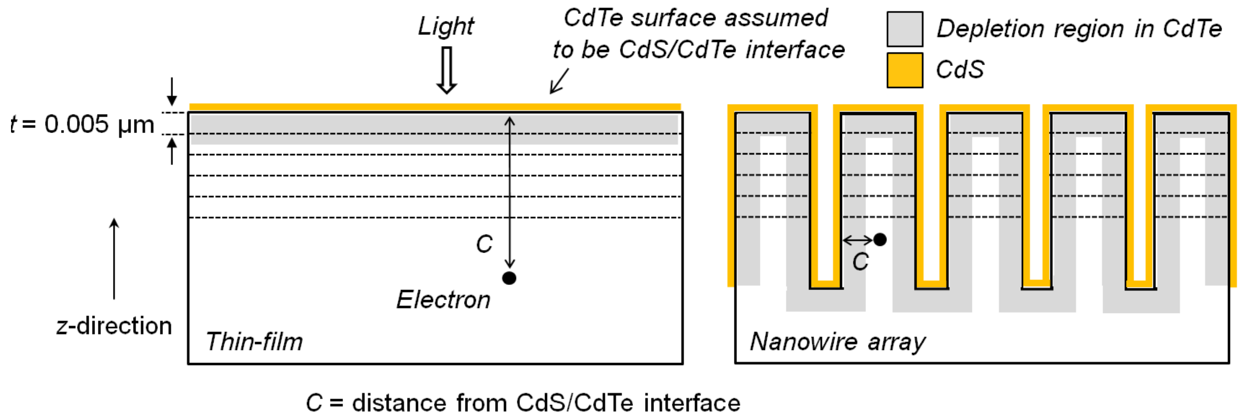

Fig 7.12: Schematic diagram showing CdTe structures used in the model. Structures are divided into lamellae, and the flux of photons absorbed in each lamellae is calculated from experimental absorbance data. Electrons generated a distance C that is less than the sum of depletion region width and minority carrier length are considered to be collected.

2. The relative amount of light absorbed, A, in each lamellae was calculated iteratively. For example, for the first lamellae, $A_1(X = t, \lambda) = T_0(X = 0, \lambda) - T_1(X = 0.005, \lambda)$ and for the nth lamellae $A_n(X = nt, \lambda) = T_{n-1}(X = nt - 0.005, \lambda) - T_n(X = nt, \lambda)$ etc.

3. To calculate the number of generated carriers in each lamellae, G_n, the product of $A(X, \lambda)$ and the photon flux, $\phi(\lambda)$ (values for $\phi(\lambda)$ were taken from data for the AM1.5 spectrum from Ref. [31]) was integrated over the entire wavelength range, as shown in the following equation;

$$G_n(X) = \int_{\lambda=375\ nm}^{\lambda=850\ nm} \big(T(X\ -0.005, \lambda) - T(X, \lambda)\big).\phi(\lambda)\ d\lambda \tag{7.2}$$

4. Collection was for $C < L + W$, so G_n was multiplied by a step function $\mathrm{H}[L + W - C]$ to calculate $G_{n,coll}$ (X);

$$G_{n,coll}(X) = \mathrm{H}[L + W - C].G_n(X) \tag{7.3}$$

where $\mathrm{H}[L + W - C] = 0$ if $(L + W - C) < 0$ and $\mathrm{H}[L + W - C] = 1$, if $(L + W - C) \geq 0$. For the representation of the depth profiles shown in Section 7.3.2, $G_{n,coll}$ was normalised. The main principle behind the difference between thin-film and NW devices is that C is modified by the adoption of radial junctions (Fig 7.12).

5. To calculate the total J_{SC}, $G_{n,coll}(X)$ was summed over the full thickness of the device and the result was multiplied by the electron charge, q;

$$J_{SC} = q \sum_{X=0}^{X=X_{full}} G_{n,coll}(x) \tag{7.4}$$

These calculations were carried out using $W = 0.2 – 1$ µm, and $L = 0.1 – 1.0$ µm for: a) Thin-film devices; b) NW devices having vertical NWs (length, $l = 2$ µm, diameter, $D = 900$ nm and spacing, $S = 200$ nm) grown on a 500 nm thick CdTe film; and c) NW devices having randomly oriented NWs but with the same dimensions as in b.

Values for $R(\lambda)$ were taken as 0.1 for thin films and vertical NWs and 0.001 for randomly oriented NWs, these values being constant across the entire wavelength range - values for thin film and random NWs taken from measurements, and value for vertical NWs assumed to be the same as thin film. For the random array of NWs, the carrier collection was modelled to be the same as that for vertical NWs, the only difference between the random and vertical NWs accounted for in the model was the different values of R.

7.4.1.3 Open-Circuit Voltage. Assuming a PV device may be modelled as an ideal diode, the relation between V_{OC} and J_{SC} can be derived from Equation 2.5, setting $J_L = J_{SC}$ and using an ideality factor of 1;

$$V_{OC} = \frac{k_B T}{q} ln\left(\frac{J_{SC}}{J_0} + 1\right) \approx \frac{k_B T}{q} ln\left(\frac{J_{SC}}{J_0}\right) \quad (7.5)$$

Hence, V_{OC} was also calculated for the different device types as a function of L and W. For thin-film devices a typical value of J_0 was used, as extracted from the PV performance parameters of a high-efficiency CdTe device[32] (η = 16.5 %, FF = 75.51 %, J_{SC} = 25.88 mA.cm^{-2}, V_{OC} = 845 mV), i.e. $J_0 = 1.7 \times 10^{-13}$ mA.cm^{-2}. For radial *p-n* junction devices, J_0 may be assumed to scale with junction area[33], i.e. $J_{0,radial} = \gamma \times J_{0,planar}$ where γ is the total junction area of a radial junction device divided by that of a thin-film device. By using the NW dimensions as above, and modelling the NWs as cylindrical, $\gamma = 1.57$. To calculate η, FF was assumed to be independent of device type and of L and W, and was taken to be FF = 75.51%.

7.4.2 Results

Fig 7.13 shows a map of T for a planar CdTe film as a function of both X and λ, the inset showing the total integrated T (in the range λ = 375 – 850 nm) as a function of X.

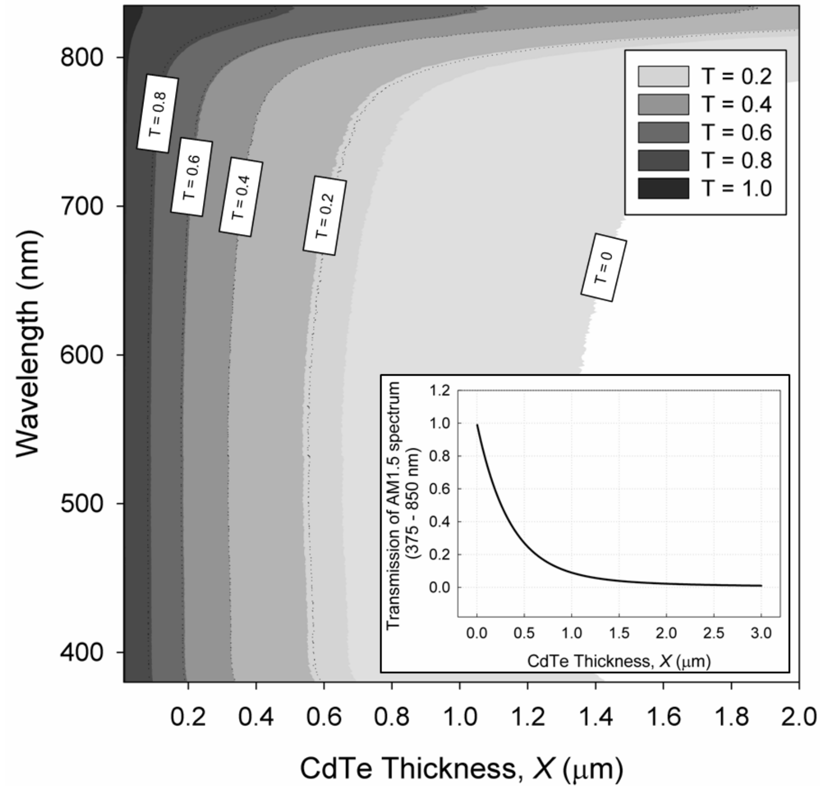

Fig 7.13: Transmittance as a function of CdTe thickness (*x*-axis) and wavelength (*y*-axis). Inset: total transmittance integrated across the wavelength range 375 – 850 nm as a function of CdTe thickness.

Approximately 99.9% of the integrated spectrum is absorbed by films 2 μm thick, ~ 90% by films 1 μm thick and ~ 75% by films 0.5 μm thick. There is little λ dependence on the depth profile of T in the range 375 – 650 nm, these wavelengths being completely absorbed by 1.4 μm of material, whereas longer wavelengths (650 – 750 nm) penetrate deeper (~ 1.8 μm). Longer wavelengths still (> 750 nm), i.e. approaching the CdTe optical band-gap, penetrate to depths > 2 μm. This data was used for generating depth profiles of carrier generation in CdTe structures and for calculating J_{SC} and V_{OC} in CdTe devices using the model described in Section 7.4.2. These results are now described.

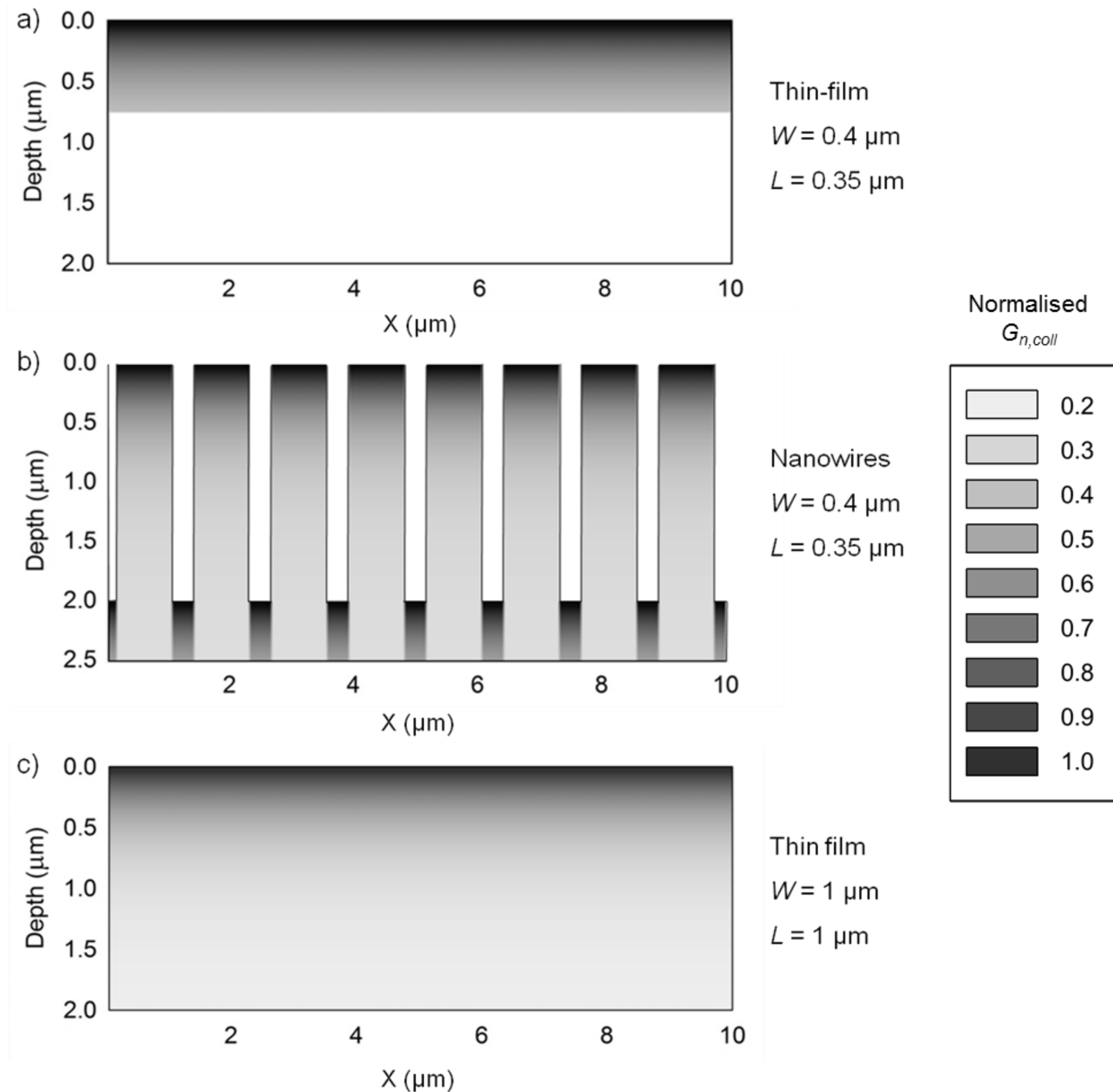

Fig 7.14: Depth profiles of photo-generated carriers that are successfully collected, $G_{n,coll}$, for a) thin-film CdTe with W = 0.4 μm, L = 0.35 μm, b) CdTe NW array with W = 0.4 μm, L = 0.35 μm and c) thin-film CdTe with W = 1 μm, L = 1 μm. $G_{n,coll}$ is normalised against the peak value.

Depth profiles of photo-generated carriers which are successfully collected, $G_{n,coll}$, for different device configurations and different values of L and W are shown in Fig 7.14. These diagrams show just the CdTe absorbing layer, be it a film or nanowire array, but the CdS/CdTe interface is assumed to be at the CdTe surface for each. Fig 7.14a shows that for relatively low quality material (L = 0.35 μm) and narrow depletion regions (W = 0.4 μm), a significant proportion of the generated carriers are not successfully collected by a planar junction, due to them being generated a distance, $C > L + W$ from the CdS/CdTe interface: This is evident from the abrupt cut-off of the generation profile 0.75 μm from the interface. In contrast, by using the NW configuration (Fig 7.14b) all photo-generated carriers are successfully collected since they are all generated a distance $C < L + W$ from the CdS/CdTe interface. However for higher quality material (L = 1 μm) and with a wider depletion region (W = 1 μm) thin-film devices may also collect all photo-generated carriers, this being evident from there being no cut-off of the generation profile in Fig 7.14c.

Fig 7.15a - c shows J_{SC}, V_{OC} and η respectively as a function of W and L for thin-film, vertical NW and random NW devices. Typical literature values of L in CdTe solar cells are included in Fig 7.15a. For thin-film devices, J_{SC} is heavily dependent on L when W is small (0.2 μm), ranging from 14 – 23 mA.cm^{-2} in the range L = 0.1 – 1 μm, but is much less so when W is large (1 μm), ranging from 23 – 24 mA.cm^{-2} in the same L range (Fig 7.15a). In the same sense, at low L, J_{SC} is heavily dependent on W but at high L values it is less so.

In contrast, the J_{SC} of NW devices is independent of L for values of W as low as 0.4 μm, because in this case all generated carriers are successfully collected as $C < L + W$. The consequence of this is that for medium-to-poor quality material (L = 0.1 – 0.7 μm) and with relatively narrow depletion regions ($W \leq 0.4$ μm), J_{SC} enhancements are obtainable via the adoption of radial junctions. However, the maximum obtainable J_{SC} of vertical NW devices (23.5 mA.cm^{-2}) is lower than that of the thin-film devices (24.1 mA.cm^{-2}) because of transmission losses. On the other hand, randomly-oriented NW devices have the highest maximum J_{SC} - similarly independent of L when $W \geq 0.4$ μm - due to them having lower reflectance (J_{SC} = 26.9 mA.cm^{-2}).

The dependence of V_{OC} on L and W for thin-film devices is similar to the dependence of J_{SC}, but to a much lesser extent since V_{OC} follows a logarithmic dependence on carrier collection. V_{OC}'s of both vertical and random NW devices are actually lower than those of thin-films for most values of L because of higher saturation current, J_0. However, since the dependence of V_{OC} on C, L and W is significantly weaker than that of J_{SC}, the overall variation

of η is mainly influenced by the variation of J_{SC}, hence significant η enhancements may be achievable (at least a few percent) by adopting the radial geometry provided L is low.

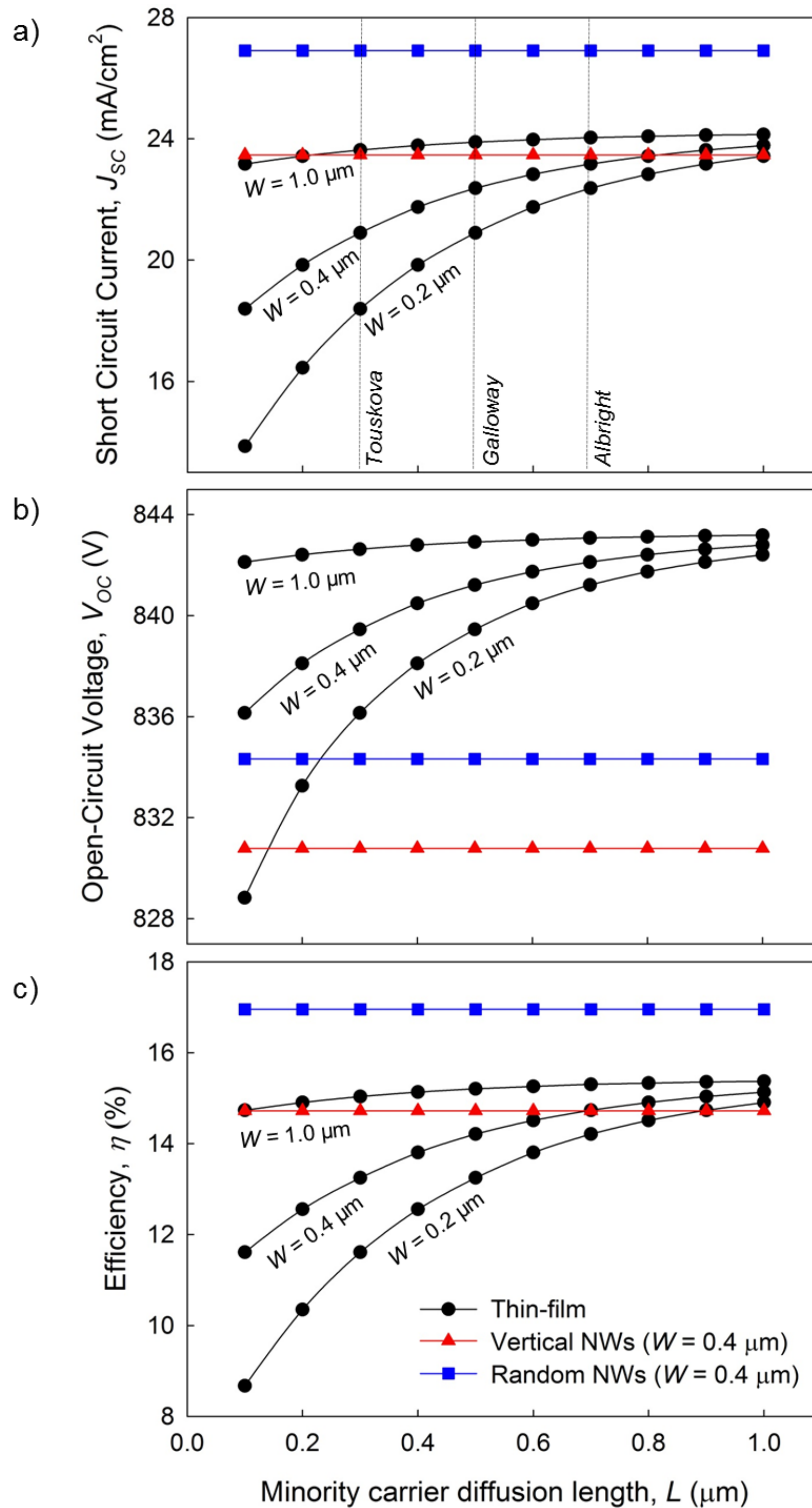

Fig 7.15: a) J_{SC}, b) V_{OC} and c) η as calculated for thin-film CdTe devices (black), vertical CdTe NW devices (red) and randomly oriented CdTe NW devices (blue) as a function of L and W. Typical values of L in CdTe solar cells, taken from the literature[34-36], are shown on a).

7.4.3 Discussion of nanowire device modelling

The principal findings from modelling are now summarised. 1) Significant improvements to η upon replacing the planar junction with an array of radial junctions may only be realised provided $L \leq 0.7$ µm and $W \leq 0.4$ µm. 2) At higher values of L or W, carrier collection in thin-film CdTe devices is sufficient that it does not limit device performance, rendering the NW device concept unnecessary (only in terms of carrier collection). 3) Transmission losses in vertical NW devices, associated with the sub-100% packing fraction, actually makes thin-film devices more favourable when L and W are high. 4) The reduced reflectance of randomly oriented NW arrays may in itself result in significant J_{SC} and η enhancements.

Whilst it appears that the advantages of the radial junction design are only apparent for a narrow range of CdTe material properties, it is quite common for L to be < 0.7 µm in CdTe[34-36]. Indeed, by lowering the limit for material quality, the cost of CdTe solar cells may ultimately be lowered. On the other hand, W is commonly at least 1 µm in CdS/CdTe devices, and such a value would render the radial geometry unnecessary, although this is dependent on the *p*-type doping density N_A (Equation 2.3).

Similar calculations have previously been carried out for comparing the performances of bulk Si solar cells and Si-NW solar cells[33], showing that the differences may be significantly greater than for the CdTe system. This is directly related to the absorption efficiency of the differing materials: CdTe films just 2 µm thick may absorb > 99% of incoming above-band gap light and so a large fraction of carriers are generated within the depletion region or sufficiently close (< L) to it, whereas in Si devices, wafers > 100 µm thick are required to absorb an equivalent amount of light, and so a significant proportion of carriers are generated far (> L) from the depletion region. Ultimately, these results support the hypothesis that the radial junction solar cell concept offers fewer advantages to direct band-gap materials than to indirect band-gap materials. Nevertheless, the reduced reflectance of random NW arrays, relative to films, for the CdTe system should in itself yield significant η improvements.

In terms of commenting on the optimal NW dimensions, it is clear that all generated carriers are collected if the NW diameter, $D < 2(L + W)$. (In these calculations, $D = 900$ nm, and so all carriers were collected in the entire L range for $W \geq 0.4$ µm). Relating this to the results of VLS-NW growth presented in Chapter 5, whereby D was in the range 50 – 500 nm, it could be argued that all NWs grown by the methods reported in this thesis are suitable. However, for relatively small values of W, such NWs would be completely depleted, this reducing the built in voltage of the device and complicating the issues of majority carrier transport[33]. Hence, it may be desirable for NWs to be sufficiently thick so that they are not

completely depleted, but sufficiently thin to collect carriers, i.e. $2W < D < 2(L + W)$. In terms of height, CdTe NWs theoretically need only be at least 2 μm long to sufficiently absorb the light, although the light-trapping advantages of random arrays may only be realised for longer NWs. In terms of NW spacing, it must be sufficiently small so to minimise absorption loss.

On the subject of light absorption it should be noted that the model used here oversimplifies the operation of random NW devices, as the angle of incidence would vary from wire to wire, resulting in varying optical path lengths, and carrier generation profiles. Indeed, even for vertical NWs, whilst non-uniformities in the carrier generation in the axial direction of NWs was taken into account, those in the radial direction were not: In reality, the radially oriented depletion regions in NW devices would affect the radial carrier concentration profile due to diffusion and drift of carriers caused by the potential drop at the *p-n* junction. For a more complex model of NW device operation for the Si and GaAs systems, the reader is referred to Ref. 33.

7.5 Growth and characterisation of CdTe nanowire solar cells on Mo

In this Section, characterisation of ITO/ZnO/CdS/CdTe(NW)/CdTe/Mo solar cells is presented, with the effect of various post-growth treatments and NW dimensions on device performance being investigated.

7.5.1 Experimental procedure

7.5.1.1 Deposition conditions for ITO/ZnO/CdS/CdTe(NW)/CdTe/Mo devices and post-growth treatment. Au-catalysed CdTe NWs were grown on CdTe/Mo substrates by the VLS mechanism using the metamorphic approach (see Chapter 5 for further details), with the CdTe films onto which NWs were grown being 0.75 – 2.5 μm in thickness. The function of this film is to prevent short-circuiting through the device, and it is referred to as the ‘blocking layer’ elsewhere in this thesis. These CdTe blocking layers were sublimation grown on Mo using a source temperature of 605°C under 25 Torr N_2 for 1 – 3 mins with the substrates held at 530°C. Following evaporation of Au films onto these blocking layers and annealing (in-situ in the CSS system at 360°C), sublimation growth of NWs took place for 4 – 8 mins using a source temperature of 570°C under 10 Torr N_2, with the substrates held at 520°C. This generated NWs of length, $l = 2 – 20$ μm, diameter, $D = 50 – 200$ nm and NW densities of 10^7 – 10^8 cm^{-3}. For some NW arrays, D was ‘thickened’ by coating the NWs with sputtered CdTe shells for 120 mins, using a target power of 70W, under 10 mTorr with the substrate held at 250°C. (Preliminary growth experiments aimed at VLS-growth of NWs with $D > 500$ nm

proved unsuccessful, largely due to the instability of larger catalysts). For *all* NW arrays, CdS, ZnO and ITO shells were generated by RF sputtering, using the same deposition conditions as for planar substrate cells (see Section 7.2.1.1) but with their respective deposition times being 120, 50 and 180 mins generating shell thicknesses of approximately 200 nm, 20 nm and 100 nm as determined by SEM (the radial uniformity of these shells were inconsistent, see Chapter 5): Longer deposition times were required since the surface area of NW arrays is greater than planar films.

Four different Cl-activation procedures were attempted, these being summarised in Table 8 and now described (all annealing stages were carried out in air for 30 mins):

Treatment A_{NW}) No Cl-treatment was applied to either the blocking layer or the NWs.

Treatment B_{NW}) No Cl-treatment to the blocking layer, but following NW growth, 200 nm $CdCl_2$ was deposited and structures were annealed at 420°C.

Treatment C_{NW}) Following growth of blocking layer, 200 nm $CdCl_2$ was deposited and films were annealed at 420°C with no Cl-treatment being applied following NW growth.

Treatment D_{NW}) Cl-treatment (as above) was applied following blocking layer growth and again following NW growth.

All samples were annealed in air for 30 mins at 500°C following growth of all layers, this stage having being shown to be necessary for planar substrate devices to improve junction formation. Samples were mechanically scribed into 2.5 mm x 2.5 mm individual devices.

Table 7.6: Annealing processes applied to NW solar cells. Each annealing step was carried out in air for 30 mins, see text.

Treatment	*After CdTe film deposition*	*After CdTe NW deposition*	*After ITO dep.*
A_{NW}	-	-	T_{Final} = 500°C
B_{NW}	-	200 nm $CdCl_2$ T_{NWs} = 420°C	T_{Final} = 500°C
C_{NW}	200 nm $CdCl_2$ T_{Film} = 420°C	-	T_{Final} = 500°C
D_{NW}	200 nm $CdCl_2$ T_{Film} = 420°C	200 nm $CdCl_2$ T_{NWs} = 420°C	T_{Final} = 500°C

7.5.1.2 Characterisation. *J-V* measurements were carried out under AM1.5 illumination, *J-V-T* measurements were conducted in the dark, in the temperature range 200 – 350K, and *EQE* data was collected with white light bias. SEM images of NW arrays and full NW devices

were recorded in secondary electron mode with cross sections of devices being prepared by mechanical scribing. The microstructure of sputtered CdTe shells was investigated by TEM.

7.5.2 Nanowire device results

7.5.2.1 SEM characterisation. For all NW devices described in this Section, the CdTe NW dimensions and the thickness of the blocking layer were kept constant and no devices included the sputtered CdTe shell. Fig 7.16a shows an SEM image of a cross section of a typical ITO/ZnO/CdS/CdTe(NW)/CdTe/Mo device and Fig 7.16b shows an array of core-triple shell NWs from the same device.

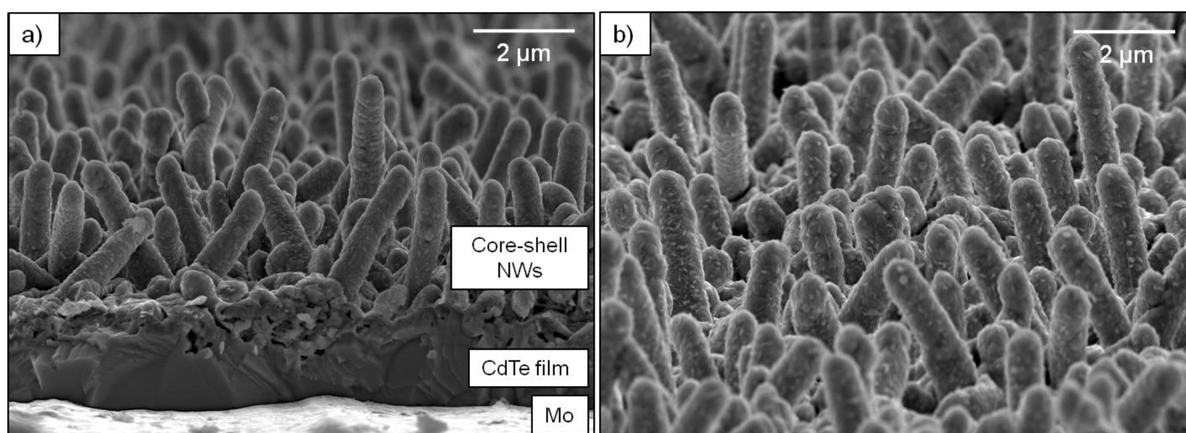

Fig 7.16: a) Secondary electron SEM image of a cross-section of an ITO/ZnO/CdS/CdTe(NW)/CdTe/Mo device. b) Core-shell NWs from the same device.

The CdTe blocking layer is ~ 1.5 µm thick and consists of grains with lateral diameters of up to 2 µm and which extend the entire thickness of the film. The NWs atop have lengths in the range 2 – 6 µm, are 300 – 600 nm in diameter (including the core and shells) and appear to have a random distribution of tilt angle with respect to the substrate. In some instances NW tilting results in adjacent NWs touching each other. There appears to be some voids towards the upper section of the blocking layer, i.e. near the CdS/CdTe interface. The ITO shell on the NWs is rough and has grain sizes of the order of ~ 100 nm.

7.5.2.2 The impact of the $CdCl_2$ activation step. The average performance parameters for devices subject to treatments A_{NW}, B_{NW}, C_{NW} and D_{NW} are shown in Table 7.7, 16 devices were measured in each case. Representative *J-V* curves for devices subject to procedures C_{NW} and D_{NW} are shown in Fig 7.17. A narrow distribution of performance was obtained upon varying the post-growth treatment procedure, relative to that obtained upon varying the treatment of planar devices (Table 7.2), with all individual devices having efficiencies in the range $\eta = 0.5 – 1.5\%$. Nevertheless, some common trends were observed. For instance, the average η for devices for which the NWs were Cl-treated (B_{NW} and D_{NW}) was higher than those for which

they were not (A_{NW} and C_{NW}), primarily due to higher J_{SC} (~ 6.5 mA.cm^{-2} compared to 4.5 mA.cm^{-2}) and *FF*. The difference in *FF* is clearly demonstrated by the shape of the respective *J-V* curves (Fig 7.17): A device for which the NWs were treated (D_{NW}) has both lower R_S (38.5 Ω.cm^2) and higher R_{SH} (982 Ω.cm^2) than a device with untreated NWs (C_{NW}, R_S = 50.8 Ω.cm^2 and R_{SH} = 441 Ω.cm^2). Indeed, the poor R_S of the device subject to treatment C_{NW} is detrimental to its J_{SC} in this case. Nevertheless R_S for both devices is remarkably high, partly due to the rollover that is to be expected from the poor CdTe/Mo contact (see Sections 7.2 and 7.3). Treatment D_{NW} yielded the best device (η = 1.32 %) of all and the highest average η compared to the other treatments.

Table 7.7: A comparison of the average performance parameters of NW devices subjected to different post-growth annealing processes (see Table 7.6 and text).

Treatment	η (%)	J_{SC} (mA/cm^2)	V_{OC} (mV)	*FF* (%)
A_{NW}	0.67 ± 0.15	4.90 ± 1.1	520 ± 7	26.8 ± 1.1
B_{NW}	1.00 ± 0.11	6.30 ± 0.66	535 ± 30	29.1 ± 1.8
C_{NW}	0.65 ± 0.20	4.58 ± 0.98	480 ± 2	29.5 ± 4.0
D_{NW}	1.10 ± 0.17	6.57 ± 0.52	478 ± 30	34.9 ± 1.6

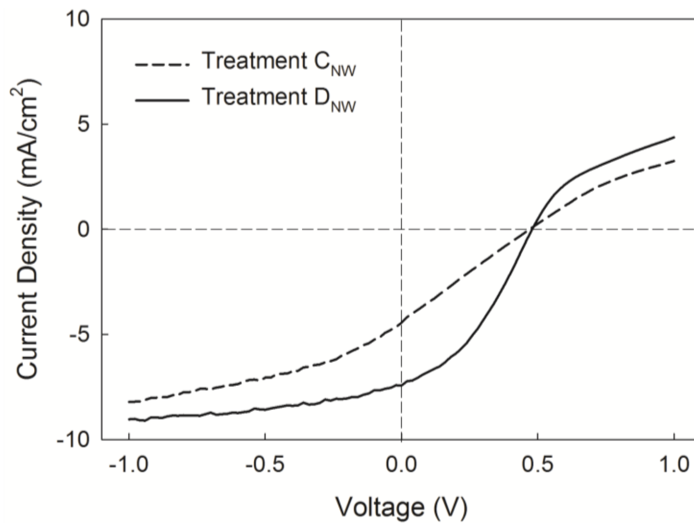

Fig 7.17: *J-V* curves of ITO/ZnO/CdS/CdTe(NW)/CdTe/Mo devices that were subject to treatment C_{NW} (dashed line, η = 0.53%) and treatment D_{NW} (solid line, η = 1.32%).

Other notable observations concerning the post-growth treatment are: a) Devices for which the blocking layer was Cl-treated (C_{NW} and D_{NW}) had lower V_{OC} (~ 480 mV) than those for which it was not (~ 530 mV); b) devices for which just the NWs were Cl-treated (B_{NW}) had efficiencies twice as high as those for which just the blocking layer was Cl-treated (C_{NW}); and

c) for all devices, V_{OC} was not significantly lower than that for planar devices (the best was 690 mV) hence J_{SC} and FF are highlighted as the major limitations to NW device efficiency.

7.5.2.3 Effect of NW dimensions and blocking layer thickness. To investigate the effect of NW dimensions on device performance, devices having NWs of different l and D were grown. Fig 7.18 shows the different NW types, these being:

a) Type-I NWs with l ~ 5 – 10 μm and D ~ 100 – 200 nm (Fig 7.18a and b), grown by sublimation for 4 mins;

b) Type-II NWs with l ~ 5 – 10 μm and D ~ 1 – 2 μm (Fig 7.18c and d) which are core-shell CdTe/CdTe NWs grown by a combination of sublimation (4 mins) and sputtering; and

c) Type-III NWs with l ~ 10 – 20 μm and D ~ 100 – 200 nm (Fig 7.18e and f), grown by sublimation for 8 mins.

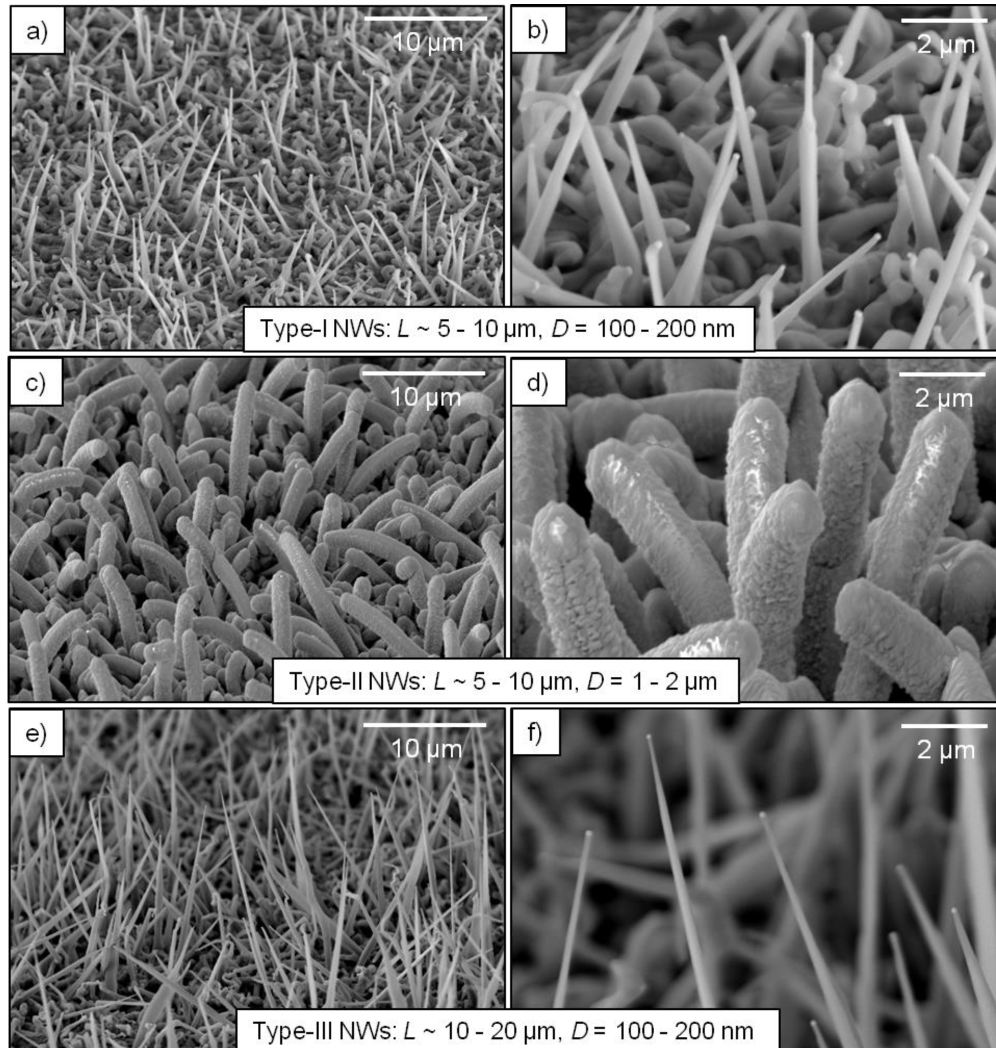

Fig 7.18: Secondary electron SEM images of NWs with different dimensions used within NW solar cells: a) and b) Type I NWs with L ~ 5 – 10 μm and D ~ 100 – 200 nm, c) and d) Type-II NWs with L ~ 5 – 10 μm and D ~ 1 – 2 μm and e) and f) Type-III NWs with L ~ 10 – 20 μm and D ~ 100 – 200 nm. See Table 7.8 and text for device performances.

Type-I and type-III NWs are assumed to be monocrystalline, as all other VLS-grown NWs reported in this work. However for the type-II NWs the sputtered outer shell was polycrystalline as may be seen from the TEM image in Fig 7.19. Within the shell numerous grains exist (~ 100 nm in diameter), each of which contains a high density of twins.

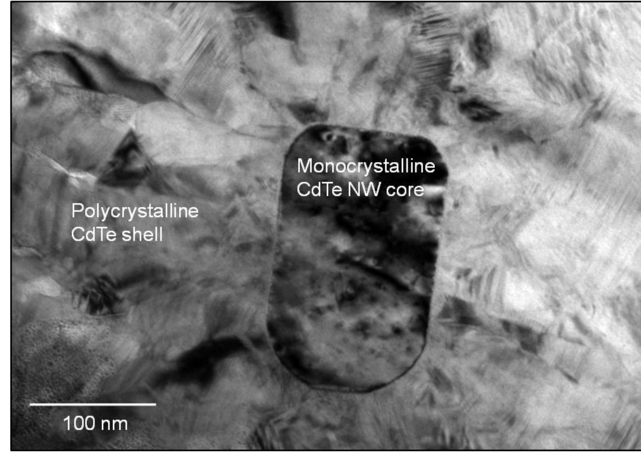

Fig 7.19: Bright-field TEM image of a cross section of a core-shell CdTe/CdTe NW (Type-II, see text and Fig 7.18). The core was VLS-grown by sublimation and the shell was sputter deposited.

Table 7.8: Performance parameters for the best devices fabricated from each NW type, see text and Fig 7.18.

NW Type	*L* (µm)	*D* (µm)	*η* (%)	J_{SC} (mA/cm²)	V_{OC} (mV)	*FF* (%)	R_S (Ω.cm²)	R_{SH} (Ω.cm²)
I	5 - 10	0.1 – 0.2	2.49	13.9	523	34.3	25.5	269
II	5 - 10	1 – 2	0.25	1.51	536	30.3	234	735
III	10 - 20	0.1 – 0.2	1.12	6.20	541	33.5	62.1	584

Table 7.8 shows the performance parameters of the best devices fabricated from each NW type (following deposition of the remaining ITO/ZnO/CdS), these devices having a blocking layer thickness of 0.75 µm and being subject to treatment D_{NW} (identified as the most effective treatment from Section 7.5.2). The *J-V* curves of these devices are shown in Fig 7.20.

The highest η (2.49%) was achieved using NW type-I and the lowest (η = 0.25%) using NW type-III. The V_{OC} and *FF* for the three device types are similar (in the ranges 523 - 541 mV and 30.3 – 34.3% respectively), but J_{SC} varies substantially (13.9, 1.51 and 6.20 mA.cm^{-2} for devices with NW types I, II and III respectively), this being the principle cause of the performance differences. The best device (type-I) has the lowest R_S (25.5 Ω.cm^2, which is

still high compared to thin film devices) but also the lowest R_{SH} (269 Ω.cm^2). The poorest device (type III) has an extraordinarily high R_S (234 Ω.cm^2) but also the highest R_{SH} (735 Ω.cm^2). All devices demonstrate significant rollover in the first quadrant as was observed for thin-film substrate devices.

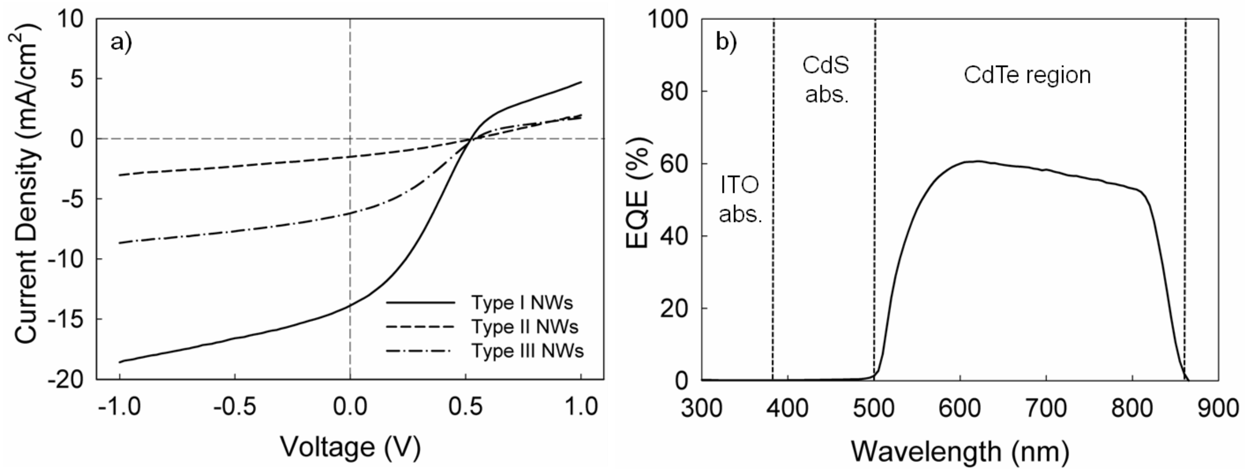

Fig 7.20: a) *J-V* curves of the best devices fabricating using NWs of different dimensions, see text and Fig 7.18 for description and images of NW types. b) *EQE* response of the best performing NW device, having η = 2.49%.

The *EQE* response of the best performing NW device is shown in Fig 7.20b, demonstrating a well-defined top hat function bound by the optical band-gaps of CdTe and CdS and peaking at ~ 60%. The gradual downward slope (from 600 to 800 nm) in the active region implies some losses at long wavelengths and the very poor blue-response (< 500 nm) suggests there is significant CdS absorption.

7.5.2.4 Effect of blocking layer thickness. Fig 7.21a - d shows, respectively, the average η, V_{OC}, J_{SC} and *FF* of NW devices fabricated from NW types I – III, having been subject to treatments C_{NW} and D_{NW}, as a function of blocking layer thickness.

Again, the highest efficiencies were achieved by using NWs of type-I (*L* ~ 5 – 10 μm, *D* ~ 100 – 200 nm) and post-growth treatment D_{NW}, this principally resulting from higher J_{SC}. It is notable that there is little dependence of device performance on the thickness of the blocking layer. In particular, the data for V_{OC} and *FF* is too scattered to confidently identify any trends.

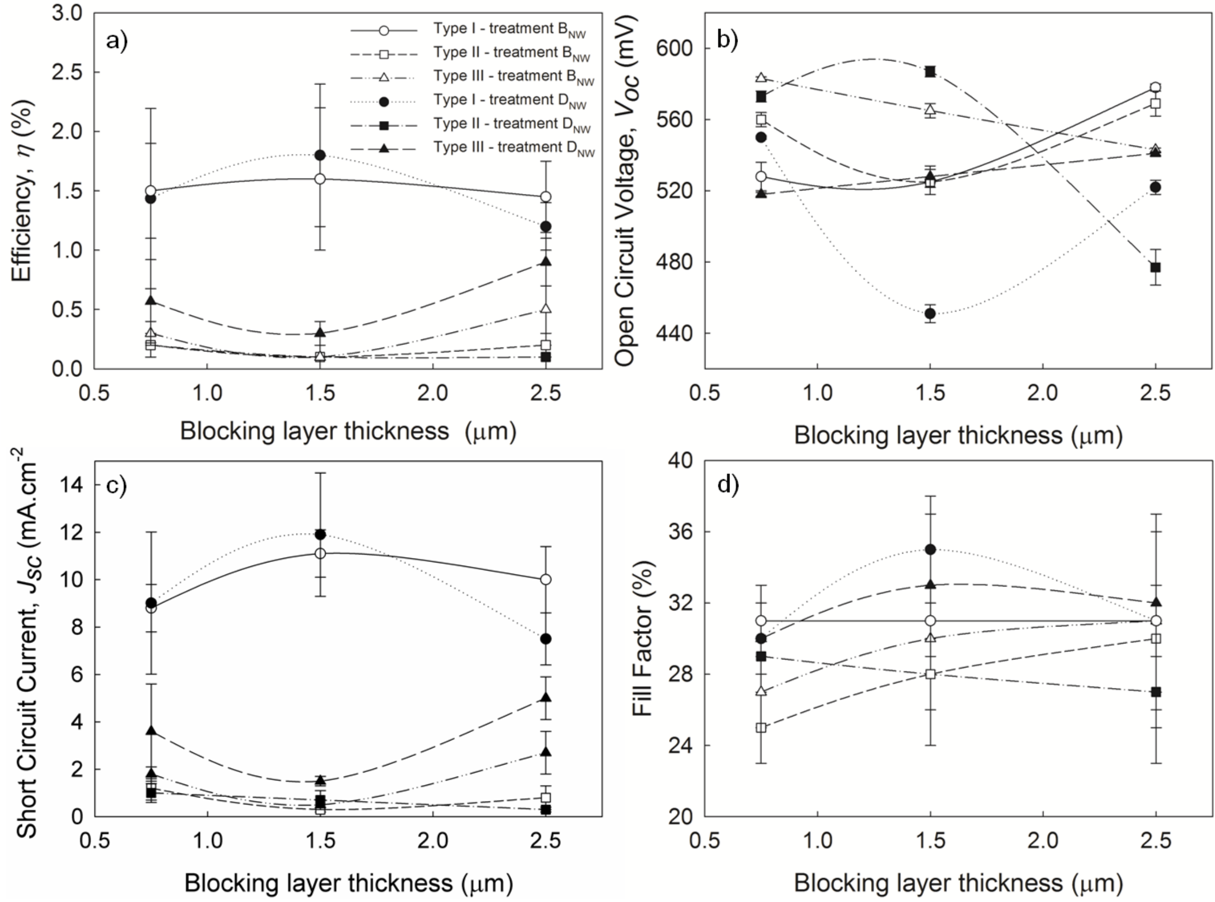

Fig 7.21: Average a) η, b) V_{OC}, c) J_{SC} and d) FF of NW devices as a function of blocking layer thickness, NW dimensions and post-growth treatment.

7.5.2.5 Temperature dependent J-V measurements. Fig 7.22 shows the results of *J-V-T* measurements carried out on a NW device (η = 1.5%) having NWs of type-I, blocking layer thickness of 0.75 μm and having been subject to treatment D_{NW}.

From the temperature dependence of R_S (Fig 7.22a), a value of ϕ_B = 0.52 eV was determined using the method of Bätzner[4], this being comparable to that measured for the thin-film substrate devices (ϕ_B = 0.51 eV). Also similar to thin-film devices is the inference from temperature dependent plots of n and J_0 (Fig 7.22b) that there are two temperature ranges within which the dominant transport mechanism is different. At high T (> 240K) the $\ln(J_0) \propto -1/T$ dependence and an ideality factor of 2 is indicative of recombination in the depletion region, whereas at low T (≤ 240K) the observation that ideality factor increases as T is decreased is indicative of a tunnelling regime. Perhaps significantly, the temperature at which the change is observed (240K) is lower than observed for thin-film devices (270K).

At room temperature (T = 300K), the saturation current density for the NW device was $J_{0,NWs} = 1.1 \times 10^{-7}$ A.cm^{-2}, whereas for the thin-film device presented in Section 7.2, it was half this value, $J_{0,thin\text{-}film} = 5.8 \times 10^{-8}$ A.cm^{-2}.

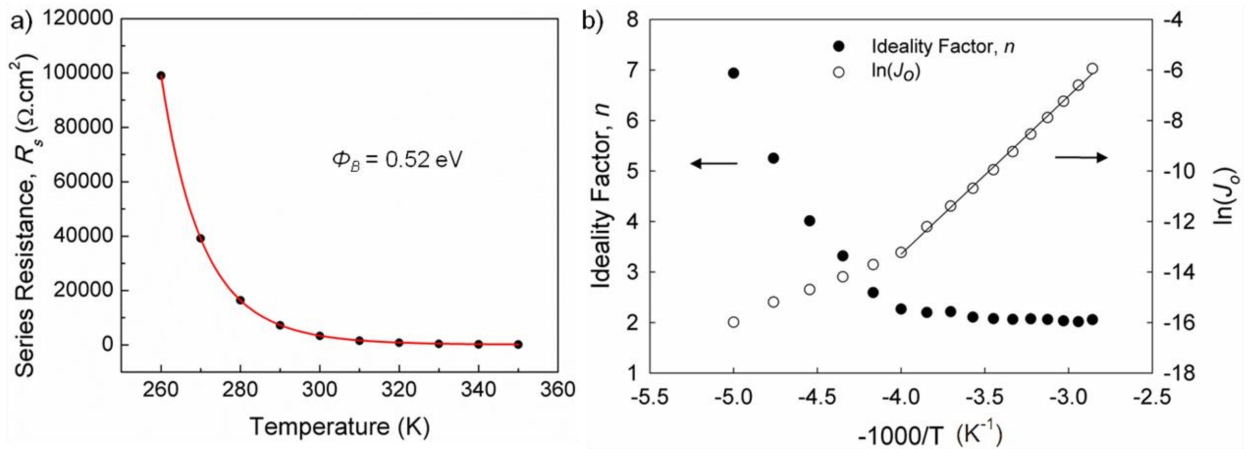

Fig 7.22: Temperature dependent electrical measurements for a nanowire solar cell. a) The temperature dependence of R_S, used to determine the back contact barrier height, $\boldsymbol{\phi_B}$. b) Temperature dependence of the ideality factor, n, and the saturation current, J_0. This data was taken from a NW device subject to treatment D_{NW}, having NWs of type-I and a blocking layer thickness of ~ 0.75 µm and for which η = 1.5%. A good fit to the relationship ln(J_0) ∝ *-1/T* was obtained in the range T = 240 – 350 K.

7.5.3 Discussion of nanowire device experimental results

The fabrication of complete solar cells based on core-triple shell ITO/ZnO/CdS/CdTe NWs has been presented, with a peak performance of η = 2.49% having been obtained. This represents the first successful demonstration of radial *p-n* junction devices using CdTe core NWs and CdS shells. The optimal post-growth treatment method was to carry out Cl-treatment subsequent to blocking layer deposition and to NW deposition, followed by a final annealing treatment after all layers had been deposited.

7.5.5.1 Losses in NW devices. The best efficiencies recorded for NW devices are approximately one third of those recorded for thin-film devices that have the same layer configuration, i.e ITO/ZnO/CdS/CdTe/Mo, reasons for this discrepancy now being discussed. Whilst there was significant rollover of the *J-V* curves of NW devices, limiting *FF* and arguably V_{OC}, this was also the case for thin-film substrate devices, and indeed the height of the Schottky barriers at the back contact in each device type were highly comparable (ϕ_B = 0.51 – 0.52 eV). Since the V_{OC} of the best NW device (523 mV) was just short of 80% of the highest achieved for thin-film substrate devices (690 mV), V_{OC} is not considered to be the principle limitation. However the *FF* and J_{SC} of the best NW device (34.9% and 13.9 mA.cm^{-2}) were significantly lower than that of the best thin-film device (51.9% and 22.4 mA.cm^{-2}). The very low R_{SH} in the NW device, which contributes to the poor *FF*, may be attributed to shunting paths associated with the voids observed in the blocking layer. Insufficient coating of

the NW arrays with the shell layers and coalescence of neighbouring wires may also be responsible. The high R_S of the NW devices (R_S = 25.5 Ω.cm^2 for the best device), also contributing to the low *FF*, is partly attributable to the poor back contact, but since it remains much higher than substrate devices (9.89 Ω.cm^2 for the best device), it may imply that there is significant intrinsic resistance within the NWs themselves. It is likely that the NWs used in this work are too long in this respect: CdTe films of thicknesses exceeding 10 μm typically have high R_S and here NWs were up to 20 μm in length. Indeed devices having NWs with l = 10 – 20 μm had greater R_S and lower J_{SC} (62.1 Ω.cm^2 and 6.20 mA.cm^{-2}) than those having NWs with l = 5 – 10 μm (25.5 Ω.cm^2 and 13.9 mA.cm^{-2}).

Whilst device modelling suggested NW diameters of $D \sim 1$ μm are suitable for obtaining high η, here the NWs with the greatest diameters (type-II NW, D ~ 1- 2 μm) had the lowest η and J_{SC} and the highest R_s, although this may largely be a consequence of the polycrystallinity and high defect density in the CdTe shell that was used in these devices. Ideally, monocrystalline NWs with large D were to be grown by the VLS mechanism, but preliminary experiments revealed that Au catalysts of D > 500 nm became unstable during growth and the VLS mechanism failed.

The *EQE* response showed significant losses in the blue-response of NW devices. Long deposition times were used for the CdS window layers to sufficiently coat the NW arrays as a result of their large surface area and the resulting high volume of CdS present in the devices increased the CdS absorption to an extent that no carriers generated by photons of wavelength < 500 nm contribute to J_{SC}.

7.5.5.2 Contribution of NWs and blocking layer to photocurrent. It remains unconfirmed as to whether the main contribution to the photocurrent in these devices is from the NWs themselves or rather from the underlying blocking layer, which at 0.75 μm thick would be able to absorb 75% of above band-gap light in the absence of NWs. From the results presented, there is evidence for and against the argument that the NWs make a significant contribution. Firstly, the observation that the performance parameters were independent of the thickness of the blocking layer but were highly dependent on NW dimensions may imply that photogeneration occurs predominantly in the NWs, particularly since the performance of thin-film devices are usually heavily dependent on CdTe thickness (see Section 7.2). Moreover, since Cl-activation of CdTe is often necessary to enhance device performance, the fact that devices whereby just the NWs were Cl-treated (treatment B_{NW}) had efficiencies twice as high as those whereby just the blocking layer was Cl-treated (treatment C_{NW}) also implies that the NWs make the most significant contribution. However, it may be the case that the η

dependence on NW dimensions is a result of their presence being detrimental to device performance via shadowing of the photoactive blocking layer, particularly since the devices that had the highest efficiencies were those with the thinnest and shortest NWs (type-I) and since devices with longer or thicker NWs mainly suffered from low J_{SC}. Indeed, NWs having diameters such as those in this work (D ~ 0.1 – 2 μm) may be completed depleted of carriers considering that a typical value for the depletion region width in CdS/CdTe devices is ~ 1 μm.

The contribution of the NWs to the photocurrent may further be investigated using the electron beam induced current (EBIC) method in the SEM. This will give a direct image of the junction position. The blocking layer was included in the device design here to prevent the formation of shunting pathways, but an alternative configuration consisting of NWs directly grown on the Mo substrate electrically isolated by an insulating in-fill could yield insights as to whether the NWs successfully generate photocurrent.

7.5.5.3 J-V-T measurement. One of the significant findings was that in NW devices the transition from a tunnelling dominated charge transport mechanism to a recombination dominated transport mechanism occurs at a lower temperature (240K) than in thin-film devices (270K). Since a tunnelling dominated mechanism involves the trapping of carriers at localised interface states, it may be said that the transition to a recombination dominated regime occurs when kT is sufficiently high such that carriers are de-trapped from localised states. The occurrence of this at lower temperatures for NW devices implies that the energy separation between traps in NW devices is smaller than in thin-film devices, hence there is a greater density of localised states distributed within the band-gap. This would be consistent with the CdS/CdTe interface having a larger surface area in NW devices and therefore more surface states. Indeed, the saturation current density, which is said to increase with junction area, was twice as large in NW devices than in thin-film devices at room temperature. Nevertheless, for both devices, J_0 exceeds that of high-efficiency (η > 10%) CdTe/CdS cells by at least an order of magnitude[37]. Recent works on Si NW solar cells have highlighted the requirement to passivate surfaces of NWs with an intrinsic shell and to ultimately form *p-i-n* core-double shell devices as opposed to *p-n* devices, in order to reduce surface recombination[38-40].

7.6 Conclusions

In this Chapter the fabrication, characterisation and modelling of thin-film ITO/ZnO/CdS/CdTe/Mo solar cells and NW-based ITO/ZnO/CdS/CdTe(NW)/CdTe/Mo solar cells has been presented.

First, varying the post-growth treatment of thin-film substrate devices was shown to have a significant impact on their performance, with the best η having been obtained by adoption of a 'double-annealing' process. Here, the first annealing stage following $CdCl_2$ deposition onto CdTe layers was presumed to dope the CdTe and induce grain growth. The second annealing stage was shown (by SIMS analysis) to enhance S and Te inter-diffusion at the CdS/CdTe interface, this having the effect of improving V_{OC} and FF.

The principle limitation to all substrate devices was the rectifying back contact at the Mo/CdTe interface, this having been determined to be 0.52 eV by *J-V-T* measurements. A PV device having a significantly large back contact barrier may be electrically represented by a model that includes two opposing and independent diodes. In this model, the barrier is thought to be detrimental to FF and, in extreme cases, to V_{OC}. Indeed, the efficiency shortcomings of substrate devices relative to superstrate devices, for which Ohmic contacts were formed by etching of the back surface, resulted from relatively lower FF and V_{OC}, whereas the J_{SC} of the two devices were comparable.

It was found that the optimum CdTe thickness for substrate devices was 3 – 6 μm: Thinner absorber layers suffered from poor V_{OC}, this being attributed to overlapping of the depletion regions of the back contact and the main junction, and thicker absorber layers introduced high R_S which resulted in low FF. FIB-SEM images demonstrated that pin-holes exist within the CdS film, highlighting the requirement for an insulating ZnO layer to prevent the formation of poor ITO/CdTe diodes. From *J-V-T* measurements, it was found that at high T (> 270 K) charge transport was dominated by recombination in the depletion region and at low T (< 270 K), a tunnelling-assisted mechanism dominated.

Modelling of substrate devices using SCAPS confirmed that the efficiency shortcomings of devices reported here (η = 8.0%) compared to the best reported substrate devices on Mo foil (η = 11.5%) is largely attributable to their poor back contact. The best reported devices in the literature include a buffer layer between Mo and CdTe in order to form an Ohmic back contact, whereas those presented here have the highest reported efficiency of substrate devices that do not have such a buffer layer. Device modelling suggested that a suitable buffer layer to use in order to form an Ohmic contact would be highly *p*-doped and should possess a work function that exceeds that of Mo but is lower than that of CdTe.

The second half of the Chapter focussed on the performance of NW-based solar cells. Simulations of the η, J_{SC} and V_{OC} achievable in CdTe devices having either an array of radial *p-n* junctions or a single planar junction were carried out, with the impact of the depletion region width, W, and minority carrier diffusion length, L, on these parameters for both

junction morphologies being investigated. The model calculated the depth distribution of photo-generated carriers within the devices, and the proportion of these carriers that could be successfully collected. It was found that for devices with short L (< 0.7 μm) and narrow W (< 0.4 μm), the adoption of radial junctions could yield significant improvements to J_{SC} and η, whereas for longer L and wider W thin-film devices were not limited by carrier collection and the radial junction approach was deemed to be unnecessary (only in terms of carrier collection). In fact, in the latter case, vertical NW devices performed worse than thin-film devices due to transmission losses. Nevertheless, for all values of L, randomly oriented NW devices had higher η than thin-films due to increased light absorption, by a reduction of reflectance. The advantages of radial junctions are considered to be less pronounced in direct bad-gap semiconductor solar cells than in indirect band-gap semiconductor solar cells due to the smaller discrepancy between absorption length and carrier diffusion length.

Growth of completed CdTe NW based devices was demonstrated, these consisting of CdTe NW arrays on CdTe thin-films (the blocking layer) on Mo substrates, all coated with a triple-layer of ITO/ZnO/CdS. The highest efficiency achieved was η = 2.49%. The impact of the post-growth treatment on device performance was investigated, with the best performances having been achieved by devices for which the CdTe blocking layer and the NW array were each separately Cl-treated. *All* devices were annealed again following ITO/ZnO/CdS deposition since this step had already been shown to improve junction formation in thin-film devices. NW device efficiency was shown to be highly dependent on NW dimensions, the peak performance being obtained for NWs with l ~ 5 – 10 μm and D ~ 100 – 200 nm, whereas it was independent of blocking layer thickness.

NW devices were thought to be limited by the following: a) A Schottky barrier at the back contact; b) increased saturation current owing to the larger surface area of the junction relative to thin-films; c) shunting pathways that form as a result of the non-uniform coating of NW arrays with the shell layers; d) high R_S introduced by NWs that are too long; e) excessive blue absorption due to an increased volume of CdS relative to thin-films; and f) non-optimised NW dimensions. Some of these issues require confirmation by further studies, and solutions to *all* of these issues are subject to future work (see Chapter 8). The answer to the question of whether the NW array or the blocking layer is mainly responsible for the operation of the device is also subject to future work. Nevertheless, this work enables future progress on a new set of architectures for NW based core-shell PV devices having complete electrical continuity, this being the first demonstration of working CdS/CdTe(NW) PV devices.

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Chapter 8 : Conclusions and suggestions for further work

8.1 Main achievements of this research

The work presented in this thesis has focussed on the development of a novel configuration for CdTe PV devices. The design replaces the traditional planar *p-n* junction with an array of core-shell NW radial *p-n* junctions in order to ensure that all carriers are photo-generated close enough to the CdTe/CdS interface to be effectively collected, and to improve the absorbance of the active material. The target structure (presented in Chapter 1) requires the growth of electrically continuous CdTe NW/film structures on a conductive substrate to which a contact can be made to CdTe, and the subsequent coating of this structure with a CdS shell to form the radial *p-n* junctions, and an ITO shell to act as the transparent front contact. All aspects of the development of this design and the characterisation of the individual structures and full devices were explored in detail, the results having been presented as follows:

a) The growth of CdTe NWs on conductive Mo substrates (both directly and on polycrystalline CdTe films) using a Au-catalysed VLS mechanism was presented in Chapter 5, as was the coating of these structures with CdS and ITO shells.

b) An evaluation of the microstructure and point defects in CdTe NW and ITO/CdS/CdTe NWs using TEM and PL spectroscopy respectively was reported in Chapter 6 along with UV-VIS spectroscopy of NW arrays and electrical measurements of individual NWs.

c) In Chapter 7, the growth, optimisation and characterisation of planar CdTe devices on Mo foils, a necessary step towards understanding the optimal processing conditions for devices grown in the substrate configuration, was first reported. Having then applied this understanding to the processing of NW devices, characterisation and optimisation of preliminary NW devices was then presented.

Although the growth of planar devices was primarily driven by the requirement to understand contacting between CdTe and Mo, and to optimise post-growth treatment of CdTe structures in the substrate configuration, the high efficiencies obtained were competitive relative to other reported substrate devices (see Section 2.5.4). Consequently, the work presented in this thesis has resulted in the development of two promising device platforms for CdTe PV, each of which have great scope for improvement:

a) A peak efficiency of 8.0% was achieved for the substrate configuration ITO/ZnO/CdS/CdTe/Mo planar device, this compared to the current best of 11.5%[1] on Mo foils. Modelling suggested this discrepancy can be eradicated by improving the back contact.

b) A peak efficiency of 2.5% was achieved for the ITO/CdS/CdTe(NW)/CdTe/Mo core-shell NW device, this representing the highest efficiency that has been reported for a CdTe NW core-shell device. These NW devices are far from optimised in terms of structure dimensions, doping and contacting, but they serve as a proof of concept that has not been demonstrated before.

Moreover, a number of insights have been obtained through extensive NW growth and characterisation studies, the grown structures having been shown to be of high quality for PV applications. A full summary of conclusions for this work is given in the next section.

8.2 Summary of conclusions

In Chapter 5 the generation of Au nanodots on conductive Mo foils, necessary for VLS growth, by thermally induced de-wetting of Au films was first reported (a full investigation of the effects of annealing conditions on nanodot size and distribution being included in Appendix A). Nanodots, having diameters of 34 ± 4 nm and densities of (3 ± 1) x 10^9 cm^{-2} were formed by annealing 5 nm thick Au films on Mo foils at 360°C for 30 mins under 100 Torr of N_2.

Au-catalysed CdTe NW growth was achieved on Mo foils using CSS as the source of deposition flux (Section 5.2). For source and substrate temperatures of 550 and 520°C respectively, the generated NWs had radii in the range 50 – 500 nm, lengths of up to 20 µm and densities of 10^6 – 10^7 cm^{-2}. The presence of a semi-continuous film at the base of the NWs was also observed (upon studying the effect of varying the growth time it was deemed that this film forms during the early stages of growth). NWs appeared to have a random distribution of inclinations with respect to the substrate. At each NW tip a droplet was observed, which was found to be Au (of at least 2N purity) by EDX analysis. This observation, along with the rounded shape of the droplets and fast growth rates was consistent with growth being governed by the VLS mechanism. Since the NW length was inversely proportional to NW diameter, it was deemed that the primary contribution to growth was the diffusion of adatoms from the substrate to the catalyst.

A mechanism for VLS growth was proposed, with the formation of a CdTe-Au liquid alloy being ruled out on the basis that no such liquid phase could form at the growth temperature. Rather, it was argued that VLS growth was catalysed either by Au-Te or Au-Cd

liquid alloys. Owing to the observation that a $CdMoO_x$ phase forms at the initial stages of growth, and to thermodynamic considerations, growth was presumed to be catalysed by a Au-Te alloy. The observed delay to NW growth, and accompanying formation of a semi-continuous film in the early stages of growth (confirmed by time-dependent growth experiments), was consistent with the proposed mechanism whereby the pure Au droplet gradually becomes alloyed with arriving Te until the necessary liquid phase is acquired.

Varying the growth conditions was shown to have a significant effect on the morphology of the grown structures. For instance, NW growth was absent when using high N_2 pressures as the deposition flux was insufficient to saturate the droplets, whereas at low pressures, NW growth proceeded. Moreover, upon increasing the substrate temperature, NW aspect ratio increased and density decreased, and upon increasing source temperature, NW length increases. A diffusion induced model for VLS NW growth (described in Chapter 2) gave a good agreement to the experimental data for both the temperature dependence and time dependence of NW dimensions. The model generated useful quantitative data describing the growth mechanism; the diffusion length of adatoms on NW sidewalls was 2 μm and the probability that adatoms stick to the sidewalls was 0.61.

NW growth was also achieved on polycrystalline CdTe films (Section 5.3). Notably, greater NW densities could be achieved than for growth directly on Mo, and there was no delay to NW nucleation. This was attributed to the more ready acquisition of the necessary liquid catalyst on polycrystalline films on account of Te being supplied to the droplet both from the vapour and the substrate. Critically, this method ensures an electrically continuous NW/film structure – necessary for the desired device structure – and it allows control of the thickness of the planar layer at the base of the NWs. XRD measurements of CdTe NWs showed that the NW arrays were less preferentially oriented than both as-grown and annealed CdTe substrates.

An evaluation of three separate methods – CBD, MOCVD and RF sputtering – for coating the CdTe NWs with conformal sulphide shells was reported in Section 5.4. CBD caused the collapse of NWs whilst MOCVD resulted in highly directional dendritic shell morphologies that did not conform around the wires. Sputtering was deemed to be the most suitable method since it did not cause any mechanical damage to the NWs and generated relatively conformal coatings, although the uniformity of the thickness of the shells varied. ITO shell layers were also sputter grown, resulting in core-double shell ITO/CdS/CdTe NW structures.

Chapter 6 reported characterisation of the NW structures and an evaluation of their potential for use in PV applications was presented. TEM characterisation demonstrated that

the microstructure of CdTe NWs was dependent on their growth axes only, but independent of post-growth annealing procedures. Stacking faults, polytypes and twins were observed in most NWs, although some were free of any extended defects. Three growth axes were identified, these being <110>, <111> and <112>, the extent of planar defects being greatest for <112> NWs. Since these defects are considered to be electrically inactive in CdTe, their presence is not deemed to be detrimental in terms of PV applications. The cross sectional geometry of NWs was also studied, <111> NWs adopting a hexagonal shape and <112> NWs adopting a rectangular shape. Wulff constructions were consistent with the former but not the latter. Notably, sputter deposited CdS was observed to grow epitaxially on the CdTe NWs, the expected reduction of surface recombination that may be associated with this being highly desirable for PV applications.

Low temperature PL of isolated CdTe NWs showed strong near-band edge features and weak DAP luminescence that is characteristic of highly pure samples (Section 6.3). Moreover, the fine structure observed in the spectra is characteristic of single crystal material, in contrast to the degraded broad spectral features observed for polycrystalline films. Annealing the NWs under N_2 at 400°C further improved the near-band edge response and resulted in the observation of above-gap luminescence. For these samples and as-grown samples, the intense phonon replica features (both for excitonic and DAP emission) indicate strong electron phonon coupling, with Huang-Rhys coupling parameters being as high as S = 2.5. The most dominant spectral feature was that attributed to the acceptor-bound exciton, this acceptor level being introduced either by Ag, Cu or Na impurities. Although Au impurities may be expected in these NWs, only a weak deep emission at ~ 1.27 eV could be attributed to Au. Annealing of the NWs in a reducing atmosphere at 400°C or in N_2 at higher temperatures (500°C) resulted in a quenching of the excitonic emission relative to the DAP band, implying the creation of new point defects, and annealing in the presence of O_2 caused degradation of the spectra. Ultimately, it was concluded that provided optimal post-growth treatment is applied, these NWs are of significantly high crystal quality. This was further demonstrated using time-resolved PL measurements, which yielded exciton lifetimes (up to 2 ns) that are some of the longest ever seen in non-quantum scale CdTe. Binding energies of excitons (3 – 5 meV and 12 - 34 meV) donor levels (2.8 meV) and acceptor levels (160 meV) were determined from temperature dependent PL measurements.

In Section 6.4, PL spectroscopy of CdS/CdTe core-shell NWs was reported. In as-grown samples, strong near-band edge CdS luminescence was observed at 2.4 – 2.6 eV, along with CdTe luminescence at 1.4 – 1.6 eV and a broad intermediate band. Upon annealing at 400°C

in N_2, the CdS and CdTe luminescence was quenched and the broad band was enhanced, this being tentatively attributed to enhanced inter-diffusion at the CdS/CdTe interface.

UV-VIS spectrophotometry demonstrated that the above-gap reflectance of NW arrays (~ 0.1%) was significantly lower than for planar films (~ 10%) - the transmittance was also lower in NW arrays. Transmittance measurements failed to accurately determine the optical band-gap of the CdTe NWs. Resistivity measurements of individual CdTe NWs proved unsuccessful owing to the failure of forming an Ohmic contact, whereas measurements of the CdS shell were more successful, the resistivity being $\rho = 0.7 \pm 0.4$ Ω.cm, assuming the shell has a cylindrical shape.

In Chapter 7 the fabrication, characterisation and modelling of thin-film and NW solar cells was presented. First, in-depth optimisation studies were first conducted for the planar devices (Section 7.2). Upon investigating a variety of post-growth treatment procedures, it was demonstrated that the use of a double-annealing process was most effective in terms of yielding high performance. This process involved a Cl-treatment to the CdTe layer at 420°C and a Cl-free treatment after the growth of all layers at 560°C. The inclusion of the second treatment stage increased efficiency from 1.96% to 6.05%. This was attributed to enhanced inter-diffusion at the CdS/CdTe interface based on SIMS results and the increased V_{OC} and FF. For all devices, a poor back contact was seen to be severely limiting, reducing FF in particular and also V_{OC}. The height of the Schottky barrier determined to be 0.52 eV by *J-V-T* measurements. Indeed, the efficiency loss compared to superstrate cells was attributed to the poor contact. The optimum CdTe thickness was 3 – 6 μm, with thinner devices having low V_{OC} due to overlapping of the main junction and back contact depletion regions, and thicker devices being limited by increased R_S. Whilst FIB-SEM images revealed that the CdTe grains were large (> 4 μm wide and extending the thickness of the film) as desired, it also showed that pinholes exist in the CdS layer. This highlighted the requirement for a highly resistive and transparent (HRT) ZnO layer to prevent the formation of weak CdTe/ITO diodes, and indeed device efficiency was increased from 6.05% to 8.01% by inclusion of such a layer, the increase to V_{OC} being consistent with a reduction of the effect of pinholes. From *J-V-T* measurements, it was inferred that charge transport is dominated by recombination at high temperatures (> 270 K) and tunnelling at low temperatures (< 270 K).

Modelling of substrate devices using SCAPS implied that the best obtained efficiency of 8.01% could be increased to 11.3% upon successful formation of an Ohmic back contact. It was demonstrated that a quasi-Ohmic contact could be achieved by inclusion of a buffer layer, between CdTe and Mo, that was either highly *p*-doped or have an optimised work function.

A separate model was developed to simulate the device performance parameters of traditional thin-film devices with single planar junctions and of NW devices with arrays of radial junctions (Section 7.4). For devices with short L (< 0.7 μm) and narrow W (< 0.4 μm), it was demonstrated that the NW devices more effectively collected photo-generated carriers than the thin film devices, and therefore yielded higher J_{SC} and η, whereas for longer L and wider W, there was no difference in collection efficiency between the two configurations. Randomly oriented NW arrays generated higher J_{SC} than vertical NW arrays and thin-films owing to their reduced reflectance. V_{OC} was predicted to be lower in NW devices upon assuming that the reverse saturation current scales with junction area, although the losses were minimal compared to the potential J_{SC} gains.

In Section 6.5, the growth and characterisation of ITO/ZnO/CdS/CdTe(NW)/CdTe/Mo NW core-triple shell NW devices was reported, the ZnO layer having been included on the basis of the efficiency enhancements it yielded for thin film devices. Upon investigating a number of post-growth processes, it was found that the highest efficiencies were achieved by using three annealing stages, these being: a) Cl-treatment at 420°C after CdTe film deposition; b) Cl-treatment at 420°C after CdTe NW deposition; and c) a Cl-free treatment at 500°C after the growth of all other shell layers. NW device efficiency was shown to be highly dependent on NW dimensions, the peak performance of 2.49% being obtained for NWs with l ~ 5 – 10 μm and D ~ 100 – 200 nm, whereas it was independent of blocking layer thickness. NW devices were thought to be limited by the poor back contact, increased reverse saturation current, shunting pathways, high R_S and excessive blue absorption, therefore there remains much scope for improvement. Questions arise as to whether the CdTe NW array or underlying CdTe blocking layer was responsible for device operation and this is subject to future work (see Section 8.3).

8.3 Future work

Further opportunities for ongoing work are now described.

8.3.1 CdTe nanowire and CdS/CdTe core-shell nanowire growth

- One of the main concerns of metal-catalysed VLS growth is the potential incorporation of impurities in the NW which may act as deep recombination centres in optoelectronic devices. As has been shown for other systems (e.g. GaAs[2]), it is possible to self-catalyse VLS growth therefore CdTe NWs of higher quality may be

achieved be they catalysed by Cd or Te droplets. Alternatively, metals that may be less electrically active than Au could be used, such as Bi.

- Although the systematic studies investigating the effect of growth conditions on NW morphology yielded a number of insights for growth directly on Mo, these experiments should also be replicated on polycrystalline films. Given the more ready nucleation of NW growth on pre-deposited films, analysis of these results would not have to account for the complexities of nucleation delay that is experienced for direct growth on Mo.
- For core-shell NW solar cells, it is generally considered that the optimum NW diameter is equivalent to the minority carrier diffusion length, which is typically in the region 0.2 – 1.0 µm in CdTe. However, NW growth experiments presented in Chapter 5 showed that NWs having diameter in the range 5 – 500 nm were achieved. Preliminary experiments designed to yield NWs of greater diameter were unsuccessful due the catalyst becoming unstable during growth. This should be subject to further investigation.
- Since results in Chapter 7 showed that the core-shell device configuration reduces the constraints on material quality it may be presumed that the structures used need not be monocrystalline or of high purity. Indeed, control of NW size and spacing is likely to be more critical in terms of optimising device efficiency as opposed to ensuring long minority carrier diffusion lengths. For a higher level of dimension control, NWs could be generated by templated-growth using, for instance, anodic alumina membranes.
- The use of atomic layer deposition to generate highly conformal CdS and ITO coatings should be investigated, this growth technique providing an unrivalled level of thickness control.

8.3.2 CdTe nanowire and CdS/CdTe core-shell nanowire characterisation

- Microstructure of CdTe NWs was analysed for just 20 individual NWs in this work. A much larger sample set is required to fully investigate this subject: <110>, <111> and <112> NWs were studied, but no <100> NWs were observed despite this often being the case in other systems (e.g Si[3] and InP[4])
- Ongoing cathodoluminescence (CL) spectroscopy measurements are being carried out to compliment PL results. The CL technique has poorer spectral resolution than PL but enhanced spatial resolution therefore can identify non-uniformities throughout the NWs.

- Since electrical measurements of individual CdTe NWs proved unsuccessful, two modifications to the measurements are suggested. Firstly, by coating the tungsten STM probes with a metal of higher work function, Ohmic contacts may be acquired. Secondly, by FIB-milling a region of a CdS/CdTe core-shell NW to partially remove the CdS shell, contacts could be made either side of the core-shell junction and dark *J-V* curves could be taken. A rectifying curve with strong rollover would be expected (owing to the poor CdTe/probe contact) but this should be verified.

8.3.3 CdTe thin-film and nanowire solar cells on Mo foils

- The rectifying back contact is the most limiting factor for both platform devices therefore it is paramount for suitable buffer layer materials to be investigated.
- To investigate whether the NWs or the underlying blocking layer contributes most to NW device operation, two studies could be carried out. Firstly, electron beam induced current measurements would directly show the regions from which current is generated. Secondly, an alternative device design that does not include the blocking layer, but instead uses an insulating in-fill to provide electrical continuity, would demonstrate whether the NWs are truly photoactive.

References for Chapter 8

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Appendix A: Preparation of Au nanodot arrays

A.1 Introduction

Here, a preliminary study of the formation of Au nanodot arrays is reported, this being achieved by annealing thin Au films (which had been evaporated onto Si and Mo substrates) to induce de-wetting. This study provides the necessary insights for the development of an appropriate procedure for preparing Au catalysts for the NW growth experiments reported in Chapter 5. Although such studies have been reported before, it was necessary to establish suitable annealing conditions for nanodot generation in our system. Moreover, as the diameter and distribution of VLS-grown NWs is dependent upon that of the catalyst particles, the effect of the annealing conditions and initial film thickness on Au nanodot size and density was investigated. Before experimental results are presented and discussed (Sections A.3 – A.5), a brief literature review of the de-wetting mechanism is given in Section A.2.

A.2 Review of de-wetting mechanism

The generation of metal nanodot arrays by the thermal annealing of thin metal films is a well-established technique[1-5], used for both catalysing NW growth and work on surface plasmons[6-8]. Similar methods have been used to form Co[9], Ni[10], Ag[11] and Si[12] nanoparticles. The method is simple but there is less control over size and position of the nanodots than may be achieved for top-down techniques. Nevertheless, some control can be obtained through consideration of the de-wetting mechanism, this now being briefly discussed.

The break-up of a film into islands of material upon annealing is a thermally induced mechanism[3], with the reduction of the film-substrate interfacial area lowering the free energy of the system. Kwon[3] demonstrated the different stages of a Au film breaking up by increasing anneal time or temperature (the results being equivalent). He explained that initially vacancies in the film cluster together to nucleate voids which grow and eventually perforate the film, therefore creating holes. These holes grow (by surface diffusion) in a fractal form isolating islands of material which eventually adopt a spherical cap shape with a contact angle defined by Equation 3.1. Kane[1] demonstrated the same process by utilising films of different thicknesses to represent the different stages, the thinner films being broken up to a greater extent after the same annealing time.

After continued annealing, coalescence of nanodots may occur, further reducing the film-substrate interfacial area and therefore the system's free energy. Coalescence in this case requires motion[13, 14] of either solid or liquid nanodots, a phenomenon also known in the case of film growth[15]. For the coalesce of two solid nanodots, coalescence may be complete if the nanodots go through a temporary liquid-like phase[16] (achievable due to energy released during the event), or incomplete if they do not.

A.3 Experimental procedure

15 mm x 15 mm substrates were cut from 380 µm Si ⟨111⟩ wafers and 100 µm thick Mo foil. They were cleaned ultrasonically and rinsed with de-ionised water, and dried with a N_2 gun. Following deposition of thin films (2 – 10 nm) of Au by thermal evaporation, samples were transferred into the CSS chamber (described in Section 4.2.1). Both upper and lower heaters of the system were used to achieve a uniform heat distribution for annealing. The Au films were annealed at temperatures of 300 – 500°C, under static N_2 pressures of 50 – 200 Torr, for 10 - 60 minutes.

Plan view SEM images of each sample were recorded in the secondary electron imaging mode. The average diameter, density and surface coverage of Au was measured using the *Image Tool*^{TM} image analysis software, with averages taken from three different regions of each sample.

A.4 Results

Results of the annealing of 5 nm thick Au films on Si substrates for 30 mins under 50 - 200 Torr of nitrogen, in the range 300 - 500°C are shown in Fig A.1 and Fig A.2. Fig A.1 shows the morphology of films processed under 100 Torr of N_2 at 300, 375 and 475°C. Fig A.2a shows the variation of the average feature diameter with annealing temperature for pressures of 50, 100 and 200 Torr. Fig A.2b shows the variation of surface coverage with annealing temperature for the set processed under 100 Torr.

Firstly, the results for the set of films annealed under 100 Torr are described. The SEM images show a progression in the development of morphology with increasing annealing temperature: At lower temperatures in the range, the film break up is incomplete and yields both islands and ribbons of material. As the temperature is increased, the degree of film break-up is increased and the average feature size reaches a minimum at 375°C. At this point the resulting nanodots are all roughly circular in shape, having a Gaussian distribution of diameters with an average of 24 ± 2 nm. Here the density is at a maximum of

(4 ± 1) x 10^9 cm^{-3}. Annealing at higher temperatures increased the average particle size and decreased the density, the values being 45 ± 3 nm and (2 ± 1) x10^9 cm^{-3} for the film annealed at 475°C and shown in Fig A.1c. As temperature was raised throughout the whole range studied, there was a linear decrease in the surface coverage, as shown in Fig A.2b.

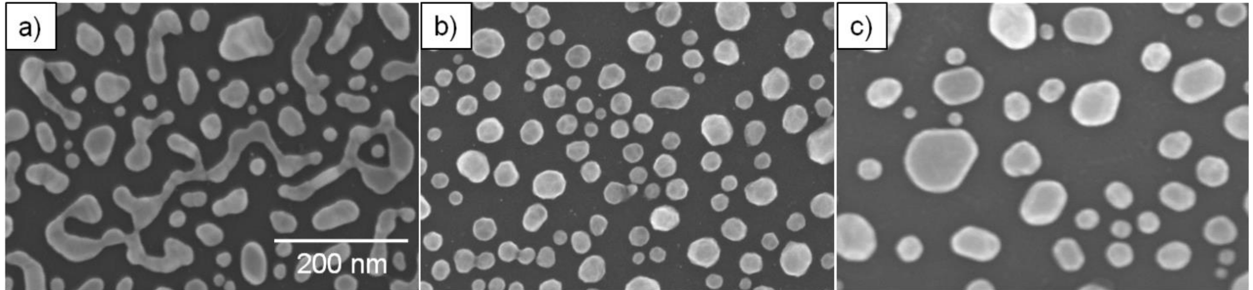

Fig A.1: Plan view SEM images of 5 nm thick films of Au/Si that had been subjected to annealing for 30 mins under 100 Torr of nitrogen at a) 300°C, b) 375°C and c) 475°C. Increasing the temperature at first encourages the formation of smaller particles and then their agglomeration into larger bodies. See Fig A.2 and text.

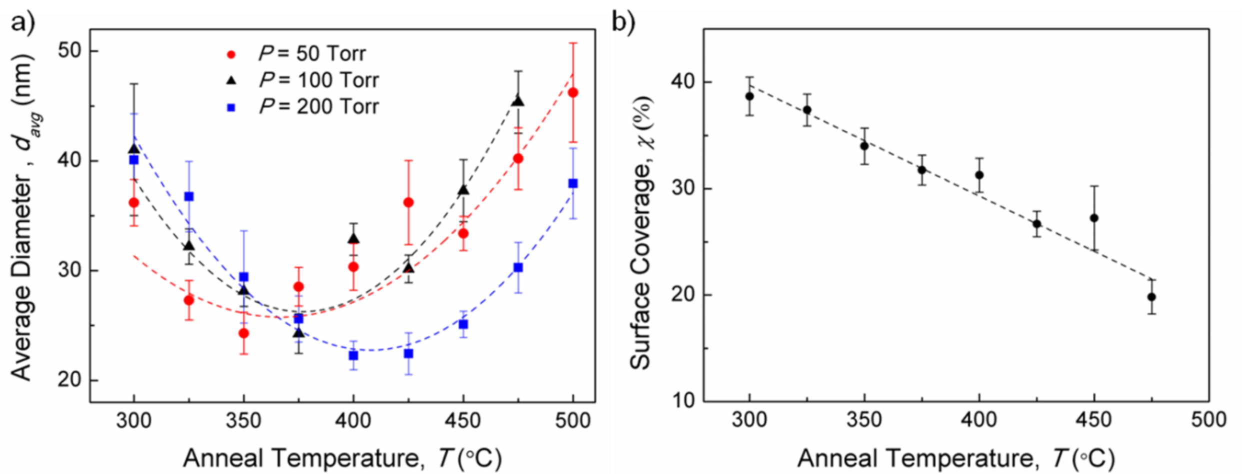

Fig A.2: a) Variation in particle size with annealing temperature for 5 nm thick Au/Si films annealed for 30 mins under 50 Torr (red circles), 100 Torr (black triangles) and 200 Torr (blue squares). b) Variation in surface coverage for 5 nm Au/Si films annealed for 30 mins under 100 Torr. See Fig 5.2 and text. Lines are added as a guide to the eye.

A similar trend, described above for the films annealed under 100 Torr, was achieved for the films annealed at 50 and 200 Torr, with the most significant difference being the temperature at which the minimum average feature size was obtained. At 50 Torr, the minimum diameter of nanodots was found to be 24 ± 3 nm at 350°C, whilst at 200 Torr, it was 22 ± 2 nm at 400°C, i.e. the minimum was at lower temperatures for lower annealing pressures.

The morphological development with time (10 – 60 mins) was also studied by SEM for films annealed under 100 Torr at 400°C. Feature development similar to that in the temperature series shown in Fig A.1 - A.3 was observed: The film break up was incomplete after 10 minutes, a minimum nanodot diameter of 22 ± 4 nm was achieved after 30 minutes, and an increase in nanodot diameter with annealing time was observed over the range 30 – 60 minutes.

Fig A.3 shows the results of annealing films of different thickness (2 – 10 nm) under 100 Torr, for 30 mins at 400°C. The average Au nanodot diameter increases with film thickness, from 17 ± 7 nm for a 2 nm thick film, to 130 ± 19 nm for a 10 nm thick film. In the same range, the density decreases from ~ 10^{10} to ~ 10^{8} cm^{-2}. Evidently, by varying the initial film thickness, a much wider range of achievable diameters was obtained (17 – 130 nm) than for the entire parameter space of anneal temperature, pressure and time that was investigated here (~ 20 - 50 nm).

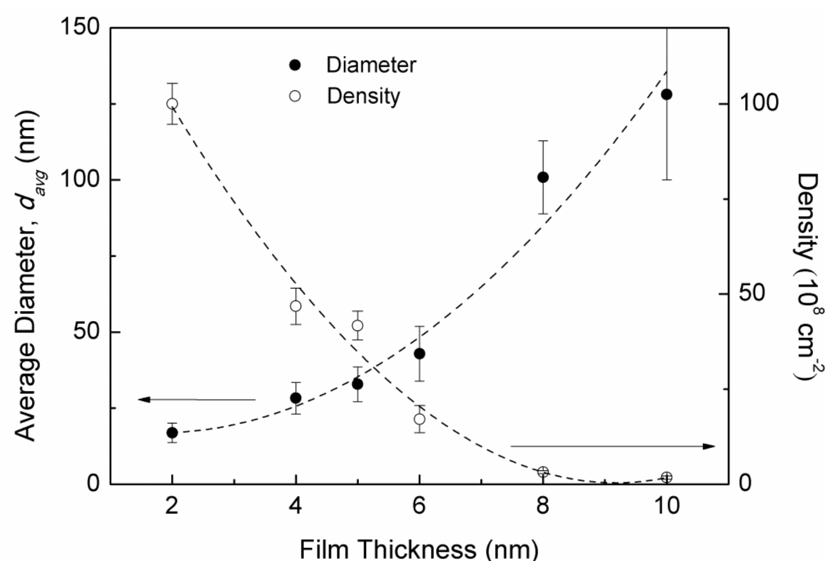

Fig A.3: Variation of the average nanodot diameter and density with the initial thickness of the deposited Au film, for Au/Si films annealed at 400°C, for 30 mins, under 100 Torr.

Fig A.4 shows the temperature dependence of the average feature diameter upon annealing Au films on Mo substrates for 30 mins, under 100 Torr at temperatures in the range 300 - 480°C. The trend is similar to that observed for films annealed on Si: a) In the range 300 - 375°C, the average diameter decreases with increased temperature; b) a minimum diameter of 34 ± 3 nm was achieved at 375°C; and c) in the higher temperature range (375 - 475°C), the average diameter increases with temperature, to 56 ± 5 nm at 475°C. Nevertheless, for the same annealing conditions, the nanodot diameters yielded on Mo substrates (34 – 56 nm) were larger than those on Si (24 – 45 nm).

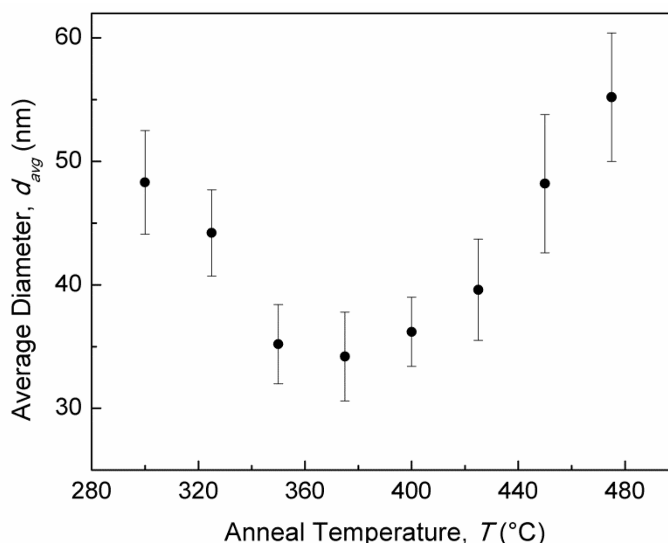

Fig A.4: Variation in particle size with annealing temperature for 5 nm thick Au/Mo films annealed at 300 - 475°C, for 30 mins, under 100 Torr. Lines are added as a guide to the eye.

A.5 Discussion

The mechanism of the de-wetting of a film is described in Section A.2. It is a thermally activated process that acts to lower the free energy of a system. In the results presented here, this process is incomplete when low annealing temperatures (e.g. 300°C, shown in Fig A.1a), or short anneal times (e.g. 10 mins) were used. However at higher anneal temperatures (e.g. 375°C, shown in Fig A.1b) or longer anneal times (e.g. 30 mins) de-wetting of the film is complete. Indeed there are many similarities between the development of both morphology and diameter with time and temperature, this being consistent with the progress of a thermally activated progression towards an equilibrium state.

For the case of Au on Si substrates it is also necessary to consider interactions between the two elements. The eutectic temperature of the Au-Si binary system (363°C) corresponds roughly with the temperature at which the minimum diameter was achieved for all sets of films (350 - 400°C, under 50 – 200 Torr of N_2). This appears to support a model of film break up that involves the eutectic phase. However, the Au-Mo system has a eutectic far exceeding the temperature range used here[17] and yet a very similar correlation between nanodot diameter and annealing temperature was observed, with the minimum being achieved at 375°C. At this temperature, the Au islands on Mo must be solid. (Melting point depression for 20 nm Au particles has been shown to be slight, with the reduction being to approximately 1000°C from the bulk value of 1063°C). Whilst the author recognises that Au-Si eutectic formation may be important in the case of Au on Si, most of the work that followed (Chapters 5 – 7) was for the Au on Mo system, and since there were considerable similarities in the evolution of nanodots

from Au films on both substrates, a detailed investigation of the Au-Si system was deemed unnecessary in this work.

The increase of nanodot diameter with higher temperatures and longer annealing times is a result of nanodot coalescence. Coalescence may occur both for liquid and solid islands and Pocza *et al.*[18], for example, report that when solid islands coalesce, they can behave as two liquid droplets that merge together before recrystallising. Throughout the temperature range studied, the surface coverage of Au/Si films decreased linearly with annealing temperature, this being consistent with the de-wetting process being driven by a reduction of the film-substrate interfacial area. Surface coverage is lower following nanodot coalescence because, for a given coalescence event, the surface-to-volume ratio of the resultant larger nanodot is lower than the combined surface-to-volume ratio of the two initial smaller nanodots. The shape of a nanodot modelled as a spherical cap (the spherical cap model being valid be the islands of liquid *or* of solid phase[3, 18]) is defined by its aspect ratio (height/diameter) which is defined by its contact angle. As the contact angle is only dependent on the vapour-substrate, nanodot-substrate and vapour-nanodot surface energies (Equation 3.2, Chapter 3), it is independent of nanodot diameter.

Notably, the complete break-up of the film was achieved more readily when a lower nitrogen pressure was used, i.e. when lower pressures were used, the minimum average nanodot diameter was achieved at lower annealing temperatures (Fig A.2a). As the contact angle is dependent on vapour-substrate and vapour-nanodot surface energies, it is dependent on the ambient pressure of the vapour surrounding the nanodot. Siemons *et al.*[19] report that under lower ambient pressures, the contact angle of a droplet on a substrate is smaller. Bearing in mind that the mechanism of film break-up involves the de-wetting of a film (contact angle = 0°) to an array of nanodots (contact angle = θ), this process is more readily achievable if the eventual contact angle, θ, is smaller, i.e. it is encouraged by lower pressure.

The parameter that had the greatest influence on nanodot diameter was that of the initial film thickness. Whereas the entire parameter space of temperature, time and pressure only yielded a diameter range of ~ 20 – 50 nm, by increasing the film thickness from 2 – 10 nm, a diameter increase from 17 – 130 nm was achieved. Depositing thicker films yields nanodots of greater diameter simply because their volume is greater whilst their aspect ratio is the same as those generated by thinner films. In practical terms, adjustment of the Au layer thickness provides a convenient means to tune the Au nanodot size for use in NW growth experiments.

In conclusion, studies of nanodot formation on the model system of Au on Si have given considerable insight into the conditions that generate nanodots having morphologies and sizes

that are appropriate for the formation of NWs by VLS growth. Moreover, there were similarities between the behaviour of Au on Si and on Mo substrates. While the mechanisms on Au/Si might be expected to be influenced by eutectic phases, the study in this section provided enough process knowledge for the generation of the Au nanodots on conductive Mo substrates that are necessary for the NW and core-shell NW device structures that are reported in Chapter 5.

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Appendix B: List of publications

Publications of work included in this thesis:

1. **B. L. Williams**, D. P. Halliday, B. Mendis and K. Durose. 'Microstructure and Point Defects in CdTe Nanowires for Photovoltaic Applications', Nanotechnology **24** 135703 (2013)

2. **B. L. Williams**, B. G. Mendis, L. Bowen, D. P. Halliday and K. Durose. 'Vapor-Liquid-Solid Growth of Cadmium Telluride Nanowires by Close-Space-Sublimation for Photovoltaic Applications' MRS Proceedings 1350, mrss11-1350-ee06-25 doi:10.1557/opl.2011.872 (Poster accompanying manuscript, San Francisco, 2011)

3. **B. L. Williams**, B. G. Mendis, A. A. Taylor, L. Bowen, L. Phillips and K. Durose. 'CdTe Nanowire and Core-Triple Shell Structures for Solar Cell Architectures', submitted to Applied Physics Letters, *in press*

4. **B. L. Williams**, J. D. Major, L. Bowen, L. Phillips, G. Zoppi, I. Forbes and K. Durose. 'Challenges and Prospects for Developing Lightweight CdTe Solar Cells on Flexible Molybdenum Substrates', submitted to Solar Energy Materials and Solar Cells, *in press*

5. **B. L. Williams**, J. D. Major, R. E. Treharne, L. Phillips and K. Durose. 'Nanowire and Substrate Geometry CdTe Structures for Flexible PV Devices', MRS Proceedings (Oral presentation accompanying manuscript, San Francisco 2012)

6. **B. L. Williams** and K. Durose. 'Nanowire and Core-Shell Structures on Flexible Mo Foil for CdTe Solar Cell Applications', PVSAT Proceedings (Poster presentation accompanying manuscript, Edinburgh, 2011)

7. V. G. Dubrovskii, A. D. Bolshakov, **B. L. Williams** and K. Durose. 'Growth Modelling of CdTe Nanowires', Nanotechnology **23** 485607 (2012)

8. D. P. Halliday, **B. L. Williams** and K. Durose. 'CdTe/CdS Core-Shell Nanowire Structures on Glass Substrates for Photovoltaic Applications - Growth and Characterisation', 37th IEEE PVSC Proceedings p234-238 (Seattle, 2011)

Other publications by the author:

1. **B. L. Williams**, R. E. Treharne and K. Durose. 'All-Sputtered Solar Cells', PVSAT Proceedings (Poster presentation accompanying manuscript: Commendation received, Southampton, 2010)

2. R. E. Treharne, **B. L. Williams**, L. Bowen, B. Mendis and K. Durose. 'Investigation of post deposition $CdCl_2$ treatment for fully sputtered CdTe/CdS thin film solar cells', 38th IEEE PVSC Proceedings p1983-1987 (Austin, 2012)

3. J. D. Major, R. E. Treharne, Y. Y. Proskuryakov, **B. L. Williams** and K. Durose. '13.6% CSS-Sputtered CdTe Solar Cells on Soda Lime Glass', PVSAT Proceedings (Won best paper prize, Edinburgh, 2011)

Manuscripts in preparation:

1. **B. L. Williams**, A. A.Taylor, T. Pennycook, B. Mendis and K. Durose. ‘Investigating the Sub-Eutectic Vapour-Liquid-Solid Growth Mechanism for the CdTe-Au system’

2. R. E. Treharne, **B. L. Williams**, K. Durose, L. Bowen and B. G. Mendis. 'Investigation of the Distribution in Performance of Fully Sputtered CdTe/CdS Thin-Film Solar Cells'

3. A. A. Taylor, **B. L. Williams**, B. G. Mendis and K. Durose. 'TEM Characaterisation of the CdS/CdTe Interface in Core-Shell NWs for Solar Cells'