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Simultaneous Tuneable Selection and Self-Assembly of Si Nanowires from Heterogeneous Feedstock

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ABSTRACT

Semiconducting nanowires (NWs) are becoming essential nano-building blocks for advanced devices from sensors to energy harvesters, however their full technology penetration requires large scale materials synthesis together with efficient NW assembly methods. We demonstrate a scalable one-step solution process for the direct selection, collection and ordered assembly of silicon NWs with desired electrical properties from a poly-disperse collection of NWs obtained from a Supercritical Fluid-Liquid-Solid growth process. Dielectrophoresis (DEP) combined with impedance spectroscopy provides a selection mechanism at high signal frequencies (>500 kHz) to isolate NWs with the highest conductivity and lowest defect density. The technique allows simultaneous control of five key parameters in NW assembly: selection of electrical properties, control of NW length, placement in pre-defined electrode areas, highly preferential orientation along the device channel and control of NWs deposition density from few to hundreds per device. Direct correlation between DEP signal frequency and deposited NWs conductivity is confirmed by field-effect transistor and conducting-AFM data. Fabricated NW transistor devices demonstrate excellent performance with up to 1.6 mA current, 10^6-10^7 on/off ratio and hole-mobility of 50 $cm^2\ V^{-1}\ s^{-1}$.

KEYWORDS. Dielectrophoresis, Clausius-Mossotti factor, Silicon Nanowires, Nanowire Conductivity, Nanowire Field-Effect Transistors, self-assembly, selection

Single-crystalline silicon (Si) nanowires (NWs) are attractive semiconducting components for solution-processed, low-cost printed electronic devices. The NWs' unique characteristics, such as the single-crystalline structure, high charge-carrier mobility, high surface-to-volume ratio, surface chemistry compatible with various functionalization processes to bind receptors

for chemical/biological sensing applications and their ability to be solution-processed and assembled from ”semiconducting inks” using various alignment techniques, make them potential key building blocks for the manufacturing of chemical and biological sensors,[1-3] high performance field-effect transistors (FETs),[4-6] optical devices,[7, 8] memory elements[9-11] and energy harvesting.[12, 13]

The availability of high quality semiconducting NWs in scalable quantities remains one of the main challenges for NW-based printed electronics. The Supercritical Fluid-Liquid-Solid (SFLS) is one of the most promising NW growth techniques, which can realistically provide the large quantities of NWs for industrial applications with an achievable throughput of a few kilograms of NW materials per day.[14] However, one disadvantage of the SFLS technique is the limited control of NW morphological parameters resulting in a synthesis of poly-disperse NWs with various lengths and diameters, as well as non-straight (*i.e.* kinked) NWs[14] (Figure 1 (a) and Supporting Information, Figure S1 (a, b, g)). The occasional NW growth with different crystallographic directions and the presence of crystal structure defects add another degree of imperfection to NWs, which can all affect the reproducible fabrication and performance characteristics of NW based devices. Finding a one-step processing technique that provides purification, selection and alignment of NWs on the desired substrate areas underpinned by an industry-scalable NW growth methods will open prospects for the efficient large-scale fabrication of low cost, high performance solution processed NW electronics.

Despite the significant progress in semiconducting NWs assembly demonstrated with Langmuir Blodgett (LB),[15] Blown-Bubble films,[16] flow-directed assembly,[17] electrostatic interactions[18] and mechanical shear forces[19] techniques, the selective deposition of NWs based on morphological or electrical properties remained mainly unexplored, and NWs are typically deposited as-synthesised. Moreover, precise deposition of NWs with respect to

device electrodes remains very challenging, and additional fabrication efforts are required, for example, to guide NWs through microfluidic channels to deposit across the device electrodes,[17] still with no control of the NWs lateral alignment. Recent progress in dielectrophoresis (DEP) alignment and deposition of NWs has demonstrated both large-area compatible processing and high accuracy isolated nanowires placement associated with the strongest DEP force exerted on the NW in the vicinity of the electrodes.[20-22] During a DEP process, a polarisable nano-object is subjected to a non-uniform alternating electric field and its charges separate and accumulate at the surface, forming a dipole,[23] which experiences the force dependant of the gradient of the electric field resulting in NWs self-assembly across the electrode gap. Opoku[24] argued that DEP deposition helps to extract the NWs with lengths comparable to transistor channel length from a poor-quality ZnO NW powders, and Collet[20] have demonstrated preferential deposition of either Si or InAs NWs from a mixed NWs formulation by using various DEP signal frequencies. The selection capabilities of DEP, applied to single-wall carbon nanotubes (SWCNTs), have been shown by Krupke *et al.,*[25, 26] who used DEP to separate metallic and semiconducting SWCNTs by taking into account the difference of the relative dielectric constants of the two species with respect to the solvent at various frequencies.

In this work, we report the demonstration of direct selection of high quality Si NWs within a heterogeneous as-grown SFLS nanowires with various levels of conductivity and crystalline quality. The nanowires assembly is based on the dielectrophoretic process coupled with impedance spectroscopy analysis of real-time NW collection rate at various signal frequencies, and is also assisted by a nanowire dispersion flow. The method provides a one-step assembly of nanomaterials, simultaneously achieving the following: NWs' alignment on pre-defined electrodes, selection based on their electrical conductivity, orientation perpendicular to the electrodes edges, selectivity of NW lengths relative to the device channel

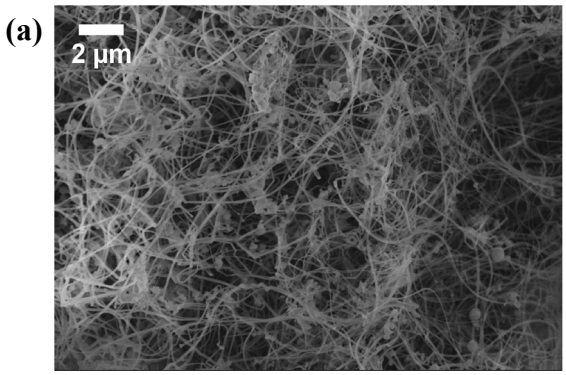
length and controllable density of deposited NWs between the electrodes.[27] The direct correlation between DEP signal frequency and deposited NWs conductivity was confirmed by FET and conducting-AFM data. The DEP-processed Si NWs FETs fabricated in this work also demonstrated high mobility values, currently being 50 times higher than the mobilities reported for the a-Si TFT backplanes used for driving active matrix organic light-emitting diode displays (AMOLEDs).[28, 29]

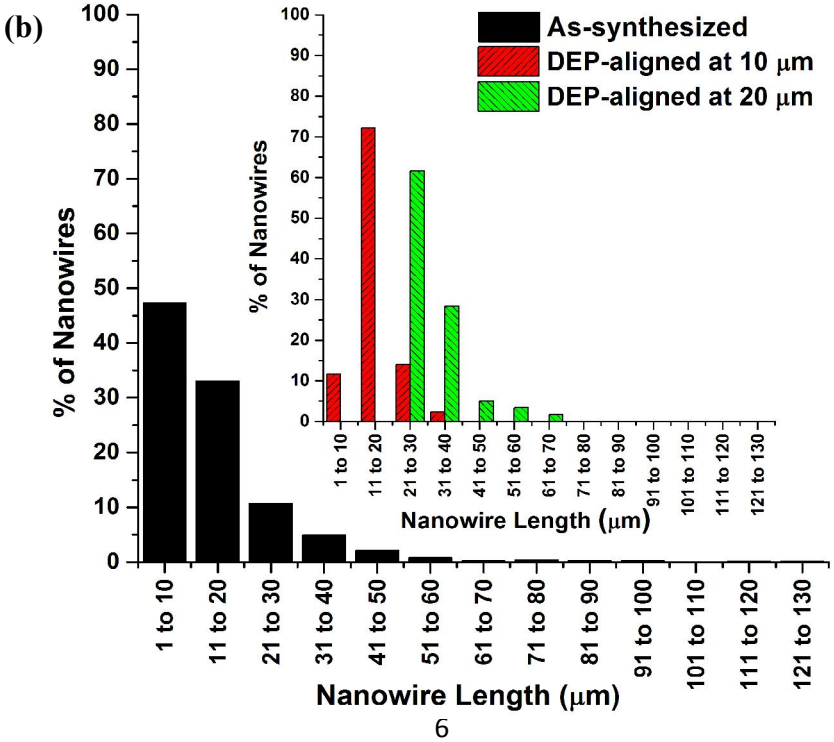
Results/Discussion

Si NWs used in this work were synthesised by the SFLS method using monophenylsilane (MPS) and Au seed nanoparticles mixed in toluene as the precursor solution and then heated and pressurised to supercritical conditions for the reaction.[14, 30] The NWs were not intentionally doped during the growth. For the preparation of the NW formulations, the as-synthesised Si NWs were dispersed in toluene and *N, N* - Dimethylformamide (DMF) in a ratio of 1:50 (see Methods: Materials, chemicals). NW dispersion was maintained, by brief sonication (~10-20 seconds) at low power (~200 W) prior to each DEP deposition and impedance analysis and FET device fabrication. Dispersions of NWs were further diluted to obtain an empirically optimal concentration (~1 μg/mL) for DEP processing. Samples for optical microscopy, scanning electron microscopy (SEM) and transmission electron microscopy (TEM) were prepared by drop-casting NW dispersions on Si/SiO_2 substrates and carbon grids (Agar Scientific).

Preferential NW growth direction was identified from high resolution TEM images and computed Fast Fourier Transform (FFT) patterns obtained from the lattice fringes to be along [111] direction (Supporting Information (SI), Figure S1 (e, f)), which is consistent with previous reports for SFLS Si NWs grown using toluene.[30]

Polarised optical microscope (POM) images (Leica DM2500) of as-grown Si NWs (Supporting Information (SI), Figure S1 (c, d)) were used to evaluate the NW lengths ranging from 1 μm to up to 130 μm. The histogram distribution of the as-synthesized Si NWs shown in Figure 1 (b) demonstrates that the majority of NWs are 1 to 20 micron long, and the fraction of long NWs (> 50μm) is less than 2%. An SEM image of a network of Si NWs with a noticeable amount of non-straight NWs, impurities, NW aggregates and defective kinked NWs is presented in Figure 1 (a) (and Supporting Information (SI), Figure S1 (a, b, g)). Both the NW length distribution and structural imperfections in the as-prepared materials highlight a significant challenge in the device fabrication requiring highly ordered assembly of the NWs, without nanomaterials selection and purification.





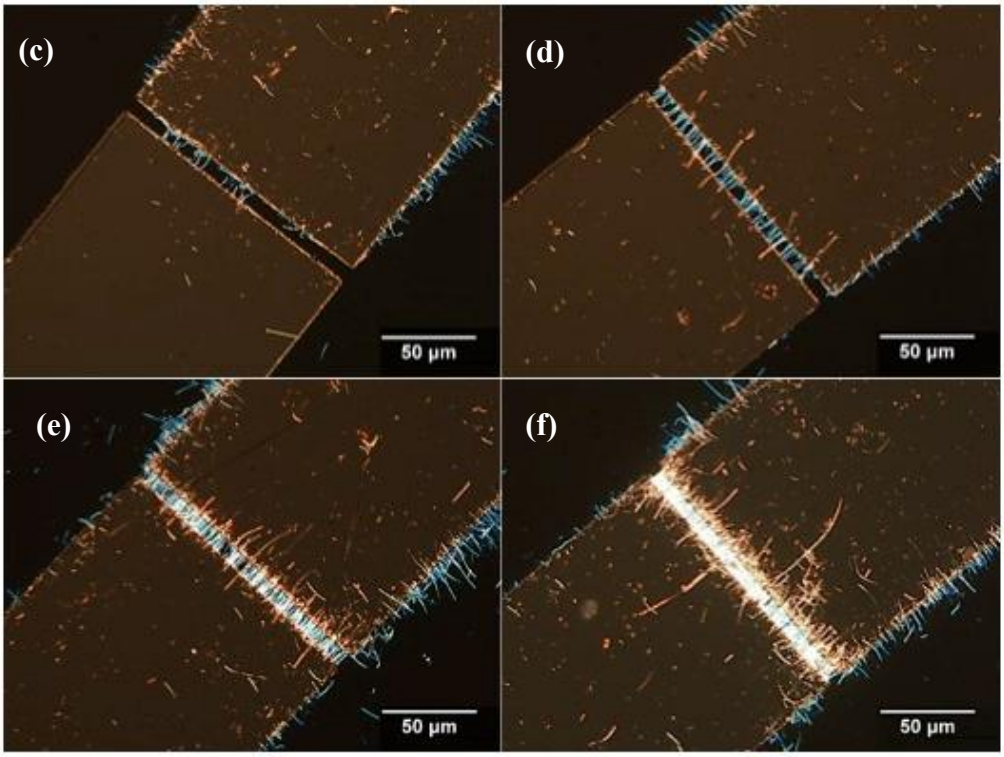


Figure 1. (a) SEM image of as-synthesized SFLS Si NW powder. (b) Length distribution of the as-synthesized (drop-casted) Si NWs, where y-axis gives the percentage of NWs with particular lengths. The majority of nanowires are less than 20µm long. The percentage of the NWs with lengths between 51 to 130 µm was 2%. Inset: lengths histogram of NWs collected by DEP across two different electrode gaps, 10 µm and 20 µm, highlighting much narrower distribution of lengths following the DEP collection. DEP alignment of SFLS Si NWs across parallel electrode-bars with 10 µm spacing, conducted at 900 kHz with various voltages: (c) 5 V, (d) 10 V, (e) 15 V and (f) 20 V. By increasing the applied voltage and/or the NW formulation concentration (~1µg/mL), the DEP assembly process results in a denser NW deposition/alignment.

The DEP assembly process employed a drop-cast method on an inclined substrate to provide a gravity-assisted slow flow of NW formulations perpendicular to the pre-patterned DEP electrode gap (Supporting Information (SI), Figure S2). This technique allowed to combine fluidic shear forces with DEP self-alignment to position NWs across the electrode gap, and to remove weakly-interacting NWs and impurities from the device channel region. The DEP

sinusoidal signal with a pre-set peak-to-peak voltage and AC frequency was applied prior to the NW dispersion being placed on the substrate. The signal parameters were systematically varied to adjust the dielectrophoretic force acting on the NWs and to study the effects of voltage and frequency changes, as we describe in more details in the following sections. The collection of NWs across the electrodes was monitored in real time by observing the corresponding impedance change associated with NWs being placed between the contacts (see Methods for the collection rate measurements). Following the DEP NW assembly process, the remaining dispersion was removed without affecting the aligned NWs, and the substrates were gently rinsed with isopropyl alcohol (IPA) or methanol to remove weakly attached NWs and impurities. Finally, the samples were dried and prepared for characterisation or further device processing. More sample preparation details can be found in the Methods/Experimental section.

Control of Si NW alignment, length distribution and orientation in the electrode gap

The DEP assembly offers a high degree of flexibility for NW positioning. Considering rectangular-shape electrodes separated by a gap (Figure 1 (c-f)), the DEP force is maximised when NWs are oriented along the channel and perpendicular to the electrode edges.[21] The great majority of the straight SFLS Si NWs in our tests was oriented at a 90^0 angle toward the electrodes edges, whereas curved shape NWs adopted the position close to a normal to the contact edge. The typical lateral alignment of NWs relative to the electrode gap was such that both ends of the NW rested to the counter-electrodes. DEP also served as a length selection tool by providing the strongest interactions for the NWs with lengths at least the same size of the electrode gap, or slightly longer. This opens the possibility of sequential separation of NWs by length through the use of device structures with varying electrode gap sizes. The

analysis of Si NW lengths following DEP collection across the 10 μm gap showed that the distribution of lengths was dramatically reduced, with 12% of NWs assembled with lengths <10 μm, and 72% of NWs with lengths from ~11 μm to 20 μm, where only 16% of NWs were in 21-40 μm range (Figure 1 (b)). The DEP collection at 20 μm gap resulted in 62% of NWs assembled with lengths from ~21 to 30 μm, where only 28% of NWs were in 31 to 40 μm and 10% longer than 40 μm.

Control of Si NWs density in the electrode gap

The NW density in the electrode gap is a critical parameter for device performance. In diodes and FETs, the conduction state current is directly related to the number of high quality semiconducting NWs bridging the gap, where the increase in NW numbers should lead to higher current.[31] However, NWs packing that is too dense, with nanoparticles' spacing being several diameters or less, can significantly reduce devices performance (*i.e.* in FETs) due to screening effect originating from electric field fringing between cylindrical shape nanoparticles, as was shown for carbon nanotube materials,[32, 33] and this effect can lead to a significantly reduced gate-to-FET channel coupling.[34] Therefore, the control of NW density is essential for high performance NW devices.

The increase of NW deposition density during the DEP process was controlled by changing two parameters: applied voltage and NW concentration in the formulation. An increase in applied voltage across the electrode gap enhances the DEP force, thus improving the deposition yield.[35, 36] Additionally, higher NW dispersion concentration results in denser NW packing in the gap between the contacts. Figure 1 (c-f) demonstrates the controllable deposition of SFLS Si NWs at different signal voltages, keeping the same applied frequency of 900 kHz, where the voltage was increased in 5 V steps, giving increased number of NWs

in the 200 μm wide electrodes (10μm gap) of: ~11 NWs at 5 V, ~45 NWs at 10 V, ~ 110 NWs at 15 V and >1000 NWs at 20 V. At the highest applied voltage of 20V, NWs tend to form a multilayer due to high packing density and non-straight morphology of some of the NWs. At the lower range of voltages from 5 to 15 V a consistent deposition of a monolayer' was achieved. The control of deposited NWs density across interdigitated electrodes was also demonstrated by changing the NW formulation density by an order of magnitude, as shown in Figure S3 (Supporting Information).

Si NWs conductivity selection through DEP frequency variation and impedance spectroscopy

DEP selectivity based on the NWs electrical parameters has been a critical challenge for poly-disperse Si NWs. Below we discuss a method to isolate and collect the highest quality SFLS Si NWs based on their conductivity properties, which can be selected according to their frequency dependence on the DEP force.

Initially, the electrical response of the NWs was systematically investigated by applying a DEP signal at various frequencies (up to 5 MHz). We examined the change of the impedance across two parallel metal electrodes following the deposition of the NW dispersion on the substrate, when the suspended NWs were attracted to the electrode gap by means of dielectrophoretic force (F_{DEP}), and the number of NWs in the gap increased with time. The time constant τ was extracted according to Eqs. 1, 2, describing the impedance drop after the placement of the NW dispersion on the electrodes. (see Methods for the impedance spectroscopy analysis). As the DEP signal frequency alters the strength of a dipole that can be induced in a particle in the presence of an external electric field,[22] the time constant is frequency dependent and reflects the conducting properties of the NWs.

Eq. 1 $$\boldsymbol{\tau = \frac{-t}{\ln\left(\frac{Z(t)-Z_0}{Z_{max}}\right)}}$$

Eq. 2 $$\boldsymbol{Z(t) = Z_{max}e^{-\frac{t}{\tau}} + Z_0}$$

where, $Z(t)$ is a time dependent impedance, empirically approximated by an exponential function, Z_{max} is the maximum impedance attained in DEP collection, Z_0 is a constant associated with a finite impedance value of the DEP electrode structure with deposited undoped NWs, t is time from the drop placement, $\tau=\tau(f)$ is the characteristic time constant of particle collection, which depends on the DEP signal frequency.

Mureau[37] suggested that since the time taken for the impedance drop during nanoparticles collection is inversely proportional to the DEP alignment force, then the inverse of the time constant is proportional to the magnitude of the force. In this case, the $1/\tau$ plot *versus* signal frequency should give us the frequency dependence of the DEP force experienced by different populations of NWs with various conductivity properties. For cylindrical shape nanowires, the dielectrophoretic force (F_{DEP}) force acting along the NW's long axis can be approximated to that of a prolate ellipsoid given by Eq. 3[21, 22, 38-41]:

Eq. 3 $$\boldsymbol{F_{DEP} = \frac{2L\pi r^2}{3}\varepsilon_m Re\{K_f\}\nabla E^2}$$

$$K_f = \frac{\tilde{\varepsilon}_p - \tilde{\varepsilon}_m}{\tilde{\varepsilon}_m}$$

$$\tilde{\varepsilon}_p = \varepsilon - j\frac{\sigma_p}{\omega}, \quad \tilde{\varepsilon}_m = \varepsilon - j\frac{\sigma_m}{\omega}$$

where, r is NW radius, L is NW length, ε_m is the permittivity of the fluid medium and ∇E^2 is the gradient of the electric field squared. K_f (the Clausius-Mossotti factor) is approximated by $\frac{\tilde{\varepsilon}_p - \tilde{\varepsilon}_m}{\tilde{\varepsilon}_m}$ for the long axis (needle) expressed as $\tilde{\varepsilon}_p = \varepsilon_p\varepsilon_o - j\frac{\sigma_p}{\omega}$ for the particle and $\tilde{\varepsilon}_m = \varepsilon_m\varepsilon_o - j\frac{\sigma_m}{\omega}$ for the medium where ε_p is the relative permittivity of the particle, ε_m is the

relative permittivity of the medium, ε_o is the vacuum permittivity, σ_p is the conductivity of the particle, σ_m is the conductivity of the medium and ω is the angular frequency of the electric field.

The time constants $\tau(f)$ were then extracted from the experimental impedance data $Z(t)$ obtained for a number of experiments conducted at DEP frequencies in the range of 5 kHz to 5 MHz. The $1/\tau$ characteristics *versus* frequency are summarised in Figure 2 (a), effectively showing the behaviour of DEP force *versus* frequency. The graph can be divided into two regions: the low frequency range, for low values below 500 kHz and the high frequency range, for values above 500 kHz. As represented by the time constant spectrum, above 500 kHz the dielectrophoretic force (F_{DEP}) reaches a plateau, compared to the lower frequency range and this trend is expected to continue to higher frequencies. At high frequencies (>500 kHz) the DEP forces, although small, are still sufficient to attract NWs to the electrodes. Lower conductivity NWs do not experience enough force to be assembled across the electrodes, so the NW collection occurs only for the higher conductivity ones, thus providing a conductivity selection mechanism. However, at lower frequencies, the DEP forces values are higher, resulting in the collection of NWs with various conductivities.

Assuming that charge carrier density is approximately the same for all of the SFLS-grown Si NWs, the conductivity is then determined by the crystal quality of the NW such as the concentration of surface and crystalline bulk defects. Variations of conductivity parameters were expected, since the SFLS synthesis produces NWs with various morphological and electrical properties. Due to the dependence of DEP force with conductivity, we infer that at the low frequency range DEP collects the various quality NWs, including poor-quality semiconducting Si NWs that may contain defects and associated traps, while high frequencies induce the collection of only the highest quality, low-defect semiconducting Si NWs, with higher conductivity.

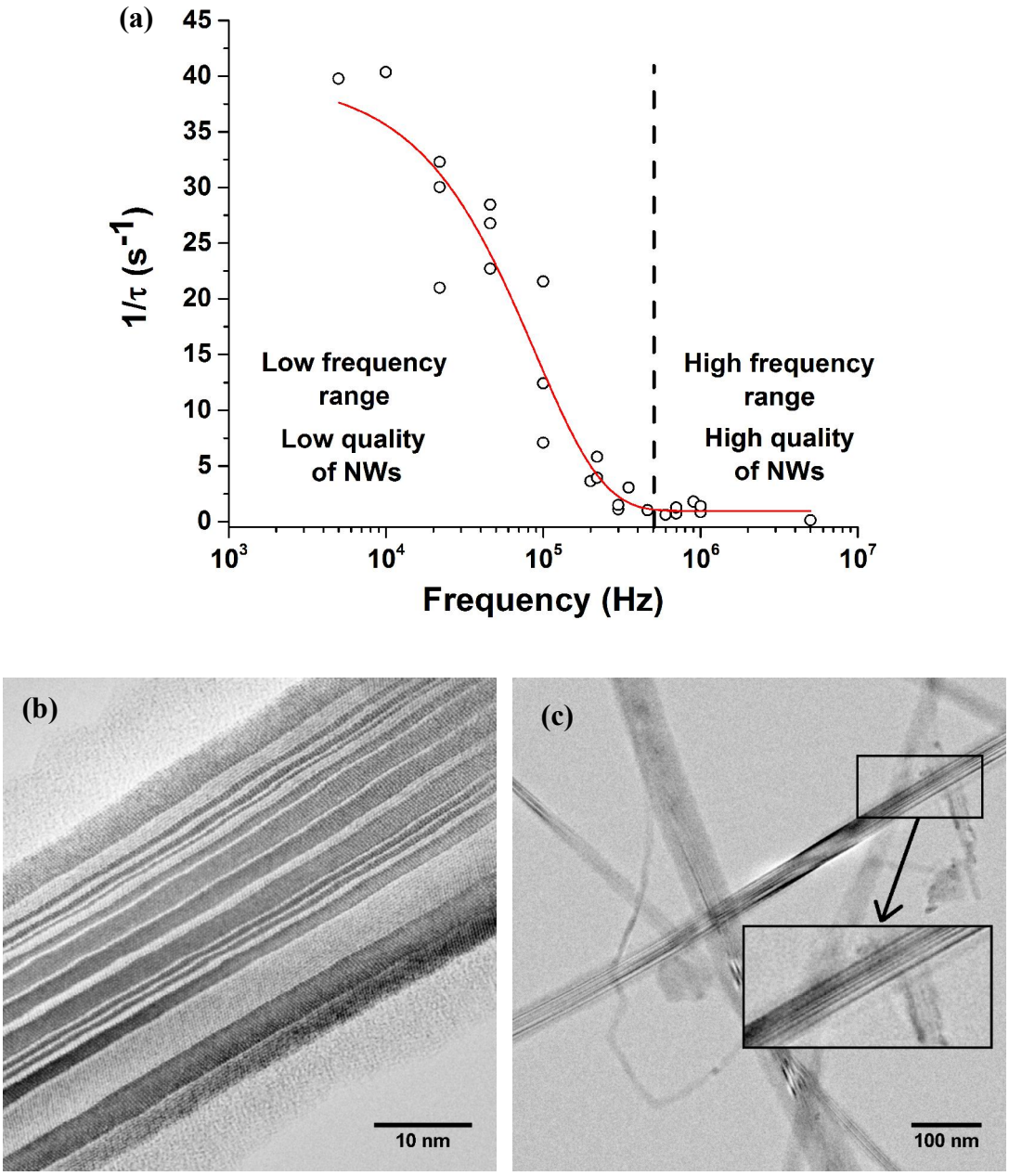


Figure 2. (a) Reciprocal of time constant (τ) as a function of DEP signal frequency. Experimental data are shown as dots, and the red line provides a guide to the eye. Data for low frequency (<500 kHz) correspond to the DEP assembly of NWs with various ranges of conductivity, whereas at higher frequencies (>500 kHz) only higher conductivity NWs are able to respond to the oscillating electric field. HRTEM images: (b) twin-defects across the NW indicated by the micro-faceting appearance; NW core diameter is 32 nm; (c) longitudinal stacking faults appear to continually follow the NW length.

Indeed, from Eq. 3 we know that the Clausius-Mossotti factor (CMF) is frequency dependent. CMF (K_f) indicates that, at different frequencies, the particle may be more or less polarisable than the medium, which in turn determines whether the NWs move towards the region of high electric field (positive DEP) or towards the region of low electric field (negative DEP).[23] If we assume that the geometry of the NW and the gradient of the applied electric field are the same, the dielectrophoretic force (F_{DEP}), becomes frequency dependent with CMF being the determining factor. Hence, the level of polarisability is related to the conductivity of the nanostructure, allowing the selection of highly conducting NWs by altering the applied frequency. Figure S4 and Table S1 (SI) shows how the calculated DEP force varies for different conductivity nanowires when subjected to the alignment at various DEP frequencies.

To experimentally evaluate the degree of crystalline imperfection, the SFLS Si NWs were analysed by high resolution transmission electron microscopy (HRTEM) for the presence of lattice defects which could affect the polarisability. Interestingly, a significant amount of twin defects (a type of grain boundary) were observed in the NWs (Figure 2 (b,c)), which were also seen in NWs synthesised by trisilane as a reactant for SFLS growth of Si NWs.[42, 43] Twin defects are considered to be formed in parallel to the crystal growth axis of the NW and are indicated by the micro-faceting appearance.[44] Effectively, they change the crystallographic orientation of the NW such as crystal-bonding disorders.[45] Also, longitudinal periodic stacking faults along the NW's length can be seen in Figure 2 (b, c). Additionally, some NWs were kinked (Supporting Information (SI), Figure S1 (a, b, g)) which is considered to originate from the interaction between NW tending to grow along preferred crystallographic axes and NW defects perpendicular to the NW growth direction.[46, 47] The conductance properties of the NW are highly affected by the kink geometry, as shown by

Cook *et al.*[48] All these defects ultimately determine the electrical properties (conductance) of the NW.

Considering that charge transport in small diameter NW (<60 nm) occurs mainly through the single crystal core,[49] the conductivity of SFLS NWs will mainly depend on charge carrier scattering from defects as described by the Eq. 4[50]:

$$\textbf{Eq. 4} \qquad \boldsymbol{\sigma = \frac{nq^2\tau_c}{m^*}}$$

where, n is the carrier concentration, q is elementary charge, τ_c is the mean free time between collisions and m^* is the charge carrier effective mass. Following Eq. 4, the variation of conductivity between the NWs is mainly determined by the value of τ_c, which is related to the density of defects (the quality of crystal lattice) in the NW structure, provided that the charge density (n) does not change, for example, as a result of trapping at the interface/surface defects. The effective, m^* can be considered as constant, since it is not likely to change significantly for the same batch of NWs. Thus, taking into account a noticeable number of crystalline defects in SFLS NWs (Figure 2 (b, c)) we can expect a certain degree of variation of NW conductivities independent of NW diameter.

FET analysis of Si NWs collected at different DEP frequencies

The electrical properties of the NWs collected at different DEP frequencies were compared using field-effect transistor devices. The NW FETs were prepared as identical bottom-gate device structures on Si/SiO_2 substrates, with pre-patterned gold electrodes with 10 μm electrode gap. The DEP NW alignment at different signal frequencies was conducted as described previously. The FET devices were completed by depositing top gold source-drain electrodes, to improve the metal contact to the NW channel (Figure 3 (c)). A more detailed

FET fabrication procedure is given in the Methods section. Transistors were characterised using a Keithley 4200 SCS semiconductor analyser in a N_2-filled glove box to minimise the effects of atmospheric contamination.

Typical FET transfer characteristics are shown in Figure 3 (a), where device current data were normalised to the number of NWs in the FET channel. All devices showed p-type accumulation behaviour. Devices with NWs collected at low DEP frequencies (100 kHz) showed low maximum current in the device on-state at the gate voltage (V_G) of -40 V. FETs fabricated with NWs collected at increasingly higher frequencies demonstrated a consistent trend of increased device current, resulting in up to 100 times higher current for NW FETs assembled at 2 MHz DEP signal. This trend clearly indicates that charge transport characteristics for NWs collected at higher frequencies (MHz range) is superior to that of NWs deposited at low signal frequencies (<500 kHz). Examination of FETs behaviour close to the threshold (Supporting Information (SI), Figure S5), when transistors turn on and current starts to increase sharply (Figure 3, a), show the slowest current rise for low frequency collected NWs, and the steepest rise for highly frequency assembled NWs. This sub-threshold behaviour indicates the difference in defect/trap states in the NWs or at the NW/dielectric interface, when higher density of traps results in a less steep current increase, as more trap states need to be filled. The sub-threshold swing (s-s) (V/dec) is the parameter that describes the amount of gate voltage required to increase FET current by an order of magnitude (see Methods). It is given by Eq. 5[51, 52] and Eq. 6,[53] and is related to the trap density (N_{trap}) as shown by Eq. 7[54, 55]:

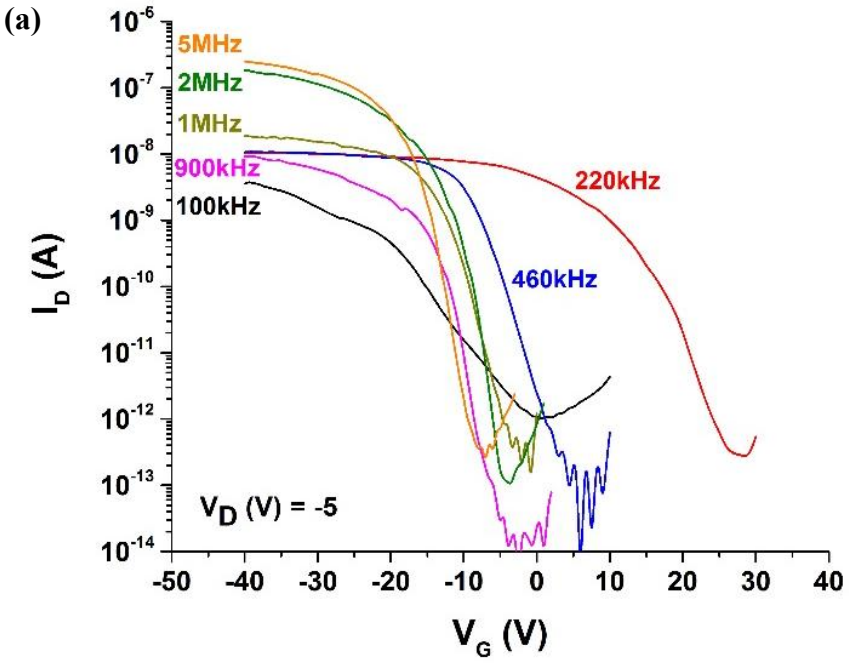
Eq. 5 $$s - s = \ln(10)\frac{\left(1+\frac{C_{it}}{C_{box}}+\frac{C_{si}}{C_{box}}\right)}{\left(\frac{q}{kT}-\frac{1}{E_{bnw}2r}\right)}$$

Eq. 6 $$s - s = \frac{\Delta V_G}{\Delta \log I_D}$$

Eq. 7 $$N_{trap} = \left[\frac{q(s-s)\log(e)}{kT} - 1\right]\frac{C_{NW}}{2\pi NrLq}$$

where, k is the Boltzmann's constant, T is absolute temperature, q is the elementary charge, E_{bnw} is the field at the bottom of the Si NW, r is the NW radius (~15 nm), C_{it} is the capacitance of interface states at the Si oxide-shell/Si region of the NW, C_{si} is the capacitance of the Si NW, and C_{box} is the back oxide capacitance (SiO_2), C_{NW} is the total gate capacitance, N is the total number of NWs across the channel, L is the channel length (10 μm).

The sub-threshold slope and trap density data were extracted from the FET characteristics and summarised in Figure 3 (b) showing a trend of consistent decrease in s-s values and trap densities for NWs collected at higher DEP signal frequencies. The lowest level of defects ($1x10^{13}$ cm^{-2}) is found for NWs collected at 5 MHz. More experimental data is also shown in Figure S6 (SI).



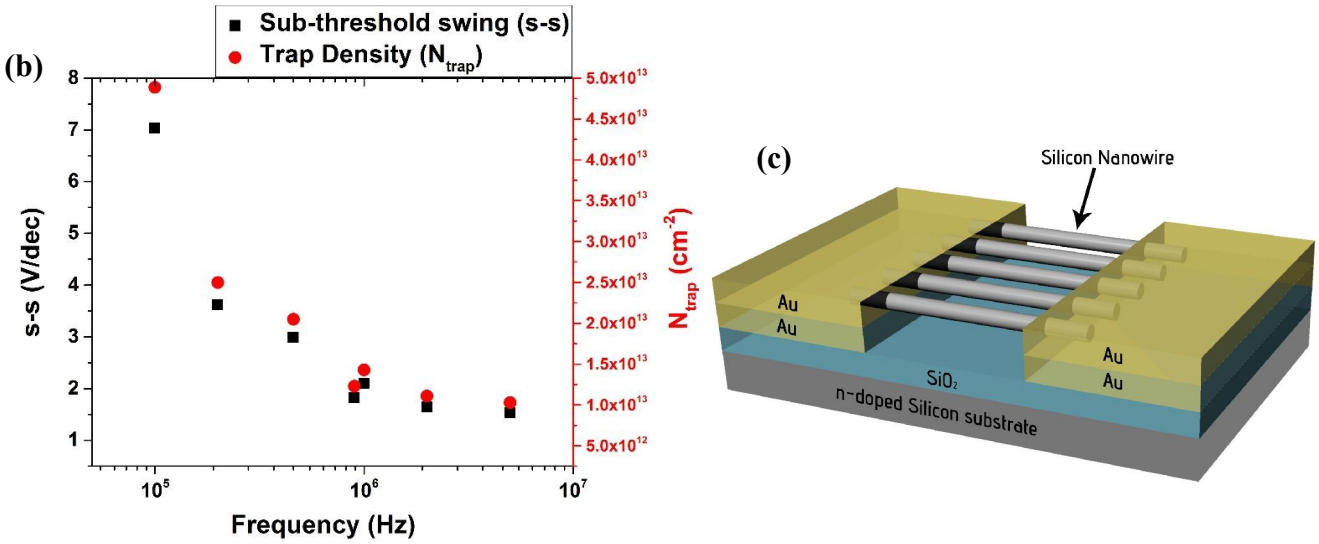


Figure 3. (a) Normalised transfer characteristics of FETs for NWs collected at DEP frequencies: 100 kHz, 220 kHz, 460 kHz, 900 kHz, 1 MHz, 2 MHz, 5 MHz. (b) Sub-threshold swing data (s-s) and NW trap density (N_{trap}) extracted from transfer FET plots presented in (a). At higher DEP collection frequencies, the value of the sub-threshold swing (s-s) and the number of traps (N_{trap}) decrease. (c) Schematic of a bottom-gate Si NW FET, showing NWs covered by a top contact.

Thus, we conclude that high-frequency DEP allows not only the alignment of NWs across the parallel micro-electrodes (source-drain contacts) but also the controlled selection of NWs with superior charge transport characteristics and lower level of defects from a mixture of different quality of Si NWs as produced by the SFLS growth method. This conclusion is consistent with our calculations using Eq. 3 (SI, Figure S4, Table S1), which show that at the same frequency, NWs with higher conductivity will experience higher DEP force than NWs with lower conductivity.

Conducting AFM analysis of Si NW collected at different DEP frequencies

In order to further investigate the conductivity of the low- and high- DEP frequency selected NWs, we performed conductive Atomic Force Microscopy (c-AFM) measurements. Device structures similar to the FETs were prepared with Si NWs assembled at DEP frequencies of 220 kHz and 5 MHz (see Methods for conductive-AFM characterisation). The samples were biased at the drain electrode of the structure, with the conductive platinum-silicide (PtSi) AFM tip being in contact with the Si NWs to act as a ground electrode (Figure 4 (a)). Such two-terminal current measurement allows probing the NW conductivity directly, as a function of position. The material for the tip was chosen in order to reduce the contact resistance with the underlying semiconducting nanostructures, without increasing the cantilever deflection, and thus allowing soft contact with the sample. By keeping the bias constant at 0.5 V and keeping constant force applied to the AFM tip, the current maps for NWs samples deposited at various DEP signal frequency were obtained by scanning the samples in contact mode in the direction perpendicular to the NWs. Both conducting AFM current data and AFM topological data were collected at the same time allowing to differentiate the NWs deposited in the channel, but not electrically connected to the contacts, from NWs that were fully electrically connected. Figure 4 (b-e) demonstrates typical images obtained for both height (AFM mode) and current (conducting mode) measurements of NWs aligned at different frequencies. During the measurement of approximately 200 NWs, a common trend was observed that NWs collected at 5 MHz DEP signal showed ~14 times higher current than the ones collected at 220 kHz. Current levels up to 233 pA were obtained for the NWs aligned at 5 MHz (Figure 4 (c)), while peak current values of 16 pA were measured for the ones assembled at 220 kHz (Figure 4 (d)). These current differences between the NWs collected at high and low DEP signal frequencies are fully consistent with the transistor measurements

demonstrating that selective nanoparticle assembly at various dielectrophoretic frequencies is directly correlated with the conductivity of the NWs.

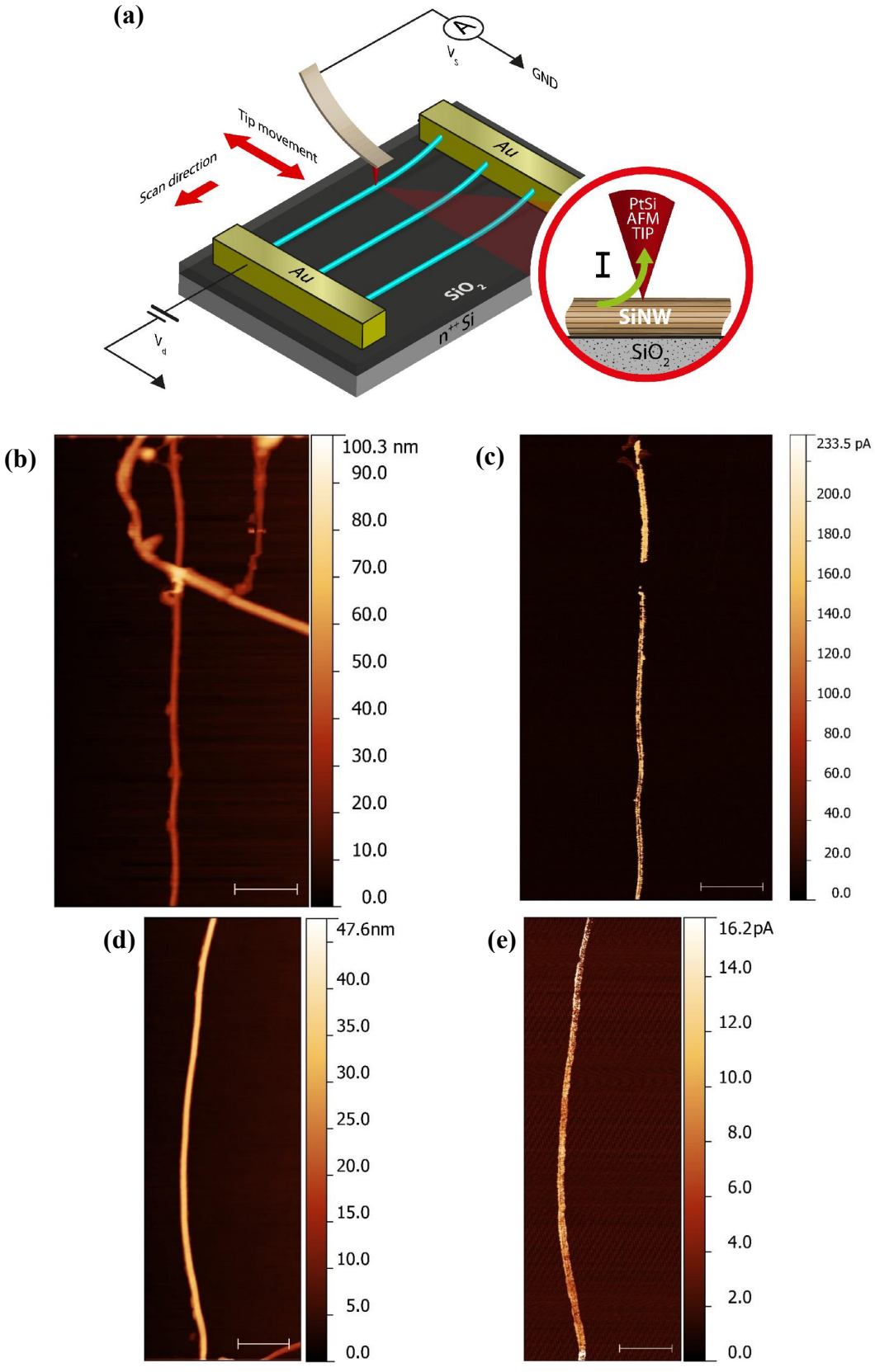


Figure 4. (a) A graphical illustration of the c-AFM measurement. The samples were biased at the gold electrode of the structure with the AFM tip (PtSi) being in contact with the Si NW (see inset) acting as the ground electrode. (b) Height map of a NW aligned at 5 MHz, and (c) the corresponding current map. Only one straight, fully electrically connected NW is visible in the image. (d) Height map of a NW aligned at 220 kHz and (e) its current map. Scale bars are 1 μm. Conducting Si NWs have similar diameters: 33 nm in (b) and 34 nm in (d). All the images were obtained in the trace mode with a pixel size of 5.9 nm. NWs aligned at higher frequency showed higher peak currents up to 233 pA (c), compared to the 16 pA peak current found in the lower frequency assembled NWs (e).

One-step solution process for high quality Si NW FET devices

Further characterisation of the high quality collected NWs was conducted by analysing parameters of bottom-gate FET devices, which were fabricated with the SFLS Si NWs assembled at 5 MHz signal frequency (see Methods for the FET fabrication). The NWs were aligned on 50 nm thick interdigitated finger electrodes with 10 μm channel length at 10 Vpeak-to-peak sinewave DEP voltage. Devices were completed with top gold electrodes, followed by a short annealing time to improve the metal-semiconductor contact.[4] Due to the higher quality of the NWs, the number of the aligned NWs was intentionally reduced to avoid gate field screening effects for closely packed NWs, which is detrimental to the maximum performance of the FET device.[56, 57] Typical transfer and output characteristics of the NW FET, which consists of approximately 20 NWs (POM shown in Figure 5 (c)), are shown in Figure 5 (a, b). The transfer scan (Fig. 5 (a)) exhibits good gate-to-channel coupling through the increase in I_D with increasing V_G. The output characteristic (Fig. 5 (b)) show near-Ohmic contact behaviour. This performance was expected, since the work function of gold (Au) (5.1 eV) for p-type transport is closely matched to the valence band edge of Si (5.17 eV).[53] Several key transistor parameters were extracted from the linear regime transfer characteristic, including the on/off current ratio ($I_{ON/OFF}$), the sub-threshold swig (s-s), the

threshold voltage (V_{TH}), the transconductance (g_m) and the device mobility (μ). The device threshold voltage (V_{TH}) was found to be ~ -9V by fitting a straight line from the linear transfer plot and finding the x-axis intercept (SI, Figure S5).[53] The device exhibited high on-current (~5.8 μA at V_G= -40 V, V_D= -0.5 V) and low off current, with a 10^6-10^7 on/off current ratio. The sub-threshold swing (s-s) was calculated to be ~1.5 V/decade and the density of traps was estimated to be 1 x 10^{13} cm^{-2} using Eq. 7[54, 55].

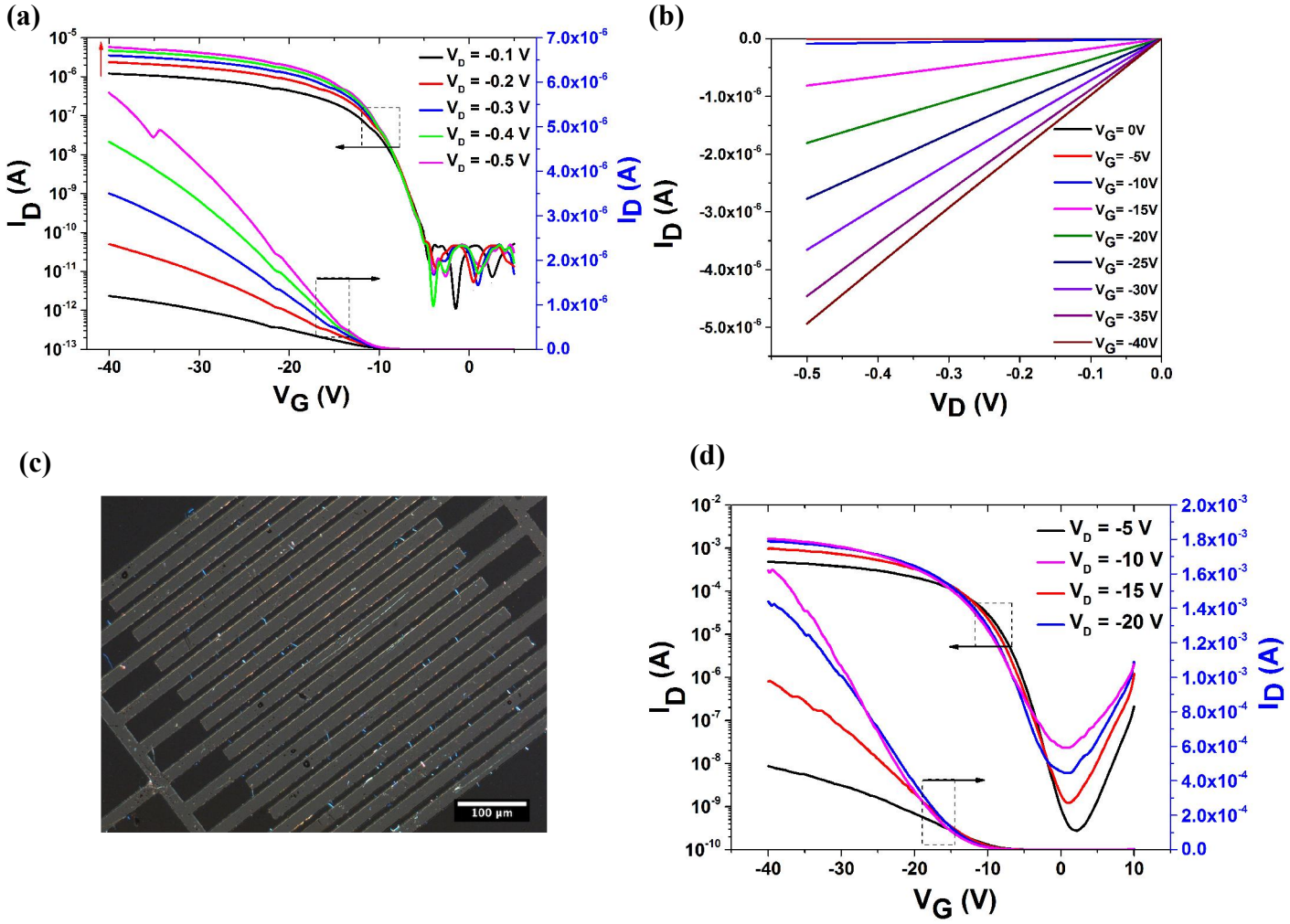


Figure 5. (a-b) Typical I-V characteristics of bottom-gate NW FET with NWs assembled at 5 MHz signal frequency. (a) Transfer characteristic showing current in logarithmic and linear scales at V_D = -0.1 to -0.5 V, in -0.1V steps for an FET with 20 NWs in the channel. (b) Output characteristic of the same FET at V_G = 0 to -40 V in -5V steps. (c) Polarised optical microscope (POM) image of the measured FET device with I-V characteristics shown in

(a,b). (d) Example of a high current characteristics FET device (300 NWs, DEP frequency 20MHz), showing current in logarithmic and linear scales at V_D = -5 to -20 V, in -5 V steps. Maximum current is 1.6mA.

The device mobility (μ) was calculated from the linear regime transfer characteristic using the cylinder-on-plate model,[24, 58-60] which takes into account the finite number of NWs in the channel and the electrostatic fringing effect of the gate field acting on the aligned NWs, using the Eqs. 8, 9:

Eq. 8 $$C_{NW} = N \frac{2\pi\varepsilon_o\varepsilon_r L}{cosh^{-1}(\frac{r+d}{r})}$$

Eq. 9 $$\mu = \frac{L^2}{C_{NW}} \frac{1}{V_{SD}} g_m$$

where, C_{NW} is the total gate capacitance, N is the total number of NWs across the channel, ε_o is the absolute permittivity, ε_r is the SiO_2 dielectric constant (~3.9), L is the channel length (10 μm), r is the NW radius (~15 nm) and d is the thickness of the gate dielectric (~230 nm). C_{NW} was calculated to be ~0.012 pF, and the transconductance ($g_m = \frac{\partial I_D}{\partial V_G}$) was found to be ~0.292 μS at V_D = -0.5 V (data from Fig. 5(a)). Based on these parameters, the device mobility (μ) was calculated to be ~ 47 ± 7 $cm^2V^{-1}s^{-1}$. We note that variation of NW diameters in the FET channels was relatively small, and as observed by AFM, the majority (60%) of the collected NWs' diameters were in the range of 20 to 39 nm (SI, Fig. S7 (b)). A typical cross-sectional AFM scan of an FET NW channel is shown in Figure S7 (a) (SI). As some variation of NW diameters was observed on all DEP assembled devices, the average diameter (30nm) was used for the mobility calculations. Small variation of the NW diameters (30nm +/- 10nm) can affect the devices' mobility by only ± 10%.

Finally, as a proof of concept, NWs were aligned by DEP at the higher frequency of 20 MHz.

Reproducible NW collections has been verified, and NW FET devices demonstrated excellent performance with low sub-threshold swing (s-s) of 1.26 V/dec and trap density (N_{trap}) of 8.42 x 10^{12} cm^{-2} as shown on Figure S8 (a, b) (SI). FET charge carrier mobility values calculated using Eqs. 8-9 ranged from 37 cm^2 V^{-1} s^{-1} to 50 cm^2 V^{-1} s^{-1} (SI, Fig. S8 (c)). Additionally, we demonstrated that such devices exhibit excellent current performance with on- currents up to 1.6 mA when measured at higher drain bias voltages (see transfer characteristics in Figure 5 (d)).

The electrical conductivity of the aligned Si NWs at 20 MHz was evaluated by calculating both CMF (SI, Fig. S4, (a)) and F_{DEP} values (SI, Fig. S4, (b)) using Eq. 3 and values ε_p=11.9, σ_p=18 S/m (for Si NWs), ε_m=36.7, σ_m=2.5 x 10^{-4} S/m (for DMF) in MATLAB. Based on Figure S4 (a, b), at 20 MHz the lowest NW conductivity value that can result in a positive DEP force for NW alignment was found to be 18 S/m (or 0.18 S/cm) corresponding to a dielectrophoretic force (F_{DEP}) of 7.7 x 10^{-29} N.

The conductivity value for Si NWs aligned at 5 MHz was also estimated using data obtained from conducting AFM studies. The resistivity of the NW, corresponding to Figure 4 (c) was extracted using the relation $\rho = \frac{\pi r^2 R}{L}$, where *r* is NW radius, *L* is the distance from the biased contact to the AFM tip position and *R* is NW resistance calculated based on two-point measurement corresponding to the applied voltage and measured current value. Conductivity (σ) was found as $\sigma = 1/\rho$=0.02 S/cm which is lower than the conductivity value estimated from CMF calculations as shown in Figure S4 (c, d), that can be explained by a possibly high contact resistance that was not taken into account in this two-point probe method.

Conclusions

In conclusion, we have experimentally demonstrated that dielectrophoresis coupled with

impedance spectroscopy provides a powerful tool for selection and collection of semiconducting NWs with different electrical and morphological properties resulting in controlled deposition of high quality, lowest level of defects/traps NWs with a narrow distribution of lengths and electrical properties. It also allows simultaneous positioning of NWs with respect to pre-patterned electrodes.

We also found that as-synthesised SFLS Si NWs show a large dispersion in mobility values due to various densities of defects and trap states all affecting the ability to form a dipole in the fast oscillating external non-uniform DEP field.

Importantly, one-process step DEP assembly at 5-20 MHz signal frequencies and a 5-10 V applied voltage allows to produce an "aligned monolayer" of NWs with controllable density that is ideal to fabricate high performance solution processed NW transistors. FET devices based on SFLS Si NWs were demonstrated with excellent performance characteristics, including high on/off current ratios of 10^6-10^7, low off current, high *on*-current of up to 1.6 mA, sub-threshold swing (s-s) of ~1.26 V/decade and device mobility of ~50 $cm^2\ V^{-1}\ s^{-1}$.

We propose that dielectrophoresis and collection rate impedance spectroscopy enable effective selection and assembly tool for the fabrication of reproducible, high quality NW based devices, providing the pathway to a printed electronics approach that can be scaled up for industrial applications.

Methods/Experimental

Materials, chemicals. Hydrous *N, N*-Dimethylformamide (319937) was purchased from Sigma-Aldrich Chemicals and used for dispersing the nanowires (NWs) as received. The silicon (Si) NWs used in this work, were grown *via* Supercritical Fluid-Liquid-Solid (SFLS). The NW dispersions were obtained using ~3 μg of NWs powder and 60 μL of toluene, and further dispersed in 3mL of *N, N*-Dimethylformamide (DMF).

Collection rate measurements. DEP collection and impedance measurements were performed using nickel bar-shaped electrodes on thin glass substrates with a 10 μm gap length. Substrates were cleaned with O_2 plasma to ensure the removal of organic residue. Sinusoidal DEP signals with amplitudes 20 Vpeak-to-peak, and frequencies ranging from 5 kHz to 5 MHz, were generated using a PSM1735 NumetriQ frequency response analyser. The impedance changes with time were recorded with PSM1735 NumetriQ, connected to a personal computer, with a "CommView" Version 1.15 software package.

To provide a slow solution flow during NW formulation deposition and DEP alignment, a *slope technique* was used (Supporting Information, Figure S2). The substrate was placed on an inclined surface of approximately 30 degrees (*versus* horizontal plane) to allow nanowire formulation droplets flow along the substrate. This method avoids the use of pumping motors and micro-fluidic channels. The flow of the NW solution was perpendicular to the micro-electrode gap to provide weak directional shear forces, which assist is the NW lateral alignment.

The impedance data recording process began few seconds prior to the NW DMF suspension being placed on the electrode gap and continued typically for one minute. This process was repeated several times, using new set of electrodes, for all the DEP frequencies used.

Impedance spectroscopy analysis. The frequency dependant time constant values were determined from the change of the total impedance over time for each DEP frequency. The change of the impedance was approximated by an exponential decay in order to determine a characteristic time constant related to the rate of nanowires collection (Eqs. 1-2). We also note that single exponential dependence was used to describe the *fast* impedance decay, immediately following the placement of the NW formulation on top of the DEP electrodes. This fast impedance decay was responsible for > 98% impedance drop compared to the total impedance change Z_{max}-Z_0. Data were processed through a MATLAB custom program and

the time constant values were extracted by fitting the exponential plot using the MATLAB curve-fitting tool (*cftool*).

The collection rate spectra were analysed for each DEP signal frequency, from 5 kHz to 5 MHz, and then summarised in a $1/\tau$ *versus* frequency plot (Fig. 2 (a)). An example of a typical impedance *Z(t)* plot at 22 kHz is shown in Figure S9 (Supporting Information).

Nanowire FET fabrication and measurements. Bottom-gate field-effect transistors were fabricated on Si/SiO_2 substrates. Dielectrophoretic gold contact structures, 50 nm thick, were patterned using photolithography (lift-off), with 2 nm titanium adhesion layer. The alignment of NWs was performed by applying an AC field across the two parallel electrodes forming the source and drain contacts of the device. The substrate was positioned on an inclined surface in order to provide a flow of the nanowire "ink" as described above. (Supporting Information, Figure S2). A ~10-20 μL drop of the NW dispersion was deposited using a syringe on top of the electrode structures, with the micro-electrodes being perpendicular to the NW flow. Si NWs were aligned under the influence of an alternating voltage potential of 10 Vpeak-to-peak and sinusoidal frequency, supplied by an AIM-TTI TG550-5 MHz function generator. After the DEP alignment, the excess of the solution at the bottom of the substrate was absorbed by a tissue (no direct contact with the aligned NWs), then the substrate was gently rinsed with isopropyl alcohol (IPA) or methanol in order to remove the weakly attracted NWs and impurities, and gently dried under an N_2 flow. All the steps related to solvent removal/evaporation or rinsing the substrates were conducted with great care not to disturb the NWs trapped in the device channel. A second photolithographic lift-off step was performed on top of the aligned NWs to improve the nanowire-contact properties. Au layer, 50 nm thick, were sputtered on top of the dielectrophoretic structures using a JLS MPS 500 Loadlocked Sputter Coating, followed a lift-off step in acetone. The top 'wrap-around' electrodes increase the nanowire-metal contact area and enhance current injection.

Afterwards, the FET devices were post-annealed at 250°C for 45 minutes. Current-Voltage (I-V) measurements of the FET devices were performed in a dry N_2-filled glove box using a Keithley 4200 Semiconductor Characterisation System (SCS).

FET sub-threshold swing values were extracted from the log-linear I-V transfer plots using Eq. 6. Figure S5 (SI) shows a graphical representation of the sub-threshold swing (s-s), on/off current ($I_{ON/OFF}$) and threshold voltage (V_{TH}).

Crystal structure characterisation of the NWs was performed using high resolution transmission electron microscopy (HRTEM) (HITACHI HD-2300A STEM). The growth direction was assigned based on the diffractograms of the HRTEM images of single crystal core nanowires, with more crystallographic data given in Supporting Information, Figure S1 (e, f).

Conducting-AFM characterisation. An MFP-3D (Asylum Research) Atomic Force Microscope (AFM) was used combined with an Orca^{TM} cantilever holder for conductive-AFM characterisation. All measurements were performed under ambient conditions using a platinum silicide (PtSi-FM) cantilever (Nanosensors^{TM}). Both the trace and retrace signals were used for extracting the average currents. Gwyddion v2.39 SPM data analysis software was used for the interpretation of the results.

NW diameter characterisation. The same AFM system was used to evaluate the NW diameters in the assembled devices. All measurements were conducted in contact mode under ambient conditions. The scanning speed was set at 0.3 Hz and the set point at 0.2 V to avoid damaging the nanostructures. Both the trace and retrace signals were analysed using the aforementioned SPM data analysis software. AFM cross-sectional profile data for a typical nanowire –FET channel is shown in Figure S7 (SI).

ASSOCIATED CONTENT

Supporting Information. SEM, polarised optical microscope (POM) and TEM images of SFLS Si NWs, NW deposition technique, CMF and F_{DEP} calculations, NW FET device characterisation (transfer, output, sub-threshold swing, corresponding trap densities and FET device mobility). AFM profile scan of the Si NWs. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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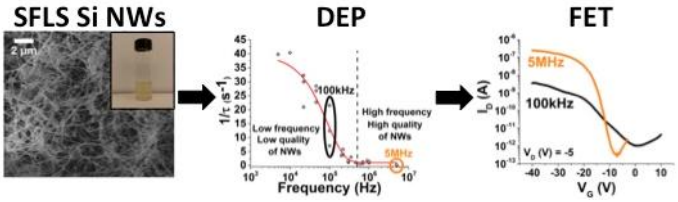
Table of Contents Graphic



Supporting Information

Simultaneous Tunable Selection and Self-Assembly of Si Nanowires from Heterogeneous Feedstock

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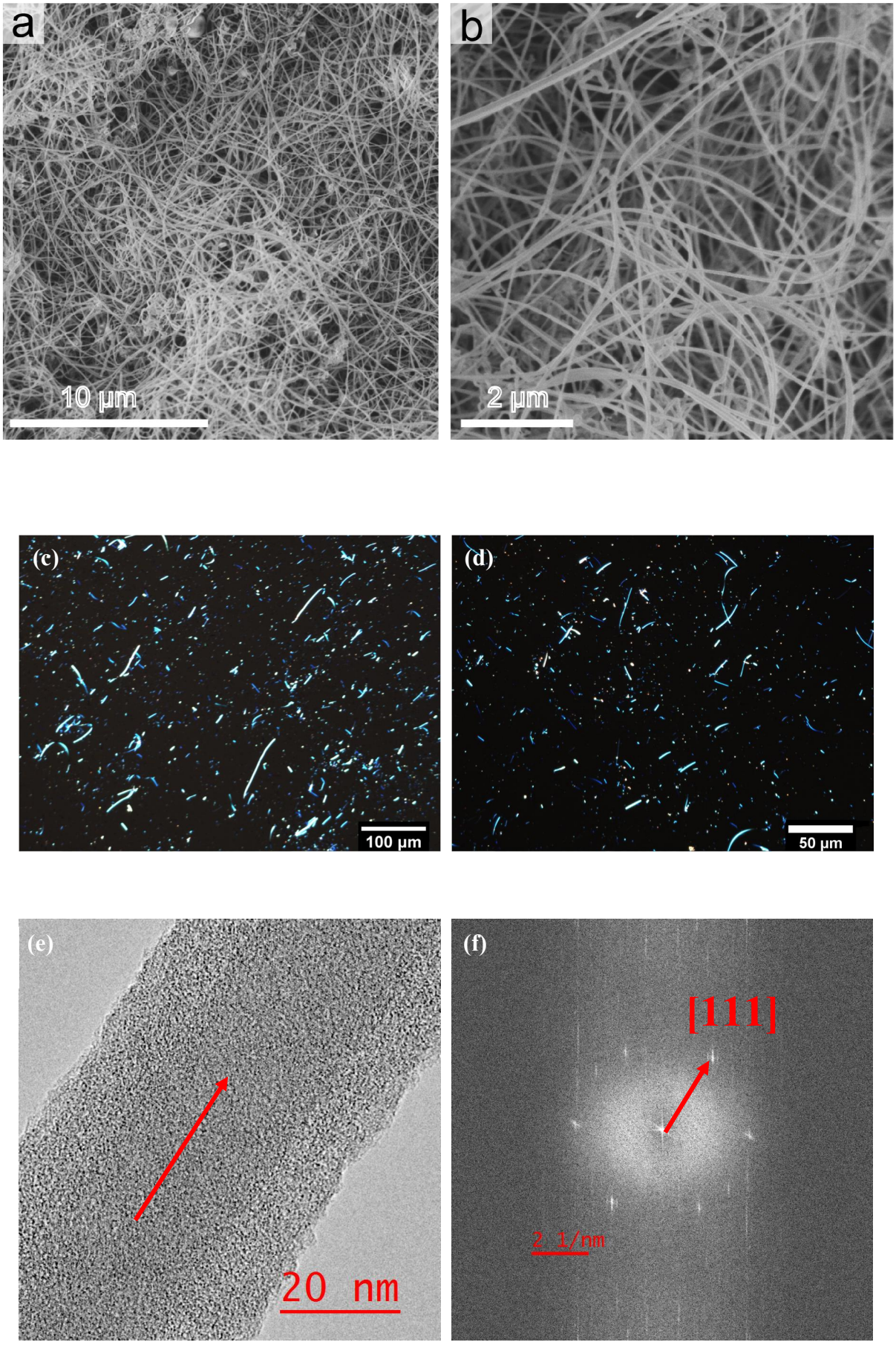

a
10 μm
b
2 μm
(c)
100 μm
(d)
50 μm
(e)
20 nm
(f)
[111]
2 1/nm

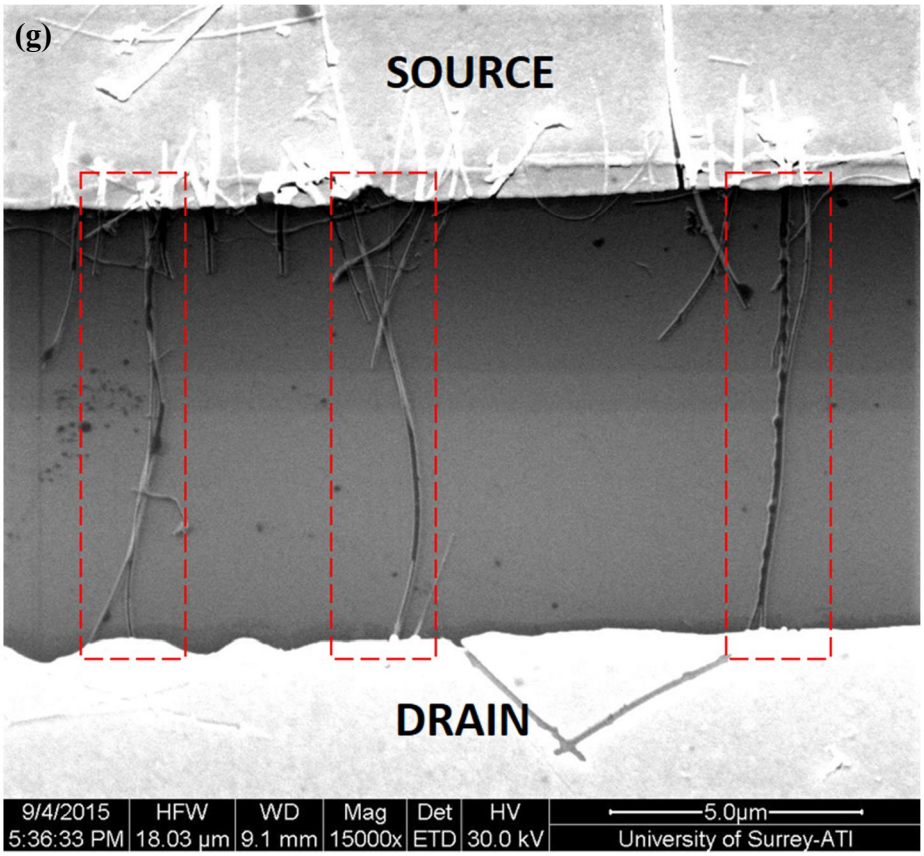


Figure S1. (a, b) SEM image of as-synthesised Au seeded SFLS-grown Si NWs. Non-straight, kinked NWs, and some amounts of impurities are clearly visible. (c, d) Examples of polarised optical microscope (POM) images of NWs on Si/SiO_2 substrates used for the analysis of NW length distribution. 100 µm scale left image, 50 µm scale right image. HRTEM image (e) and FFT pattern (f) of a drop-casted Si NW dispersion in DMF on TEM carbon grid. The reflection at 55 degrees is 6.211 nm^{-1} - equals 3.2 ± 0.1 Å. NW growth direction is [111]. (g) SEM image of the DEP aligned Si NWs across 10 µm gold (Au) source-drain electrodes. The red-dotted lines highlight the aligned Si NWs. The SEM reveals the non-straight nature of the SFLS Si NWs.

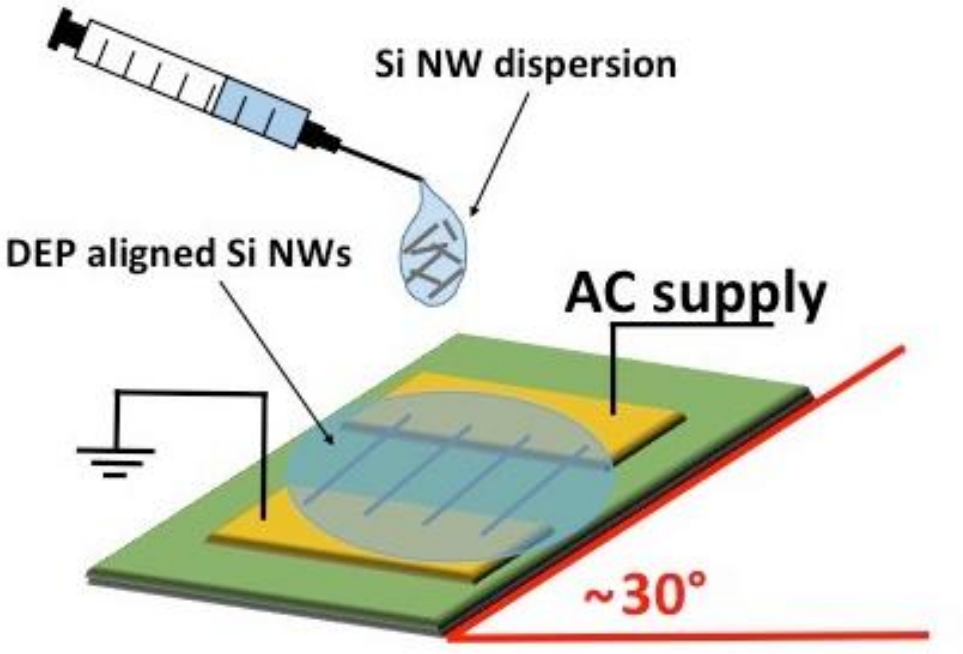


Figure S2. Graphical illustration of the *slope technique* used in this work for the NW deposition and DEP alignment. Substrate was tilted at approximately 30^{o} angle (*versus* horizontal plane) to provide gravity assisted flow of NW dispersion.

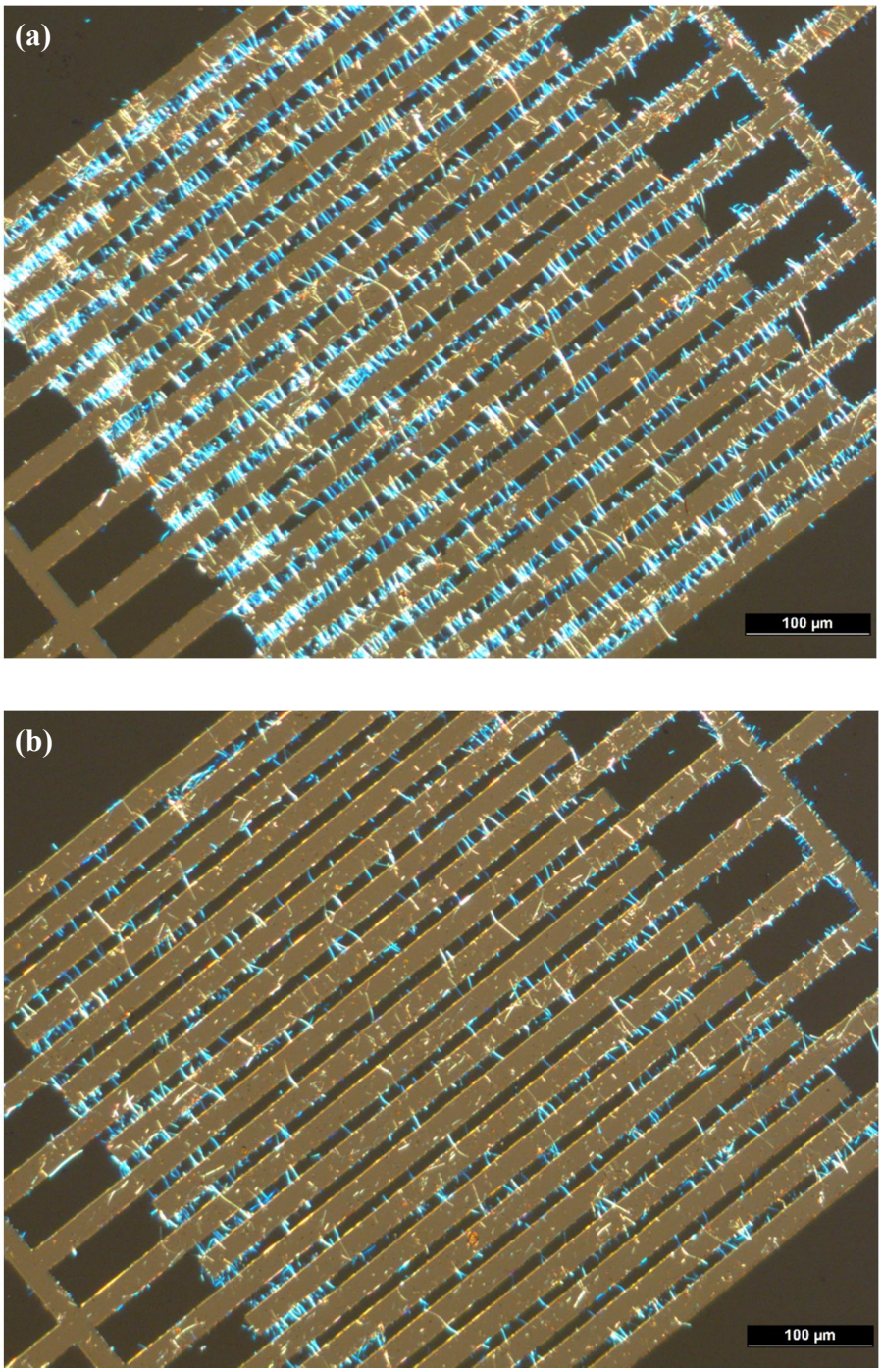
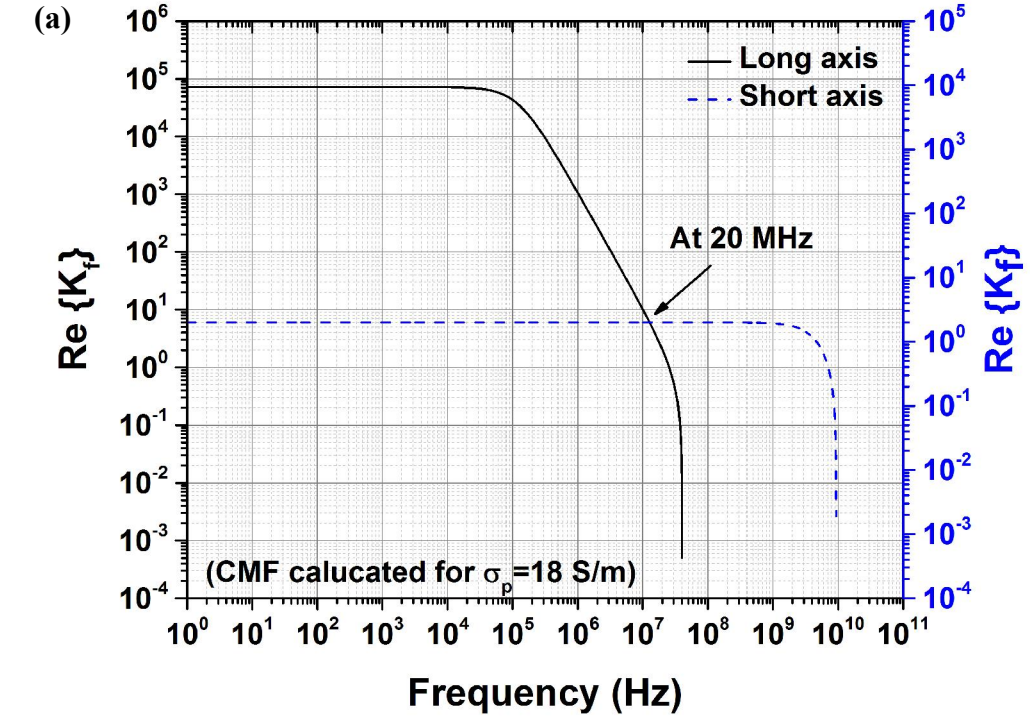
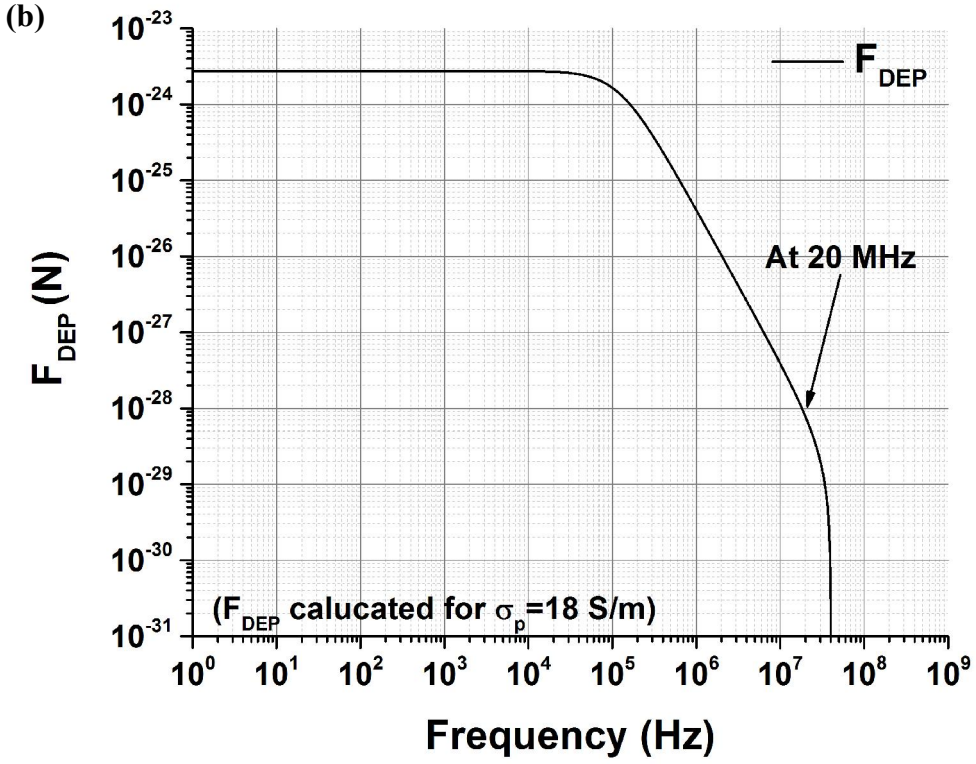


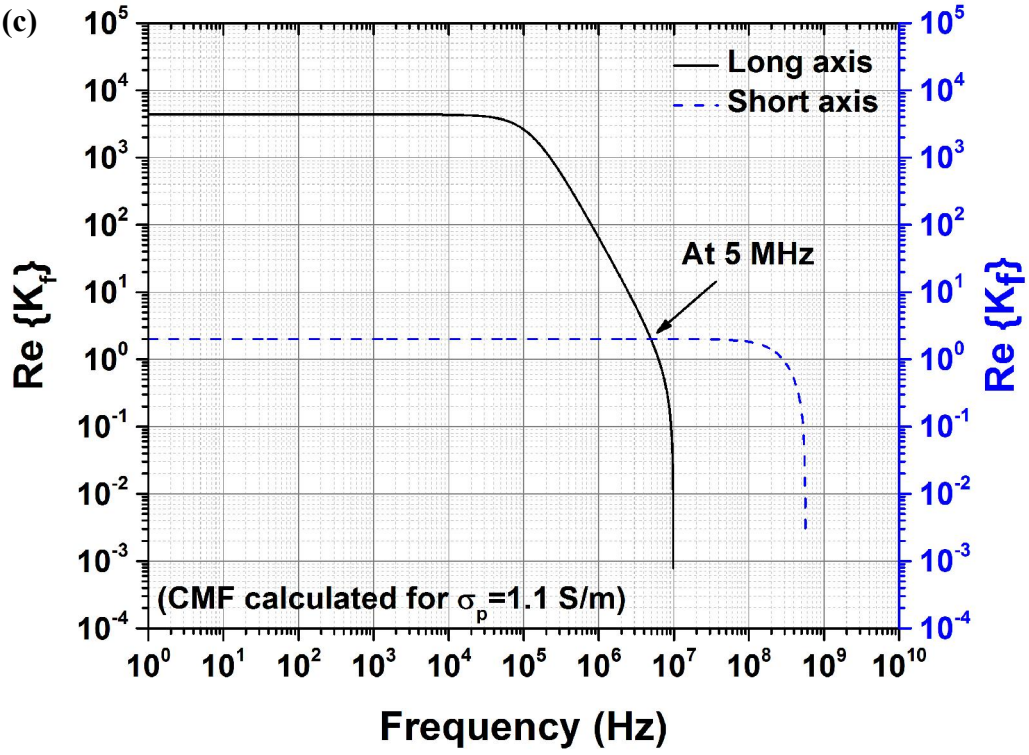
Figure S3. POM image of DEP alignment of SFLS Si NWs across interdigitated finger electrodes at (a) high and (b) low (10 times less) NW density concentrations. NWs were aligned at 900 kHz, 10 Vpeak-to-peak across 10 µm electrode gap.

The following 4 pages are related to Fig. S4

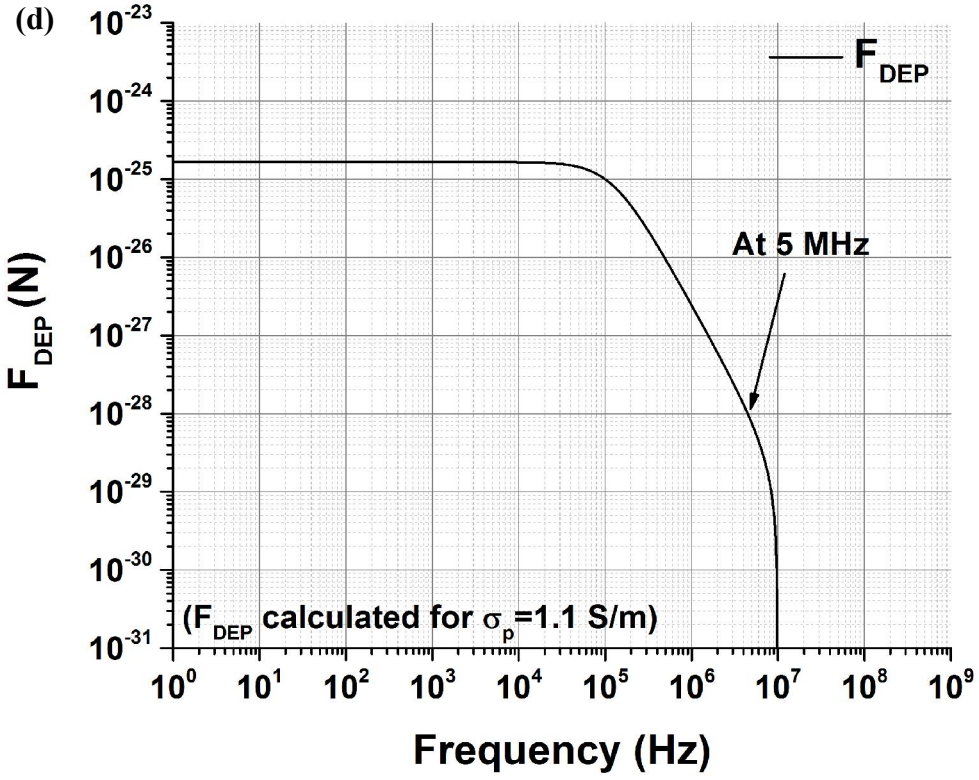




(c)


Long axis
Short axis
At 5 MHz
(CMF calculated for σp=1.1 S/m)
Re {Kf}
Re {Kf}
Frequency (Hz)

(d)


FDEP
At 5 MHz
(FDEP calculated for σp=1.1 S/m)
FDEP (N)
Frequency (Hz)

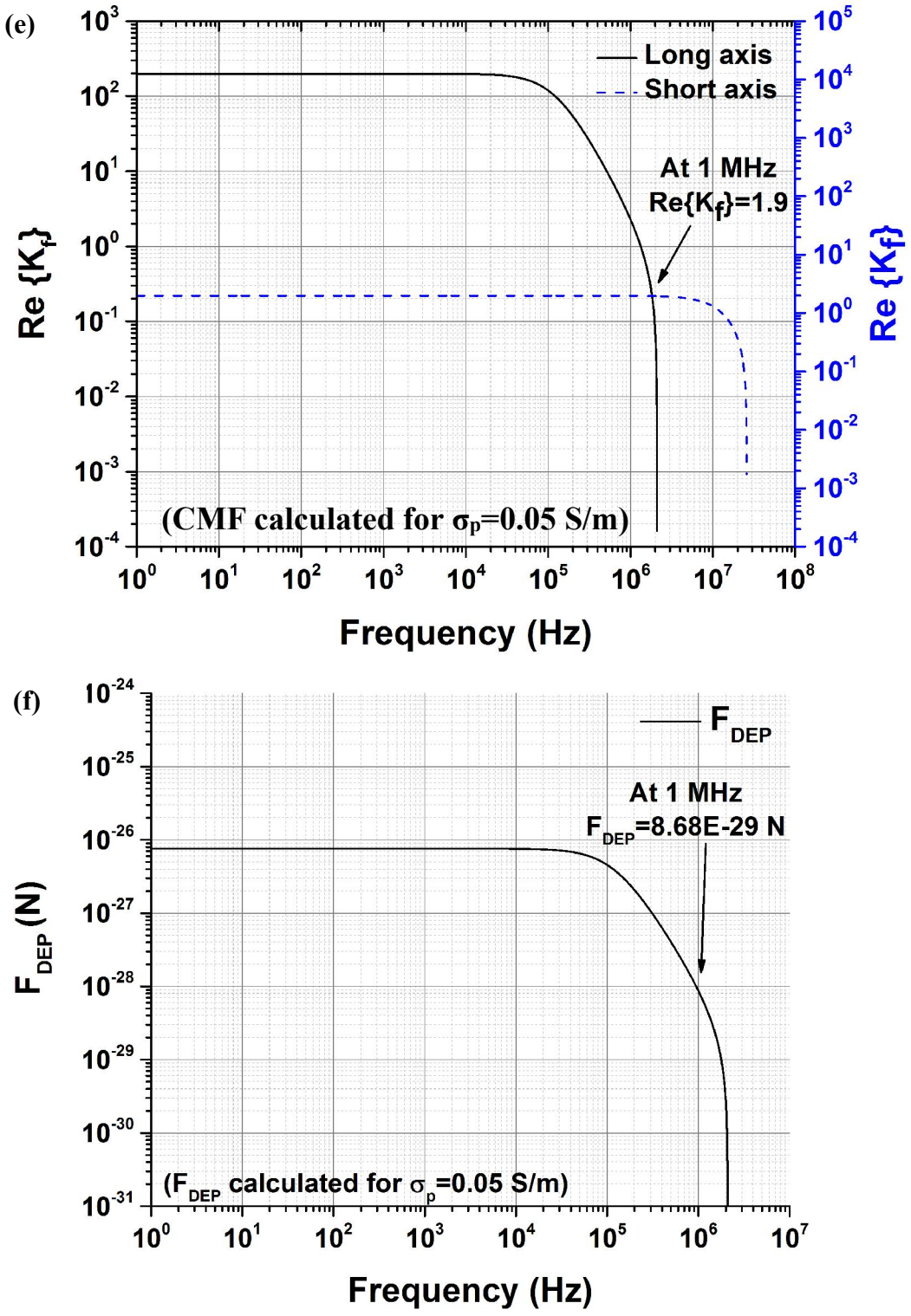


Figure S4. Calculated values of the real part of the Clausius-Mossotti factor (CMF) and estimated applied dielectrophoretic force (F_{DEP}) for the long and short axis of Si NWs (ε_p=11.9) with three conductivity values (σ_p=18 S/m, σ_p=1.1 S/m, σ_p=0.05 S/m) suspended in DMF (ε_m=36.7, σ_m=2.5 x 10^{-4} S/m) plotted as a function of DEP AC signal frequency. Plots for various conductivity NWs are shown in: (a, b) for σ_p=18 S/m, (c, d) for σ_p=1.1 S/m, and (e, f) for σ_p=0.05 S/m. The CMF plots (a, c, e) show that at a particular frequency, CMF

values for long and short axis will be equal, thus defining the maximum frequency at which DEP alignment of nanowires will occur. As the conductivity of the NWs increases, this maximum dielectrophoretic frequency increases. If we choose a fixed DEP alignment frequency, we can follow each plot (b, d, f) to find a DEP force that will act on the nanowire (long axis), overall showing a trend that higher conductivity nanowires will experience a higher DEP force. (see Table S1 below)

Table S1: Dielectrophoretic forces (F_{DEP}) at 1MHz DEP frequency calculated for Si nanowires with three different conductivity values corresponding to that shown in Figure S4 (b, d, f). The highest conductivity nanowires experience the highest DEP force.

	For σ_p=18 S/m	For σ_p=1.1 S/m	For σ_p=0.05 S/m
Frequency (MHz)	**F_{DEP} (N)**	**F_{DEP} (N)**	**F_{DEP} (N)**
1	4E-26	2.5E-27	8.7E-29

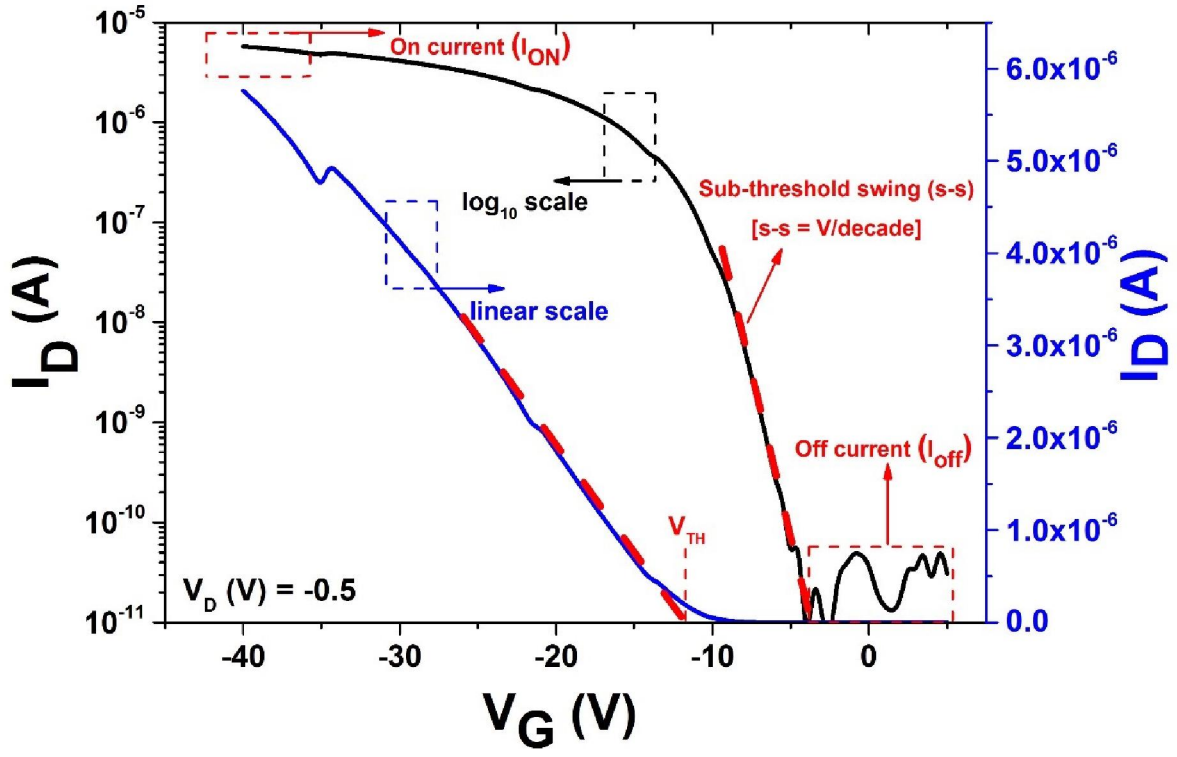


Figure S5. A graphical presentation of the sub-threshold swing (s-s), on/off current ($I_{ON/OFF}$) and threshold voltage (V_{TH}).

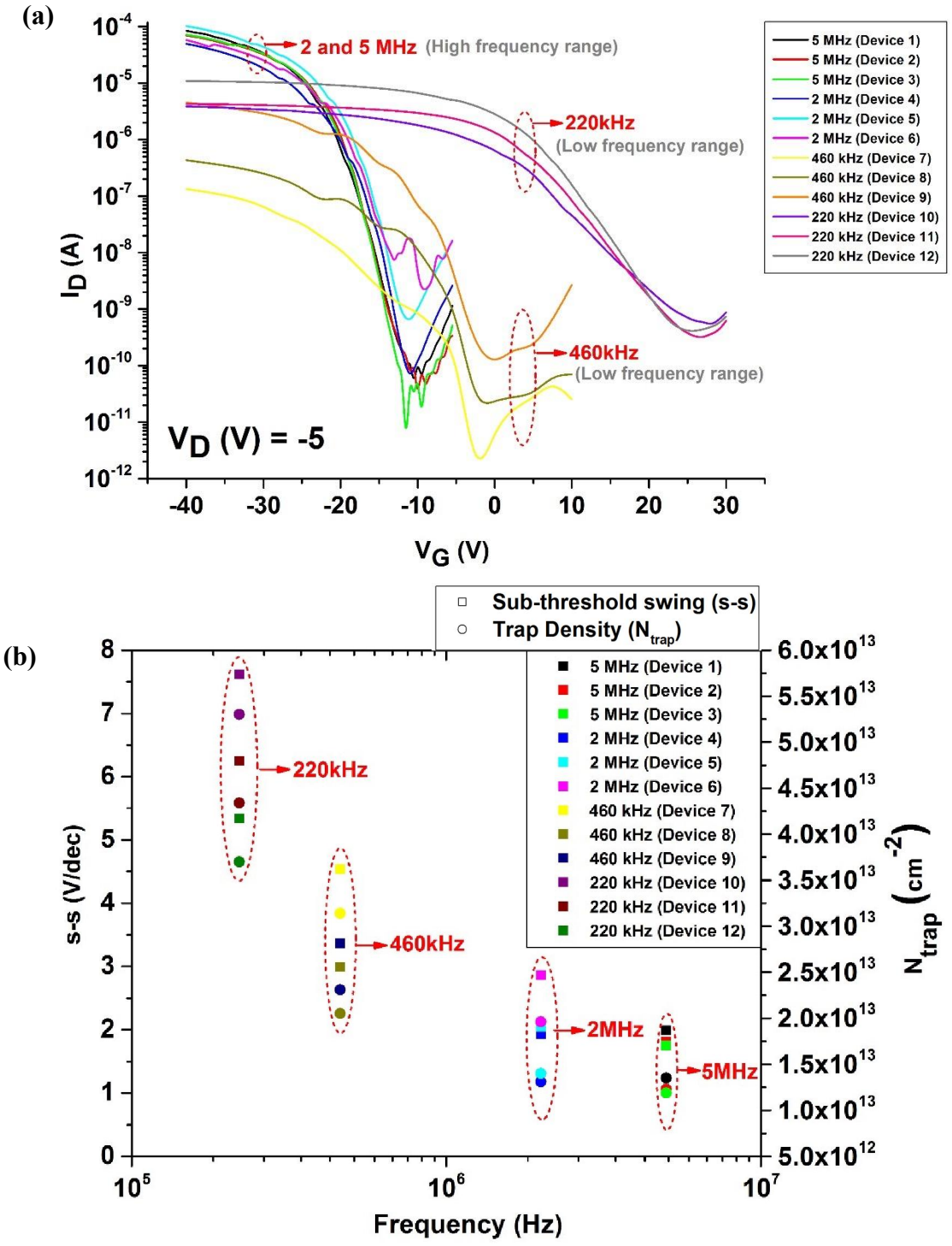


Figure S6. Typical behaviour of Si NW FET devices with NWs aligned using dielectrophoresis, at 220 kHz, 460 kHz, 2 MHz and 5 MHz, 10 Vpeak-to-peak, sinewave. Three devices are shown for each DEP frequency. (a) Transfer characteristic of the Si NW FETs used for the extraction of sub-threshold swing (s-s). (b) Sub-threshold swing (s-s) and surface trap density (N_{trap}) *versus* frequency (Hz) for the devices shown in (a).

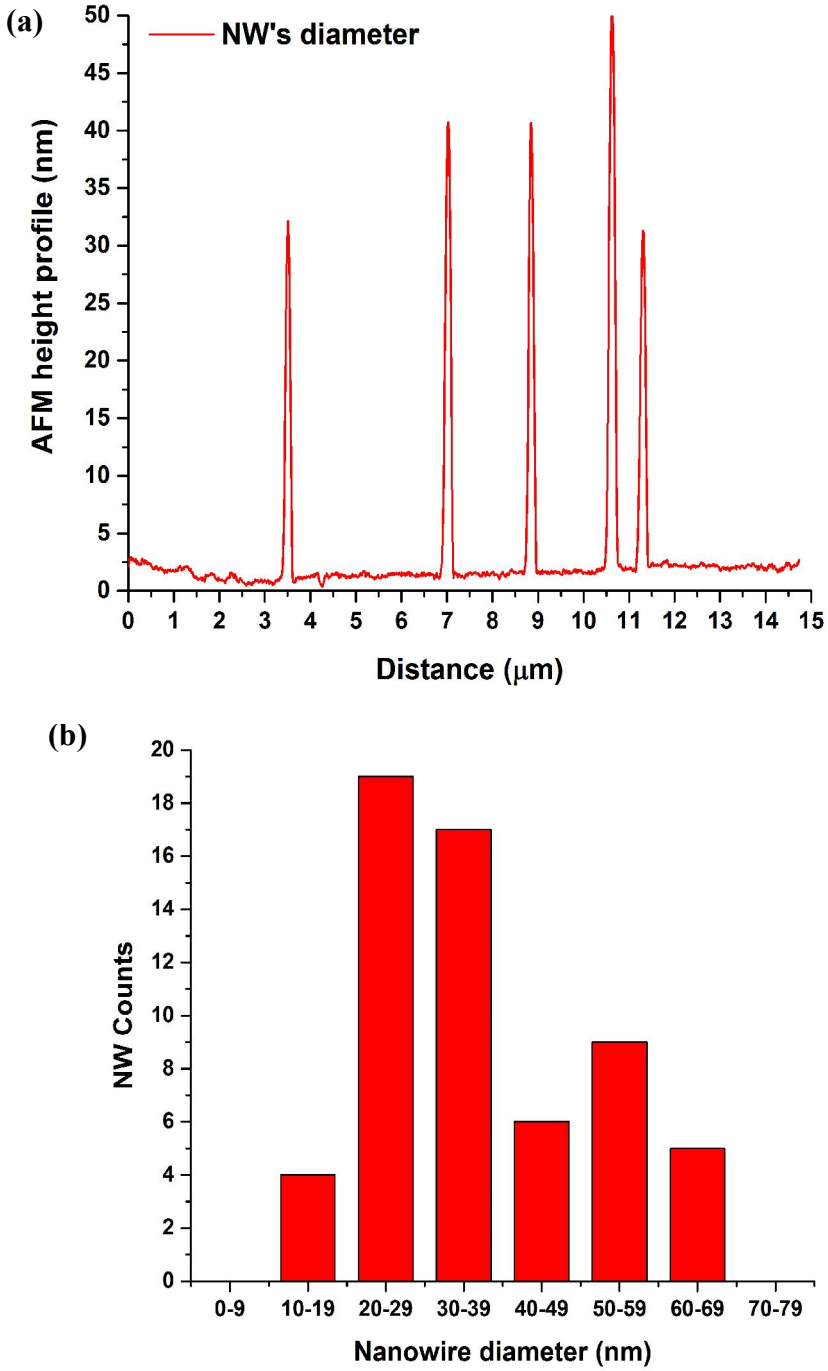
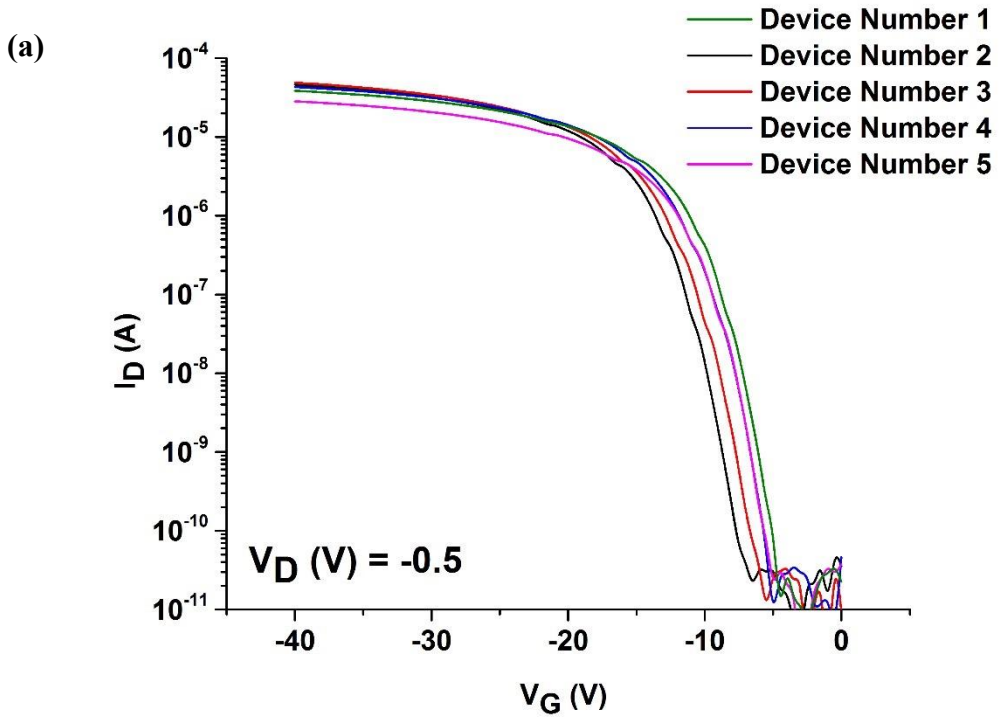
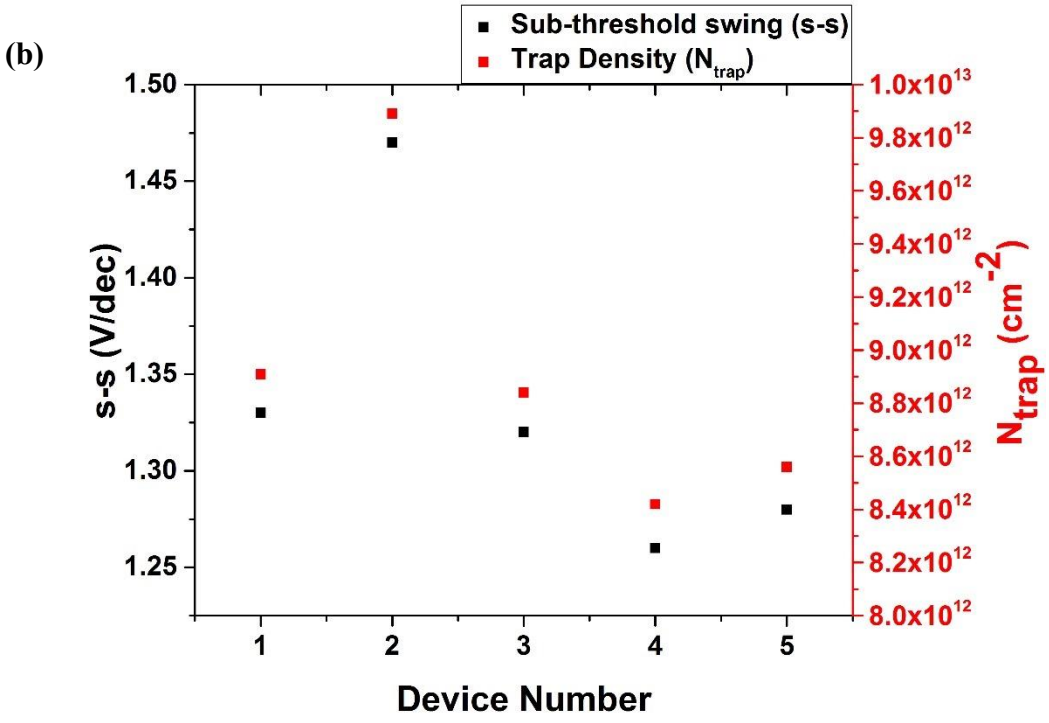


Figure S7. (a) Atomic Force Microscope (AFM) cross-sectional image of the FET device, taken approximately in the middle of the channel area, showing 5 NWs. AFM tip movement is parallel to the edge of the electrode, being perpendicular to the NWs in the FET channel. AFM image gives direct measurement of the NW diameters.

(b) A summary of AFM profile scans of 50 NWs in the FET channels. The graph shows the number counts of a range of NW diameters that was observed. An average diameter on 30 nm was used for the mobility calculations.

The following two pages are related to Fig. S8





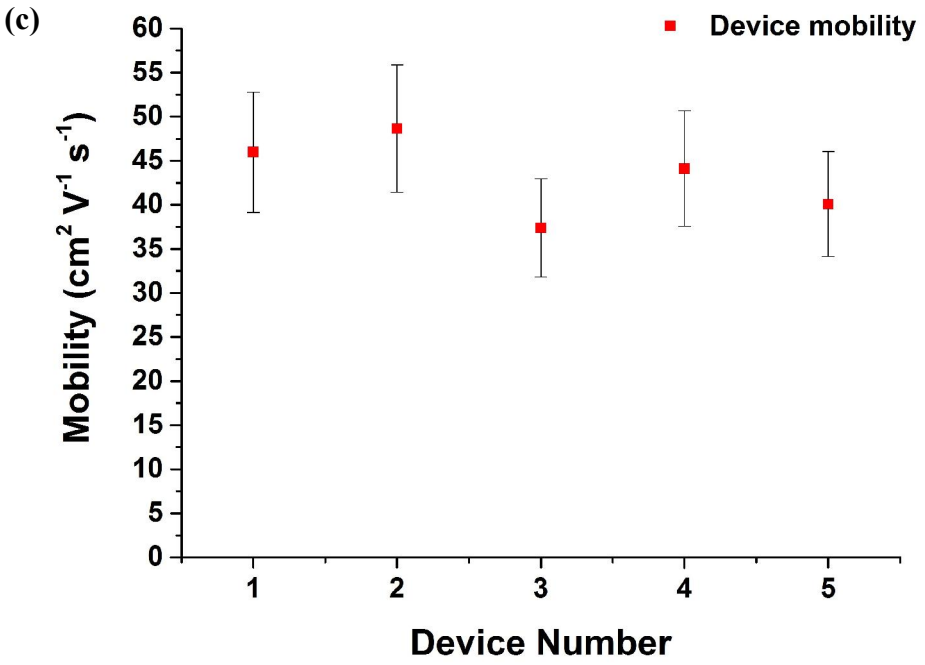


Figure S8. Reproducible behaviour of Si NW FET devices aligned using the same dielectrophoresis parameters, at 20 MHz, 10 Vpeak-to-peak, sinewave. (a) Transfer characteristic of the Si NW FETs used for the extraction of sub-threshold swing (s-s). (b) Sub-threshold swing (s-s) and number of traps (N_{trap}) *versus* frequency (Hz) from the devices shown in (a). Trap density is calculated using Eq. 7. (c) Device mobility calculated using Eq. 8-9 of the devices shown in (a).

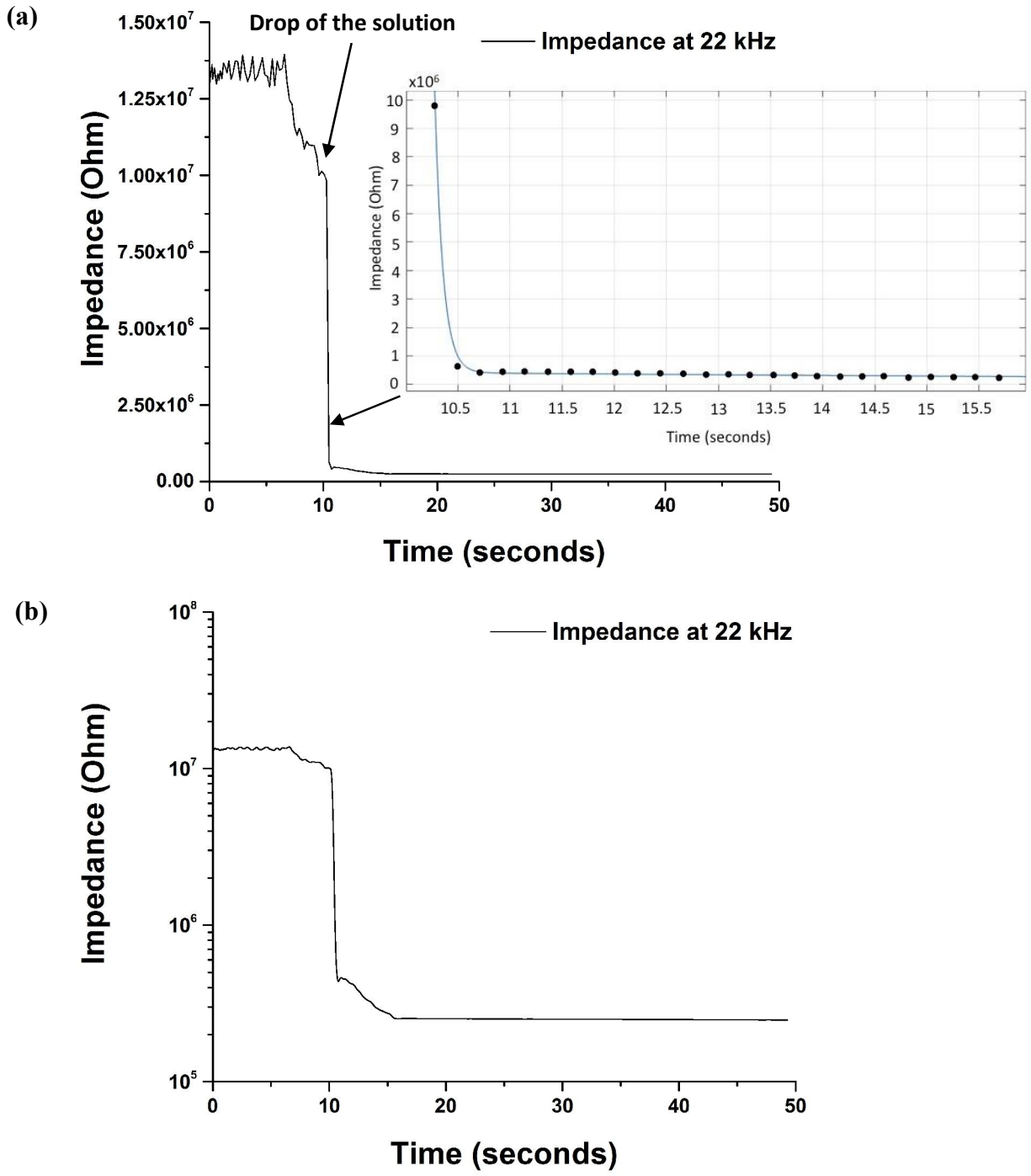


Figure S9. Plot of impedance as a function of time at DEP signal 20 Vpeak-to-peak, 22 kHz, sinewave. (a) Impedance drop indicates the assembly of the semiconducting NWs between the device electrodes. Fast drop of the impedance occurs after the placement of NW dispersion on top of the DEP contacts. Inset: a MATLAB fit of an exponential decay, giving fast decay time constant (τ) of 21 s^{-1} at 22 kHz. (b) Log-linear representation of the same impedance drop, showing fast exponential decay between 10 and 11 seconds on the time scale. This decay is responsible for the 98% of the total impedance drop. Slow-varying impedance decay (t = 11s-15s) contributes to only 2% of the total impedance drop.