UNIVERSITY OF LIVERPOOL

DESIGN AND TESTING OF ORGANIC DEVICES FOR CIRCUITS

Thesis submitted in accordance with the requirements of the University of Liverpool for the degree of Master of Philosophy by

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Abstract: Design and Testing of Organic Devices for Circuits

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As the success and scope of organic electronics increases, there is a pressing need, and valuable potential, in ensuring the technology is available to make organic circuits that can be fully integrated. Integrating output and control technologies allows for simpler product manufacturing processes and opens up the possibilities for applications which may have in the past been restricted (such as use of flexible substrates). Due to the increased complexity of organics evolving from devices into circuitry, there are a number of factors to take into account and familiarity with all steps towards the final aim allows for more conscientious design.

The aims of this study were to consider and implement a range of stages between basic organic device fabrication and analysis through to a simulation circuit design for an organic dynamic shift register. This range of investigation created a wider field of understanding, as it considers not only the final circuit design but all of the building blocks needed to reach this stage, highlighting how all of these link together. Exploring the distribution possibilities as well as a newly introduced Two Condition Theory not only proposes answers to some of the uncertainties regarding organic semiconductor transport, but provides a firm foundation for the theoretical process that leads to the parameters used in further stages of the circuit design. In order to do this, existing current models for both the disordered and polycrystalline current equations were modelled with parameters extracted from devices made within the project.

As the physical restrictions in terms of the sensitivity of organic semiconductors have a crucial impact on the performance of organic circuitry, a further aim was to fabricate and understand the processing methods for organic devices using a new polycrystalline material, Lisicon™ S1200. This was necessary for producing samples that were modelled using the theoretical analysis and also gave valuable understanding of the physical considerations when completing circuit designs. This practical experience was extended to the production of devices with the aim of studying scaling implications relative to those faced in the silicon industry. Various tests were performed including the variation of semiconductor, aluminium oxide and organic dielectric thickness with the results analysed and compared. Finally, a dynamic shift register was designed and simulated for two different

configurations of inverter using model parameters based upon the theoretical and practical work of earlier chapters. These were compared, and a final mask design was created incorporating all of the previous stages

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Nan, this is dedicated to you and your love that brought me to Liverpool.

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List of Symbols

a	grain size	m
A	area	m^2
C_0	capacitance per unit area	Fm^{-2}
C_T	total capacitance	F
C_i	capacitance per insulator unit area	Fm^{-2}
C_{ox}	capacitance of oxide	F
$C_{surface}$	capacitance of semiconductor	F
c	constant in carrier concentration expression	
C_g	gate capacitance	F
C_{gd}	gate-drain capacitance	F
C_{gs}	gate-source capacitance	F
C_L	load capacitance	F
c_{diff}	exponential mobility parameter for diffusion	
c_{drift}	exponential mobility parameter for drift	
D_D	dielectric displacement of dielectric	Cm^{-2}
D_S	dielectric displacement of semiconductor	Cm^{-2}
E	Energy	eV
E_F	Fermi level	eV
E_{MN}	Meyer-Neldel energy	eV
E_X	energy level at placeholder point x	eV
E_a	Activation energy	eV
E_z	energy in field z	eV
E_θ	energy at which maximum L1 DOS occurs	eV
EAJ	code for organics model file in Cadence	
E_{Fom}	Fermi level for Ohmic metal	eV

E_{Fosc}	Fermi level for organic semiconductor	eV
E_{Fsm}	Fermi level for Schottky metal	eV
E_{FVapp}	Fermi level after voltage applied	eV
E_i	intrinsic Fermi level	eV
E_T	mobility edge – minimum energy at which carrier transport is observed	eV
E_{vac}	vacuum energy level	eV
F	field	Vm^{-1}
$F(\phi)$	field in terms of surface potential	Vm^{-1}
F_D	field applied to dielectric	Vm^{-1}
F_S	field applied to semiconductor	Vm^{-1}
F_{xmean}	average field at particular depth of channel	Vm^{-1}
F_y	field in y direction	Vm^{-1}
F_z	field in direction z of polycrystalline grain	Vm^{-1}
$f(E)$	Fermi-Dirac distribution	
$f_{mb}(E)$	Maxwell Boltzmann distribution	
H_{diff}	diffusive carrier flux	$m^{-2}s^{-1}$
H_{drift}	drift carrier flux	$m^{-2}s^{-1}$
I	current	A
I_D	drain current	A
$I_D(t)$	drain current with respect to time	A
I_{drift}	drift current	A
$I_{driftunsat}$	drift current in unsaturated region	A
I_{lin}	current in linear region	A
I_{sat}	saturation current	A
i_c	charge current	A
I_d	discharge current	A

is	model parameter for leakage current is	A
J	current density	Am^{-2}
J_1, J_2	current density at points 1 and 2	Am^{-2}
K	universal mobility law parameter constant	AV^{-m}
k	Boltzmann's constant	eVK^{-1}
K_{c1}, K_{c2}	mobility parameter constant	AV^{-m1}, AV^{-m2}
K_{diff}	constant mobility parameter for diffusion	AV^{-cdiff}
K_{drift}	constant mobility parameter for drift	$AV^{-cdrift}$
L	length	m
$L1(E)$	Laplace 1 distribution	
L_D	Debye Length	m
L_D	length of driver channel	m
L_L	length of load channel	m
L_{OV}	overlap of source/drain contact with gate	m
m_{c1}, m_{c2}	mobility parameter exponential	
m	universal mobility law parameter exponential	
$N'(0)$	rise in density of states at point E = 0	$cm^{-3}eV^{-1}$
$N'(E)$	rise in density of states	$cm^{-3}eV^{-1}$
$N_1(0)$	base level density of states at reference point 0 in L1 DOS	cm^{-3}
N_C	density of states at conduction band	cm^{-3}
N_{max}	density of states at maximum point of L1 DOS	cm^{-3}
N_{sub}	donor ion concentration	cm^{-3}
$N(E_\theta)$	density of states at energy E_θ of L1 DOS	cm^{-3}
$N(E)$	Density of states at energy E	cm^{-3}
n	carrier concentration	cm^{-3}
$n(\phi)$	carrier concentration in terms of surface potential	cm^{-3}
n_1	carrier concentration in branch 1 of L1 DOS	cm^{-3}

n_2	carrier concentration in branch 2 of L1 DOS	cm^{-3}
n_i	intrinsic carrier concentration	cm^{-3}
p_0	carrier concentration in flat band condition of polycrystalline material	cm^{-3}
q	electron charge	C
$q\varphi_{drain}$	work function energy of drain	eV
$q\varphi_{gate}$	work function energy of gate	eV
$q\varphi_{om}$	work function energy for Ohmic metal	eV
$q\varphi_{osc}$	work function energy for organic semiconductor	eV
$q\varphi_{sm}$	work function energy for Schottky metal	eV
$q\varphi_{source}$	work function energy of source	eV
qX	electron affinity	eV
Q_0	charge per unit area	Cm^{-2}
Q	total charge	C
R_P	resistor	Ω
t	time	s
T	Absolute temperature	K
T_0	characteristic temperature describing energetic distribution of carriers	K
T_C	characteristic temperature describing distribution of traps	K
T_1, T_2	transistors 1 and 2 in inverter	
T_D	driver transistor	
t_{osc1}, t_{osc2}	thickness of semiconductor at 2 different thicknesses	m
t_{OSCG}	thickness between semiconductor and gate	m
t_{OSCOX}	thickness between semiconductor and oxide	m
t_{OXG}	thickness between oxide and gate	m
T_P	pass transistor label	m

t_{SDG}	thickness between source/drain contacts and gate	m
t_{SDOX}	thickness between source/drain contacts and oxide	m
t_{OTFT}	thickness of oxide in OTFT	m
v	velocity	ms^{-1}
V_{bi}	built in voltage potential	V
V_C	dynamic clock pulse voltage	V
V_{DS}	drain-source voltage	V
V_F	applied forward voltage	V
V_G'	difference of gate and threshold voltage	V
V_{GD}	voltage at gate of driver transistor	V
V_{GS}	gate-source voltage	V
V_{in}	input voltage	V
V_R	applied reverse voltage	V
V_{SP}	voltage applied to source of pass transistor	V
V_T	threshold voltage	V
V_{T0}	model parameter for threshold voltage	V
W	width	m
W_L	width of load channel	m
W_{acc}	width of accumulation region	m
W_{dep}	width of depletion region	m
W_{depFB}	width of depletion region in forward bias	m
W_{depRB}	width of depletion region in reverse bias	m
X	constant property	
ε_b	relative permittivity of material	
ε_{ox}	permittivity of oxide	Fm^{-1}
ε_{sil}	relative permittivity of silicon dioxide	
ε_{OTFT}	relative permittivity of oxide of organic OTFT	

ϕ_B	potential of bulk material	V
ϕ_S	surface potential	V
μ	mobility	$cm^2V^{-1}s^{-1}$
μ_0	effective mobility parameter	$cm^2V^{-1}s^{-1}$
μ_{FE}	Field effect mobility	$cm^2V^{-1}s^{-1}$
μ_{eff}	effective mobility in terms of Universal Mobility Law	$cm^2V^{-1}s^{-1}$
λ_m	minimum feature size	m
β	aspect ratio	
γ	ideality factor	
ε	permittivity	Fm^{-1}
ρ	carrier density	cm^{-3}
ϕ	potential	V
ϕsp	surface potential variation	V

Chapter 1 INTRODUCTION

1.1 Background and Introduction

Rising through the ranks of electronics from an obscure discipline of publishing no more than 12 papers in 1993[1] to a predicted multibillion[2] dollar industry by the end of the decade, the Organic Electronics industry has now swollen into vastly diverse areas ranging from photovoltaics[3][4]to large area structure light emission.[5]–[8] As the possibilities grow, so does the need to keep the costs low and, subsequently, the circuitry used to drive them [9][10]. This is an ambition that organics is well equipped to handle due to its versatile advantages. These include its ability to be manufactured on flexible substrates and the photovoltaic and organic light emitting diode (OLED) potential of the materials. The industry could be developed to produce cheaper, flexible applications that would be a lot harder and more expensive to produce with silicon technology[11]. At the beginning of 2011 the first organic microprocessor was developed by IMEC[12], a processor that currently has the speed of an equivalent 1970s silicon processor. Despite this being a relatively low speed compared to the processors that dominate the industry, it is the first major step in consumer organic electronic circuitry. MIT have also published a paper about the implementation of a mixed-signal organic integrated circuit showing the development of organic electronics expanding into mixed signal circuitry[13]. If circuit technology is improved, integrated organic electronic circuits can have significant impact, particularly if thin film rechargeable batteries[14]and UHF antennas can be integrated on larger area flexible substrates [15]. Such technology involves the use of Organic Thin Film Transistors (OTFTs) [16].

Organic Electronics has the potential to implement circuitry that cannot be achieved easily with other technologies and therefore expand the possibilities for the future of the worldwide electronics industry[17]. One of the main benefits of electronics is the large area production for relatively low costs[18]. For this reason, more work is being put into the design and production of organic circuits and the additional benefits that organics could bring to a product if it was possible to implement.

In order to be able to design robust and reliable circuits across the board, it is becoming increasingly important to develop accurate models that can represent organic devices for integration. Although similarities exist with Organic TFTs, the difference in structure and transport mechanisms of silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [19] yield different current models. There are still disputes over the exact processes involved in organic transport as the level of disorder makes it harder to predict behaviour. Studying the behaviour of individual devices allows for more comprehensive understanding of how the devices, and subsequently the circuits, will function under certain circumstances.

One of the factors highlighted as a hindrance to good performance of processors and more complex circuitry is the low mobilities. Although mobilities[20] have seen improvement over the years, the mobility values are still much lower than that of silicon which yield a much lower frequency response and therefore seriously hinder the speed of switching. In order to counteract the issues of these slow mobilities, alternative methods of enhancement can also be considered. Silicon was able to achieve unrivalled success in the electronics industry and this was governed by a statement by Moore[21] about the doubling of the number of transistors on a chip. For that reason, another point of interest now that the technology is improving is the potential for scaling down devices. In order to do this however, a thorough understanding is needed of the limitations that could be encountered.

1.2 Thesis Organisation

This thesis is structured around the stages involved in developing a good enough understanding of organic materials and devices in order to produce a design for an organic dynamic circuit. In this case, an organic shift register.

1.2.1 Chapter 2 – Materials and Modelling

Chapter 2 looks at the basic principles behind organic materials and the differences between the polycrystalline and disordered materials used in the development of current models. It focuses especially on the modelling methods for the way the current behaves within both diodes and thin film transistors. As organic materials do not exhibit the predictable behaviours of their silicon counterparts, statistical analysis is needed to produce accurate models. So far the distributions used are either a Gaussian distribution or an exponential justified by an assumption that conduction takes place within the band tails of the Gaussian. This chapter considers the possibility of using an alternative Laplace 1 distribution and how this can be approximated to the exponential model to develop both the disordered and polycrystalline alternatives. It then aligns this with existing models that can be used for parameter extraction and tested by practical results in Chapter 3 and subsequently used for simulations in Chapter 5. Expanding this theory further, a Two Condition Theory is introduced to explain the occurrence of two characteristic temperatures, T_C and T_O, that have been known to occur in diode results and suggests the energy band behaviour that causes this to occur. This chapter also looks at the functionality of particular organic devices and how these can be used for producing current models. It also discusses the phenomenon known as the universal mobility law and why, using the concept of mobility for organic materials is thought to be more of an effective parameter rather than a physical one.

1.2.2 Chapter 3 - Fabrication and Characterisation of Devices

Chapter 3 considers the processing steps involved in producing diodes, transistors and capacitors. The stages of the fabrication process are detailed for both diodes and transistors along with the device structure and any observations that occurred during the process. Two different techniques are detailed for the TFT as these were both used in the project. The differences are noted, highlighting the benefits of particular fabrication processes. Different TFT structures are also discussed and diodes characterised for both a polycrystalline and disordered material. This chapter also looks at the methods of extracting parameters and uses these to test the models featured in Chapter 2. It also discusses some of the processing challenges and results that were experienced during the experimental stages including hysteresis, contact resistance and source/drain material.

1.2.3 Chapter 4 – Scaling

This chapter looks at the benefits of scaling devices and the success that it has been evidenced by throughout the history of electronics. It considers the scaling rules for silicon and the implications of these for organics with respect to how the structure of the devices differ for each technology. This gives an indication of which of these rules organics could obey and follows through some of the analysis to see if the rules still hold. It also contains experimental evidence based on the results from devices made with the methods detailed in Chapter 3 but with process changes to adjust the thicknesses of oxide and semiconductor layers. These results are then related to the theoretical predictions about scaling impact made earlier in the chapter.

1.2.4 Chapter 5 – Circuit Design

This chapter focuses on the response to the benefits of CMOS and the possibility of implementing similar designs without the ability to combine p and n type devices within the same circuit. It considers the possibility of pseudo-CMOS and looks at two different configurations of inverter – the enhancement mode saturated load inverter and the pseudo-CMOS inverter in order to assess this. Chapter 5 also does basic tests on dynamic pass transistor simulations and uses the parameters extracted in Chapter 3 based on the model analysis from Chapters 2 to reflect the devices used in the project. These are also used to simulate the inverters and subsequently the shift register designs for each configuration in order to consider the use of organic parameters. The two shift registers are compared and a mask design for one of the configurations is then designed and detailed in order to study the circuit fabrication process involved and the rules that must be taken into account. This unites the three major stages of theoretical derivation, experimentation and simulation into a practical design.

1.2.5 Chapter 6 – Conclusions and Further Work

This chapter looks at the project as a whole and the steps that can be taken next.

1.3 Contributions

This thesis contributes the step by step process of analysing organic devices in the context of carrier transport behaviour based on density of states distribution and considers a new concept of whether this distribution can shed light on the behaviour of organic Schottky diodes. This introduces the Two Condition Theory based on the relative position of the Fermi level, E_F, and mobility edge, E_T. The characterised results from the practical work detailed in Chapter 3 are used to test the viability of the models discussed in Chapter 2 and compare the polycrystalline and disordered form in relation to a new Lisicon™ polycrystalline material. As this is a relatively new material that is still under development there is very limited characterisation published on Lisicon™ S1200 and these are the first results to be studied with these models and fabrication process. There is limited information on scaling of organics, and while this study was more of an overview, the results from the tests performed show a trend in line with theory developed from the new equation models. This comparison against a silicon backdrop has not been significantly published. Finally, this project looks at a multi-stage process of development including theoretical, experimental and simulation analysis and combines all three into a final shift register design. This produces a step-by-step process covering all three major bases and combining these as necessary delivering a wider context to all stages involved rather than focussing solely on theory, practical or simulation. While the techniques were learned from within the research group and early stages done with support of colleagues, all of the models derived and devices fabricated were done so within the project, by the author. This also applies to the simulations and mask designs. This scope is generally not applied within a single project, especially including the proposal of a new distribution model and with a new material.

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Chapter 2 MATERIALS AND MODELLING

2.1 Introduction – Importance of materials understanding for modelling of devices

Regardless of the complexity in a circuit, be it a basic operational amplifier or a system as complex as a processor, the elements of the circuit can be broken down into individual devices. Once individual devices are studied and understood down to an atomic level, the behaviour of these devices can then be predicted (with varying degrees of accuracy) in order to simulate the more complex circuit designs as effectively as needed. Without a coherent understanding of how devices work, it would be impossible to generate the level of accuracy needed to represent the current and small signal capacitance voltage characteristics which can then be applied to a multi-device structure.

As discussed in the Introduction, organic technology relies on utilising the semiconductor properties of materials made with either conjugated polymers[1]–[3] or a number of small molecule strings that are stacked together[4]–[8]. These materials are deposited within an electronic device structure and, on the simplest level, the reaction that takes place at the metal to organic semiconductor (OSC) interface either hinders or facilitates flow of carriers producing a state of operation for the device.

In order to understand how carriers will behave, the inherent structure of these materials is important. In an ordered crystalline structure, a lattice can be formed on the basis that atoms connect adjacently with strong covalent bonds[9]. This periodicity forms bonding of atoms from atomic orbitals in which electrons can sit, and the different strength of bonding determines the energies of the orbitals[10]. This combined with De Broglie's wave function determines the momentum of electrons and therefore kinetic energy of electrons. Combining these factors with potential energy gives rise to discrete energy levels for each electron. It can be assumed that the number of atoms is so large within the structure that discrete energy levels merge to form bands. The materials being considered for the purpose of this project do not have this level of order and therefore the transport mechanisms that have been used in technologies based on crystalline structures are not applicable other than for approximation and comparison. As being able to understand transport mechanisms in materials is crucial for producing the aforementioned equations, thorough understanding of these alternative materials is needed to minimise errors at circuit design and production level when reduction of time and cost is a necessity.

2.2 Disordered Materials

In disordered materials, gaps in potential energy prevent certain energies from being achieved. Highly disordered materials are formed through weaker Van der Waal bonds rather than the stronger covalent bonds and conduction is controlled by highly localised orbitals[11]. The bonding of the carbon-based atoms stems from the hybridisation of orbitals forming overlaps either constructively or destructively.[12] This produces equivalent energy levels to those of crystalline structures (though not continuous) with the conduction band minimum being equivalent to the Lowest Unoccupied Molecular Orbital (LUMO) and the valence band maximum being equivalent to the Highest Occupied Molecular Orbital (HOMO). These vacant energies form 'traps' which trap electrons that cannot contribute to conduction. These traps prevent the continuous band theory from being applicable.

2.3 Polycrystalline Materials

Polycrystalline materials, as the name suggests, are materials that are formed of many crystallites (or grains) but still have a level of disorder at the point where the grains connect together (the grain boundaries). Within the grain there is a level of order, however, conduction is restricted by the highly disordered grain boundaries because of phenomena such as Fermi level pinning[13]–[15] which will be explored later in this chapter. For practical scope of this project, the polycrystalline material Lisicon™ S1200 has been used. This is a material based on acene chemistry – the synthesis of polycyclic aromatic hydrocarbons with fused benzene rings[16] and is a small molecule OSC. An example of an equivalent material of this type would be pentacene where five of these benzene rings form a small molecule string.

2.4 Density of States

In order to understand conduction through semiconductors it is important to be able to have as accurate an idea as possible of the energy distribution of electrons so that the number of conducting carriers can be estimated. As it is not possible to know the exact energy state of an electron at a specific moment in time, statistical relationships must be considered to obtain the most likely scenario as a basis for calculation. As different states are generated for different energy levels (determined by the wave equation) there are certain states that do not exist (such as those in the forbidden gap) and therefore cannot be occupied by carriers. Primarily, the Density of States (DOS) represents the number of states that can be occupied and therefore, when combined with a distribution function, the number of occupied states can be calculated.

Although the DOS represents the states over certain energies; this information is only useful for carrier concentration when combined with the probability that each of those states is occupied. Combined theory from Fermi and Dirac led to a probability distribution function[17] *f(E)* which states that:

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)}. \qquad \textit{Eqn. 2.4-1}$$

In Eqn. 2.4-1, *E* represents the energy level that the probability of occupation is being determined for, E_F the Fermi level (level at which probability of occupation is 0.5), *k* is Boltzmann's constant and *T* is temperature in Kelvin. *f(E)* was plotted with an arbitrary Fermi level set at 0.8 eV, for 2 temperatures: 0 K and 300 K. This shows that the occupation probability is related to temperature. At 0 K the function is shown by the dotted blue line in Figure 2.4-1 and clearly no energy levels above the Fermi level are occupied by carriers – the probability of occupation is 0. The distribution at room temperature of 300 K is plotted with the red line and shows that as temperature increases, more of the carriers can be excited into higher energy bands and the probability of occupation increases.

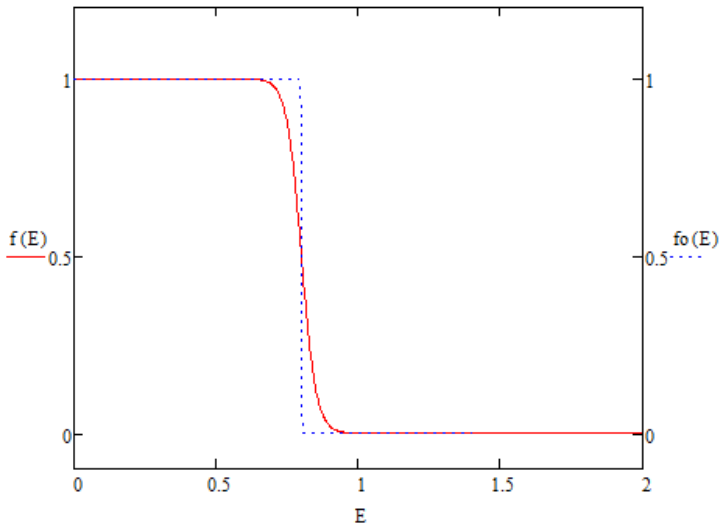

Figure 2.4-1 Plot of f(E) at T > 0 K as marked by the Red, solid trace and f_0(E), f(E) at T = 0 K marked by the blue, dotted trace. f_0(E) has a step-like shape as no electrons are excited above the valence band and into higher states where they can conduct. When the temperature is above 0 K, some electrons can be excited into conduction band and the distribution begins to indicate the presence of electrons above the Fermi Level and presence of holes below. .

Analysis corresponding to energies within a certain range of the Fermi level must be represented by the Fermi-Dirac distribution, however, if only energies greater than a few *kT* above the Fermi level are

to be considered then this distribution can be assumed to follow the simpler distribution derived by Maxwell and Boltzmann which states:

$$f_{mb}(E) = \exp\left(-\frac{E - E_F}{kT}\right). \qquad \textit{Eqn. 2.4-2}$$

As can be seen in Figure 2.4-2, this is because at these energies the distribution follows the same form as *f(E)*.

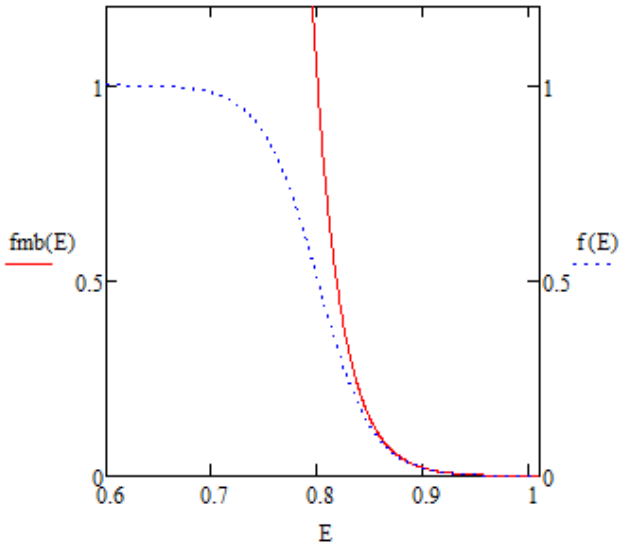

Figure 2.4-2 Maxwell Boltzmann distribution, $f_{mb}(E)$, plotted against the Fermi-Dirac Distribution. Both traces follow the same pattern at energies that are more than kT above the Fermi level.

Combining this relationship with an appropriate distribution of DOS provides information regarding the carriers that are contributing to conduction. If it is assumed that any carriers within a certain energy range are conducting and therefore contributing to the current flow, the value for *n* - the carrier concentration - can be determined as shown in Eqn. 2.4-3. For this general equation, the limits are set at infinity and some lower level E_X below which carriers would not be contributing to conduction. In this circumstance, E_X is just a placeholder energy to represent a lower limit that would be dependent on the distribution chosen.

$$n = \int_{E_x}^{\infty} N(E).f(E)dE \qquad \textit{Eqn. 2.4-3}$$

The DOS, represented as *N(E)* in Eqn. 2.4-3, and what kind of distribution the DOS has, is a subject with varying theories. It is a common assumption there is a Gaussian distribution of the DOS; as probably the most widely recognised theory, many models are based on this. Some experiments however have been based around an exponential distribution of states, one of the most pertinent being by Vissenberg and Matters[18] to facilitate the theory of hopping models. This paper used the assumption that the energy is sufficiently lower than the Fermi level which gives the grounds for assuming an exponential distribution based on the energy levels concerned only occurring in the band tails. It states that this breaks down should the temperature become higher than a characteristic temperature, T_0, which represents the width of the distribution. The paper derived an Arrhenius-like behaviour for the conductivity where there was a dependence on an activation energy E_a; this ratified the use of the exponential model based on the evidence in that hopping in exponential DOS models can be described by an activation energy. Another alternative distribution, that does not have a strong presence in papers but is used by Horowitz *et al.*[19] in order to develop the theory of multiple trapping and release models, is the double exponential distribution; a distribution that follows the path of two exponential places back to back. This will be explored further in Section 2.6.2.

In contrast to both of these ideas, papers suggesting a universal law linking mobility dependence of charge carriers and temperature have been modelled with a Gaussian distribution [20], [21]. Pasveer *et al.* indicates experimental support for a Gaussian distribution [1] backed up through experiments done by Bässler[22] amongst others. Pasveer's model for a Gaussian distribution has also been used in the very recent development of Meyer-Neldel dependence found by Fishchuk *et al.*[23]–[25] and Ullah *et al.*[26] There will no doubt be further debate on the distributions involved in carrier transport mechanisms and how this affects the mobility in organic materials.

2.5 Meyer Neldel Energy

There has been much debate on the processes involved in charge transport for organic materials of different levels of disorder and which transport processes dominate conduction. A clear recurrence in the literature is the universal mobility law (UML). In 2005 Pasveer gave evidence for a unified description for charge-carrier mobilities[20], furthering Bässler's proposal that there was a dependence of the mobility on the electric field and temperature[27]. Tanase *et al.* demonstrated the

dependence of mobility on carrier concentration[28]. This theory came from the differences in diode and TFT mobilities, the significance of the difference implying a link corresponding to the major difference – carrier density. This dependence on density, however, seems to be relative to temperature as at low temperatures the field energy is more dominant, implying more of a drift dependency rather than diffusive. Pasveer[20] developed an expression for the current density derived using the Fermi-Dirac distribution along with the Mott-Gurney law to produce an expression that fits well with temperature dependence as well as with previous work done by Tanase. This was further backed up in another paper by Pasveer [2] providing further evidence for a relationship between mobilities, temperature, electric field and carrier charge density highlighting the deviation from an Arrhenius dependence of mobility and suggesting that the dependence can be explained by a dependence on a Gaussian disorder.

Developing this further, Meijer linked this dependency of mobility on the temperature and gate voltage, stating that this was a key difference with silicon materials[29] and the band-like transport that could be assumed in such cases. Drawing on the theory that in disordered, or partially disordered, materials localised states control the transport (as shown by Vissenberg and Matters[18]), Meijer highlighted the models of trapping, hopping and Coulomb blockade giving possible descriptions for explaining transport. These implied a relationship caused by a common factor: the gate voltage dependency of the activation energy. He explained this in terms of a general property, *X*, governed by thermally activated behaviour shown in Eqn. 2.5-1.

$$X = X_0 \exp\left(\frac{-E_a}{kT}\right) \qquad \textit{Eqn. 2.5-1}$$

This meant that when temperature is the cause of activation, the property follows an exponential relationship in terms of the temperature and Boltzmann's constant with a prefactor multiplier, X_0, that also changes and increases exponentially with the activation energy E_a. He then stated that the relationship between this E_a and prefactor X_0 increased exponentially based on the Meyer Neldel (MN) energy, E_{MN}.

$$X_0 = X_{00} \exp\left(\frac{E_a}{E_{MN}}\right) \qquad \textit{Eqn. 2.5-2}$$

This means that after combination, the exponential factor to determine the thermally activated property could be made up of two energies:

$$X = X_{00} \exp\left[-E_a\left(\frac{1}{kT} - \frac{1}{E_{MN}}\right)\right], \qquad \textit{Eqn. 2.5-3}$$

and thus that the energy at which activation occurs could be determined by the MN energy.

This analysis in the context of the Meyer Neldel Rule (MNR) applied to the field effect mobility for pentacene shows how the relationship shown in the mobility of TFTs possibly explains the origin of the MNR. There is an overwhelming correlation between conduction and the MN energy with conflicting theories on what the MN energy really is[26] and how it can be extracted and used in order to model carrier transport, but this could be key in settling the conflict over the state distribution, and used to improve understanding of device behaviour.

Using the general equation for mobility in Eqn. 2.5-4, Meijer's study further reported an experiment calculating field effect mobility, μ_{FE}, at various temperatures from low to high T and plotted it against the inverse temperature.

$$\mu_{FE} = \frac{L}{WC_iV_{ds}}\frac{\partial I_{ds}}{\partial V_{gs}} \qquad \textit{Eqn. 2.5-4}$$

Here, *W* and *L* are the channel width and length respectively, C_i is the capacitance of the insulator per unit area, and I_{ds} and V_{ds} are the drain-source current and voltage respectively and V_{gs} is the gate-source voltage. There is a clear point of intersection of all of the mobilities which provides the common crossing point that all activation energies pass through. From this, the prefactor for different activation energies can be calculated by plotting on a log scale and calculating the gradient in order to find the MN energy. Comparing this method with other literature results, it held true that the E_{MN} was always in a range of 35 – 43 meV, and centre on ~40meV.

Yelon showed that the relaxation frequency being exponentially dependent on activation energy lead to physically unreasonable values having to be calculated for the frequency for hopping in order to produce a reasonable prefactor[30]. Additionally, Meijer highlighted that the occurrence of the MNR was too general to be attributed solely to exponential DOS models as would be suggested. It was therefore proposed that multiple hopping steps were needed such as in the case when the activation energy is much higher than the phonon energies. This followed the theory that as activation energy increases, the number of paths to reach the higher energies increases. Yelon also explains that in phonon assisted electron hopping the electron is more likely to meet many small phonons rather than

one large phonon to provide the energy and therefore adding up many energies will provide a larger energy overall. This could generally explain the unfeasible prefactors needed to support a single phonon model. If this behaviour was exponential then MNR can be proven. This would also follow the theory that at higher energies there are many paths possible, i.e. MN only holds when large activation energies are needed. If there is a temperature dependence proven then this would explain the varying behaviours at low and high temperatures, as mentioned previously.

Meijer's work is heavily supported by the work of Ullah *et al.*[26]and Fishchuk *et al.* in various papers [23]–[25],

2.6 Carrier Concentration Derivation

For the purpose of this thesis, there are two DOS distributions that will be suggested for the carrier concentration. These are the exponential distribution as an estimation of the Gaussian band tails, and the aforementioned double exponential used by Horowitz [19]. Another name for this is the Laplace 1 distribution of states (L1DOS). The grounds for introducing this is to propose analysis that could better explain the role of the MN energy found in the aforementioned studies, however all analysis will be based upon the exponential model.

2.6.1 Exponential Distribution Theory

In order to find the carriers that are free to conduct, the rate of change in DOS, *N'(E)* is needed as this is an indicator for the probability that a carrier can occupy higher energy levels. For ordered materials, this can be represented by an exponential relationship of energy E (relative to the intrinsic energy E_i occurring at $E = 0$) and a temperature T with a multiplier of the effective DOS, $N(0)$. When dealing with disordered materials, the level of disorder within the material, or the number of traps, is the governing factor. As discussed in Section 2.5 this level of disorder can be represented as the MN energy. The value T_c can be used to represent the characteristic temperature of the distribution of traps. Energy kT_C, where k is Boltzmann's constant, can be considered as the width of the distribution. These characteristics produce the relationship in Eqn. 2.6-2. The DOS, $N(E)$, can be expressed as an exponential relationship in terms of energy, E, and T_C:

$$N(E) = N(0)\exp\left(\frac{E}{kT_C}\right). \qquad \textit{Eqn. 2.6-1}$$

This can be differentiated to form the change in DOS in Eqn. 2.6-2.

$$N'(E) = \frac{N(0)}{kT_C}\exp\left(\frac{E}{kT_C}\right) \qquad \textit{Eqn. 2.6-2}$$

As introduced in Section 2.4, *n* is obtained by considering this DOS along with the likelihood of occupation of states; thus Eqn. 2.6-2 can be combined into Eqn. 2.4-1 to obtain the expression shown in Eqn. 2.6-3.

$$n = \int_{E_F}^{\infty} \frac{N(0)}{kT_C}\exp\left(\frac{E}{kT_c}\right).\exp\left(-\frac{E-E_F}{kT}\right)dE \qquad \textit{Eqn. 2.6-3}$$

As carriers below the Fermi level do not contribute to conduction, the limits can be set between E_F and infinity to encompass all conducting carriers.

With respect to the disorder in organic materials the two factors of disorder, thermal and trap-related, conversely result in a density of carriers. This means that a third characteristic temperature, T_o, can be symbolised. As an energy kT_o, this value represents the net effect of kT and kT_C and follows the expression in Eqn. 2.6-4.

$$\frac{1}{kT_0} = \frac{1}{kT} - \frac{1}{kT_C} \qquad \textit{Eqn. 2.6-4}$$

This expression in Eqn. 2.6-4 can be used to simplify Eqn. 2.6-3, producing Eqn. 2.6-5.

$$n = \int_{E_F}^{\infty} \frac{N(0)}{kT_C} exp\left(-\frac{E}{kT_0} + \frac{E_F}{kT}\right)dE \qquad \textit{Eqn. 2.6-5}$$

The integration of Eqn. 2.6-5 can then be easily executed to produce Eqn. 2.6-7.

$$n = \int_{E_F}^{\infty} \frac{N(0)}{kT_C} exp\left(\frac{E_F}{kT}\right)\left\{exp\left(-\frac{E}{kT_0}\right)\right\}dE \qquad \textit{Eqn. 2.6-6}$$

$$n = -\frac{T_0}{T_C}N(0)exp\left(\frac{E_F}{kT}\right)\left[exp\left(-\frac{E}{kT_0}\right)\right]_{E_F}^{\infty} \qquad \textit{Eqn. 2.6-7}$$

Since $\left(-\frac{E_\infty}{kT_0}\right) \ll exp\left(-\frac{E_F}{kT_0}\right)$, the expression in Eqn. 2.6-8 is found, proving a dependence of the density of carriers on T_o and an even stronger, exponential dependence on kT_C in line with MN theory, i.e.

$$n = \frac{T_0}{T_C} N(0) exp\left(\frac{E_F}{kT}\right) exp\left(\frac{E_F}{kT_c}\right). \qquad \textit{Eqn. 2.6-8}$$

If used in conjunction with the UML (as mentioned in Section 2.5) in comparison with existing crystalline equations, mobility parameters can be isolated and materials can be characterised and compared for performance analysis and modelling.

2.6.2 Laplace Distribution Theory

L1 DOS distribution method for DOS was introduced by Afzal [31], however it was not explored beyond it being a possible alternative distribution. Mathematically, it is based on the first of two laws of error by Pierre Simon Laplace [32] and allows for the use of an exponential function without need for the justification of operating within the band tails of the Gaussian.

The arguments for L1 DOS are best evidenced in exploration of the Schottky diode as an explanation for the occurrence of the MN energy in its slope. As the shape of the distribution is based on T_C, the slope allows for the MN energy to be extracted over more orders of magnitude than the Gaussian. It is for this reason it is worth exploring as a possibility.

The full L1 distribution takes the form of two exponentials with the first increasing up to an energy, E_θ, where the number of states reaches its peak and thereafter decreases at the same rate.

The two branches of the distribution can be represented using expressions in Eqn. 2.6-9 and Eqn. 2.6-10:

$$N_1(E) = \frac{N(E_\theta)}{2kT_c} exp\left(\frac{E - E_\theta}{kT_c}\right) \qquad \textit{Eqn. 2.6-9}$$

where $E < E_\theta$ and

$$N_2(E) = \frac{N(E_\theta)}{2kT_c} \exp\left(\frac{E_\theta - E}{kT_c}\right) \qquad \textit{Eqn. 2.6-10}$$

where $E > E_\theta$.

Here $N_1(E)$ and $N_2(E)$ is the number of states with respect to energy E in branch 1 and 2 respectively, $\frac{N(E_\theta)}{2kT_c}$ is the peak number of states and kT_C is the width and MN energy. The distribution is shown in Figure 2.7-1 on both a linear and a logarithmic scale.

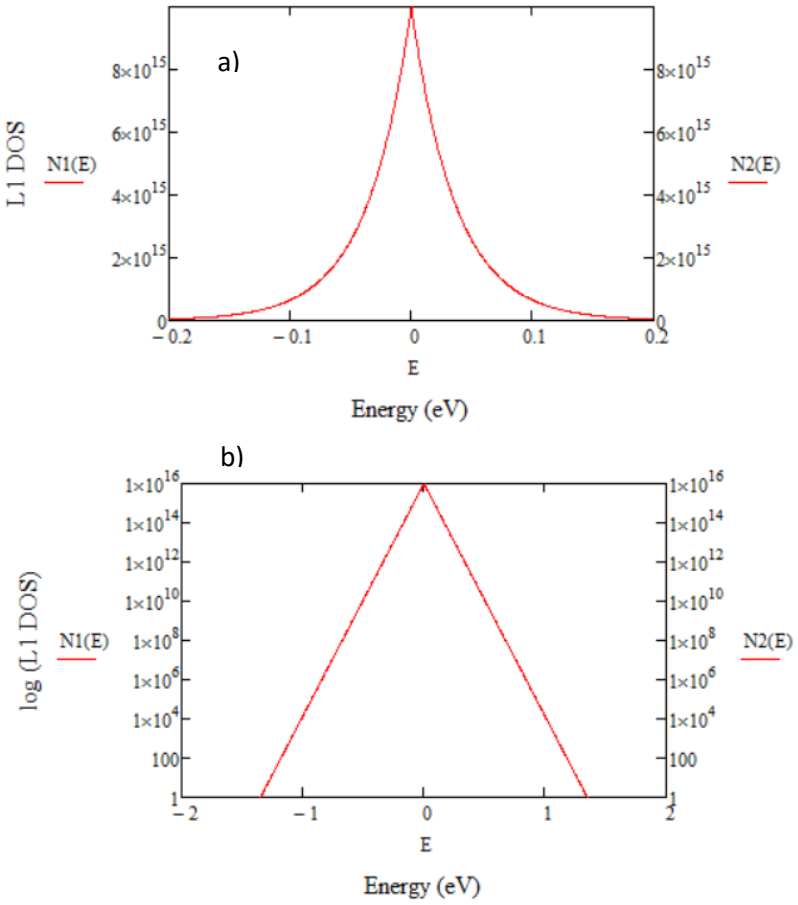

Figure 2.6-1 – a) Linear and b) Logarithmic Graphical representation of the Laplace distribution with values set as N_T=1x10^{16} and E_θ =0 eV.

In order to obtain the integration from Eqn. 2.4-1 can be applied, defining the limits as necessary. Here the rate of change $N_X'(E)$ is used to obtain carrier concentration n_X where x represents branch 1 or 2 respectively.

$$n_1 = \int_{E_F}^{E_\theta} N'(E).f_{MB}(E)\,dE \qquad \textit{Eqn. 2.6-11}$$

$$n_2 = \int_{E_\theta}^{\infty} N'(E).f_{MB}(E)\,dE \qquad \textit{Eqn. 2.6-12}$$

As it can be assumed that the carriers below the Fermi level will not contribute to conduction, and that the Fermi level will be below E_θ, this can be taken as a lower limit for n_1 and with n_2 including all energy values above E_θ through to infinity.

A base level *N(0)* can be found by applying a value of 0 to the energy *E*. If the multiplier to the distribution can be taken as $N(E_\theta)$ then the expressions for $N_X(E)$ can be simplified respectively in the forms below. These expressions for *N(E)* are in a form more comparable to that which was used for exponential distribution.

$$N_1(0) = N(E_\theta)\,exp\left(-\frac{E_\theta}{kT_C}\right), \qquad \textit{Eqn. 2.6-13}$$

$$N_1(E) = N_1(0)\,exp\left(\frac{E}{kT_C}\right). \qquad \textit{Eqn. 2.6-14}$$

Similarly for $N_2(E)$:

$$N_2(E) = N(E_\theta)\,exp\left(\frac{E_\theta - E}{kT_C}\right), \qquad \textit{Eqn. 2.6-15}$$

$$N_2(E) = N_1(0)\,exp\left(\frac{2E_\theta - E}{kT_C}\right). \qquad \textit{Eqn. 2.6-16}$$

As shown, the exponential nature of L1DOS means that as long as E_F is a few multiples of kT below E_θ, occupation of branch 2 will be negligible and the L1DOS can be approximated to a single exponential. It follows that the same models derived using the exponential DOS, such as those that will be discussed in Section 2.9, can therefore be used for an L1DOS.

2.7 Two Condition Theory

A second concept which has been explored within this project is the introduction of the two condition theory in relation to the DOS. Figure 2.7-1 shows the two conditions under which carriers could flow; Condition 1 and Condition 2.

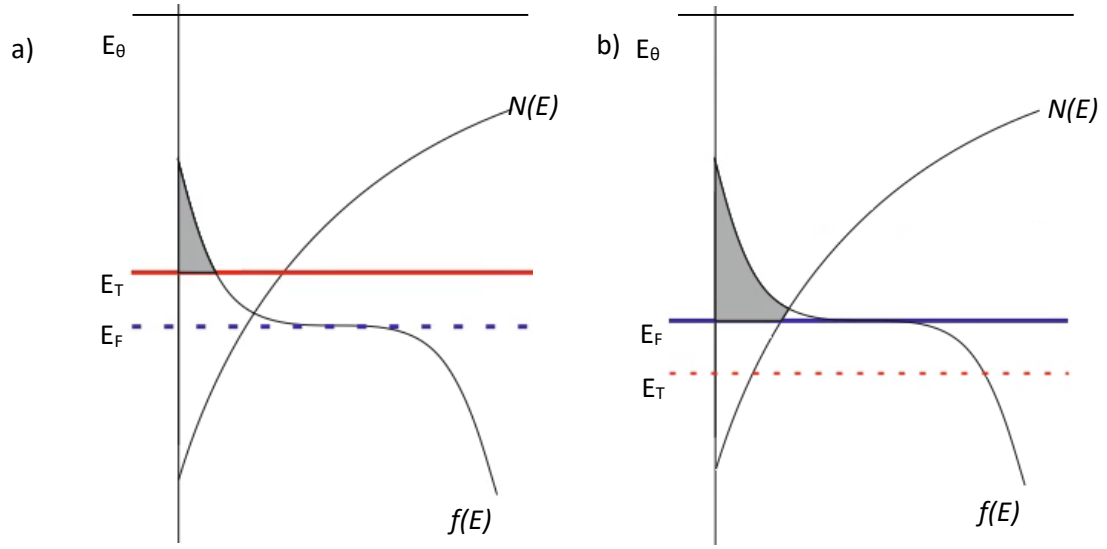

Figure 2.7-1 Energy band diagrams for the two condition theory. a) shows Condition 1 where the mobility edge, E_T is higher than the Fermi level E_F. b) shows that In Condition 2, the Fermi level is higher than the transport level and there is an accumulation of trapped charge below which must be overcome for charge to easily flow. This causes a change in gradient of the IV characteristics. NB: spacing of energy levels not to scale.

The conditions of operation are determined by the position of the mobility edge at the measurement temperature, E_T, with respect to E_F. In the context of conduction of the semiconductor, E_T is the lowest energy at which conduction is observed and therefore only carriers above this energy are contributing to the concentration.

In Condition 1 E_T is above E_F and therefore all conducting carriers are above this level. As shown by the shaded portion of Figure 2.7-1 a), any carriers can be encompassed between this lower limit E_T and the boundaries of the combination of the DOS, $N(E)$ and occupancy distribution $f(E)$. As stated in Section 2.6.2, the energy range will be within the lower branch and therefore anything above E_θ can be disregarded.

In the case of Condition 2, energy band bending as the number of carriers in the OSC increases has caused E_T to drop to below E_F. This change in position results in E_F acting as the lower limit and a build-up of static charge between E_T and E_F. It was proposed by Eccleston[33] that this could be an explanation for the behaviour in diodes. As it was proven that L1 can be simplified to only consider a single branch, the *N'(E)* derived in Eqn. 2.6-1 would apply for either distribution.

Following the process in Section 2.6, the carrier concentration can be found by integrating Eqn. 2.6-1 between the appropriate limits for each condition with the appropriate distribution of states and the rate of change in DOS, *N'(E)*. The two distribution of states used, as explained in Section 2.4, are the Fermi-Dirac, $f_{FD}(E)$, in Eqn. 2.4-1 and the approximated Maxwell Boltzmann $f_{MB}(E)$, in Eqn. 2.4-2. These can now be applied to both conditions using the form in Eqn. 2.7-1. Here the term *f(E)* is used to denote a general case for the distribution and L_U and L_L are the upper and lower limits, respectively, determined by each condition. The expressions the result from this prove the slope dependency relationships that can be extracted from diode results

$$n = \int_{L_L}^{L_U} N'(E) f(E)\, dE \qquad \textit{Eqn. 2.7-1}$$

2.7.1 Condition 1

For the integration of Eqn. 2.7-1 applied to Condition 1, it can be assumed that the upper limit for integration is E_θ, an energy higher than carriers would ever reach, and that E_T acts as the lower limit. As this condition operates on the assumption $E_T - E_F > kT$, Maxwell Boltzmann statistics apply. The integration for Condition 1 carrier concentration, n_1, takes the form of Eqn. 2.7-2:

$$n = \int_{E_T}^{E_\theta} \frac{N(0)}{kT_C} exp\left(\frac{E}{kT_c}\right).exp\left(-\frac{E - E_F}{kT}\right) dE \qquad \textit{Eqn. 2.7-2}$$

This can be expanded out and Eqn. 2.6-4 can be applied, producing Eqn. 2.7-4 through the final integral form in Eqn. 2.7-3:

$$n = \frac{N(0)}{kT_C} exp\left(\frac{E_F}{kT}\right) \int_{E_T}^{E_\theta} exp\left(-\frac{E}{kT_0}\right) dE \qquad \textit{Eqn. 2.7-3}$$

$$n = -\frac{T_0}{T_C} N(0) exp\left(\frac{E_F}{kT}\right) \left[exp\left(-\frac{E_\theta}{kT_0}\right) - exp\left(-\frac{E_T}{kT_0}\right)\right]. \qquad \textit{Eqn. 2.7-4}$$

Based on the ratio of the exponentials, it can be assumed that $\left(-\frac{E_\theta}{kT_0}\right) \ll exp\left(-\frac{E_T}{kT_0}\right)$ and therefore that

$$n = \frac{T_0}{T_C} N(0) exp\left(\frac{E_F}{kT}\right) exp\left(-\frac{E_T}{kT_c}\right). \qquad \textit{Eqn. 2.7-5}$$

In terms of an energy E_θ, the original form of Eqn. 1.6-1 can be used to deduce that

$$n = \frac{T_0}{T_C} N(E_\theta) exp\left(-\frac{E_\theta}{kT_c}\right) exp\left(\frac{E_F}{kT}\right) exp\left(-\frac{E_T}{kT_0}\right). \qquad \textit{Eqn. 2.7-6}$$

2.7.2 Condition 2

It was explained in 2.7 that the origins of Condition 2 come from the principle that as charge is injected into the semiconductor, E_F rises and adjusts its relationship to the corresponding point on the DOS distribution. As the distribution is increasing exponentially, at each increase in energy the concentration is higher and carriers are able to hop more easily to conduct. What condition 2 implies is that there is a point at which E_F surpasses the lowest level at which significant conduction can be observed (E_T). This could be an indicator that the carriers in between E_F and E_T form a block of charge which traps more of the carriers, slowing the rate of exponential. It was proposed by Eccleston [33] that this could be an explanation for extracted values of T_0 in higher voltage regions of disordered diodes.

The analysis that takes place is similar to Condition 1, however there are two extra considerations; the limits for the overall integration are between E_F rather than E_T and the Fermi-Dirac distribution must be used for states less than $2kT$ higher than E_F. The carrier concentration can therefore be found in two parts, $n_{2.1}$ and $n_{2.2}$. For energies $2kT$ above E_F, Eqn. 2.7-7 can be used to find $n_{2.1}$. This follows the same technique as Condition 1 but with the appropriate limits implemented to reflect Condition 2, producing the expression in Eqn. 2.7-8 from Eqn. 2.7-7.

$$n_{2.1} = \frac{N(0)}{kT_C} exp\left(\frac{E_F}{kT}\right) \int_{E_F+2kT}^{E_\theta} exp\left(-\frac{E}{kT_0}\right) dE \qquad \textit{Eqn. 2.7-7}$$

$$n_{2.1} = -\frac{T_0}{T_C} N(0) exp\left(\frac{E_F}{kT}\right) \left[exp\left(-\frac{E_\theta}{kT_0}\right) - exp\left(-\frac{E_F + 2kT}{kT_0}\right)\right]. \qquad \textit{Eqn. 2.7-8}$$

This can be further expanded using Eqn. 2.6-4 to the form in Eqn. 2.7-9Eqn. 2.6-13,

$$n_{2.1} = -\frac{T_0}{T_C} N(0) exp\left(\frac{E_F}{kT}\right) \left[exp\left(-\frac{E_\theta}{kT_0}\right) - exp\left(-\frac{E_F}{kT_0}\right) exp\left(-\frac{2kT}{kT_0}\right)\right]. \qquad \textit{Eqn. 2.7-9}$$

Eqn. 2.7-10

As before, since $\left(-\frac{\mathrm{E}_\theta}{kT_0}\right) \ll exp\left(-\frac{E_F}{kT_0}\right)$ can be used to produce Eqn. 2.7-11:

$$n_{2.1} = -\frac{T_0}{T_C} N(0) exp\left(\frac{E_F}{kT}\right) exp\left(-\frac{E_F}{kT_0}\right) exp\left(-\frac{2kT}{kT_0}\right). \qquad \textit{Eqn. 2.7-11}$$

In terms of an energy E_θ the original form of Eqn. 1.6-1 can be used for the final form for this section of Condition 2:

$$n_{2.1} = \frac{T_0}{T_C} N(E_\theta) exp\left(-\frac{E_\theta}{kT_c}\right) exp\left(\frac{E_F}{kT_c}\right) exp\left(-\frac{2T}{T_0}\right). \qquad \textit{Eqn. 2.7-12}$$

As stated, this section only caters for the range where the MB can be applied. For energy levels between E_F and E_F*+2kT* the FD distribution must be applied and Eqn. 2.7-2 is written in the form of.

$$\mathrm{n}_{2.2} = \int_{E_F}^{E_F+2kT} N'(E) f_{FD}(E)\, dE \qquad \textit{Eqn. 2.7-13}$$

As this integration is more complex, it needs to be put in a form that can be solved using integration by parts. This is done by combining all exponentials into the denominator. This process is shown in Eqn. 2.7-14 and Eqn. 2.7-15.

$$n_{2.2} = \frac{N(0)}{kT_C} \int_{E_F}^{E_F+2kT} \frac{exp\left(\frac{E}{kT_C}\right)}{1 + exp\left(\frac{E - E_F}{kT}\right)} dE \qquad \textit{Eqn. 2.7-14}$$

$$n_{2.2} = \frac{N(0)}{kT_C} \int_{E_F}^{E_F+2kT} \frac{1}{exp\left(-\frac{E}{kT_C}\right) + exp\left(\frac{E - E_F}{kT}\left(-\frac{E}{kT_C}\right)\right)} dE \qquad \textit{Eqn. 2.7-15}$$

With the application of Eqn. 2.6-4, the term is now in a form, Eqn. 2.7-16, which can extract a value, *u*, stated in Eqn. 2.7-17 for the integration by parts analysis.

$$n_{2.2} = \frac{N(0)}{kT_C} \int_{E_F}^{E_F+2kT} \frac{1}{exp\left(-\frac{E}{kT_C}\right) + exp\left(\frac{E}{kT_0}\right) exp\left(-\frac{E_F}{kT}\right)} dE \qquad \textit{Eqn. 2.7-16}$$

$$u = exp\left(-\frac{E}{kT_C}\right) + exp\left(\frac{E}{kT_0}\right) exp\left(-\frac{E_F}{kT}\right) \qquad \textit{Eqn. 2.7-17}$$

By differentiating *u* with respect to *dE* expressions to substitute back into Eqn. 2.7-16 can be found.

$$\frac{dU}{dE} = -\frac{1}{kT_C} exp\left(-\frac{E}{kT_C}\right) + \frac{1}{kT_0} exp\left(\frac{E}{kT_0}\right) exp\left(-\frac{E_F}{kT}\right) \qquad \textit{Eqn. 2.7-18}$$

As for each limit there will be a different value of *E*, two expressions can be formed. One for the lower limit $E = E_F$:

$$\frac{dU}{d(E_F)} = -\frac{1}{kT_C} exp\left(-\frac{E_F}{kT_C}\right) + \frac{1}{kT_0} exp\left(\frac{E_F}{kT_0}\right) exp\left(-\frac{E_F}{kT}\right) \qquad \textit{Eqn. 2.7-19}$$

$$\frac{dU}{d(E_F)} = \frac{1}{kT} exp\left(-\frac{E_F}{kT_C}\right), \qquad \textit{Eqn. 2.7-20}$$

and one for the limit $E = E_F+2kT$:

$$\frac{dU}{d(E_F + 2kT)} = -\frac{1}{kT_C} exp\left(-\frac{E_F + 2kT}{kT_C}\right) + \frac{1}{kT_0} exp\left(\frac{E_F + 2kT}{kT_0}\right) exp\left(-\frac{E_F}{kT}\right) \qquad \textit{Eqn. 2.7-21}$$

$$\frac{dU}{d(E_F + 2kT)} = exp\left(-\frac{E_F}{kT_C}\right)\left(\frac{1}{kT_C} exp\left(-\frac{2T}{T_C}\right) + \frac{1}{kT_0} exp\left(\frac{2T}{T_0}\right)\right). \qquad \textit{Eqn. 2.7-22}$$

As the approximate ratios of T/T_C and T/T_0 are known, the exponential terms $\frac{1}{kT_C} exp\left(-\frac{2T}{T_C}\right)$ and $\frac{1}{kT_0} exp\left(\frac{2T}{T_0}\right)$ can be estimated to be estimated to be a constant not much greater than 2. For simplicity, K_{FD1} can be used to represent this number.

$$K_{FD1} = \left(\frac{1}{kT_C} exp\left(-\frac{2T}{T_C}\right) + \frac{1}{kT_0} exp\left(\frac{2T}{T_0}\right)\right) \quad \textit{Eqn. 2.7-23}$$

The new limits in terms of u can be calculated using Eqn. 2.7-17 where U_L represents the lower limit (at energy E_F) and U_U the higher limit (at energy $E = E_F+2kT$. The results of this analysis are in Eqn. 2.7-25 and Eqn. 2.7-27 respectively.

$$U_L = exp\left(-\frac{E_F}{kT_C}\right) + exp\left(\frac{E_F}{kT_0}\right) exp\left(-\frac{E_F}{kT}\right) \quad \textit{Eqn. 2.7-24}$$

$$U_L = 2\, exp\left(-\frac{E_F}{kT_C}\right) \quad \textit{Eqn. 2.7-25}$$

$$U_U = exp\left(-\frac{E_F + 2kT}{kT_C}\right) + exp\left(\frac{E_F + 2kT}{kT_0}\right) exp\left(-\frac{E_F}{kT}\right) \quad \textit{Eqn. 2.7-26}$$

$$U_U = K_{FD2}\, exp\left(-\frac{E_F}{kT_C}\right) \quad \textit{Eqn. 2.7-27}$$

As with K_{FD1}, a constant K_{FD2} is declared to simplify the multiplier, the value of which is in Eqn. 2.7-28.

$$K_{FD2} = \left(exp\left(-\frac{2T}{T_C}\right) + exp\left(\frac{2T}{T_0}\right)\right) \quad \textit{Eqn. 2.7-28}$$

Substituting this analysis into Eqn. 2.7-16 and applying Eqn. 2.6-1 produces the term in Eqn. 2.7-29, completing the second stage of carrier concentration derivation.

$$n_{2.2} = \frac{N(E_\theta)}{kT_C} exp\left(-\frac{E_\theta}{kT_c}\right) exp\left(\frac{E_F}{kT_C}\right)\left[\left(ln(K_{FD2}) - \frac{E_F}{kT_C}\right)\frac{1}{K_{FD1}} - \left(ln(2) - \frac{E_F}{kT_C}\right)kT\right] \quad \textit{Eqn. 2.7-29}$$

The total carrier concentration n_T is found by combining $n_{2.1}$ and $n_{2.2}$,

$$n_T = \frac{T_0}{T_C} N(E_\theta) exp\left(-\frac{E_\theta}{kT_c}\right) exp\left(\frac{E_F}{kT_c}\right)\left(exp\left(-\frac{2T}{T_0}\right). + \frac{T}{T_0}\left[\left(ln(K_{FD2}) - \frac{E_F}{kT_C}\right)\frac{1}{K_{FD1}} - \left(ln(2) - \frac{E_F}{kT_C}\right)\right]\right), \quad \textit{Eqn. 2.7-30}$$

And is proportional to an exponential of kT_C, unlike the Condition 1 form which was shown to have a dependence on kT_0.

$$n_T \propto \frac{T_0}{T_C} N(E_\theta) exp\left(-\frac{E_\theta}{kT_c}\right) exp\left(\frac{E_F}{kT_c}\right) \quad \textit{Eqn. 2.7-31}$$

Both of these values for carrier concentration can then be used to isolate mobility parameters for the diodes as will be shown in the following section.

2.8 Organic Diodes

In order to further analyse the impact of the distribution function, its behaviour must be explored in conjunction with the operation of the individual organic devices. As the building blocks of the discipline, these devices are not only the keystones of the more complex circuitry but they help to give a clearer understanding of how the carriers behave. By dissecting this behaviour for its simplest applications, more can be understood, assumptions can be justified and models can be projected onto more complicated systems to enhance performance. The most basic device to consider is the organic diode, the functionality of which is generated by a simple metal and semiconductor interface.

The diode consists of three main parts, each with a distinctive work function: the Ohmic contact (such as gold) with a work function Φ_{om}, the Schottky contact, such as aluminium, with work function Φ_{sm} and the organic semiconductor with work function Φ_{osc}. Any work function is defined by the difference in energy between the fermi level E_F and the vacuum energy E_{vac}, the energy at which an electron would be able to break free from the material.

The energy diagram of the three material sections of the diode is shown in Figure 2.8-1.

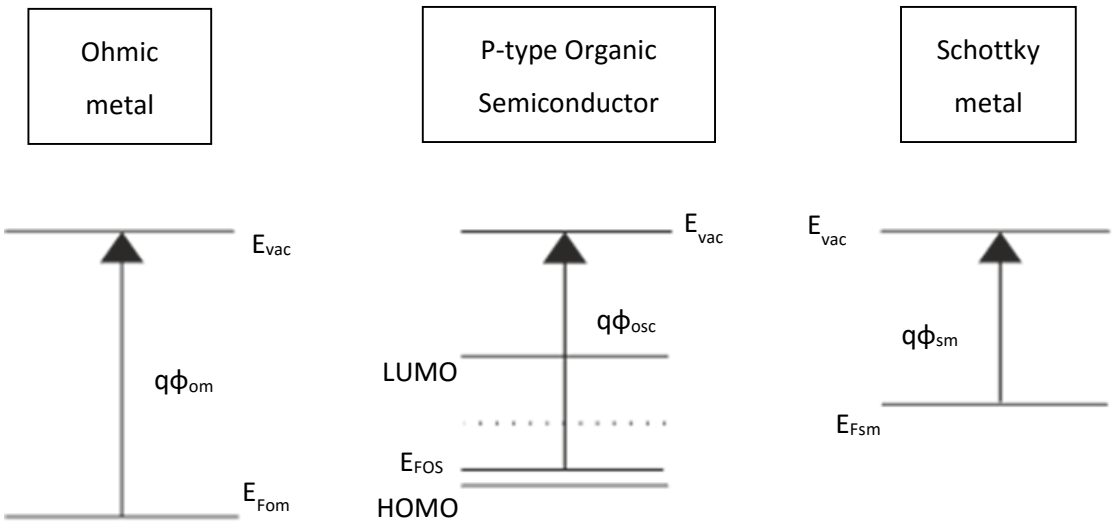

Figure 2.8-1 Energy band diagrams for Metal-Semiconductor interfaces of two different metals before contact. Each material has a distinctive work function and the difference in energy between them governs whether a material will have an Ohmic or Schottky contact.

As explained in Section 2.4, for a completely intrinsic semiconductor E_F will lie at an energy equidistant from the HOMO and LUMO known as E_i, otherwise, if doped to be either a p-type or n-type material

it would be closer to either the HOMO level or LUMO level respectively. For the case of a conducting metal at T = 0 K, the Fermi level is the highest filled energy level.

Depending on whether the material is p-type or n-type, the work function of the contact will be greater or smaller than that of the semiconductor. The diagram shown in Figure 2.8-1 contains the energy diagrams for a p-type semiconductor, as shown by the Fermi level being closer to the HOMO level (more possibility of a hole occupying an energy state due to the presence of acceptor ions). In this case $\Phi_{om}>\Phi_{osc}>>\Phi_{sm}$. Combined with the charge of an electron, q, the diagram shows each work function with respect to the E_{vac} and E_F of each material. For an n-type semiconductor the condition would be $\Phi_{om}<\Phi_{osc}<<\Phi_{sm}$.

When a metal and a semiconductor are in contact, carriers are exchanged across the interface until a thermal equilibrium is reached and the respective Fermi levels align. This means that the energy at the interface is now higher or lower and represented by a built-in value qV_{bi}, as shown in Figure 2.8-1. The electron affinity, X (as represented on the diagram in Figure 2.8-2 as the difference in energy between the LUMO and E_{vac}), cannot change as it is a material property. This results in band bending at the interface, referenced from a common E_F as all energy levels other than the Fermi level change proportionally.

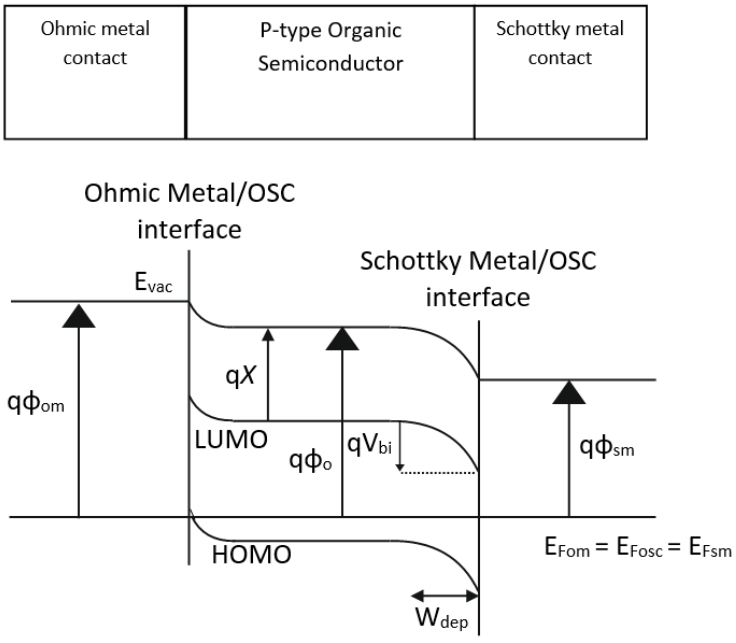

Figure 2.8-2 - Energy diagram of Ohmic and Schottky metals after contact. The band bending that occurs due to the aforementioned differences in work functions determines whether carriers can easily pass through the interface or whether a depletion region is formed due the field created from the energy difference.

For the Ohmic contact, it can be seen that the holes have an increase in energy towards Fermi level as the gap between the Fermi level and the HOMO level is reduced after contact. This eases conduction as there is little resistance and holes are able to flow freely, facilitating an effective contact for carriers.

At the Schottky metal interface, the gap between the Fermi level and HOMO level has increased. This forms a depletion region of ionised dopant ions and produces a field of charge of width W_{dep}.

This barrier formed by the work function difference is one element of the Schottky interfaces between metals and OSCs. The other is that an equal and opposite image charge is generated from the carriers within the metal, causing a barrier lowering effect just before the interface.

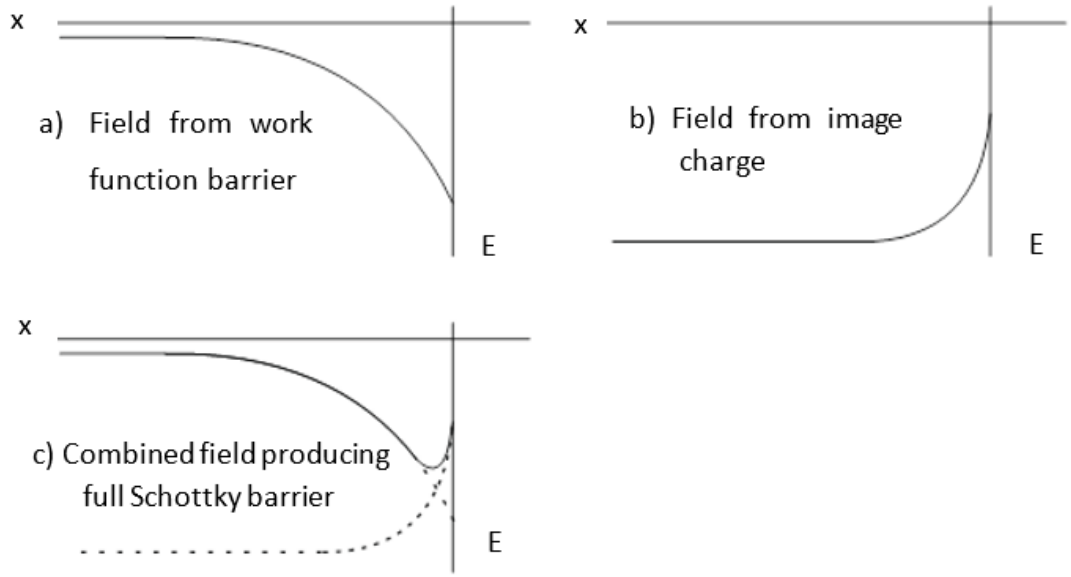

Figure 2.8-3 a) The field from the band bending caused by the differences in work function. B) The field due to the image charge where an equal and opposite charge appears on the opposite side of the interface. C) Combination of the two fields leading to the formation of a Schottky Barrier. X denotes the distance away from the interface and E the energy

The diagrams in Figure 2.8-3 a)-c) show how the two effects combine to produce the full Schottky effect. This variation associated with image charge can be shown using Coulomb's Law

$$F = -\frac{q^2}{16\pi\varepsilon\varepsilon_0 x^2}. \qquad \textit{Eqn. 2.8-1}$$

As this is a p-type semiconductor, when a negative bias is applied to the metal, $V_{app} = V_{FB}$, holes are emitted from the semiconductor into the metal. The Fermi level of the metal increases with respect to the semiconductor and the new width of the depletion region, $W_{depFB,}$ is smaller than that of W_{dep}. The energy difference is now $q(V_{bi} - V_{FB})$.

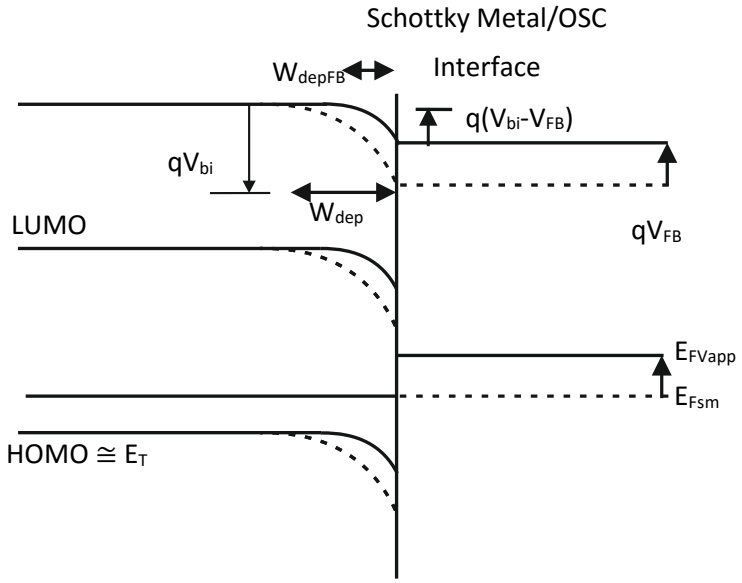

Figure 2.8-4 - Barrier lowering in Forward Bias. The applied, negative voltage injects electrons into the material and alters the position of the Fermi level. This causes the depletion region to reduce allowing current to flow.

The Fermi level increase in energy can therefore be attributed to an extra charge per unit voltage applied. If the initial built in barrier was qV_{bi}, then, temporarily disregarding image force effects, this can be represented as the difference between the mobility edge, E_T (for the purpose of this band diagram it is portrayed in a condition where this level is comparable to the HOMO level) and E_F:

$$qV_{bi} = E_T - E_F \,, \qquad \textit{Eqn. 2.8-2}$$

then with an applied forward bias V_{FB} it becomes:

$$\varphi_{osc} = E_T - (E_F - qV_{FB}). \qquad \textit{Eqn. 2.8-3}$$

Now incorporating the image force for a more physical explanation, the sharp drop from this effect causes carriers to cascade into the interface altering the Fermi level. In an effort to restore thermal equilibrium, the material generates carriers to restore the Fermi level caused by the drop. This means that the carrier concentration at the peak drops. As this concentration reduces, the generation of carriers causes the forward current and this impacts the quasi-Fermi level. Due to the dependence on *kT* for ordered, or partially ordered materials, this can be represented by the relationship in Eqn. 2.8-4

for a crystalline like material or the grain in polycrystalline. J_F is the carrier density and qV_{FB} is energy height of the barrier.

$$J_F \propto exp\left(\frac{qV_{FB}}{kT}\right). \quad \textit{Eqn. 2.8-4}$$

It was mentioned that E_T can be approximated to the HOMO level in the diagram. This assumes a condition that E_T is the highest energy at which conduction is seen, however, if applying the two condition theory then both conditions must be considered. Eqn. 2.7-6 and Eqn. 2.7-31 are presented here still in the current concentration form but now in terms of the forward bias V_{FB}.

$$n = N(E_\theta)exp\left(-\frac{E_\theta}{kT_C}\right)exp\left(\frac{E_F}{kT}\right)exp\left(-\frac{E_T - qV_{FB}}{kT_0}\right), \quad \textit{Eqn. 2.8-5}$$

or

$$n = N(E_\theta)exp\left(-\frac{E_\theta}{kT_C}\right)exp\left(\frac{E_F + qV_{FB}}{kT_C}\right), \quad \textit{Eqn. 2.8-6}$$

where *n* is the deficiency of the carrier concentration at the top of the barrier. Note that in the case of the first condition, V_{FB} is applied from E_T as it was assumed that no carriers below this point are conducting. As the material is attempting to reach thermal equilibrium, it tries to replace the carriers at the top of the barrier to an extent that depends on the deficiency of carriers at the barrier peak. Since the carriers are efficiently removed at the peak the deficiency is defined by extending the quasi Fermi level. This allows for a proportional relationship depending on which condition of the diode is performing in:

$$n \propto exp\left(\frac{qV_{FB}}{kT_0}\right), \quad \textit{Eqn. 2.8-7}$$

or

$$n \propto exp\left(\frac{qV_{FB}}{kT_C}\right), \quad \textit{Eqn. 2.8-8}$$

respectively for Condition 1 and Condition 2.

An alternative expression for an exponential DOS can be derived from integrating the current concentration from the top of the barrier to infinity. This uses the same process as developing the current density equations detailed in Section 2.6.2 and results in the form:

$$J \propto \frac{N_0 T_0}{T_C} exp\left(-\frac{E_F}{kT}\right) exp\left(-\frac{E_{Barrier}}{kT_o}\right) exp\left(\frac{qV_{FB}}{kT_o}\right), \qquad \textit{Eqn. 2.8-9}$$

where $E_{Barrier}$ is the width of the barrier at the interface and V_{FB} is still the applied voltage. Due to the difference in dependency on either T_0, T or T_C, a more general way to express the current density is in the form of Eqn. 2.8-10.

$$J \propto exp\left(\frac{qV_{app}}{k\gamma T}\right) \qquad \textit{Eqn. 2.8-10}$$

The parameter γ represents the ideality factor. A value significant larger than the ideal value of unity is interpreted as the level of disorder in the organic semiconductor. By plotting J against V_{FB}, the gradient yields a value for γ.

A value close to T_0 is often obtained but there is evidence from previous data that a value closer to the expected value of T_C is found. This observation which prompted the exploration of applying the two condition theory to give a conclusive explanation.

Applying a reverse bias causes a transient effect of carriers to be taken from the semiconductor into the metal until the system reaches equilibrium; the Fermi level decreases and the Fermi level shifts away from the transport level.

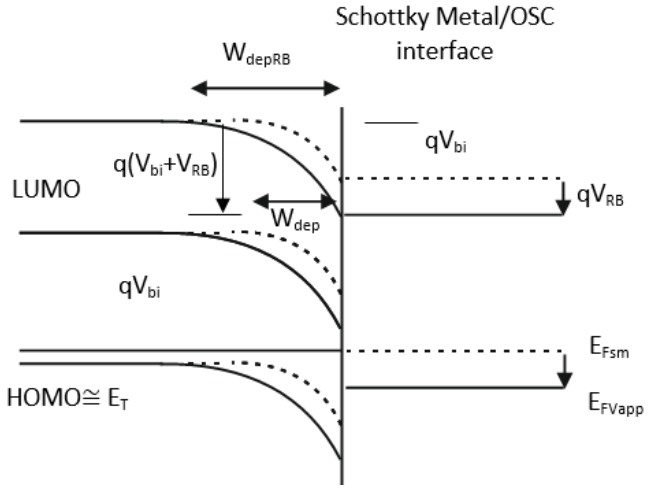

Figure 2.8-5 - Energy Diagrams for Reverse Bias. When a positive voltage is applied the Fermi-level reduces as holes are injected into the material. This causes a wider depletion region to be formed and significant energy is needed for carriers to cross the interface.

The barrier, and therefore, depletion region increases.

$$\varphi_{osc} = E_T - (E_F + qV_R). \qquad \textit{Eqn. 2.8-11}$$

When the diode is in reverse bias (with bias voltage expressed as V_R) it is in its off current state. A leakage current flows due to the influence of residual dopants. In very thin films the off current is lower as it can be shown to be related to the bulk charge of the semiconductor. This is due to the resistivity of the semiconductor being higher[34] and is explored in greater detail in Chapter 4 in the context of scaling of devices. Image effects have not been included for clarity, but were they included it could be assume that V_R would be taken to an extra $V_R^{0.5}$.

2.9 Thin Film Transistors

The second building block of organic electronics is the TFT. This is a more complex device than the diode but similar principles can be explored. Whereas a vertical diode is difficult to integrate into circuits, the TFT is more adaptable in its fabrication. It follows that the current models developed for the TFT have a direct impact on circuit design.

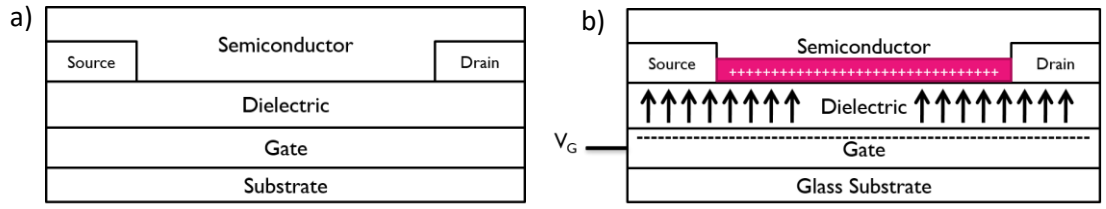

Figure 2.9-1 a) Cross section of bottom gate bottom contact OTFT consisting of a substrate, gate, dielectric layer, source and drain contacts and a semiconductor. b) Operation of OTFT when Gate Voltage is applied. This produces an electric field across the dielectric which induces a charge of opposite sign in the semiconductor forming a channel through which current can flow. This field is indicated by the arrows.

The structure of a TFT in a neutral state and after a gate voltage is applied can be seen in Figure 2.9-1. Although there are various structures of TFT (these will be explained further in Chapter 3) this is the structure which has been used within this project

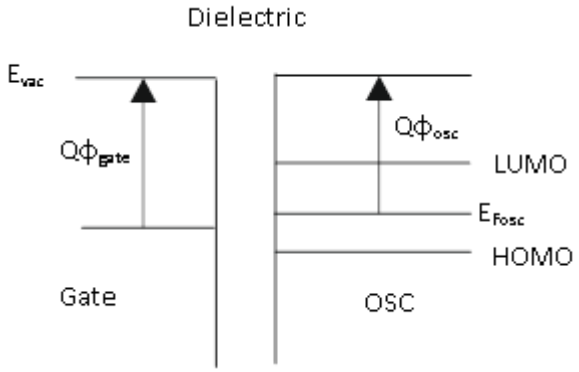

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Figure 2.9-2 Energy band diagram of OTFT before applied gate voltage. The semiconductor is shown to be p-type by the Fermi-level E_F being closer to the HOMO than the LUMO level.

The TFT consists of 4 main parts: the aluminium gate, the dielectric, the semiconductor and the Ohmic source/drain contact. Three of these are shown in the energy band diagrams in Figure 2.9-2 and Figure 2.9-3. The source drain contact is shown in Figure 2.9-5. Gold is used for the Ohmic contacts. The interface of main relevance is that of the dielectric and the semiconductor. In the flat-band state the carriers are distributed evenly throughout the material.

A positive gate voltage causes the Fermi level of the metal to drop; the field in the dielectric is negative. This causes a depletion region of width W_{dep} as shown in Figure 2.9-3. There is no path for hole current flow. This corresponds to the yellow shaded region of Figure 2.9-6 where the transistor is in an off-state. A leakage current flows through the bulk of the semiconductor. The leakage current is directly related to the thickness of the semiconductor, the dependence of which will be examined in Chapter 4.

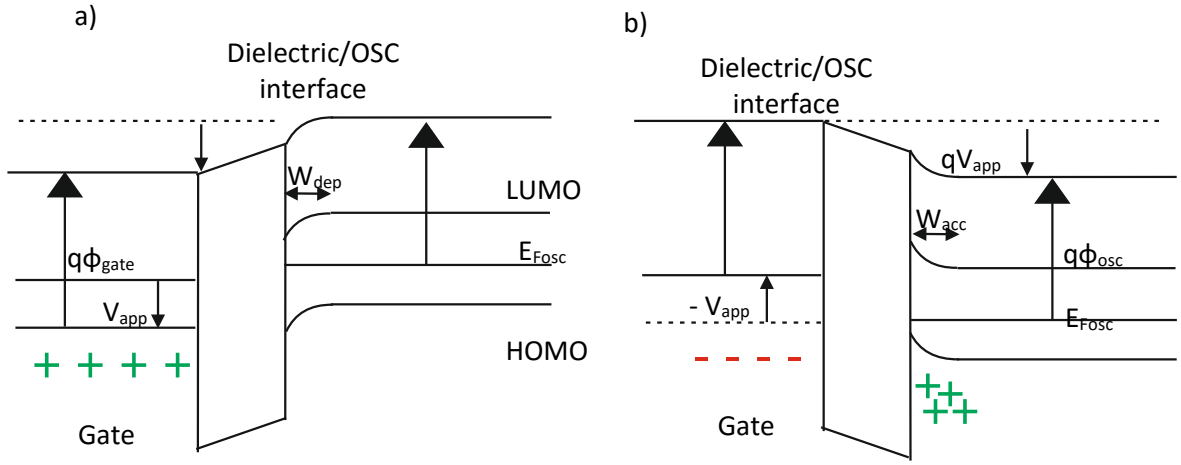

Figure 2.9-3 Energy diagrams for the OTFT operating in a) depletion and b) accumulation. When a positive voltage is applied, the Femi-level of the gate metal drops and a depletion region. This field drives carriers away and any conduction is due to the resistivity of the device.

If a negative gate voltage, $-V_{app}$, is applied, the charge across the oxide is positive at the interface and the hole carriers in the doped semiconductor migrate to form a channel of accumulated charge, shown by width W_{acc}. At this point, above the threshold voltage, V_T at which this channel is formed, the channel will begin to allow current to flow and any voltage applied to the source and drain will pass through the channel. The field is at a maximum at the interface and slowly reduces as it goes into the bulk of the semiconductor. The majority of the conducting charge accumulates within a small material dependent length approximated as the Debye length, L_D. The scaling implications on this parameter are discussed in Chapter 4. The transistor will remain on for as long as it is within this operating regime and any applied source-drain potential will occur. The transistor operates within this region with any applied gate voltage above V_T but can be further categorised into two sections relating to the size of the applied $V_{DS.}$

As mentioned, the source/drain interface has a basic Ohmic contact, working in the same way as the diode and allowing carriers to flow freely due to the work-function based band bending that occurs. When a potential drop is applied across the contacts, the Fermi level at the drain contact will cause a shift in energy and carriers will be able to flow across this potential, provided there is a channel within the semiconductor between.

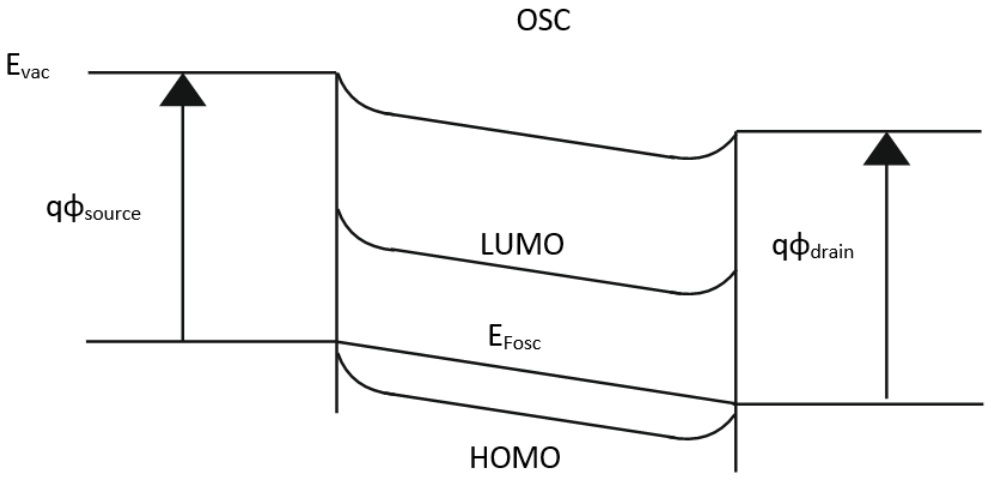

Figure 2.9-4 - Energy band diagram for the Ohmic contacts with the semiconductor material. As with the diode, the larger work function of the metals in comparison with the semiconductor have minimal bending when the Fermi-levels align. This facilitate carriers to be able to easily flow if a voltage is applied across them.

The operating regimes of the OTFT are shown by the transfer characteristic in Figure 2.9-6.

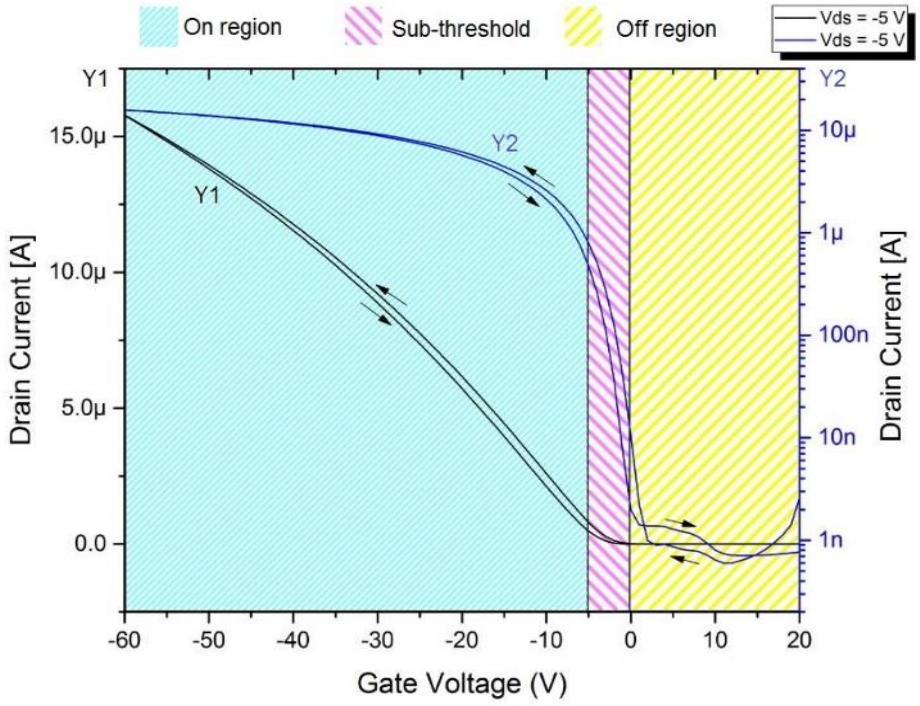

Figure 2.9-6 Transfer characteristics of an OTFT fabricated using the process detailed in Section 3.5.2. A 20 - -60 V sweep was applied to the gate voltage with an applied V_D of -5 V. Highlighted regions show the different regimes that OTFT goes through under these conditions. The yellow region to the right, highlighted with yellow diagonal lines shows the off and depletion region when the voltage applied is below turn-on voltage or positive. The central pink region indicated when the device is in subthreshold where V_D has no impact on current. The left, solid, blue region shows the condition where the device is in full operation and dependent on both of the applied voltages. Y1 shows the Drain Current on a linear scale and Y2 on a log scale.

Referring to Fig. 2.9-5, two operating regions can be identified, namely the subthreshold region, highlighted in pink and the on-region highlighted in blue. The subthreshold region is defined by the exponential dependence between the turn on voltage and the threshold voltage, V_T. Above this point the device is considered to be fully on. In the sub-threshold region $V_{GS} - V_T$ is smaller than any applied V_{DS} which means that the current is strongly dependent on V_{GS} and very weakly on V_{DS}. This is indicated in terms of the output characteristics (shown in Figure 2.9-7) as the saturation region highlighted in brown that occurs above the pinch off point shown by the line $V_{GS} - V_T = V_{DS}$.

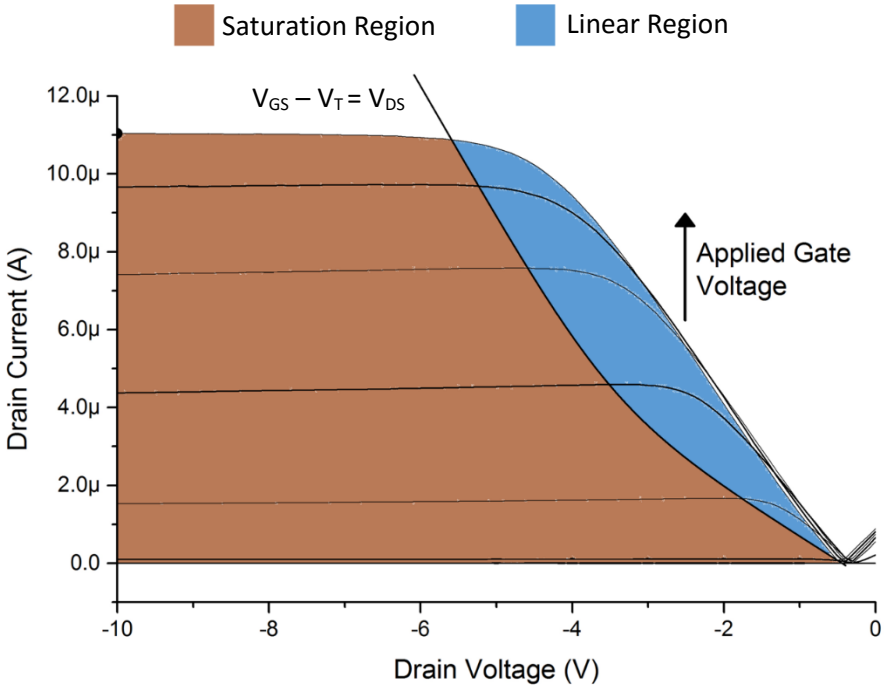

Figure 2.9-7 Output characteristics of OTFT for 6 different applied gate voltages with linear and saturation regions indicated. These correspond to the same conditions as indicated on the transfer characteristics, however this time there is a varying V_D with a constant V_G.

Before the increasing V_{DS} reaches this point, there is a dependence on both V_{DS} and V_{GS} with a linear increase. This is the linear, or Ohmic, region as it depends directly on the applied V_{DS} and operates as would a variable resistor. This region can be used for parameter extraction, as will be detailed in Chapter 3.

For ordered devices, these two regions can be represented as:

$$I_{lin} = C_0 \mu \frac{W}{L}(V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2} \qquad \textit{Eqn. 2.9-1}$$

for the linear region and

$$I_{sat} = C_0 \mu \frac{W}{2L}(V_{GS} - V_T)^2 \qquad \textit{Eqn. 2.9-2}$$

for the saturation region. It should be noted that in an ideal transistor, the drain current in the saturation region would be flat, as indicated in Eqn. 2.9-1. and the V_{GS} - V_T = V_{DS} line parabolic. The results shown here are measured from fabricated devices and there is a loss of current with V_{DS}. It is

also clear from Eqn. 2.9-2 that the increase in the linear region should have a slope proportional to (V_{GS} - V_T). It is clear from these results that this is not the case and is due to a high series resistance that would not occur in an ideal device. In ideal devices this would not be the case and the shortcomings in these fabricated devices will be explore in Chapter 3.

As stated, Eqn. 2.9-1 and Eqn. 2.9-2 are for an ordered TFT, but in the case of the disordered TFT a different form must be used. This can be derived using the carrier concentration developed in Section 2.6 and was carried out by Raja *et. al* in 2012[35] to produce the current forms in Eqn. 2.9-3 and Eqn. 2.9-4 for the linear and saturation regimes respectively:

$$I_{lin} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(\frac{(V_G - V_T)^{(2m+2)}}{2(m+1)(2m+1)} - \frac{(V_G - V_T - V_D)^{(2m+2)}}{2(m+1)(2m+1)}\right), \qquad \textit{Eqn. 2.9-3}$$

$$I_{sat} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(\frac{V_G - V_T{}^{(2m+2)}}{2(m+1)(2m+1)}\right). \qquad \textit{Eqn. 2.9-4}$$

As explained in the aforementioned section, it is assumed that this theory holds for both the L1DOS model and the exponential model as long as E_F is several kT below E_θ. This means that these forms of the equation are appropriate to use for the device analysis that takes place in Chapter 3.

2.10 POLYCRYSTALLINE CURRENT EQUATION

The derivations produced in the previous section apply to materials of total disorder. There is no level of crystalline behaviour and therefore the carrier behaviour is dependent entirely on the disorder of the material. With polycrystalline materials, as explained in Section 2.3, they inhibit a level of disorder within the grain boundaries; however there is a level of order within the grains. Figure 2.10-1 shows a 3D energy band representation of a polycrystalline grain. If x represents the distance from the boundary edge, it can be assumed that as x increases the number of traps decreases and, for p-type materials, the Fermi level would move towards the valence band edge E_V – or more accurately when considering organics materials, the HOMO level, or the effective mobility edge transport level transport level E_T.

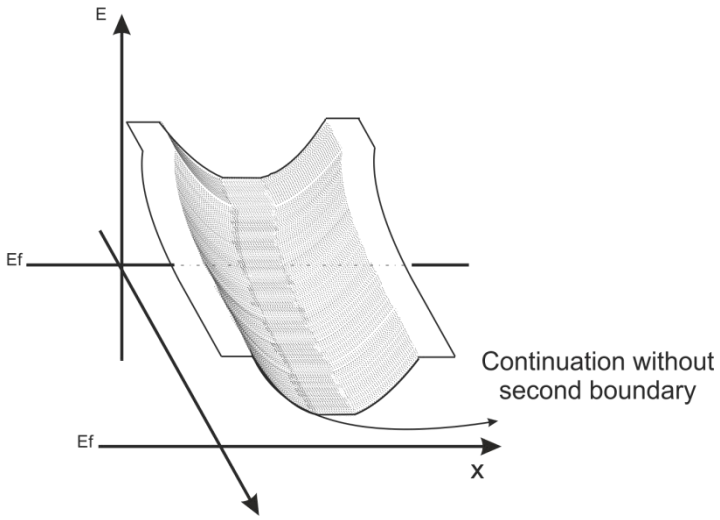

Figure 2.10-1 Polycrystalline grain energy levels considering energy bands both with and without second grain boundary. The crystalline structure within the grain has an energy level close to the Fermi-level as it is indicating its ease of conduction. X indicates the distance away from the interface and E_F indicates the Fermi-level with respect to an increasing energy, E. The arrow indicates that without the second boundary the energy would continue in a flat band manner.

For a crystalline material without any concern of boundary trapping, this would continue infinitely onwards as the surface potential increases. As the traps reduce the further the distance from the boundary edge, the hole density is at its highest and the device can exhibit more crystalline-like behaviour. The introduction of a second boundary results in the introduction of more traps as *x* approaches the full length of the grain and a well-like structure is formed where the dip of the energy band is determined by the relative size of the grain and a parameter known as the Debye Length. This was introduced in the context of the TFT structure. As *x* extends beyond $L_{D,}$ the carrier concentration returns to its intrinsic value and therefore conducting charge subsides into a neutral region. When a voltage is applied, the charges congregate closer to the interface and L_D decreases in length.

The conduction in Polycrystalline TFTs was discussed by Eccleston [36]. In this paper he proposed that the current flow in TFTs consisted of three regions: quasi-drift, quasi diffusion and a combination of the two. This can be described with three distinctive band diagrams and can be used to produce a relationship related to Einstein's equation. A summary of this model is presented for clarity.

The model considers the scenario of each grain being of length 2a and with the assumption that the contacts are Ohmic and, therefore, do not affect the performance of the device. In the sub-threshold region there is an increasing voltage being applied across the contacts but not yet a net potential drop across grains. This causes a rise in carrier concentration in grains closest to the contact but, with no voltage driving current flow, the hole density within the grains decreases in each adjacent grain as

distance increases from contact. This is assumed to be controlled by diffusion and is shown in Figure 2.10-2 by the increasing gap between E_F and HOMO in each adjacent grain.

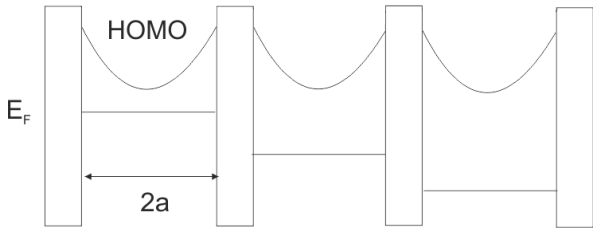

Figure 2.10-2 – Polycrystalline band diagram for Quasi-diffusion mode of operation.

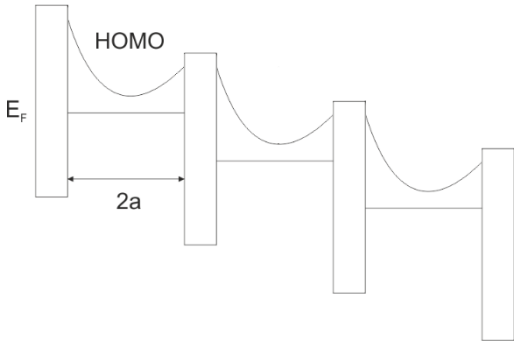

Figure 2.10-3 - Polycrystalline band diagram for Quasi-drift mode of operation

As the applied voltage at the drain increases, the potential barriers at each of the boundaries decreases. This results in lowering of the bands as the source drain voltage begins to dominate and drive the carriers. With the help of this voltage, the current is now able to flow and the gap between HOMO (for p-type materials) and E_F remains consistent, irrespective of distance from the injection of carriers. This is the quasi-drift mode of operation and is shown in Figure 2.10-3. When the grains are subject to both modes of operation there is a combined effect with a net drop in voltage across grains as well as a change in hole density for each. This is represented in Figure 2.10-4 by the increasing gap between E_F and HOMO in each grain as well as the lower potential of each.

By considering the flux of carriers across grain boundaries, an expression can be developed based on a combination of the quasi-drift and quasi-diffusion models as shown in Figure 2.10-4. This combination accounts for the point at which both diffusion and drift takes place and the device is switching. This point is irrespective of the drain and gate voltage and is consistent when comparing

transfer characteristics to isolate the material properties of polycrystalline materials. This is explored later in Section 3.7.2 in the context of characterisation of experimental results.

The flux across grains was used to prove an Einstein relationship by Eccleston in the aforementioned paper and then further explored by Myers[37] to develop a current equation for polycrystalline materials. By repeating the method that was used, the expression for the carrier concentration developed in Section 2.6 can be applied to produce a newer model based on the exponential (and the approximated Laplace) DOS.

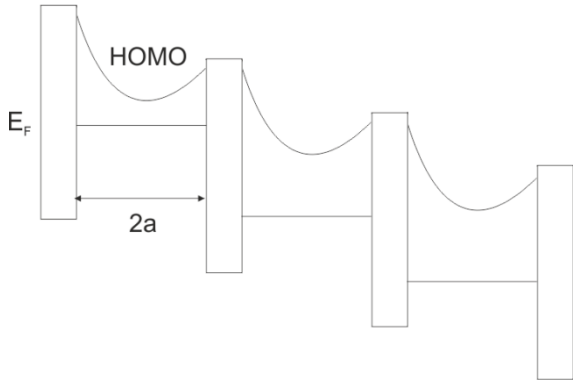

Figure 2.10-4 - Polycrystalline band diagram for combined Quasi-Diffusion and Quasi-drift mode of operation

Myers polycrystalline equation was derived in terms of the channel width and the surface potential ϕ_{sp} in terms of a distance into the channel *z*. He combined this with the derived expressions for the flux H_{diff} and the field across the channel, *F*, obtained using the continuity of dielectric displacement.

Using the flux analysis carrier out by Myers based on the models Eccleston developed, this process can be replicated with the derivations for *N(E)* detailed in Section 2.6. Raja *et al.* [35] derived this for the exponential model in 2012 by integrating out the expression for $I_{diff,}$. This produces an expression in terms of all of the constant parameters based on the dimensions and charges of the grains and is shown in Eqn. 2.10-1 and Eqn. 2.10-2 for the diffusion model:

$$I_{diff} = W\frac{4qva^2p_0}{L}\left(\frac{2N_0kT_0}{\varepsilon_b}\right)^{\frac{1}{2}}\int_0^{\phi_{sp}}\exp\left(\frac{\phi_{sp}(z)c_{diff}}{2kT_c}\right)d\phi(z), \qquad \textit{Eqn. 2.10-1}$$

$$I_{diff} = W\left(\frac{{C_{ox}}^{c_{diff}}}{L}\right)\left(\frac{4qa^2vp_0}{c_{diff}}\right)\left(\frac{2N_0kT_C}{\varepsilon_b}\right)^{\frac{-(c_{diff}+1)}{2}}\left(\frac{1}{\varepsilon_b}\right)^{c_{diff}}\left(\frac{2kT_c}{q}\right)(V_G - V_T)^{c_{diff}}. \qquad \textit{Eqn. 2.10-2}$$

In order to simplify the terms for obtaining the parameters, all constants can be absorbed into a term K_{diff} where

$$K_{diff} = W\left(\frac{{C_{ox}}^{c_{diff}}}{L}\right)\left(\frac{4qa^2vp_0}{c_{diff}}\right)\left(\frac{2N_0kT_C}{\varepsilon_b}\right)^{\frac{-(c_{diff}+1)}{2}}\left(\frac{1}{\varepsilon_b}\right)^{c_{diff}}\left(\frac{2kT_c}{q}\right). \quad \textit{Eqn. 2.10-3}$$

Now:

$$I_{diff} = K_{diff}(V_G - V_T)^{c_{diff}}. \quad \textit{Eqn. 2.10-4}$$

The same principle was applied for the drift current, however the different value for flux is required.

$$I_{drift} = W\int_0^{\phi_{sp}} \frac{qH_{drift}}{E_z}\,d\phi \quad \textit{Eqn. 2.10-5}$$

$$I_{drift} = W\frac{4qva^2p_0}{kT}\left(\frac{2N_0kT_C}{\varepsilon_b}\right)^{-\frac{1}{2}}\int_0^{\phi_{sp}} \exp\left(\frac{\phi_{sp}(z)c_{drift}}{2kT_c}\right)F_{xmean}\,d\phi(z) \quad \textit{Eqn. 2.10-6}$$

$$I_{drift}\int_0^L dx = W\frac{4qva^2p_0}{kT}\left(\frac{2N_0kT_C}{\varepsilon_b}\right)^{-\frac{1}{2}}\int_0^{V_D}\int_0^{\phi_{sp}} \exp\left(\frac{\phi_{sp}(z)c_{drift}}{2kT_c}\right)d\phi(z)dV_x \quad \textit{Eqn. 2.10-7}$$

The drift region can be in either unsaturated or saturated regions and the final expressions are shown below.

$$I_{driftunsat} = K_{drift}[(V_G{'})^{c_{drift+1}} - (V_G{'} - V_{DT})^{c_{drift+1}}], \quad \textit{Eqn. 2.10-8}$$

and

$$I_{driftsat} = WK_{drift}[(V_G{'})^{c_{drift+1}}]. \quad \textit{Eqn. 2.10-9}$$

Where:

$$K_{drift} = W\left(\frac{{C_{ox}}^{c_{drift}}}{L}\right)\left(\frac{4qa^2vp_0}{c_{drift}}\right)\left(\frac{2N_0kT_0}{\varepsilon_b}\right)^{\frac{-(c_{drift}+1)}{2}}\left(\frac{1}{\varepsilon_b}\right)^{c_{drift}}. \quad \textit{Eqn. 2.10-10}$$

Using these existing models for polycrystalline and disordered organic materials, it is possible to perform the parameter extraction needed for modelling based on the experimental work detailed in Chapter 3, the scaling calculations in Chapter 4 and the simulation models in Chapter 5.

2.11 Summary and Conclusions

This chapter looked at the distinctive properties of organic materials on a more intricate level. The differences between disordered and polycrystalline organic materials in comparison with crystalline structures were explained. The impact this chemical structure has on the way that organic devices behave must be understood in order for optimum models to be produced that reflect the behaviour of carrier transport and associated device models. As a preface to developing current models, a feature of a unifying relationship for the mobility within organic materials, the Universal Mobility Law, was discussed. Incorporating this feature within current models is important to reflect the variable nature of mobility within organics and is a main reason that the constant mobility approximation used with crystalline analysis is not appropriate for accurate representation of device behaviour. Also discussed were the various statistical distributions for the DOS and the evidence for these within literature including the exponential and Laplace 1 model. A newly introduced concept was the Two Condition Theory; this is the idea that carrier transport in organic devices may operate in two distinctive conditions in order to explain the occurrence of not just T_C as a unifying energy, but also that of T_O that can occur in higher voltage regions of diodes. It was proposed that this change in gradient of the *IV* characteristics is due to a build-up of trapped charge that occurs when the Fermi level, E_F, crosses the mobility edge E_T. By changing the limits of the integration based on which of these level sees minimum conduction changed the carrier concentration dependency from T_C to T_O, supporting the idea that above a certain applied voltage the energy law relationship switches

The energy band diagrams for the organic diode and the OTFT were presented and explained. The account included a background to the structures of devices featured in Chapter 3. The background of the development for the polycrystalline model was included for the same purpose of analysing the experimental work. This allows for analysis of both polycrystalline and disordered films.

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Chapter 3 FABRICATION AND CHARACTERISATION OF DEVICES

3.1 Fabrication of Organic Devices

The structure and fabrication processes involved in the organics industry vary greatly depending on many factors, for example the equipment available and the ultimate purpose of the device. The structure chosen for the devices, as well as the materials used, all have an impact on the device performance. This study included the fabrication of 3 main devices, the structures of which are shown in Figure 3.1-1; a diode, metal oxide semiconductor capacitor (MOSC) and OTFT.

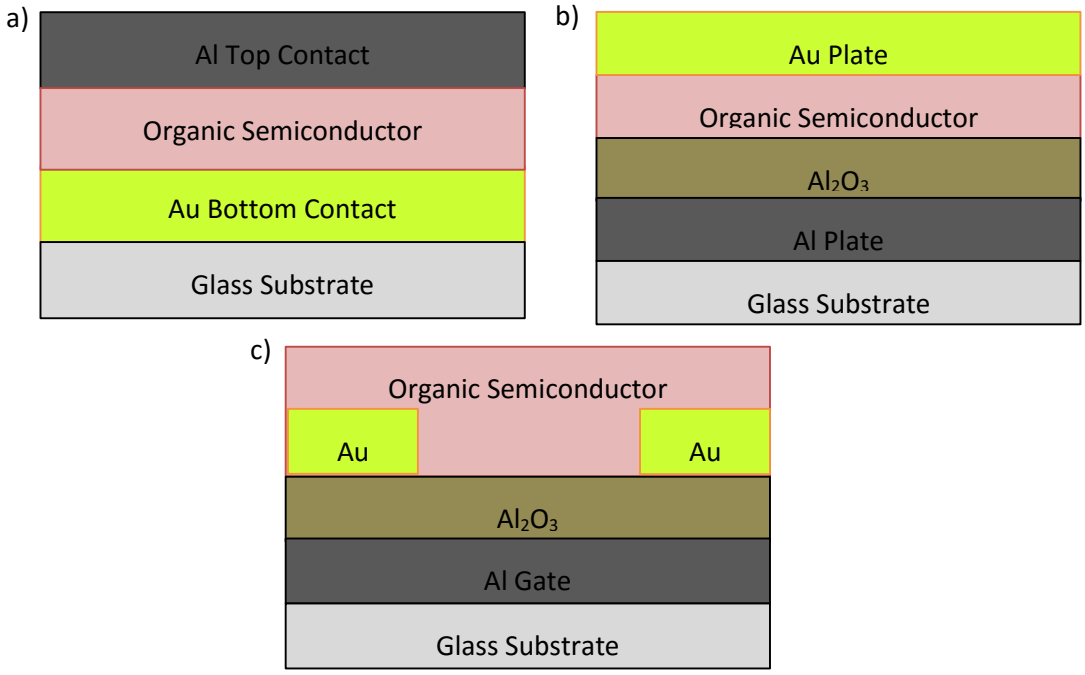

Figure 3.1-1 – Diagrams of device structures used in project. a) Represents diode structure consisting of gold Ohmic contact and aluminium Schottky contact with a Lisicon™ polycrystalline material for the semiconductor. b) Represents a MOSC structure with an aluminium bottom plate and aluminium oxide dielectric grown on top. c) Thin film transistor structure constructed by same layers as MOSC but with semiconductor layer above gold source and drain contacts. These diagrams do not include contact solution stages detailed later in this chapter.

Regarding the OTFT, there are 4 main structures that exist that are defined by the placement of the contacts with respect to the adjacent layers. They are all a combination of either bottom (BG) or top (TG) gate contact and bottom (BC) or top (TC) source and drain contacts.[1][2]. Figure 3.1-1 c) features a BG-BC structure as this was the structure used for the scope of this project. The other three, TG-BC, TG-TC and BG-TC are shown in Figure 3.1-2 and labelled as a)-c) respectively.

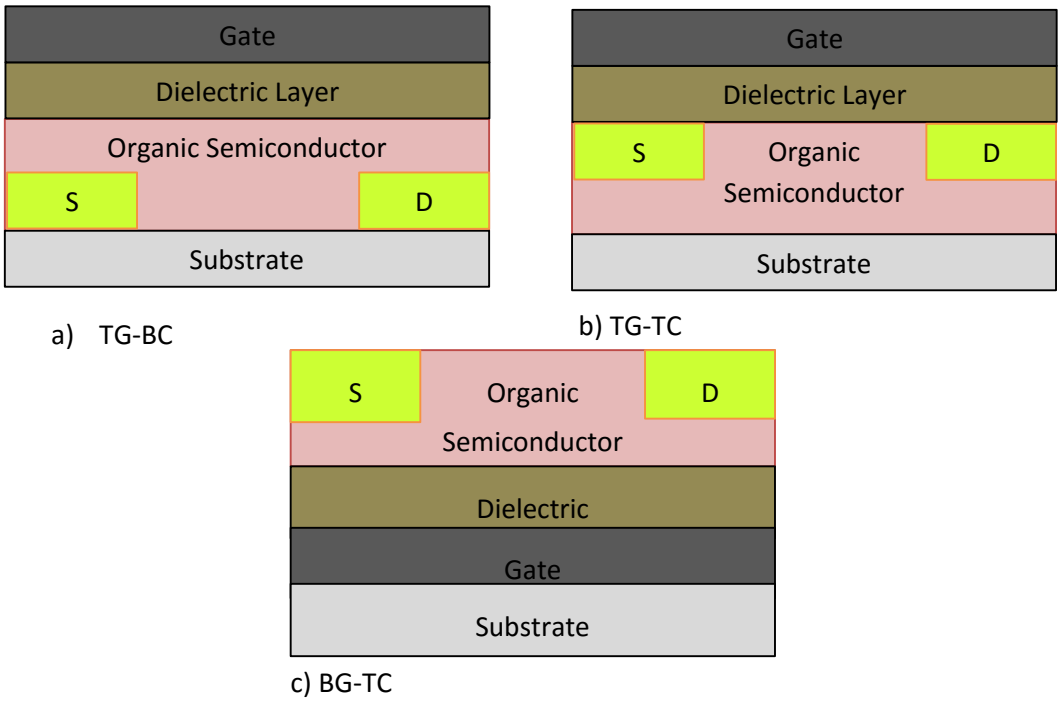

Figure 3.1-2 Device structures for three remaining structures of OTFT. These are a) Top Gate – Bottom Contact, b) Top Gate – Top Contact and c) Bottom Gate - Top Contact. Each of those configurations have implications for the performance of the device and each requires a different method of fabrication.

Each configuration has its own advantages and disadvantages[3] and therefore the appropriate structure should be chosen in context of the purpose of the transistor but also with any experimental restrictions in mind. In terms of testing devices and circuits for the purpose of understanding carrier transport behaviour, it is important to be able to obtain as reliable and reproducible results as possible with the conditions available and as the performance of individual organic device samples can be volatile it is important to be able to produce them easily so that many samples can be made to provide a greater range. This increases the chances of producing a working device. The structures that provide the easiest fabrication process are the bottom gate structures[4] as top gate structures involve more steps. They also involve processes on top of the organic semiconductor (OSC), which can be very delicate[5], and it is therefore simpler for this to be the final layer[6] rather than an intermediate one. While it can introduce series resistance, the bottom gate structure is easier to integrate with other devices such as diodes and with the wider aim of this research to be applied to circuits, the ability to combine different types of devices was also a deciding factor. For these reasons, and the lab equipment available, this project is centred on a bottom gate structure – although the models derived should apply to top gate structures as well.

As discussed in Chapter 2, the semiconductor material produces different conduction processes but the metal that forms the interface with the material also plays a crucial part, as do any self-aligned monolayers (SAMs). Different fabrication processes that exist affect performance greatly. One of the major benefits of OTFT technology is the low cost[7] printing potential due to the cheapness of casting and spin coating[8] at low temperatures from solution. On the other hand the best results have been obtained under the much more expensive vacuum evaporation method[9].

Although each device has its own unique structure, many of the processing steps are common across all of those detailed in this thesis.

3.2 Substrate

Due to the nature of organic devices, the substrate used to build upon does not need to have an electrical bias. This means that the range of materials that can be used is much less restricted than other semiconductors[1]. Despite its compatibility, the substrate does form the foundation layer for devices and the preparation of the substrate has a major impact on the quality of the device that is fabricated. All of the devices prepared go through a similar cleaning process to ensure that there are as few defects as possible at this crucial, first stage of the process.

Substrate cleanliness is important for device performance as impurities or roughness of the substrate layer when working on the micro or nanoscale can result in a low yield, however as with transistor structure there are also lab restrictions that can affect the choice of cleaning method. An enhanced cleaning process makes a significant difference in the quality of the device but due to restrictions on using particular chemicals in the facilities provided, acid based methods such as Piranha and RCA were unavailable. For this reason, solvent based cleaning was used. While less rigorous than acid based methods it still improves the surface to a sufficient degree. Depending on the dimensions required for the sample, 250 mm x 750 mm glass slides were visually examined and selected based on the quantity of defects on of the glass. Defects included scratches and deposits left from factory cleaning process in production of the glass at manufacture. The quality of glass has shown to have less impact on diode performance, however these defects were found to be detrimental to the oxide growth for TFTs (which will be detailed in Section 3.5.1). Once slides were selected, they were rinsed in de-ionised water (DIW) to remove any loosely attached dirt or residue. The slides were blow-dried using a nitrogen gun to neutralise them as well as remove water droplets. The next stage was to submerge them fully in a 3% Decon 90: De-ionised water (DIW) solution in a beaker that was sonically radiated in an ultrasound bath. The ultrasonic waves agitate any contaminants on the surface by both kinetic motion and through cavitation[10]. This solution acts as a cleaner for any surface impurities such as

dust or grease that were not removed by the preliminary wash. The Decon 90 solution was then rinsed from the sample with DIW and dried with a nitrogen gun. This process of sonication, rinsing and drying was then repeated with acetone to perform a more aggressive clean. In the final cleaning stage the process was repeated with isopropanol (IPA) to clean off any residue that may have been left by the former cleaning agents. After the routine rinse with DIW and drying with nitrogen gas, the glass was then dried at 120° C in an oven to evaporate any residue from the cleaning stages.

3.3 Diode Fabrication

Step 1 - Substrate

The substrate was prepared as detailed in Section 3.2 with slides being cut to be approximately 325mm in length.

Step 2 - Ohmic Contact

At the next stage of the process 50 nm contacts were evaporated onto the slide producing the Ohmic contact to the diode. Two metals, gold and copper, were used and compared (detailed in Section 3.8). There was also a selection of samples that had both gold and copper applied to the same slide (ensuring consistency with OSC). The metal was cleaned for evaporation using an acetone ultrasound bath for 15 minutes, rinsed using DIW and then dried in a hotbox at 120 ° C to remove moisture. The pressure at which the evaporation took place was kept in the region of $2x10^{-7}$ mbar, however the voltage needed to evaporate each metal varied each time and was carefully controlled to ensure the desired thickness was applied. It was found that the copper required a higher voltage.

Step 3 - OSC application

Once the evaporation was complete the samples were soaked in a pentafluorobenzenethiol and proponal contact solution. Two different OSC formulations were used for diode characterisation. The disordered material PTAA and the polycrystalline material Lisicon™ S1200. In the case of the former 50 mg of PTAA was weighed out and added to 5 ml of Xylene and in the case of the latter the Lisicon™ S1200 was applied directly to the sample. There were two methods of deposition: spin coating and drop casting. The comparison of these methods is explored later in this chapter.

Step 4 - Schottky Contact

Once the OSC had dried, aluminium Schottky contacts were evaporated through a shadow mask to form 1 mm diameter contacts of 200 nm thickness. Similar to the Ohmic contact, the pressure for

evaporation was kept as low as possible. The rate of evaporation was kept at 5 nm/s as the thicker layer and better adhesion allowed for a faster rate of deposition.

3.4 Diode Characterisation

Typical diode characteristics are shown Figure 3.4-1. These were generated using a Hewlett Packard 4155b Semiconductor Parameter Analyser and performing a -10 V to 10 V sweep across the device. The forward and reverse bias regions are identified. These areas follow the theory described in Chapter 2. Notable parameters to extract from the diode characteristics have been the maximum current which in this example is in the region of 10 μA.

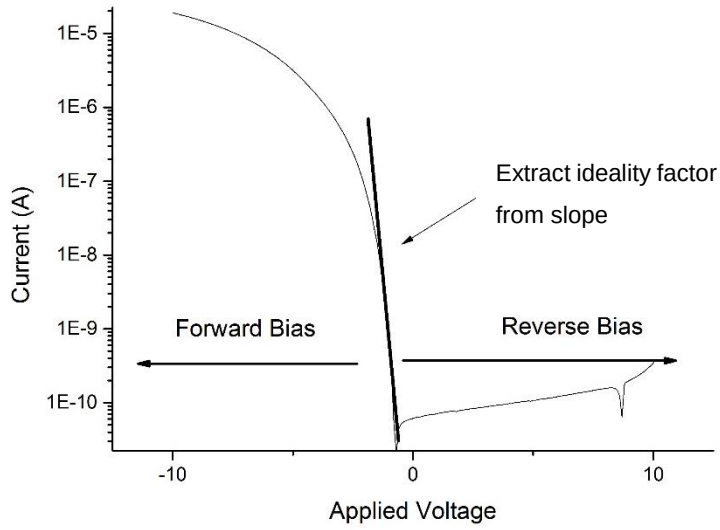

Figure 3.4-1 Diode Characteristics showing Forward and Reverse Bias Regions with indicated ideality. These correspond to the theory discussed in Section 2.8.

Another parameter, as derived in Section3.4, is that of T_o – or in a more general sense, the ideality factor γ.

A Matlab program was developed to select two points on the diode data to allow γ to be found for the diode characteristics. Once γ is obtained, this can then be used to calculate the value m and subsequently, characteristic temperatures T_C or T_0.

Figure 3.4-2 and Figure 3.4-3 are of a PTAA diode and a Lisicon™ S1200 diode respectively. The ideality values extracted were 2.9 and 2.3 respectively yielding a T_o of 870 K for the PTAA and 690 K for the Lisicon™ S1200. The current performance is compared in Table 3.4-1.

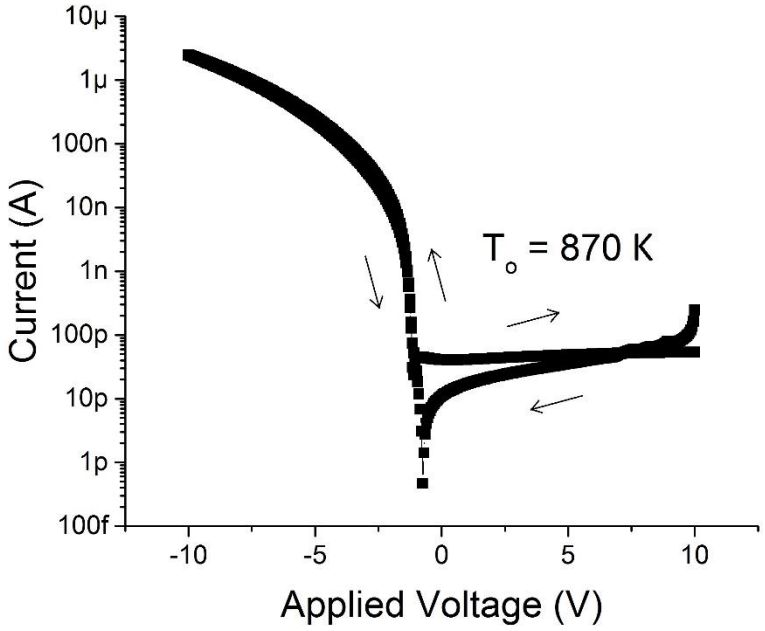

Figure 3.4-2 Output of 1 mm² aluminium Schottky contact for PTAA drop cast diode with gold Ohmic contact. The device was swept from 10 V to -10 V and then -10 V to 10 V to have a double sweep. The T_0 was extracted to be 870 K.

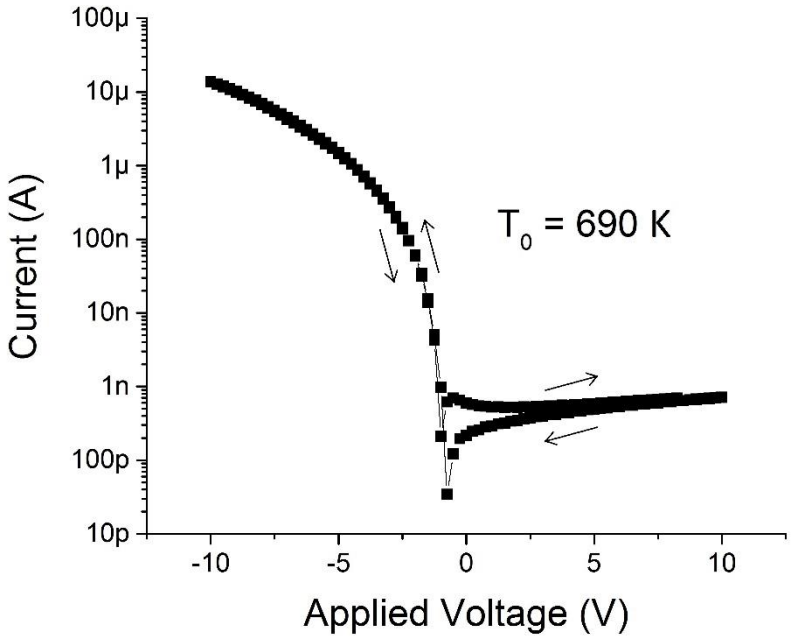

Figure 3.4-3 Output of 1 mm² aluminium Schottky contact for Lisicon™ S1200 drop cast diode with gold Ohmic contact. The device was swept from 10 V to -10 V and then -10 V to 10 V to have a double sweep. The T_0 was found to be 690 K.

Table 3.4-1 – Comparison of the characteristics of two diodes, one with disordered PTAA as the p-type semiconductor and one with polycrystalline Lisicon™ S1200.

	PTAA	Lisicon™ S1200
γ	3.16	2.5
T_o (K)	870	690
kT_o (eV)	0.075	0.060
Max Current (A)	2.49×10^{-6}	1.37×10^{-5}
Average Off Current (A)	4.01×10^{-11}	6.51×10^{-10}
On-Off Ratio	6.4×10^{5}	2.1×10^{5}

These values were a lot closer to each other than expected, as with the crystalline grains within the polycrystalline OSC it was expected that the device would exhibit an ideality closer to unity. The similarity to that of the disordered material is further evidence that the conduction within the material could be restricted, if not primarily controlled, by the disordered grain boundaries. It is also clear that the Lisicon™ S1200 has a higher on current, however the PTAA device had less off current leakage making the on-off ratios within the same order of magnitude.

3.5 Thin Film Transistor Fabrication

3.5.1 Photolithography Samples Technique

Two types of TFT were fabricated and will be compared at the end of this section. They have been named based on the method of device formation. The first and most common process was one using photolithography to define the feature sizes of the devices.

Photolithography is used to define components. Factors such as the development time, solvent used and exposure time all can affect the process and samples can be over or under developed if all of the factors are not carefully taken into account. These variables will be explored in more detail in Section 3.5.1.

Step 1 - Preparation of Substrate

The substrate for TFTs was prepared in the same way as those detailed in Section 3.2, the only difference being that the glass slides were cut to approximately 500 mm. This allowed extra space to clamp the slide for the anodisation technique detailed in Step 3.

In order to obtain as uniform a layer as possible, the samples were loaded and held on a plate that rotated during deposition. Three separate coils were used to melt the aluminium with the pressure being regulated to $<3x10^{-7}$ mbar in between each stage of deposition. This allowed for careful control of the deposition rate and thickness, the latter of which was chosen as desired depending on the sample (this is furthered detailed in Chapter 4). Deposition rate was kept constant at 0.5 nm/s. It was found that this rate was achieved at an evaporating pressure usually in the range of $2.0 – 2.5 x10^{-6}$ mbar and when the voltage applied to the coils was in the range of 30 - 35 V. These values were observed in the majority of processes.

After the aluminium layer was obtained the samples were annealed for a minimum of 2 hours at 106^{o} C in a nitrogen filled hotbox. It had been found in past experiments within the research group that this improved the quality of the oxide grown in the anodisation process and had been optimised to this temperature.

Step 2 - Aluminium Evaporation

As the technique used consisted of an aluminium bottom gate, the second step in processing involved a 250 nm aluminium layer evaporated at a sufficiently low pressure within the evaporation chamber. As the aluminium layer is later used to produce the Al2O3 dielectric layer, the uniformity and quality of the layer is crucial to produce a viable oxide. The aluminium wire used was thoroughly cleaned beforehand in a two stage sonification and rinse process in both acetone and DIW. The wire was dried with a nitrogen gun before any residual moisture was removed in a hotbox at 120 °C.

Step 3 - Anodisation

The dielectric layer of the TFT is formed by growing an Al2O3 layer using an aqueous citric acid solution. The solution was mixed to have a concentration of 0.001 mmol and the anode was a sheet of high grade platinum. The anodisation rig consisted of the positive supply of a voltage connected to the sample through a 1 Ω resistor and the negative connected to the platinum sheet. The platinum and sample were lowered into the acid solution serving as the cathode and anode respectively and a current meter was connected to monitor the current across the resistor. A voltage was applied to the circuit causing oxidisation at the anode. As the thickness of the oxide is proportional to the applied

voltage, the voltage was set at a level dependent on the thickness required. This was one of the factors altered for the experiments documented in Section 4.4.2. The anodisation stage proved a strong indicator for the quality of the cleaning and evaporation stages prior to it as a poor aluminium layer has a detrimental effect on oxide growth [15]. After each anodisation stage samples were checked for etching at the boundary as well as for any dust spots or etching within the body of the sample. Two different substrates, Substrate 1 and Substrate 2 (distinguished only by manufacturer) were used to obtain the best performance. Based on the quality of the oxide, Substrate 2 consistently had a high level of etching and out of 18 samples produced none produced an oxide fit for purpose. Substrate 1 was not free from etch spots however, these could be reduced by being more thorough in the cleaning process and with careful control of aluminium deposition. The only notable difference between the two substrates was an extra factory cleaning process. It is possible that there was some reaction based on this process or some residue that was unable to be removed by the cleaning process. As the details of the pre-lab cleaning by the manufacturer is unavailable, the only conclusions that can be drawn is further proof that substrate quality has a direct impact on oxide quality.

Step 4 - Evaporation and Patterning for Source and Drain Contacts

Using the same process as detailed in Section 3.3, gold was evaporated over the whole surface of the sample to a thickness of 35 nm. Unless evaporation took place immediately after anodisaton, each sample was subject to a cleaning process of 15 minutes in IPA, rinse with DIW and dried in hotbox at 120 ° C for 15 minutes. As with diodes, evaporation took place at approximately $2x10^{-7}$ mbar and monitored, carefully adjusting the applied current to maintain a rate of 0.1 nms^{-1}.

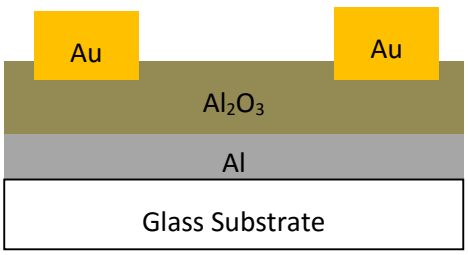

Figure 3.5-1 Cross section of device with all layers previously mentioned including gold source and drain contacts. These were patterned using photolithography.

Photoresist was applied to the gold layer and aligned under a UV light for 12 s through a device mask. When UV light is passed through the mask the photoresist reacts to the UV light and either cross-links to resist the development stage or dissociates in order to be removed at the development stage. In this case HPR504 was spun, a negative photoresist, and the samples were exposed for 12s under the

UV light. The sample was then developed in HPRD429 for 15s and then rinsed in DIW. To remove the unwanted gold, the sample was rinsed in Microstripper 2001 for increments of 5 mins at a time, rinsing with DIW in between doses to check under the microscope if all unwanted gold had been removed. This was done until only source and drain contacts remained.

Step 5 - -Application of OSC

The final step in the fabrication process observed was the application of the OSC. The semiconductor can be applied by either a drop method or spinning method.

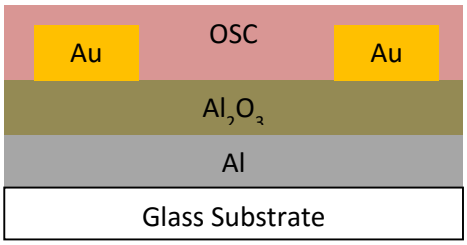

Figure 3.5-2 – Cross section of OTFT including the OSC layer spun over device.

Although the diode samples did not respond well to spinning deposition (the layers were too thin and devices failed), the results for OTFTs were more reliable and therefore it was the preferred method compared to drop casting which allows less control over thickness. As stated before another method of application of OSC is through vacuum evaporation – a technique that would achieve a uniform distribution with controlled thickness rather than the methods mentioned already.[16]

3.5.2 Shadow Evaporation Samples Technique

A second method of TFT fabrication was carried out at Merck Chemicals Ltd. Contrary to the Photolithography Patterned Samples; these samples were made in a non-clean environment and used a shadow mask technique for evaporation. The device had a bottom gate structure, however instead of an Al_2O_3 layer for the oxide, a single, organic dielectric Lisicon™ D206 was used. Without the use of Al_2O_3, the gate contact was not restricted to Aluminium and instead, silver was used for all contacts. The use of a dielectric resulted in a second Self-Aligned Monolayer (SAM) Lisicon™ M011 being used as well as a contact solution Lisicon™ M001. These layers enhance adhesion between the respective organic materials and the underlying layers. The procedure steps are detailed below.

Step 1 - Substrate Treatment

Four Corning Eagle 2000 slides were placed into a single slotted beaker filled with 3% Decon 90 and sonicated for 15 minutes at 65 °C. After thorough rinsing with DIW the slides were then sonicated in DIW. The rinsing process was then repeated followed by sonication in IPA. The final cleaning stage involved an IPA rinse for each slide on a spinner. After the cleaning procedure the surface energy is reduced and yields a more applicable surface for the deposition stages - it was possible to see the difference in the surface texture of the glass and a water beading test could be used to see the effectiveness of the cleaning procedure proving a change in hydrophobicity.

Step 2 - Gate Evaporation

Following the cleaning the first major process step was the evaporation of the gate contacts. The evaporation took place through an evaporation mask in order to shape the gate contacts. A bead of silver was used and evaporated at a pressure of $5x10^{-6}$ mbar at a rate of 0.09 nm - 0.12 nm until a layer of 35 nm was obtained. The mask used allowed for 6 gate lines to be evaporated that would match up with the corresponding source/drain mask that would be used in later stages.

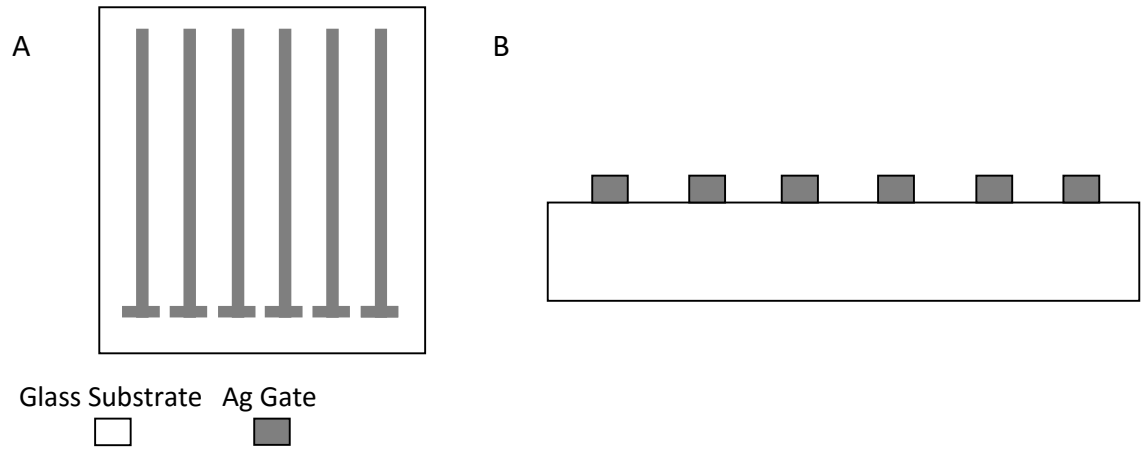

Figure 3.5-3 - Diagram of Device after gate evaporation. Line of evaporated silver form the gates of devices. Being able to reduce the gate area reduces unnecessary capacitances caused by fields across the dielectric forming anywhere other than the channel.

Step 3 - M011 Deposition

In order to facilitate adhesion between the glass substrate and Lisicon™ D206, the SAM Lisicon™ M011 was deposited over the substrate and gate contacts. After a spinning process, the remaining Lisicon™ M011 was then evaporated from the sample at 100 °C on a hotplate, left for one minute to cool and then spin-rinsed with IPA. This process had previously been optimised in order to apply the right amount of solution for adhesion.

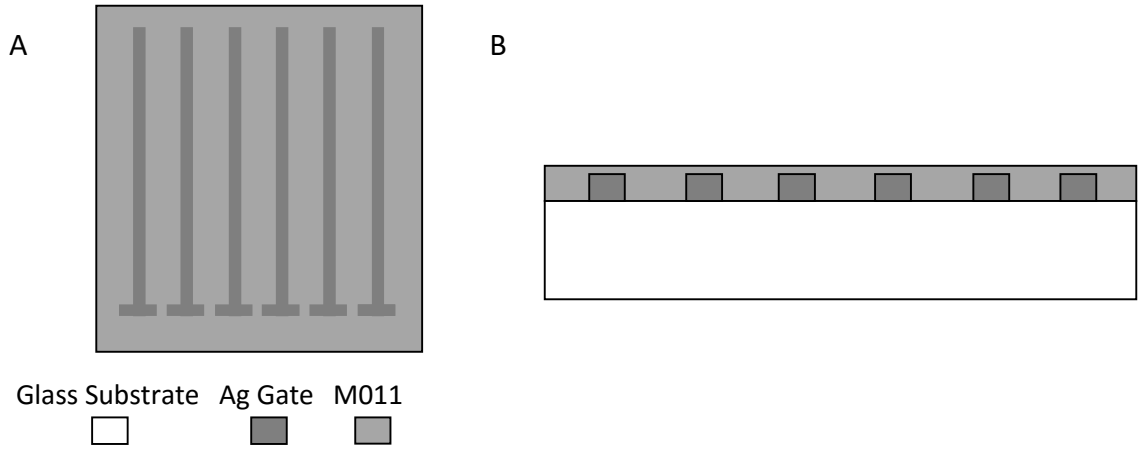

Figure 3.5-4 - Surface contact enhancer is deposited over silver and glass to improve adhesion between the dielectric and the gate.

Step 4 - Dielectric Deposition

The dielectric currently being used for this TFT process was Lisicon™ D206. With a dielectric constant of 2.9, D206 is a low-k dielectric and responds well to cross-linking, therefore is a candidate for patterned dielectrics and has potential in circuit design due to the reduction of internal capacitances if the overlap between the gate and source drain materials can be limited. This is explored further in 5.4. The solution used generally is a 13% aqueous solution, however, a lower concentration was made for comparison in order to gauge the possibility of scaling by reducing concentration, the results of which will be explored in Section 4.4.4. In experiments where only the OSC process was altered a 13% solution was always used.

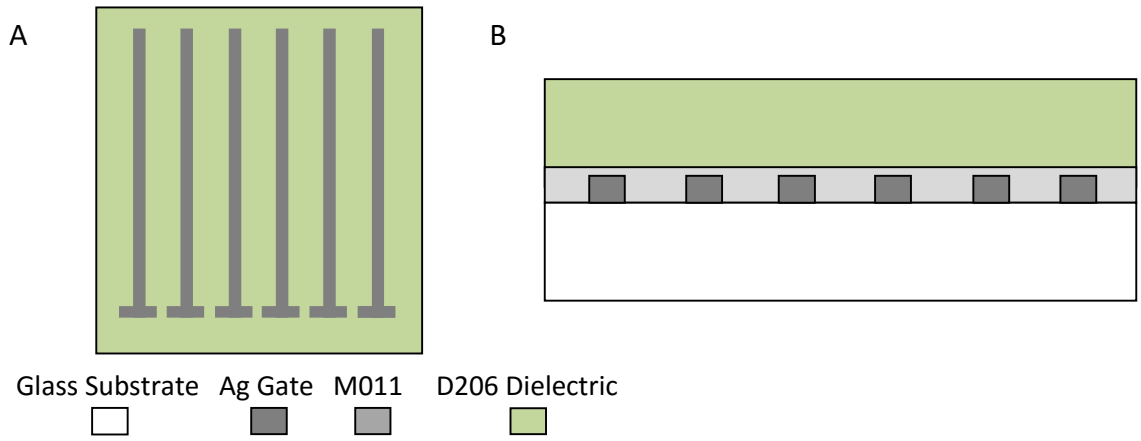

Figure 3.5-5 – Organic dielectric layer deposited over the contact solution and crosslinked under UV Light

The optimised process for D206 application was applying the dielectric onto the slides with a pipette

and spinning the sample at 1500 rpm for 30 s. This is proven to produce a thickness of approximately 1 µm dielectric layer. Once the dielectric had been applied samples were annealed at 120 °C for 1 minute and then cooled. Samples were then cross-linked to enhance the bonding of molecules by applying a light with a high intensity wavelength (in this case UV). The energy from the light causes the polymers to bond and form a firmer surface that is harder to break at later process steps. This process can be used for patterning dielectrics if done through a mask as it allows for desired sections to be firmed by cross-linking and for unwanted parts to be removed in a development stage. Various exposure times were investigated for this process and the results are detailed in Table 3.5-1.

Each sample was exposed one at a time beginning with an arbitrary exposure time within a 0 – 1 s range. The sample was then developed and the height of the remaining pattern was measured using the profiler in order to assess the performance of the combination.

In order to demonstrate the process a dummy gate mask was used as the exposure mask. The aligner was set up with a UV 300 mirror at a wavelength of 302 nm at a power of 0.6 $mWcm^{-2}$. Because of the power of the UV, the exposure time was very short.

Table 3.5-1 – Thickness of dielectric layer measured for 6 different dielectric samples. These were measured by a profiler after different exposure times for cross linking. The quality of these layers are also noted with a graphical representation in Figure 3.5-6 and further detailed in .

Sample	Time (s)	Thickness and comment
1	0.70	0.577 µm – thinner than expected. Exposure time needs to be reduced.
2	0.50	0.474 µm – 15 nm deep remainder. Exposure time too long.
3	0.10	0.305 µm – Pattern only 1/3 of expected thickness and cracking on pattern seen. Either too short exposure time or too long development time. Next sample will be developed for shorter period
4	0.10	0.3529 µm – developed for shorter time and still eroded – exposure time must be too short and dielectric not crosslinked enough.
5	0.20	Spoiled in fabrication, no results.
6	0.35	0.3883 µm – eroded so exposure time too short.

In order to test the result of the exposure and development a scratch needs to be made across the substrate and the depth of the scratch measured in the profiler. Ideally, in this case, the thickness of the dielectric should be 1µm – this would be as shown in Figure 3.5-6 a) below.

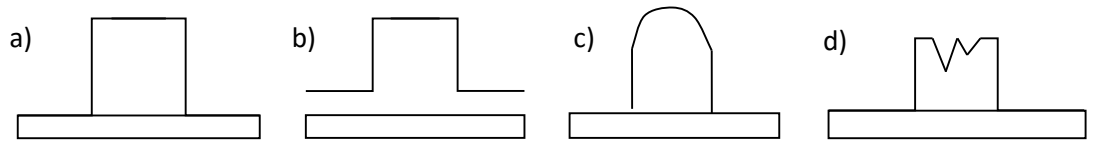

Figure 3.5-6 Graphical representation of problems encountered with pattering process for dielectrics. These 4 situations a)-d) are described in the corresponding section of Table 3.5-2

Table 3.5-2 – Details of problems caused in patterning process including the reasons the problem occurred and the solution. Each situation is linked to Figure 3.5-6.

Problem	Caused by	Solution
Un-removed dielectric outside of pattern (Figure 3.5-6 b))	Too long exposure time or too little development time. If the UV is exposed for too long it can diffract under the protected parts and harden the unwanted dielectric.	In the case of the former decrease the exposure time without exposing for so long that the pattern will not crosslink. Increase the development time if the latter.
Bad edge definition, too rounded (Figure 3.5-6 c))	Too long a development time and therefore corners of the edges begin to round off	Reduce development time
Cracking in the pattern or pattern begun to remove (Figure 3.5-6 d))	Too short and exposure time and therefore developed too early	Increase the exposure time
Loss of thickness	Too long an exposure time.	Exposure time must be decreased to optimum.

In the case of the standard TFT fabrication, patterning was not required and the whole of the sample was cross-linked before evaporation.

Step 5 - Source/Drain Contact Evaporation

Similarly to the gate evaporation, silver source and drain contacts were evaporated through a mask in order to line up the contacts correctly above the gate contacts. The formation of the mask was such that 21 TFTs of W = 1000 µm were evaporated over each gate contact with alternating lengths of 10 µm, 20 µm and 50 µm vertically along the gate and of 2 different contact sizes (determined by the area of the gold contact) alternating from gate to gate. Only the 1000 x 50 μm^2 TFTs were measured in these experiments producing 18 TFTs per sample. The evaporation was complete at a thickness of 35 nm.

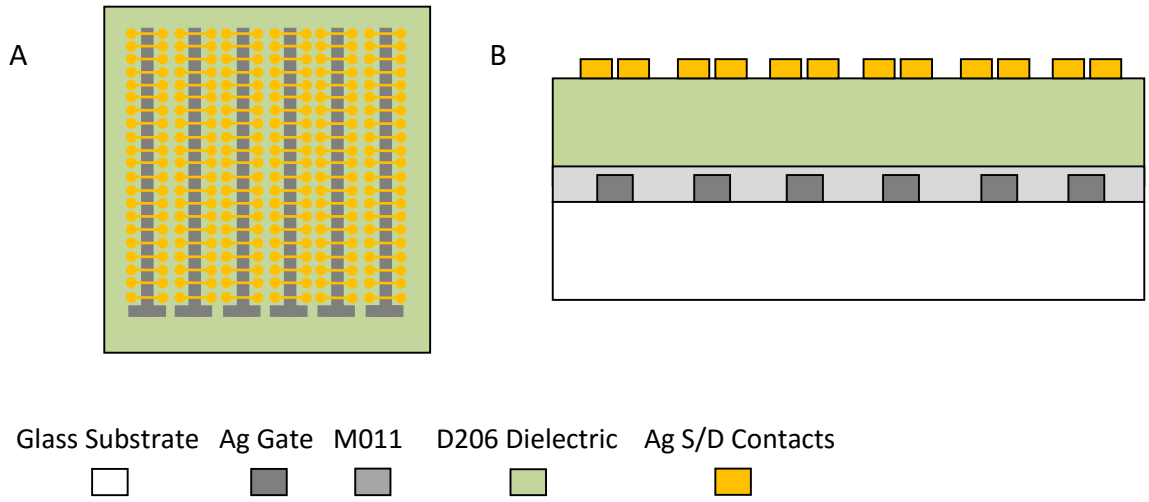

Figure 3.5-7 – A second layer of silver is evaporated to create source and drain contacts. This was done through a shadow mask to form the shape of the contacts.

Step 6 - Lisicon™ M001 Contact Solution

The penultimate process step involved applying a contact solution Lisicon™ M001 to the sample in order to improve contact between OSC and dielectric layer. Similarly to the previous contact solution the Lisicon™ M001 was dripped onto each sample. Each sample was then spin-rinsed with IPA. After this step has taken place OSC deposition should be done as soon as possible.

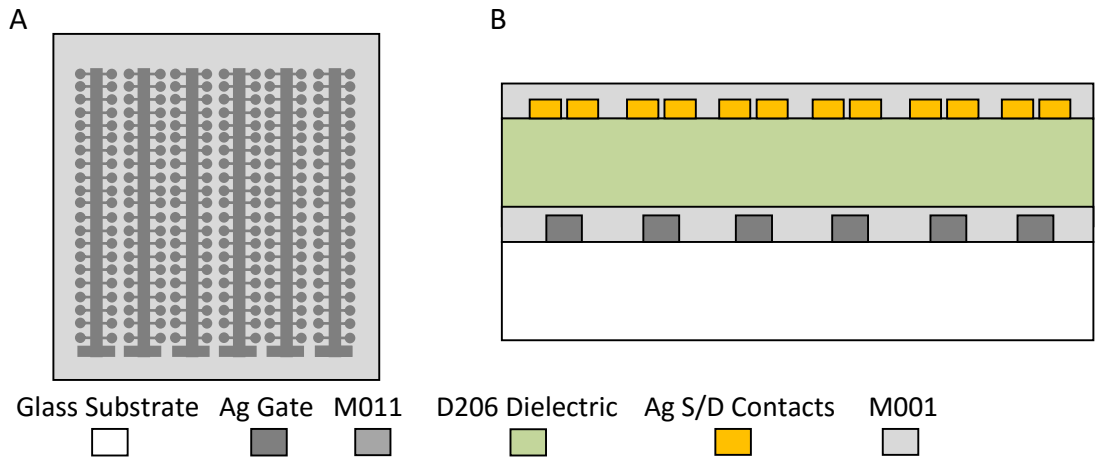

Figure 3.5-8 - A second contact layer is deposited to facilitate easy conduction between the contacts and the semiconductor.

Step 7 - Application of OSC

The semiconductor used in this process was Lisicon™ S1200, a p-type crystalline semiconductor. The concentration in the general case is 2% (though this was varied in experimentation as detailed later on). The optimised process for OSC application is spinning at 1500 rpm for 30 s. The devices were then

annealed on the hotplate at 120 °C for 1 minute. The spinning had to be done immediately to prevent the OSC from drying too fast before it had been evenly applied across the whole surface of the sample.

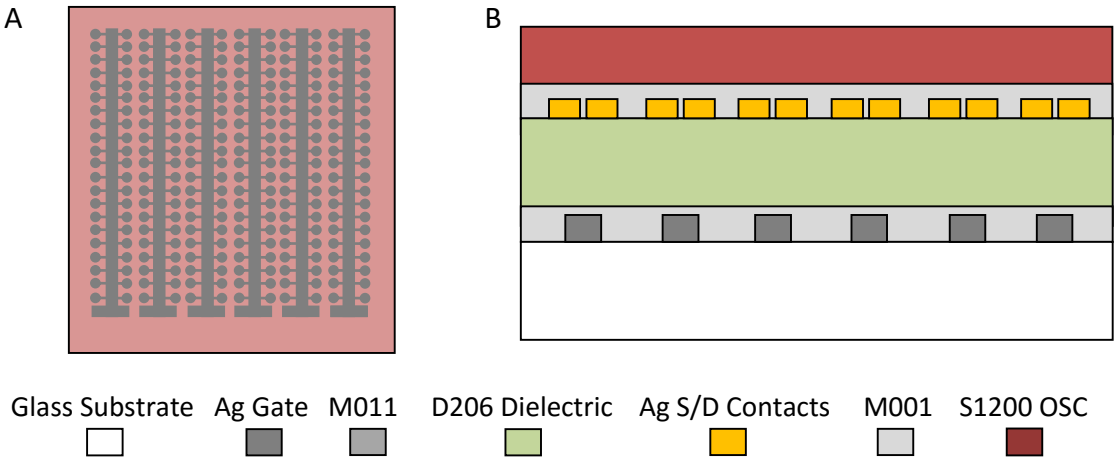

Figure 3.5-9 - Organic semiconductor is deposited over whole sample.

3.6 Capacitor

The structure of the organic capacitor is shown in Figure 3.6-1. The process consists of steps 1-4 of the photolithography sample method as detailed in Section 3.5.1. As the MOSC has a top contact structure, photolithography is not a necessary stage so the OSC can be applied directly to the Al_2O_3 layer. The gold contacts can then be evaporated as with Step 5 of the shadow evaporation method.

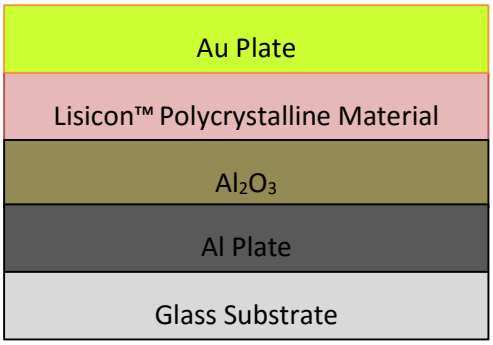

Figure 3.6-1 –Structure of MOSC. This consists of an Al plate evaporated on a glass substrate, an Al_2O_3 dielectric anodised as with TFT. An OSC is then deposited with a gold layer on top as a second plate.

This produced devices of 1 mm^2. It should be noted that Metal-Insulator-Metal capacitors (MIMs) were also fabricated which consisted of the same structure as the MOSC, however the semiconductor stage was missed out. This allowed for the capacitance of the oxide layer to be found for the different thicknesses of oxide.

3.7 TFT Characteristics

3.7.1 Extraction of Parameters for Disordered Equation

Analysis is carried out using the equation models derived in Chapter 2. The transconductance, I_{DS} vs V_{GS} and the output characteristics, I_{DS} vs V_{DS}, were measured using a Hewlett Packard 4155b Semiconductor Parameter Analyser. Devices were characterised by either applying a varying V_{GS} at a constant V_{DS} or applying a varying V_{DS} at various V_{GS} values. The results were analysed to extract the parameters necessary to test the modelling equations developed in Chapter 2.

Two different methods were used for producing the important parameters *K* and *m* – one for the disordered equations and ones for the polycrystalline. These are compared at the end of Section 3.7.2 with the method detailed in the following sections.

The linear and log plot of the $I_{DS}V_{GS}$ characteristics of one of the devices fabricated using the photolithography method in Section 3.5.1 is show below. The device measured had *W/L* = 150, and oxide thickness of 32 nm with a Lisicon© S1200 polymer. They were measured with V_{DS} = -5 V.

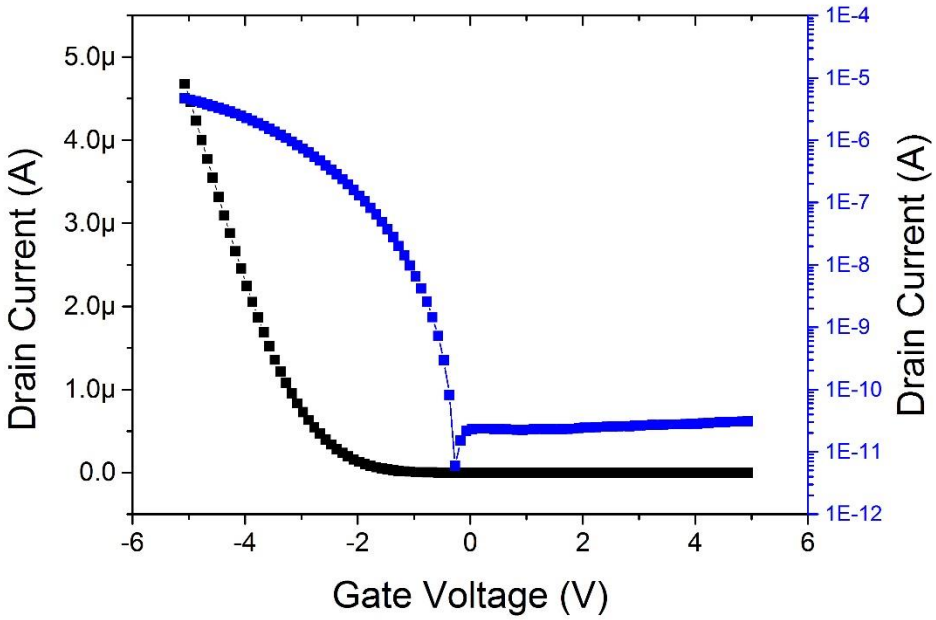

Figure 3.7-1 – Log and linear plot of I_{DS} current measured in saturation for a device of 150 W/L. The V_T was measured as -1.6 V and an on-off ratio of 5 orders of magnitude. V_{DS} = -5 V.

As the trace was measured in saturation, a threshold voltage V_T was extracted using the slope of $I_{DS}^{0.5}$ and found to be -1.6 V as shown by the graph in Figure 3.7-2

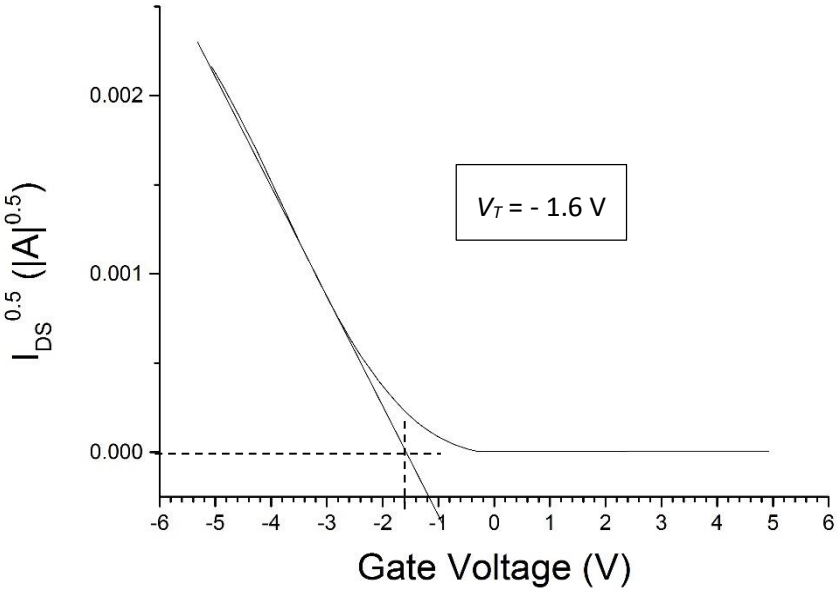

Figure 3.7-2 – $I_{DS}^{0.5}$ plot to extract threshold voltage of device in saturation. This yielded a V_T of -1.6 V.

The derivation for I_{DS} in both linear and saturation mode for disordered materials are shown in Eqn. 3.7-1 and Eqn. 3.7-2 respectively.

$$I_{lin} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(\frac{(V_G - V_T)^{(2m+2)}}{2(m+1)(2m+1)} - \frac{(V_G - V_T - V_D)^{(2m+2)}}{2(m+1)(2m+1)}\right), \qquad \textit{Eqn. 3.7-1}$$

$$I_{sat} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(\frac{(V_G - V_T)^{(2m+2)}}{2(m+1)(2m+1)}\right). \qquad \textit{Eqn. 3.7-2}$$

It can be seen that Eqn. 3.7-2 consists of a power relationship of:

$$I = K_{dis}(V_G{}')^{m_{dis}}, \qquad \textit{Eqn. 3.7-3}$$

with the saturation form of I_{DS} being a function of V_G' (where $V_G' = V_{GS} - V_T$) multiplied by a constant K_{dis} to some power factor m_{dis} where

$$K_{dis} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)} \quad \textit{Eqn. 3.7-4}$$

and

$$m_{dis} = 2m + 2. \quad \textit{Eqn. 3.7-5}$$

These parameters can then be rearranged to isolate that material properties *m* and *K* as

$$m = \frac{m_{dis} - 2}{2}, \quad \textit{Eqn. 3.7-6}$$

and

$$K = \frac{K_{dis}L\{2kT_C\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)}{WC_0{}^{2m+1}} \quad \textit{Eqn. 3.7-7}$$

for the disordered equation.

By taking the logarithms, the gradient can be isolated. Using the derivative of the drain current against gradient produces a straighter line in order to get a more accurate slope from the data. These expressions are detailed in Eqn. 3.7-8 and Eqn. 3.7-9.

$$\frac{dI_D}{dV_G} = m_{dis}K_{dis}V_G{}^{m_{dis}-1}, \quad \textit{Eqn. 3.7-8}$$

$$\log\left(\frac{dI_D}{dV_G}\right) = \log(m_{dis}K_{dis}) + \log(V_G)^{m_{dis}-1}, \quad \textit{Eqn. 3.7-9}$$

The logarithm of the transconductance, $\frac{dI_D}{dV_G}$ was plotted against the logarithm of V_G' (where $V_G' = V_{GS} - V_T$) and the gradient of the saturation region was fitted to isolate a slope and intercept, as shown in Figure 3.7-3.

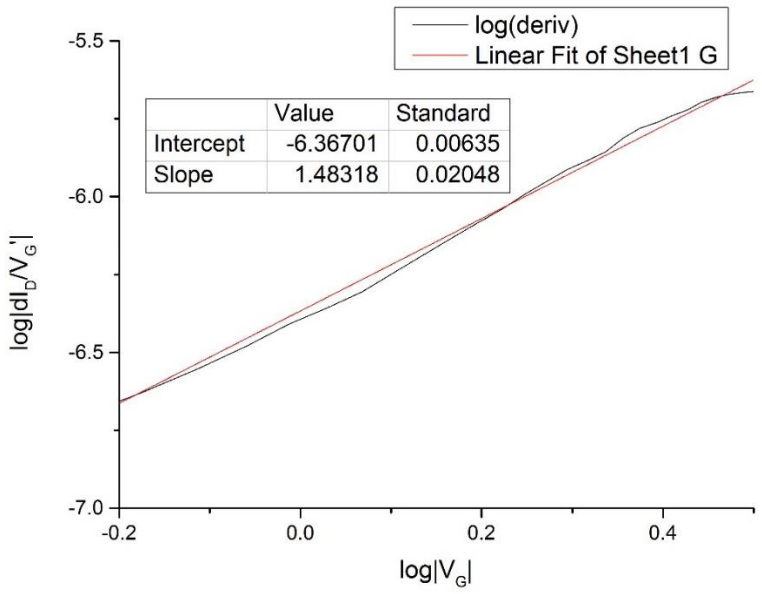

Figure 3.7-3 – Plot of log(dI_g/V_G) against log(V_G') in order to isolate the slope and intercept in order to extract the mobility parameters m and K.

The gradient and intercept of the line can then be used to find the parameter values based on Eqn. 3.7-9.

$$m_{dis} = slope + 1 = 2.48318 \qquad \textit{Eqn. 3.7-10}$$

$$K_{dis} = \frac{10^{intercept}}{m_{dis}} = 1.7297 \times 10^{-7}\,. \qquad \textit{Eqn. 3.7-11}$$

These values were then substituted into Eqn. 3.7-5 and Eqn. 3.7-7 to produce m = 0.74 and K = 2.5295 x 10^{-11} AV^{-m}. With m and K obtained, further values could be derived such as T_C.

$$T_C = mT + 1 = 522\ K \qquad \textit{Eqn. 3.7-12}$$

A Matlab program was designed to generate the values of I_{DS} using the parameters extracted and the disordered equation. This was then plotted against the experimental data, the result of which is shown in both log and linear form in Figure 3.7-4.

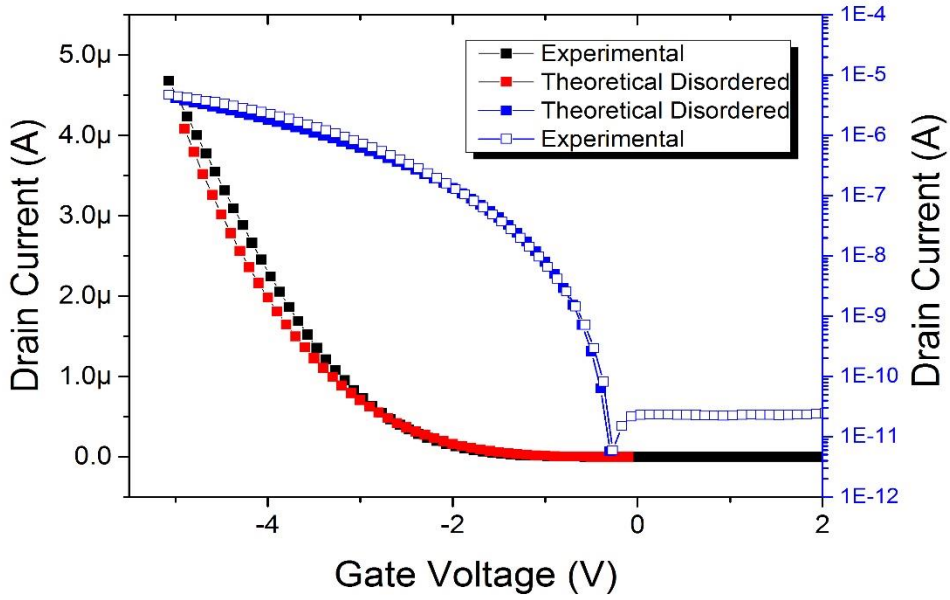

Figure 3.7-4 – Comparison of $I_{DS}V_{GS}$ characteristics for both the experimental, measured value and the theoretical model plotted as a combination of the disordered equation stated in Section 2.9 and the parameters extracted from the fabricated devices.

These results show a decent fit with the biggest discrepancies occurring at higher V_{GS} values. It is possible that the values in the saturation region are caused by a drain leakage causing a drain voltage dependency. This would corroborate with the output characteristics of some measured devices that show a continuing, albeit gradual, increase in current where ideal characteristics would otherwise be flat.

3.7.2 Extraction of Parameters using Polycrystalline Theory

The theory for the polycrystalline derivation is based around the same principle as the disordered, however an extra stage is needed due to the drift and diffusion parameters within the equation.

First of all the V_{Tdiff} and V_{Tdrift} were isolated. This can be done by comparing the transconductance characteristics for 3 different values of V_D. Based on the theory explored in Chapter 2, the two regions of operation can be identified as indicated in Figure 3.7-5.

For this diffusion model,

$$I_{diff} = K_{diff}\left(V_{GS} - V_{Tdiff}\right)^{c_{diff}},$$

Eqn. 3.7-13

as detailed in Chapter 2.

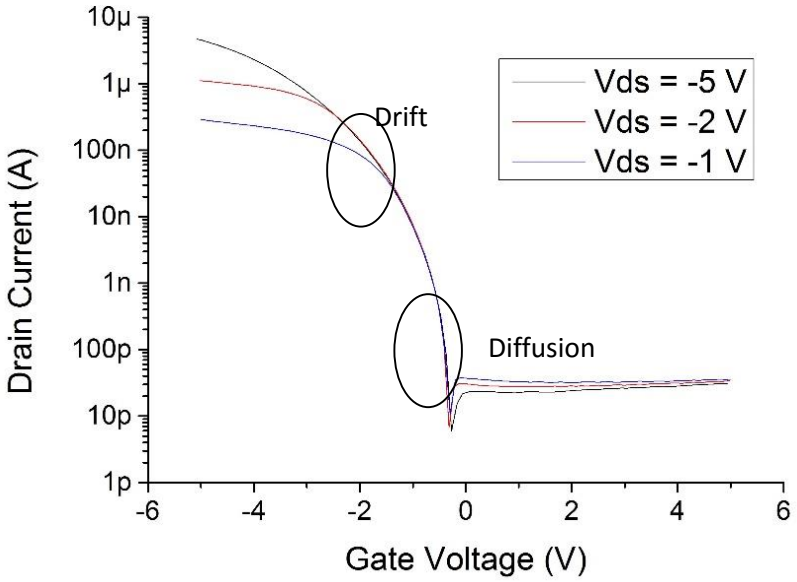

Figure 3.7-5 –Drift and diffusion areas of operation with the points where the respective threshold voltages occur circled. By examining these regions, these values can be extracted and used to model the polycrystalline equation.

The diffusion threshold sees the point where the transistor is in operation, but V_{GS} is much lower than V_{DS} which means that it still impacts the current and therefore each different V_{DS} current will follow a different path.

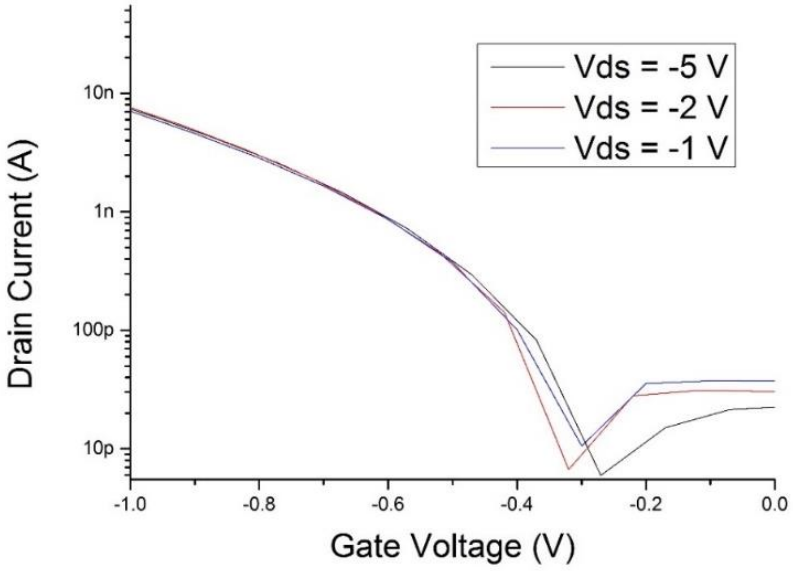

Figure 3.7-6 Isolating the diffusion threshold. At this point the different values of V_{DS} converge together as the I_{DS} is independent of V_D.

While these values all vary in the subthreshold region, the important point to note is the point at which all V_{DS} converge together.

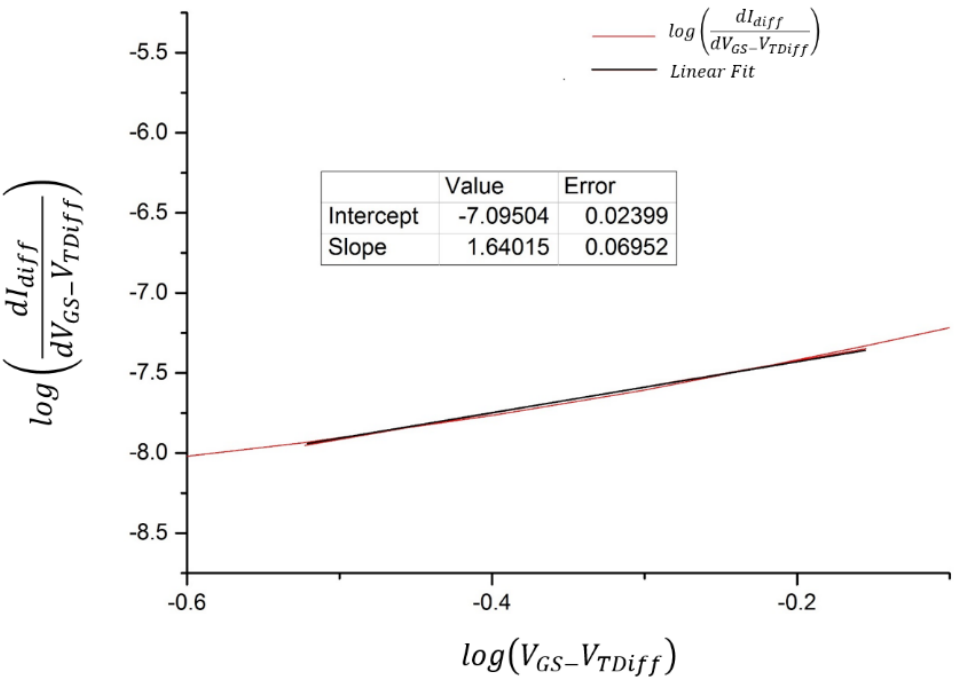

Figure 3.7-7 Log plot used to isolate m and K for diffusion equation. This takes the slope and intercept within the diffusion region to extract these values which can then be used for the model.

It is here that the diffusion threshold can be obtained as this marks the point when there is no longer a V_{DS} dependence. For this device, V_{diff} was found to be 0.4 V. This can then be fitted into the polycrystalline drift equation.

As with the case for the disordered, a log plot of this form at the point of the diffusion threshold provides the slope to give values of K_{diff} and c_{diff} as given by the intercepts.

$$c_{diff} = slope + 1$$

Eqn. 3.7-14

$$K_{diff} = \frac{10^{intercept}}{c_{diff}}$$

Eqn. 3.7-15

For this TFT these values were c_{diff} = 2.64 and K_{diff} 3.04x10^{-8} AV^{-cdiff}.

A similar process can be used for the drift region, but this is found at the point when the characteristics diverge. At this point the respective V_Ds are now no longer bigger than the gate voltage and therefore the dependence returns. This means that the drift threshold has been met and once again the log plot of the derivative can be used to isolate the appropriate parameters.

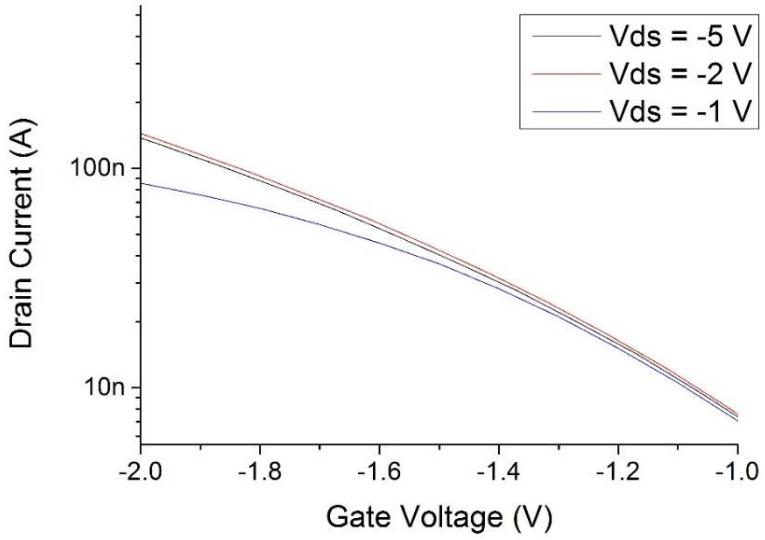

Figure 3.7-8 - Comparison of V_{DS} transfer characteristics to isolate drift threshold. The drift mobility parameters can then be extracted from the log plot above this threshold.

The log plot for this point is shown in Figure 3.7-9 with the slope and intercept of a linear fit isolated within the graph.

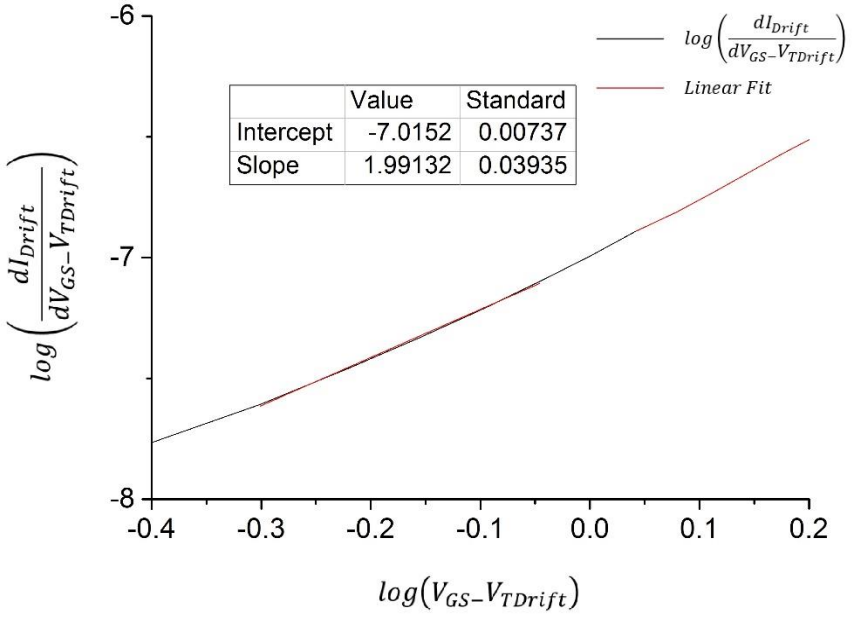

Figure 3.7-9 Log plot of derivative in order to isolate m and K for drift region.

For the drift section of the data, the K_{drift} and c_{drift} were given by:

$$c_{drift} = slope$$

Eqn. 3.7-16

$$K_{drift} = \frac{10^{intercept}}{c_{drift} + 1}.$$

Eqn. 3.7-17

For this transistor, the drift values were found to be V_{drift} = 0.9 V, C_{drift}=1.99 and K_{drift}=3.22x10^{-8} AV$^{-cdrift}$.

As with the disordered model, the polycrystalline parameters for the devices were put into a Matlab program designed to plot the individual regions. It can be seen from the data in Figure 3.7-10 that the polycrystalline fit produced a viable estimate, however the disordered form had a closer accuracy. This was unexpected, considering the materials being tested are polycrystalline, however it is possible that this was due to the accuracy of the drift and diffusion threshold extraction.

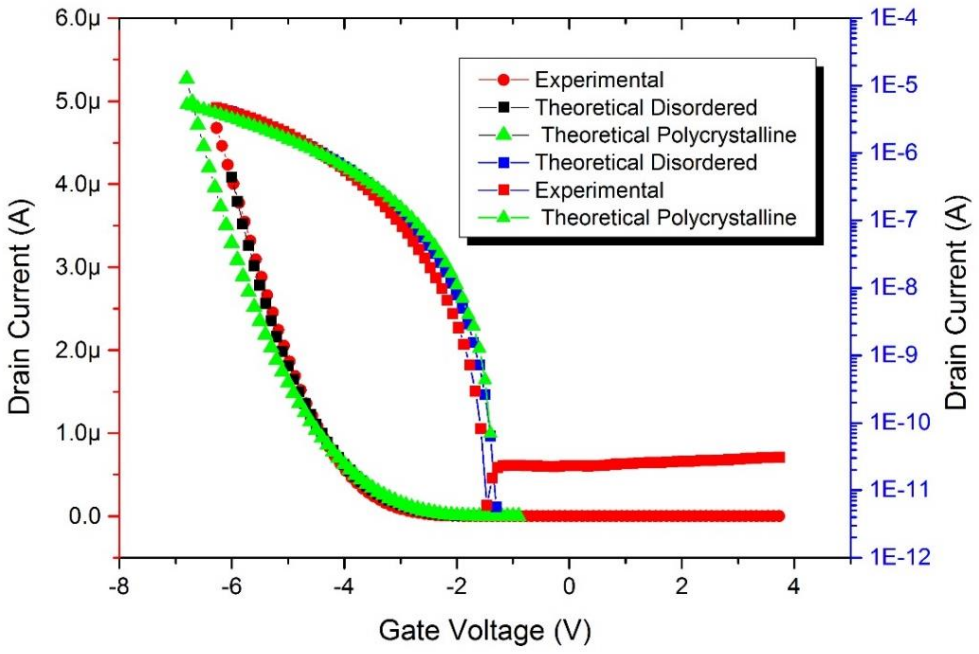

Figure 3.7-10 – Log and linear plots for the modelled I_{DS}. The green trace indicates the theoretical polycrystalline model, plotted using the extracted m and K values for the drift and diffusion regions. The blue and black traces show the theoretical disordered model as plotted in Section 3.7.1 and the red shows the measured experimental results All traces are at a V_D = -5 V.

It is not unexpected that the polycrystalline material is exhibiting a similar behaviour as a disordered material as the grain boundaries within the material are disordered. This is further evidence that they control the current through the device. Combined with the diode results, these results indicate a higher level of disorder within this particular material compared to other polycrystalline materials.

3.7.3 Mobility

There are various methods that can be used to extract a mobility value. The simplest of these is to apply the same theory as with the crystalline form.

$$I_D = C_0 \mu \frac{W}{L}\left[(V_G - V_T)V_D - \frac{{V_D}^2}{2}\right] \qquad \textit{Eqn. 3.7-18}$$

If using the crystalline form, the mobility can be derived from the unsaturated form in Eqn. 3.7-18 at very low V_D values, assuming the term $\frac{{V_D}^2}{2}$ can be ignored, giving

$$\frac{dI_D}{dV_{GS}'} = C_0 \mu \frac{W}{L}(V_D). \qquad \textit{Eqn. 3.7-19}$$

Here $V_{GS}' = V_{GS} - V_T$. Hence, an average mobility can be found from

$$\mu = \frac{\frac{dI_D}{dV_G} L}{W C_0 (V_D)} \qquad \textit{Eqn. 3.7-20}$$

The same principle can be applied for the disordered materials equation derived in Chapter 2.10. This is justified by the good fit to device output characteristics. Recall:

$$I_{dlin} = \frac{W}{L} \frac{K {C_0}^{2m+1}}{\{2kT_C \varepsilon_0 \varepsilon_S\}^m} \left(\frac{(V_G - V_T - V_D)^{(2m+2)}}{2(m+1)(2m+1)} - \frac{(V_G - V_T)^{(2m+2)}}{2(m+1)(2m+1)} \right). \qquad \textit{Eqn. 3.7-21}$$

Eqn. 3.7-20 is equated to Eqn. 3.7-18 to produce an expression for an average and effective mobility:

$$\mu = \frac{KC_0{}^{2m}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)}\left(\frac{(V_G - V_T - V_D)^{(2m+2)} - (V_G - V_T)^{(2m+2)}}{(V_G - V_T)V_D - \frac{V_D{}^2}{2}}\right). \quad \textit{Eqn. 3.7-22}$$

This has a dependence on the extracted parameters *m* and *K* as well as all of the relevant voltages, however it loses the dependence on the aspect ratio of the device.

The same process can be used for the saturation mobility with the respective saturation equations.

$$\mu = \frac{KC_0{}^{2m}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)}(V_G - V_T)^{2m}. \quad \textit{Eqn. 3.7-23}$$

Plotting mobilities for the device in Figure 3.7-1 using Eqn. 3.7-23 produces Figure 3.7-11.

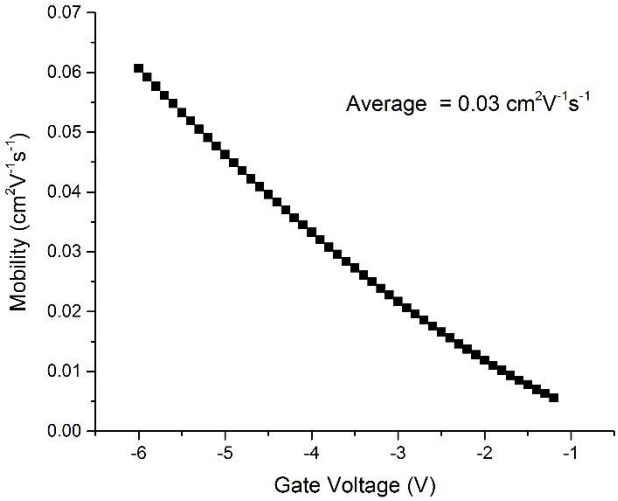

Figure 3.7-11 – Mobility for the extracted m and K values of the 150 W/L device. These values of m and K were calculated the theory stemming from the expression in Eqn. 3.7-3 and with the mobility equation in Eqn. 3.7-23.

As a single mobility value cannot be extracted, the average is taken to be 0.03 $cm^2V^{-1}s^{-1}$. This can be used as a comparative analysis for performance of devices.

3.8 Processing With Copper

Over a significant part of the early fabrication stages there was an issue with gold adhesion. At the development stage of fabrication the gold was peeling away from the Al_2O_3 at the patterning stage and in order to produce any devices compromises were being made with development times to the detriment of the devices. A previous study[17] had suggested that copper may be a better alternative

due to its better adhesion, as well as evidence of improved performance. Earlier devices were repeated with copper and the fabrication process was altered to accommodate copper instead of gold. The basic structure of the device is shown in Figure 3.8-1 for the diode and TFT respectively.

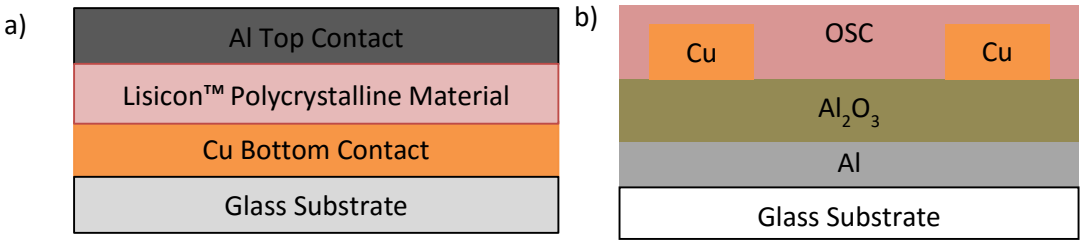

Figure 3.8-1 a) Copper diode structure featuring a copper Ohmic contact instead of gold. A contact solution treatment was used in order to enhance Cu/OSC adhesion. b) Copper TFT structure showing Cu source/drain contacts.

Based on the theory in Section3.4, in order to form an Ohmic contact the work function of the metal needs to be greater than that of the p-type semiconductor. Table 3.8-1 shows the 3 work functions of copper, gold and aluminium. As the latter functions as a Schottky contact and gold as a proven Ohmic contact, it can be deduced that the work function of Lisicon™ S1200 is somewhere within the region of 4.08 and 5.10 eV.

Table 3.8-1 – The work functions of gold, copper and aluminium to show their attributes as a Schottky or Ohmic metal.

Metal	Work Function (eV)
Copper	4.65
Gold	5.10
Aluminium	4.08

With the work function of copper being 4.65 eV, it falls within this range, however as this number is much smaller than that of gold, the contact resistance will not be as low as it would be with a larger work function difference. Figure 3.8-2 shows the $I_{DS}V_{GS}$ characteristics of a copper TFT and a gold TFT, both with a *W/L* of 150, t_{ox} = 32 nm and the same semiconductor deposition process. The data shows that the copper produced inferior on currents although the off currents were in the same range. As explained further in Chapter 4, the off current leakage is heavily dependent on oxide and semiconductor thickness which could explain why the source/drain material doesn't show a notable

effect on the off current. Another difference was the significant reduction of hysteresis with the copper.

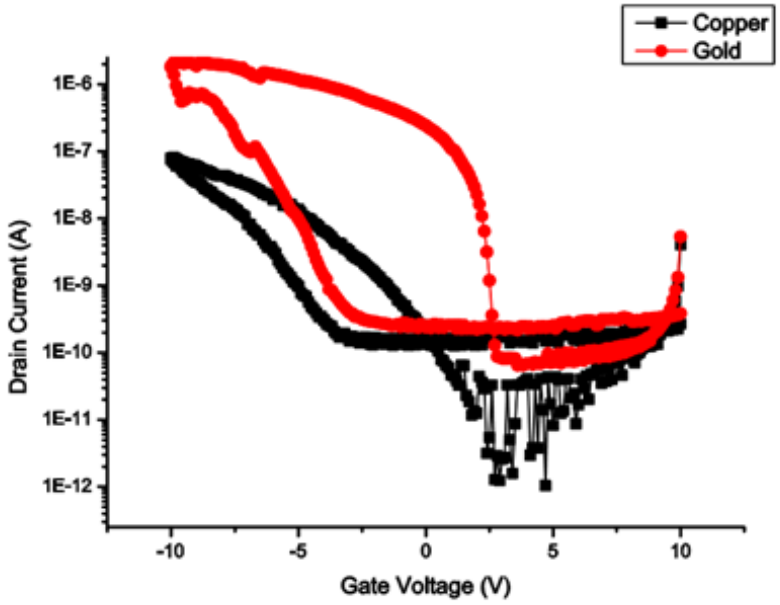

Figure 3.8-2 Comparison of TFTs fabricated with gold and copper. The red line shows the gold device displaying large hysteresis but higher on currents. The black line shows the copper trace with poor mobility and lower current performance

Similarly, Figure 3.8-3 shows the *IV* characteristic of 3 different diode samples each fabricated using the same fabrication process, apart from the contact metal, and with an area of 1 mm^2. The three different metals were a gold contact, a copper contact and a sample of both gold and copper connected together on the same substrate.

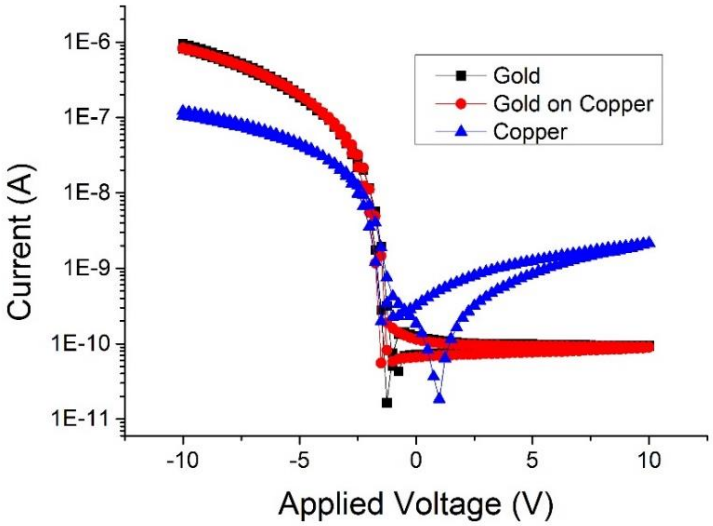

Figure 3.8-3 Output characteristics of 3 probed Schottky contact diodes. One with gold, one with gold and copper and one with only copper.

The comparisons of the three devices are shown in Table 3.8-2.

Table 3.8-2 Extracted ideality factor, T_0, and key current values from the three diodes in Figure 3.8-3

Contact Metal	Ideality	T_0 (K)	On Current (A)	Off Current (A)	On/Off Ratio
Gold	5.26	1560	9.52274E-7	9.389E-11	1.01E+04
Gold on Copper	4.60	1380	8.21528E-7	9.009E-11	9.12E+03
Copper	11.34	3372	1.22086E-7	2.16535E-9	5.64E+01

It is apparent in both the diode and TFT results that copper produced inferior devices in terms of both the on current performance and had significantly lower gradients implying that the mobility of the device was not as good. This could be down the aforementioned lower work function. If the work function was closer to the Schottky range then there would be a potential barrier to overcome and higher resistance. Another possibility that was observed practically was a reaction that took place between the copper and the stripper used in the development stage. This, however, would not account for the lower diode performance. As the concurrent methods to improve the gold adhesion had been successful, it was decided that copper fabrication would be abandoned.

3.9 Hysteresis and Contact Resistance

By going through the process of fabricating devices as well as performing the theory or analysing pre-made samples, certain observations can take place regarding how to improve the fabrication technique. One of the unexpected results of the scaling experiments detailed in Section 4.4.4 was the

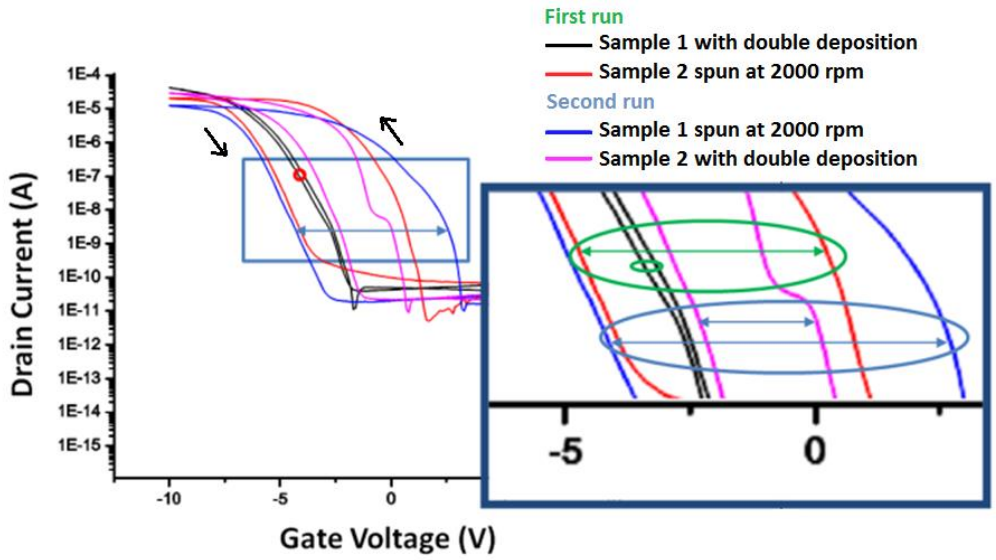

Figure 3.9-1 Changes in hysteresis based on reapplication of semiconductor. Devices shown were initially a sample spun at 2000rpm and the twice applied semiconductor re-application.

reduction of hysteresis that occurred when the semiconductor was removed and then reapplied to the same sample.

In the first case the aim was to compare a relatively thinly spun sample (2000 rpm so producing a thickness measured between 10 and 20 nm on corresponding AFM measurement). The polymer was then removed and a higher concentration solution was applied twice (polymer was heated to evaporate solvent and then applied at a 500 rpm spin speed.) This was then repeated forming a double layer. It can be seen in Figure 3.9-1 that 2 different devices measured on the 2000 rpm sample had hysteresis of ~7 V and ~5 V (as shown by the blue and red traces). With the reapplied semiconductor the thicker samples not only improved on current performance but the hysteresis was reduced to ~2 V and 0.6 V respectively.

Although this could have been down to the double semiconductor, the same was observed in the other two samples to which polymer was re-applied. These samples experienced the same reduction.

This can be seen in Figure 3.9-2 where the red arrows show the reduction in S1 (from ~11 V to ~3 V) and the blue arrows show the reduction in S2 (~10 V to ~1.5 V). As the hysteresis is anti-clockwise it is probably due to trapped hole charges either in the semiconductor or at the interface between the semiconductor and the oxide[19]–[22].

A possible explanation for the reduction of trapping with a second application is that a second application of polymer includes a second application of contact solution. Although it is expected that the contact solution is removed naturally in the process, both the transparent layer residue observed by the AFM (as detailed in Section 4.4.1) and the improved hysteresis could indicate that not all of the original contact solution is removed in the chloroform removal of polymer.

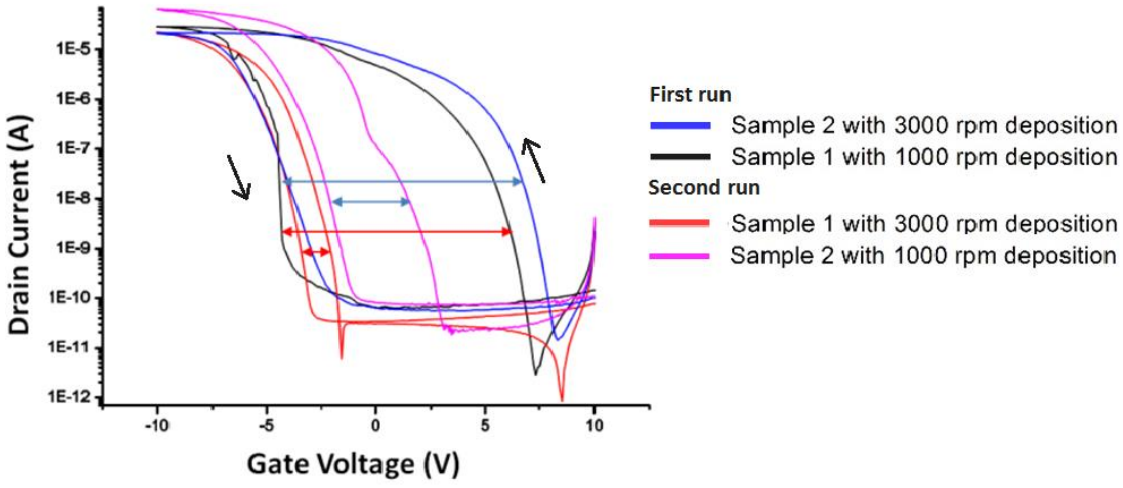

Figure 3.9-2 Changes in hysteresis based on reapplication of semiconductor to Sample 1 and Sample 2 for devices studied in Section 4.4.4..

Another indicator that the improvement in hysteresis may be as a result of improved contact is study of the region around V_{DS} = 0 V.

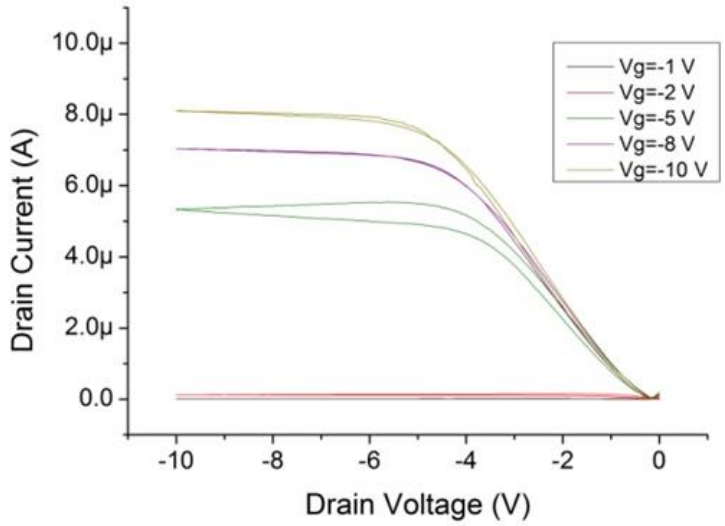

Figure 3.9-4 Output characteristics of device before semiconductor had been re-applied

Comparison of the two output characteristics (Figure 3.9-4 and Figure 3.9-5) show that the contact resistance and leakage changes with the re-application (shown by the slopes of the I_DV_D characteristics below -4 V). Figure 3.9-4 shows signs of gate leakage as shown by the offset from the origin. This extra current leakage prevents the device from switching on as abruptly as expected and this combined with the contact resistance does not reflect the V_G' proportionality expected in the linear region. This is behaviour is more like a diode contact resistance.

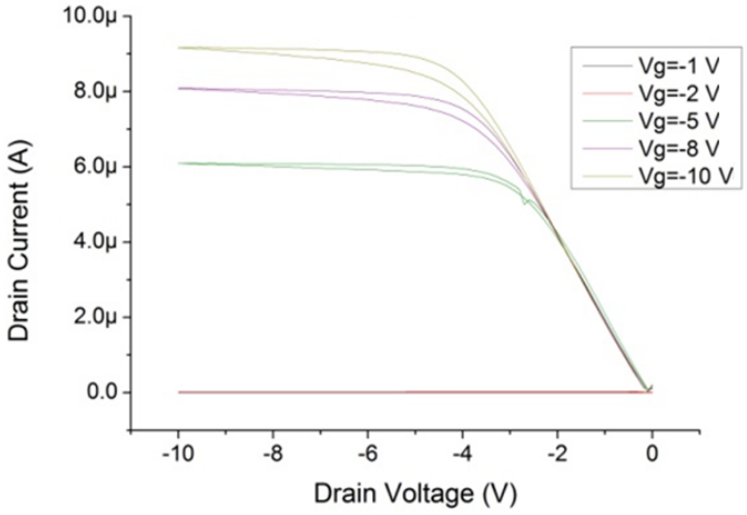

Figure 3.9-5 – Output characteristics of device after a second application of semiconductor. There is a clear reduction in contact resistance within the linear region in comparison with the pre-application results in Figure 3.9-4

With the second application of the polymer, there is a reduction in the effect of the Schottky barrier that causes the offset along the V_{GS} axis. Reducing this offset also reduces the effect on the linear region and while Figure 3.9-5 still exhibits signs of a strong contact resistance, the effect is now more like a resistive series resistance.

3.10 SUMMARY AND CONCLUSIONS

The main focus of Chapter 3 was the practical work of the project in the context of the fabrication methods that were used to produce the devices for characterisation and model parameter extraction. These devices were then used to test the current models derived in Chapter 2 and to adapt the simulation models for the circuits designed in Chapter 5.

It first introduced the cross-section diagrams for the diode, capacitor and OTFT that were fabricated for the project and then considered the different possible device structures that exist for OTFTs and the advantages and disadvantages for each. That stages of diode fabrication were then broken down and explained and the *IV* sweep characteristics were compared for both the disordered material, PTAA, and the new polycrystalline material, Lisicon™ S1200, that was provided by Merck Chemicals Ltd. for use within the project. The T_O values were extracted for these materials and compared to show a higher T_O for the disordered material. While this was in line with the higher levels of disorder for PTAA, the polycrystalline Lisicon™ S1200 still showed a higher ideality factor than expected for polycrystalline materials, implying that there is still a strong level of disorder controlling carrier transport. This is in line with the claim that the disordered grain boundaries of the polycrystalline material have high control over the carrier mobility that was stated in Chapter 2.

Two processing methods for OTFTs were then described, differing in the method of source and drain definition, metals used for contacts and material for dielectric. Samples made at the University of Liverpool used an aluminium gate with an Al_2O_3 dielectric with a photolithography technique for gold source and drain contact definition, while devices fabricated at Merck Chemicals Ltd. used silver for both the aluminium and source drain contacts, all of which were patterned using a shadow evaporation mask. These devices used a patternable, organic dielectric Lisicon™ D206 as a low-*k* dielectric. The use of organic dielectric creates a much thicker layer, however the prospect of patterning the gate could reduce internal capacitances – something which will be discussed further in Chapter 5.

Using the theory from which that the models stated in Chapter 2 were devised, mobility parameters *K* and *m* were extracted from a set of $I_{DS}V_{GS}$ results from one of the characterised devices. This was done for the polycrystalline and disordered models with both producing a decent fit with the

experimental results. The similarity in the two forms provided more evidence for the control of the grain boundary disorder within polycrystalline materials. An effective mobility expression was also devised with the average effective mobility taken for the modelled device which can then be used in Chapter 5 for the purposes of simulation. Due to the varying mobility within organics, this is more of a property for comparison and crystalline based modelling rather than a relevant device property for theory.

The performance of devices fabricated with copper source and drain contacts, as opposed to gold, were discussed and compared. It was found that the copper produced inferior devices, this could either be due to the lower work function causing it to act more like a Schottky metal than an Ohmic one, or due to degradation from the chemicals used in processing. The hysteresis and high contact resistance was also considered, noting an unexpected correlation between the reduction of hysteresis and change in contact resistance on devices that had semiconductor removed and reapplied.

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Chapter 4 SCALING

4.1 Background and Relevance

History shows that the success of the silicon industry has been based heavily on the ability to scale the minimum feature size following Moore's law[1]. Despite the many barriers that emerged over the evolution of silicon[2], progress continued in the years following Moore's Law and even accelerated[3] leading to its multi-decade dominance in the industry. While this rate has since slowed and the timeframe for halving minimum feature size has lengthened to 2.5 years[4], the lessons learnt from reducing device size in silicon is a good base from which to analyse a similar process in other technologies. Although the potential of organic electronics applications is of more interest than its viability as a silicon replacement[5], the path of development that silicon has taken is a good indicator for the roadmap for organics.

As OTFTs possess different transport mechanisms as well as a different structure to traditional Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), it follows that a new set of design rules must be defined. For example, one of the key parameters in scaling of silicon technology was the dopant in the depletion regions. Channel length was reduced to improve speed and performance but as a result the depletion regions could eventually overlap and ultimately gate control of the device was lost. This was compensated with doping to enable smaller depletion regions which had a detrimental effect on threshold voltage and so forth. With OTFTs operating in accumulation mode, depletion region doping is not a scaling parameter for organics, but other factors such as grain size, dielectric pinholing and contact resistance have been found to impact performance as device size reduces[6].

Considering the differences, there is the question of whether scaling will have the same benefits that have served the silicon industry. There are of course the universal scaling benefits not defined by structure such as yield - the smaller the devices are, the less chance there is of hitting defects, plus more devices can be produced per area of substrate. Another attractive benefit for scaling organics is that, like silicon, the switching speed follows the relationship $t \propto \frac{L^2}{\mu}$, where the switching time of an inverter is proportional to the square of the channel length and inversely proportional to the mobility[7]. With organic materials generally operating at lower mobilities, scaling could potentially act as a compensating factor.

A potential hindrance of scaling is the limiting Debye length[8] – the depth of the channel in which the majority of the carriers are contained. Scaling down to thicknesses thinner than the Debye length would therefore have an effect on the number of conducting carriers in the channel This is covered in Section 4.4.4.

4.2 General Benefits of Scaling

The success of silicon, driven by the ability to downsize circuits, was achieved by various enhancements, not just of the technology (some of which came as a result of scaling and will be explored later in this chapter) but also in some practical and economic terms[9].

A major hindrance for integrated circuit technology is that of defects. Devices have been fabricated to have dimensions as small as a single atom length[10] and even for dimensions on a micrometre scale any foreign bodies within the circuit can prove problematic. Entire portions of the circuit could become unusable due to contamination of even a particle of dust on a key device. Along with improvements in cleanliness during fabrication, scaling can counteract this issue by improving the proportion of working devices. An example of this can be explained with the samples produced for this thesis. As detailed in Section 3.5, each sample of TFT selection was an approximately 2.5 cm x 5 cm rectangle of glass slide. The oxidised part of the sample was approximately 2.5 cm x 2.5 cm and contained approximately 20 patches of devices with a selection of channel sizes. As detailed in Section 3.8, there was a period of fabrication where difficulties in the gold deposition combined with the photolithography caused parts of the gold to be etched away. The majority of the gold that failed to adhere to the sample was focussed in a circular shape based on the shape of the chuck used in photoresist deposition. This resulted in a significant portion of the devices being removed in processing, however devices in other parts outside of this main ring were left intact and in some cases measurements were obtained (although they were generally discarded due to the sample being compromised). The comparison in Figure 4.2-1 considers the hypothetical scenario in which those devices were scaled down to a quarter of the total device area.

In the first case, the larger dimension of device results in 80% of the devices being affected by the large defect whereas in the second example where each dimension is half the size in length and width, only 45% of devices are affected. This is a simplistic example, however on an industrial basis the principle is the same whereby the smaller the devices, the smaller the proportional impact of any defect.

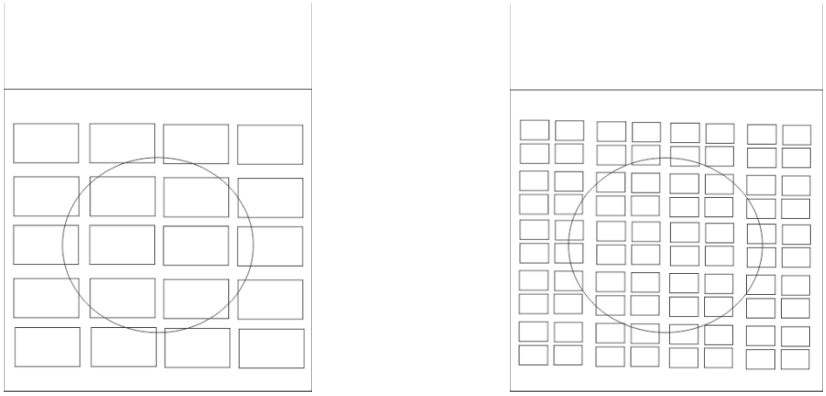

Figure 4.2-1 – Visual comparison of device size in proportion to fabrication deformities. The smaller the size of the device, the larger the number of working devices is.

There is also the cost benefit of scaling. As the stages of processing are interlinked the number of devices that can fit onto a single substrate allow for more complex circuits to be produced. The smaller these circuits are, the smaller the product which can have consumer benefit, but this also means that more complex circuits can be produced for the same cost as simpler, larger ones. The processing technique for general circuits would be the same regardless of complexity – unless of course superior technologies were needed, but the same principle would then follow for that generation of process.

4.3 Comparison of Scaling Rules

It follows that in order for organics to achieve comparable success in production that the lessons learned from silicon must be assessed as a benchmark and indeed used to estimate a roadmap timetable for organic success. This approach, however, is not flawless as silicon devices are of a different structure than those of organics, as discussed in the previous chapters. These differences do however give a platform for comparison and therefore by dissecting the issues faced by the Silicon industry the structures of devices can be compared and assessed in order to isolate the factors which may have a bearing on the scaling of organic devices.

As organics is a relatively new field, the information regarding scaling is still relatively unconfirmed. So far the focus has been on enhancing device performance and materials as well as improving techniques but various institutions have begun to consider the scaling effects regarding the channel length [11] [12] [13]and efforts have been made to reduce dimensions by using alternative techniques[14] including nanoimprint lithography[15], micro-contact printing[16] and inkjet printing[17] [18].

The physical structure of silicon transistors hinders the practicalities of scaling while also providing the basis for its need. To put the need for scaling into context, it can be proven from transient analysis that the performance of a transistor improves with smaller channel length[19]. The switching speed of an inverter is proportional to the load capacitance C_L and inversely proportional to device constant, β. β is specific to each individual MOSFET and consists of the combination of the mobility μ, the capacitance per unit area, C_0, and ratio of the channel width, W, to the channel length, L. This is shown in Eqn. 4.3-1.

$$\beta = \mu C_0 \frac{W}{L}. \qquad \textit{Eqn. 4.3-1}$$

Considering the case for a CMOS inverter where another transistor is the load capacitance C_L, it can be assumed that this C_L is equivalent to the capacitance at the gate i.e. the device area W x L of the channel and the number of gates at the load.

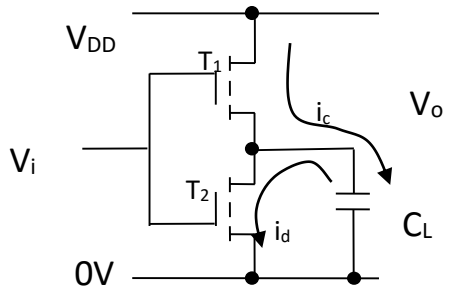

Figure 4.3-1 - Circuit depicting the transient nature of CMOS inverter.

The drain current, I_D, can be equated to the rate of discharge, $-Q$, over time, t, this value can be expressed in terms of the change in output voltage, V_o, and the capacitance, C_L to obtain I_d as a function of time, $I_D(t)$:

$$i_D = -\frac{dQ}{dt} = -C_L \frac{dV_O}{dt} = I_D(t). \qquad \textit{Eqn. 4.3-2}$$

Eqn. 4.3-2 can then be integrated between appropriate limits to obtain the switching time. This analysis takes place in the saturation region of operation so the current I_D is that of Eqn. 4.3-3, the saturation current for a MOSFET with a crystalline semiconductor, I_{DSatC}.

$$I_D = I_{DSatC} = \frac{\beta}{2}[V_{DD} - V_T]^2$$

Eqn. 4.3-3

$I_D(t)$ can be integrated with respect to time, equating the I_D from Eqn. 4.3-3 with.

$$\int_0^{t_1} dt = \int_0^{t_1} I_{DSatC}\, dt = \int_0^{t_1} \frac{\beta}{2}[V_{DD} - V_T]^2\, dt = \int_{0.9V_{DD}}^{V_{DD}-V_T} -C_L \frac{dV_O}{dt}\, dt$$

Eqn. 4.3-4

$$\int_0^{t_1} dt = \int_{0.9V_{DD}}^{V_{DD}-V_T} -\frac{2C_L}{\beta[V_{DD} - V_T]^2}\, dV_O$$

Eqn. 4.3-5

The limits are defined as the time from reference 0 to a time t_1 where transistor T_2 is no longer in saturation. The corresponding voltage limits are the time it takes for V_o to go from 90% (using the 90/10 fall time estimation[20]) to the point at which $V_{DS} < V_{GS}-V_T$. As V_i is high, $V_{GS} = V_i = V_{DD}$.

Solving integration of Eqn. 4.3-5 produces the expression for the fall time in the saturated region:

$$t_1 = \frac{2C_L(V_T - 0.1V_{DD})}{\beta(V_{DD} - V_T)^2}.$$

Eqn. 4.3-6

For the unsaturated region a similar method takes place but with the unsaturated MOSFET equation I_{DLinC} in Eqn. 4.3-7.

$$I_{DLinC} = \beta\left[(V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

Eqn. 4.3-7

As with Eqn. 4.3-4, this can be substituted for I_D. The limits are from t_1 to a time t_1+t_2, where t_2 is the time for V_o to drop to 10% of the total voltage V_{DD}.

$$\int_{t_1}^{t_1+t_2} dt = \int_{t_1}^{t_1+t_2} I_{DLinC}\ dt$$

$$\int_{t_1}^{t_1+t_2} dt = \int_{t_1}^{t_1+t_2} \beta\left[(V_{GS}-V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right]dt = \int_{V_{DD}-V_T}^{0.1V_{DD}} -C_L\frac{dV_O}{dt}\,\mathrm{dt} \qquad \textbf{Eqn. 4.3-8}$$

As $V_{DS} = V_O$, this can be re-written in terms of V_O and as with the previous limit range, $V_{GS} = V_i = V_{DD}$.

$$\int_{t_1}^{t_1+t_2} dt = \int_{V_{DD}-V_T}^{0.1V_{DD}} -\frac{C_L}{\beta\left[V_o\left((V_{DD}-V_T)-\frac{V_O}{2}\right)\right]}dV_O. \qquad \textbf{Eqn. 4.3-9}$$

This equation can be solved using partial fractions to produce Eqn. 4.3-10.

$$t_2 = \frac{2C_L}{\beta[(V_{DD}-V_T)]}ln\left[\frac{2(V_{DD}-V_T)-0.1V_{DD}}{0.1V_{DD}}\right]. \qquad \textbf{Eqn. 4.3-10}$$

This was obtained due to the natural log of 1 being equal to 0 and thus eradicating the term for $V_o = (V_{DD} - V_T)$. Combining the two expressions for Eqn. 4.3-6 and Eqn. 4.3-10, the final expression for fall time is obtained as

$$t_f = t_1 + t_2 = \frac{2C_L}{\beta(V_{DD}-V_T)}\left\{\frac{(V_T-0.1V_{DD})}{(V_{DD}-V_T)} + ln\left[\frac{2(V_{DD}-V_T)-0.1V_{DD}}{0.1V_{DD}}\right]\right\}. \qquad \textbf{Eqn. 4.3-11}$$

This relationship for the switching of the inverter can be simplified in the form shown in Eqn. 4.3-12.

$$t_f \propto \frac{C_L}{\beta} \sim \frac{C_0WL}{\mu C_0\frac{W}{L}} \sim \frac{L^2}{\mu}. \qquad \textbf{Eqn. 4.3-12}$$

This shows that the time it takes for an inverter to switch is proportional to the channel length squared i.e. a smaller channel length means faster switching. What this also shows is that faster switching is inversely proportional to mobility. As it is known that organics suffers from lower mobilities than its

silicon counterparts, should this relationship follow for organics, reducing channel length to improve speed would also be a method of compensating for the poorer mobility.

For the case of an organic inverter, a saturated load configuration can be assumed (although different inverter configurations will be explored in Section 5.3).

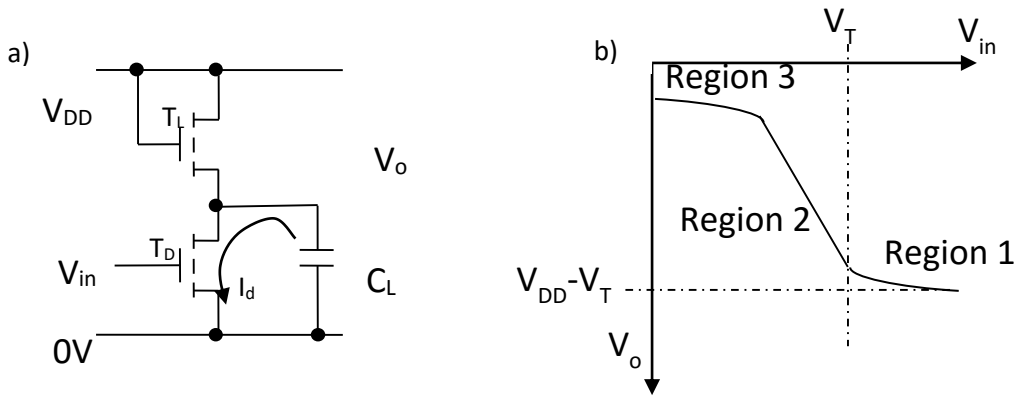

Figure 4.3-2– a) Circuit and b) inverter transfer characteristics for saturated load inverter showing three regions of significance

The transfer characteristics for this inverter can be considered as being split into three regions of operation, as shown in Figure 4.3-2 (b). For Region 1, the driver is in an off state due to V_{GS} being lower than V_T and the output fixed at V_{DD}-V_T. As the gate is tied to the drain, the highest output voltage is V_{DD}-V_T. This is a disadvantage which will be discussed further in Section 5.3.1. In Region 2, V_{GS} is higher than V_T putting both devices in saturation as $V_o > V_i$ and therefore V_D of the driver is greater than V_G. In Region 3 the driver is now unsaturated with the load remaining saturated. The analysis that was done for the CMOS inverter can now be applied to the organic saturated load inverter, using the models stated in Chapter 2 for disordered organic semiconductor devices.

An expression for the fall time dictated by the pull-down, drive transistor is now derived. The driver is initially in saturation. The equations in Eqn. 4.3-13 and Eqn. 4.3-14 (as stated in Section 2.9 and repeated here for clarity) can be used to represent the current in the linear and saturation regions respectively.

$$I_{lin} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(\frac{(V_{GS}-V_T)^{(2m+2)}}{2(m+1)(2m+1)} - \frac{(V_{GS}-V_T-V_{DS})^{(2m+2)}}{2(m+1)(2m+1)}\right), \qquad \textit{Eqn. 4.3-13}$$

$$I_{sat} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(\frac{(V_{GS}-V_T)^{(2m+2)}}{2(m+1)(2m+1)}\right). \qquad \textit{Eqn. 4.3-14}$$

Define

$$Y = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)}, \qquad \textit{Eqn. 4.3-15}$$

where *Y* represents all of the constant multipliers in Eqn. 4.3-13 and Eqn. 4.3-14. The limits can be obtained by considering when $V_{DS} < V_{GS} - V_T$, which in this circuit configuration will be when $V_o = V_{DD} - V_T$. As with the CMOS case, $V_{GS} = V_i = V_{DD}$

$$\int_0^{t_1} dt = \int_0^{t_1} I_{sat}\, dt = \int_0^{t_1} Y(V_{DD}-V_T)^{(2m+2)}\, dt = \int_{0.9V_{DD}}^{V_{DD}-V_T} -C_L dV_0 \qquad \textit{Eqn. 4.3-16}$$

$$\int_0^{t_1} dt = \int_{0.9V_{DD}}^{V_{DD}-V_T} -\frac{C_L}{Y(V_{DD}-V_T)^{(2m+2)}} dV_0 \qquad \textit{Eqn. 4.3-17}$$

$$\int_0^{t_1} dt = -\frac{C_L}{Y(V_{DD}-V_T)^{(2m+2)}}[V_0]_{0.9V_{DD}}^{V_{DD}-V_T}. \qquad \textit{Eqn. 4.3-18}$$

Integrating Eqn. 4.3-18 produces:

$$t_1 = -\frac{C_L(0.1V_{DD}-V_T)}{Y(V_{DD}-V_T)^{(2m+2)}}. \qquad \textit{Eqn. 4.3-19}$$

Once the driver is unsaturated, the unsaturated equation for the disordered model I_{lin} is used as I_D and the limits are from t_1 to t_1 plus an additional time t_2 that is the time it takes for the inverter to switch from the pinch off point $V_o = V_{DD} - V_T$ to 10% of the total V_{DD}.

$$\int_{t_1}^{t_1+t_2} dt = \int_{t_1}^{t_1+t_2} (V_{GS}-V_T)^{(2m+2)} - (V_{GS}-V_T-V_{DS})^{(2m+2)}\, dt = \int_{V_{DD}-V_T}^{0.1V_{DD}} -C_L \frac{dV_0}{dt} d$$ ***Eqn. 4.3-20***

$$\int_{t_1}^{t_1+t_2} dt = \int_{V_{DD}-V_T}^{0.1V_{DD}} -\frac{C_L}{Y(V_{GS}-V_T)^{(2m+2)} - (V_{GS}-V_T-V_{DS})^{(2m+2)})} dV_0.$$ ***Eqn. 4.3-21***

This can be rearranged and adapted to include $V_{DS} = V_o$ and $V_{GS} = V_{DD}$:

$$\int_{t_1}^{t_1+t_2} dt = -\frac{C_L}{Y}\int_{V_{DD}-V_T}^{0.1V_{DD}} \frac{1}{[(V_{DD}-V_T)^{(2m+2)} - (V_G-V_T-V_0)^{(2m+2)}]} dV_0.$$ ***Eqn. 4.3-22***

A substitution variable u is defined as

$$u = \left[(V_{DD}-V_T)^{(2m+2)} - (V_{DD}-V_T-V_0)^{(2m+2)}\right],$$ ***Eqn. 4.3-23***

with

$$\frac{du}{dV_O} = \left[0-(2m+2)(V_{DD}-V_T-V_0)^{(2m+1)}\right].$$ ***Eqn. 4.3-24***

Substituting this form into the integral in Eqn. 4.3-22 gives

$$\int_{t_1}^{t_1+t_2} dt = \frac{C_L}{Y}\int_{(V_{DD}-V_T)^{(2m+2)}}^{(V_{DD}-V_T)^{(2m+2)}-(0.9V_{DD}-V_T)^{(2m+2)}} \frac{1}{u}\frac{(V_{DD}-V_T-V_0)^{-(2m+1)}}{(2m+2)} du.$$ ***Eqn. 4.3-25***

Where the limits have been calculated using Eqn. 4.3-23. Evaluating the equation with the appropriate values of V_o and u, t_2 can be calculated as Eqn. 4.3-26.

$$t_2 = \frac{C_L}{Y}\left(\frac{ln\left[(V_{DD}-V_T)^{(2m+2)} - (0.9V_{DD}-V_T)^{(2m+2)}\right]}{(2m+1)(0.9V_{DD}-V_T)^{(2m+1)}}\right)$$ ***Eqn. 4.3-26***

As with Eqn. 4.3-11, combining the two expressions for Eqn. 4.3-13 and Eqn. 4.3-26, the final expression for fall time is obtained:

$$t_f = t_1 + t_2$$

$$t_f = .\frac{C_L}{Y}\left[\left(\frac{ln\left[(V_{DD}-V_T)^{(2m+2)} - (0.9V_{DD}-V_T)^{(2m+2)}\right]}{(2m+1)(0.9V_{DD}-V_T)^{(2m+1)}}\right) - \frac{(0.1V_{DD}-V_T)}{(V_{DD}-V_T)^{(2m+2)}}\right]$$

Eqn. 4.3-27

This relationship for the fall time of the inverter can be simplified into the form shown in Eqn. 4.3-28 and, if it is assumed that the constants in the expression will not have as much impact on the overall value due to the power factors, this can be approximated to Eqn. 4.3-29.

$$t_f \propto \frac{C_L}{Y} \sim \frac{C_0 WL}{\frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)}}$$

Eqn. 4.3-28

$$t_f \propto \frac{L^2\{2kT_C\varepsilon_0\varepsilon_S\}^m}{C_0{}^{2m}}$$

Eqn. 4.3-29

This indicates that the fall time for an organics inverter still has a strong dependence on the square of the length of the channel but a notable difference between Eqn. 4.3-29 and the crystalline counterpart in Eqn. 4.3-12 is the presence of C_o. This adds to the evidence that a higher C_o will help with scaling and is explored in the context of oxide thickness in Section 4.4.2. While the use of UML has removed the dependency on μ that would otherwise appear in its crystalline counterpart, it is clear that the UML parameter m does have a bearing on the speed which shows how the level of disorder could be a hindrance.

Reducing channel length is a limited solution for improving the performance without the scaling of other dimensions to support the change to the device behaviour. Returning to a crystalline silicon device structure, source and drain contacts are each surrounded by a doped depletion region. If the channel length is reduced without adjusting the size of these regions this can lead to punchthrough whereby a leakage current occurs between the source and drain and the channel is no longer controlled by the gate[21]. This is one of the main causes of scaling limitations[22].

There are methods to reduce punchthrough by using spatially restricted dopant implants[23], however a simpler approach is to alter the dopant density, N_{sub}[24]. Although this reduces the size of the depletion regions it comes at the cost of threshold voltage due to the relationship $V_t \propto t_{ox}\sqrt{N_{sub}}$.

It is undesirable to have a high threshold voltage as this results in higher power consumption. This is especially true in the case of saturated active load inverters where the device would be permanently on due to the gate being connected to the drain. As a result, further compensation techniques are needed - in this case, adjusting the oxide thickness. As the threshold voltage is controlled by the capacitance of the oxide layer, thinning of the oxide layer will reduce the threshold voltage. As this factor is also then being scaled down this has dual benefit. Unfortunately, thinning the oxide increases off currents producing unnecessary leakage[25]. A small leakage is expected but if the purpose of scaling is to increase packing density, this could add up to a large power loss. In response, the oxide capacitance, C_{ox}, relationship can be used, increasing the dielectric constant as opposed to reducing the oxide thickness. This will still result in a higher capacitance as needed to reduce the threshold voltage. This can be achieved by using high-*k* dielectrics.

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}}. \qquad \textit{Eqn. 4.3-30}$$

Once again it is necessary to consider these drawbacks and solutions in the context of the organic structure. As has already been discussed there are benefits of scaling, shown by the dependence proved in Eqn. 4.3-29 as there is an implication that at least the benefits of channel length reduction will stand as well as the mobility dependency. Improving the switching speed is imperative for efficient operation as well as all of the yield and cost efficiency benefits.

Regarding the difficulty of punchthrough, the difference in the structure of the OTFTs means that the aforementioned issues caused by doping region size is not applicable. On the basis of this, doping can be ruled out as a scaling factor. The limitation on channel length is more likely restricted by the dimension of the source and drain edges. This can be improved with technology and OTFTs on scales of 100 nm [26] and lower [14] have been achieved, although there is evidence that lengths of less than 10 nm may have implications for transport[27].

Regarding the threshold voltage, this is not controlled by dopant (although natural dopants exist in the materials), but by the work functions of materials[28] and by insulator trapped charges. If threshold voltages are too low, however, noise immunity is threatened and the transistor could switch at inputs caused by noise spikes. Independent scaling characterisation throughout this project, as

detailed in the results in this chapter, has proven that threshold voltage is generally inconsistent, as seen in Section 4.4.2. It is possible that this is related to air exposure (measurements in nitrogen rather than air have proven more stable), but further work would need to be done that is beyond the scope of this project.

Although the structure eradicates the need to compensate for a higher threshold voltage due to the lack of dopant, scaling would require the reduction of all dimensions including the oxide thickness. As previously stated, thin oxides result in higher off currents, which increase the use of power when considering many devices in a circuit. These off currents, however, are also controlled by the thickness of the semiconductor[8] as they are dependent on the resistivity of the layer[29][30]. Reducing the semiconductor thickness reduces the off currents, but a physical restriction to this lies with the electrostatic screening distance; the Debye length. This is caused by the high electric field adjacent to the gate dielectric, causing the carrier density to be at a maximum and can be considered to be the thickness of the accumulation layer.

Drawing on the theory of Raja *et al.*[31], an expression for the field, *F*, can be used in order to produce the estimated thickness of the accumulation region and serves as an estimate of the depth into the channel that the majority of the conducting charges are. This is defined as the Debye length, L_D, and derived as follows:

$$F = \left(\frac{2qn_0}{\varepsilon\varepsilon_0}\right)^{\frac{1}{2}}\left[\frac{kT}{q}\right]^{\frac{1}{2}}\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)^{\frac{1}{2}} \qquad \textit{Eqn. 4.3-31}$$

$$F = \left(\frac{2qn_0}{\varepsilon\varepsilon_0}\right)^{\frac{1}{2}}\left[\frac{kT}{q}\right]\left[\frac{kT}{q}\right]^{-\frac{1}{2}}\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)^{\frac{1}{2}} \qquad \textit{Eqn. 4.3-32}$$

$$F = \left(\frac{\varepsilon\varepsilon_0}{2qn_0}\right)^{-\frac{1}{2}}\left[\frac{kT}{q}\right]\left[\frac{kT}{q}\right]^{-\frac{1}{2}}\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)^{\frac{1}{2}} \qquad \textit{Eqn. 4.3-33}$$

$$F = \frac{\left[\frac{kT}{q}\right]}{\left(\frac{\varepsilon\varepsilon_0 kT}{2q^2n_0}\right)^{\frac{1}{2}}}\left(\exp\left(\frac{q\phi}{kT}\right)-1\right)^{\frac{1}{2}}, \qquad \textit{Eqn. 4.3-34}$$

where the Debye Length can be isolated as:

$$L_D = \left(\frac{\varepsilon\varepsilon_0 kT}{2q^2 n_0}\right)^{\frac{1}{2}}. \qquad \textit{Eqn. 4.3-35}$$

The Debye Length is relevant for the analysis on scaling as it proves to be a physical restriction to the reduction of channel depth.

Consider Eqn. 4.3-36; the drift and diffusion currents must equate due to there being no loss of charge. The charge is determined by the gradient of carriers as shown in Eqn. 4.3-31 and clearly this is much steeper at the interface.

$$qD\frac{dn}{dz} = q\mu Fn \qquad \textit{Eqn. 4.3-36}$$

L_D is at a minimum when carrier density is at its lowest and there is a low surface potential. The surface concentration can be represented by Eqn. 4.3-37 where $\emptyset_s$ represents the surface potential and n_0 is the equilibrium carrier density – comparable to the density of the active dopant.

$$n_S = n_0 exp\left(\frac{q\emptyset_s}{kT}\right) \qquad \textit{Eqn. 4.3-37}$$

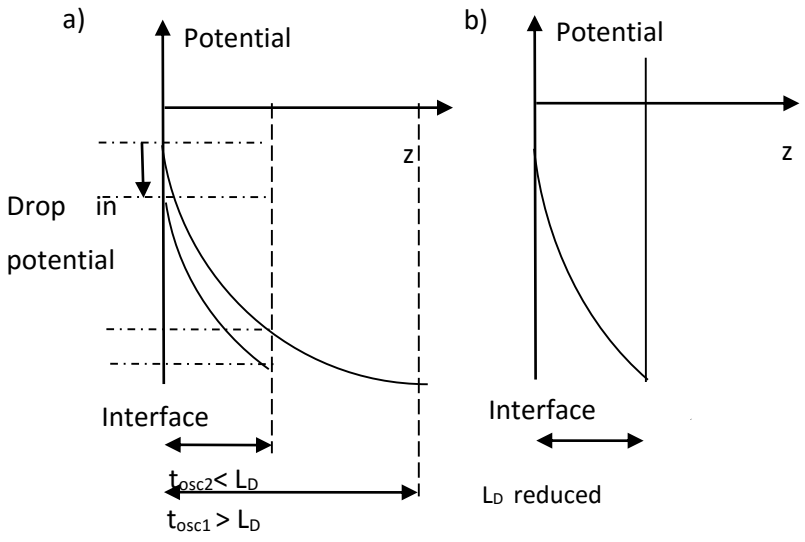

Figure 4.3-3 – a) Diagram at the accumulation interface considering two different oxide thicknesses, t_{osc1} and t_{osc2}. As t_{osc2} is smaller than the Debye length L_D the result is a drop in overall potential and therefore current. b) shows the recovery of potential based on a reduction of the Debye length so that $t_{OSC2} = L_D$ to compensate for the reduction in semiconductor thickness.

If the semiconductor film thickness t_{osc} is reduced this impacts the distribution of the carriers within it as the charge must remain the same. If the slope of the curve is the charge which must remain the same, there is a resultant loss of potential as indicated in Figure 4.3-3, illustrated by the reduction of t_{osc} to a thickness smaller than L_D. Should L_D also be reduced this can be avoided with the field potential recovered. This would need to be achieved by altering the dopant n_O or the permittivity of the material.

Assuming the case where L_D is not reduced, the re-distribution of charge and subsequent effect on the field within the semiconductor has implications for the simple model analysis based on the structure of the TFT effectively being 2 series capacitors C_{ox} and $C_{surface}$. The total capacitance is

$$\frac{1}{C_T} = \frac{1}{C_{ox}} + \frac{1}{C_{surface}}. \qquad \textit{Eqn. 4.3-38}$$

The effective mobility is derived on the assumption that the semiconductor capacitance is much larger than the oxide capacitance and is therefore negligible when looking at the total capacitance per unit area. This is only valid if the semiconductor layer is much thinner than the oxide thickness.

In order to counteract this, the oxide thickness needs to be reduced or the dielectric constant needs to be increased. This can also be done by introducing a double dielectric as long as a balance is maintained. The benefits of this can be proven by applying Gauss's Law to the dielectric displacement for the semiconductor, D_S, and the dielectric, D_d. These values are calculated from the relative permittivity of the semiconductor, ε_s, and dielectric, ε_D, respectively, combined with the permittivity of free space ε_0. V_G-V_T represents the voltage applied at the gate and kT_o/q represents the potential across the accumulation layer:

$$D_D = D_S \qquad \textit{Eqn. 4.3-39}$$

$$\varepsilon_D \varepsilon_0 \left(\frac{V_G - V_T}{t_{ox}}\right) = \varepsilon_S \varepsilon_0 F_s. \qquad \textit{Eqn. 4.3-40}$$

Or, in terms of L_D:

$$\varepsilon_D \varepsilon_0 \left(\frac{V_G - V_T}{t_{ox}}\right) \approx \varepsilon_S \varepsilon_0 \frac{\left(\frac{kT_C}{q}\right)}{t_{osc}}. \qquad \textit{Eqn. 4.3-41}$$

Assumed that the thickness of the semiconductor is value t_{osc1} as shown in Figure 4.3-3, and that this is equivalent to L_D (as $t_{osc1} \geq L_D$), Eqn. 4.3-41 can be re-written as:

$$\varepsilon_D \varepsilon_0 \left(\frac{V_G - V_T}{t_{ox}}\right) \approx \varepsilon_S \varepsilon_0 \frac{\left(\frac{kT_C}{q}\right)}{L_D}, \qquad \textit{Eqn. 4.3-42}$$

in terms of L_D. For reduced thickness t_{osc2} the oxide would need to be reduced to a corresponding value t_{ox2} to compensate for the reduction in thickness of the semiconductor.

$$\varepsilon_D \varepsilon_0 \left(\frac{V_G - V_T}{t_{ox2}}\right) \approx \varepsilon_S \varepsilon_0 \frac{\left(\frac{kT_C}{q}\right)}{t_{osc2}} \qquad \textit{Eqn. 4.3-43}$$

These two equations can then be combined to find the ratio:

$$t_{ox2} \approx \frac{t_{osc2}}{L_D} t_{ox}. \qquad \textit{Eqn. 4.3-44}$$

This provides a means of determining the required thickness of gate dielectric for any thickness of semiconductor film less than the Debye Length. It should be noted, however, that reducing the oxide thickness returns full circle to the issue of off currents. This is evidence that although the nature of the scaling rules may be different, there are still trade-offs to be made with organic scaling.

4.4 Methodology and Results of Scaling in Fabrication

In order to see some of the experimental effects of scaling, various devices were fabricated using the stages detailed in Chapter 3 but with alterations to specific parameters. These included altering semiconductor thickness, oxide thickness, aspect ratio, concentration of semiconductor and a basic look at the possibilities of using double dielectrics.

These were implemented in various ways, though in general only one factor was changed. In order to control the semiconductor thickness, the spin speed was altered and the concentration of the semiconductor was changed. For thicker samples, some devices were drop cast and in one case there

was a second layer of semiconductor added. For the oxide thickness the voltage controlling the anodisation was altered. The lower the voltage, the thinner the oxide grown. In order to measure the effects of aspect ratio masks were used with various widths and lengths and some devices were made with an organic dielectric, again using different spin speeds in order to vary the thickness.

4.4.1 AFM Measurements for Layer Thickness

In order to get values for comparison, Atomic Force Microscopy (AFM) was used to obtain measurements and a clearer idea of the thicknesses. As shown in-Figure 4.4 1 a), the AFM works by scanning over the edge of a sample with a microfabricated, flexible cantilever that bends based on the force from the sample. The bending of the cantilever is recorded using a laser and photodiode setup which can detect nano-scale dimensions [31]. The AFM used in this project was a Brucker Innova AFM with a standard silicon nitride probe.

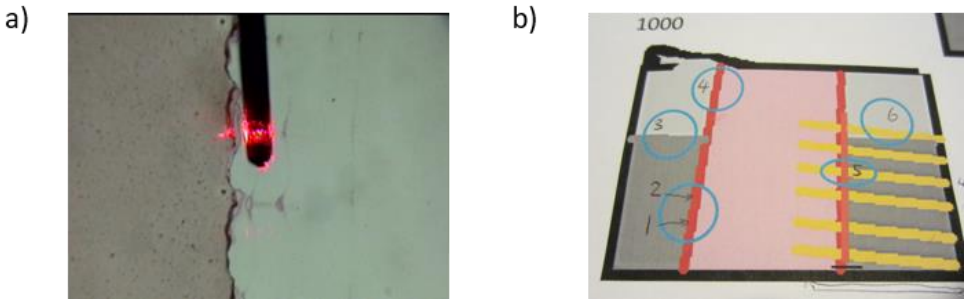

Figure 4.4-1 a) Photo of AFM cantilever measuring semiconductor thickness of sample. b) Graphical guide distinguishing different areas of sample for measuring. These correspond to the areas in table 4.4 1 and are marked in the device structure in Figure 4.4 2-b). This allowed for the 6 distinctive regions, itemised in Table 4.4-1 to be measured and obtain the relevant heights for all combinations of layers.

Specially designed sample for AFM readings were fabricated for a range of spin speeds between 1000 rpm and 3000 rpm. These were designed to have the same fabrication process as TFT characterisation, but with accessible edges to be measured – as shown by the graphical representation in Figure 4.4 1 b).

Table 4.4-1 Thickness label for areas 1-6 from

Area	Thickness	Surface 1	Surface 2
1+2	t_{OSCOX}	Semiconductor	Al_2O_3 Dielectric
3	t_{OXG}	Al_2O_3 Dielectric	Aluminium Gate
4	t_{OSCG}	Semiconductor	Aluminium Gate
5	t_{SDOX}	Gold Contact	Al_2O_3 Dielectric
6	t_{SDG}	Gold Contact	Aluminium Gate

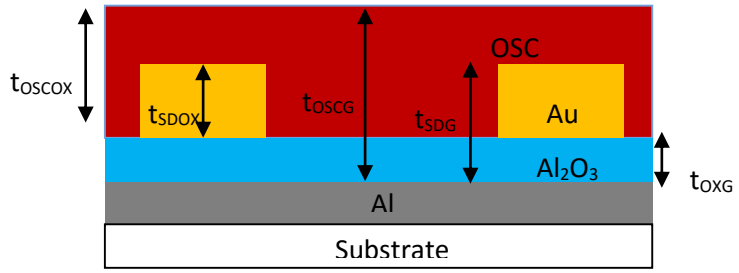

Figure 4.4-2 Thicknesses as shown on TFT structure diagram. Each of the area labels in Figure. 4.4.-1 b) are noted with their label showing the thickness they represent.

The AFM returned an image and a height chart which could then be compared to give a physical idea of the dimensions. Semiconductor thicknesses appeared to be in the nanometre range with the lowest spin speeds.

Figure 4.4-3 AFM measurement of t_{oscox} for samples with semiconductor spun at 1000 rpm. It can be seen that the thickness is not uniform across the sample. There is a protruding bump in the measurement caused by the method of semiconductor removal. The effect of this can be disregarded.

Each of the measurements produced a chart such as that shown Figure 4.4-3 that displays the thickness across the surface. The results for the thicknesses across all three samples are recorded in Table 4.4-2.

Table 4.4-2 Results of AFM measurements. These were measured over 6 areas of custom made samples to ensure thicknesses between all materials on the sample were obtained. Included in the table are just the ones relevant to the scaling detailed.

Spin Speed (rpm)	t_{OSCOX} (nm)		t_{OXG} (nm)	t_{OSCG} (nm)	t_{SDOX} (nm)
	Min	Max			
1000	30	90	10	30	No height
2000	10	20	10	25	No height
3000	~0	20	10	20	No height

It can be seen from the range that the thickness is not necessarily uniform, especially in the thicker samples. It can be seen that in the thickest sample the range of measurement was as large as 60 nm. This may be due to the semiconductor not spreading as efficiently because of the slower speed. Despite this inaccuracy in thickness, a clear trend confirms that higher spin speeds reduce the thickness of the sample, and that 3000 rpm appears to be a maximum speed at which semiconductor material can be applied. Finally it was observed from these results that there was no height detectable for the gold evaporated onto the sample. There appeared to be a transparent layer that prevented any difference in height. A possible explanation for this would be some residual contact solution that had not evaporated. If this is the case then it may explain the improvement in contact resistance denoted in Hysteresis and Contact Resistance in Section 3.9. With the non-uniformity of the lower spin speed and physical restriction of the higher, semiconductor thickness measurements were not possible to accurately measure with the facilities available – there is also a question as to whether the range obtained provides enough of a difference in thickness to have a noticeable effect on the output – the variation in thickness per sample alone is on occasion larger than the difference between samples. However, there is some recorded impact on results and these are studied later in this chapter.

4.4.2 Oxide Variations

Adjusting and measuring of changed in oxide thickness were more controllable as these can be altered in the anodisation process by changing the constant voltage. In the AFM measurements the thickness of the oxide was 10 nm across all 3 samples, however as anodisation is a chemical process this is not an accurate reflection of the thickness as the oxide will be grown below the surface of the aluminium as well. In order to measure oxide thicknesses, simple parallel plate capacitors were fabricated by measuring one of the TFT contacts just after the development stage. A capacitance, C, was measured and then divided by the measured area of the sample (W = 2.5x10^{-4} m, L = 1.3x10^{-3} m) to obtain the capacitance per unit area C_{ox}. This could then be combined with the relative permittivity for Al_2O_3, which is ε_{ox} = 9, and the permittivity of free space, ε_0, to obtain the thickness t_{ox} as first shown in Eqn. 4.3-30 and repeated here for clarity.

$$t_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{C_{ox}} \qquad \textit{Eqn. 4.4-1}$$

The results (as shown in Figure 4.4-4) show the expected inverse relationship between C_{ox} and t_{ox} as discussed in Section 4.3.

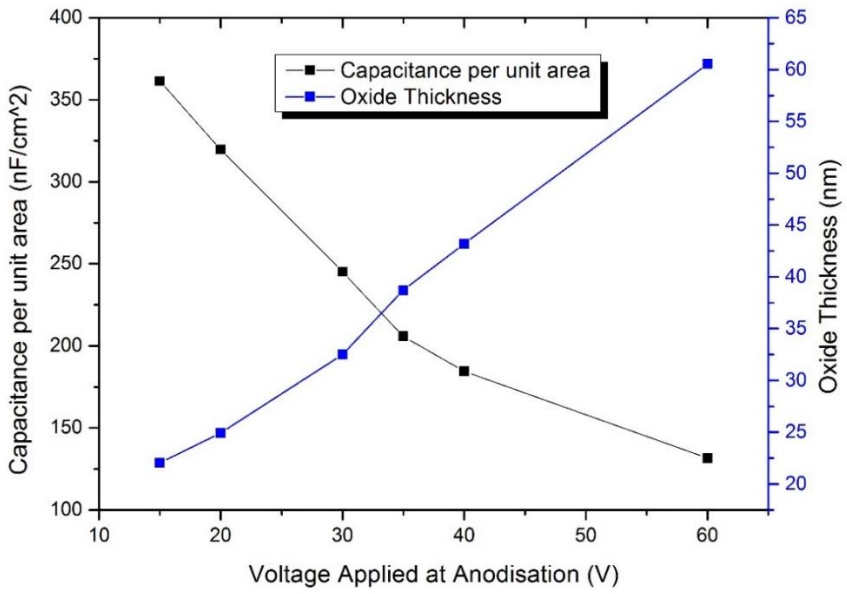

Figure 4.4-4 - Graph showing the relationship between dielectric thickness and capacitance based on a varying applied anodisation voltage. These capacitances were measured by measuring capacitors of Al and Au plates separated by Al_2O_3.The dielectric constant was then used to calculate the corresponding t_{ox}.

This can be confirmed by the results in Figure 4.4-4 showing the comparison of the capacitance and dielectric thickness. This figure also shows that the thickness is controlled by the anodisation process – a higher applied voltage produces a thicker dielectric layer. As C_0 is inversely proportional to oxide thickness then as the thickness is reduced the capacitance increases. In terms of the impact this has on the device performance the drain current is directly proportional to C_0^{2m+1}, as shown by the derivation for current shown in Eqn. 4.4-2. This means it is expected that the current will increase based on the oxide capacitance and therefore with the reduction of the thickness. (NB: disordered form used for simplicity).

$$I_{DS} = \frac{W}{L}\frac{K{C_0}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(\frac{V_G - {V_T}^{(2m+2)}}{2(m+1)(2m+1)} - \frac{(V_{GS} - V_T - V_{DS})^{(2m+2)}}{2(m+1)(2m+1)}\right) \qquad \textit{Eqn. 4.4-2}$$

As a result, it is expected that the drain current will increase with a reduction in oxide thickness as a combined effect of the reduced capacitance to a factor of 2m+1. Figure 4.4-5 shows the $I_{DS}V_{GS}$ results for three devices with t_{ox} of 22 nm, 35 nm and 45nm respectively. Both devices had a *W/L* of 150 and were fabricated in the same batch of samples to minimise variation between thicknesses of other layers as much as possible. It can be seen in these results that there is an order of magnitude between on currents which follows the estimated inverse proportionality of I_{DS} on oxide thickness. While t_{ox} has only been reduced by 50% the x10 increase in current can be attributed to the 2m+1 exponential.

Thinner oxides also have an impact on the value m, as will be discussed later in this chapter, which accounts for the increase in current not being linearly proportional.

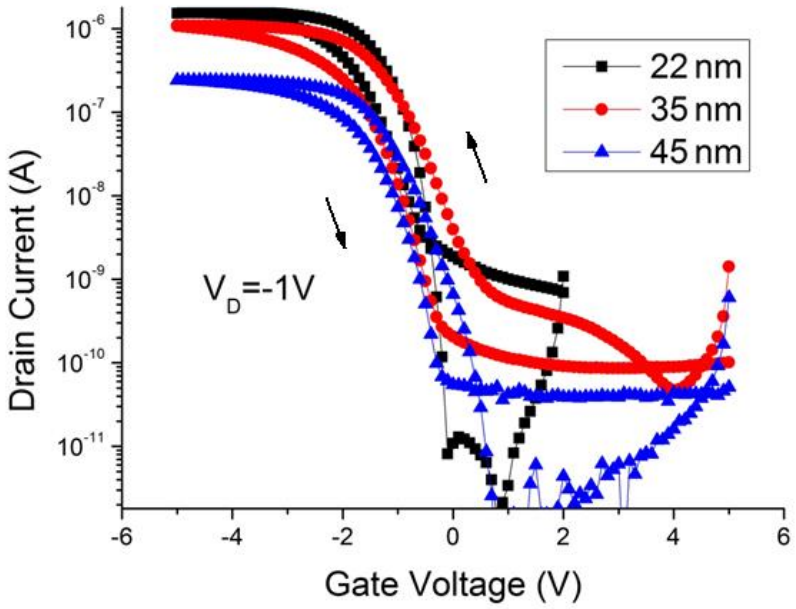

Figure 4.4-5 Results of thinning oxides down to 22 nm and 35 nm. The $I_{DS}V_{GS}$ characteristics indicate an increase in off current at the cost of off current leakage. Measurements were taken at a low drain voltage of -1V as the reduction in oxide also resulted in a lower breakdown voltage.

The difference in on currents are shown more clearly in the linear plot of the same data in Figure 4.4-6.

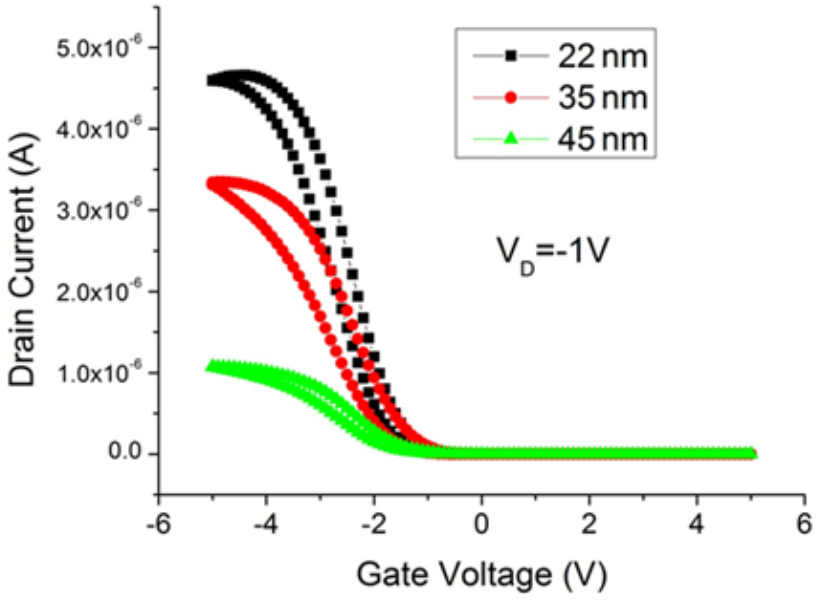

Figure 4.4-6 – Linear plot of the 22 nm, 35 nm and 45 nm devices to better show the difference in on current. The 22 nm has the highest on current as shown by the black line, the 35 nm in the middle is shown by the red line and the 45 nm had the lowest on current as shown by the green. The V_D = -1 V

The results also show the predicted increase in leakage current with thinner oxides, as evidenced by the difference in off current below the threshold voltage. This is shown in Figure 4.4-7 where it is clear that the 22 nm oxide device, the thinnest, exhibits the highest gate leakage

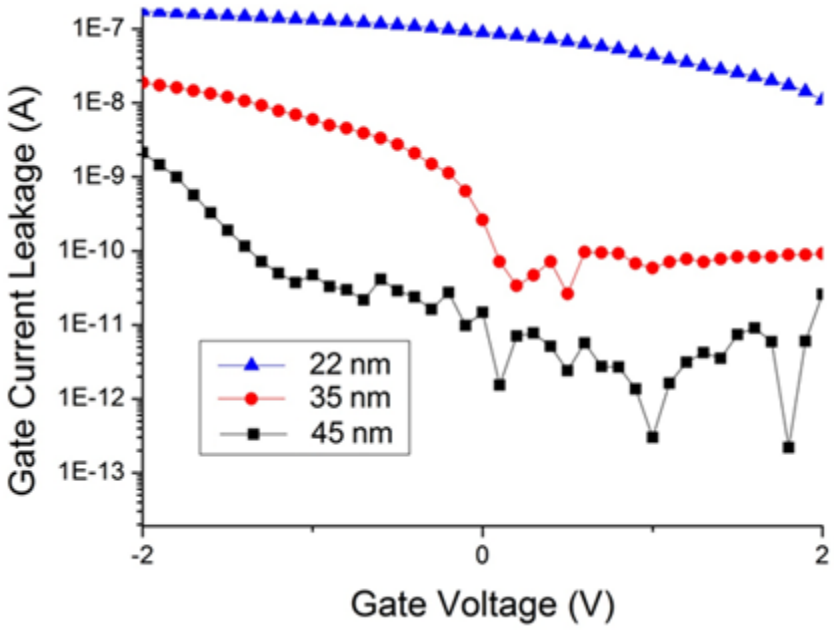

Figure 4.4-7 – Off currents of the 3 devices displaying the same expected differences in leakage currents based on oxide thickness. As with the on currents, the black 45 nm device has the lowest off current, followed by the red 35 nm device. The blue 22 nm device has the highest off current which is in line with thinner oxides having highest leakage. As with the previous graphs, V_D = -1 V.

A practical issue that emerged at the measurement stage was the breakdown voltage. Oxides as thin as 20 nm were not able to handle more than 7 V either as a gate voltage or as a drain to source voltage. Samples also proved difficult to probe due to the measuring needles piercing through the oxide, even due to the force of the air circulating in the room. This is a design consideration that will be taken into account for the circuits designed in Chapter 5 as it highlights the importance of measurement pads not being directly above the oxide layer. Measurements of thicker oxides at a drain voltage of -10 V also supported the t_{ox} relationship in Eqn. 4.3-30. As shown in Figure 4.4-8, the 60 nm device correspondingly has the lowest on current, an order of magnitude lower than that of the 35 nm device.

As the 45 nm device is the standard device that the process has been optimised for, it is possible that this is the cause of the higher output – however, as the processing and level of disorder in these materials can be unpredictable and, as stated previously, the semiconductor thickness can be difficult to control, it is possible that this was due to other factors influencing the results.

The silicon theory implies that the threshold voltage should reduce if oxide is thinned. While there is clearly a variation with V_T for different thicknesses, these examples do not appear stable enough to

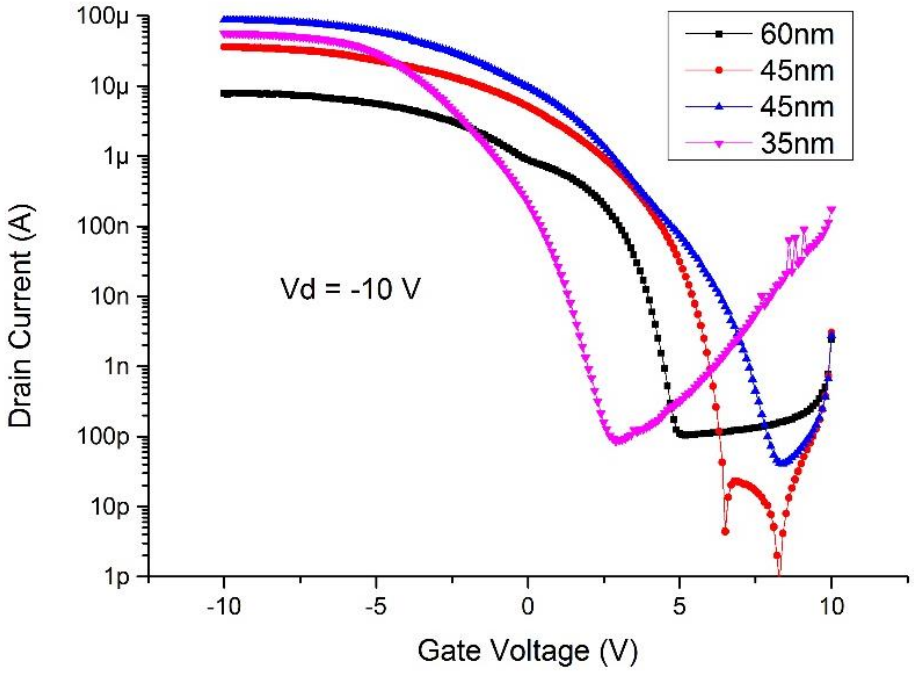

Figure 4.4-8 Transfer characteristics for TFTs with varying oxide thickness. Sweep from 10V to -10V showing variation in off current and on current performance. These results show the same dependence as the thinner devices with the exception of a higher performing 45 nm device shown by the blue line. The black, red and pink line represent a 60 nm, second 45 nm and 35 nm device respectively.

secure a trend. From another angle, however, this lack of consistency could serve as a possible explanation for the discrepancies in on current proportionality. If the threshold voltages were aligned, extrapolating the traces could indicate that the loss of current could be a result of this offset and that were a higher voltage applied, the current for the 35 nm device could at least match that of the thicker devices.

There is also the improvement of mobility with scaling of devices. In order to test this, the mobility parameters *K* and *m* were extracted for the 22 nm and 35 nm devices from Figure 4.4-5. These were extracted from the slope and intercept fits shown in Figure 4.4-9.

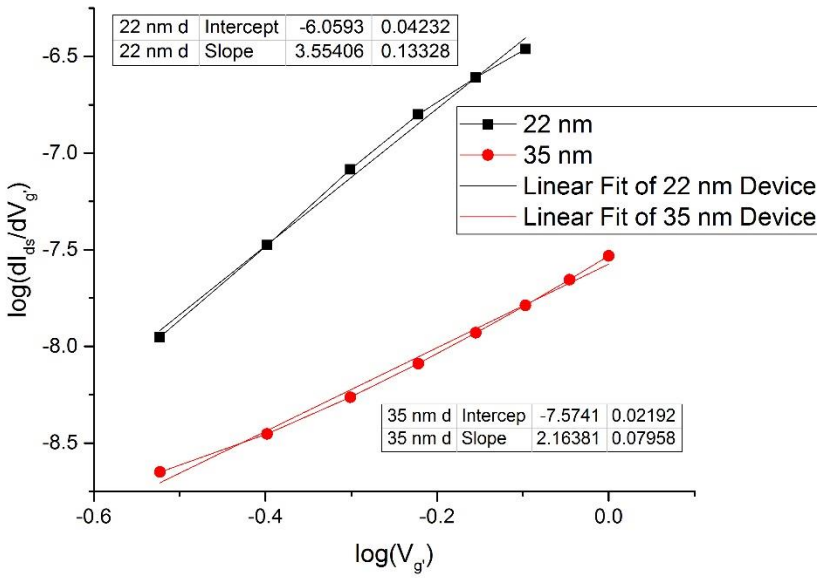

Figure 4.4-9 Slope and intercept for the two thinnest oxide devices.

The slope and intercept were run through a Matlab program written to extract m and K and the results were as shown in Table 4.4-3.

Table 4.4-3 m and K values extracted from the log plots of the 22 nm and 35 nm device

t_{ox} (nm)	*m*	*K* (AV^{-m})
22	1.770	2.1075e-18
35	1.082	1.2904e-14

It can be seen in with these that while the constant *K* is lower for the thinner material, the exponential parameter *m* is higher, producing a much steeper mobility than the thicker oxide. This is in line with the theory that as the oxide thins, the mobility is increased.

4.4.3 Organic Dielectric Variations

An alternative to using aluminium oxide for the gate dielectric is the use of an organic dielectric. The main benefit of organic dielectrics are that if there is a reduction in thickness of the dielectric, this can be compensated for by using a lower-*k* dielectric. There is also a benefit in low-*k* dielectrics for the purposes of insulation in circuits. They form a better interface with the OSC and, as there is the possibility of patterning dielectrics (as discussed in Chapter 3). For this reason, there is scope for exploring this as the interest in organic circuitry grows.

In order to see how the thickness of the dielectric can be controlled by spin speed, 6 samples were created by spinning the dielectric Lisicon™ D206 onto glass slides at 3 different spin speeds, 1000 rpm, 1500 rpm and 3000 rpm. Two different concentrations, 13% and 10%, were used. These were custom made by Merck Chemicals Ltd and measured using a profiler. In general, a lower concentration results in a thinner solution and therefore a thinner layer. The different spin speeds and concentrations produced the results in Table 4.4-4.

Table 4.4-4- Dielectric thicknesses corresponding to different spin speeds and concentrations

			1000		**1500**		**2000**		% Reduction of thickness
			Thickness (µm)	**σ^2 (µm)**	**Thickness (µm)**	**σ^2 (µm)**	**Thickness (µm)**	**σ^2 (µm)**	
Concentration	13%		1.360	1.78×10^{-10}	1.08	0	0.910	$2.50\text{x}10^{-11}$	
			1.380	$4.44\ \text{x}10^{-11}$	1.08	0	0.920	$2.50\text{x}10^{-11}$	
			1.380	$4.44\ \text{x}10^{-11}$	-	-	-	-	
		Avg.	**1.370**	**1.33** $\text{x}10^{-10}$	**1.08**	**0**	**0.915**	**5.00** $\text{x}10^{-11}$	**32%**
		Avg.		**1.15** $\text{x}10^{-2}$		0	**-**	**7.07** $\text{x}10^{-3}$	
		Error		**6.67** $\text{x}10^{-3}$		0	**-**	**5.00** $\text{x}10^{-3}$	
	10%		0.590	$5.88\ \text{x}10^{-7}$	0.510	0	0.450	$2.50\ \text{x}10^{-11}$	
			0.630	$5.78\ \text{x}10^{-7}$	0.510	0	0.440	$2.50\ \text{x}10^{-11}$	
			0.620	$5.44\ \text{x}10^{-7}$	N/A	-	N/A		
		Avg.	**0.613**	**5.83** $\text{x}10^{-7}$	**0.510**	**0**	**4.45E-07**	**5.00** $\text{x}10^{-11}$	**26%**
		Avg.		**0.764**		0		**7.07** $\text{x}10^{-3}$	
		Error		**0.441**		**0**		**5.00** $\text{x}10^{-3}$	
		% Red.	55%		53%		51%		

This data implies that reducing concentration seems to have a large impact on the thickness, almost halving it with a 3% lower concentration. This means a 33.3% reduction in concentration produces a thickness reduction of 55-51%, with the size of the reduction also showing a dependence on the thickness of the layer.

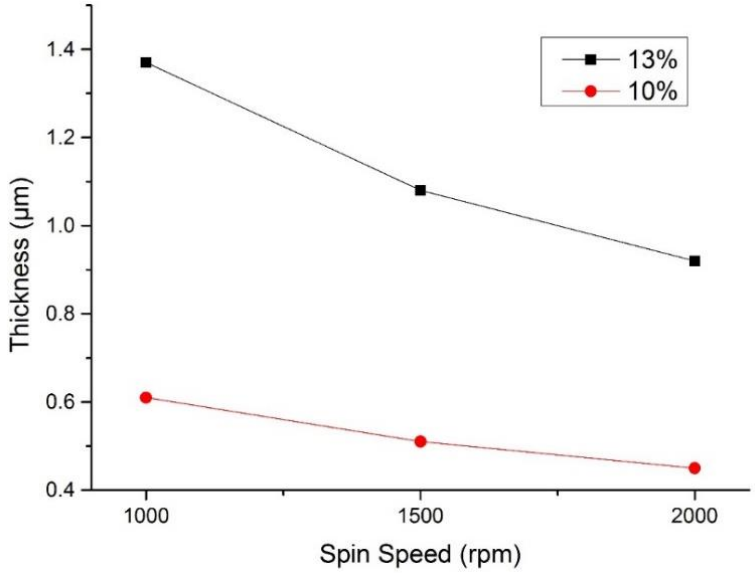

Figure 4.4-10 - Variation of dielectric thickness as a result of altering spin speed for two different concentrations. The black points represent the 1000, 1500 and 2000 rpm spun devices with organic dielectric Lisicon™ D206 with a concentration of 13% and the red points correspond to the same for 10% concentration.

The effect of increasing spin speed for the lower concentration does not have as much impact as it does for the higher concentration, as the thickness reduces by 26% between the 1000 rpm and 2000 rpm spun samples at 10% compared to a 32% reduction at 13% concentration. While the sample size for the experiment is small, the overall trend still follows a reduction, even when errors are taken into consideration.

These results show that both deposition speed and concentration are effective methods of reducing dielectric thickness, both combined and using just one of these methods. At lower concentrations, spin speed has less of an effect on the reduction, however, that would indicate that it is easier to control the thickness at lower concentrations, provided the desired thickness is within this range. This means that there would be more control over thickness at lower concentrations, however, there is less variation between thicknesses.

Table 4.4-5 Drain current values as extracted from devices with varying dielectric thickness. The off and on currents are noted as well as the on/off ratio for the three spin speeds at both concentrations. For each set of readings, the top corresponds to a V_D of -5 V and the bottom to a V_D of - 60 V

			SPIN SPEED (RPM)		
		MEASUREMENT	1000	1500	2000
CONCENTRATION	10%	Off currents (nA)	0.95 10.6	0.66 4.4	1.1 10.4
		On currents (µA)	95 95	110 110	6 6
		On/off ratio	1.40×10^4 9.00×10^3	2.10×10^4 2.50×10^4	5.80×10^2 5.80×10^2
	13%	Off currents (nA)	0.33 3.3	1 5.8	0.63 4.3
		On currents (µA)	8.2 59	12 83	13 88
		On/off ratio	2.50×10^4 1.80×10^4	1.10×10^4 1.40×10^4	2.00×10^4 2.00×10^4

It can be seen from the on current data in Figure 4.4-11 that the highest current produced for the 10% solution was at the optimised spin speed of 1500 rpm. This was also the case for the 13% dielectric as well which could be due to the materials being optimised to perform with this processing technique. The worst for the 10% concentration was the sample spun at 2000 rpm and therefore would have been the thinnest layer tested.

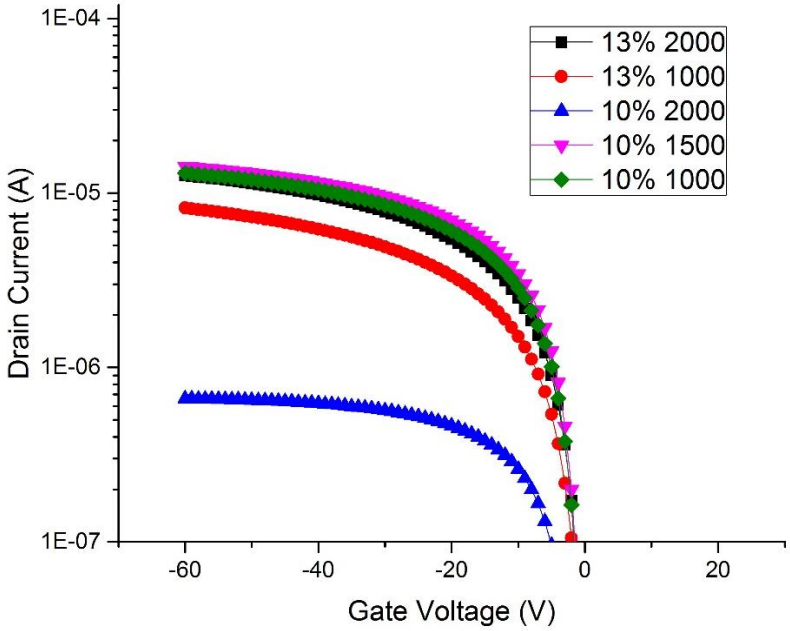

Figure 4.4-11 –On currents of devices with the dielectric thicknesses detailed in Table 4.4-5. V_D = -5 V.

It could be that the combination of the lower concentration and the fastest spin speed damaged the dielectric and worsened performance due to the layer being too thin. Aside from this sample, the other results followed the expected trend that thinner dielectric produced higher on currents.

The off current data shows that the lowest off currents produced were for the 10% concentration spun at 1500 rpm; this complements the on current data showing that at 10% 1500 rpm is the most effective deposition speed for the best results. There is little difference for the 1000 and 2000 rpm speeds which shows that the difference in relative quality for off currents was not as bad as for the on currents for the 2000 rpm speed however it still produced the most inferior device. As with the aluminium oxide samples, the thinner layers once again have the highest leakages. Data for devices with a concentration of 13% showed the lowest currents for a speed of 1000 rpm and the device spun at 2000 rpm the second lowest. For both the 10% and 13% samples the results indicate that the thinning of samples, either through concentration reduction or spin speed, can act as a compensating factor for either loss of on current or leakage.

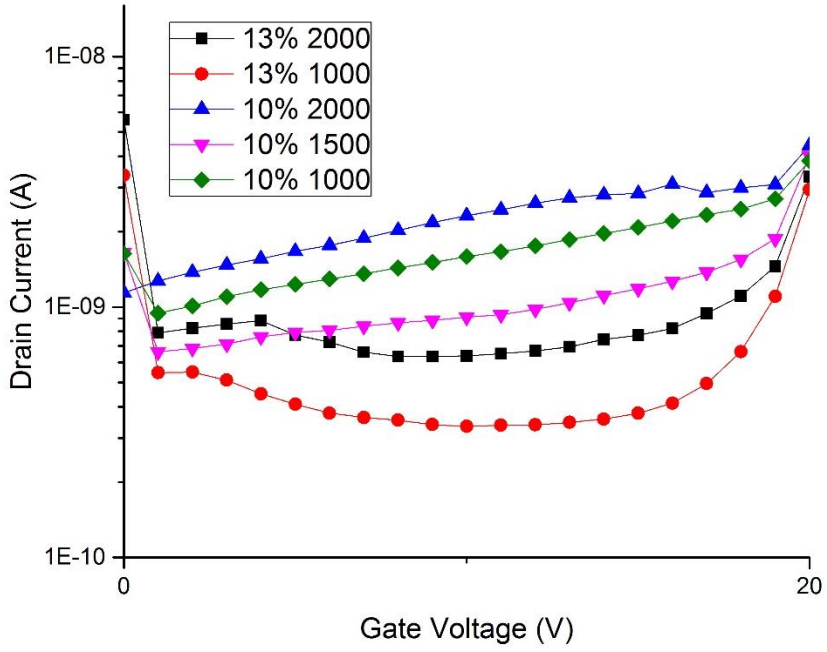

Figure 4.4-12 – Off currents of 5 of the devices. This shows that the 13% concentration devices have the lowest off currents and the 10% concentration devices have the highest. Both concentrations have shown an increase in off current with increasing spin speed indicating an inverse relationship with the increase of dielectric thickness. These samples were measured with V_D = -5 V.

Comparatively with the aluminium oxide samples, the leakage was lower for the organic dielectric samples, but as the devices compared were of a different structure this is potentially invalid. Also, in the context of comparative scaling, the thickness of the dielectric was within the micron region as opposed to the nanometre region of the aluminium oxide.

4.4.4 Organic Semiconductor Variations

Based on the impact that both spin speed and concentration had on thinning of the dielectric, the same experiments were carried out for semiconductor deposition.

The semiconductor thickness was altered by changing spin speeds. For a direct performance comparison, two device samples were fabricated: Sample 1 and Sample 2. Each were made in the same processing batch, with the same oxide, gate and contact thickness. The samples were then deposited with the semiconductor at differing spin speeds, Sample 1 at 1000 rpm and Sample 2 with a thinner layer deposited at 3000 rpm. After measuring, the semiconductor was then removed from each sample and reapplied but with the opposite alternative spin speed. This is denoted by Sample 1 and Sample 2 at 3000 rpm and 1000 rpm respectively in Figure 4.4-13. It is clear from these results that regardless of the order of testing or quality of sample the off currents reduced with the thinner semiconductor.

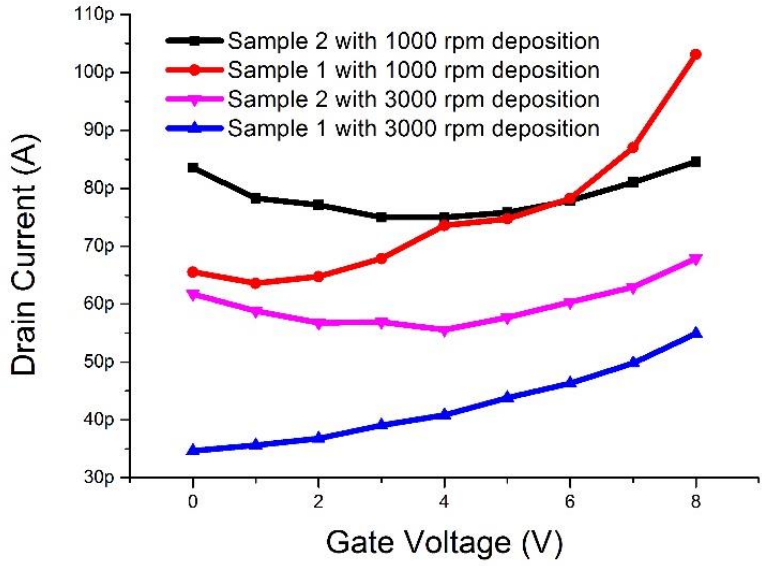

Figure 4.4-13 – Off currents for 2 different samples with W/L 150 and t_{ox} of 32 nm. Each device had semiconductor deposited at either 1000 rpm or 3000 rpm and measured. This was then removed and had a semiconductor spun at the higher/lower spin speed. This was to reduce as many variables in device as possible. V_D = -5 V.

Contrary to these results, a second set of samples produced very similar off currents, despite being different thicknesses. For these devices the different thicknesses of semiconductor consisted of one being spun at the faster speed of 2000 rpm and the thicker sample being spun at 500 rpm with a double application. The off current results for these devices were the same for two different aspect ratios as well, as shown by Figure 4.4-14. While off currents for the thicker semiconductor were expected to be higher, it was the case that these dropped down below the thinner device and were in the same order of magnitude.

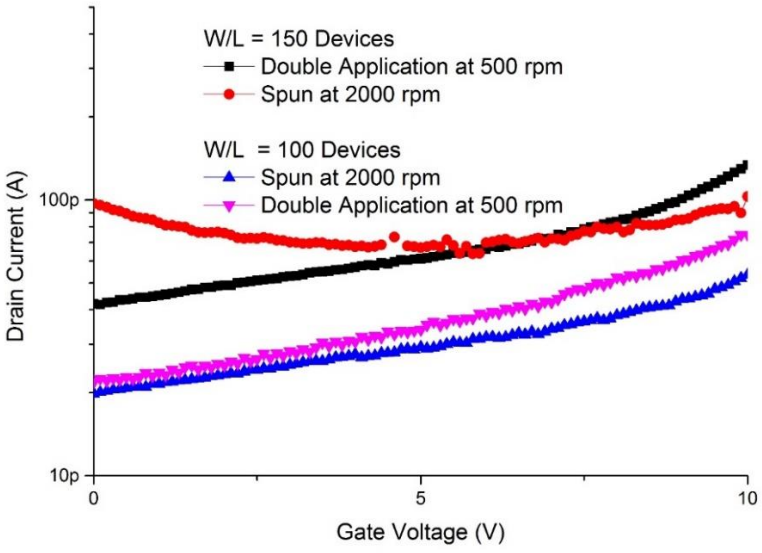

Figure 4.4-14 – Off currents of 2 devices with W/L of 150 and 100 respectively. As with the samples in Figure 4.4-13, these had a semiconductor deposited to create two different thicknesses. The thicker layer was 2 layers of semiconductor deposited at 500 rpm and the thinner was spun at 2000 rpm. V_D = -5 V.

When analysed alongside the on currents in Figure 4.4-15, it is also clear that the double deposition exhibited higher on currents for both aspect ratios of devices. While the thickness of the semiconductor in this case showed no trend in terms of aspect ratio, it was clear from the 2000 rpm device that the smaller device size had a lower off current but also a lower on current. This was also in line with what was expected from the current equations.

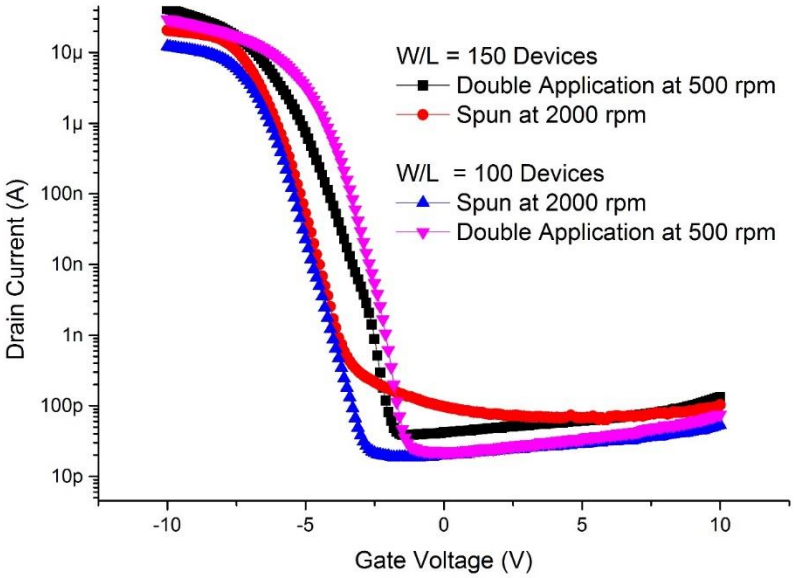

Figure 4.4-15 – Full $I_{DS}V_{GS}$ characteristics of the devices in Figure 4.4-14. The black and red lines represent the 150 W/L device with the thinner and thicker semiconductor layer respectively and the blue and pink lines represent the same for the 100 W/L devices.

Another method for thinning the semiconductor was to reduce the concentration. This had been ratified by the direct result on the thinning of the dielectric with a reduced concentration, and as with the dielectrics custom made materials from Merck Chemicals Ltd were used made to compare concentrations of 1%, 1.5% and 2%. The three different concentrations were measured for their current characteristics, the results of which are detailed in Figure 4.4-16 and Figure 4.4-17.

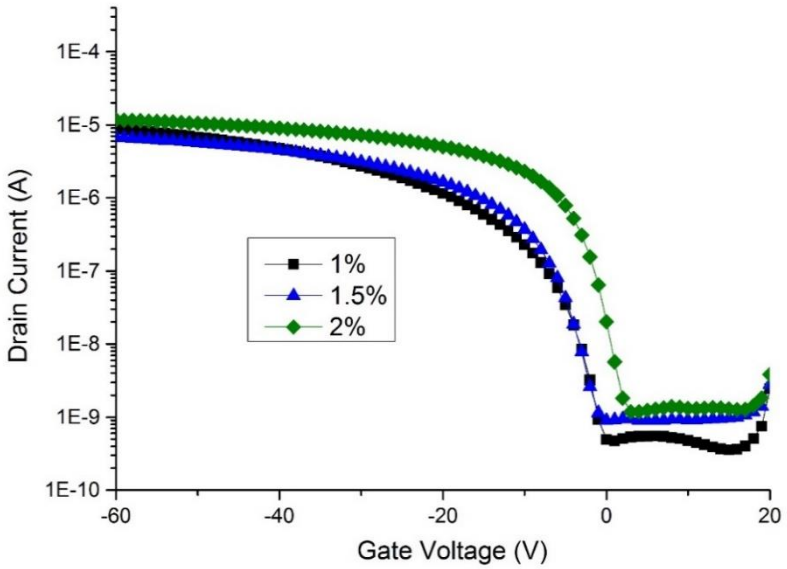

Figure 4.4-16 – Full transfer characteristics for 3 devices with semiconductor thickness altered by change in concentration. Each of these devices has a W/L of 20. The three different concentrations of 1%, 1.5% and 2% are represented by the black, blue and green lines respectively.

It can be seen from the graph above that 1% concentration has the lowest off current in comparison with the standard 2% concentration. This may well be due to the reduction of density of states similar to the effects found in polycrystalline silicon[32]. This yields the larger on/off ratio in comparison with the 2% solution however the on currents for the standard solution remain better. It was noted that the 1.5% solution produced the worst results; this implies that either the data was not reliable or an optimum must be found if reducing size through concentration variation.

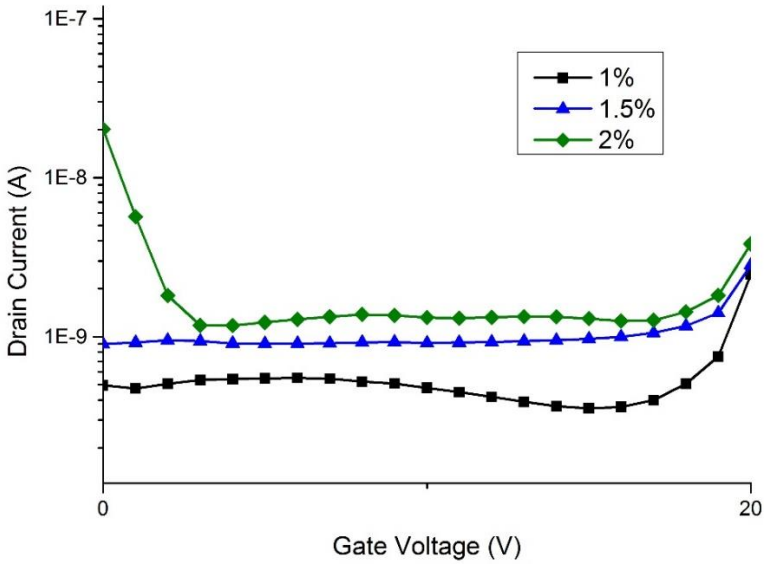

Figure 4.4-17 – The off currents of the device in Figure 4.4-16 showing an increase in off currents with higher concentration. This is in line with the thinner semiconductors reducing the leakage current

4.5 Summary and Conclusions.

This chapter considered the rules of scaling for crystalline materials and the implications for OTFTs if the same theory was to be applied. As OTFTs possess different transport mechanisms as well as a different structure to traditional MOSFETs, it follows that a new set of rules must be defined. For example, one of the key parameters in scaling of silicon technology was the dopant in depletion regions. The channel length was reduced to improve speed and performance but as a result the depletion regions will eventually overlap and ultimately gate control of the device was lost. This was compensated for with doping to enable smaller depletion regions which has a detrimental effect on threshold voltage and so forth. With OTFTs operating in accumulation mode, depletion region doping is not a scaling parameter for organics, but other factors such as grain size, dielectric pin-holing and contact resistance have been found to have an impact.

Considering the differences, there is the question of whether scaling will have the same benefits that have served the silicon industry. There are of course the universal scaling benefits not defined by structure such as yield - the smaller the devices are, the less chance there is of hitting defects, plus more devices can be produced per square of substrate. This was looked at in the context of practical issues that had occurred within the project and it was shown how smaller devices would have prevented the number of devices that had been affected. Another attractive benefit for scaling organics is that, like silicon, the time for switching follows the relationship $t \propto \frac{L^2}{\mu}$, where the switching time of an inverter is proportional to the square of the channel length and inversely proportional to the mobility. This was derived to be also true for organics by examining the fall time of a saturated load transistor examined with organic current models derived in Chapter 2. This derivation also showed a relationship between the mobility parameters, *K* and *m*, so with organic materials generally operating at lower mobilities, scaling could potentially act as a compensating factor.

In order to find practical evidence for the proposed scaling theories, various samples were fabricated and tested to compare results with a scaling variable applied. These included a range of tests that compared changes in oxide thickness for both Al_2O_3 and the organic dielectric Lisicon™ D206 as well as semiconductor thickness varied by both spin speed and concentration.

Experiments on oxide thickness supported the scaling theory proven in silicon devices that a thinner oxide produced a higher current output. This was shown across a range of devices and showed a clear dependency on both the increase of on current but also in off current leakage, displaying the down side of this method of scaling. One anomaly to this was the performance of devices at the optimum fabrication, an oxide thickness grown at an anodisation voltage of 30 V. This produced better results

in both on and off currents as well as a higher on/off ratio compared to the other samples produced within the same batch. This could be due to the fabrication method having been tailored to this thickness. The tests run on Lisicon™ D206 examined both the scaling of the material using material concentration and spin speed to control the thickness of material. It was clear that both concentration and spin speed altered the thickness of dielectric, with control over thickness being easier at a lower concentration. While the results generally showed that a thinner oxide produced a higher current and higher leakage, it was also found that once again the thickness at 1500 rpm with a concentration of 13%, the conditions used in the normal fabrication process, produced the best results and the thinnest layer, 10% spun at 2000 rpm produced the weakest across all samples. This could imply that there is either an optimum thickness for performance, or that the process is customised to facilitate this and also that layers begin to degrade if too thin. Implies that processing techniques could also need to be adapted if devices were to be scaled.

Other indications for the benefits of scaling would be the reduction of leakage current when the OTFT is in an off-state as shown in Section 4.4.4. As this current is dependent on the resistivity of the semiconductor, it follows that reducing the thickness of the semiconductor layer should reduce the resistivity and in turn reduce the off current value. This was tested by altering the semiconductor thickness across a range of samples with a constant oxide thickness. This was shown to be true for samples that had two different thicknesses applied to the same sample. An initial semiconductor thickness had first been spun and tested before being removed and replaced with one spun at a lower or higher spin speed. Another discovery made with this process was the reduction of hysteresis and contact resistance commented upon in Chapter 2. This has an implication that the second application of contact solution, or the chloroform cleaning process, improve the OSC interface. It was also found that a double application of semiconductor can improve performance as well. In two samples, an OSC layer spun at 2000 rpm was compared with a thicker layer formed by a double deposition and both found an improved performance with the dual-deposition sample in spite of its larger thickness. This indicated that there could be benefits in double deposition outside of the context of scaling.

A potential hindrance of scaling is the limiting Debye length, as scaling down to thicknesses thinner than the Debye length would therefore have an effect on the number of conducting carriers in the channel. This was explained in a diagram of the semiconductor/dielectric interface and showed that in order to combat a reduction in semiconductor performance, the charge at the interface could be increased by improving the capacitance. This could be achieved by further scaling of the oxide thickness (as shown in Section 4.4.2), though this comes at the cost of increasing gate leakage. Other

proposed methods include adding a second dielectric layer to increase the dielectric constant and exploring organic dielectrics.

4.6 References

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Chapter 5 CIRCUIT DESIGN

5.1 Background

As organics becomes a more viable contender in commercial industries and the scope of organics increases there is a pressing need, and valuable potential, in ensuring the technology is available to make organic circuits that can be fully integrated[1]. Integrating output and control technologies allows for simpler manufacturing processes and opens up the possibilities for applications which may have in the past been restricted (such as use of flexible substrates)[2].

Development of shift registers in organics is the foundation for controlling fully organic row-column drivers, such as the backplanes used to control OLED active matrix displays[3]. Shift registers allow for signals to be controlled by remembering an input condition and passing it along a series of outputs – as detailed in the following section. Dynamic shift registers in particular do so by using pass transistors to effectively trap a charge until a clock allows for the charge to be used in the next stage of the circuit (usually to feed an inverter). With this method, the timing of the clock pulses allow for the stored charge to be fed through systematically and the input conditions remembered until needed. This has benefits in terms of power consumption and ease of use – however, leakage of the stored charge can be an issue if the time constant is not carefully accounted for in the design.

The evolution of designs from NMOS through to CMOS and Pseudo-NMOS optimised the benefits of the predecessors of organics. Similarly to how silicon developed Pseudo-NMOS by implementing a PMOS load, the possibility has been examined as to how the complementary function of CMOS using only PMOS devices could be implemented, thus saving power and eliciting the benefits along with the added advantage of having to only fabricate one type of transistor device. It also looks at the aforementioned use of device parameters to design and simulate a shift register with these technologies.

5.2 Inverter Design Based on Parameters

5.2.1 Adapting Simulation Models

While the Cadence software used is based mainly upon silicon models, it is possible to adapt these to achieve more organic like device behaviour. While prior models had been devised by other group members, all of the inverters for this study were implemented with values extracted from the devices characterised in Chapter 3 based on the models in Chapter 2. While the spice models are still inherently based on silicon, these amendments allowed the designs to reflect the results from the project as closely as possible with the software available for the project.

Table 5.2-1 shows the parameters that can be adapted within the Cadence model files. The majority of these relate to the structure of a silicon device and could not be altered, but 4 of the core values were able to be changed to better reflect the parameters extracted from the analysis in Chapter 3. The rows of these values are highlighted and they include the threshold voltage, V_{T0}, oxide thickness, t_{ox}, surface mobility, μ_0 and off current value, *is*.

Table 5.2-1 – SPICE Parameters that can be altered within the model file to run simulations. The default values for the organics models devised previously are shown in the table, but those that can be changed based on the devices characterised in Chapter 3 are highlighted in grey.

Parameter	Description	Value devised for default organic model	Unit
pmos level	Selection of empirical model	3	-
V_{T0}	Threshold voltage	0	V
nsub	surface doping	9.15×10^{15}	cm^{-3}
t_{ox}	Oxide thickness	9.25×10^{-9}	m
gamma	Body effect factor	0.69	$V^{1/2}$
theta	mobility degradation factor	0.5	V^{-1}
phi	surface inversion potential	0.67	V
μ_0	mobility	0.18	cm^2Vs^{-1}
delta	narrow width factor used to adjust threshold	0.96	-
cj	junction bottom capacitance density	3.1×10^{-4}	Fm^{-2}
mj	junction bottom grading coefficient	0.5	-
pb	junction bottom built in potential	0.76	V
cjsw	periphery capacitance	3.67×10^{-10}	Fm^{-1}
nfs	fast surface state density	1×10^{10}	$cm^{-2}V^{-1}$
eta	static feedback	0.06	-
kappa	saturation field factor	9.23	V^{-1}
xj	metallurgical junction depth	0.5×10^{-6}	m
js	leakage current density	1×10^{-8}	Am^{-2}
xw	width bias (corrections for etching/masking effects)	0	m
xl	length bias (corrections for etching/masking effects)	0	m
hdif	length of heavily doped diffusion	3×10^{-6}	m
wd	lateral diffusion into channel width	0.034×10^{-6}	m
is	leakage current	5×10^{-9}	A

The values shown in Table 5.2-1 represent the default model that had been devised previously and used within the research group. The necessary parameters will be adapted to fit the values extracted from Chapter 3 in Section 5.2.2. It is assumed for the purpose of this project that the other values can remain unaltered as they have previously been optimised for organic device simulation.

Based on the evidence in Chapter 4, it was found that the optimised concentration of 2% with semiconductor spun at 1500 rpm was the most viable for performance and therefore the device with *W/L* of 150, t_{ox} of 32 nm measured at V_D = -5 V will be used. The $I_{DS}V_{GS}$ characteristics are shown in Figure 5.2-1. The processing code-name for this device was EAJ which will be the name used for the model code.

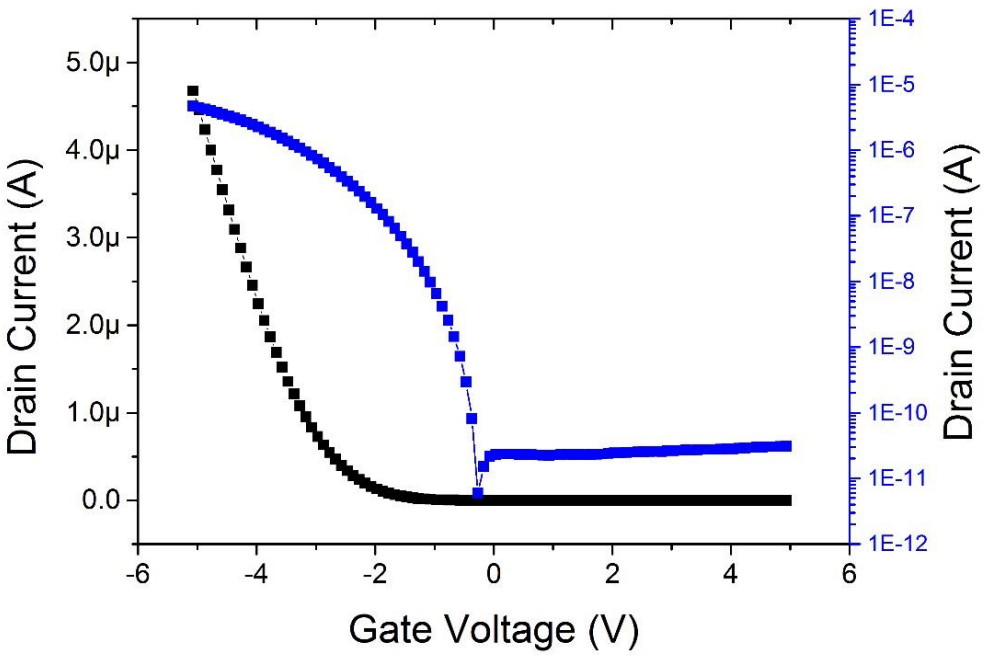

Figure 5.2-1 – Transfer characteristics for device used for parameter extraction to simulate circuits. V_D = -5 V.

By focussing on specific regions of these characteristics the values for V_{TO} and *is* can be obtained using the $\sqrt{I_{DS}}$ trace and the off current values respectively. This is shown in Figure 5.2-2 and were extracted as -1.6 V and 3×10^{-11} A respectively.

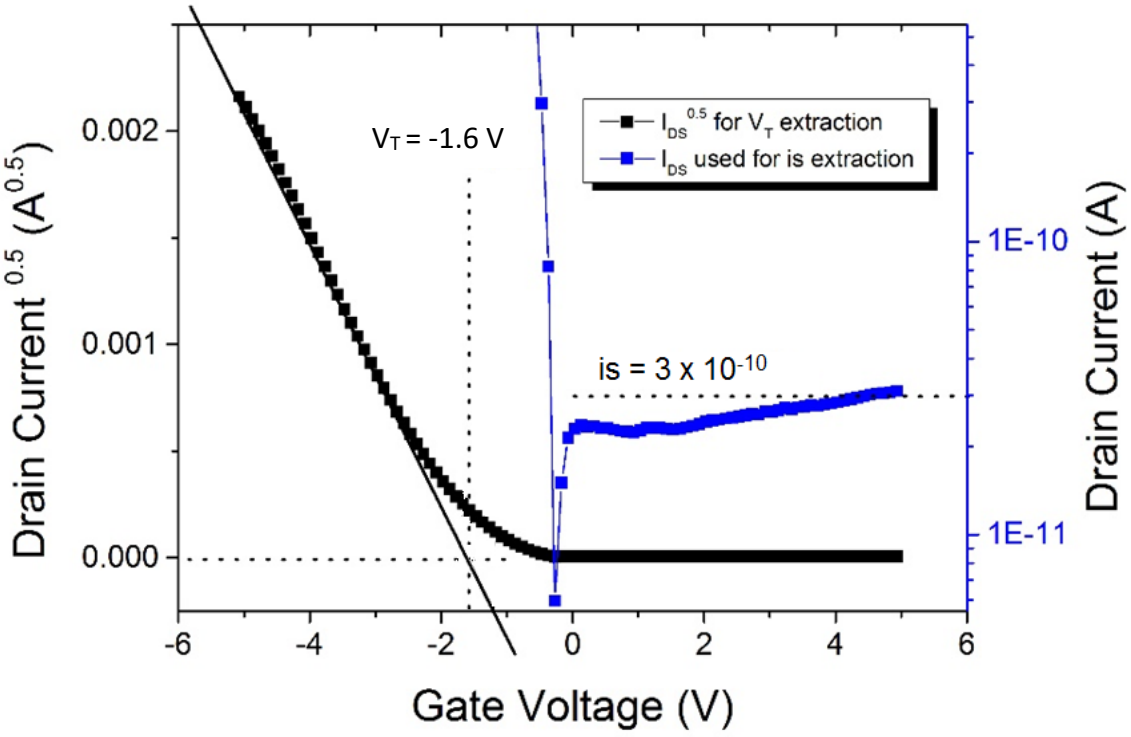

Figure 5.2-2 – Extraction of is and V_T from the $I_{DS}^{0.5}$ and I_{DS} traces respectively. The values for these parameters are shown to be -1.6 V and 3x10^{-11}A and can be used to optimise the simulation models.

5.2.1.1 Mobility

As detailed significantly in Chapter 2, the mobility depends on carrier concentration in organic materials. This means that simulation models used for crystalline materials are inaccurate and an effective mobility must be used.

The mobility for the device was calculated in Section 3.7 and has been shown to vary with gate voltage in Eqn. 1.7-24. In order to best emulate the use of a single mobility, an average mobility was taken rather than using the varying mobility for which the model could not cater. This value was calculated as 0.03 $cm^2V^{-1}s^{-1}$ using Eqn. 3.7-24.

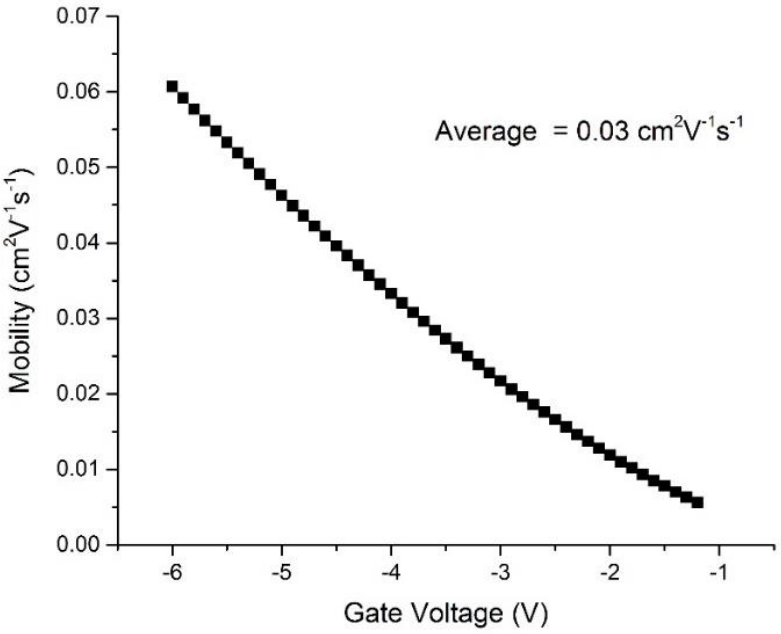

Figure 5.2-3 – Plot of the mobility for device characterised in Section 3.7.1 to obtain model parameters. This mobility is calculated using the equation derived in Section 3.7.3.

5.2.1.2 Dielectric Thickness

The models used for simulation throughout this project were those that had been adapted to work with organics variables. The gate oxide thickness was extracted as

$$t_{ox} = \frac{\varepsilon}{C_{ox}} \qquad \textit{Eqn. 5.2-1}$$

As alumina was used as the gate dielectric, an equivalent oxide thickness (OTFT) was found as follows:

$$C_{ox} = \frac{\varepsilon_{sil}}{t_{ox}} = \frac{\varepsilon_{OTFT}}{t_{OTFT}} \qquad \textit{Eqn. 5.2-2}$$

Hence

$$t_{ox} = t_{OTFT}\frac{\varepsilon_{sil}}{\varepsilon_{OTFT}} \qquad \textit{Eqn. 5.2-3}$$

For t_{OTFT} = 32.5 nm, the silicon dioxide permittivity of 3.9 and the Al_2O_3 permittivity of 9.8, t_{ox} = 12.9 nm.

5.2.2 Parameter Application and New Model

The parameter values for devices using the Lisicon™ S1200 material are shown in Table 5.2-2.

Table 5.2-2 – Relevant parameters from Table 5.2-1 updated with the values calculated and extracted for devices characterised in Section 3.7.1.

Parameter	Value	Unit
μ_0	0.03	cm^2/Vs
t_{ox}	12.9×10^{-9}	m
V_{T0}	-1.6	V
is	3×10^{-11}	A

The test configuration for the transistor, with the model code name “EAJ” is shown in Figure 5.2-4.

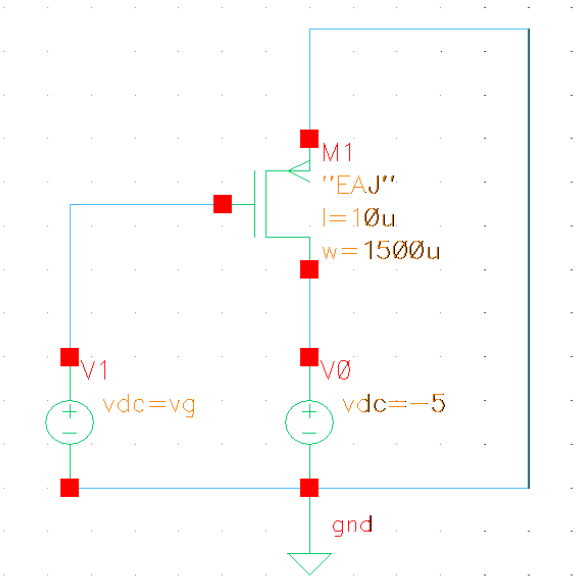

Figure 5.2-4 –Circuit used to test transistor performance with EAJ optimised models

The results of a transconductance sweep plotted against the experimental and theoretical data is shown in Figure 5.2-5.

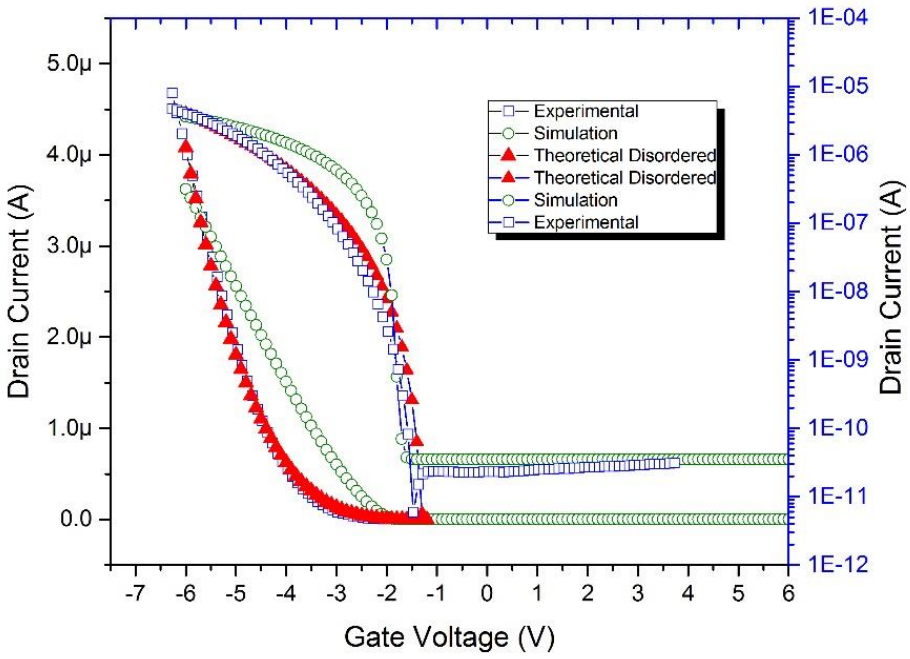

Figure 5.2-5 – Comparison of log and linear plots for the experimental and theoretical results modelled in Section 3.7.1 with the simulated data obtained from circuit in Figure 5.2-4.

It can be seen from this that the simulation model has a much steeper gradient than the theoretical and experimental models. This is due to the constant mobility that is generated within the simulation models based on the crystalline equation. Various mobility values were applied in order to try and optimise this, however it was found that there was no way of improving this value to reflect the gradient without sacrificing the on current value. For this reason, the average mobility was kept as the optimised model.

5.3 Inverter Configurations

A major restriction in organics, and specifically in this project, is to implement inverters using only PMOS transistors. The Lisicon™ material used is p-type and the nature of the fabrication does not allow for integration of different polarity devices. In general PMOS is used as the mobilities are found to be higher than those of organic NMOS devices[7].

The major benefit of CMOS technology is the power saving, as the complimentary function of the PMOS and NMOS transistors means power is only dissipated when switching. This is shown in Figure 5.3-1 a) by the current increase that occurs during switching. This means that the use of saturated load in organics is restrictive in circuit design.

a) b)

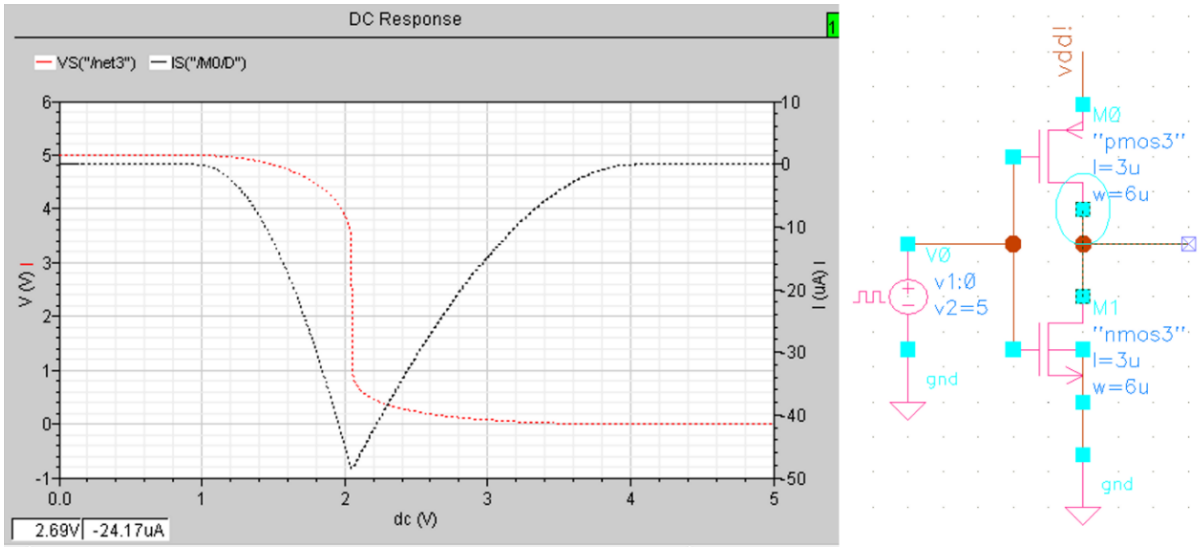

Figure 5.3-1 a) DC characteristics and power output of CMOS configuration inverter in b). This was generated using Cadence models for a p and nmos device, each of L = 3 µm and W = 6 µm.

Pseudo-NMOS is commonly adopted whereby a current source load is produced from a saturated load transistor. The disadvantage is that one device is permanently on and constantly DC power is dissipated when the inverter is static.

5.3.1 Saturated Load Inverter

The circuit diagram for a saturated load inverter and its corresponding dc characteristics are shown in Figure 5.2-3.

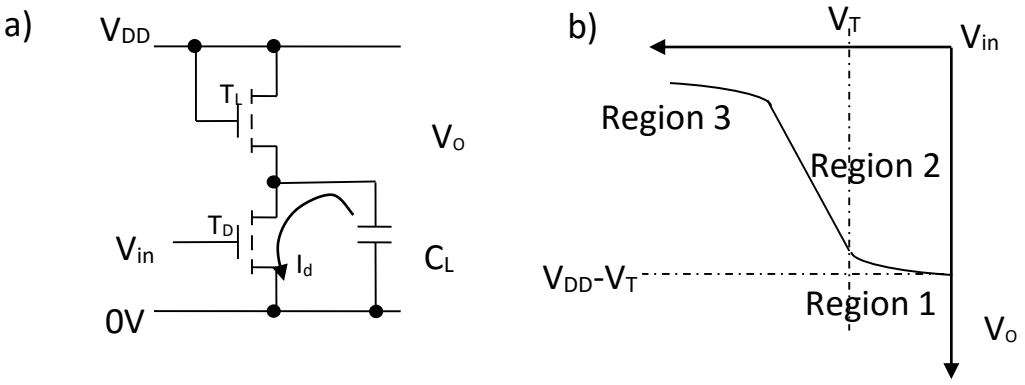

Figure 5.3-2 – Circuit a) and inverter transfer plot b) for saturated load inverter showing three regions of significance

The gate of the load device is connected to V_{DD}. Note that as this is dealing with a p-type material all voltages are negative. As described in Chapter 4, the inverter operates in three main regions. These are summarised in Table 5.3-1 to avoid repetition.

Table 5.3-1 – Descriptions for load and driver states of the 3 regions in Figure 5.3-2. The comparative sizes of voltages for V_{in}/V_T and V_D/V_{in} are noted to clarify the current region within which region is operating as well as the resultant output.

Region	V_{in}/V_T	V_O/V_{in}	Driver	Load	Output
1	$V_{in} < V_T$	$V_O > V_{in}$	Off	On (Sat)	High
2	$V_{in} > V_T$	$V_O > V_{in}$	On (Sat)	On (Sat)	Switching
3	$V_{in} > V_T$	$V_O < V_{in}$	On (Lin)	On (Sat)	Low

Key values that can be extracted from the dc characteristics are the Driver:Load ratio that can be extracted using the slope of region 2, and the threshold voltage, given by the point at which region 1 moved into region 2. Extracting these and comparing them to the theoretical values can give an indication of if the simulation is an accurate reflection.

5.3.1.1 Driver:Load Ratio

As detailed in Section 4.3, ratioed logic for the saturated load inverter is key to ensure a working inverter. For the purpose of the calculations the disordered form of the current equations with an exponential distribution will be used. This is viable due to the conduction in polycrystalline materials being controlled mainly by boundaries, as stated before.

The two current equations for the saturation and linear region of the TFT are repeated in Eqn. 5.3-1 and Eqn. 5.3-2 respectively and a simplified constant is stated in Eqn. 5.3-3.

$$I_{lin} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT\varepsilon_0\varepsilon_S\}^m}\left(\frac{V_{GS}-V_T{}^{(2m+2)}}{2(m+1)(2m+1)} - \frac{(V_{GS}-V_T-V_{DS})^{(2m+2)}}{2(m+1)(2m+1)}\right) \qquad \textit{Eqn. 5.3-1}$$

$$I_{sat} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT\varepsilon_0\varepsilon_S\}^m}\left(\frac{V_{GS}-V_T{}^{(2m+2)}}{2(m+1)(2m+1)}\right). \qquad \textit{Eqn. 5.3-2}$$

For simplicity assumed that the multiplier can be incorporated as a term Y_x where *x* denotes either the driver or load transistor, *D* or *L*, respectively.

$$Y_x = \frac{W_x}{L_x}\frac{KC_0{}^{2m+1}}{\{2kT\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)}. \qquad \textit{Eqn. 5.3-3}$$

To begin with, consider the output V_O to be in an off state. This would put the driver TFT *'T_D'* in an on state with V_{in} being at V_{DD} (in this case 15 V) and V_O at 0.1 (a safely low value). This would put $V_T < V_{in}$ for T_D causing it to operate in a linear regime (where $V_{DS} < V_{GS}$). As T_L is permanently saturated, the two currents can be equated to form

$$I_{lin} = Y_D\left((V_{GS}-V_T)^{(2m+2)} - (V_{GS}-V_T-V_{DS})^{(2m+2)}\right) = Y_L(V_{GS}-V_T)^{(2m+2)}. \qquad \textit{Eqn. 5.3-4}$$

Using the circuit diagram, the following voltages could be substituted and the correct values entered. For simplicity, all voltages have been inputted as absolute values to that they are positive. This works on basis of a V_T of 1.6 V.

Table 5.3-2- Equivalent voltage values for saturated load setup

Voltage from Equation	Voltage Equivalent from circuit	Numerical Value
V_{GS}	V_{DD}-V_T	15-1.6 V
V_{GD}	V_{DD}	15 V
V_T	V_T	1.6 V
V_{DS}	V_O	0.1 V

Substituting these values into Eqn. 5.3-4 provides the ratio shown in Eqn. 5.3-7:

$$Y_D\left((V_{DD}-2V_T)^{(2m+2)} - (V_{DD}-2V_T-V_O)^{(2m+2)}\right) = Y_L((V_{DD}-V_T)-V_T)^{(2m+2)} \qquad \textit{Eqn. 5.3-5}$$

$$Y_L = \frac{Y_D\left((V_{DD}-2V_T)^{(2m+2)} - (V_{DD}-2V_T-V_{out})^{(2m+2)}\right)}{((V_{DD}-V_T)-V_T)^{(2m+2)}} \qquad \textit{Eqn. 5.3-6}$$

$$Y_L = 0.0292Y_D. \qquad \textit{Eqn. 5.3-7}$$

This shows that for the TFTs fabricated with the Lisicon™ S1200 at a C_o of 27 nFcm^{-2} and the extracted m of 0.72 from Section 3.7.1, the ratio for Driver:Load should be 1/Y_L. Using 1/0.03 (Y_L to 2 decimal

places) gives a ratio of 33. While this is larger than other inverters in literature, it was found to provide viable simulation results and could be accounted to the mobility of the devices fabricated.

The load was chosen to use the minimum channel length of 20 µm. This due to the minimum feature size, λ_m, being 20 µm which means no patternable dimension can be smaller than this. Using this value, the driver transistor, $T_{D,}$ was chosen to have a *W/L* of 5, hence 100 µm as the *W* value. As the ratio of the two devices must be 33, the *W/L* for the load transistor needed to be 165. Once again using λ_m for the channel length, this needed a *W* dimension of 3300 µm.

The saturated load configuration of the inverter is shown in Figure 5.3-3 including the model file "EAJ" which is the code name for the optimised models from the sample in Chapter 3 and detailed in Section 5.2.1.

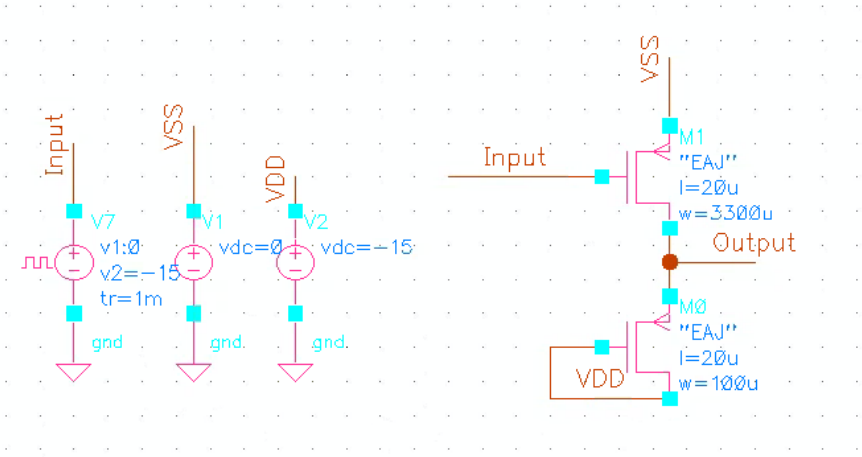

Figure 5.3-3 – Circuit diagram for saturated load inverter with EAJ model files. The applied V_{DD} is -15 V, V_{SS} is 0 V and the input is a variable device which can be pulsed to test the inverter output. The W/L ratios of the load and driver are as calculated in Section 5.3.1.1

The inverter was tested by running dc analysis which produced the output in Figure 5.3-4. The key points on the trace are noted with respect to the different regions of the saturated load from Figure 5.2-3.

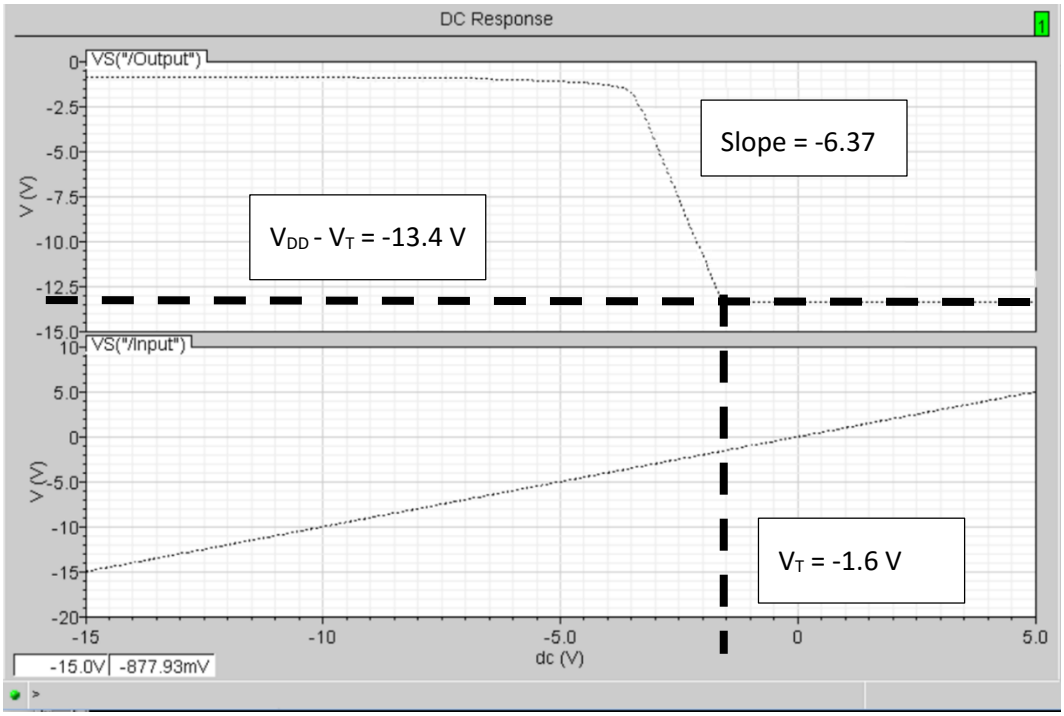

Figure 5.3-4 – DC Characteristics of the saturated load inverter in Figure 5.3-3.

It was clear that the inverter switched at ~-1.6 V (V_T). The slope was 6.37 meaning that if this is $\sqrt{\frac{W_D/L_D}{W_L/L_L}}$ then, as $\frac{W_D/L_D}{W_L/L_L}$=33 and $\sqrt{33}$=5.74, this is only 10% more than the expected, calculated value.

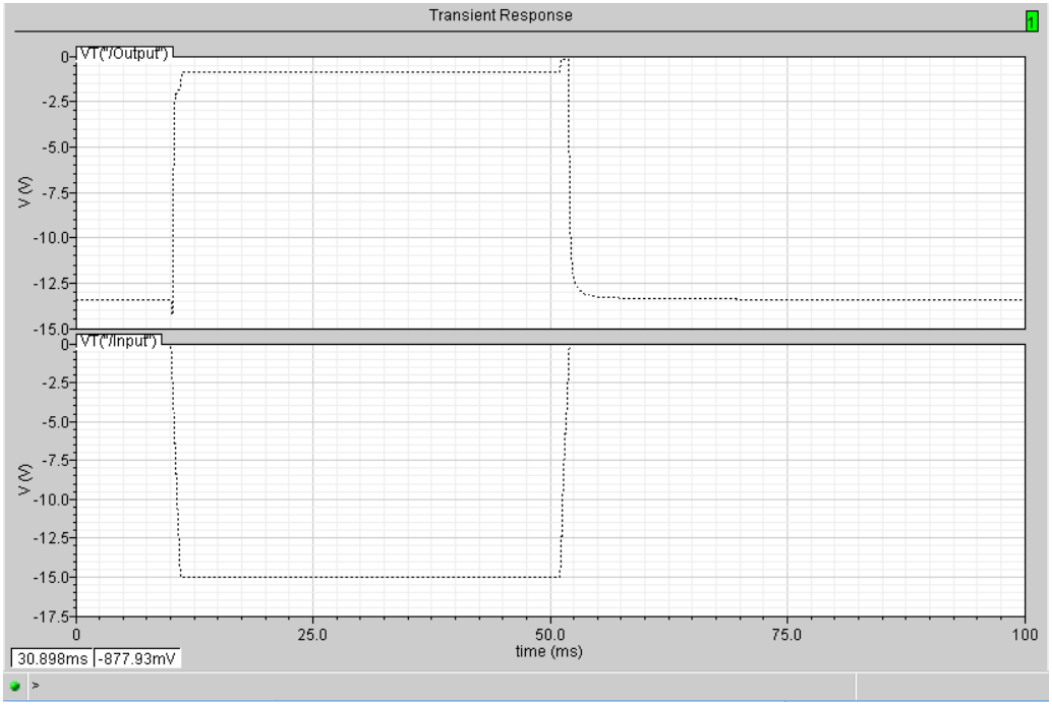

Figure 5.3-5 Transient response of the inverter in Figure 5.3-3. An input signal of -15 V was applied for 40 ms with rise and fall times of 1 ms. The inverter returned an output of -13.38 V with rise and fall times of 0.40 ms and 0.27 ms respectively as detailed in Table 5.3-3.

The transient response is shown in Figure 5.3-5 and shows the inverter function with rise and fall times of 0.40 ms and 0.27 ms respectively. The details of these values including the overshoot and undershoot values are stated in Table 5.3-3.

Table 5.3-3 Extracted values from transient response in Figure 5.3-5.

Rise time	0.40 ms
Fall time	0.27 ms
Overshoot	0.78 V
Undershoot	0.69 V
Min voltage	-0.88 V
Max voltage	-13.38 V

The minimum V_o is within 6% of the total V_{DD} and well below V_T for a second device which means that it is a viable for an off-state. The on-state is -13.38 V which is the expected V_{DD}-V_T for a V_T of -1.6V. The fall and rise times are both under 1 ms with undershoots/overshoots of 0.69/0.78 V respectively. Neither of these differences in voltage would cause any major power loss, or significantly affect any subsequent devices, therefore this inverter model is appropriate for usage.

5.3.2 Pseudo-CMOS Inverter

A design for a pseudo-CMOS inverter was proposed by Huang *et al.*[8] as a comparable configuration to CMOS with benefits of robust tunability and claiming a similar performance to CMOS technology. The structure is essentially two inverters side by side with the output of the first controlling the second. The two driver gates are controlled by the same input but the gate of the second load transistor is controlled by the inverted input. This means that, as with a CMOS inverter, the two transistors will always be switched on inversely. As with the saturated load inverter, the circuit for the pseudo-CMOS inverter was built as shown in Figure 5.3-6 and the same dc analysis performed as detailed in Figure 5.3-7.

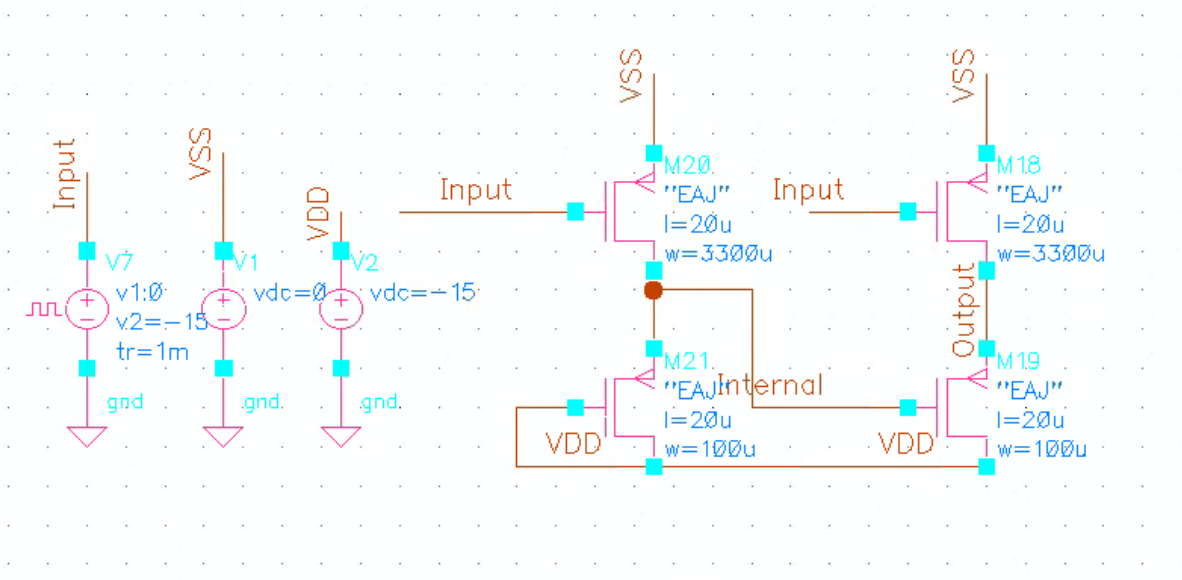

Figure 5.3-6 Circuit diagram for pseudo-CMOS inverter with EAJ model files. The applied V_{DD} is -15 V, V_{SS} is 0 V and the input is a variable device which can be pulsed to test the inverter output. As the design is based on the saturated load inverter, The W/L ratios were kept as calculated in Section 5.3.1.1

This combination of 2 inverters means that the load of the second inverter is not permanently saturated, in fact it is working inversely to the input and therefore will have a slightly different DC response from the first inverter.

Table 5.3-4 - Descriptions for load and driver states of the 3 regions in Figure 5.3-2 but for both the internal and output inverter of the pseudo-CMOS configuration. The current regions of the driver transistor for the output inverter depends on the output of the load of the internal inverter.

	Region	V_{in} / V_T	V_O / V_{in}	Driver	Load	Output
Internal	1	$V_{in} < V_T$	$V_O > V_{in}$	Off	On (Sat)	High
	2	$V_{in} > V_T$	$V_O > V_{in}$	On (Sat)	On (Sat)	Switching
	3	$V_{in} > V_T$	$V_O < V_{in}$	On (Lin)	On (Sat)	Low
Output	1	$V_{in} < V_T$	$V_O > V_{in}$	Off	On (Sat)	High
	2	$V_{in} > V_T$	$V_O > V_{in}$	On (Sat)	On (Lin)	Switching
	3	$V_{in} > V_T$	$V_O < V_{in}$	On (Lin)	Off	Low

Table 5.3-4 show the state settings for the internal and the output inverter, similar to that of Table 5.3-1, but with an extra set of values. The main difference is the region of operation of the load

transistor for the output inverter. As this is being controlled by the output of the internal, it simulates the same push-pull mechanism as CMOS.

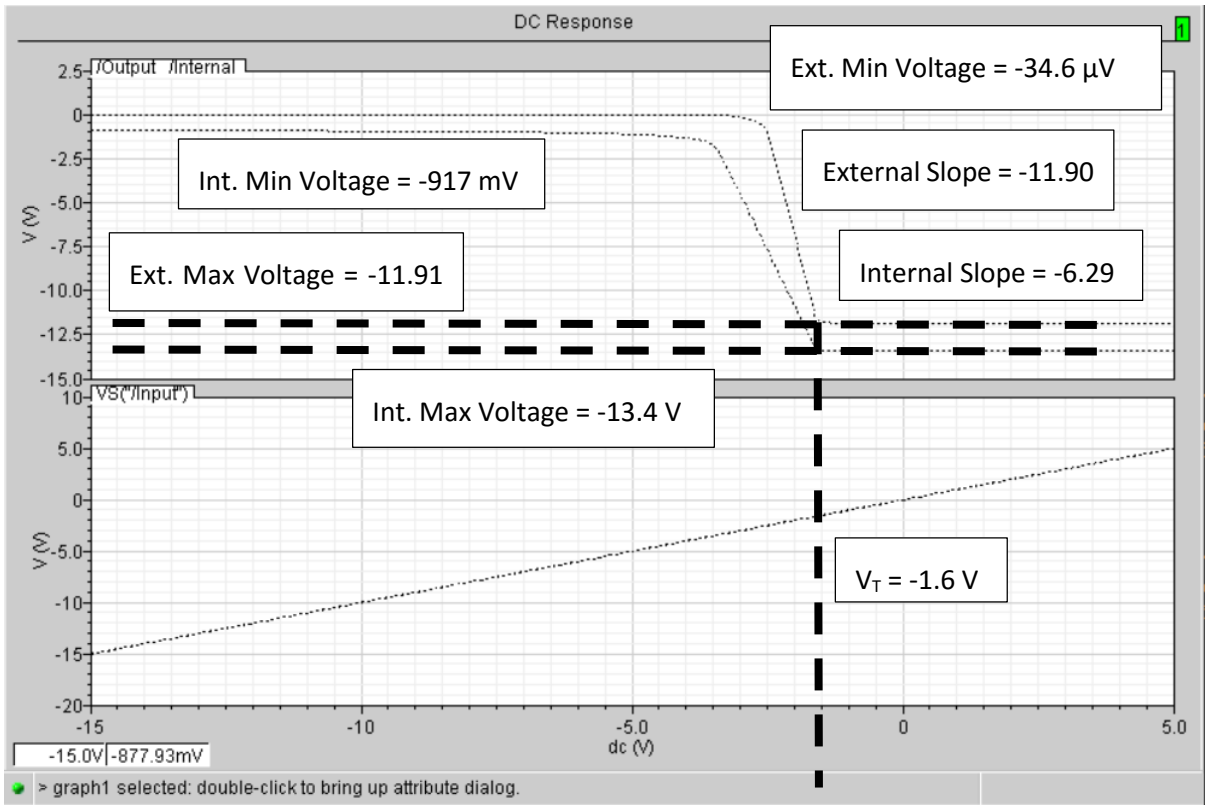

Figure 5.3-7 - DC response for pseudo-CMOS inverter with the extracted values for the slope, V_T and voltage values for both the output and internal inverters.

The slope of the output in this configuration is much steeper at 11.90, almost double the slope of the internal inverter, which (as expected) is the same as the saturated load inverter with a ratio of 6.29. In comparison to the saturated load configuration, the voltage swing is the same however the saturated load suffered the offset. This is probably due to the source and drain being connected, a factor which is not relevant when only considering the output for the second inverter in this case.

The transient response for this setup can be taken at both the internal node and at the output Figure 5.3-8 shows the response and the numerical values are in Table 5.3-5 alongside those featured in Table 5.3-3 for the saturated load inverter.

It can be seen from these results that while the internal inverter has very similar characteristics to the saturated load, the additional inverter has a slower fall time due to the extra stage. It does, however, yield a minimum voltage much closer to 0 as the V_T is not wasted in the permanent saturation.

Table 5.3-5 – Extracted values for the rise and fall times, under/overshoots and the voltage levels of the pseudo-CMOS inverters compared to those extracted for the saturated load.

	Pseudo Internal	Pseudo Output	Saturated Load
Rise time	0.38 ms	0.59 ms	0.40 ms
Fall time	0.17 ms	0.35 ms	0.27 ms
Overshoot	0.82 V	0.93 V	0.78 V
Undershoot	0.59 V	0.34 µV	0.69 V
Min voltage	-0.88 V	-0.33 µV	-0.88 V
Max voltage	-13.40 V	-11.89 V	-13.38 V

Conversely to this, the disadvantage is the extra loss of output voltage governed by the two V_Ts that are needed to hold the output high.

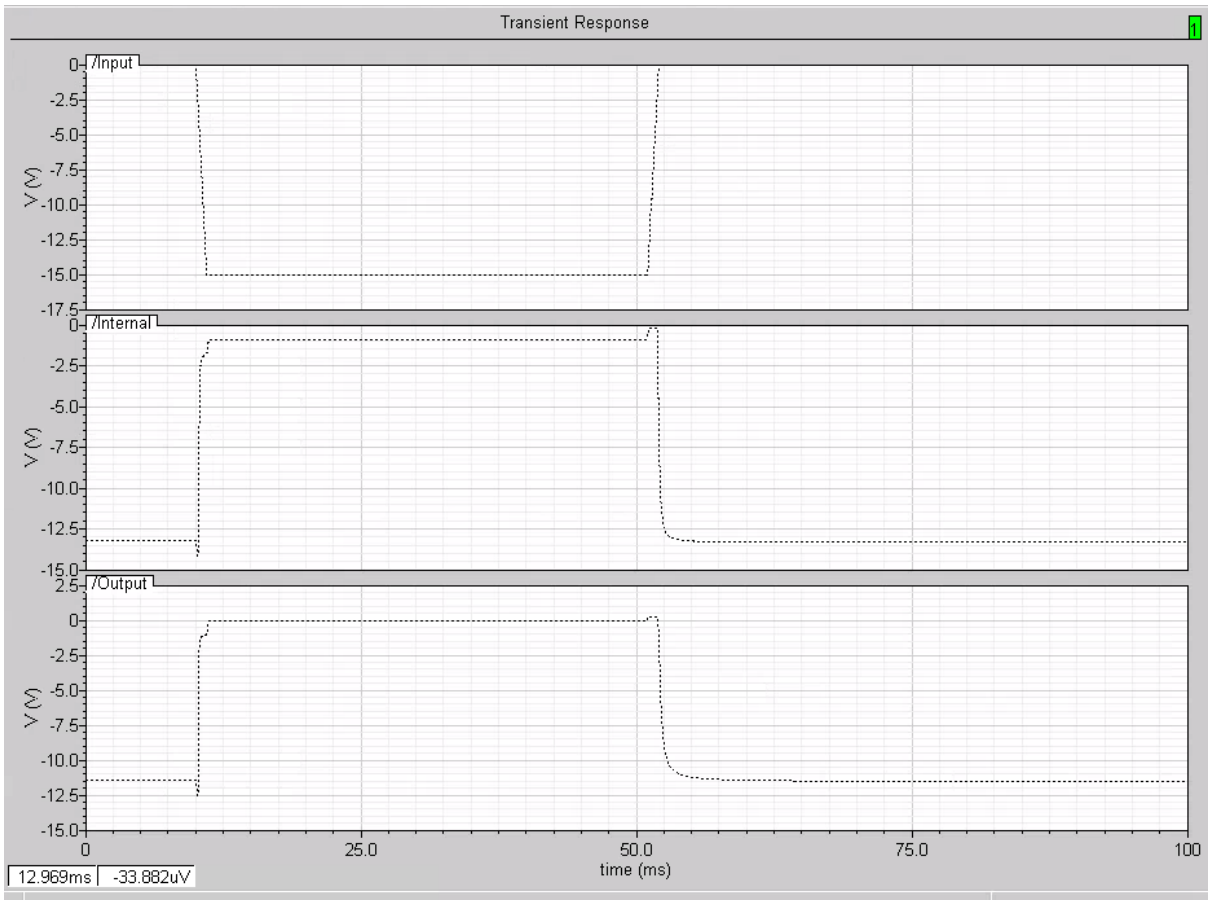

Figure 5.3-8 – Transient response of the pseudo-CMOS inverter that the values in Table 5.3-5 represent.

5.4 Load Capacitance

In an ideal case for a TFT, there would be no capacitance associated with either the source or drain contacts, this is desired due to the limiting effects of overlap capacitance on switching speed[10]. It is possible[11] to reduce these internal capacitances using a self-aligned or auto-registered gate which reduces the error compensation needed when designing the layout. The Lisicon™ S1200 was tested with a self-aligned TFT structure. The polymer was deposited onto an existing self-aligned TFT inverter circuit fabricated previously by another group member and measured with an $I_{DS}V_{GS}$ sweep from 10 V to -10 V with a V_D of -10 V.

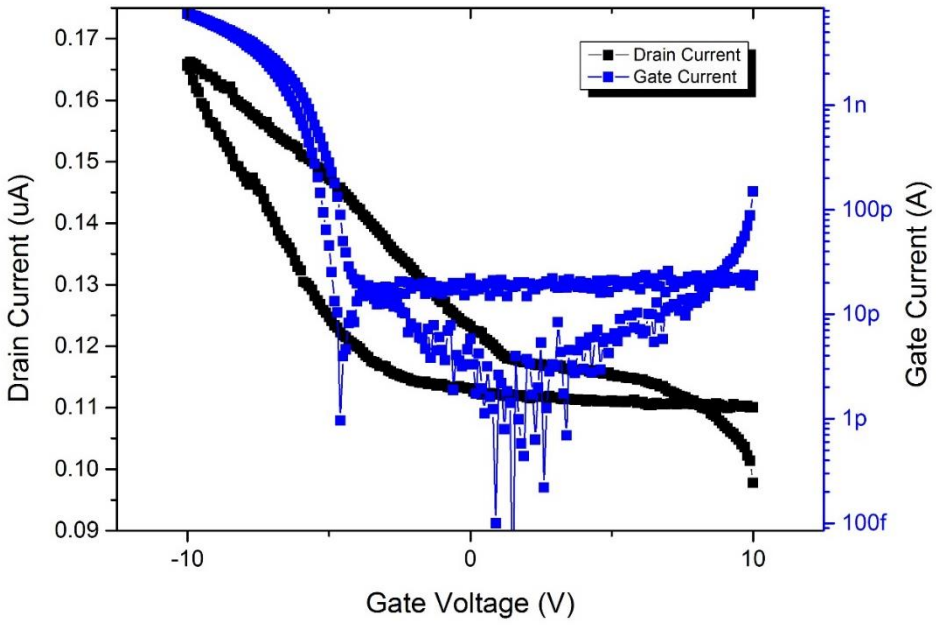

Figure 5.4-1- Transfer characteristic for TFT measured on Self-aligned structure with Lisicon™ S1200 Semiconductor deposited

As can be seen from the low current values of Figure 5.4-1, the transistor failed to turn on, however there was evidence that the device was working at some level. A gate current was present and exhibited consistent behaviour with the lone device transistors and showed an increase of about 3 orders of magnitude. The drain current, however, failed to exhibit either an on or off-state. It flowed at a current of approximately 0.1 µA which is too high for a successful transistor and increased less than an order of magnitude. This was an indication that the current self-aligned processing used within the research group was not compatible with the Lisicon™ S1200 polymer and therefore internal capacitances need to be considered.

The non-self-aligned structure used in this project with the internal capacitances are noted in Figure 5.4-2.

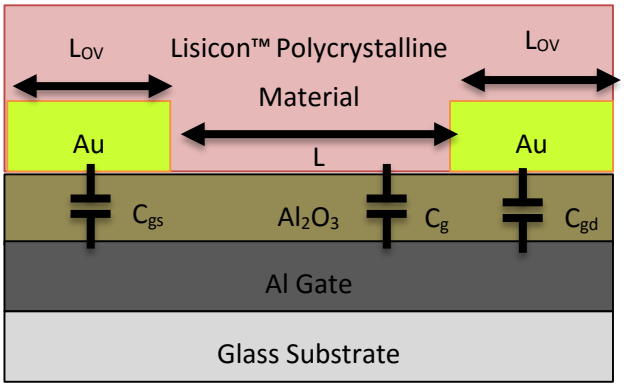

Figure 5.4-2 – Structure of OTFT with positioning of the internal capacitances C_{gs}, C_{gd} and C_g and the channel and overlap lengths L and L_{ov} respectively.

While capacitances within the simulation are accounted for within the models, an approximation for a load capacitance can be obtained by a summation of the capacitance of the load determined by the gate and the drain, the gate and the source and the capacitance of the gate itself. This is not an accurate reflection for the intrinsic or parasitic capacitances, however on the assumption that one inverter will likely be driving a second (as is the case with the shift registers), this approximation can be used to emulate the load on the output. This analysis is also useful to estimate a reasonable fall time for the simulation traces and allows for some general layout design practices to be considered to reduce unnecessary capacitance loss.

The main capacitances can be calculated using the area of the device where there is an electromagnetic field, and therefore a capacitance, across the gate oxide. For a self-aligned transistor, the fabrication process reduces the overlap of anything other than the channel with the gate oxide whereas for the photolithography method discussed in Section 3.5.1, the gate oxide is present for the entire area of the source and drain contacts. This is not desirable as it causes unnecessary capacitances. As the self-aligned process failed to work for the materials within this project, it is a necessary disadvantage until circuits can be optimised to work with self-aligned circuitry. It is also worth noting that this is where patternable dielectrics could have benefit as introduced in Section 3.5.2. This will be discussed in Chapter 6.

Based on the layout that will be detailed in Section 5.6, the following expressions were developed in terms of the oxide capacitance per unit area, C_o, and the device areas.

Gate - Drain Capacitance C_{ds}

The gold contact has a length of the minimum feature size, λ_m, as this is one of the design rules for circuit fabrication (see Section 5.6 Step 5).

This can be approximated to the channel length, assuming that the channel length will generally be the minimum feature size.

Although the circuit design within this project is based upon the photolithography process technique, one feature that was optimised based on the comparison of the two fabrication techniques in Chapter 2 is the slot like shape of devices as shown in Figure 5.4-3.

Figure 5.4-3 – Shape of the transistor used in mask designs for transistors. The slot-like shape is to reduce unnecessary capacitances and packing density for large W/L ratios.

This was originally done with the shadow mask technique, but as this can be done within the design rules, it can be used within the design. This not only is better for packing density, but it removes the problems suffered with characterisation that was mentioned in Section 4.4.2. If the devices can be measured using bond pads, away from the gate oxide, pressure is not applied directly to the oxide and the device is less likely to break down. This has major benefits based on the analysis in Chapter 4 regarding the practical issues with scaling.

Another benefit of this is to combat the phenomenon of the Miller capacitance. This is caused by the double swing of the drain switching on as the gate is being pulled low, effectively doubling the capacitance. If the slot like shape is used then the width of the channel takes up half as much space on the device, improving packing density and capacitance waste. The source contact is effectively wrapped around the drain and therefore the length of the drain contact is halved as current can flow to the source on two sides instead of just one. This is more efficient than the case of a parallel contact configuration where the width of the channel would have to equal the width dimension of the whole device. This half factor cancels out the Miller capacitance and C_{gd} is found as in Eqn. 5.4-1.

$$C_{gd} = C_o \frac{2W}{2} \lambda = C_o W \lambda \qquad \textit{Eqn. 5.4-1}$$

Gate – Source Capacitance C_{gs}

The expression for C_{gs} works under the same principal as C_{gd} regarding the dimensions, although there is no Miller capacitance. As this factor of 2 is not present, the source is chosen to be the u-shaped section of the transistor configuration. This equates the two capacitances and it can be assumed that $C_{gs} = C_{gd}$.

$$C_{gs} = C_o W \lambda \qquad \textit{Eqn. 5.4-2}$$

Gate Capacitance C_g

The gate capacitance in the linear regime is simply the capacitance of the total channel area.

$$C_{glin} = C_0 W L \qquad \textit{Eqn. 5.4-3}$$

For the saturated region it follows the form from

$$C_{glin} = \frac{C_0 2WL}{3} \qquad \textit{Eqn. 5.4-4}$$

Combining these expressions and assuming that $\lambda_m = L$ produces the approximate C_L values in in Eqn. 5.4-5 and Eqn. 5.4-8:

$$C_{L\_lin} = C_0 WL + 2C_0 WL = 3C_0 W_L L \qquad \textit{Eqn. 5.4-5}$$

$$C_{L\_sat} = \frac{C_0 2WL}{3} + 2C_0 WL \qquad \textit{Eqn. 5.4-6}$$

$$C_{L\_sat} = \frac{C_0 2WL + 6C_0 WL}{3} \qquad \textit{Eqn. 5.4-7}$$

$$C_{L\_sat} = \frac{8C_0 WL}{3}. \qquad \textit{Eqn. 5.4-8}$$

If it can be assumed that $\lambda_m = L$ = 20 µm, W_D = 3300 µm and C_o = 245 x10^{-3} Fm^{-2} then based on the parameters in the designed circuit. If this C_L is calculated for both transistors in the inverter then they

can be combined to find the total approximation across the inverter. This is obtained by substituting in the appropriate *W* and *L* values for each device.

$$C_{LT\_lin} = 3C_0W_LL + 3C_0W_DL = 49.98\,nF. \qquad \textit{Eqn. 5.4-9}$$

$$C_{LT\_sat} = \frac{8C_0W_LL}{3} + \frac{8C_0W_DL}{3} = 44.43\,nF. \qquad \textit{Eqn. 5.4-10}$$

This capacitance can also be used to estimate the rise/fall times needed, specific to the new derivation of the equation.

With the saturated load configuration, a charge, *Q*, can be equated to the voltage applied to the gate of the load, V_{GS}, multiplied by the capacitance C_L.

$$Q = C_LV_{GS} = C_LV_{in} \qquad \textit{Eqn. 5.4-11}$$

The discharge current is therefore the rate of this charge over time and is shown in Eqn. 5.4-11.

$$I = -\frac{dQ}{dt} = -C_L\frac{dV_{in}}{dt} \qquad \textit{Eqn. 5.4-12}$$

Applying this to the disordered equation, the expression in Eqn. 5.4-13 can be deduced.

$$-C_L\frac{dV_{in}}{dt} = \frac{W}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(-\frac{(V_G - V_T)^{(2m+2)}}{2(m+1)(2m+1)}\right) \qquad \textit{Eqn. 5.4-13}$$

If the C_L term can be applied (assuming only one device as when discharging, the current will only be passing through the driver circuit and therefore saturated) and V_D can be assumed to be negligible due to $V_G - V_T > V_D$, then

$$\frac{8}{3}C_O\cancel{W}L\frac{dV_{in}}{dt} = \frac{\cancel{W}}{L}\frac{KC_0{}^{2m+1}}{\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(\frac{(V_G - V_T)^{(2m+2)}}{2(m+1)(2m+1)}\right). \qquad \textit{Eqn. 5.4-14}$$

The *W* term is cancelled, V_G replaced with V_{in} and the C_O terms combined to obtain a form that can be integrated to isolate the fall time.

$$\frac{dV_{in}}{dt} = \frac{8}{3}\frac{KC_0{}^{2m}}{L^2\{2kT_C\varepsilon_0\varepsilon_S\}^m}\left(\frac{(V_{in}-V_T)^{(2m+2)}}{2(m+1)(2m+1)}\right). \quad \textit{Eqn. 5.4-15}$$

$$\int_0^{V_{DD}} \frac{dV_{in}}{(V_{in}-V_T)^{(2m+2)}} = \int_0^{t_f}\left(\frac{8}{3}\frac{KC_0{}^{2m}}{L^2\{2kT_C\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)}\right)dt. \quad \textit{Eqn. 5.4-16}$$

$$\frac{1}{(2m+1)(V_{GS}-V_T)^{(2m+1)}} = t_f\frac{8}{3}\frac{KC_0{}^{2m}}{L^2\{2kT_C\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)} \quad \textit{Eqn. 5.4-17}$$

The fall time is then found in the expression in Eqn. 5.4-18 and the fall time can be found for the design parameters in this circuit using a Matlab program.

$$\frac{8}{3}\frac{L^2\{2kT_C\varepsilon_0\varepsilon_S\}^m 2(m+1)(2m+1)}{KC_0{}^{2m}(2m+1)(V_{GS}-V_T)^{(2m+1)}} = t_f \quad \textit{Eqn. 5.4-18}$$

The value returned was 150.56 µs which is within the same order of magnitude as the fall times for the internal inverter of the pseudo-CMOS inverter at 170 µs and the saturated load inverter at 270 µs.

5.5 Dynamic Shift Register

5.5.1 Dynamic Logic and Shift Register Theory

Dynamic logic has been used for memory devices[4] and row column drivers[5] allowing the circuit to store the memory of a signal. The diagram in Figure 5.5-1 shows a pass transistor as a gate input to a second transistor.

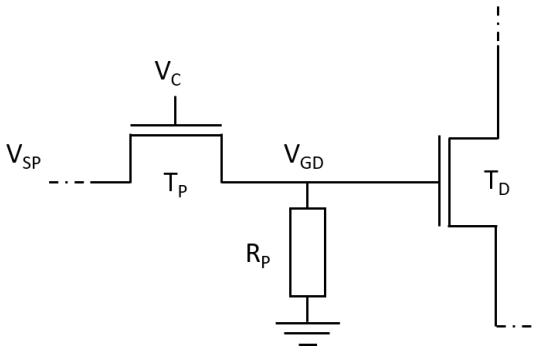

Figure 5.5-1 – Diagram of pass transistor, T_P, feeding into driver T_D. There is a resistor R_P to hold the voltage at the gate input to T_D. The voltages V_{SP} and V_{GD} are labelled to indicate the potentials at either side of T_P. A clock pulse V_C is applied to the gate of T_P.

When a voltage, V_C, is applied to the gate of the pass transistor, T_P, it is switched on and the I_{DS} current is able to flow. The voltage at the source of T_P, V_{SP}, is now passed to V_{GD} – the gate voltage of transistor T_D. This is facilitated by the source – drain flow and therefore will remain there as a voltage across a pass resistor, R_P, or a charge across a load capacitor, C_L. If the transistor T_D is part of a wider circuit then the current producing V_{GD} can be used to essentially record a former input. An example of this is shown in Figure 5.5-2.

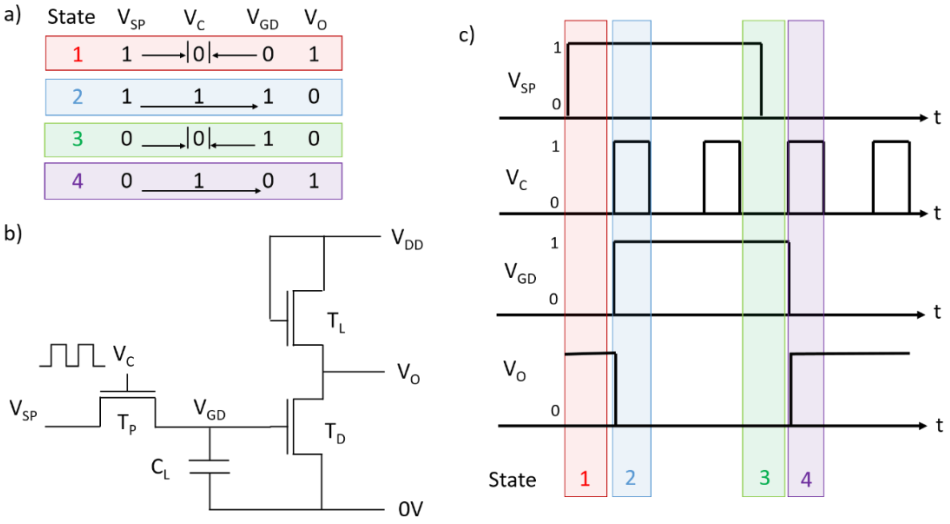

Figure 5.5-2 –a) States of voltages V_{SP}, V_C, V_{GD} and the resultant output voltage V_O. The arrows indicated the passing or blocking of charge depending on V_C. b) Circuit diagram of pass transistor T_P as an input to a saturated load inverter with load and driver T_L and T_D respectively. c) The timing diagram of the 4 voltages with a corresponding state number of 1-4 detailed in a).

In this setup, Figure 5.5-1 as an input to an inverter circuit (b) with a timing diagram (c) and table of states (a). Here T_D is driving a saturated load inverter load transistor, T_L, to produce an output voltage, V_O. The functionality of this form of inverter is explained in Section 5.3.1 but, for the purpose of this

diagram, only the inverting behaviour is relevant. The pass transistor voltage, V_{SP}, is stored on a capacitor C_L.

The 4 distinctive points in the operation, States 1-4 are highlighted across (a) and (c) and show the following situations:

1. As V_C has not been clocked, the voltage V_{SP} is not connected to V_{GD} so the input to T_D remains low. V_O is high as it is an inverted form of $V_{DP.}$
2. V_C is now clocked and V_{SP} allows V_{GD} to get to voltage V_C - V_T (high), charging C_L and clocking the inverter to switch V_o low.
3. V_{SP} switches low but, as V_C is also low, charge is trapped at V_{GD} and is unable to discharge maintaining the state of V_{DP} and therefore V_O also remains unchanged.
4. The low state of V_{SP} is clocked through to V_{DP} and C_L discharges, switching the inverter high.

The current can be expressed as the rate of change of charge over time. This can be represented in terms of capacitance and voltage and produce Eqn. 5.5-1. If considered in terms of a resistance R_P across the pass transistor then Eqn. 5.5-2 can also be stated.

$$I = \frac{dQ}{dt} = C\frac{dV_{GD}}{dt} \qquad \textit{Eqn. 5.5-1}$$

$$I = \frac{V_{SP} - V_{GD}}{R_P} \qquad \textit{Eqn. 5.5-2}$$

$$\frac{V_{SP} - V_{GD}}{R_P} = C\frac{dV_{GD}}{dt} \qquad \textit{Eqn. 5.5-3}$$

Their combined form in Eqn. 5.5-3 can then be used to isolate the theoretical charge and discharge times and used for circuit design parameters.

$$\int_0^t dt = R_P C \int_0^{V_{DP}} \frac{dV_{GD}}{V_{SP} - V_{GD}} \qquad \textit{Eqn. 5.5-4}$$

$$V_{SP}\left\{1 - \exp\left(-\frac{t}{R_P C}\right)\right\} = V_{DP} \qquad \textit{Eqn. 5.5-5}$$

Of course, in terms of fabrication, there would be a limit on controlling oxide thicknesses across the circuit but it would be considered when deciding upon best thickness to use overall.

The principal function of a shift register is to pass a signal across various outputs, each controlled by the output of the last. The dynamic shift register utilises the benefits of being able to store and control charges using pass transistors and a clocking sequence. There are various reasons why dynamic circuitry can be beneficial compared to static circuitry, although there are advantages to both forms [6]. The equivalent static design would use flip flops connected to a clocking mechanism. Dynamic technology offers an alternative system whereby they are not always active, although dynamic designs have a limit on the minimum speed as the charge at the node eventually discharges due to the constant path to ground. The circuit contains fewer devices though, and therefore is more efficient in both power and packing density.

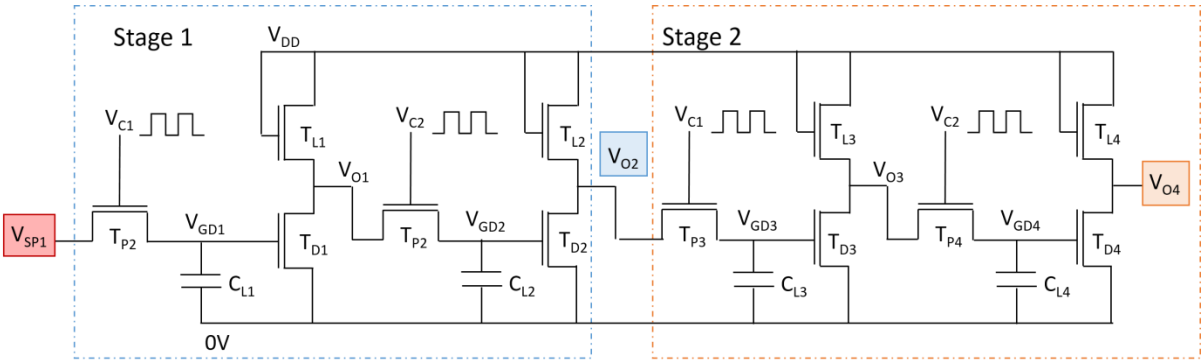

Figure 5.5-3 – Circuit for a 2 stage shift register designed with saturated load transistors and the dynamic pass transistor setup shown in Figure 5.5-2. 4 of these are attached together with the V_o and V_{GD} voltages labelled 1-4 to reflect each set of inverters. There are two clock pulses V_{C1} and V_{C2} which control alternate dynamic inputs to operate the shift register.

The circuit shown in Figure 5.5-3 is a further expansion of the setup explored in Figure 5.5-2 and works as a shift register. It is formed into stages by connecting V_O, re-labelled as V_{O1} to clarify its position in the circuit, to the input a second pass transistor, T_{P2}. All voltages and components have been re-labelled with a numerical subscript reflecting their position in the circuit. The two stages, 1 and 2, comprise of a set of the pass transistor/inverter setup also with the addition of a second clock pulse, V_{C2} to facilitate the control of the extra components.

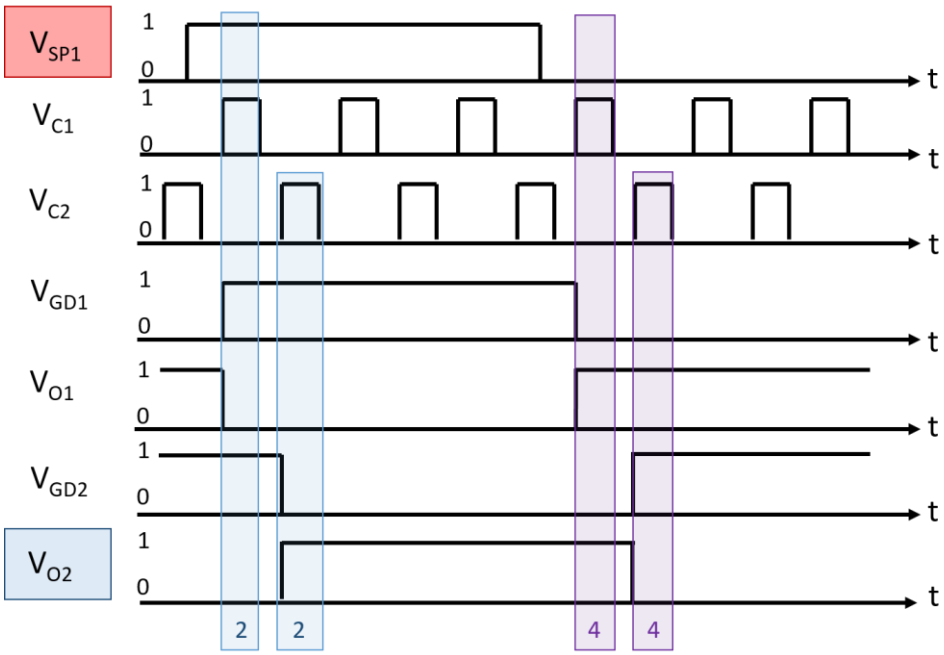

Figure 5.5-4 – Timing diagram for Stage 1 of the shift register with highlighted states 2 and 4 to relate it to the states in Figure 5.5-2 showing the charge of the pass transistor either being passed or saved. These states are shown for both V_{C1} and V_{C2} showing how the passing of the signal works with 2 clock pulses. The initial input V_{SP1} and output of Stage 1 V_{O2} are highlighted to correspond to their position on Figure 5.5-3.

Part of the timing diagram for the dynamic shift register can be seen in Figure 5.5-4. This shows the output for Stage 1 of the circuit as indicated by each of the gate drain voltages, V_{GD1} and V_{GD2}, and the two outputs V_{O1} and V_{O2}. V_{O1} is now the V_{SP1} equivalent of T_{P2}. The highlighted timing sections correspond to the State 2 and 4 of Figure 5.5-2 when either V_{C1} or V_{C2} switches on the gate of T_{P1} and T_{P2} respectively allowing the voltage V_{SP1} or V_{O1} to pass through.

The two inputs can transfer charge at a staggered timing rather than an instantaneous switch. This is an example of how dynamic design can maintain tight control over the timings of the signal passing and it is therefore important that the clock pulses of the inputs do not coincide. It is clear from the timing diagram that the input voltage at V_{SP1} has been passed on to V_{O2} with a short time delay caused by the time it takes for the signal to be inverted and pass through. By applying this same principle, more stages can be added, each working in the same way, but using the input of the previous. Figure 5.5-5 shows the timing diagram of the Two Stage circuit in Figure 5.5-3 but only containing the output of each inverter and omitting the intermediate pass transistor stage.

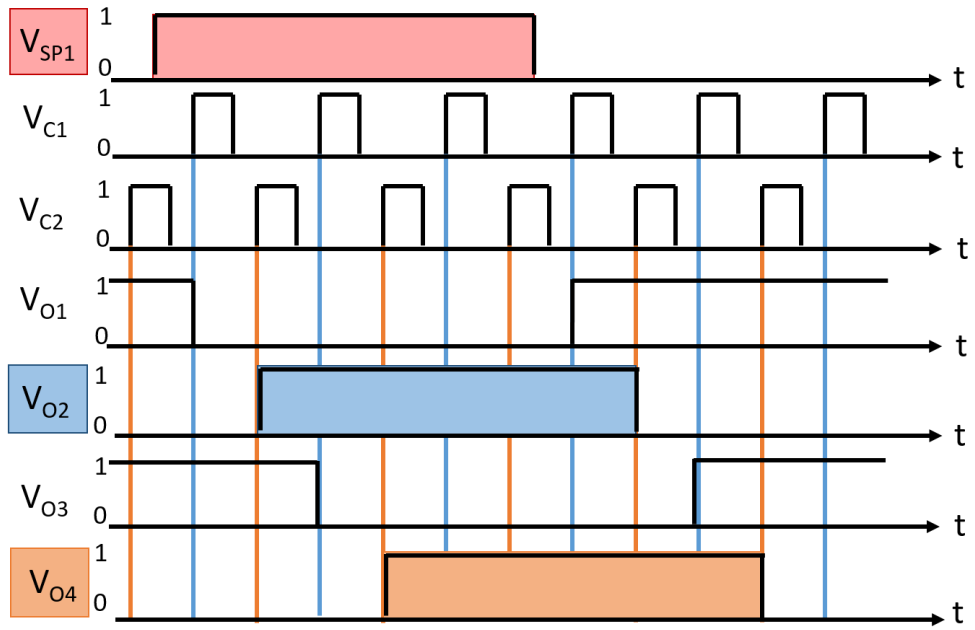

Figure 5.5-5 – Timing diagram for both outputs of stages 1 and 2 highlighted by the blue and orange highlighted areas. The outputs of V_{O2} and V_{O4} are seen to be the same voltage state and width of the original signal but occur at least 2 periods later. The timing diagram breakdown for Stage 2 is not featured, but this is the same as that for Stage 1.

This process continues with each sequence of clocking and it can be seen from the diagrams that it is successful in transferring the signal while keeping it in time. Two inverters are needed per stage in order to obtain the correct polarity of signal, but it is evident that charge is passed along each stage.

5.5.2 Dynamic Pass Transistor Simulation

Before devising circuits for the shift register designs, a dynamic pass transistor was needed. In order to check that the simulations would behave as desired, preliminary tests were done to test only the function of a pass transistor during the pre-charge and charge phase. Figure 5.5-6 shows a simple pass transistor input into a saturated load inverter, similar to that explored theoretically in Figure 5.2-3.

The saturated load inverter values are the same as those in 5.3.1.1 and the pass transistor ratio was chosen iteratively based around a minimum ratio, at first $W = L = 20$ µm but then increased slowly in increments of 20 µm until the result produced an output reasonable rise and fall times.

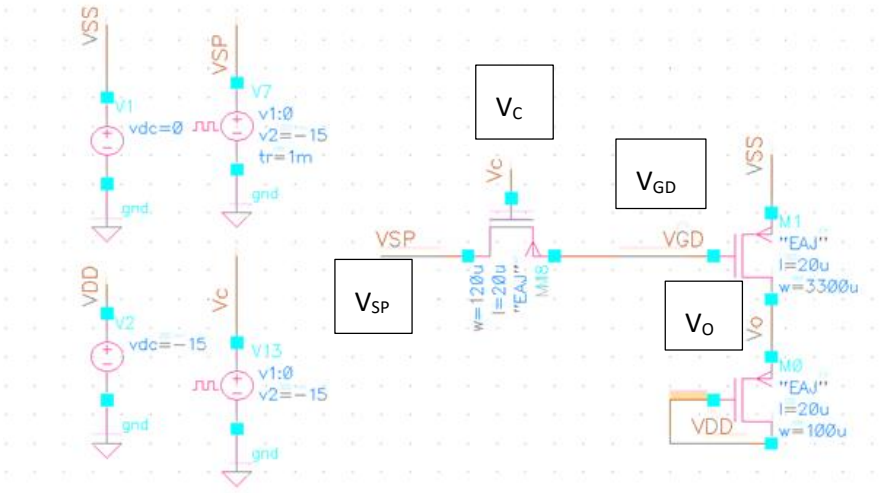

Figure 5.5-6 – Circuit diagram of dynamic pass transistor setup with marked voltages V_C, V_{SP}, V_{GD} and V_O. This is a simulation circuit based on the design in Figure 5.5-2. An input signal of voltage -15 V and width 40 ms is applied the pass transistor. The dynamic clock is a pulse of 0 to -15 V with a width of 5 ms.

As explored in Figure 5.2-4, the pass transistor should only allow the charge at the input of the inverter to charge and discharge when a clock pulse is applied. A transient response was run for the circuit over a time period of 100 ms with a 1 ms clock pulse every 30 ms. The output is shown in Figure 5.5-7.

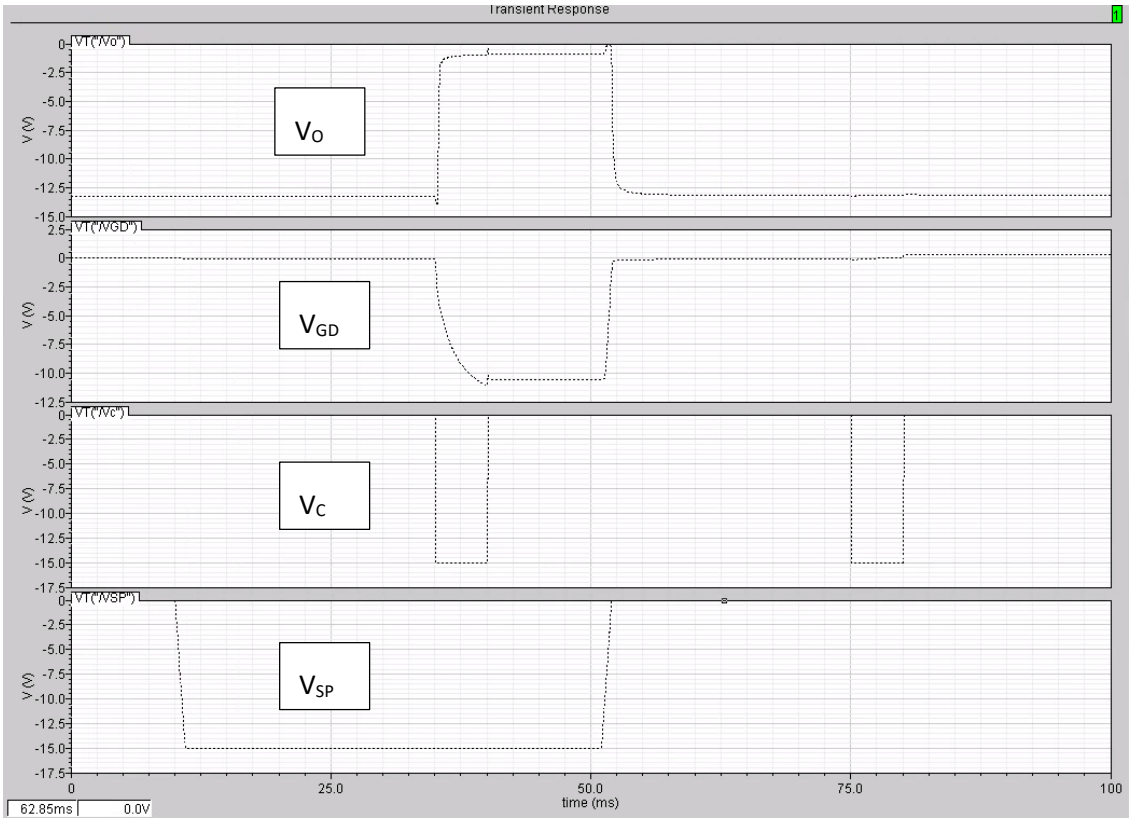

Figure 5.5-7 Transient response of the circuit in Figure 5.5-6. The four voltages V_C, V_{SP}, V_{GD} and V_O are plotted. It can be seen that the pass transistor succeeds in only passing the high signal when it is clocked, but the charge is lost as soon as the input signal goes low.

The traces are labelled with the same labels as Figure 5.3-2 for clarity. It is clear from the switching of V_{GD} that the pass transistor does not allow the high signal of V_{SP} to pass through until the clock pulse of V_C, however the charge was immediately lost when V_{SP} went low. This setup therefore did not function as a pass transistor and more investigation was needed.

It was found that one of the properties of the transistor was the bulk node tie. This was allocated to the source and is necessary for the Cadence models with the absence of a substrate tie.

As one of the functions of the pass transistor is that the source switches side depending on whether the V_{GD} or V_{SP} is at the higher potential, this solid tying of the source meant that the pass transistor could only function in one direction. This was proven by simulating the same circuit but with the bulk node now tied to the drain. As expected, this produced the opposite phenomenon; the charge on the output immediately went high in line with the pulse at V_{SP} but it switched low only when V_C went high after V_{SP} was once again low.

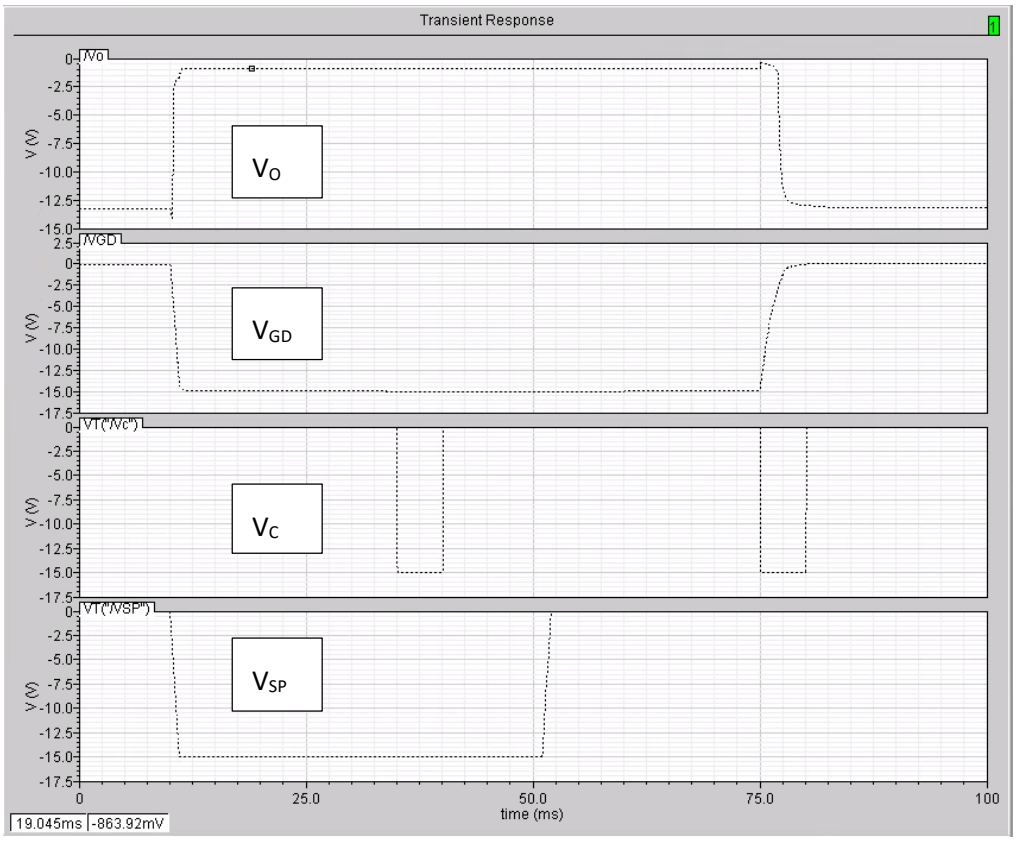

Figure 5.5-8 – Transient response of pass transistor and inverter setup but with the bulk node tied to drain. It shows the output signal holding the passed charge until a clock pulse but the signal is passed as soon as the input goes high.

As it was not possible to alter the transistor properties to allow a variable source/drain, the solution

implemented was to place two pass transistors in series; one had the bulk node attached to the drain and one attached to the source. This is shown in Figure 5.5-9.

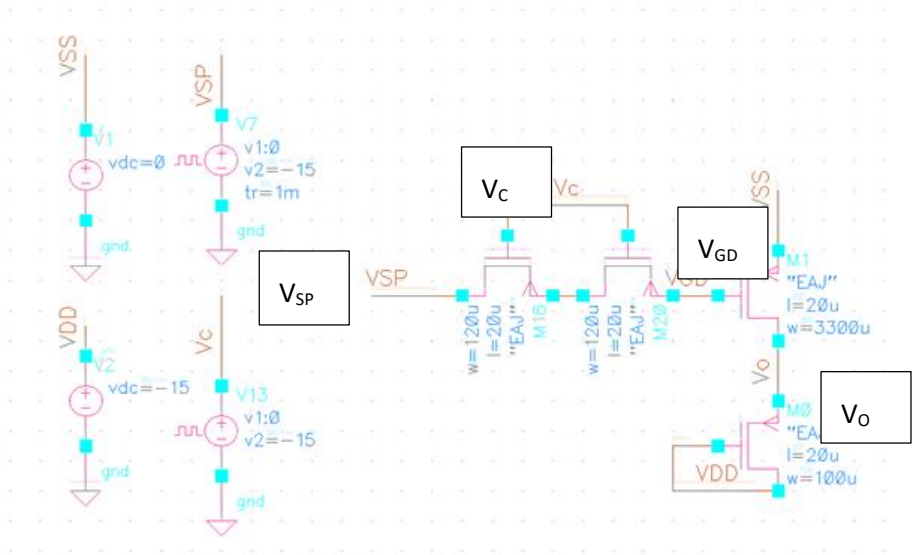

Figure 5.5-9 – Adapted circuit diagram of Figure 5.5-6 to include a second pass transistor in order to combat the source/drain tie that is necessary for the Cadence simulation.

This method proved successful, as demonstrated in Figure 5.5-10. It is clear from this trace that the output both charges and discharges in time with the clock pulse as desired and the width of the pulse is maintained.

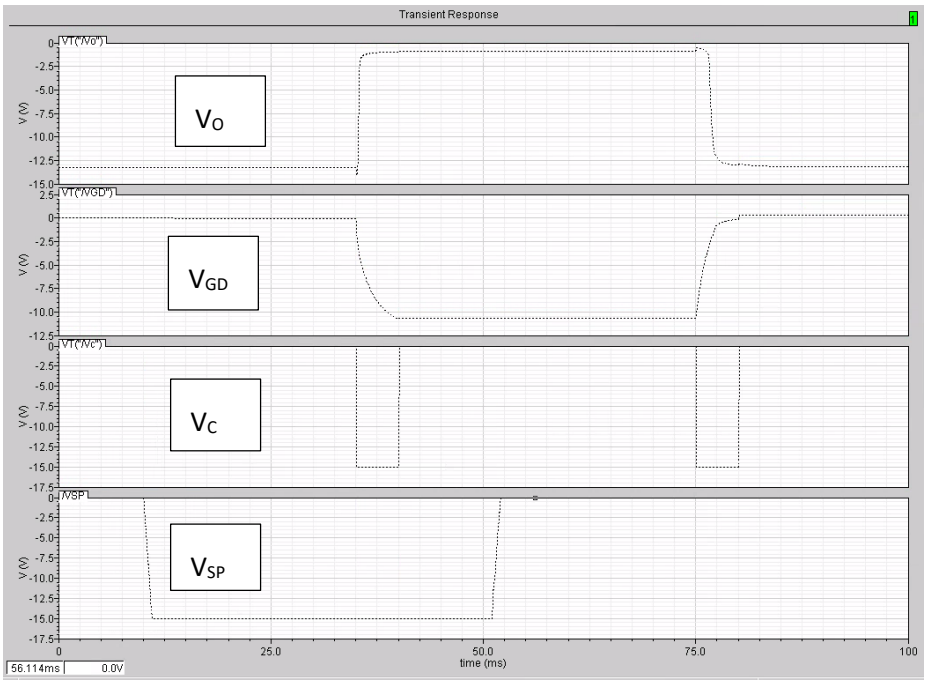

Figure 5.5-10 – Transient response of Figure 5.5-9 showing that the double pass transistor setup functions as desired. The signal is only passed on the clock pulse and holds the charge until the first clock after the input signal has gone low.

One thing that was evident from the additional pass transistor was that the rise and fall time of the output increased. This was due to the capacitance of the extra transistor. The pulse width of the clock must take this charge time into account and will need to be calculated carefully for the shift register design.

5.5.3 Saturated Load Shift Register Simulation

Figure 5.5-11 shows a 2-stage Saturated Load shift register simulated with the EAJ organics model in Cadence software. This was simulated over a timescale of 200 ms. Initially the clock pulses were set at 5 ms as a reasonable fall time greater than that calculated in 5.4, however it was found that a longer time was needed, possibly due to the second pass transistor.

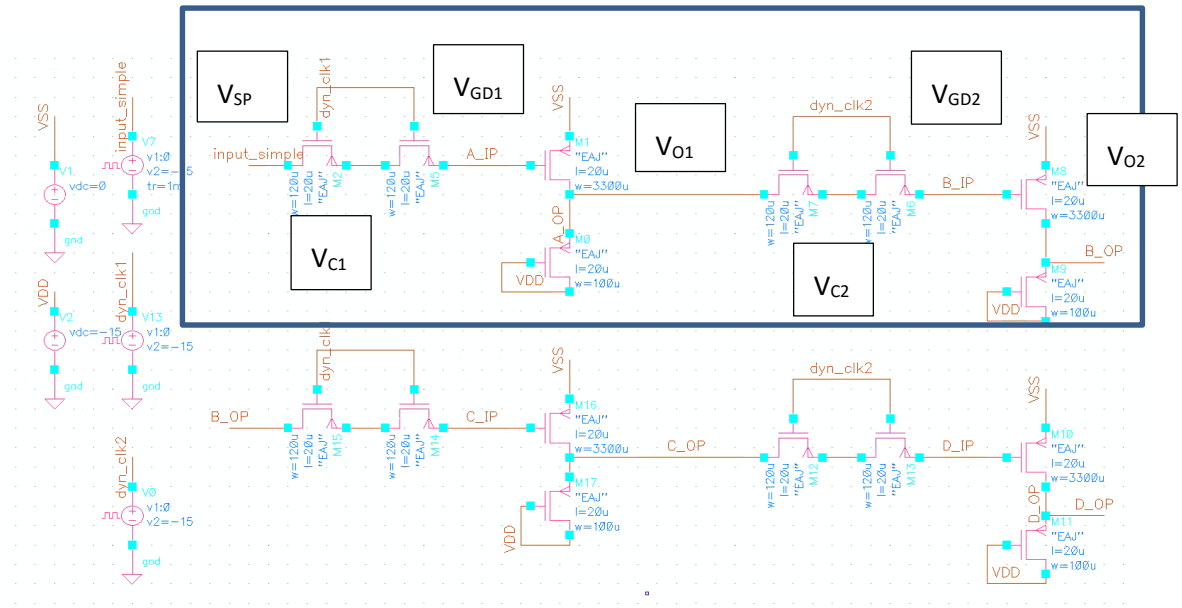

Figure 5.5-11 Circuit diagram of saturated load shift register with double pass transistor input and the models and ratios as designed. The blue box highlights Stage 1 of the shift register with all of the relevant V_O, V_{GD} and V_C outputs and inputs labelled.

The blue box surrounding the first part of the circuit is the same setup as the dynamic pass transistor circuit shown in Figure 5.5-9. The output of this inverter then drives the input of the 2nd set of pass transistors as with the V_{SP2} voltage in Figure 5.2-5 and the V_{O2} of this section acts as the output voltage of Stage 1. Stage 2 is comprised of the same design but being fed by V_{O2} as the input voltage and so forth, as described in Section 5.5.1. The transient response for this stage is shown in Figure 5.5-12 and clearly passes along the signal. The rise and fall times are tabulated in Table 5.5-1 for comparison with Stage 2.

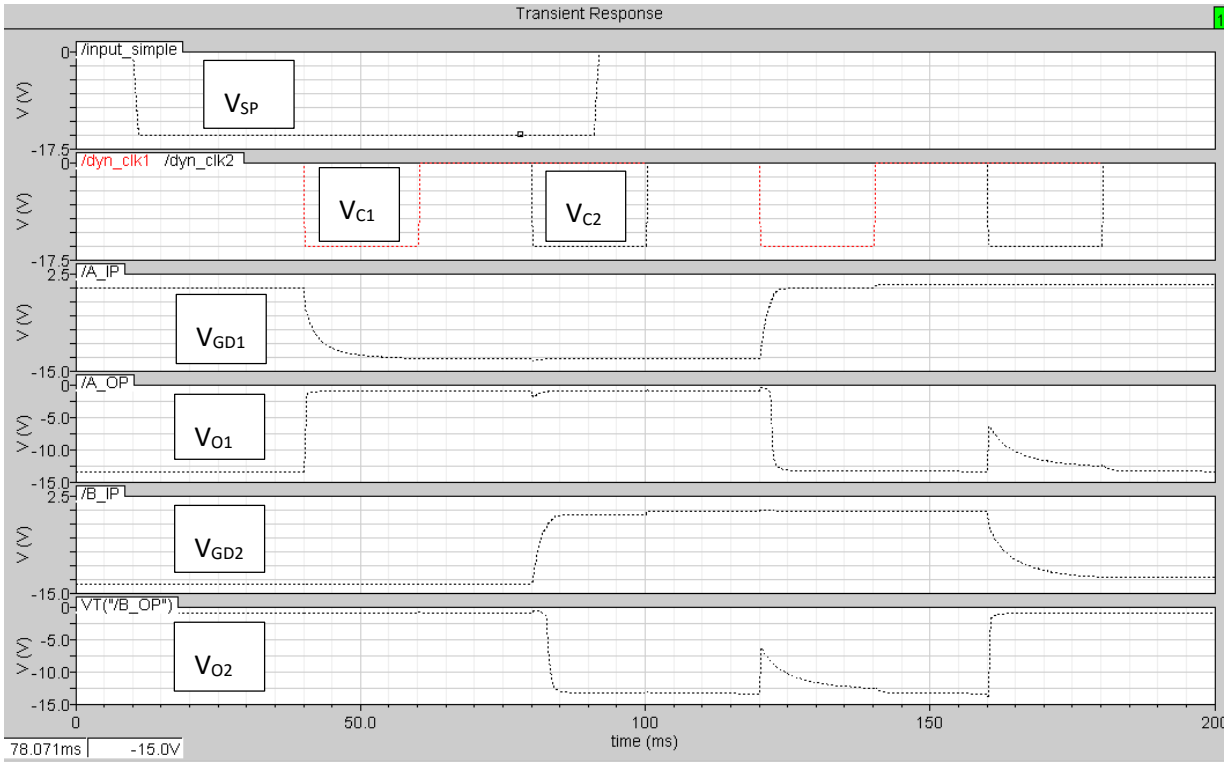

Figure 5.5-12 Transient response for the saturated load shift register. The V_{GD} and V_O voltages are labelled and show that the shift register functions as expected for Stage 1. The detailed values from the rise and fall times of the response and maximum/minimum voltages are recorded in Table 5.5-1. The input signal is a 40 ms pulse of -15 V with a rise and fall time of 1 ms. Clock pulses have a width of 10 ms.

Figure 5.5-13 focuses on Stage 2 of the shift register and one again contains the labels used in Section 5.5.1.

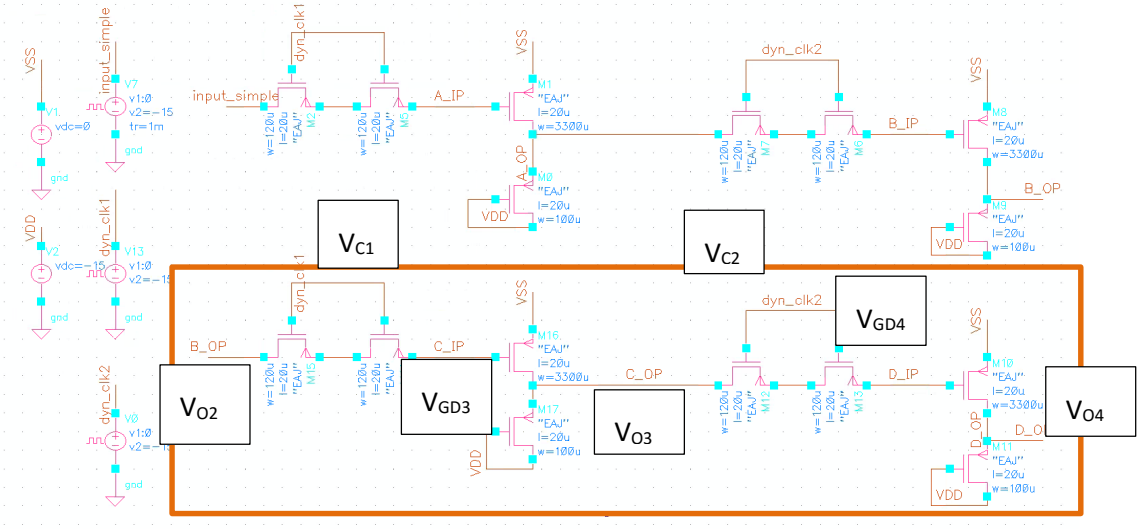

Figure 5.5-13 - Circuit diagram of saturated load shift register with double pass transistor input and the models and ratios as designed. The blue box highlights Stage 2 of the shift register with all of the relevant V_O, V_{GD} and V_C outputs and inputs labelled.

The transient response for Stage 2 is shown in Figure 5.5-14 and shows that the signal also survives the 2nd stage with limited degradation. One thing that is prevalent is the 6.2 V loss at 200 ms from the dynamic clock pulse. This occurred at V_{O2} as well but is highlighted here in red. This loss is probably due to some of the charge leaking at the point of the pass transistor opening from the previous inverter, however it recovers itself in the charge balancing and the signal is recovered before the end of the pulse.

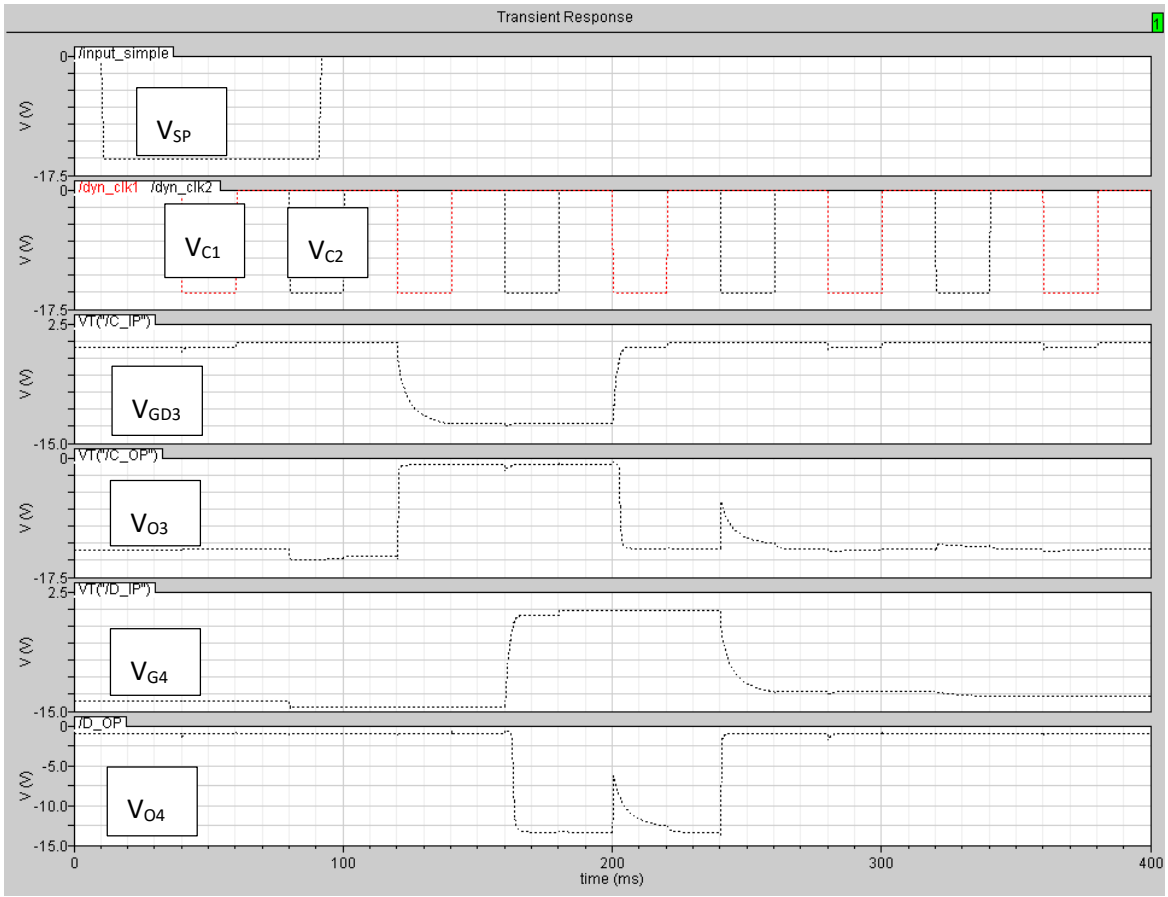

Figure 5.5-14 - Transient response for the saturated load shift register. The V_{GD} and V_O voltages are labelled and show that the shift register functions as expected for Stage 2. The detailed values from the rise and fall times of the response and minimum/maximum voltages are recorded in Table 5.5-1.

The rise and fall times of all of the inverter inputs and outputs are in Table 5.5-1. It is very clear is that the rise times for V_{GD} inputs 2, 3 and 4 that occur past the first inverter can take > 10 ms to charge. This is due to the input from the pass transistor, however there is not an increase with stage which means that it is local to each inverter setup. Conversely, the fall times of the inverters are all < 1 ms showing that past the inverted signal this has no bearing on the output. This allows for the circuit to function regardless of slow rise times.

Table 5.5-1 – Rise and fall times comparison of saturated load configuration for both stages.

	Rise Time (ms)	Fall Time (ms)	High voltage (V)	Low voltage (V)	Max Voltage range (V)
V_{GD1}	6.15	2.08	-12.73	0.50	13.23
V_{O1}	1.19	0.49	-13.42	-0.89	12.53
V_{GD2}	13.39	2.53	-13.40	-0.89	12.51
V_{O2}	1.49	0.29	-13.33	-0.89	12.44
V_{GD3}	13.32	3.17	-12.07	-0.04	12.03
V_{O3}	1.27	0.63	-13.34	-0.90	12.44
V_{GD4}	13.95	3.80	-12.71	-0.04	12.67
V_{O4}	1.27	0.63	-13.35	-0.89	12.46

It is apparent from the V_{GD} inputs that the off-state voltage can go beyond 0 into a voltage > 1 V. This is more likely to occur in sync with a clock pulse, possibly due to the input obtaining some extra charge from the pulse as well as its own input. It is this path that can also cause the voltage losses in the passed signal that was mentioned previously.

There is also an overall loss in voltage compared to the input signal which can vary between a loss of the threshold voltage 1.6 V (as shown by voltages close to 13.4 V) or sometimes greater. Generally, any the high losses are as a result of the slow rise times. A couple of tests were run that showed that if the clock pulse size is increased, the output voltage was closer to that of the V_{DD}-V_T. This means that there would have to be a trade-off between the size of these pulses and output voltage loss. Less output voltage is lost for wider clock pulses, however this would increase the amount of time that there is disruption to the output signal from the pass transistor being open. Also, it was clear that in all cases the rise times are an order of magnitude slower than the fall times; this is caused by the aspect ratio of the devices. The load device is a much smaller device which reduces the charge time. This dependence on size restricts design and is why ratioed logic was replaced by CMOS.

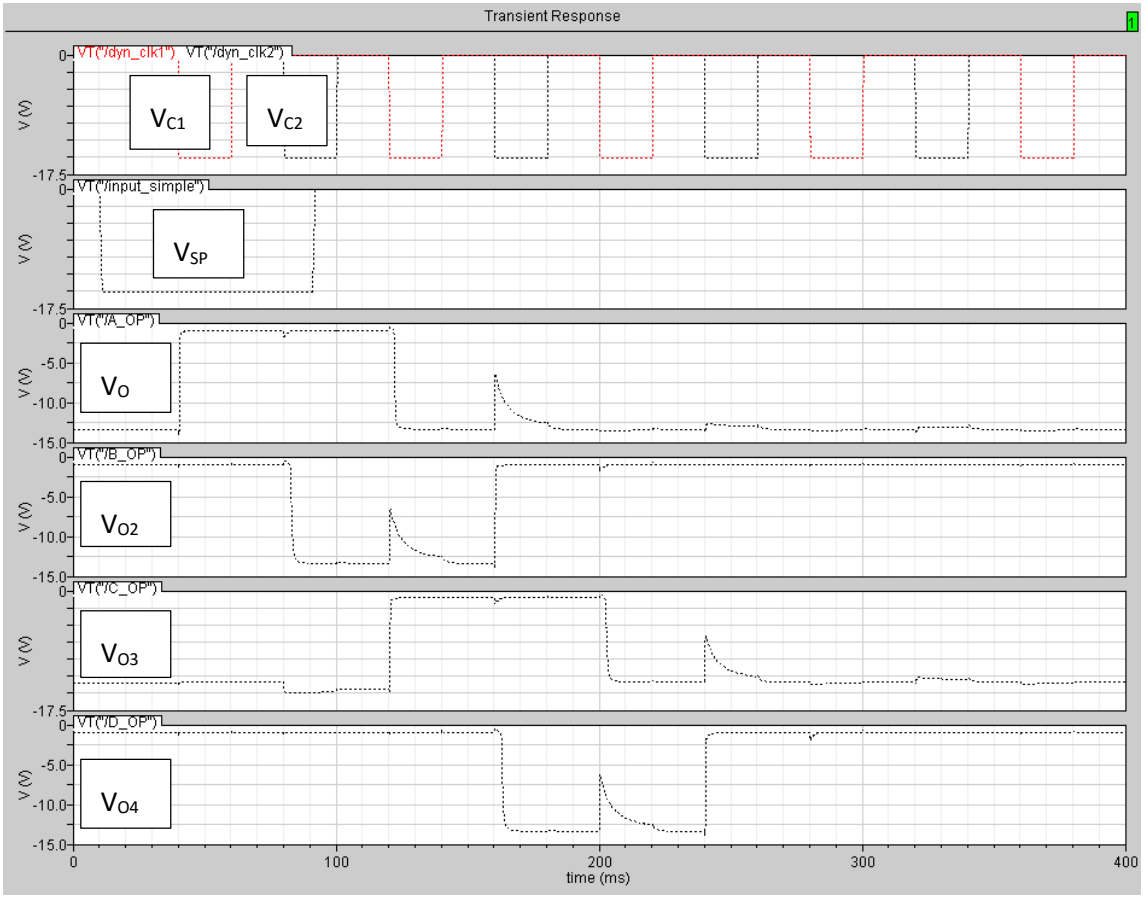

Figure 5.5-15 – Transient response for the 4 main outputs of the shift register.

The four main V_o are shown in Figure 5.5-15. Despite the loss of voltages at particular points and the slow rise and fall times from the V_{GD} inputs, it is clear that the shift register works to pass along the original V_{SP} signal while also maintaining the pulse width and without any loss of voltage due to number of stages passed. This proves that a viable shift register can be simulated based on the organic devices characterised in Chapter 3 and modelled in Chapter 2.

5.5.4 Pseudo-CMOS Inverter Shift Register Simulation

The pseudo-CMOS shift register is simulated in the same manner as the saturated load shift register with all outputs and inputs having the same connections, the only difference being the addition of the second inverter set. The circuit for this can be seen in Figure 5.5-16.

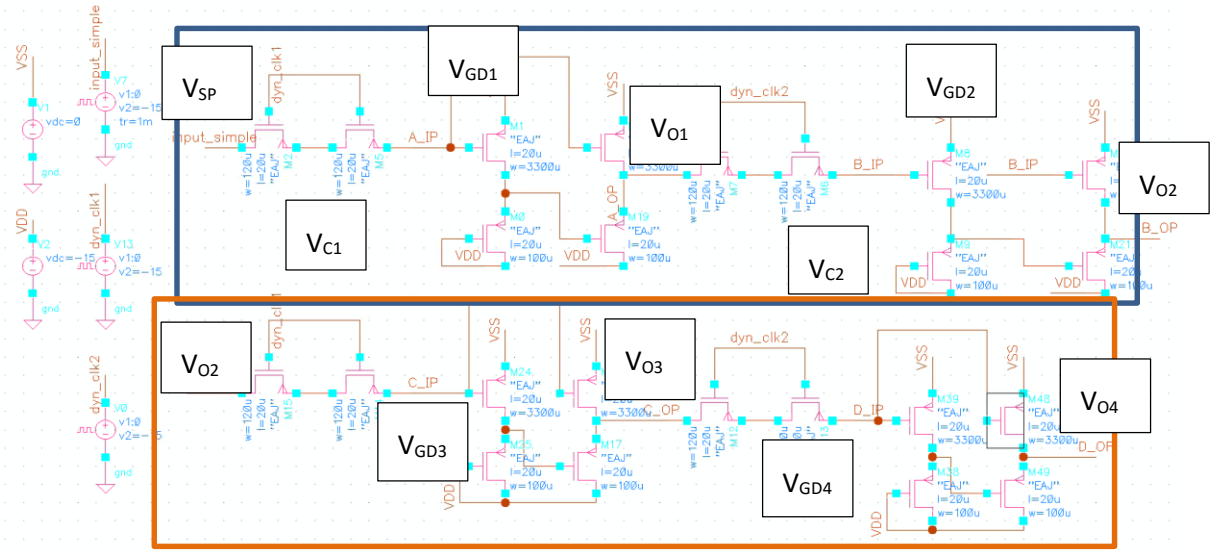

Figure 5.5-16 Circuit diagram of pseudo-CMOS shift register with double pass transistor input and the models and ratios as designed. The blue box highlights Stage 1 of the shift register and the orange box highlights Stage 2. All of the relevant V_O, V_{GD} and V_C outputs and inputs labelled.

As with the saturated load configuration, the dual pass transistor is needed for the purpose of the Cadence simulation. The transient response for this setup can be seen in Figure 5.5-17 and Figure 5.5-18 with all 4 outputs shown in Figure 5.5-19. As with the previous configuration has various values extracted and tabulated.

These outputs, as shown in Figure 5.5-17 and Figure 5.5-18, are akin to those of the saturated load transistor, suffering the same voltage losses at the same points and the same slow rise times. The main difference is that all of these disadvantages are of a higher value. It can be seen in Table 5.5-2 that the rise times for V_{GD}s range from 13.41 – 16.77 ms. These are greater than those from the saturated load, in the first case approximately double. This is in line with the original inverter measurements.

Table 5.5-2- Rise and fall times comparison of pseudo-CMOS configuration for both stages

	Rise Time (ms)	Fall Time (ms)	High voltage (V)	Low voltage (V)	Max Voltage range (V)
V_{GD1}	13.41	4.55	-12.15	0.32	-12.47
V_{O1}	1.44	0.28	-11.81	-0.02	-11.79
V_{GD2}	15.57	5.15	-11.59	0.32	-11.91
V_{O2}	1.68	0.48	-13.36	-0.02	-13.34
V_{GD3}	13.41	4.79	-10.60	0.32	-10.92
V_{O3}	1.44	0.48	-13.09	-0.01	-13.08
V_{GD4}	16.77	5.27	-12.02	0.32	-12.34
V_{O4}	1.40	0.48	-13.35	-0.01	-13.34

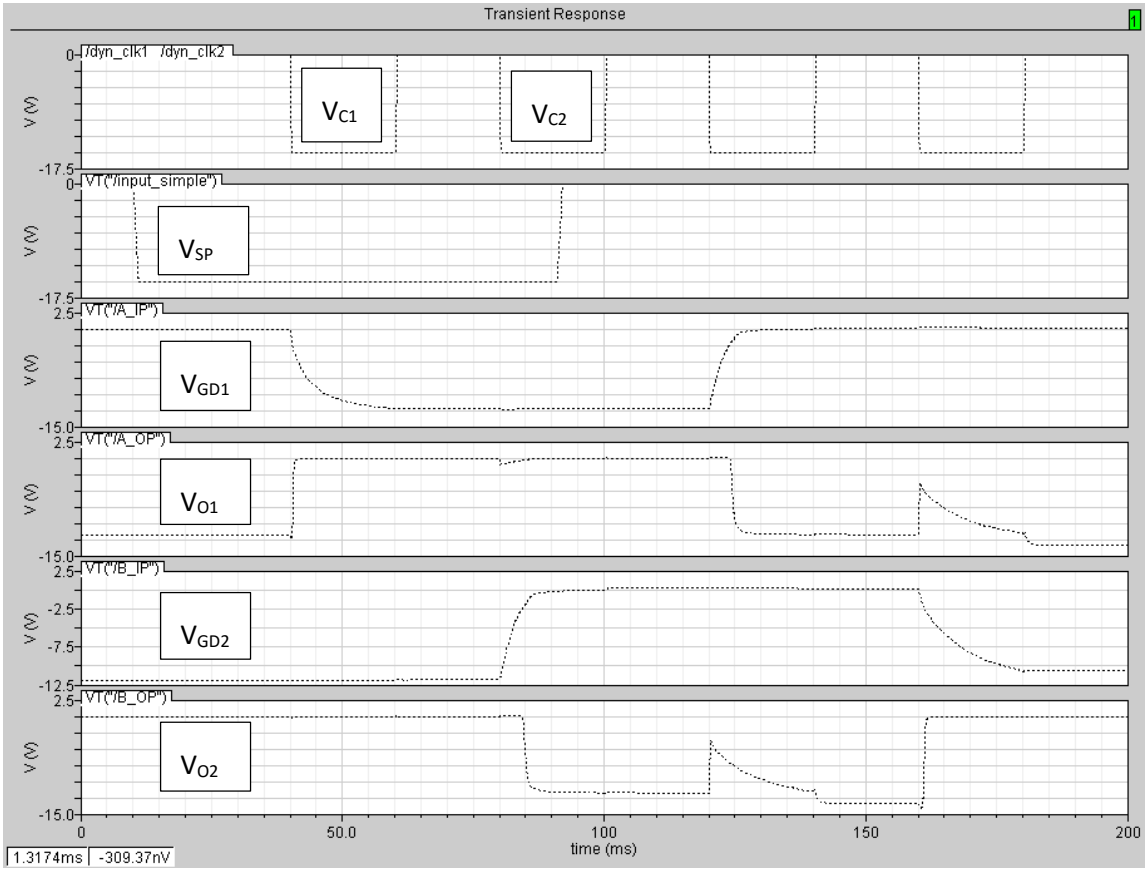

Figure 5.5-17 – Transient response for the pseudo-CMOS shift register. The V_{GD} and V_O voltages are labelled and show that the shift register functions as expected for Stage 1. The detailed values from the rise and fall times of the response are recorded in Table 5.5-2. As with the saturated load setup, the input signal is a 40 ms pulse of -15 V with a rise and fall time of 1ms. The clock pulses have a width of 10 ms

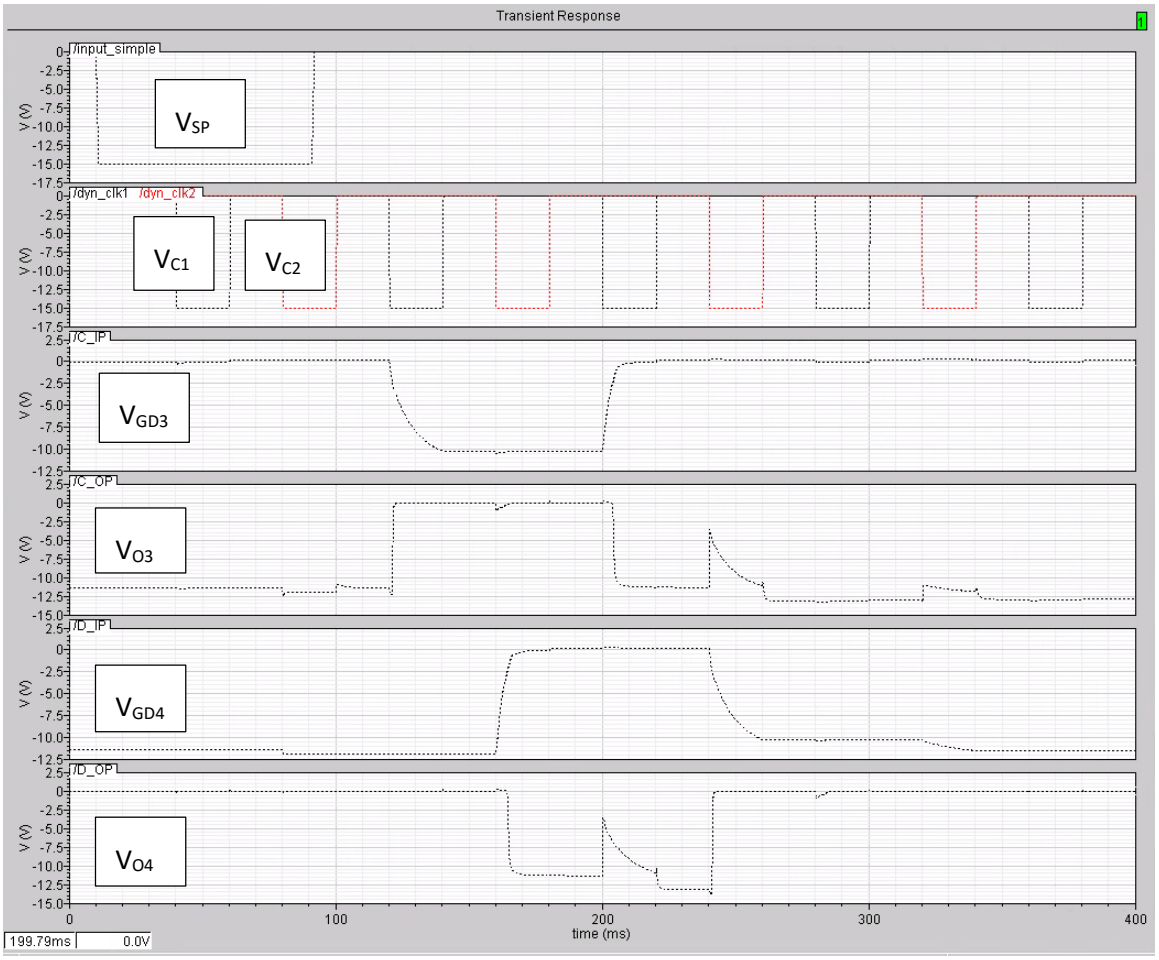

Figure 5.5-18 – Transient response for Stage 2 of the pseudo-CMOS shift register. The detailed values from the rise and fall times of the response are recorded in Table 5.5-2. As with the saturated load setup, the input signal is a 40 ms pulse of -15 V with a rise and fall time of 1ms. The clock pulses have a width of 10 ms

A comparison of the voltage swings for the two configurations of inverter are shown in Table 5.5-3.

Table 5.5-3 – Voltage parameters of the two configurations of shift registers for all of the V_{GD} and V_O outputs

Voltage Output	Saturated Load			Pseudo-CMOS		
	High voltage (V)	Low voltage (V)	Max Voltage range (V)	High voltage (V)	Low voltage (V)	Max Voltage range (V)
V_{GD1}	-12.73	0.50	13.23	-12.15	0.32	-12.47
V_{O1}	-13.42	-0.89	12.53	-11.81	-0.02	-11.79
V_{GD2}	-13.40	-0.89	12.51	-11.59	0.32	-11.91
V_{O2}	-13.33	-0.89	12.44	-13.36	-0.02	-13.34
V_{GD3}	-12.07	-0.04	12.03	-10.60	0.32	-10.92
V_{O3}	-13.34	-0.90	12.44	-13.09	-0.01	-13.08
V_{GD4}	-12.71	-0.04	12.67	-12.02	0.32	-12.34
V_{O4}	-13.35	-0.89	12.46	-13.35	-0.01	-13.34

The side by side comparison shows that while the fall times are longer for the pseudo configuration, the inverted outputs do not seem to suffer from any issues with voltage loss or time from the V_{GD} inputs. There is, however, still the impact of the larger voltage loss from the double threshold voltage loss shown in the initial inverter responses.

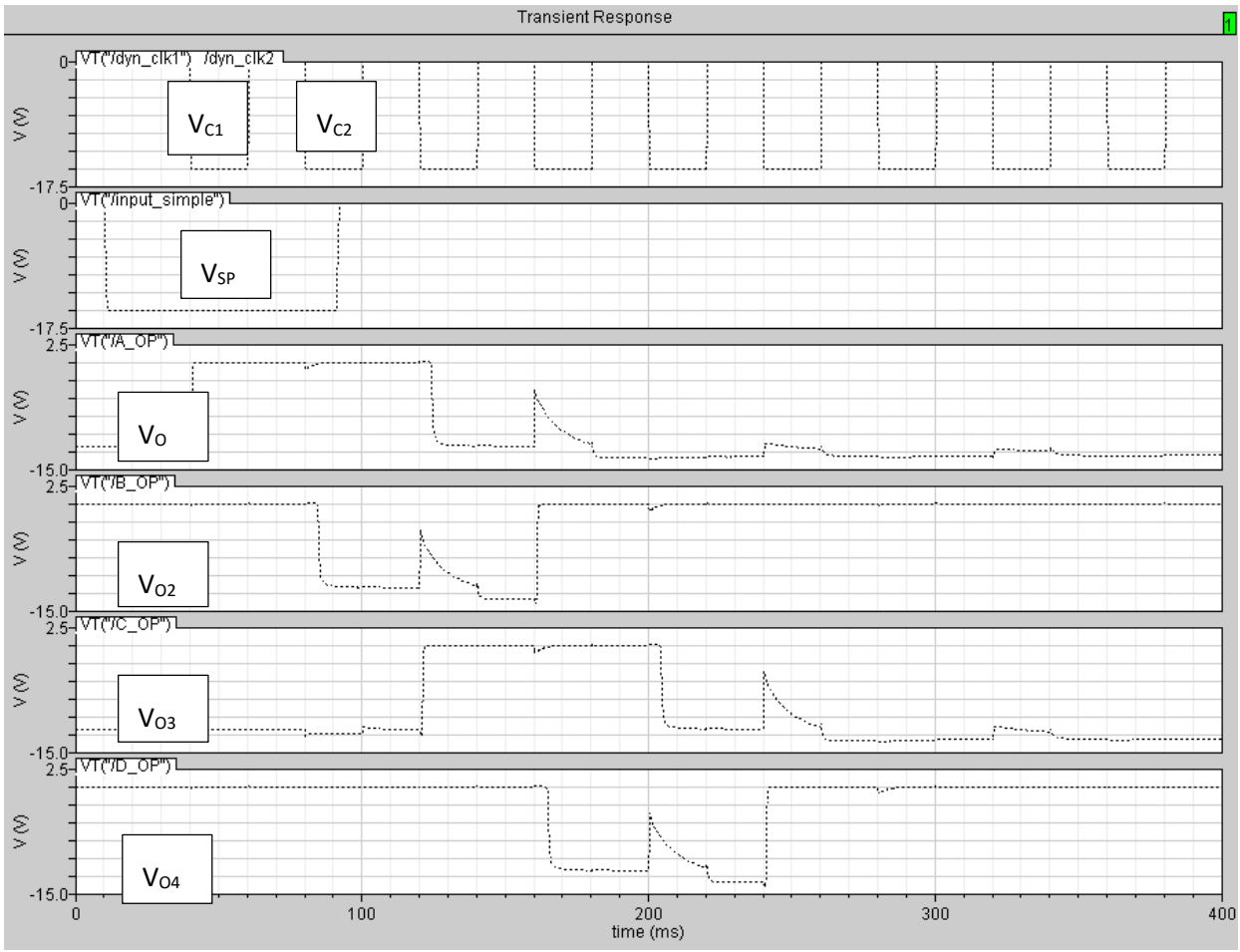

Figure 5.5-19 - All 4 outputs for the simulated 2 stage pseudo-CMOS shift register.

As with the saturated load, the pseudo-CMOS configuration produces a viable shift register design with the organics models. The slower rise times, however, prove it to be an inferior setup to use and Table 5.5-3 shows that while, in practice, the voltage swings are very similar to those of the saturated model there are still some greater losses in maximum voltage in spite of the minimum voltages being closer to zero. It is for this reason that it was decided to use the saturated form for the mask design.

5.6 Layout Design For Fabrication

The fabrication process involved for circuit design is much more complex than that of single devices. There are many more process steps involved and with each stage comes further risks that can affect

the formation of former layers. A single defect at an early stage of the process can jeopardise the performance of the circuit as each stage is interlinked and care has to be taken to ensure that any sensitive part of the circuit is protected from chemical reactions or interference. Measures are also necessary to reduce risk of short circuit or poor oxidation. An extra concern with organic processing is the sensitivity of the semiconductor, as discussed in Section 3.1 which is therefore left until the final stages of the process.

Both the design and fabrication of organic circuits are heavily interlinked with the practical experience of the process involved pivotal at every stage. Once a viable schematic has been produced, the physical structure of the design must be conceptualised and divided into corresponding stages of the process. For each of these stages a mask design is produced taking into account the physical restrictions that need to be considered. In general, stages follow a pattern of application of a material, photoresist deposition and pattering and then an etching stage; this results in approximately one mask design per major stage of process and these are detailed below in tandem with the corresponding fabrication stage.

Figure 5.6-1 shows the completed masks. These were designed within the scope of this project and within the rules featured in the respective tables for each mask.

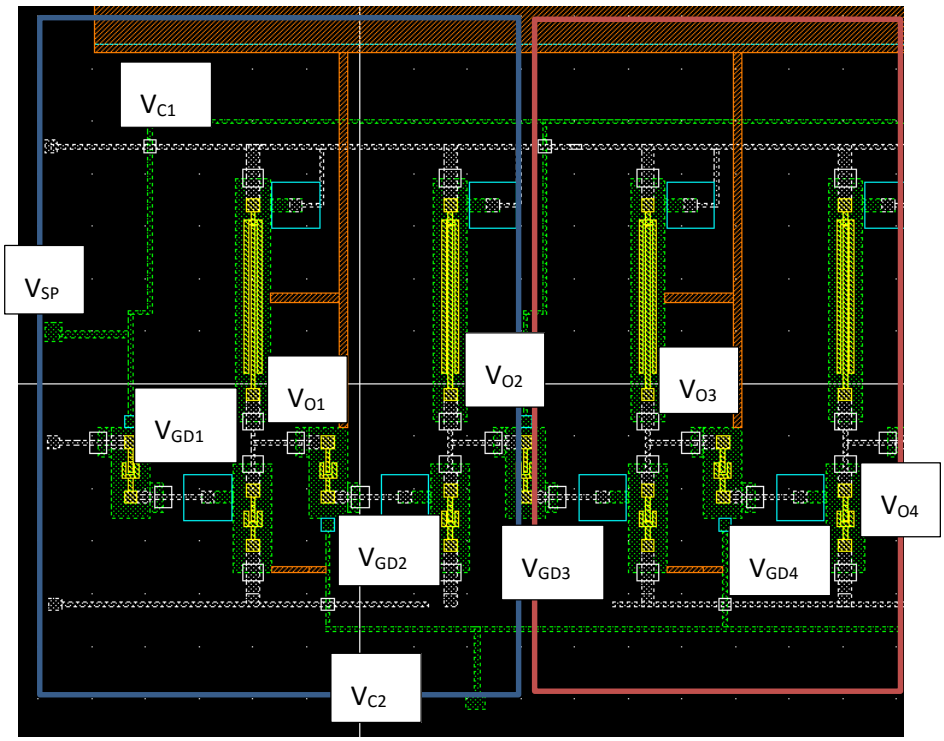

Figure 5.6-1 - Full Layout design for dynamic organic shift register based on the models from devices in Section 3.7.1 and the circuit design in Section 5.5.3. All layers were drawn obeying the design rules featured.. The blue box contains Stage 1 and the orange contains Stage 2.

The shift register was developed as a mask design with care to adhere to any rules based on knowledge of clean room techniques and focussed on alignment error and minimum feature size. The minimum feature size was λ_m = 20 µm and the alignment error λ_a = 40 µm. This is to take into account processing tolerances. The voltage inputs/outputs for Stage 1 can be seen in Figure 5.6-1 to match the inverters with their respective parts on the circuit design. It can be seen that the two V_C are positioned as one above and one below in order to clock their alternate inverters. Also note the shape of the transistors. This allows for the large Driver:Load ratio to fit comfortably within the circuit and improves packing density.

Many of the processing steps involved for this particular process are similar to those documented in previous sections; however they are reviewed along with the rule guide. These rules take into account the possibility of more than one layer being misaligned and therefore, especially in cases where contact could have detrimental effects, great care would need to be taken.

Step 1 - Substrate

As detailed in Chapter 3, the substrate is prepared using the same techniques as with the devices. For larger circuits, flex can be used as an alternative to glass as this allows for more complex designs and greater potential in application. A flexible substrate however comes with its difficulties in processing and therefore carriers are needed in order to keep the surface flat and uniform throughout the process. For the non-self-aligned, glass substrate circuits, however, this is not an issue.

Step 2 - Aluminium 1 Layer

As the complexity of the circuit increases, so does the likelihood of crossover of current paths. In order to avoid short circuits, two aluminium layers are needed and a form of insulation is required whenever these two layers overlap (detailed in Step 4). At the first stage, there is no restriction in safeguarding any part of the circuit. Aluminium was evaporated across the entire samples at a thickness of 250 nm using the same method as detailed in Section 3.5.1. This formed the gate contact. In order to isolate devices, the aluminium 1 layer was patterned, spinning a layer of photoresist and using the first mask design, ALU1.

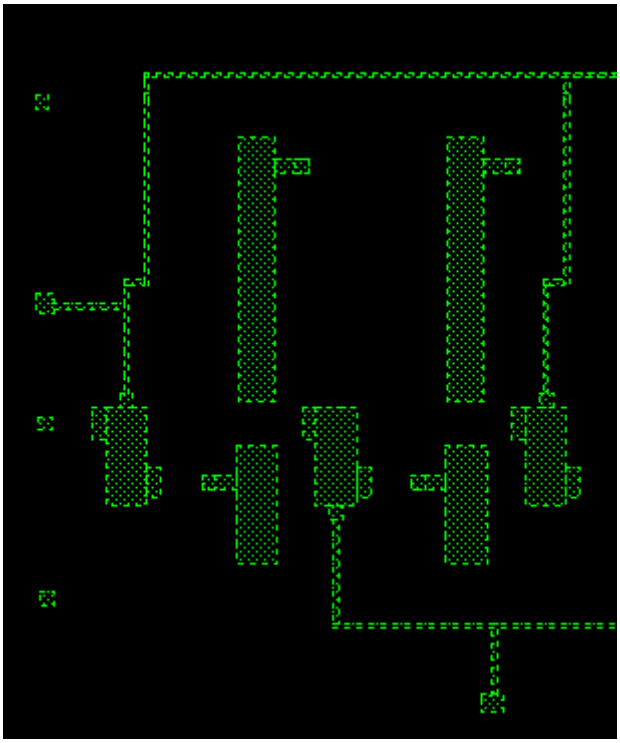

Figure 5.6-2 ALU patterned mask showing gate islands and voltage rails

As can be seen in Figure 5.6-2, this ALU1 layer forms the gate for each device, producing islands of aluminium. As each of these areas needs to be oxidised at the later stage, the ALU1 mask also must have a path to a large contact for anodisation. This contact strip is featured at the top of the design. It is > 1 cm in height and stretches across the full width of the sample. This size is to allow the contact of a crocodile clip without any risk of touching the circuit. Once patterned, the sample is then etched, removing any of the redundant aluminium. Likewise, the later ETCH stage will ensure that any paths needed solely for anodisation will be removed.

Layout considerations for ALU1 mainly consist of being large enough to accommodate future components. The other crucial dimension (and applicable to all stages) is the minimum feature size λ_m. As discussed earlier in the chapter, this is set at 20 µm and therefore is the designated size for channel length. The summary of considerations for this stage of development are listed in Table 5.6-1.

Table 5.6-1 – Table of rules for ALU1 layer

1.01	ALU1 must be minimum of λ_m
1.02	There must be at least λ_a between unconnected ALU1 sections
1.05	There must be at least $2\lambda_a$ surrounding any Au layer
1.06	There must be at least $2\lambda_a$ extension over OSC
1.07/1.08	ALU1/ALU2 needs $2\lambda_a$ needed for contact (perpendicular or in line)

Step 3 - Gatecon

As the entire sample will be submerged for anodisation, it was necessary to cover sections that are not to be oxidised (i.e. the gate contacts). This was patterned in the same way as the previous stage, however it becomes crucial from this point onwards to use the alignment crosses in order to ensure that the masks are in line; this manual process of alignment is the cause for λ_a.

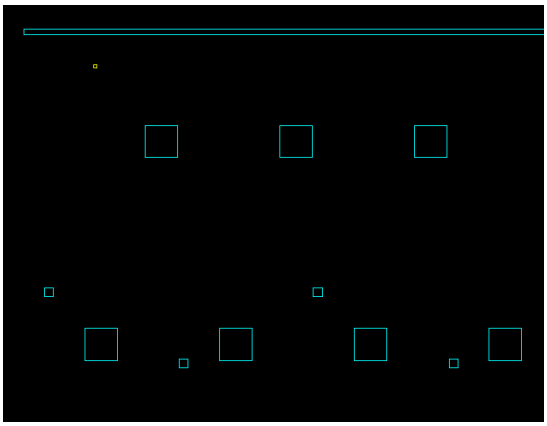

Figure 5.6-3 Gatecon mask showing the sections that need to avoid oxidation such as gate contacts. These points can be seen as the blue squares.

A gatecon layer is generally only applied to sections where it is imperative for there to be contact. Although only the channels require oxidation, it is simpler to oxidise the rest of the sample even if just pathways. It should be noted however that any oxide will form a capacitance with a parallel plate metal. This has to be taken into account, but it is easier to reduce this by carefully patterning ALU1 to reduce excess metal rather than reducing the oxidised areas.

Table 5.6-2 Table of rules for Gatecon layer

1.03	Gatecon must have a λ_a enclosure surrounding ALU1

Step 4 - Anodisation & Etch

The anodisation process follows the same procedure as that for the devices with the exception of a photoresist spin beforehand to protect the areas that are not to be anodised. In order for the anodisation to work, all relevant aluminium patches must be connected to the main contact. It is for this reason that an Etch stage is needed as this then removes the aluminium once the anodisation has taken place. This include the large contact that the sample is held by, and all of the ALU layers that mustn't be short circuited.

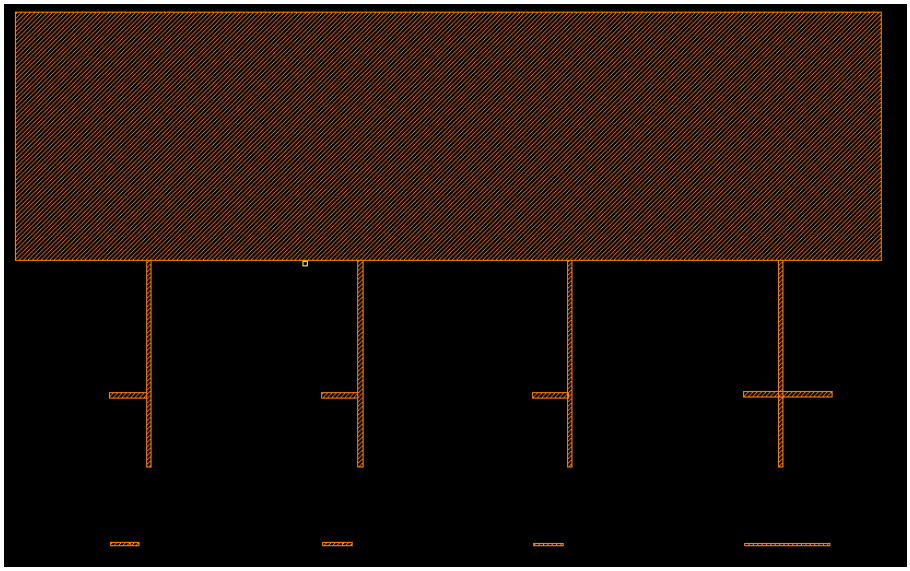

Figure 5.6-4 Etch mask shows the areas that will be removed once anodisation is complete.

Step 5 - Gold deposition

The gold layer is deposited with another photoresist patterning and follows the same process as with the devices.

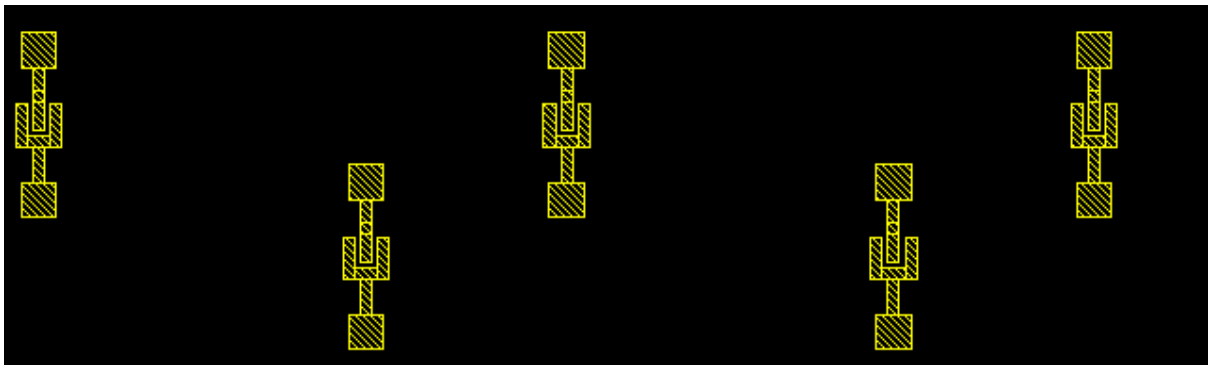

Figure 5.6-5 Driver and pass transistor source and drain contacts. These clearly show the transistor shape explained in earlier section.

The gold patterning allows for the slot-like transistors to be formed and reduce the internal capacitances and improve packing density.

Table 5.6-3 - Table of rules for Gold layer

3.1	Au width must be minimum of λ_m
3.2	There must be at least λ_a between unconnected AU sections
3.3	Must be $2\lambda_a$ gap between any unrelated ALU2
3.4	Must be $3\lambda_a$ gap between any ALU2/AU contact to SU8
3.4	Must be $3\lambda_a$ overlap beyond polymer
3.6	Must be $3\lambda_a$ spacing between unrelated polymer

Step 6 - SU8

The SU8 stage is a stage that is unique to the circuit process as opposed to the devices. It is a high contrast photoresist that works as an insulation layer. It is used over the edges of the metal surfaces to avoid cracking in the layers. It was found that having an overhang even on thin layers could affect the performance of the circuit. It also provides a cross over for when the ALU1 layer and ALU2 layer need to pass over. This is generally avoided as it causes unnecessary capacitance, however it is sometimes unavoidable for complex circuits. One of the major problems in design was being able to attach the aluminium contact to the gold beneath it. SU8 was needed not just for the edge of the device but also to prevent shorting between the two aluminium layers. Figure 5.6-6 shows both ALU layers with the SU8 (as shown by the empty white boxes). This not only prevents unwanted contacts but also helps ease the metal over sharp edges.

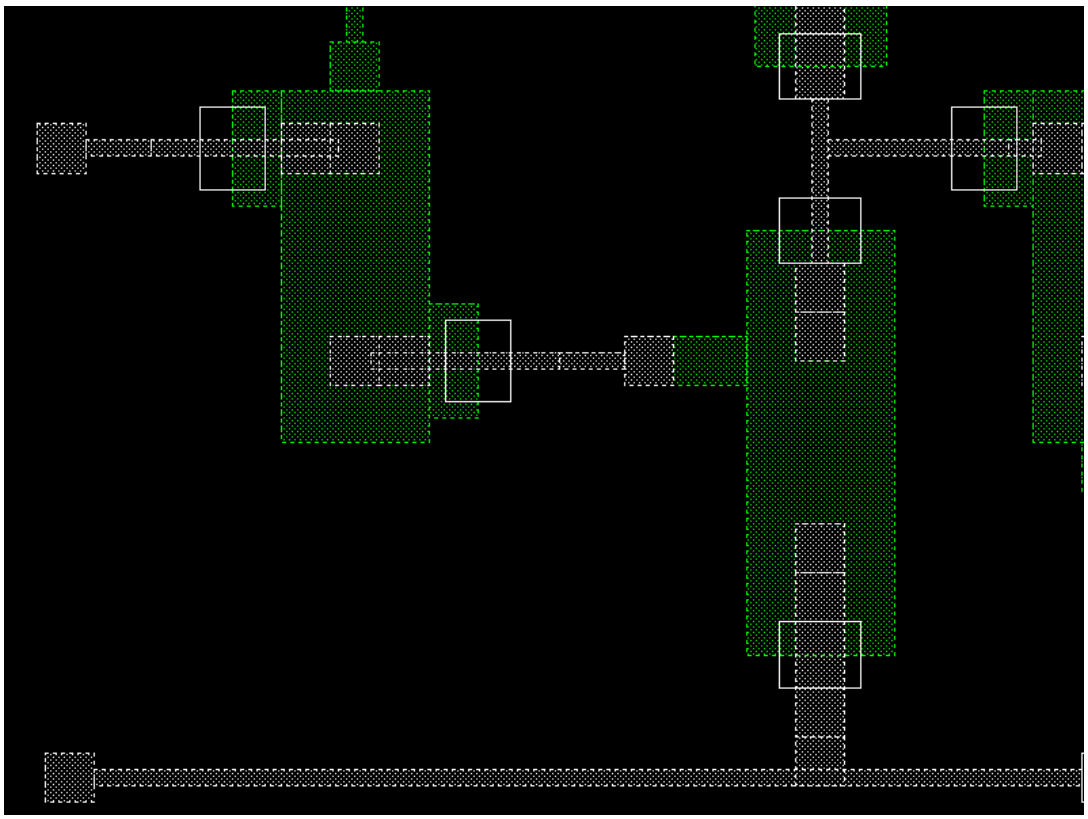

Figure 5.6-6 The ALU 1 and 2 layers to show the SU8 layer protecting the edges from connecting.

Step 7 - Aluminium 2 Layer

The second aluminium layer follows the same process as the first aluminium layer however the rules take into account larger error margins because of the possibility that stages below have also been misaligned. The further into the process, the more likely it is that there has been a misalignment and the greater the danger. These shaded white patches can be seen in Figure 5.6-6.

Table 5.6-4 Table of rules for ALU2 layer

2.1	ALU1 must be minimum of λ_m
2.2	There must be at least λ_a between unconnected ALU2 sections
2.3	There must be at least λ_a for Au contact
2.4	There must be at least λ_a surrounding any Au layer as both can be misaligned
2.5	ALU2 must extend λ_a over any ALU1/Gatecon contact it is connected to
2.6	Must be $3\lambda_a$ gap between any ALU1/Gatecon contacts
2.6	Must be $3\lambda_a$ gap between any ALU1/SU8 contacts
2.7	Must be $3\lambda_a$ gap between any unrelated polymer

Step 8 - Polymer deposition

The final process in the stage is to have polymer spun over the top of the circuit. Doing this at the end of the process protects the polymer from getting damaged during any other process stages. It is beneficial to only put polymer over devices where it is needed in order to avoid stray leakage throughout the circuit. It is also possible to have a passivation layer that protects the polymer from outside effects of air or moisture which may cause degradation.

5.7 Summary and Conclusion

Chapter 5 was focussed on pulling together the theoretical and experimental work performed in Chapters 2 & 3 to produce a working shift register design simulation. This allowed for the mobility parameters extracted based on the L1 distribution models to calculate driver/load ratios for two different inverter design configurations and highlighted the viability and limitations of a dynamic shift register based on these devices.

The two different inverter setups, the enhancement mode, saturated load inverter and the pseudo-CMOS inverter were chosen based on the evolution of silicon inverters that led to the development of the power saving CMOS configuration. As CMOS is not possible with the p-type devices that were made, and because n-type materials have only recently begun to rival p-type mobility levels for organics, these alternative setups were used and the challenges associated with them tested and compared within the simulation. Both of these were explained and the regions of operations considered. Using the models optimised to the devices fabricated within the project, the inverters were built and the DC characteristics and transient response for each was taken. The slope of the voltage swing was found to be in line with the driver/load ratio for the saturated load inverter, however the pseudo-CMOS inverter was found to have a much steeper slope due to the second inverter stage. The pseudo-CMOS inverter was able to mimic the switching of the output without a

constant supply to the load. This was due to a second internal inverter controlling the driver of the output inverter however, despite the efficiency in fall time, this increased the overall rise as a result of the extra capacitances involved. There was also a greater voltage drop at the output from needing two applied V_Ts to hold the output high. This was echoed in the design of the shift registers for each configuration and therefore it was decided that the saturated load was the superior configuration in this case.

The internal capacitances were considered in the context of the total load capacitance and the design methods to combat the wastage from these capacitances was considered in the mask design. Although the possibility of using a self-aligned gate was ruled out based on a test of the material with such a circuit, it was decided based on the design of the transistors in the masks used to fabricate devices at Merck Chemicals Ltd. that both the packing density and load capacitance could be improved by incorporating a slot-like transistor into the design. This also would combat the issues detailed in Chapters 3 and 4 regarding measuring of devices directly above the oxide.

A study was done in simulating a dynamic pass transistor in Cadence and it was found that in order to replicate the behaviour with the software two transistors would be needed. This was for simulation purposes, however, and would not need to be incorporated for the final mask designs. As stated previously, shift registers designs were then simulated for both configurations of inverter and while both performed as expected the saturated load circuit was the more efficient of the two. Due to the low mobilities of the organic device models and the large driver/load ratio, the rise times were found to be very slow. This was made worse by the extra pass transistor incorporated into the simulation design. As a result of this, the width of the dynamic clock pulses had to be as long as 10 ms in order to allow the signals to pass. While the simulations are not ideal, due to the reliance on silicon current behaviour, this is the kind of drawback of organics that could potentially be solved by scaling of devices and optimising the materials to produce higher mobilities. While fabricating a circuit was not part of the wider scope of the project, a working simulation based on the parameters extracted using the current models was achieved and finally masks were designed to reflect the circuit. This was done within the design rules of a non-self-aligned circuit process as well as with consideration of practical knowledge gained from device fabrication.

5.8 References

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Chapter 6 CONCLUSIONS AND FURTHER WORK

6.1 Overview and Conclusions

As interest and popularity grows for the Organic Electronics discipline, the need for better understanding and improved methods increases. As the market need increases, the output has to deliver and, just as a concept such as Moore's Law accompanied the success of silicon technology, organics continues to explore new avenues that have been unable to be accessed up to this point.

As the discipline broadens it is becoming increasingly important to develop more accurate models in order to help make clearer the intricate properties of materials and in line with that, the restrictions which will need to be overcome as interest grows.

This study has seen a wider look at the building blocks and steps towards the more complex possibilities that organics provides. While many areas focus on one specific area, this study has been an exercise in the whole outlook, from understanding devices to considering the comparisons with successful technologies in order to anticipate problems which may occur.

The first main section of this work looked at the basic differences between disordered organic materials and polycrystalline materials. As more materials are developed, a better understanding of the transport within them and the way in which they can be modelled is becoming more important. There are still many differing opinions in organics, for example the nature of the distribution of states. One of the things considered in this section was a third distribution option; the Laplace 1 distribution. This provided a solution to the Meyer Neldel energy occurring across a wider range with diodes as well as producing a more mathematical argument for using an exponential distribution. Along with this possibility, it also provides a solution for obtaining either T_o or T_C in diode behaviour based on a proposed Two Condition Theory. This theory proposes that the extraction of T_o or T_C could be related to the relative position of E_F with respect to the mobility edge E_T. Although there is still no definitive explanation or proof for the governing distribution, the further exploration of Laplace could be of benefit to understanding more about the way carriers behave. It was stated that while this distribution comes from a different root, it can be approximated to an exponential for energies that take place several kT below an energy level E_θ and thus the derived models that exist are still appropriate. These existing derivations were then used to extract parameters from experimental results in Chapter 3 to test their compatibility.

The practical side of this study looked at the fabrication technique of devices with the aim to develop a better understanding of how individual circuits work for the future context of circuit design. In order

to do this, many samples of TFTs and diodes were fabricated, using two different techniques for the former as well as capacitors in order to derive load capacitance and understand scaling implications. Through practical experience, various processing challenges were encountered providing insight into the practical importance of device design. Phenomena such as hysteresis were prominent and a study was done to reduce the effect based on re-application of the semiconductor. There was also a comparison of copper and gold as Ohmic contacts in a diode. This was initially due to difficulties with gold processing however it proved to identify an issue with copper processing based on a reaction with the stripper. A circuit was also fabricated in order to gain understanding of the more complex stages involved in circuit processing. This provided the basis for designing mask layouts for which is it imperative to have a thorough understanding of the practical side of circuit fabrication. The devices made could be used to test the theory derived in Chapter 2 and the models proved successful for both the polycrystalline and disordered derivations. The compatibility of the disordered equation with the polycrystalline material is evidence that the disorder in the grain boundaries has a strong impact on carrier conduction within polycrystalline materials.

A more specific focus of the practical stage of the project was a study on the scaling implications of organic devices. In order to assess this, a comparative look was taken of silicon scaling rules and each considered in the context of the behaviour of organic devices. Analysis on the saturated load inverter was performed to prove if the dependence on L was an important factor when removing the concept of mobility, as done by the inclusion of the Universal Mobility Law. This was found to still have an impact. Scaling difficulties were considered such as the effect of thinning the semiconductor layer to reduce off currents. The importance of the Debye Length was discussed, as was the impact of concentration.

In order to understand the study of devices in a wider context, parameters were extracted and it was discussed how these parameters can be used in circuit design the mobility, load capacitance, oxide thickness and aspect ratios were derived for a saturated load set up of an inverter. While the software is currently unable to cater for organic models, the possibilities of how to enhance simulation could be done and basic use of these values were used at least in a theoretical capacity to compare the impact of load/driver ratio on an inverter. A model file was created using the parameters extracted from the theory in Chapter 2 and the devices in Chapter 3.

Inverter characteristics for two configurations of inverter, the pseudo-CMOS and saturated load inverter were looked at comparatively, each providing their own advantages and disadvantages for application within a shift register design and some simulations were run to produce a dynamic pass transistor within the simulation. This was due to the shift register being based on a dynamic input

whereby charge can be stored at the node of a pass transistor and controlled using a clocking sequence of alternating devices. Both configurations were able to produce a shift register and could be compared based on their packing density and performance. Based on the design of the saturated load inverter, a shift register layout was produced tying together the practical understanding of circuit fabrication along with the theoretical considerations.

6.2 Further Work

As there were several aspects explored within this project, there are many paths that could be taken depending on what direction was desired.

Theoretically there is much analysis still needed in order to prove whether Laplace offers a viable alternative to the more widely received distributions of Gaussian and exponential. This could be done in the context of developing more accurate models for the current through a transistor, but also further study on the evidence of the implication of E_F and E_T. It would be beneficial to assess responses under different temperatures and discuss the impact in the context of Laplace, especially for diodes. There could be a study into a more direct correlation between the point at which the diode saturates and whether this could be linked to the dominance of T_C becoming a dominance of T_0.

From a practical perspective techniques could be enhanced with much more study done on concentration implications of scaling as well as the possibility of fabricating more reliable devices. It would be beneficial to consider a different structure of TFT to allow characterisation in the glove box as the inability to do this hindered work on hysteresis and stability. There is also scope for further understanding of the significance of the improved hysteresis based on re-application of semiconductor and whether this is tied to contact solution as indicated by the improved contact resistance. There was also a practical indication of the inferiority of using mesitylene as an exposing solvent at the final stages of fabrication. This could be based on the moisture levels in chloroform and is worth understanding in order to reduce device failure should the link be quantifiable.

In terms of circuit design there is the most scope for exploration. It would be of huge benefit to develop accurate simulation models that are not reliant on adaptation of silicon models, as well as a more thorough theoretical analysis of the impact of the dynamic elements. Without accurate models it is difficult to compare any theoretical results with the simulations, but a better use of mathematical modelling could provide a more solid design. Finally, in the contact of fabrication it would be useful to develop and produce masks based on a comprehensive, parameter developed layout in order to truly compare both the accuracy of theoretical models as well as the practical implications of a dynamic

organic circuit. There is also scope for understanding the issues with self-aligned structures and whether the problem lies in the morphology of the material or in the fabrication process.