Structure of the interface in sub-nm EOT $TmSiO/HfO_2$ gate stack

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Abstract

The scaling of the interfacial layer plays a central role in further advancement of high-k dielectric/metal gate CMOS technology. In this work, we focus on a high-k interfacial layer approach based on thulium silicate. A sub-nanometre scaled interfacial layer can be achieved via post deposition anneal at 550°C, which promotes the existence of a graded Tm-Si-O interface with strong sub-oxide Si 3+ presence.

1. Introduction

State-of-the-art CMOS technology employs HfO_2 due to its high dielectric constant (> 20) and ability to achieve suitable n- and p-MOSFET threshold voltages [1-4]. Hf-based dielectric is deposited on top of a sub-nm chemical oxide (SiOx) or oxynitride interfacial layer (IL), whose thickness can be controlled using different oxidation methods and carefully designed scavenging steps [2,3]. A general trend has been observed of strong degradation of the inversion layer mobility with decreased IL thickness, independent of the method used. Even stronger mobility and reliability degradation occurs if no IL is employed [4]. It has been demonstrated recently [1,6] that thulium silicate (TmSiO) is a contender for integration as a high-k IL, achieving equivalent oxide thickness (EOT) of the IL of ~ 2Å with interface state density $<2\times10^{11}$ $cm^{-2}eV^{-1}$. An optimized annealing condition has been reported leading to gate leakage current density comparable with state-of-the-art $SiOx/HfO_2$ nFETs (0.7 A/cm^2 at gate bias of 1 V) at 0.6 nm EOT. However, there is no current understanding of the physical properties of this interface which can lead to the best-scaled gate stack. This paper addresses the latter and provides evidence of a graded IL with strong Si 3+ sub-oxide component.

2. Experimental

The TmSiO IL was formed via atomic layer deposition (ALD) of Tm_2O_3 at 225°C, using $TmCp_3$ and H_2O as precursors, on an HF-last Si surface and annealing [6]. A silicate formation anneal was performed in N_2 at three different temperatures 550°C, 650°C and 750°C for 60 s, leading to the formation of a $TmSiO/Tm_2O_3$ dielectric stack with a target physical thickness of the TmSiO layer of 0.9 nm, 1.3 nm and 2.1 nm respectively. Subsequently, the unreacted Tm_2O_3 was removed selectively in H_2SO_4. HfO_2 was then deposited by ALD at 350°C, using $Hf[C_5H_4(CH_3)]_2(OCH_3)CH_3$ and H_2O as precursors, to a target physical thickness of 3 nm. Core level (CL) structure and the occupied density of states in the valence band were probed by x-ray photoelectron spectroscopy (XPS) using a SPECS monochromatic Al Kα x-ray source (hν = 1486.6 eV) operating at 200 W, and a PSP Vacuum Technology electron energy analyser. The atomic structure and elemental analysis were investigated on TiN capped samples using high-resolution transmission electron microscopy (HRTEM) and electron energy-loss spectroscopy (EELS) performed on a field emission image-corrected FEI Tecnai™ F20 microscope operating at 200 kV.

3. Results & Discussion

Fig. 1 shows an HRTEM image of a $TmSiO/HfO_2$ stack, with two amorphous layers with a bright (TmSiO) and a dark (HfO_2) contrast. The thickness of the IL of ~2.2 nm is within the expected (2.1 nm) value from the annealing condition at 750°C. Figs. 2(a) and (b) show the XPS Tm 4d and Si 2p CL spectra for reference and $TmSiO/HfO_2$ samples. There is a clear

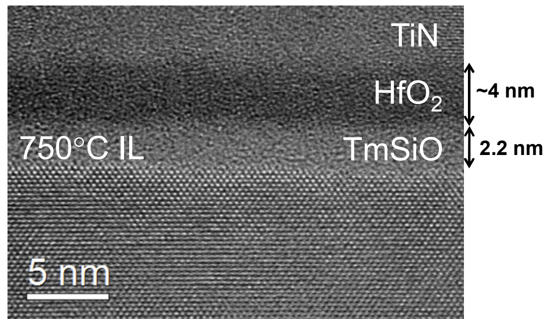

Figure 1. HRTEM image of $TmSiO/HfO_2$ gate stack with IL formed by post deposition anneal at 750°C.

shift of the Tm $4d_{5/2}$ peak position from 175.6 eV for sample with IL processed by post deposition anneal (PDA) at 550°C towards higher binding energies (BE) of 175.8 eV and 176.4 eV for 650°C and 750°C PDA samples, respectively (Fig. 2(a)). The latter is in agreement with forming a thicker IL (from 0.9 nm to 2.1 nm) as annealing temperature increases, and in line with that reported in the literature [7,8].

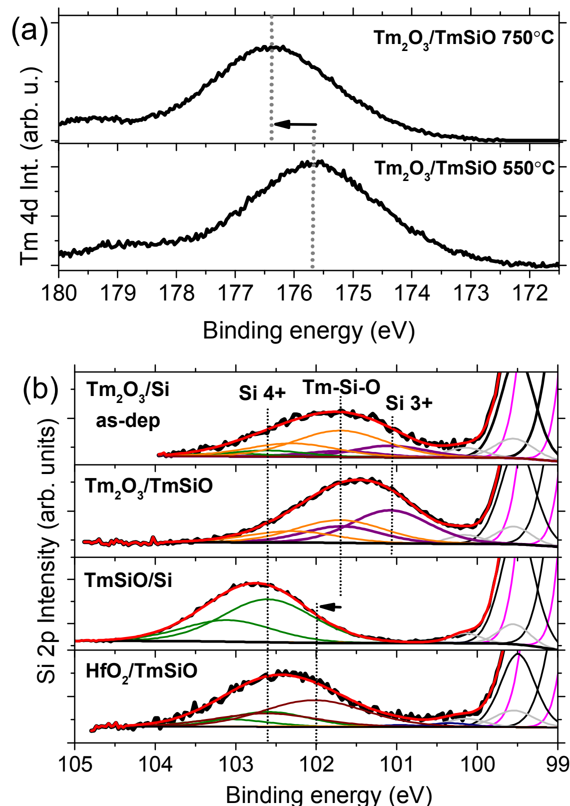

Figure 2. (a) XPS Tm 4d CLs for Tm_2O_3/TmSiO; (b) Si 2p CLs for $TmSiO/HfO_2$ stack with reference CLs for as-deposited Tm_2O_3/Si & TmSiO/Si (550°C PDA).

The XPS Si 2p spectrum is used in this study to resolve different bonds and the oxidation states of Si atoms in the IL via the chemical shift of the Si 2p core level. The spectrum is decomposed into the Si $2p_{1/2}$ and Si $2p_{3/2}$ spin-orbit partner lines (Fig. 2(b)). The spin-orbit splitting and area ratio of 0.6 eV and 1:2 respectively were fixed for the fit [9]. The high BE side sub-peak from the mean substrate Si $2p^0$ peak (Si $2p_{3/2}$ @ 98.60 eV) gives a signature of the IL. It is evident from Fig. 2(b) that the centroid of the sub-peak is closest to the Si $2p^0$ substrate peak for the sample after 550°C PDA and before etching of the remaining Tm_2O_3 on top. The presence of the Tm-Si-O bond can be de-convoluted from the spectra at the chemical shift of 3.1 eV prior etching, and at 3.4 eV after etching and deposition of HfO_2. The chemical shift of 3.6 eV has been reported for TmSiO from the Si 2s spectra [10]. Interestingly, a strong presence of the Si 3+ oxidation state at 2.48 eV chemical shift [9] is found, in particular for the stack processed at 550°C PDA. As the annealing temperature increases to 750°C, the intensity of Tm-Si-O component increases and Si 3+ component diminishes (not shown). The Si 4+ (i.e. SiO_2) has a strong presence only in uncapped ILs likely to be due to their exposure to air prior XPS measurements.

4. Conclusion

We have given a quantitative structural analysis of the $TmSiO/HfO_2$ interface using XPS, TEM and EELS techniques. The gate stacks were processed using three post deposition annealing temperatures from 550°C to 750°C. The best-scaled stack reveals a graded interface with a strong SiOx component.

Acknowledgements

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