**Rare-earth oxide interfacial layer for sub-nm EOT CMOS technology**

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Aggressive downscaling of CMOS device chips, following Moore’s law, means that transistor sizes are in the nanometer scale range. As processors shrink in size, energy waste due to leakage current becomes a major issue. State-of-the-art CMOS technology employs HfO2 due to its high dielectric constant (> 20) and ability to achieve suitable n- and p-MOSFET threshold voltages [1-4]. Hf-based dielectric is deposited on top of sub-nm chemical oxide (SiOx) or oxynitride interfacial layer (IL), whose thickness can be controlled using different oxidation methods and carefully designed scavenging steps [2,3]. A general trend has been observed of strong degradation of the inversion layer mobility with decreased IL thickness, independent of the method used. Even stronger mobility and reliability degradation occurs if no IL is employed [4]. It has been demonstrated recently [1] that rare-earth thulium silicate is a contender for forming an adequate IL and can be integrated with the HfO2 gate oxide layer. However, there is no current understanding of the physical properties of this interface, which can lead to the best-scaled gate stack. In this paper, a quantitative structural analysis of the TmSiO/HfO2 interface using x-ray photoelectron spectroscopy is presented. The gate stacks were processed using atomic layer deposition and three post deposition annealing temperatures from 550 °C to 750 °C. The best-scaled stack shows evidence of a graded IL with strong Si 3+ sub-oxide component.

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