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First results on the ATLAS HL-LHC H35DEMO pixel prototype

Content :

The H35DEMO is a prototype ASIC aimed at proving that High Voltage-CMOS (HV-CMOS) sensor technologies can be qualified as tracking detectors for harsh working environments such as that of the High Luminosity-LHC (HL-LHC). The prototype is in the 0.35 μm HV-CMOS process from ams and was fabricated through an engineering run in which wafers with four different substrate resistivities that range from the standard value of 20 Ω·cm to a high value of 1k Ω·cm were used as a solution to increase the depletion region of the sensor. To allow studying yield issues, the prototype has a large area of 24.40 mm x 18.49 mm that is divided into four independent matrices with a few thousand pixels each. Two of the matrices can be read out using a readout ASIC only, whilst the other two are completely monolithic. All the matrices can be bump bonded or glued to the FE-I4 ASIC for readout in a one-to-one connection. A few test structures for sensor characterization were also integrated in the chip.

A new experimental set-up based on a custom made pcb and the ZC706 evaluation board from Xilinx has been developed by the Liverpool group. The set-up allows measuring one of the monolithic matrices by using the on-chip digital readout block. This matrix has nMOS only discriminators with and without time-walking compensation inside the pixel area. Features such as gain, speed and sensitivity to a radioactive source have been tested, showing that measured results are in good agreement with Cadence simulations. TCT and edge-TCT measurements on back biased thinned chips have allowed us to analyze the benefits of this type of biasing on charge collection effects. The first measured results on the H35DEMO prototype will be presented at the workshop.

Primary authors : Mr. POWELL, Sam (University of Liverpool) ; Dr. VOSSEBELD, Joost (University of Liverpool) ; Dr. VILELLA FIGUERAS, Eva (University of Liverpool) ; Dr. CASANOVA, Raimon (IFAE) ; Prof. CASSE, Gianluigi (University of Liverpool and FBK) ; Prof. PERIC, Ivan (KIT Karlsruhe Germany)

Co-authors :

Presenter : Dr. VILELLA FIGUERAS, Eva (University of Liverpool)

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