A Cost-Effective Fault Tolerance Technique for Functional TSV in 3D-ICs

Ravi Teja Reddy P, Amit Acharyya, *Member, IEEE*, Saqib Khursheed, *Member, IEEE*

***Abstract*—Regular and redundant Through-silicon via (TSV) interconnects are used in fault tolerance techniques of 3D-IC. However, the fabrication process of TSVs results in defects which reduces the yield and reliability of TSVs. On the other hand, each TSV is associated with significant amount of on-chip area overhead. Therefore unlike the state-of-the art fault tolerance architectures, here we propose Time Division Multiplexing Access (TDMA) based fault tolerance technique without using any redundant TSVs, which reduces the area overhead and enhances the yield. In the proposed technique by means of TDMA we re-route the signal through defect-free TSV. Subsequently, architecture based on proposed technique has been designed, evaluated and validated on logic-on-logic 3D IWLS'05 benchmark circuits using 130-nm technology node. The proposed technique is found to reduce area overhead by 28.70 – 40.60% compare to the state-of-the-art architectures and resulting a yield of 98.9 - 99.8%.**

***Index Terms*—3D-IC, Through-silicon via (TSV), Fault Tolerance, Time Division Multiplexing Access (TDMA), Yield.**

I. INTRODUCTION

The smaller nodes of CMOS technology are leading to new levels of efficiency in transistor density, low power, form factor and limits the interconnect performance with increased delay. 3D-IC Through-silicon via [1] consisting of vertical interlayer communication instead of long horizontal wires results in reduction of interconnect length and thus can improve the system performance. There are challenges which need to be addressed such as reliability and yield are major concerns when migrating from traditional IC design to 3D IC design [2-6]. TSV in 3D ICs can have latent defects due to thermal stress, such as crack in TSVs, delamination between TSVs and landing pad, as well as open and short defects increases RC that can lead to signal delay and malfunctioning of the system. Reliability of 3D-IC is degraded by thermal stress during its operation and fabrication process [2-4] resulting in defects and affecting the yield of 3D-IC [5-6] adversely. The existing methods for improving yield and reliability [7-13] of 3D-IC as well as developing new testing methods [14-17] are associated with using redundant TSVs, as well as grouping the regular TSVs with redundant TSVs and respective logic blocks for normal operation in the presence of defective TSVs. Zhao *et. al.* [7] presented an exhaustive search algorithm for the optimum grouping ratio of regular and redundant TSVs to improve the yield. The increase in the number of redundant TSV results in an area overhead of 4% - 17% and the entire system may fail if the number of defective TSVs outnumbers the redundant TSVs. Similarly [8-10] uses the idea of redundant TSVs to improve the yield by repairing the defective TSV. On the other hand, to improve the repair efficiency and reliability, [11] uses a dedicated switch for repair of TSV across the groups. An on-chip processor [12] is used for online fault detection, recovery and to improve in-field reliability of TSV but at the expense of high cost and area overhead. An improved online fault tolerance technique for fault detection and recovery was proposed in [13]. However it has the penalty in terms of area overhead owing to the fact that the number of TSV increases due to the inclusion of redundant TSV. The additional TSV may be added as required, for example on chip inductor [34] and for thermal mitigation [37].

We address in this paper, the fore-mentioned challenges by proposing a novel fault tolerant technique with low hardware complexity and high yield without using redundant TSV. The principle of the proposed architecture is based on Time Division Multiplexing Access (TDMA). TDMA assigns time slot for each TSV present in the design and provides necessary control signals for inter-die communication and testing of the individual TSV. Unlike the existing techniques [13-17], the proposed technique brings flexibility of using configurable testing where voltage changes attributed by the defective TSV are compared with variable reference voltage and it can measure the delay in high resolution (nsec to psec). The process flow of the proposed methodology involves grouping of TSVs, detecting TSV defects and re-routing the signal through defect-free TSV without the need of using redundant TSV. Furthermore the proposed technique switches off the signal path through defective TSV so that it does not lead to thermal stress, electro-migration affect and degradation of reliability.

This work is supported partly under grants-in-aid for research project titled "Indigenous Hybrid Sensor and Processing Integration Technology Development for Defence System on Chip Applications" from Defence Research and Development Organization, Govt. of India under grant No. ERIP/ER/RIC/2015-6/10/M01.
RTRP would like to acknowledge Visvesvaraya PhD fellowship under Ministry of Electronics and Information Technology (Meity), Govt. of India for funding his Ph.D. AA would like to acknowledge Visvesvaraya Young Faculty fellowship from Meity, Govt. of India. SK would like to acknowledge Department of Electrical Engineering and Electronics, University of Liverpool, U.K.
Ravi Teja Reddy P, Amit Acharyya, are with the Department of Electrical Engineering, Indian Institute of Technology, Hyderabad, India (e-mails: {ee15resch11006, amit_acharyya}@iith.ac.in).
S. Khursheed is with the Department of Electrical Engineering and Electronics, University of Liverpool, U.K. (e-mail: S.Khursheed@liverpool.ac.uk).

II. PROPOSED FAULT TOLERANCE TECHNIQUE

A. *Motivational Background*

Integration of heterogeneous technology such as logic, memory, analog device, RF circuits, processors and MEMS can be realized using 3D-IC where logic-on-logic/memory and memory on memory communication takes place using the concept of regular and redundant TSV [13]. On the other hand, recently High Speed Time Division Multiplexing (HSTDM) method was introduced in [18] to resolve the high trafficking issue in inter-FPGA communication without affecting the delay. It was shown that very high inter-FPGA communication efficiency can be achieved by introducing this time-division multiplexing technique that would reduce the overall interconnect hardware complexity, thereby reducing overall area and power consumption. It was also stated in [18] that with strict time-budgeting and user-constraints no extra delay was incurred due to this newly introduced HSTDM technique [18]. TSVs can transfer data at very high clock frequency in the range of Giga hertz [19], used as high speed interconnects in [20] and they are used in 3D NOC as inter-die communication interface in stacked 3D-IC [21]. To reduce the test time and TSV count a two-dimensional time-division multiplexing 3D–SoC testing was proposed [22]. From contributions of [19-22] we can exploit the high speed characteristics of TSV to design TDMA based 3D-IC. The design operating at high clock frequency leads to high data rate transfer for inter-die communication and due to this no additional delay induced on signal path. Furthermore proposed TDMA design assigns time slots to regular TSVs and this in turn avoids using redundant TSVs for fault tolerance, thereby decreasing the area overhead and enhances the yield.

In the light of above mentioned facts and motivated by the contributions of [13] and [18-22], we envisage here a hybrid 3D IC TSV design strategy where logic-on-logic/memory and memory-on-memory still would use the state-of-the art redundant TSV concept as well as our proposed technique based on Time-Division Multiplexing Access (TDMA) model that will be discussed next.

B. *Proposed Technique*

Fig. 1 shows the proposed fault tolerance technique. It comprises of three modules - TDMA, Testing, and Routing. These proposed modules are used for-

1. Detecting all the defective TSV.
2. Re-route the signal through defect free TSV

As per the widely used state-of-the art techniques, a design may comprise of 'm' number of TSVs which can be divided into groups at the design time [7]. Based on the number of TSVs per group, we propose the respective *TDMA*, *Testing* and *Routing* modules as mentioned above as well as depicted in Fig. 1. Here, as an illustration, one single such group of four TSVs is shown in Fig 1 and is described next. TDMA enables the joint utilization of a common communication channel by a plurality of independent message sources without mutual interference among them [23]. For example in Fig. 1, input signal 1 (TSV1) uses time slot 1, input signal 2 (TSV2) uses time slot 2, etc. until the last input signal. Then it starts again in a repetitive pattern, until the input signals are ended and that slot becomes free or assigned to another input signals (TSVs).

The proposed TDMA module in this context of detecting the defective TSVs present on die1 (Fig. 1), assigns time slot for each TSV present in the design and provides necessary control signals for inter-die communication and testing the individual TSV. It consists of Multiplexers, De-multiplexers, Oscillator and counter. Inputs are *Testmode*, *Enable* (*En*) and signal lines for respective TSVs. The clock is generated by the oscillator on die1 when *En* is active high, counter receives the clock signal for generating the required selection signal for mux1, mux2, demux1, demux6 on die1 and demux1 on die-2. Mux1 on die1 is 4:1 which is used to select particular input signal lines based on the selection signal provided by the counter. Mux2 on die1 is a 2:1 which makes the entire system to work in normal mode or *Testmode* (Fig. 1). *Testmode* could be visualized as the external signal which is used as a selection line for mux2 (in Fig. 1). If the *Testmode* = 0 output of mux2 is any one of the input signal lines else output is *Testmodebar*. Demux1 on die1 is used for passing input signal lines and *Testmodebar* to the Routing module based on the selection lines. Similarly demux6 on die1 and demux1 on die2 are 1:4 type which takes *Testresult* (Fig. 1) from the comparator as input, selection lines from the TDMA module and the output of these de-multiplexers (demuxes as shown in Fig. 1) are selection lines for the demuxes in the Routing modules on die1 and die2 respectively. Fig. 2 provides the algorithm of the proposed fault tolerance technique.

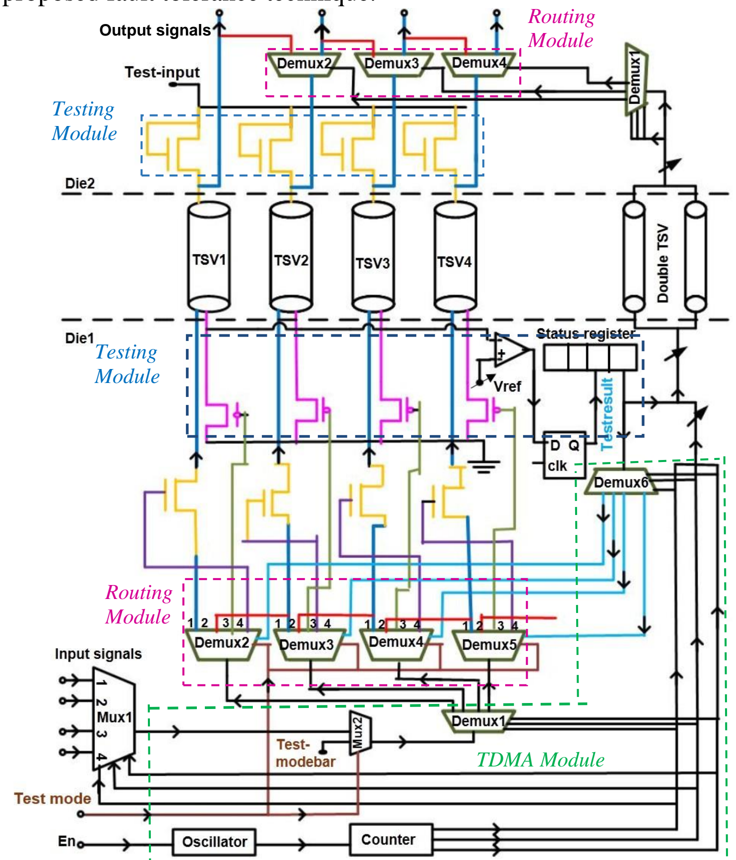


Fig. 1. Architecture of the proposed technique

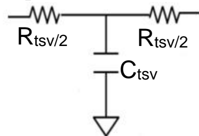
Algorithm Proposed Fault Tolerance Technique (PFTT)
Input: Number of Regular TSV ‘m’
Output: PFTT with *TDMA*, *Testing* and *Routing* modules

1 Grouping of Regular TSV with ‘n’ TSV per group
2 Building of *TDMA*, *Testing* and *Routing* modules
% *Testing of TSVs for fault detection*
3 **While** *Testmode* = 1 **do**
4 **for** I = 1 to n **do**
5 Switch ON PMOS and test TSV
6 Compare V_{ref} with V_{TSV}
7 *Testresult* is passed to the Routing Module
% *Re-routing of signal through defective-free TSVs*
8 **If** (*Testresult* = 1)
9 Cut-off the signaling path of defective TSV (NMOS off)
10 Re-route the signal
11 **end if**
12 **end for**
13 **end while**
% *Normal mode of operation*
14 **If** (*Testmode* = 0 and *Testresult* = 0) // Normal mode
15 Pass input signals from die1 to output signals on die2
16 **end if**
17 Return Proposed fault tolerance technique

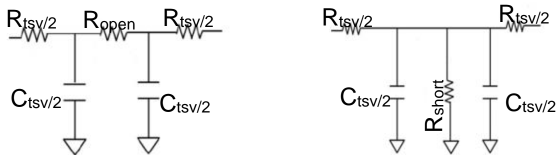
Fig. 2. Algorithm of the proposed fault-tolerance technique

B. 1 Detection of defective TSVs

The proposed Testing module (Fig. 1) tests each TSV in a group. A pull-up network on die2 and pull-down network on die1 are used for testing and test results are observed at the flip flop output and stored in TSV status register (shown in Fig. 4 and 5) on die1. Subsequently, test results are passed to the routing module on die1 and die2 through double TSV interconnect. A double TSV interconnect [5] is used for propagation of signals between dies to pass selection lines and *Testresult* for demux1 of die2 from die1. Proposed method is demonstrated using double TSV between dies, however it can be used with single TSV [30, 31] just as well. The *Testing* module uses delay test to distinguish between faulty and fault free TSVs where each TSV is tested for void/delamination defect and short-to-substrate defect types [35, 36]. If the TSV is defective, signal is re-routed through the defect-free TSV (second row in Table-I and Fig. 1), otherwise it takes the normal path (first row in Table-I and Fig. 1). A TSV can be viewed as a transmission line T-model [24], where R_{tsv} and C_{tsv} indicate TSV resistance and capacitance respectively as shown in Fig. 3(a) [24].



(a) TSV T-model [24]



(b) Void/delamination defect [17] (c) Short to substrate defect [14]

Fig. 3. Equivalent circuit models for TSV

The equivalent electrical model of a void/delamination defect is shown in Fig. 3(b) [17], R_{open} represents the open circuit defect which increases the signal delay. The short-to-substrate defect is a resistive path between TSV to substrate is shown in Fig. 3(c) [14]. The resistance R_{tsv} and capacitance C_{tsv} are taken as 200 mΩ and 200 fF respectively, based on the models presented in [24]. Signal propagation properties of TSV would be affected due to either the TSV fabrication process or die stacking leading to deterioration of chip speed or intended functionality. Postbond test helps to find the defects that occur due to the process variation steps involved in the stacking process and it ensures that chip is operating according to the timing specifications provided at the design time [25]. Hence delay testing of TSVs is necessary to retain at-speed characteristics of the system.

The time constant gives the delay across a defect free TSV which is extremely small. Due to the presence of defects, RC value increases which in turn violates the timing specification resulting in malfunctioning of the system. Fig. 4 shows testing of single TSV in the Testing module. Here, pull-up network is the N-MOS acting as a resistive circuit and pull-down network is P-MOS acting as a resistive load which is ON during testing. The voltage divider circuit is used to measure the varied resistance of the TSV due to defects and the output voltage V_{tsv} function of resistance ratio of on-resistance of N-MOS transistor (R*pull-up*), on-resistance of P-MOS transistor (R*pull-down*), the resistance of TSV (R_{tsv}) and the capacitance (C_{tsv}). To detect void and delamination defect, the TSV in Fig. 4 is replaced by equivalent open circuit defect as shown in Fig. 3(b). Similarly to detect short-to-substrate defect, TSV in Fig. 4 is replaced by with equivalent short circuit defect as shown in Fig. 3(c).

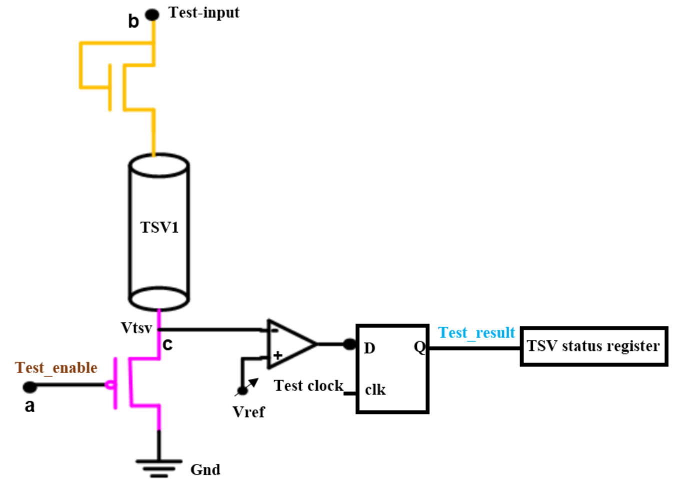


Fig. 4. Voltage divider circuit for testing of TSV

To test the TSV, closed-loop current path will be formed by setting *Testmode* high to turn ON the die-1 P-MOS transistor (third row in Table-I and Fig. 4) and based on the fore-mentioned method, all the TSVs can be tested under the control of the proposed TDMA module without increase in the peak current consumption, as a result this testing method does not lead to thermal stress and reliability degradation. The reference voltage V_{ref} is compared with V_{tsv} for the measurement of the increase in the delay due to the defective TSV. To illustrate reference voltage V_{ref} is set to 50% of Vdd

[13] and it can also be selected based on the TSV delay ($\Delta R_{tsv}C_{tsv}$) corresponding to the change in TSV resistance (ΔR_{tsv}) [25]. The later approach is useful to the designs where the timing paths of the designs can have delay and retain its functionality in accordance with the design specification. TSV open circuit resistance and short circuit resistance are function of V_{ref} and signal capture time, as well as effected by technology in smaller nodes and process variation [26]. Based on the timing specification of the design and by changing the V_{ref}, delay across TSV can be determined. The output of comparator is high if $V_{tsv} < V_{ref}$ indicates TSV delay is larger than the expected delay and turning-off the signal path through defective TSV (fourth row in Table-I and Fig. 1). The output of the comparator is low if $V_{tsv} \geq V_{ref}$ implies TSV is defect-free.

B. 2 Re-route through defect-free TSV

The proposed Routing module (Fig. 1) present on both die1 and die2, consists of De-Multiplexers that re-route the signals through defect-free TSVs. It is configured by the signals provided by *Testing* module (as discussed above) and control signals generated by the TDMA module (as discussed before). The routing module of die1 consists of four 1:4 type de-multiplexers that receive the input signals from the demux1 of the *TDMA* module (Fig. 1), selection lines from the *Testmode* and *Testresult* (Fig. 1) of the comparator and respective output signals functionality is explained in Table I. *Testmode* is the input signal used for testing of TSVs, when *Testmode* is high indicates die is under test, else die is under normal operation. If *Testresult* is high indicates TSV is defective and *Testresult* low implies TSV is defect-free. The routing module of die2 consists of 1:2 type de-multiplexers that receive the input signals from the TSVs and selection lines are provided by demux1 of die2.

B. 3 Illustration of proposed technique

Fig. 5 shows how a signal through defective TSV is re-routed via defect-free TSV. For illustration TSV1 is considered as defective. Input signal1 of TSV1 is passed from die1 to die2 based on the *Testresult*, *Testmode* and control lines generated from *TDMA* module. If *Testmode* and control line are active low, input signal1 from mux1 is passed to demux1 via mux2 as shown in Fig. 5. From demux1 it passes to demux2 and based on the selection lines it passes to the output signal1 of die2 via TSV1 or TSV2. If *Testmode* and *Testresult* are active low, output1 of demux2 passed to TSV1 (shown in Fig. 5) and received on die2 output signal1. If *Testmode* is active low and *Testresult* active high, output2 of demux2 is passed to TSV2 (shown in Fig 5). On die2 the signal of TSV2 is passed to demux and further demux on die2 passes the output signal1 to its original TSV1 path via TSV2, (shown in Fig. 5) based on selection line (*Testresult*) obtained from double TSV. To switch over from defective to defect-free of a single TSV requires two De-Multiplexers each on die1 and die2, control lines generated from the *TDMA* module and *Testresult*. The extra hardware incurred to switch over for a group of TSV is included in Table-VII of section III D.

C. Generalized Model and Scalability

By analyzing the detailed hardware architecture with respect to the illustration in Fig. 1, it can be scaled to the generic design with 'm' number of TSV per design and 'n' number of TSVs per group resulting in a design consisting of 'n' input and output signal lines for each group. For each group it consists of *TDMA*, *Routing* and *Testing* modules. All these modules on both dies requires one n-to-1 multiplexer, one 2-to-1 multiplexer, three 1-to-n de-multiplexers, $\log_2 [n]$ bit counter, 'n' 1-to-4 de-multiplexers, 'n' 1-to-2 de-multiplexers, n-bit TSV status register , one comparator, one flip flop, 'n' N-MOS and P-MOS as a pull-up and pull-down networks respectively.

TABLE I
OUTPUT LINES OF DE-MUX IN ROUTING MODULE

Testmode	Testresult	Output functionality	Symbol
0	0	**Normal path to TSV**	▲
0	1	**Re-routing Path**	●
1	0	**For switching On P-MOS**	▰
1	1	**For switching Off N-MOS**	◆

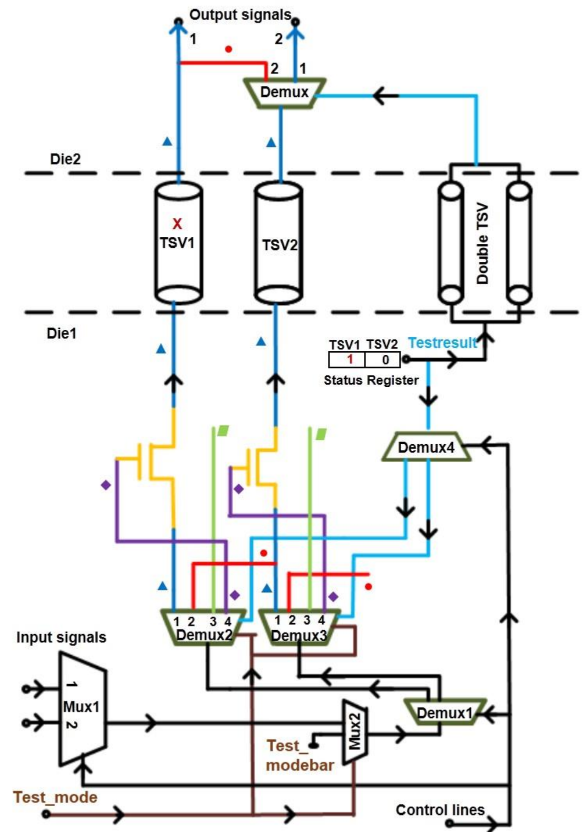


Fig. 5. Switch over of signal for a single TSV

III. SIMULATION RESULTS

A simulation flow of the proposed fault tolerance technique is presented in Fig. 6. Four sets of simulations are conducted to validate and evaluate the proposed technique. The first set of simulation (section A) functionally validates the *Routing* and *TDMA* modules through RTL model implementation of fault tolerance technique using Modelsim. The second set of simulation (section B) validates the *Testing* module through Cadence Virtuoso for open and short circuit defects. Section C performs the yield analysis, which is evaluated using

MATLAB. Section D analyses the hardware cost and power consumption for the added hardware using Synopsys Design Compiler. The last set of simulation (section E) analyses signal integrity of the proposed technique.

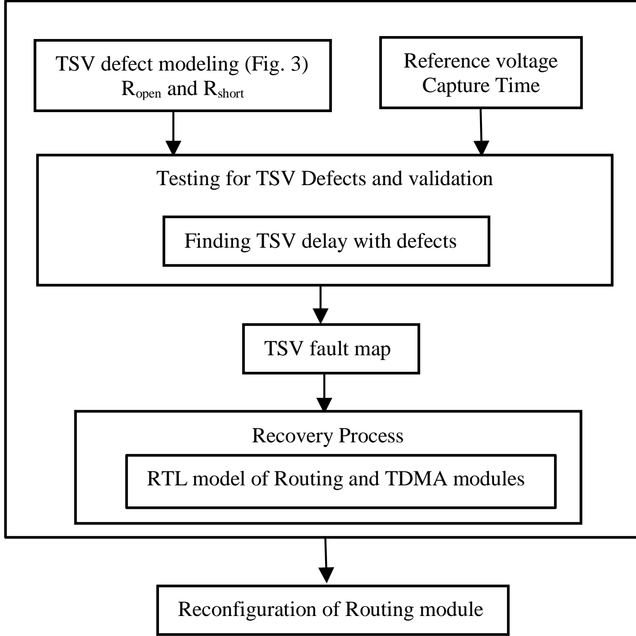


Fig. 6. Simulation flow of the proposed fault tolerance technique

A. Validation of TDMA and Routing Modules

Simulations are done to functionally validate the routing of signals through defect-free TSV and generating the control signals from the *TDMA* module using Modelsim. For illustration purpose simulation is done for the architecture shown in Fig. 1, considering one defective TSV (*TSV1*) in group of four TSVs and Fig. 7 shows simulation results for the same for each clock cycle. Initially we analyze the simulation for TSV1 and then generalize for remaining TSVs.

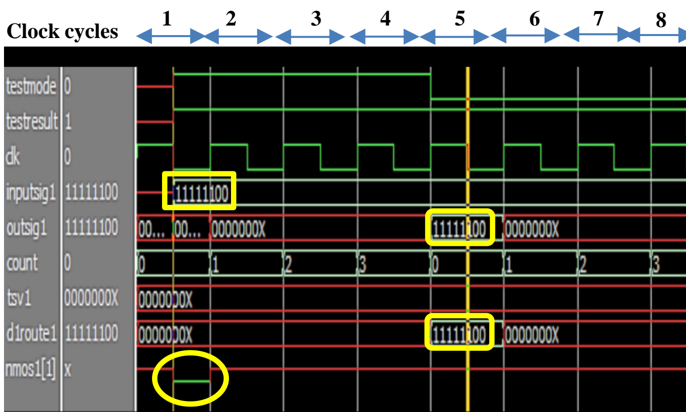
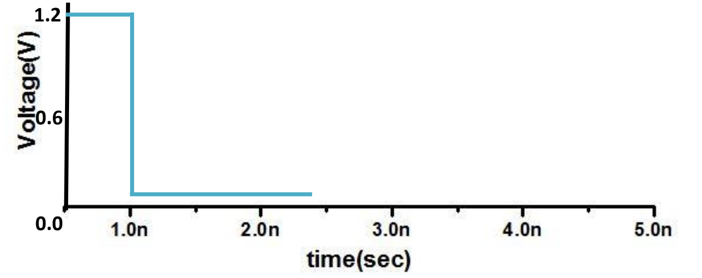


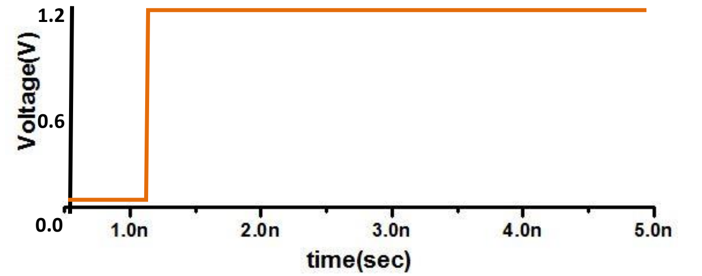
Fig. 7. Functional Validation of TDMA and Routing Modules

As shown in Fig. 7, in the first clock cycle TDMA module generates *count*=0 and assigns time slot for TSV1. *Testmode*=1 and *Testresult (TSV1)* =1 indicate TSV1 is faulty and its normal path (tsv1 signal) should be switched-off, this is done by applying active low signal to *nmos1* (as shown in Fig. 7 with circle). Subsequently *count* signal assigns time slots for remaining TSVs. At the end of four clock cycles when count=0 it again assigns time slot for TSV1, with *Testmode*=0 and *Testresult (TSV1)* =1 inputsig1 (11111100) is re-routed to outsig1 (11111100) via d1route1 (11111100) as shown in fifth clock cycle of Fig. 7. From the waveform of Fig. 7 one can conclude that for fault detection and re-routing of TSV1 requires 2 clock cycles, same holds for remaining TSVs. Overall, for a group 'm' regular TSV's this technique requires 'm' clock cycles for detecting and 'm' clock cycles for re-routing signal in the presence of defects. Therefore the proposed architecture requires '2m' clock cycles for fault detection and re-routing.

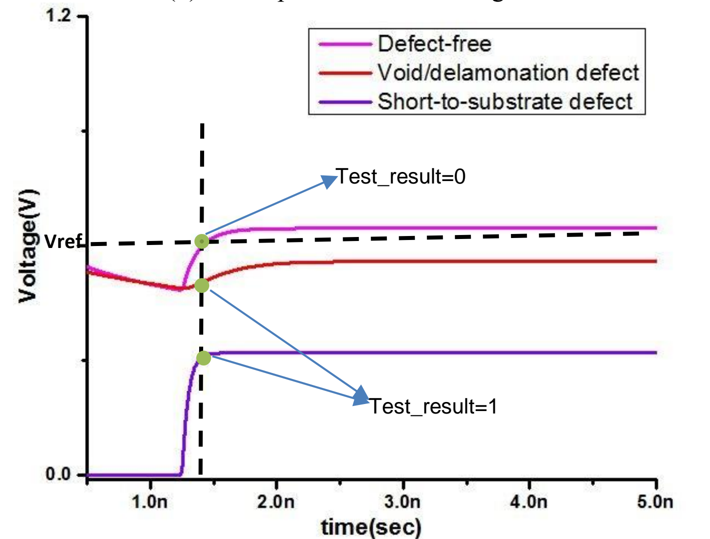
B. Validation of Testing Module



(a) Test enable at node 'a' of Fig. 4



(b) Test input at node 'b' of Fig. 4



(c) V_{tsv} at node 'c' and Test_result at node'Q' of Fig. 4

Fig. 8. Test pattern for detection of defects.

Simulation results are presented to verify the functionality of the *Testing* module (Fig. 8). These simulations employ electrical models of TSVs for void/delamination defect and short to substrate defect as shown in Fig. 3. The test circuits are modeled with Cadence Virtuoso using 65-nm gate library and all the simulations are carried out at 25°C. The defect free

TSVs resistance and capacitance are 200 mΩ and 200fF respectively [24]. The W/L size of transistor in both pull up and pull down network is taken as 2µm/180 nm, which is for both N-MOS and P-MOS respectively. We have performed analysis with a pulse input of 1.2V, active low test enable signal and 0.7 GHz test frequency (signal capture time at 1.42 nsec). Fig. 8 shows the detection of void/delamination and short-to-substrate defects with V_{ref} set to 50% of V_{dd}. The TSV R_{open} (Fig. 3(b)) increases due to void or delamination defect, as a result voltage at V_{tsv} is lower than the V_{ref} at a given signal capture time and therefore the test detects a faulty TSV with Test_result=1 (Fig. 8(c)). Similarly, in short-to-substrate defect R_{short} (Fig. 3(c)) forms a resistive path between TSV and substrate this leads to very low voltage levels at V_{tsv} compared to the V_{ref} as shown in Fig. 8(c).

TABLE II

RELATION BETWEEN V_{tsv} AND R_{tsv}

Void or Delamination Defect		Short-to-substrate defect	
Ropen (Ω)	Voltage at TSV end V_{tsv} (mV)	R_{short} (Ω)	Voltage at TSV end V_{tsv} (mV)
1K	546.3	500	310.1
2K	527.2	1K	380.0
3K	517.1	1.5K	409.6
4K	510.8	2K	431.6
5K	506.4	--	--
10K	489.3	--	--
50K	442.2	--	--

As R_{open} increases, voltage at the V_{tsv} decreases from the defect-free value of 600.4 mV at the capture time and delay in the RC circuit can be obtained by product of ΔR_{tsv} and C_{tsv}, a 1KΩ increase in R_{tsv} causes (1KΩ X 200 fF) 200psec delay. If the application required to detect 200 psec delay (ΔR_{tsv}=1K), then a V_{ref} of 546.3 mV is required shown in TABLE II and similarly we can detect 10 nsec delay (ΔR_{tsv}=50K) by a V_{ref} of 442.2 mV as shown in TABLE II. Simulation results show that testing module can find fault TSV with resolution of 200 psec to 10 nsec delay and in order to find short-to-substrate defect a V_{ref} of 310.1 mV is applied as shown in TABLE II. Finally, testing module gives high resolution test results.

C. *Yield Analysis*

If a design consists of “m” number of regular TSV, they are divided into “t” number of groups with a uniform group size of “n” and each group is independent of each other. Initially we obtain the yield of one group Y_{group}, then the overall yield of all “t” groups is Y_{total} can be obtained by multiplying all individual group yields, expressed as

$$Y_{total} = (Y_{group})^{t}$$

TSVs in a group are independent and has a uniform failure rate “p”. The maximum number of defective TSV for each group is “k”. The number of defective TSVs in a group follows binomial distribution [7], where X is a variable of defective TSV in a group and the probability of having x defective TSV can be expressed has

$$P(X = x) = {}^{n}C_{x}\, p^{x} (1-p)^{n-x}$$

Where ${}^{n}C_{x}$ gives various combinations of x defective TSV in a group of “n” number of TSVs. Therefore the overall yield of a group is

$$Y_{group} = \sum_{x=0}^{k} [{}^{n}C_{x}\, p^{x} (1-p)^{n-x}]$$

We have performed the yield analysis for the benchmark circuits [27] with uniform failure rate of 0.001 for illustrative purpose as shown in Table III. The total number of regular TSV for each design obtained from [28, 29]. The grouping ratio is taken according to [7, 13] without any redundant TSVs.

TABLE III

YIELD COMPARISON

Circuits	Regular TSV Number (m)	Existing[13]			Proposed
		n	k	Yield (%)	Yield(%) with n = 4 and k = 1
Aes-core	1362	80	2	99.87	99.80
Ethernet	3782	80	2	99.64	99.43
Des-perf	3678	80	2	99.65	99.45
Vga-lcd	7356	240	3	99.64	98.90
Net-card	9112	240	3	99.56	98.64
FFT	2100	-	-	-	99.69
Cf_rca	1454	-	-	-	99.78

D. *Evaluation of Hardware Cost and Power*

The area overhead due to *TDMA*, *Testing*, and *Routing* modules on both dies of the proposed technique can be computed as follows:

$$\begin{aligned} Area_{overhead} &= A_{Routing} + A_{TDMA} + A_{Testing} + A_{Double\ TSV} \\ &= n\,[Demux_{1\text{-}to\text{-}4}] + \log_2[n]\text{-bit counter} \\ &\quad + \text{One } Mux_{n\text{-}to\text{-}1} + \text{One } Mux_{2\text{-}to\text{-}1} + \text{Three De-}mux_{1\text{-}to\text{-}n} \\ &\quad + \text{One Comparator} + 1\text{flipflop} + n\,\{\text{N-MOS} + \text{P-MOS}\} \\ &\quad + A_{Double\ TSV} + n\text{-bit TSV status register} \qquad (1) \end{aligned}$$

The design is implemented in Verilog Hardware Description Language [HDL] and its cost effectiveness is evaluated on logic-on-logic 3D benchmark design from IWLS 2005 [27]. The proposed fault tolerance technique is synthesized using Synopsys Design Compiler at 130nm. Table IV and V shows the hardware cost in terms of area overhead for respective benchmark circuits and the total number of regular TSVs for each design obtained from [28, 29]. It can be noted from Table-IV and V that 28.70 – 40.60% reduction in area overhead is achieved, compared to the existing technique. Similarly we have compared area overhead of the proposed fault tolerance technique with [30] in TABLE VIII by replacing double TSV interconnect in Fig. 1 with single TSV, resulting in 49.28% to 75.19% compared to UAGD [30] . The power overhead (included dynamic and leakage) due the proposed technique on the various benchmark circuits at 100MHz is shown in TABLE VI.

TABLE IV

AREA OVERHEAD ANALYSIS

Circuits	Synthesis area overhead due to TDMA, Testing and Routing Modules/(µm)^2		
	Existing [13]	Proposed	% Area Overhead reduced
Aes-core	143007	101959	28.70
Ethernet	397080	282854	28.76
Des-perf	386190	275080	28.77
Vga-lcd	828748	549861	33.65
Net-card	1133868	681122	39.92
FFT	-	156975	-
Cf_rca	-	108836	-

TABLE V
AREA OVERHEAD ANALYSIS OF THE PROPOSED FAULT TOLERANCE TECHNIQUE

Circuits	Design Area (um)^2	Regular TSV number	Area overhead due to TDMA, Testing and Routing Modules /(μm)^2										
			Double TSV Structure		Detection/Testing module		Recovery/TDMA module		Routing module		Total Area		
			[13]	Proposed	[13]	Proposed	Existing [13]	Proposed	[13]	Proposed	[13]	Proposed	%reduc-tion
Aes-core	818750	1362	850	17000	16,857	16538.5	81,832	9923.10	28,874	39692.40	129264	83154	35.67
Ethernet	2858975	3782	2350	47300	46,809	45881.0	227,232	27528.6	80,178	110114.4	358920	230824	35.68
Des-perf	3428571	3678	2300	46000	45,522	44620.0	220,983	26772.0	77,974	107088.0	349079	224480	35.69
Vga-lcd	4400000	7356	1550	91950	89,934	89191.5	408,738	53514.9	252,311	214059.6	754857	448716	40.55
Net-card	28034722	9112	1900	113900	111,403	110483	506,310	66289.8	312,542	265159.2	935005	555832	40.60
FFT	1509619.9	2100	1300	26250	-	25462.4		15277.5	-	61110.00	-	128100	-
Cf_rca	686815.26	1454	900	18200	-	17654.0		10592.4	-	42369.60	-	88816	-

TABLE VII
COMPARISON BETWEEN PROPOSED TECHNIQUE AND [11, 12 AND 13] (REGULAR TSV NUMBER IS 1000)

Technique		Proposed Technique	Fault Tolerance [13]	TSV Repairing [11,12]
Objective		Detecting open and short to substrate defect	Detecting open and short to substrate defect	Repairing
COST	No. redundant TSV	N/A	25	128
	Routing	2000Demux	1000Mux	3000Mux
	TDMA (Recovery)	2 Mux+ 1 counter+ 2 Demux	13*Signal line counter +13*Fault TSV adder +13*comp +3025*FF	On-chip microprocessor + Router configuration block
	Testing	1000 nMOS+ 1000 pMOS+ 1comparator+ Status register + 1 flip-flop	1025*Nand + 1025*FF	On-chip test block

A comparison is made with state of the art techniques [11-13] as shown in Table VII. For illustration purpose regular number of TSV is considered as 1000. Methods proposed in [11, 12] uses a redundant TSV concept, results in large area overhead as the routing resources uses more number of muxes and on-chip processor for recovery. The idea presented in [13] uses redundant TSVs for routing, resulting in more hardware complexity in recovery and routing blocks. In the proposed work it does not use any redundant TSVs as well as the TDMA and Testing modules are of very low complexity to that of [13]. Here we can ignore the number of N-MOS and P-MOS transistors to that of a number of N-MOS and P-MOS transistors required to design a single nand gate, flip-flop and adder in [13]. So this technique outweighs the existing techniques due to its low hardware complexity.

E. *Signal integrity*

a) Crosstalk

TSV-TSV coupling is one of major signal integrity characteristic in 3D-ICs. TSV-TSV coupling forms capacitive coupling network and causes a coupling noise between two adjacent TSVs. TSV-TSV coupling paths includes TSV copper, liner layer, silicon substrate and I/O drivers. TSV coupling is also affected by the neighboring and non-neighboring aggressors as shown in Fig. 10. Therefore, a signal path that includes TSVs can suffer from significant cross talk in 3-D ICs. We have taken TSV-TSV coupling model of [32] as shown in Fig. 9 and incorporated in between two TSVs of the proposed fault tolerance technique as shown in Fig. 10. We have performed the SPICE simulation using 65nm technology and equations for capacitance (liner, silicon substrate and bump) and resistance (TSV and silicon substrate) are obtained from reference [32, 33]. The design rules used in the equations are shown in TABLE IX.

TABLE VI
POWER OVERHEAD OF THE PROPOSED TECHNIQUE

Circuits	Without proposed Technique (mW)	With proposed Technique (mW)	% Overhead
Aes-core	6.39	8.07	26.27
Ethernet	25.90	30.58	18.06
Des-perf	37.16	41.71	12.24
Vga-lcd	47.68	56.79	19.09
Net-card	303.85	315.13	3.70
FFT	16.36	18.95	15.80
Cf_rca	7.44	9.24	24.20

We perform the cross talk analysis in two cases:

Case 1: We apply simultaneous input signals at Port 1, 3 and 4 of TSVs as shown in Fig. 10 and observe the crosstalk voltage at port 6 of TSV2, this case is similar to the functionality (parallel communication) of the existing fault tolerance technique [13] of 3D-IC. The respective input signal and cross talk voltage observed at port6 are shown in Fig. 11(a) and Fig. 11(b) respectively.

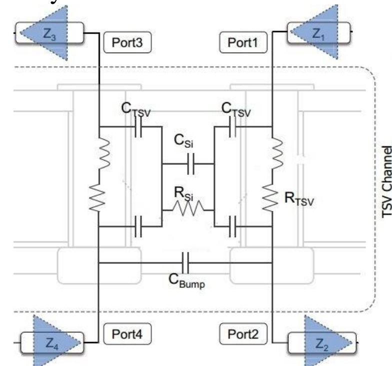


Fig. 9. TSV-TSV Coupling model [32].

TABLE VIII
AREA OVERHEAD ANALYSIS OF THE PROPOSED FAULT TOLERANCE TECHNIQUE IN $(\mu m)^2$

Test bench	#TSV	Yield	Proposed @130nm				NN[30] @45nm		DAGD[30] @45nm		UAGD[30] @45nm	
			Yield	Spare TSV	Overall	Overall* Normalized	Spare TSV	Overall	Spare TSV	Overall	Spare TSV	Overall
Circuit-1	186	95	99.97	1150	14904	1788.48	13973	15373	7065	9600	4161	7198
Circuit-2	188	95	99.97	1175	15228	1827.36	9106	11269	4789	7710	1492	5002
Circuit-3	256	90	99.96	1600	20736	2488.32	10127	13412	5417	9541	1649	6389
Circuit-4	458	90	99.93	2850	36936	4432.32	25591	30341	13188	20003	3376	11768
Circuit-5	600	85	99.91	3750	48600	5832.00	23236	31102	13188	23601	7458	19538
Circuit-6	721	85	99.89	4500	58320	6998.40	29124	38303	15151	26797	4789	18098
Circuit-7	800	85	99.88	5000	64800	7776.00	35247	44740	20724	33308	14601	28830
Circuit-8	1157	80	99.83	7225	93636	11236.32	18605	38367	10990	33169	8321	33532
Circuit-9	1327	80	99.80	8275	107244	12869.28	20332	43730	12403	39004	10127	40400
Circuit-10	1849	80	99.72	11550	149688	17962.56	73712	97392	41056	72586	31479	67247

* Normalized to 45nm from 130nm and the normalization factor is $(45/130)^2$.

Case 2: We apply the input signals at port1 and 4 one after the other and observe the crosstalk voltage at port6 of TSV2 and this case is similar to that of the proposed TDMA approach. The respective crosstalk voltage at port6 due the input signal at ports are shown in Fig. 11(c) and Fig. 11(d).

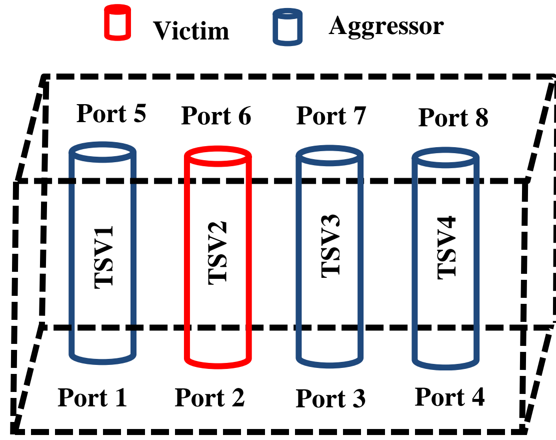
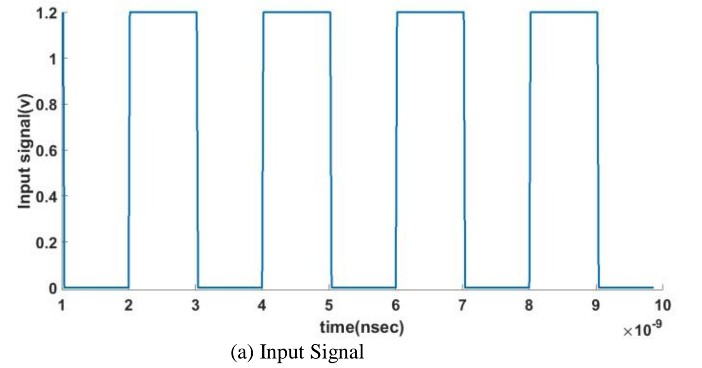


Fig. 10. Proposed Technique Crosstalk model

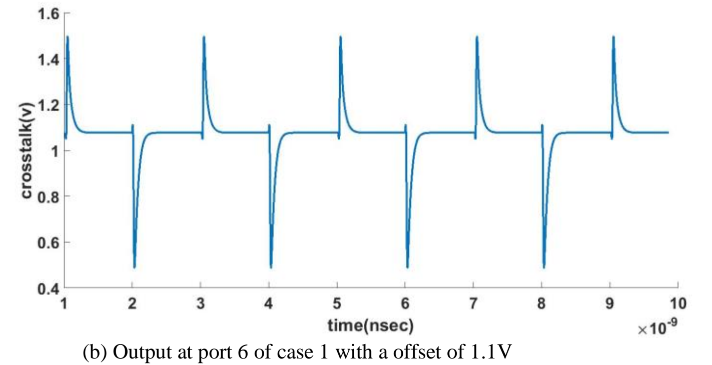
TABLE IX
DESIGN RULES USED IN THE CROSS TALK MODEL

Parameter	Value
TSV diameter	2.5µm
TSV Pitch	10 µm
Keep out Zone (KoZ)	0.5µm
Insulator thickness	0.5µm
Bump pad diameter	5.0µm
Bump height	10µm
Dielectric constant of silicon	11.9
Dielectric constant of liner	3.9
Dielectric constant of under fill	4
Process technology	65 nm
Supply voltage	1.2V
Frequency	500 MHz
Doping Concentration	10^{15} /cm^3

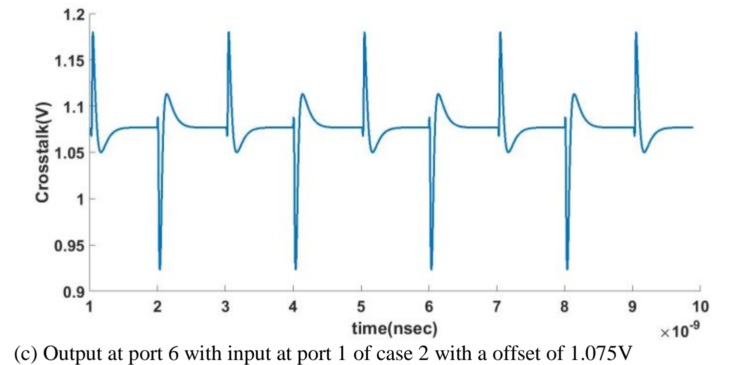
From *case1* of Fig. 11(b) we observed a crosstalk voltage of 400mV, which is not negligible because of single victim experiencing a cross talk from three aggressors simultaneously. In *case 2* of Fig. 11(c) we noticed a crosstalk voltage of 110mV due to the neighboring aggressor (TSV1) and less than *case 1*. In Fig. 11(d) we noticed a crosstalk voltage of 65mV due to the non-neighboring aggressor (TSV4) and less than neighboring aggressor (TSV1). From the above cases we conclude that the cross talk voltage of the proposed technique will be lower than the existing techniques and it can be further alleviated by TSV-TSV coupling optimization techniques proposed in [33].



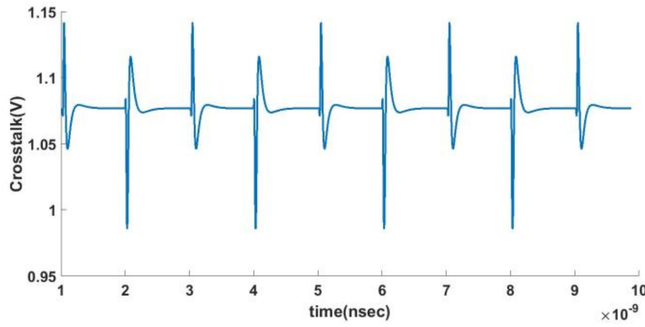
(a) Input Signal



(b) Output at port 6 of case 1 with a offset of 1.1V



(c) Output at port 6 with input at port 1 of case 2 with a offset of 1.075V



(d) Output at port 6 with input at port 4 of case 2 with a offset of 1.075V

Fig. 11. Crosstalk Voltage of the proposed model

b) Delay

The working environment of previous techniques [11-13] is a parallel communication between dies and whereas the proposed TDMA is sequential in nature. The TDMA environment reduces the performance in terms of number of clock cycles. We have performed the cost function analyses between number of clock cycles and frequency for various benchmark circuits as shown in Fig. 12. The performance of the TDMA technique can be enhanced by varying the operational frequency of TSVs and the same can be noticed in Fig. 12 at 500MHz. The proposed fault tolerance and existing techniques provides tradeoff between area overhead, yield, and signal integrity (crosstalk and delay). Finally, proposed technique is a lower area overhead fault tolerance technique, all most same yield is achieved, reduced cross talk and increased delay (number of clock cycles) compared to the existing techniques. However, delay can be reduced by increasing the clock frequency.

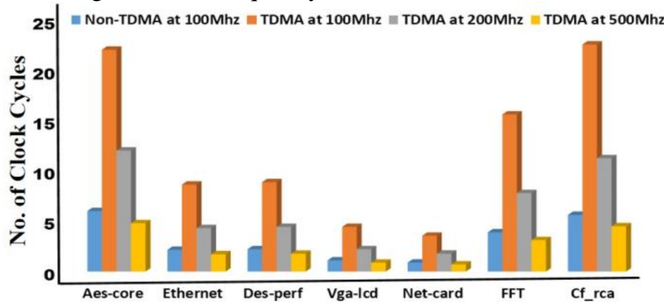


Fig. 12. Performance Trade-off

IV. CONCLUSION

We have proposed a novel fault tolerance technique with TDMA, Routing and Testing modules. Which is cost effective in terms of area overhead reduction (28.70 – 40.60%), high yield (98.9 - 99.8%), improved reliability and high resolution delay test for post bond testing. This technique outscores the existing architecture without using redundant TSVs and on-chip processors for fault tolerance. All these promising attributes can facilitate this architecture to be adopted in the 3D-IC designs.

Our future work is targeted for further enhancement of fault tolerance technique, by considering clustering effect [7] and polling mechanism to re-route the signal through neighboring group of TSVs.

ACKNOWLEDGMENT

Ravi Teja Reddy P thanks his colleagues Akbar, Mukthadar, Sisir Maity, and Shashank in the preparation of the manusscript.

REFERENCES

[1] Banerjee, K., Souri, S. J., Kapur, P., & Saraswat, K. C. (2001). 3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. *Proceedings of the IEEE*,*89*(5), 602-633.

[2] Trigg, A. D., Yu, L. H., Xiong, Y. Z., Lin, S. J., Kuo, C. C., Khan, N., ... & Shan, G. (2010, December). Design for reliability in via middle and via last 3-D chipstacks incorporating TSVs. In *Electronics Packaging Technology Conference (EPTC), 2010 12th* (pp. 328-332). IEEE.

[3] Lee, G., Kim, Y. H., Jeon, S. W., Byun, K. Y., & Kwon, D. (2011, May). Interfacial reliability and micropartial stress analysis between TSV and CPB through NIT and MSA. In *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)* (pp. 1436-1443). IEEE.

[4] Frank, T., Chappaz, C., Leduc, P., Arnaud, L., Moreau, S., Thuaire, A., ... & Anghel, L. (2010, December). Reliability approach of high density Through Silicon Via (TSV). In *Electronics Packaging Technology Conference (EPTC), 2010 12th* (pp. 321-324). IEEE.

[5] Miyakawa, N., Hashimoto, E., Maebashi, T., Nakamura, N., Sacho, Y., Nakayama, S., & Toyoda, S. (2008). Multilayer stacking technology using wafer-to-wafer stacked method. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, *4*(4), 20.

[6] Topol, A. W., La Tulipe, D. C., Shi, L., Alam, S. M., Frank, D. J., Steen, S. E., ... & Patel, J. (2005, December). Enabling SOI-based assembly technology for three-dimensional (3D) integrated circuits (ICs). In *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.* (pp. 352-355). IEEE.

[7] Zhao, Y., Khursheed, S., & Al-Hashimi, B. M. (2011, November). Cost-effective TSV grouping for yield improvement of 3D-ICs. In *2011 Asian Test Symposium* (pp. 201-206). IEEE.

[8] Loi, I., Mitra, S., Lee, T. H., Fujita, S., & Benini, L. (2008, November). A low-overhead fault tolerance scheme for TSV-based 3D network on chip links. In*Proceedings of the 2008 IEEE/ACM International Conference on Computer-Aided Design* (pp. 598-602). IEEE Press.

[9] Kang, U., Chung, H. J., Heo, S., Park, D. H., Lee, H., Kim, J. H., ... & Lee, J. W. (2010). 8 Gb 3-D DDR3 DRAM using through-silicon-via technology.*IEEE Journal of Solid-State Circuits*, *45*(1), 111-119.

[10] Hsieh, A. C., & Hwang, T. (2012). TSV redundancy: architecture and design issues in 3-D IC. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *20*(4), 711-722.

[11] Jiang, L., Xu, Q., & Eklow, B. (2012, March). On effective TSV repair for 3D-stacked ICs. In *2012 Design, Automation & Test in Europe Conference & Exhibition (DATE)* (pp. 793-798). IEEE.

[12] Jiang, L., Ye, F., Xu, Q., Chakrabarty, K., & Eklow, B. (2013, May). On effective and efficient in-field TSV repair for stacked 3D ICs. In Proceedings of the 50th Annual Design Automation Conference (p. 74). ACM.

[13] Zhao, Y., Khursheed, S., & Al-Hashimi, B. M. (2015). Online Fault Tolerance Technique for TSV-Based 3-D-IC. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *23*(8), 1567-1571.

[14] Cho, M., Liu, C., Kim, D. H., Lim, S. K., & Mukhopadhyay, S. (2010, November). Design method and test structure to characterize and repair TSV defect induced signal degradation in 3D system. In *Proceedings of the International Conference on Computer-Aided Design* (pp. 694-697). IEEE Press.

[15] Chen, P. Y., Wu, C. W., & Kwai, D. M. (2009, November). On-Chip TSV Testing for 3D IC before Bonding Using Sense Amplification. In *Asian test symposium* (pp. 450-455).

[16] Huang, S. Y., Lin, Y. H., Tsai, K. H. H., Cheng, W. T., Sunter, S., Chou, Y. F., & Kwai, D. M. (2012, June). Small delay testing for TSVs in 3-D ICs. In*Proceedings of the 49th Annual Design Automation Conference* (pp. 1031-1036). ACM.

[17] Ye, F., & Chakrabarty, K. (2012, June). TSV open defects in 3D integrated circuits: Characterization, test, and optimal spare allocation. In *Proceedings of the 49th Annual Design Automation Conference* (pp. 1024-1030). ACM.

[18] "High Speed TDMA", SNUG Silicon Valley 2015, https://www.synopsys.com/news/pubs/snug/2015/siliconvalley/ta07_maheshwari_pres_snps.pdf.

[19] Ndip, I., Curran, B., Lobbicke, K., Guttowski, S., Reichl, H., Lang, K. D., & Henke, H. (2011). High-frequency modeling of TSVs for 3-D chip integration and silicon interposers considering skin-effect, dielectric quasi-TEM and slow-wave modes. *IEEE transactions on components, packaging and manufacturing technology*, *1*(10), 1627-1641.

[20] Sheibanyrad, A., & Pétrot, F. (2011). Asynchronous 3D-NoCs Making Use of Serialized Vertical Links. In *3D Integration for NoC-based SoC Architectures*(pp. 149-165). Springer New York.

[21] Sun, F., Cevrero, A., Athanasopoulos, P., & Leblebici, Y. (2010, September). Design and feasibility of multi-Gb/s quasi-serial vertical interconnects based on TSVs for 3D ICs. In *2010 18th IEEE/IFIP International Conference on VLSI and System-on-Chip* (pp. 149-154). IEEE.

[22] Georgiou, P., Vartziotis, F., Kavousianos, X., & Chakrabarty, K. (2016, May). Two-dimensional time-division multiplexing for 3D-SoCs. In *Test Symposium (ETS), 2016 21th IEEE European* (pp. 1-6). IEEE.

[23] Haykin, S. (2008). *Communication systems*. John Wiley & Sons.

[24] Katti, G., Stucchi, M., De Meyer, K., & Dehaene, W. (2010). Electrical modeling and characterization of through silicon via for three-dimensional ICs. *IEEE Transactions on Electron Devices*, *57*(1), 256-262.

[25] Sung, H., Cho, K., Yoon, K., & Kang, S. (2014). A Delay Test Architecture for TSV With Resistive Open Defects in 3-D Stacked Memories. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *22*(11), 2380-2387.

[26] Khursheed, S., Shi, K., Al-Hashimi, B. M., Wilson, P. R., & Chakrabarty, K. (2014). Delay test for diagnosis of power switches. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *22*(2), 197-206.

[27] IWLS 2005 Benchmark circuits.-URL: http://iwls.org/iwls2005/benchmarks.html

[28] Cong, J., Luo, G., & Shi, Y. (2011, June). Thermal-aware cell and through-silicon-via co-placement for 3D ICs. In *Proceedings of the 48th Design Automation Conference* (pp. 670-675). ACM.

[29] Noia, B., Panth, S., Chakrabarty, K., & Lim, S. K. (2015). Scan test of die logic in 3-D ICs using TSV probing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *23*(2), 317-330.

[30] Chen, Y. G., Wen, W. Y., Shi, Y., Hon, W. K., & Chang, S. C. (2015). Novel spare TSV deployment for 3-D ICs considering yield and timing constraints. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *34*(4), 577-588.

[31] Lung, C. L., Su, Y. S., Huang, S. H., Shi, Y., & Chang, S. C. (2011, June). Fault-tolerant 3D clock network. In *Proceedings of the 48th Design Automation Conference* (pp. 645-651). ACM.

[32] Song, T., Liu, C., Kim, D. H., Lim, S. K., Cho, J., Kim, J., ... & Yoon, K. (2011, March). Analysis of TSV-to-TSV coupling with high-impedance termination in 3D ICs. In *Quality Electronic Design (ISQED), 2011 12th International Symposium on* (pp. 1-7). IEEE.

[33] Song, T., Liu, C., Peng, Y., & Lim, S. K. (2016). Full-Chip Signal Integrity Analysis and Optimization of 3-D ICs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *24*(5), 1636-1648.

[34] Tida, U. R., Yang, R., Zhuo, C., & Shi, Y. (2015). On the efficacy of through-silicon-via inductors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *23*(7), 1322-1334.

[35] Zhong, S., Khursheed, S., Al-Hashimi, B. M., & Zhao, W. (2014). Efficient variation-aware delay fault simulation methodology for resistive open and bridge defects. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *33*(5), 798-810.

[36] Zhong, S., Khursheed, S., & Al-Hashimi, B. M. (2011). A fast and accurate process variation-aware modeling technique for resistive bridge defects. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *30*(11), 1719-1730.

[37] Zhao, Y., Khursheed, S., Al-Hashimi, B. M., & Zhao, Z. (2016, September). Co-optimization of fault tolerance, wirelength and temperature mitigation in TSV-based 3D ICs. In *Very Large Scale Integration (VLSI-SoC), 2016 IFIP/IEEE International Conference on* (pp. 1-6). IEEE.

Ravi Teja Reddy P is currently working towards his Ph.D degree at Indian Institute of Technology, Hyderabad, India. His area of research includes design-for-testability, reliability and yield of 3D integrated circuits.

Amit Acharyya (M'11) received the Ph.D. degree in 2011 from the School of Electronics and Computer Science in the University of Southampton, UK. Currently he is working as an Assistant Professor in the Indian Institute of Technology (IIT), Hyderabad, India. His research interests include signal processing algorithms, VLSI architectures, low power design techniques, computer arithmetic, numerical analysis, linear algebra, bio-informatics and electronic aspects of pervasive computing.

Saqib Khursheed is currently working as a lecturer (Assistant Professor) with Department of Electrical Engineering and Electronics, University of Liverpool, UK. In 2010, he received his PhD degree in Electronics and Electrical Engineering from University of Southampton, UK. After completing his PhD, he worked as a Senior Research Fellow at the University of Southampton on two EPSRC funded research projects.

He is interested in all issues related to reliability, test and yield improvement of low-power, high-performance designs and 3D integrated circuits. He has published a number of papers in internationally leading journals and conferences in these areas. He served as the Guest Editor for a special section on "Robust 3-D Stacked ICs" in IEEE Design & Test magazine (May/June 2016 issue) and special session co-chair of European Test Symposium (ETS 2016).