Unified Non-Inverting and Inverting PWM AC-AC Converter with Versatile Modes of Operation

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***Abstract*—This paper proposes a pulse width modulation (PWM) based unified non-inverting and inverting AC-AC converter (UNI-AC) for utility voltage compensation. It offers four effective switching states to regulate the output voltage in bipolar manner, facilitating versatile modes of operation with different number of switching states being modulated. Each mode of the UNI-AC is able to compensate both the grid voltage sag and swell problems due to its bipolar voltage gain. The operational principle and comparison for all these modes are investigated in details. Also, the UNI-AC is reversible and compatible with full range of power factor. Other technical merits offered by the proposed approach include the compact hardware installation, reduced voltage stress (low *dv*/*dt*) and decreased control complexity. Detailed analysis and experimental verification are presented in this paper.**

***Index Terms*—PWM AC-AC converter; bipolar voltage gain; versatile modes of operation; utility voltage compensation.**

I. INTRODUCTION

Owing to the rapidly increasing diversity of load conditions and various disturbance sources at the distribution level of power system, the grid voltages supplied to the local consumers are usually exposed to an increasing risk of power quality problems such as utility voltage sag/swell, three-phase unbalance and the voltage fluctuation (flicker) phenomenon, which are usually originated from severe load variations, for example, the transient of large power motors; as well as the vast use and uneven spread of single-phase load [1, 2].

The flexible ac transmission system (FACTS) devices are a range of techniques to address the grid control issues. Among all kinds of FACTS devices, the series compensator is able to stabilize the distributive grid voltage during the power quality events, serving as the dynamic voltage restorer (DVR) [3-5].

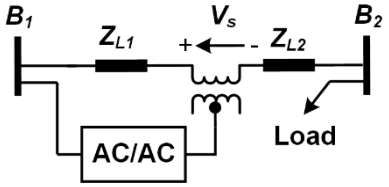

Fig. 1. The ac-ac converter based DVR for grid voltage compensation.

Typical DVR employs the dc-ac voltage source converter (VSC) to generate the desired ac voltage in series with the grid and supply proper amount of power to the load. Specifically, to maintain the grid voltage amplitude without considering the harmonic distortion and phase-shift, the direct ac-ac converter is viable to replace the sizeable dc-ac solution by saving the dc-link capacitor bank; therefore, reducing the footprint and cost. Typical configuration of ac-ac based DVR is shown in Fig. 1. Under this motivation, ac-ac converters for voltage amplitude regulation are of interest to be studied continuously [6, 7].

The basic ac-ac converters including buck, boost and buck-boost topologies all suffer from a unipolar voltage gain range, which, in use of the grid voltage compensation, restricts them to mitigate either voltage sag or swell but not both. Although the tapped-winding transformer can assist them in generating bipolar voltage, the combined system cost and total volume are uneconomical [8].

In order to overcome this constraint, the Z-source topology based ac-ac converter has been presented to achieve the bipolar voltage output ability by an additional impedance network [9]. However, this converter has a discontinuous voltage transfer ratio; also its input and output ports are floating to each other, increasing the insulation demand for the coupling transformers when used in grid applications. An alternative version of Z-source ac-ac converter in [10] is able to share the same ground for input and output but still has a high cost due to the passive device network. In [11, 12], a variety of quasi-Z-source based ac-ac converters are reported with some advantages compared to the original Z-source ac-ac converter such as the reduced passive devices, improved input profile and common ground shared by input and output terminals. The Gamma structure Z-source ac-ac converter in [13] employs the coupled inductor to offer an extra hardware design degree of freedom for varying the voltage gain. The main constraint of the above solutions is their incapability of generating in-phase step-down ac voltage; and hereby, the extremely sharp change in its gain curve that is challenging for the adaptive adjustment of the duty cycle command from the controller. A reversed scheme of [12] is analyzed in [14]. This solution has a continuous bipolar voltage transfer ratio with the use of the inner voltage boosting cell; besides, the ground sharing feature is kept. However, it still suffers from the high voltage and current stresses for the power switches (low device utilization) as in the Z-source type converters due to the voltage lifting capacitors; also, in these approaches, the high order passive elements in the impedance network result in a low bandwidth for the converter transfer functions; hence, slow dynamic response.

In an effort to reduce the passive device volume, a current source type composite ac-ac converter using six unidirectional switches is proposed in [15] with a wide range bipolar voltage generation capability. It uses less number of passive elements compared to the Z-source based schemes; therefore, reducing the voltage (current) stress on the semiconductor device and enhancing the converter dynamic response. The drawbacks of

this solution include the lack of common ground sharing and the complex modulation due to its composite structure.

This paper investigates a voltage source type unified non-inverting and inverting ac-ac converter (UNI-AC) operating in versatile modes thanks to the extra control degree of freedom. The UNI-AC offers following features: it achieves continuous and bipolar voltage transfer ratio without sharp changes as in Z-source based converters; it has improved controllability and various operation modes with increased number of control variables; the use of less passive devices in the UNI-AC leads to a reduced footprint and higher switching device utilization (low electrical stresses); also, the common ground between the input and output ports is retained. The reminder of this paper is arranged as follows: section II describes the principles for different operation modes of the UNI-AC; in section III, the performance evaluation for the proposed converter under each mode is carried out; based on which, the design guidelines of the UNI-AC is supplied in section IV; then, in section V, the experimental test results are presented to verify the proposed approach; finally, useful conclusions and main contributions are highlighted in section VI.

II. Operational Principle of The Proposed UNI-AC

The proposed UNI-AC is depicted in Fig. 2, where the four bidirectional switches using the back-to-back series-connected insulated gate bipolar transistor (IGBT) are adopted to facilitate the bidirectional current conduction and bidirectional voltage blocking capability. In Fig. 2, the two switches in the same leg such as S_1 and S_2 (or S_3 and S_4) are complementarily triggered using pulse width modulation (PWM) scheme; and also, there must be two conducted switches to form a power path at each instance. Based on these constraints, it is concluded that there are four switching states are valid for regulating the output voltage as described in Fig. 3.

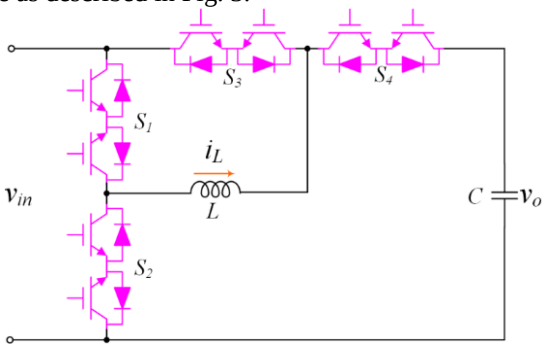

Fig. 2. The schematic of the proposed UNI-AC.

The switching state I in Fig. 3(a) turns on S_1 and S_4 to force the inductor L to release energy for charging the capacitor C. While for switching state II in Fig. 3(b), L is charged by the input source with S_3 and S_2 turned on; and the output current i_o is directly drawn from the output capacitor C. In Fig. 3(c), S_4 and S_2 conduct to form a zero-input power loop between L and C, which is noted as switching state III. The switching state IV when S_3 and S_1 are turned on as in in Fig. 3(d) represents the inductor current i_L freewheeling mode with the output current supplied by capacitor C. Based on Fig. 3, it is observed that different combinations of the four states can result in versatile modes of operation; and its control degrees of freedom varies accordingly. Detailed analysis for all possibilities is supplied in this section.

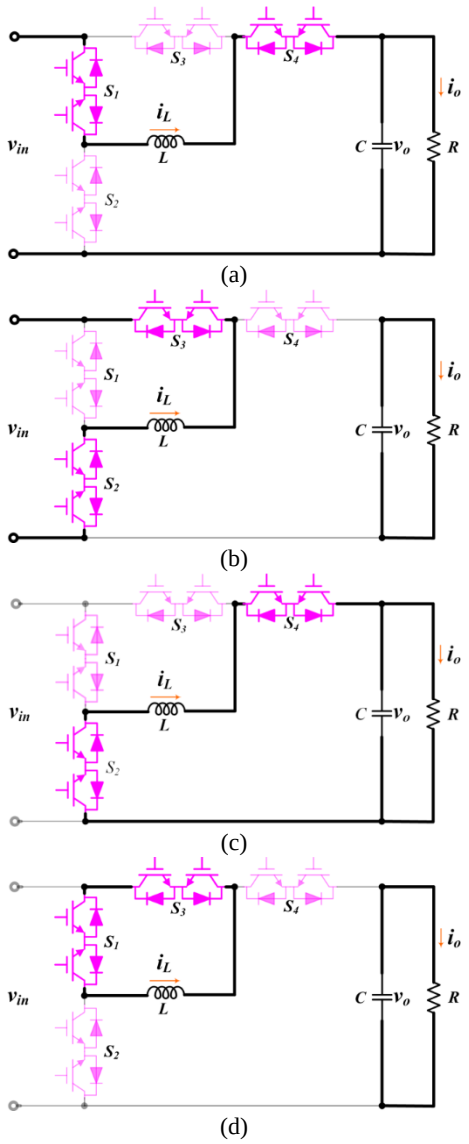

Fig. 3. Four effective switching states of UNI-AC: (a) state I with S_1 and S_4 turned on; (b) state II with S_2 and S_3 turned on; (c) state III with S_2 and S_4 turned on; (d) state IV with S_1 and S_3 turned on.

A. Operation mode A

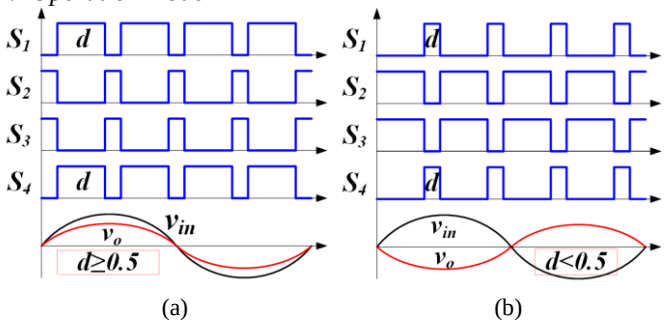

Fig. 4. Gate signals of the UNI-AC in operation mode A: (a) positive voltage gain; (b) negative voltage gain.

With the gate signals arranged as in Fig. 4, this mode uses the switching states I-II of Fig. 3 for the voltage conversion. The four switches are viewed to be separated into two groups $\{S_1, S_4\}$ and $\{S_2, S_3\}$; and these two groups are conducted in a complementary manner. Assuming the switching frequency is

sufficiently high compared to the fundamental frequency, if d is the duty cycle of $\{S_1, S_4\}$ in pulse width modulation (PWM), the switching average model of the UNI-AC is achieved as (1) using the established modelling procedures in [16, 17].

$$\begin{cases} L\cdot\dfrac{di_L}{dt} = d\cdot(v_{in}-v_o)-(1-d)\cdot v_{in} \\ C\cdot\dfrac{dv_o}{dt} = d\cdot(i_L-i_o)-(1-d)\cdot i_o \end{cases} \tag{1}$$

In steady state, since all state variables of the UNI-AC are purely distributed in fundamental frequency, the right terms of (1) is approximately viewed as zero due to their low variation rates. Hence, the transfer ratio of the voltage amplitude from input voltage to output voltage is achieved based on a quasi-steady-state analysis as shown in (2), where v_{o_m} and v_{in_m} are the magnitude of the output and input voltages respectively.

$$M_A = \frac{v_{o\_m}}{v_{in\_m}} = 2-\frac{1}{d} \tag{2}$$

Then, the plot for the relationship between M_A and d can be drawn as in Fig. 5. Notice that d is the only control degree of freedom in the operation mode A of UNI-AC; therefore, its voltage magnitude gain in this case can be described by a two-dimensional curve, where it is observed that the UNI-AC can offer bipolar voltage gain to either compensate the voltage sag or swell as a voltage stabilizer.

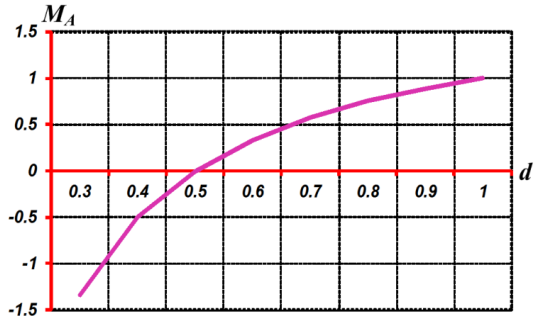

Fig. 5. Voltage amplitude transfer ratio of the UNI-AC under operation mode A using switching states I-II.

B. Operation mode B

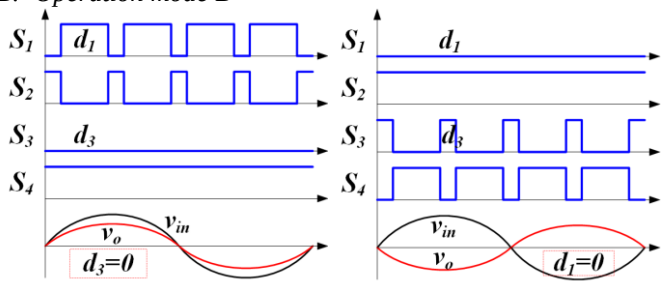

Fig. 6. Gate signals of the UNI-AC in operation mode B: (a) positive voltage gain; (b) negative voltage gain.

This operation mode of the proposed UNI-AC employs the switching states I-III in Fig. 3 to offer a bipolar voltage transfer ratio. For positive voltage gain, S_4 is kept to be conducted while S_3 is turned off constantly; at the same time, S_1 and S_2 are modulated in a PWM manner. This scheme combines switching states I and III to form a normal buck type operation for the UNI-AC with a gain range from 0 to 1. If negative voltage gain is required, states II and III are used, where S_1 remains blocked and S_2 is turned on as short circuit. Hence, the UNI-AC operates as a typical buck-boost converter with native voltage amplitude transfer ratio.

In mode B, the gate signals are shown in Fig. 6; also, the duty cycles of S_1 and S_3, d_1 and d_3, are used to describe the UNI-AC performance. Due to the hybrid buck and buck-boost operation, the dynamic equations of the UNI-AC in this case are piecewise, see (3) and (4). It is observed, when d_3=0, the UNI-AC works in buck mode; while if d_1=0, it is an inverting buck-boost converter. In further, by neglecting the variation of the state variables in (3) and (4) under steady state, the UNI-AC voltage gain in mode B can be achieved as in (5) with bidirectional voltage output ability in a piecewise pattern.

$$\begin{cases} L\cdot\dfrac{di_L}{dt} = d_1\cdot v_{in}-v_o \\ C\cdot\dfrac{dv_o}{dt} = i_L-i_o \end{cases}, \begin{cases} M_B\in[0,1] \\ d_3=0 \end{cases} \tag{3}$$

$$\begin{cases} L\cdot\dfrac{di_L}{dt} = -d_3\cdot v_{in}-(1-d_3)\cdot v_o \\ C\cdot\dfrac{dv_o}{dt} = -d_3\cdot i_o+(1-d_3)\cdot(i_L-i_o) \end{cases}, \begin{cases} M_B<0 \\ d_1=0 \end{cases} \tag{4}$$

$$M_B = \frac{v_{o\_m}}{v_{in\_m}} = \begin{cases} d_1, & \text{when } d_3=0 \\ -d_3/(1-d_3), & \text{when } d_1=0 \end{cases} \tag{5}$$

From (5), the voltage gain of UNI-AC in mode B can be displayed by Fig. 7 with a three-dimensional piecewise curve being produced. In the coordinates of d_1, d_3 and M_B, the first part of the space curve is distributed in the d_1-M_B plane with d_3=0 for the buck operation; while the second piece is located in d_3-M_B plane (d_1=0) as a buck-boost converter for inverting voltage generation.

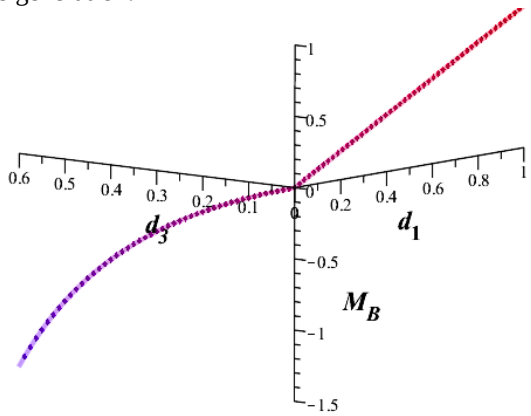

Fig. 7. Voltage amplitude transfer ratio of the UNI-AC under operation mode B using switching states I-III.

Also, mode B offers lower switching losses for UNI-AC compared to mode A due to its reduced total switching actions offered by the buck and buck-boost piecewise operation.

C. Operation mode C

The mode C employs all switching states I-IV in Fig. 3 to supply maximum control degree of freedom for the UNI-AC. In this scenario, the duty cycles of both legs are in PWM manner as in Fig. 8, i.e. d_1 and d_3 are free variables that are coordinated to regulate the output voltage. Hence, the dynamic equations

for UNI-AC mode *C* is described by (6). Similarly, the voltage gain for this mode is manipulated to be (7).

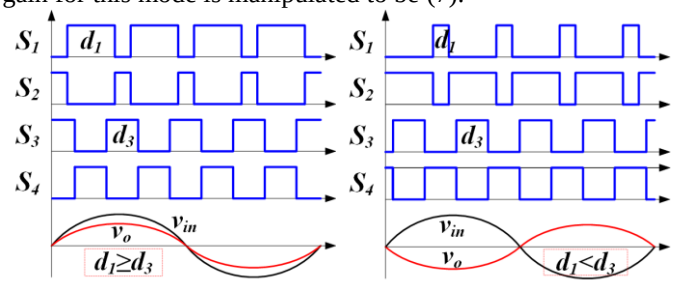

Fig. 8. Gate signals of the UNI-AC in operation mode *C*: (a) positive voltage gain; (b) negative voltage gain.

$$\begin{cases} L\cdot\dfrac{di_L}{dt} = d_1\cdot v_{in} - d_3\cdot v_{in} - (1-d_3)\cdot v_o \\ C\cdot\dfrac{dv_o}{dt} = (1-d_3)\cdot i_L - i_o \end{cases} \tag{6}$$

$$M_C = \frac{v_{o\_m}}{v_{in\_m}} = \frac{d_1 - d_3}{1-d_3} \tag{7}$$

In (7), since d_1 and d_3 are both free variables for the control of output voltage, the plot of M_c depending on d_1 and d_3 is a three-dimensional surface as shown in Fig. 9. In this mode, to achieve a certain voltage gain for the UNI-AC, the two control inputs can have infinite number of combinations as observed from Fig. 9. In practical control design of the proposed UNI-AC in operation mode *C*, the signal of d_s can be set to adjust the maximum inverting output voltage range and maintained constant when d_1 is changing for regulating the output voltage. In this manner, the linearity of the UNI-AC transfer function can be guaranteed. For example, in (7), if d_3 is set to be 0.5, the voltage gain M_c becomes a linear expression of d_1 ranging from -1 to 1 as shown by the line 'S' in Fig. 9. In further, with different preset values of d_3, M_c can be a family of straight lines in parallel with 'S', resulting in the variant output voltage range. This method is an optimized way for indexing d_1 and d_3 from the three-dimensional surface of voltage gain in Fig. 9 when operating the UNI-AC under mode *C*.

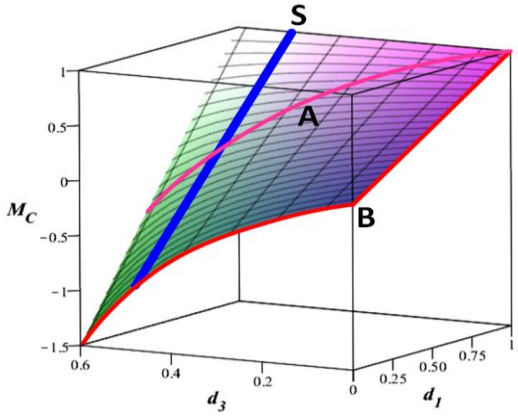

Fig. 9. Voltage amplitude transfer ratio of the UNI-AC under operation mode *C* using switching states I-IV.

It is worth noticing that the UNI-AC gain curves in mode *A* and *B* are both special cases of the voltage transfer ratio for mode *C*. When setting d_1=1-d_3=d in (7), it is simplified to be the same as (2) for mode *A*; while if (7) is restricted by the assumption of either d_1=0 or d_3=0, the same conclusion as (5) for mode *B* can be achieved. In Fig. 9, the identified curves 'A' and 'B' are transplanted version of the gain curves in Fig. 5 and Fig. 7 for operation mode *A* and *B*, respectively.

III. Performance Evaluation of UNI-AC

In this section, the performance evaluation for the UNI-AC is carried out; and then, a comprehensive comparison between different operation modes of UNI-AC and other traditional ac-ac converters are presented.

A. UNI-AC and current source AC-AC Converter

The conventional current source type ac-ac converter in [18] employs an intermediate current dc-link to connect two back-to-back unidirectional switch based bridge circuits, where twice number of switches are used in the conduction path compared to that in the proposed UNI-AC, resulting in higher losses.

Another main drawback of this converter compared to UNI-AC is the increased size and weight due to the dc current carried by the intermediate inductor. While in the UNI-AC, the inductor current is in ac pattern with small footprint. Also, the common ground feature between input and output is lost in the current source ac-ac converter.

B. UNI-AC and Other Bipolar AC-AC Converters

Observed from Fig. 3, the voltage stresses of S_1 and S_2 in UNI-AC are the same as the input voltage v_{in}; while S_3 and S_4 sustain a voltage of v_{in}-v_o. The current rating for all switches of UNI-AC are equal to the inductor current i_L.

By assuming the state variables variation rates in (1), (3), (4) and (6) to be zero, the steady state voltage transfer ratio of the UNI-AC under different modes have been achieved by (2), (5) and (7). Similarly, the transfer ratios {K_A, K_B, K_C} for the inductor current magnitude i_{L_m} from load current magnitude i_{o_m} can be solved into (8), (9) and (10) for mode *A*, *B* and *C*, respectively. Since mode *C* is the generic case of UNI-AC, it is employed for a comparison with the bipolar ac-ac converter in [14], the (modified) quasi-Z-source schemes in [11, 12], and the original Z-source ac-ac converters in [9, 10], see TABLE I.

$$K_A = \frac{i_{L\_m}}{i_{o\_m}} = \frac{1}{d} \tag{8}$$

$$K_B = \frac{i_{L\_m}}{i_{o\_m}} = \begin{cases} 1, \text{ when } d_3 = 0 \\ 1/(1-d_3), \text{ when } d_1 = 0 \end{cases} \tag{9}$$

$$K_C = \frac{i_{L\_m}}{i_{o\_m}} = \frac{1}{1-d_3} \tag{10}$$

In this comparison, the fixed input voltage and load current magnitude v_{in_m} and i_{o_m} are assumed for each converter; and based on (7) and (10), the voltage and current stresses of UNI-AC power switches under mode *C* can be quantified as in TABLE I, where it is observed the proposed solution employs reduced number of passive components than the Z-source type converters, resulting in lower switching voltage and current ratings. Therefore, although more power switches are used in UNI-AC, its total semiconductor device cost and conduction losses are not increased compared to its rivals with high power rated switches in TABLE I. Besides, the overall size of UNI-AC is reduced drastically with the significant save on the

TABLE I. Comparison results between the proposed UNI-AC and representative Z-source type ac-ac converters.

	UNI-AC (in mode *C*)		Bipolar ac-ac converter in [14]	(modified) quasi-Z source ac-ac converters in [11, 12]	Original Z-source ac-ac converters in [9, 10]
Voltage gain	$\frac{d_1 - d_3}{1 - d_3}$		$\frac{2d-1}{d}$	$\frac{1-d}{1-2d}$	$\frac{1-d}{1-2d}$
Switching voltage stress	S_1, S_2	v_{in_m}	$v_{in\_m} \times \frac{1}{d}$	$v_{in\_m} \times \frac{1}{1-2d}$	$v_{in\_m} \times \frac{1}{1-2d}$
	S_3, S_4	$v_{in\_m} \times \frac{1-d_1}{1-d_3}$			
Switching current stress	$i_{o\_m} \times \frac{1}{1-d_3}$		$i_{o\_m} \times \frac{1}{d}$	$i_{o\_m} \times \frac{1}{1-2d}$	$i_{o\_m} \times \frac{1}{1-2d}$
Passive device	one inductor, one capacitor		two inductors, two capacitors	three or two inductors, three or two capacitors	three inductors, three capacitors
Ground sharing	Yes		Yes	Yes	Possible

passive elements, leading to a compact hardware design and a high power density. Also, the proposed converter is able to share a common ground for the input and output ports by the solid connection of the reference terminals.

Due to the increased control degree of freedom in the UNI-AC, its voltage gain is controlled by two variables, d_1 and d_3; while other candidates have only one control input. This can bring versatile modes of operation to the proposed converter as analyzed in section II with advanced features. For example, the dynamic response of UNI-AC is fast due to the less use of passive elements; further, in operation mode *B* of the UNI-AC, the switching losses can be reduced significantly since there is only switching actions in one leg; also, the mode *C* offers two independent control degrees of freedom in the UNI-AC with the possibility for a linear bipolar modulation range that is beneficial for the robustness and bandwidth of the controller due to the time-invariant features of the converter model. In contrast, the Z-source based converters usually have higher number of poles and zeros in their transfer functions including right-half-plane (RHP) zeros, which, as a time-variant model, will drift when the operation point changes in an ac system. This deteriorates the global stability and dynamic response of the ac-ac converter applied as a voltage compensator [16].

C. Different Operation Modes of the UNI-AC

In further, detailed performance of UNI-AC in different operation modes are investigated. If the desired voltage gain of the UNI-AC is from -1.5 to 1, the switching voltage stresses are the same for all operation modes with v_{in_m} (input voltage) for $\{S_1, S_2\}$ and $2.5 \times v_{in\_m}$ (maximum difference between input and output voltages) for $\{S_3, S_4\}$; while the current ratings for the power switches under each mode are different depending on its extreme value of the duty cycle.

TABLE II. Comparison between each operation modes of UNI-AC with fixed voltage gain from -1.5 to 1 and fixed load current i_{o_m}.

UNI-AC operation mode	Mode *A*	Mode *B*	Mode *C*
Switching current rating	$3.5 \times i_{o\_m}$	$2.5 \times i_{o\_m}$	$2.5 \times i_{o\_m}$
Maximum voltage ripple	$0.7143 \times \frac{i_{o\_m}}{f_{sw}C}$	$0.6 \times \frac{i_{o\_m}}{f_{sw}C}$	$0.6 \times \frac{i_{o\_m}}{f_{sw}C}$
Maximum current ripple	$0.7143 \times \frac{v_{in\_m}}{f_{sw}L}$	$0.6 \times \frac{v_{in\_m}}{f_{sw}L}$	$0.6 \times \frac{v_{in\_m}}{f_{sw}L}$
Conduction loss	Relatively high	Low	High
Switching loss	Relatively high	Low	Relatively high
Control degree of freedom	One	One	Two

From (2), the control signal d (duty cycle of S_1) should range from 0.2857 to 1 in operation mode *A* to guarantee the desired output voltage range; similarly, using (5) for mode *B*, d_1 varies from 0 to 1 for non-inverting buck operation and d_3 changes from 0 to 0.6 for the inverting buck-boost voltage generation; in mode *C*, using the linear indexing method, d_3 is fixed as 0.6 and d_1 is modulated from 0 to 1. Based on above observations and (8)-(10), the current stresses for the power devices of UNI-AC in each operation mode can be calculated as in TABLE II, where it is found mode *A* suffers from the highest switching current stresses due to its higher duty cycle for S_3 than other cases for generating out-of-phase voltage.

From (1), the ripple voltage and ripple current on the state variables of the UNI-AC in mode *A* can be estimated by (11), where f_{sw} is the switching frequency. The maximum ripple components are then achieved as in TABLE II by substituting the minimum value of d into (11) to generate the maximum out-of-phase voltage (inverting).

$$\begin{cases} \Delta i_{L\_A} = \dfrac{v_{in\_m} \cdot (1-d)}{f_{sw} \cdot L} \\ \Delta v_{o\_A} = \dfrac{i_{o\_m} \cdot (1-d)}{f_{sw} \cdot C} \end{cases} \tag{11}$$

Based on (3) and (4) for mode *B*, the ripple components equations are in a piecewise pattern. Within positive gain area, the UNI-AC works in typical buck mode with minimum ripple components; thus, the ripple expressions in the inverting gain region are focused, see (12). As in TABLE II, the maximum ripples happen at the negative peak voltage gain point when d_3 reaches its maximum, which is 0.6.

$$\begin{cases} \Delta i_{L\_B} = \dfrac{v_{in\_m} \cdot d_3}{f_{sw} \cdot L} \\ \Delta v_{o\_B} = \dfrac{i_{o\_m} \cdot d_3}{f_{sw} \cdot C} \end{cases}, \text{ when } d_1 = 0 \tag{12}$$

In mode *C*, from Fig.7 and (7), when d_1 is larger than d_3 for positive voltage gain, the switching state II in Fig. 3 will not be used; while if d_1 is smaller than d_3 for negative voltage transfer ratio, the switching state I does not emerge. Similarly, in this mode, the UNI-AC ripple performance becomes worse during the voltage inverting region; hence, (13) is employed to calculate the maximum ripple current and voltage, which are shown in TABLE II with d_3=0.6 and d_1=0.

$$\begin{cases} \Delta i_{L\_C} = \dfrac{v_{in\_m}\cdot(d_3-d_1)}{f_{sw}\cdot L} \\ \Delta v_{o\_C} = \dfrac{i_{o\_m}\cdot(d_3-d_1)}{f_{sw}\cdot C} \end{cases}, \text{when } d_1<d_3 \tag{13}$$

To evaluate the conduction losses of power semiconductor devices in the proposed UNI-AC, two operational points with bipolar voltage transfer ratio of 0.8 and -1 are examined for each mode. It is observed from Fig. 3, in each instance, there are always two switches from different legs in the conduction path. Since the voltage ratings of power switches are the same for each mode, the equivalent IGBT parameters including their total forward voltage drop and equivalent resistance are fixed and denoted by V_F and R_{av}, respectively. Thus, if the output current is expressed by (14), from (10), the generic conduction losses are obtained by (15). For given output voltage v_{o_m}, the output power S_o is equal to $\frac{1}{2}v_{o\_m}\times i_{o\_m}$; and the percentage of semiconductor conduction losses are calculated using (16).

$$i_o = i_{o\_m}\cdot\sin\omega t \tag{14}$$

$$\begin{aligned} P_{con} &= \frac{1}{\pi}\int_0^{\pi}(V_F\cdot i_L + R_{av}\cdot {i_L}^2)\cdot d\omega t \\ &= \frac{2V_F}{\pi}\cdot\frac{i_{o\_m}}{1-d_3} + R_{av}\cdot\frac{{i_{o\_m}}^2}{2(1-d_3)^2} \end{aligned} \tag{15}$$

$$\lambda = \frac{P_{con}}{S_o + P_{con}} \tag{16}$$

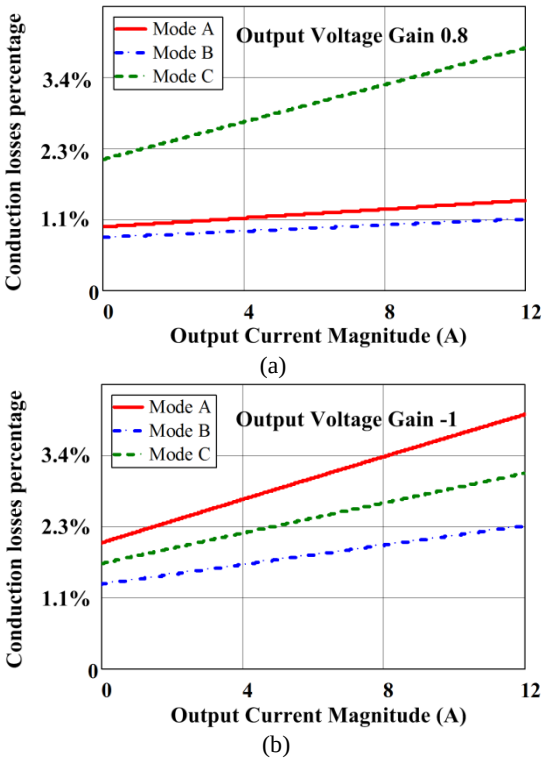

Fig. 10. Percentage of the semiconductor device conduction losses in the UNI-AC: (a) output voltage gain is 0.8; (b) output voltage gain is -1.

Specifically, the equivalent duty cycle of d_3 for two cases with 0.8 and -1 voltage gains can be determined using (2), (5) and (7). Then, assuming v_{in_m}=150V, V_F=0.8V and R_{av}=0.03Ω, the conduction losses in percentage for the above cases can be plotted in Fig. 10, where mode *B* has the lowest on-state power dissipations. Also, as stated previously, mode *B* can reduce the switching losses with the decreased switching actions.

The above conclusions are listed in TABLE II, where it is concluded that mode *B* is an optimized operational trajectory for the UNI-AC in terms of efficiency performance; while the mode *C* offers superior control flexibility.

IV. Design of the UNI-AC

Based on previous analysis, the guidelines of the parameter selection for the UNI-AC are provided using a scale-down case study in following procedure:

- The known parameters: input peak voltage v_{in_m}=150V, output voltage gain range [M_n, M_p]=[-1.5, 1], total load impedance Z_L=40Ω, switching frequency f_{sw}=25kHz, allowable current and voltage ripples κ_i=20% of i_{L_m} and κ_v=10% of v_{o_m} (or v_{in_m});
- Recall Fig. 2, voltage stresses of S_1 and S_2 are equal to v_{in_m}=150V; the voltage stresses of S_3 and S_4 are the subtraction of v_{in_m} and the maximum inverting output voltage, which is expressed as $v_{in\_m}\times(1-M_n)$ =375V;
- Based on (2), (5) and (7), the duty cycle of S_3 for generating the maximum out-of-phase voltage (the voltage gain M_n) in each mode can be obtained as (17);

$$\begin{cases} d_{3\_A}^{\max} = 1-1/(2-M_n) = 0.7143 \\ d_{3\_B}^{\max} = 1-1/(1-M_n) = 0.6 \\ d_{3\_C}^{\max} = 0.6 \end{cases} \tag{17}$$

- With maximum load current in (18); the switch current stresses in each mode can be calculated by (19);

$$i_{o\_m}^{\max} = \frac{v_{in\_m}\cdot\max(|M_n|,|M_p|)}{Z_L} \approx 5.6\text{A} \tag{18}$$

$$\begin{cases} I_{str\_A} = i_{o\_m}^{\max}/(1-d_{3\_A}^{\max}) \approx 20\text{A} \\ I_{str\_B} = i_{o\_m}^{\max}/(1-d_{3\_B}^{\max}) \approx 14\text{A} \\ I_{str\_C} = i_{o\_m}^{\max}/(1-d_{3\_C}^{\max}) \approx 14\text{A} \end{cases} \tag{19}$$

- The inductance value can be determined by (20), based on (11)-(13);

$$\begin{cases} L_A^{\min} = \dfrac{v_{in\_m}\cdot d_{3\_A}^{\max}\cdot(1-d_{3\_A}^{\max})}{f_{sw}\cdot\kappa_i\cdot i_{o\_m}^{\max}} = 1.09\text{mH} \\ L_B^{\min} = \dfrac{v_{in\_m}\cdot d_{3\_B}^{\max}\cdot(1-d_{3\_B}^{\max})}{f_{sw}\cdot\kappa_i\cdot i_{o\_m}^{\max}} = 1.28\text{mH} \\ L_C^{\min} = \dfrac{v_{in\_m}\cdot d_{3\_C}^{\max}\cdot(1-d_{3\_C}^{\max})}{f_{sw}\cdot\kappa_i\cdot i_{o\_m}^{\max}} = 1.28\text{mH} \end{cases} \tag{20}$$

- The required input capacitance depends on the duration of current discontinuity in the input, which is nearly zero for mode *A*. For other modes, with the maximum fundamental input current in (21); the needed minimum capacitance can be calculated based on (22);

$$i_{in\_m}^{\max} = \frac{v_{in\_m}\cdot {M_n}^2}{Z_L} \approx 8.44\text{A} \tag{21}$$

$$C_{in}^{\min} = \frac{i_{in\_m}^{\max}\cdot(1-d_{3\_B}^{\max})}{\kappa_v\cdot v_{in\_m}\cdot f_{sw}} = 9\mu\text{F} \tag{22}$$

- The output capacitance is chosen by (23) based on the voltage ripple requirement.

$$\begin{cases} C_A^{\min} = \dfrac{i_{o\_m}^{\max} \cdot d_{3\_A}^{\max}}{f_{sw} \cdot \kappa_v \cdot v_{in\_m} \cdot |M_n|} = 7.15\mu\text{F} \\ C_B^{\min} = \dfrac{i_{o\_m}^{\max} \cdot d_{3\_B}^{\max}}{f_{sw} \cdot \kappa_v \cdot v_{in\_m} \cdot |M_n|} = 6\mu\text{F} \\ C_C^{\min} = \dfrac{i_{o\_m}^{\max} \cdot d_{3\_C}^{\max}}{f_{sw} \cdot \kappa_v \cdot v_{in\_m} \cdot |M_n|} = 6\mu\text{F} \end{cases} \quad (23)$$

- For all above calculated passive devices, their reactive power ratings should be reexamined as for an ac system, which are required be within the reasonable range of the total power capacity.

To be compatible with all operation modes, the experiment specifications of UNI-AC are selected as in TABLE III, where MOSFETs and diodes are adopted as bidirectional switches in this low voltage design case.

TABLE III. Specification of the UNI-AC experiment.

Input voltage peak value v_{in_m}	150V
Load impedance Z_L	40Ω
Power rating	300VA
Switching frequency f_{sw}	25kHz
Inductance L	1.3mH
Output capacitance C	10μF
Input capacitance C_{in}	10μF
Bidirectional switch S_1-S_4	SPHX0N60S5 and STTH6012

In fact, the right terms of the volt-second balance equations in (1), (3), (4) and (6) are not zero in steady state due to the reactive power consumption of inductors; instead, they should be equal to the loop voltage drop caused by inductor current i_L flowing the inner impedance r (loop resistance) and ωL (ω is the fundamental angular frequency). If the load impedance is Z_L and λ is impedance ratio in (24), the voltage gains of UNI-AC in each mode can be revised as (25), (26) and (27).

$$\lambda = \frac{\sqrt{\omega^2 L^2 + r^2}}{Z_L} \quad (24)$$

$$M_A^* = \frac{v_{o\_m}}{v_{in\_m}} = \frac{(2d-1)\cdot d}{d^2 + \lambda} \quad (25)$$

$$M_B^* = \frac{v_{o\_m}}{v_{in\_m}} = \begin{cases} \dfrac{d_1}{1+\lambda}, \text{ when } d_3 = 0; \\ -\dfrac{d_3 \cdot (1-d_3)}{(1-d_3)^2 + \lambda}, \text{ when } d_1 = 0. \end{cases} \quad (26)$$

$$M_C^* = \frac{v_{o\_m}}{v_{in\_m}} = \frac{(d_1 - d_3)\cdot(1-d_3)}{(1-d_3)^2 + \lambda} \quad (27)$$

With the parameters in TABLE III and the total conduction path resistance of 0.45Ω, the voltage gains in (25), (26) and (27) can be plotted by Fig. 11. It is observed from Fig. 11(a) and (c), when the duty cycle of S_3 is larger than a critical value, the output voltage gain will decrease significantly due to its inner voltage drop, which is similar as in normal boost dc-dc converter. This has resulted in an uncontrollable region for the proposed UNI-AC. Hence, in the test case of TABLE III, d_3 is limited to be lower than 0.75.

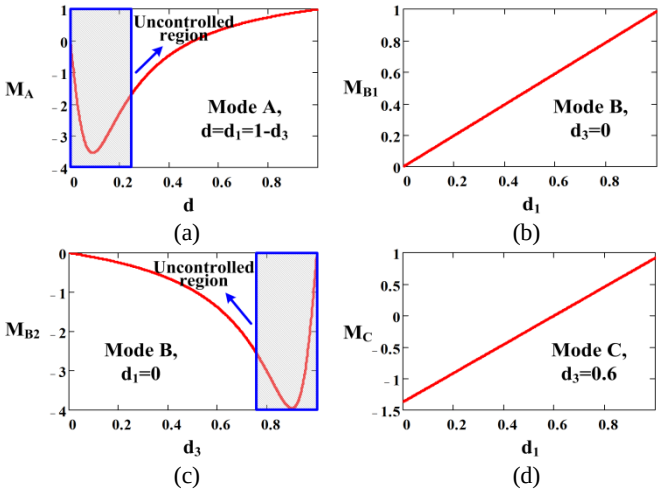

Fig. 11. The practical gains of UNI-AC considering inner impedance: (a) mode *A*; (b) mode *B* (positive); (c) mode *B* (negative); (d) mode *C*.

V. Simulation and Experiment

A. Simulation Results

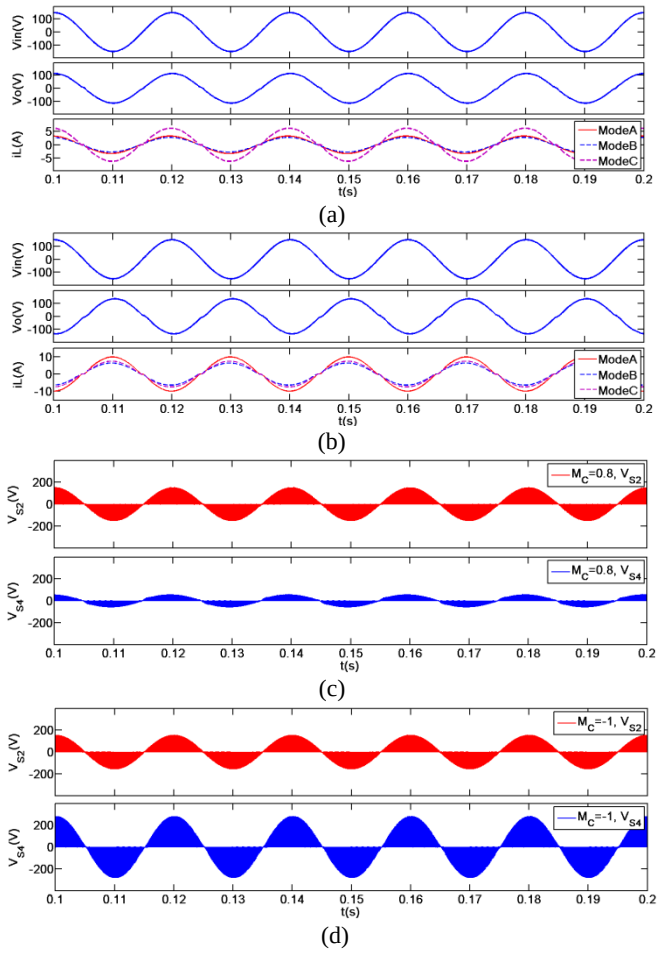

Fig. 12. Simulation results of UNI-AC: (a) 120V non-inverting output voltage and inductor current; (b) 150V inverting output voltage and inductor current; (c) voltage of switches S_2 and S_4 with in-phase output voltage under mode *C*; (d) voltage of switches S_2 and S_4 with out-of-phase output voltage under mode *C*.

The simulation results of the UNI-AC with specifications in TABLE III are shown in Fig. 12. In this test, the output voltage is controlled as 120V in-phase in Fig. 12(a) with the largest inductor current in mode *C*; then, the output voltage is set to be

150V out-of-phase in Fig. 12(b); and inductor current in mode *A* is largest. This observation agrees with previous analysis.

Furthermore, the sampled waveforms of voltage across the bidirectional switches S_2 and S_4 with both positive and negative voltage gains are given for operation mode *C* in Fig. 12(c) and (d), respectively.

B. *Experiment Verification*

For further verifications, a prototype of the UNI-AC has been built and tested using the same specifications in TABLE III; then, an Infineon TC1796 DSP platform is adopted for the digital modulation of the proposed converter. The photo of the experimental setup is displayed by Fig. 13.

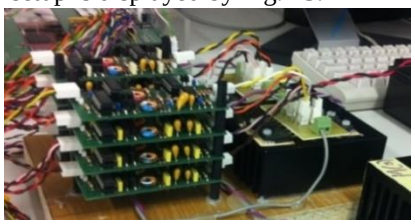

Fig. 13. The photo of the experimental setup for UNI-AC.

The UNI-AC test rig works in operation mode *A*, *B* and *C* at pre-set output voltage gain of 0.8 and -1, respectively. In the PWM implementation, all the gate signals are arranged in the centre-aligned pattern. Specially, the duty cycle d_3 is set to 0.6 for operation mode *C*. The safe commutation strategy in [13, 19] is adopted to avoid additional passive snubber circuits.

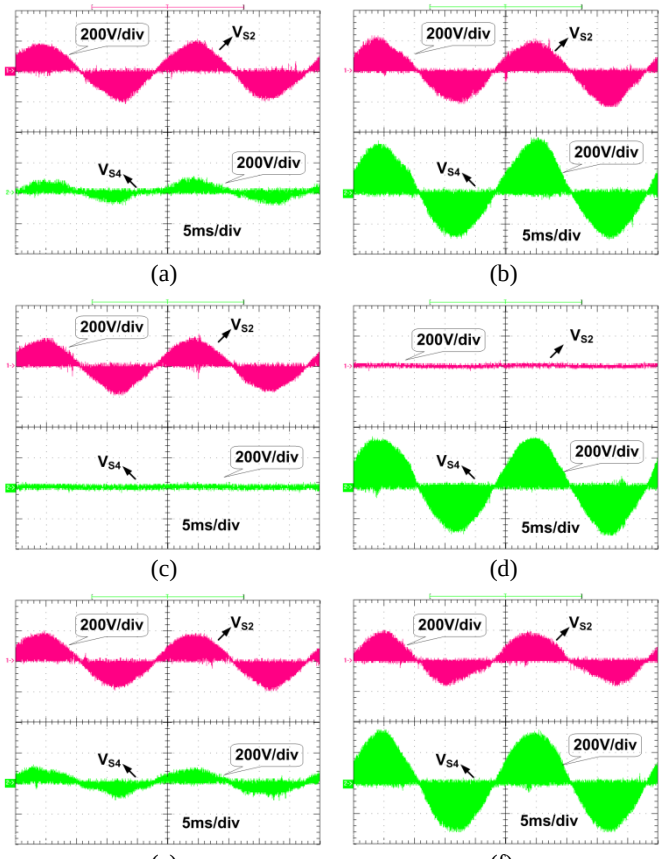

Fig. 14. Voltage on the bidirectional switches (V_{S2} and V_{S4}): (a) mode *A* with voltage gain of 0.8; (b) mode *A* with voltage gain of -1; (c) mode *B* with voltage gain of 0.8; (d) mode *B* with voltage gain of -1; (e) mode *C* with voltage gain of 0.8; (f) mode *C* with voltage gain of -1.

Fig. 14 shows the voltage waveforms of the bidirectional switches S_2 and S_4 for each case. It is observed that when the voltage gain of the UNI-AC changes to negative direction, for all the operation modes, the switching voltage stresses on the switches S_3 and S_4 become larger than those in positive gain region. This is because the switch leg composed by S_1 and S_2 sustains a total voltage equal to input voltage; while the S_3 and S_4 together have to block the voltage difference between the input and output terminals. Specially, minimized switching action (thus, switching losses) can be achieved by the operation mode *B* of the proposed converter as in Fig. 14 (b) and (c).

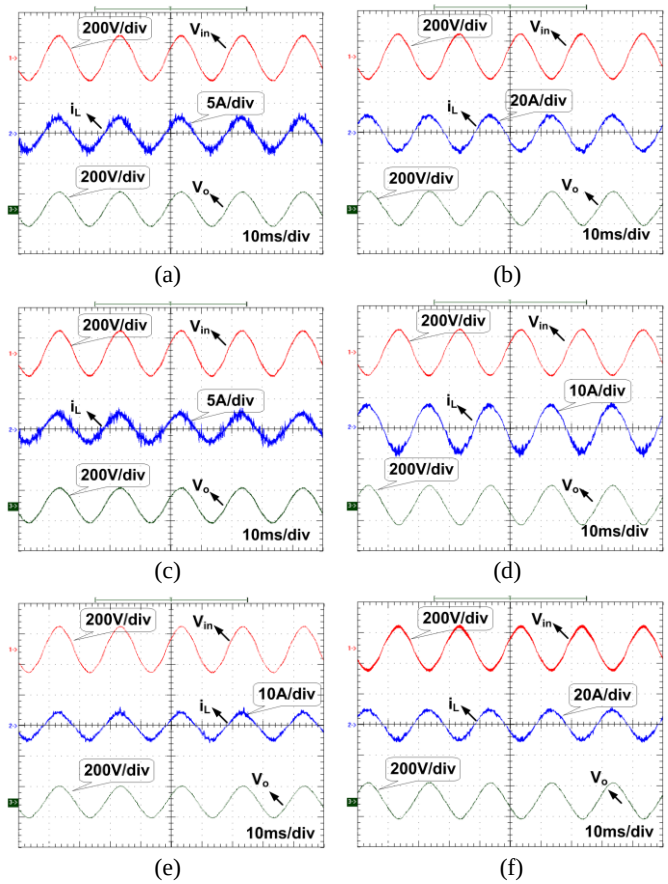

Fig. 15. The input voltage (v_{in}), output voltage (v_o) and inductor current (i_L) waveforms: (a) mode *A* with voltage gain of 0.8; (b) mode *A* with voltage gain of -1; (c) mode *B* with voltage gain of 0.8; (d) mode *B* with voltage gain of -1; (e) mode *C* with voltage gain of 0.8; (f) mode *C* with voltage gain of -1.

The line frequency waveforms for UNI-AC are also shown in Fig. 15, where the input voltage v_{in}, inductor current i_L and output voltage v_o are displayed for the two pre-set operation points under each mode, respectively. In positive gain region, operation mode *C* has the highest current stress for the power switches (inductor current) due to the large conduction period of S_3, which results in poorest efficiency performance in this region. On the other side, within the negative voltage gain area, the average switching current for mode *A* increases and finally exceeds that in mode *C*. Hence, mode *A* is not competitive for producing high magnitude out-of-phase voltage compared to mode *B* and *C* due to the relatively large circulating current stimulated through the power switches. Among all operation cases, mode *B* offers the lowest average current and conduction

losses for the power switches. These observations are in line with the analysis and conclusions in TABLE II.

The measured total harmonic distortion (THD) values of the UNI-AC output voltage with -1 voltage gain for each operation mode are listed in TABLE IV. As is analysed previously, the switch voltage stresses of the UNI-AC are much lower than those in the impedance network based converters, which means the overall *dv*/*dt* is smaller. Thus, generally, a reduced THD in the UNI-AC can be expected. Further, different modes of the UNI-AC have different PWM patterns and harmonic content. The use of zero voltage states in mode *B* reduces the total number of switching instances and achieves lowest THD.

TABLE IV. Measured UNI-AC output voltage THD in each mode

	Mode *A*	Mode *B*	Mode *C*
UNI-AC output voltage THD	3.56%	3.34%	3.88%

If the input voltage is 150V (peak value) and the nominal resistive load is R_L=40Ω, by varying the load *R*, the UNI-AC efficiency for mode *A*, *B* and *C* at voltage gain of 0.8 and -1 are shown in Fig. 16, which indicates that mode *B* has highest efficiency performance for both 0.8 and -1 voltage gains. This is achieved by the reduced average current in the power device and the minimized switching actions. The efficiency for mode *A* changes drastically for different operational points since the duty cycle d_3 (thus, average current in the power switches) has the largest variation range among all modes. While in mode *C*, since d_3 is fixed to offer a linear modulation range as shown in Fig. 11(d), the conduction losses of the UNI-AC in this case are less influenced by the voltage gain change; thus, its overall efficiency difference at different operational points are mainly determined by the switching losses.

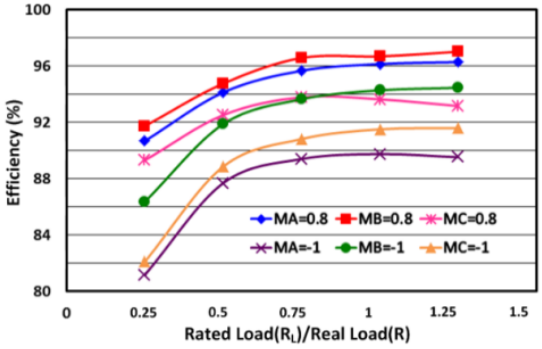

Fig. 16. The efficiency performance of UNI-AC in different modes and operation points with load variations.

C. Simulation Study of UNI-AC Based DVR

Simulation of the UNI-AC applied as a DVR is carried out based on the configuration of Fig. 1. The nominal grid phase voltage is 240V (root-mean-square, RMS). In the UNI-AC device, 10μH inductor and 10μF output capacitor are adopted. The system power rating is 10kVA per phase.

Fig. 17 shows that the UNI-AC is able to generate either in-phase or out-of-phase voltage to compensate both voltage sag and swell problems. During 0s~0.1s, the grid remains stable, and the UNI-AC device produces dominantly reactive power to support the grid voltage at the load bus. Then, at 0.1s, the grid voltage starts a 20% swell and the UNI-AC generates out-of-phase voltage to force the voltage at the critical bus to track the reference. Finally, at 0.2s, the grid experiences 30% sag, which is managed by the UNI-AC with in-phase voltage injection.

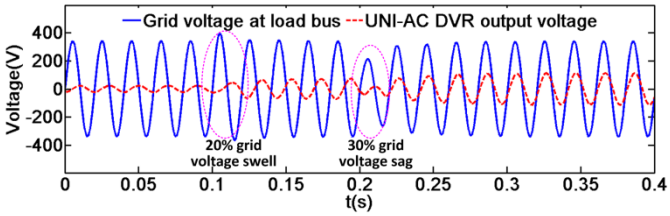

Fig. 17. DVR application of the proposed UNI-AC for distributed grid voltage sag/swell compensation.

VI. CONCLUSIONS

In this paper, the unified non-inverting and inverting PWM ac-ac converter (UNI-AC) with reduced passive components and high power density is analysed. Thanks to its increased control degrees of freedom, versatile modes of operation can be established for the UNI-AC. Further, the law of operation and the performance analysis for each mode are presented in details. Mode *A* has the simplest modulation scheme with only two switching states being used; however, its power switch current stresses, conduction losses and ripple performances are uncompetitive compared to other operation modes. Mode *B* is able to reduce the losses significantly due to its lower current stresses for switches and the decreased total switching actions. Mode *C* offers maximum control flexibility with both two legs being modulated independently (higher switching losses than mode *B*). By certain arrangement for the modulating signals, this mode is able to manipulate the converter average model to be a linear form with enhanced global stability and robustness. The UNI-AC also has a common ground shared by the input and output ports. Experimental work has been carried out to verify the feasibility and effectiveness of the UNI-AC.

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