Publishing d determination of nanowires electrical properties using a dielectrophoresiswell based system

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The use of high quality semiconducting nanomaterials for advanced device applications has been hampered by the unavoidable growth variability of electrical properties of one-dimensional nanomaterials such as nanowires and nanotubes, thus highlighting the need for the efficient semiconducting nanomaterials characterization. In this study, we demonstrate a low-cost, industrially-scalable dielectrophoretic (DEP) nanowire assembly method for the rapid analysis of the electrical properties of inorganic single crystalline nanowires, by identifying key features in the DEP frequency response spectrum from 1kHz to 20MHz in just 60 seconds. Nanowires dispersed in anisole were characterized using a three-dimensional DEP chip (3DEP), and the resultant spectrum demonstrated a sharp change in nanowire response to DEP signal in 1-20MHz frequency range. The 3DEP analysis, directly confirmed by field-effect transistor data, indicates that nanowires with higher quality are collected at high DEP signal frequency range above 10MHz, whereas lower quality nanowires, with two orders of magnitude lower current per nanowire, are collected at lower DEP signal frequencies. These results show that 3DEP platform can be used as a very efficient characterization tool of the electrical properties of rod-shaped nanoparticles to enable dielectrophoretic selective deposition of nanomaterials with superior conductivity properties.

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Semiconducting single-crystalline nanowires (NWs) offer many advantages for the fabrication of **Publishing** solution-processed, low-cost printed electronic devices. Their unique characteristics make them potential key building blocks in many emerging applications, such as chemical and biological sensors,¹⁻³ high performance FETs,⁴⁻⁶ optical devices,^{7, 8} memory elements⁹⁻¹¹ and energy harvesting nanogenerators.^{12, 13}

However, NW bottom-up synthesis methods, e.g., vapor-liquid-solid (VLS) growth, often produce heterogeneous mixtures of NWs with a range of different electrical properties, and as a consequence, the purification of one-dimensional nanomaterials based on their electrical properties is a significant hurdle for the fabrication of reliable and high-performance devices. Whilst the deposition of NWs into ordered arrays has been demonstrated with various techniques, such as Langmuir-Blodgett,¹⁴ Blown-Bubble films,¹⁵ flow-directed assembly¹⁶ and electrostatic interactions,¹⁷ these techniques do not include a selection step to separate the most desirable NW based on their electrical performance.

We have previously demonstrated the direct selection of Supercritical Fluid–Liquid–Solid grown silicon (Si) nanowires based on their conduction properties from poly-disperse as-synthesized NWs using dielectrophoresis (DEP) coupled with impedance spectroscopy, highlighting the selective collection of NWs with different electrical properties at various applied frequencies.¹⁸ DEP is an electrostatic phenomenon of induced motion of a polarizable particle when subjected to an inhomogeneous electric field. Depending on the electrical properties of the particle and suspending medium, the induced DEP force causes the particle to either be attracted towards the region of high electric field gradient (positive DEP) or repelled (negative DEP) along the direction of the field gradient¹⁹; the magnitude and direction of the force is dependent on the electrical properties of particle and medium, and on the frequency of the applied field. Consequently, the analysis of the DEP response of nanomaterials over a range of frequencies can be used to determine the properties of suspensions, whilst particles with different properties can be separated by selecting a frequency, where the different populations experience stronger or weaker DEP forces¹⁸. The use of DEP characterization has been widely explored in the biosciences,



funtil recently was restricted to laboratories with expertise in the field. However, a new commercial Publishing platform that utilizes a disposable, three-dimensional (3D) well electrode chip (3DEP by DEPtech, Uckfield, UK) coupled with a prototype 3DEP system reader (Labtech, Uckfield, UK) makes DEP characterization suitable for a wider range of nanomaterials.²⁰ This 3DEP platform has been used in the measurement of the electrical properties of cells used in cancer studies²¹⁻²⁴ (incl. keratinocyte. OOPC and OSCC cells) and drug interaction.²⁵ The system is engineered principally for the rapid and nearreal-time analysis of the electrical properties of cells, taking typically 10 seconds to analyze a population of ca. 20000 cells. However, 3DEP system has not been previously used for the characterization of nanomaterials.

Traditionally, DEP electrodes are constructed with dimensions that reflect the size of the particles, however, the 3DEP chip used in this work with electrode gap size of 150µm still provided an efficient characterization tool for ~22µm long silicon nanowires used in this study.

In this letter, we demonstrate the efficacy of the 3DEP system as a rapid evaluation tool of the electrical properties of as-synthesized SiNWs ensemble using a frequency spectrum analysis. 3DEP chip frequency response of dispersed SiNWs showed a 'threshold' DEP signal frequency of ~1MHz, above which, the DEP started to collect higher quality NWs, whereas nanowires collected at low DEP signal frequencies range (Hz to kHz) were, on average, significantly inferior to high frequency assembled NWs. The whole response spectrum (1kHz-20MHz) measurement of NWs took only one minute. This DEP frequency response information was then used to fabricate fully functional nanowire devices, and direct correlation between DEP signal frequency and the SiNWs conductivity was confirmed by comparing field-effect transistor (FET) data for devices fabricated with multiple NWs collected in the FET channels at various DEP frequencies (30Hz, 300kHz, 10MHz and 20MHz), demonstrating that average current per nanowire can increase by two order of magnitude from bad to good nanowires.

Appr-iquid-solid growth of SiNWs was catalyzed using commercially-available 60nm Au nanoparticles randomly dispersed on poly-L-lysine-functionalized Si(111) substrates. Growth was performed at 900°C and 80kPa using 30sccm (standard cm³/min) of SiCl₄ and 200sccm of H₂ diluted with N₂ to a total flow rate of 1000sccm. Small pieces of Si wafer with as-grown nominally undoped NWs were placed in small vials containing 2mL of anisole. NWs were dispersed by using ultrasonic agitation at low power (≈200W) for 10s to 15s. The homogeneous as-grown and dispersed SiNWs exhibited an average 22µm length and ≈75nm diameter (FIG.1), as analyzed by Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM), respectively. TEM studies confirmed [111] growth direction of NWs. The NWs' diameter was also evaluated and confirmed from the Atomic Force Microscopy (AFM) results (not shown).

A DEPtech 3DEP microwell electrode system was used for the determination of the DEP-frequency response of SiNWs dispersions. The 3DEP electrode chip contained 20 wells of 1mm diameter, each comprising eight gold-plated copper electrodes in a ring configuration separated by polyimide layers, with thicknesses of 70 μ m of copper and 150 μ m of polyimide, with a cross-section schematic shown in FIG.2(a). For each experiment, approximately 75 μ L of SiNWs dispersed in anisole were injected into the wells of the electrode chip. The principle of operation of the 3DEP is based on the attraction of nanoparticles towards the imbedded electrodes during positive DEP, resulting in a reduction of light scattering, and repulsion from the electrodes during negative DEP, leading to an increased light scattering, when an alternating electric signal is applied to the electrodes. The relative strength of the dielectrophoretic force can be evaluated by measuring the changes of the transmitted light intensity through the well, for each applied DEP signal frequency. During the experiment, each of the 20 wells received a different frequency energizing signal in the range 1kHz–20MHz, at peak-to peak signal (V_{pk-pk}) of 10V. The applied frequency remained constant for each well during the experiment. Wells were excited with AC signal for 60s, during which NWs were expected to experience positive DEP, and to

nove away from the well center. Software was then used to assess the change in NW distribution by **bishing** measuring the change in light intensity within each well, as the NWs, suspended in anisole, reoriented and moved in response to the applied field. The change in light intensity was normalized to intensity of the image of the well captured before applying the electric field, and the relative dielectrophoretic force acting on NWs was then related to the changes of light intensity. When dispersed NWs experience a DEP force in a liquid, they reach their terminal velocity in milliseconds, and, so for any observed movement we can assume that velocity is proportional to the DEP force (F_{DEP}) exerted on the particle. F_{DEP} for NWs with cylindrical shape is commonly approximated to that of a prolate ellipsoid with major and minor axes equal to the nanowire length and diameter using the relationship given by Equation 1(a-c)²⁶⁻³¹:

$$\mathbf{F}_{\mathbf{D}\mathbf{E}\mathbf{P}} = \frac{2L\pi r^2}{3} \boldsymbol{\varepsilon}_m \mathbf{R} \boldsymbol{e} \{ K_f \} \nabla E^2 \quad (1a)$$
$$K_f = \frac{\tilde{\varepsilon}_p - \tilde{\varepsilon}_m}{\tilde{\varepsilon}_m} \qquad (1b)$$
$$\tilde{\varepsilon}_p = \boldsymbol{\varepsilon} - j \frac{\sigma_p}{\omega}, \quad \tilde{\varepsilon}_m = \boldsymbol{\varepsilon} - j \frac{\sigma_m}{\omega} \qquad (1c)$$

where, *r* is NW radius, *L* is NW length, ε_m is the permittivity of the fluid medium and is the gradient of the electric field strength squared, K_f is the Clausius-Mossotti factor and *Re* denotes "the real part of". $\tilde{\varepsilon}_p$ is the permittivity of NW, $\tilde{\varepsilon}_m$ is the permittivity of the medium, ε_o is the vacuum permittivity, σ_p is the conductivity of NW, σ_m is the conductivity of the medium and ω is the angular frequency of the electric field.

Examination of Equation 1a shows that the DEP force scales with particle volume. This means that small-volume nanoparticles typically require larger ∇E^2 , which is usually obtained by using electrodes with small gap sizes. However, the electrodes gap in the commercial 3DEP chip is 150µm. Nevertheless, the nature of semiconducting NWs is that the dipole along the long axis is sufficiently substantial to

Publishing alignment is observed even at distances few tens of microns away from these electrodes.

The dielectrophoretic force spectrum of undoped VLS grown SiNWs obtained by this method is shown in FIG.2(b). The points represent the mean (n=3) DEP system response at different frequencies; the solid line represents the best fit of the data. The graph shows a plateau response between 1kHz and 100kHz, followed by a decrease of relative DEP force at around 1MHz signal frequency. At frequencies 10MHz–20MHz, the DEP force reaches lower, however non-zero values, indicating that a smaller population of NWs is still able to respond to the DEP field.

Whilst VLS growth of SiNWs could be expected to provide a mono-dispersed collection of nanowires, both in terms of their lengths and electrical properties, the frequency range over which the DEP dispersion takes place (beginning at *ca*. 1kHz and continuing to over 20MHz) suggests a range of NW conductivity heterogeneity; the dispersion of electrically homogeneous NWs would typically take one decade to move from <10% of the transition to >90% 32 . We note that VLS growth provides silicon nanowires with highly consistent lengths and diameters, unlike Supercritical-Fluid-Liquid-Solid synthesis we have reported previously¹⁸, so in the current study we can disregard the influence of morphological properties such as length and diameter on the DEP response characteristics.

As the frequency increases, the dipole across the nanowires weakens, causing the relative DEP force to drop, so that NWs with the lowest conductivity will exhibit DEP assembly only at low frequencies. The variations in conductivity are expected to originate from the crystal quality of the NWs, such as the concentration of surface and crystalline defects and associated traps. However, at higher frequencies we predict that F_{DEP} will reach a plateau, where highest conductivity nanowires can still be collected, and then decline close to zero DEP force. For DEP nanowire assembly this means that SiNWs with various conductivity properties will respond to the DEP signal in the range from few Hz to approximately few hundred kHz, as shown in FIG.2(b), resulting in a collection of nanowires with an average mediocre

A conductivity properties, whereas DEP assembly at high frequencies 10-20MHz will results in the **Publishing** collection of exclusively highest quality and highest conductivity nanowires. In relation to other semiconducting nanowires and nanomaterials such as groups IV, III-V, and II-VI etc., we anticipate that DEP threshold frequency separating the collection of good and bad quality nanoparticles will vary according to their different doping levels and corresponding charge carrier mobilities, and will need to be determined experimentally.

The electrical properties of the SiNWs collected at different frequencies were investigated by FET analysis to establish a direct correlation with the effective DEP force spectrum. The FET devices were prepared on Si/SiO₂ substrates, with pre-patterned source-drain electrodes with 10µm gap, where highly doped Si substrate served as the bottom-gate electrode. The dielectrophoretic bottom-contact structures consisting of 2nm Ti acting as an adhesion metal followed by 50nm gold (Au) or palladium (Pd) layers were patterned with photolithographic lift-off technique. The choice of the contact metals is dictated by p-type conductivity that is usually observed in undoped SiNWs.³³ Both Au and Pd metals workfunctions are closely matched to the valence band edge of Si to enable near-Ohmic contact for ptype transport.³⁴ The alignment of the SiNWs was performed using DEP by applying an AC field across two electrodes (at V_{pk-pk}=12V) forming the source-drain contacts of the FET device. The substrate was placed on an inclined surface ($\approx 30^{\circ}$ versus the horizontal plane) to allow NW dispersion to flow along the substrate and to cross the dielectrophoretic electrodes, as described previously.¹⁸ A 10µL-20µL drop was placed on top of the dielectrophoretic structures after the AC field was applied from an AIM-TTI TG120-20MHz function generator. After alignment, the substrates were gently rinsed with IPA to remove weakly attached NWs, followed by gentle drying with nitrogen flow. An example of aligned monolayer of nanowires across FET electrodes with 10µm gap is shown in FIG.3a-b. The fabrication of the FET devices was completed by performing a second lift-off process to deposit 80nm thick metal contacts on top of the aligned NW for the improvement of the charge carrier injection. Prior to the metal

A deposition, the edges of the NWs at the source-drain contacts regions underwent a diluted hydrofluoric **Publishing** acid freatment for 12s to remove the native oxide layer of the NWs³⁵⁻³⁷ thereby forming a "clean" semiconductor-electrode contact region. Following metal layer deposition, a brief sonication (\approx 10s) at low power (\approx 200W) was applied to conduct lift-off structuring of the electrodes, and the same time preserving the integrity of nanowires. The final step included the post-anneal of the FET devices at 250°C–300°C for 45min to improve the metal-semiconductor contact for optimum charge transport characteristics.⁴ A schematic of the bottom-gate FET device with Au contacts is shown in FIG.4(b). The transistors were characterized using a Keithley 4200 SCS analyzer system in a N₂-filled glove box in order to minimize effects of atmospheric contamination.

Typical transfer characteristics of FETs prepared with NWs aligned at various DEP frequencies are shown in FIG.4(a). The transfer characteristics were normalized to the number of NWs that bridge the source–drain electrodes, typically between 50 and 230 nanowires. FET devices with NWs aligned at higher DEP frequencies (10MHz and 20MHz) consistently demonstrated higher currents, highlighting nanowires' superior conductivity properties.

In order to evaluate the FET performance, the sub-threshold slope (s-s), the trap density (N_{trap}) and mobility were calculated as a function of DEP frequency. The sub-threshold behavior (V/decade) indicates how much gate voltage is needed to turn-on the transistor, and, in addition to the FET geometrical parameters, it also depends on the density of defect/trap states on the NW surface or at the NW/dielectric interface. Thus, higher trap density results in less steep current increase and high subthreshold values. The sub-threshold slope is given by Equations 2^{38, 39} and 3³⁴, and is related to the trap density (N_{trap}) according to Equation 4^{40, 41}:

$$s - s = \ln(10) \frac{\left(1 + \frac{C_{it}}{C_{box}} + \frac{C_{si}}{C_{box}}\right)}{\left(\frac{q}{kT} - \frac{1}{E_{bnw}^{2r}}\right)} \quad (2)$$
$$s - s = \frac{\Delta V_G}{\Delta \log I_D} \quad (3)$$



This manuscript was accepted by Appl. Phys. Lett. Click here to see the version of record. $N_{trap} = \left[\frac{q(s-s)\log(e)}{kT} - 1\right] \frac{C_{NW}}{2\pi NrLa} \quad (4)$

where, k is the Boltzmann's constant, T is absolute temperature, q is the electron charge, E_{bnw} is the field at the bottom of the SiNW, C_{it} is the capacitance of interface states at the Si oxide-shell/Si region of the NW, C_{si} is the capacitance of the SiNW, and C_{box} is the back oxide capacitance (SiO₂), C_{NW} is the total gate capacitance, N is the total number of NWs across the channel.

The carrier mobility (μ) was calculated using the cylinder-on-plate model which takes into consideration the electrostatic fringing effect acting on the finite number of NWs in the channel as shown in Equations 5 and $6^{18, 42-45}$:



where, ε_r is the SiO₂ dielectric constant (3.9), *d* is the thickness of the gate dielectric (230nm), V_{SD} is the applied source-drain voltage and g_m is the transconductance $(g_m = \frac{\partial I_D}{\partial V_G})$.

The sub-threshold swing, trap density and mobility of the devices shown in FIG.4(a) as a function of DEP alignment frequency are presented in Table 1. Furthermore, similar data from a number of devices fabricated at a range of DEP signal frequencies (30Hz, 300kHz, 10MHz, 20MHz) are also shown in FIG.4(c). It is clear, that SiNWs aligned at the low DEP frequencies (30Hz and 300kHz) showed low maximum on-state current at the gate voltage (V_G) of -40V (FIG.4d). For NWs collected at the high frequencies (10MHz and 20MHz), the FETs showed a significantly improved performance, with two orders of magnitude higher current (per nanowire), 50% lower sub-threshold swing and with up 100 times higher mobility values as compared to FETs with NWs collected at low frequencies (see Table 1, FIG.4c-d). The increase of the mobility values from low to high frequencies can be attributed to several factors, including the collection of nanowires with higher crystal quality and lower densities of defects

A and traps states, which all affect the ability of the nanowires to respond to the fast oscillating external **Publishing** non-uniform DEP field.¹⁸ The reduction of subthreshold slope and nanowire surface trap density for FET devices containing nanowires collected at 20MHz provides further support of the selective propertied of the DEP process to assemble nanowires with lower trap density.

Finally, to evaluate the range of maximum on-currents that can be supported by a high quality NW FET, a device with approximately 200 nanowires in the channel was prepared by assembling nanowires at 20MHz DEP signal frequency. This device was capable of supporting a total current of ≈ 0.65 mA (V_G=-40V, V_D=-25V) high on/off ratio of 10⁵ and the hole mobility of 16±2.3cm²V⁻¹s⁻¹.

In summary, our results demonstrate that NWs grown in the same controllable CVD process, still have significant variations in properties as evidenced by the FET data for nanowires collected at various DEP frequencies. By analyzing the frequency spectrum obtained using the 3DEP system, we obtain a direct correlation between the properties of NWs collected at different frequencies and the corresponding FET characteristics. Thus, by altering the dielectrophoretic frequency, high or low quality NWs can be discriminated. DEP aligned NWs in the high frequency range (10MHz and 20MHz) showed up to 100 times higher on-current and carrier mobility values as compared to the lower frequency range (30Hz, 300kHz). We propose that beyond the immediate application for SiNWs, 3DEP analysis can be applied for efficient evaluation the properties of a wide variety of nanostructures such as metallic and semiconducting nanowires, carbon nanotubes and nanoflakes.

ACKNOWLEDGMENTS

M.C. thanks A.G. Leventis Foundation for providing an Educational Grant. S. K. acknowledges support from the U.S. Department of Commerce, National Institute of Standards and Technology under the financial assistance award 70NANB16H043.

TABLES and FIGURES CAPTIONS



Sub-threshold swing, trap density and mobility values of the FET devices shown in FIG. 4a.

DEP Frequency	S - S	N_{Trap}	μ (cm ²
(Hz)	(V/decade)	(cm^{-2})	$V^{l}s^{-l}$)
30	4.1	$1.7 \mathrm{x} 10^{13}$	0.1
300 k	5.0	2.1×10^{13}	0.06
10 M	2.1	8.9×10^{12}	7.05
20 M	2.6	1.1x10 ¹³	8.7

FIG. 1 (a) SEM image (30° tilt) of CVD-grown Si NWs. (b) low- and (c) high-resolution TEM images of a typical Si NW with ~70 nm Si core and ~2 nm thick shell of native oxide. Inset in (c) shows the corresponding selected area electron diffraction pattern.

FIG. 2 (a) A cross-section schematic of the 3D well electrode chip used in this work. Wells, that are filled with nanowire dispersions, are 1mm in diameter and encircled by 70µm thick electrodes separated by 150µm gap. The nanoparticles can either be attracted towards the electrodes (the walls of the well) by applying a positive DEP or repelled from the electrodes by applying a negative DEP. The movement of the nanowires is tracked by image analysis and detected by measuring the light intensity of the beam passing through the well for a period of 60 seconds. (b) Relative DEP force (arbitrary units) as a function of DEP signal frequency for SiNWs suspended in anisole generated by the commercially available 3DEP system reader (3DEP by DEPtech, Uckfield, UK). The points represent the mean DEP response of three independent experiments. The solid red line represents the best fit. Error bars were evaluated from the fluctuations of light intensity due to NWs random movement in the liquid.

FIG. 3 (a) Polarized microscope image (POM) and (b) SEM image of SiNWs aligned across 10µm FET channel gaps via DEP. POM imaging was used to evaluate the total number of nanowires crossing the FET electrodes.

FIG. 4 (a) Transfer characteristic of FETs with NWs aligned *via* DEP at 30 Hz, 300 kHz, 10 MHz and 20 MHz. The plot is normalized to the number of NWs across the FET channel, thus showing an average current per NW. (b) Schematic of a bottom-gate SiNW FET device with Au source-drain contacts. Layer thickness: Si substrate 675 μ m, SiO₂ 230nm, first Au contact layer 50nm, second Au contact layer on top of nanowires 80nm. Source-drain contact gap 10 μ m. (c-d) Typical performance data, including sub-threshold swing (s-s), trap density (N_{trap}), mobility (μ) and normalized on-current (I_{ON}) for a number of FET devices with nanowires aligned at 30 Hz, 300 kHz, 10 MHz and 20 MHz.

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