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First results on the ATLAS HL-LHC H35DEMO prototype

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ABSTRACT: This article presents the first measured results from the H35DEMO pixel demonstrator. The H35DEMO is a prototype ASIC in the 0.35 μm High Voltage-CMOS (HV-CMOS) process from ams aimed at proving that HV-CMOS sensor technologies are suitable as tracking detectors for the ATLAS High Luminosity-LHC (HL-LHC) upgrade. The prototype was fabricated in an engineering run, in which wafers with four different substrate resistivities, ranging from the standard value of $20\,\Omega \cdot \text{cm}$ to a high value of $1\,\text{k}\Omega \cdot \text{cm}$, were used to increase the depletion region of the sensor. The prototype includes four large area matrices and a few test structures. New experimental set-ups have been developed to measure the ASIC with radioactive sources and laser beams. The experimental set-ups and the measured results obtained will be discussed in this article.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Front-end electronics for detector readout; Radiation-hard electronics

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1 Introduction

The industry standard High Voltage-CMOS (HV-CMOS) technology is a very attractive option to develop a new generation of fast and radiation tolerant position sensitive detectors [1]. Tracker detectors in HV-CMOS technologies are unique in the sense that they combine a high bias voltage to create a wide depletion region in the bulk substrate material, which is needed for fast signal collection and high radiation tolerance, and high integration density of CMOS electronics. These detectors are in principle able to meet the extreme demands of future experiments in particle physics, such as the ATLAS inner tracker upgrade (single bunch crossing resolution of 25 ns and expected radiation of some $10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ at the outer pixel layers) [2], the Mu3e experiment (extremely lightweight silicon pixel detector of $50 \mu\text{m}$ with precise time accuracy) [3] and the future linear colliders ILC and CLIC (10 ns time stamping capabilities) [4, 5].

The H35DEMO is an HV-CMOS pixel demonstrator aimed at proving that this sensor technology can be qualified as a tracking detector for the pixel silicon layers of the ATLAS High Luminosity-LHC (HL-LHC) upgrade. The demonstrator is in the $0.35 \mu\text{m}$ HV-CMOS process from ams. It has a total area of $18.49 \text{ mm} \times 24.40 \text{ mm}$, the maximum area allowed by the foundry. The design comprises two monolithic matrices and two analogue matrices with a large number of pixels, and a few test structures for sensor characterization. The monolithic matrices have analogue and digital readout electronics on-chip — the analogue readout electronics in the collecting electrode and digital readout electronics at their periphery. The analogue matrices have analogue readout electronics only in the collecting electrode and a readout ASIC such as the FE-I4 is needed to process and extract the generated data. The ASIC was fabricated in an engineering run on 8 inch wafers with four different substrate resistivities, which are $20 \Omega \cdot \text{cm}$ (standard value), $80 \Omega \cdot \text{cm}$, $200 \Omega \cdot \text{cm}$ and $1 \text{ k}\Omega \cdot \text{cm}$, to widen the sensor depletion region and therefore improve the sensor signal-to-noise ratio (SNR).

Each pixel has a total area of $50 \mu\text{m} \times 250 \mu\text{m}$ for compatibility with the FE-I4 readout ASIC. The sensor is implemented by means of a deep nwell/p-substrate junction, on top of which sits the readout circuit. The deep nwell or collecting cathode is biased at the power supply voltage (i.e.,

3.3 V in the present technology) through a bias circuit that works as a high ohmic resistor, whilst the p-substrate or anode is biased at a negative high voltage. In all the matrices, the readout circuit includes a bias block, a charge sensitive amplifier (CSA) that is capacitively coupled to the deep nwell, and a passive RC-CR filter. In addition, the pixels in the first monolithic matrix have nMOS discriminators inside the sensing area, whereas in the second monolithic matrix the digitization of the sensor induced signal is done with CMOS comparators placed at the periphery of the matrices. In the first monolithic matrix, the first half of the pixels have simple nMOS comparators and the second half of the pixels have complex nMOS comparators with special electronics to compensate time-walk variations. All the pixels of the monolithic matrices are connected to a digital readout cell in the periphery in a one-to-one connection. The digital cells present the same functionality as the FE-I3 readout ASIC [6]. For testing purposes, the CSA output of a few pixels can be connected to a monitor line. More details about the design aspects of the H35DEMO can be found in [7].

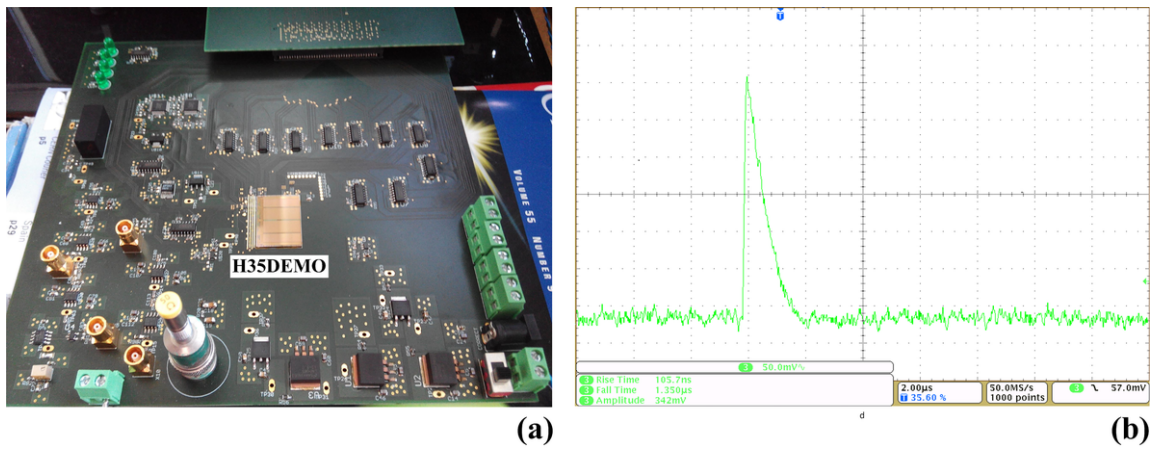


Figure 1. Custom made pcb (a) and CSA output when irradiated with a Sr90 source (b). In this particular measurement, the rise time of the sensor is 105 ns, the fall time 1.35 μ s and the amplitude 342 mV.

2 Source measurements

A new experimental set-up based on a custom made pcb designed at Liverpool and a ZC706 evaluation board from Xilinx has been developed. In this set-up, all the connections between the ASIC and the peripheral pads on the pcb are made by wire-bonding. Low-voltage differential signaling (LVDS) links between the pcb and the FPGA development board are through an FPGA mezzanine card (FMC) connector. With this pcb, it is only possible to measure the monolithic matrix with nMOS comparators inside the pixel area. Figures 1a,b show the custom made pcb and the monitor line that corresponds to the CSA output of one pixel with a simple nMOS comparator of the matrix in the standard resistivity of $2 \Omega \cdot \text{cm}$ when biased at -60 V and irradiated with a Sr90 source. This demonstrates that the ASIC works well. Features such as gain and speed of the sensor are within expected values according to Cadence simulations. Further measurements with this set-up are already planned.

3 Edge-TCT measurements

Samples of the H35DEMO fabricated with a high resistivity wafer of $1 \text{ k}\Omega \cdot \text{cm}$ were backside processed at Ion Beam Services (IBS) to allow backside biasing, as this feature is not offered by the foundry, and thus achieve a stronger, more uniform electric field in the sensing volume. The backside processing consists of thinning to $100 \mu\text{m}$, backside p^+ implantation with boron (dose of $5 \cdot 10^{14} \text{ at/cm}^2$), thermal annealing and backside metallization to a thickness of 1022 nm with titanium and aluminium. To study the electric field and the depletion region of the detector, edge-Transient Current Technique (edge-TCT) measurements [8] were performed on a test structure based on a small 3×3 matrix of HV-CMOS pixels without on-chip readout electronics. The sensor area and cross-section in this small matrix is the same as in the other larger matrices of the ASIC. To show and compare the advantages of backside biasing in HV-CMOS detectors, edge-TCT measurements were done on a sample biased from the back and a standard sample biased from the top.

3.1 Experimental set-up

The experimental set-up is based on a TCT/edge-TCT system and a user interface from the company Particulars [9], and it uses an analysis script prepared by DESY. The experimental set-up is shown in figure 2. The results presented here correspond to the edge-TCT technique only. With this system, the edge of the device under test (DUT) is scanned with a focused and collimated pulsed laser beam of infrared light ($\lambda = 1064 \text{ nm}$, as the absorption length of silicon allows photons to penetrate the sensor active volume, $\approx 350\text{--}400 \text{ ps}$ pulse width, 1 kHz repetition rate and $1 \mu\text{m}$ scan step). Motorized XYZ stages are used to control the position of the laser beam and the DUT. In response to the laser beam, electron-hole pairs are created inside the targeted detector volume

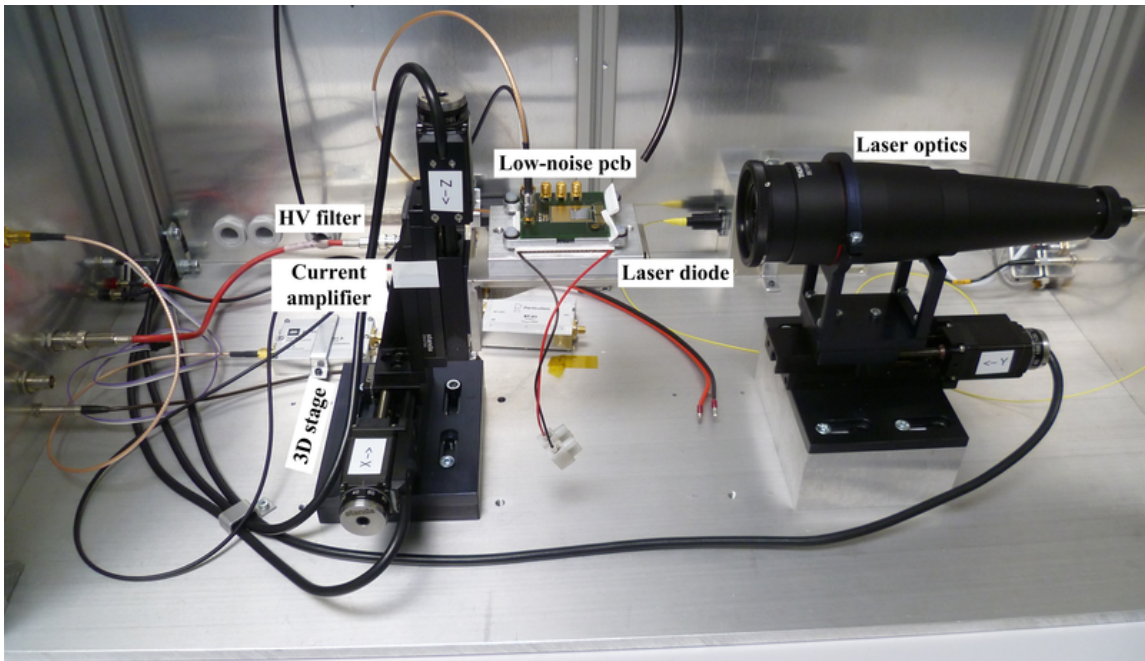


Figure 2. Experimental set-up for edge-TCT measurements.

emulating a signal due to minimum ionizing particles (MIP). The generated carriers drift in the electric field and induce current which is read out by an off-chip amplifier connected to the collecting electrode. In our case, the collecting electrode is the deep nwell of the central HV-CMOS pixel, as the 8 neighboring pixels are grounded. The amplified signal is monitored and recorded using an oscilloscope. By integrating this signal over the collection time with the analysis script, it is possible to map the collected charge as a function of the position at which the charge was generated in the bulk of the sensor and therefore obtain information about the detector depletion region. More details of the edge-TCT set-up and measurement technique can be found in [8].

The edge of the detector was polished to avoid light diffraction in the experiment. The polishing procedure applied to the detector consists of two steps. In the first step, the ASIC was coarse polished with a $3\text{ }\mu\text{m}$ grit lapping sheet. In the second step, it was fine polished with $1/10\text{ }\mu\text{m}$ grade diamond paste and cotton bud. The HV-CMOS ASIC sits on a custom developed ultra low-noise pcb designed at Liverpool. The beam size and focusing position were calculated using the knife-edge-technique [10]. To find the focus, the DUT was placed in the experiment and scanned in the Z direction with different focus values (Y position of the laser). The focus was identified as the position where the beam width was minimum ($\approx 5\text{ }\mu\text{m}$). Once the focus was found, vertical scans were done at different voltages. This scan provided a depth profile of the depletion region in the sensor. All the measurements were performed at room temperature.

3.2 Measured results

The charge collection profile along the pixel for back biased and top biased samples are presented in figures 3a,b, respectively. It can be clearly seen in figure 3a that the charge collection region is around $100\text{ }\mu\text{m}$ wide (the surface is at $200\text{ }\mu\text{m}$ and the backside at $100\text{ }\mu\text{m}$), therefore the sensor is fully depleted. This measured result is in good agreement with our TCAD simulated results [11]. The fact that the sensor is fully depleted at low biasing voltages of -40 V is also a remarkable aspect. At very low biasing voltages, however, it is possible to see a second peak close to the backside of

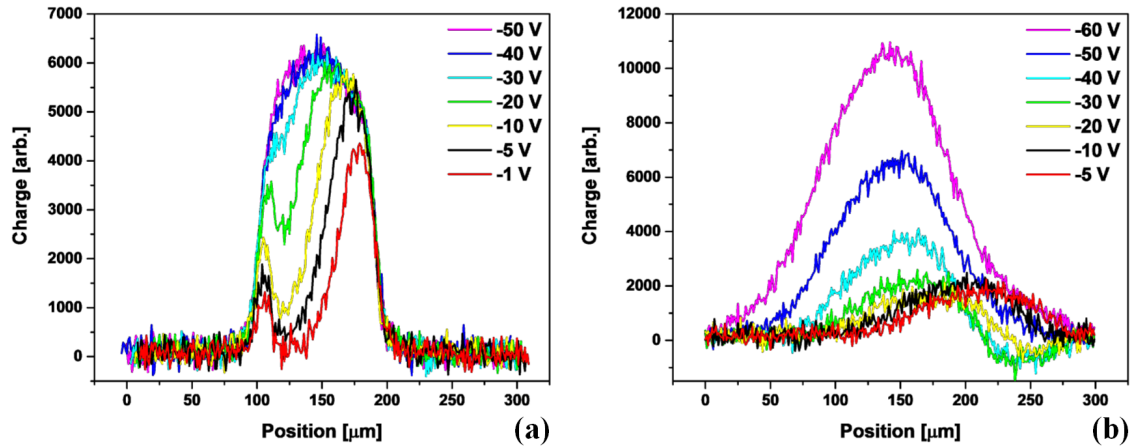


Figure 3. Charge collection profile of a $1\text{ k}\Omega\cdot\text{cm}$ H35DEMO when: the sensor is back thinned to $100\text{ }\mu\text{m}$ and biased from the back (a) and the sensor has the standard thickness of $700\text{ }\mu\text{m}$ and it is biased from the top (b). In both cases, the measurements were performed at room temperature.

the chip. This happens because the sensor is implanted in the back with boron and annealed at low temperatures. As a result of this, not all the boron is properly activated and the lattice damage not fully recovered. A gradient of effective space charge and therefore an electric field is created, as typically happens with irradiated sensors. This peak cannot be seen in figure 3b, as the top biased sensor lacks a backside implantation. This plot does not show the full thickness of the detector, which is $700\text{ }\mu\text{m}$, but it demonstrates that the depleted region is not well defined for top biased high-resistivity HV-CMOS sensors. Similar results with top biased high resistivity HV-CMOS sensors have been obtained by others [12]. It can also be seen in figures 3a,b that the amount of collected charge is different for the backside and topside biased detectors. The amount of collected charge depends on the laser power, which can vary, and therefore this parameter cannot be compared between different measurements. This issue could be solved with beam intensity monitoring.

4 Conclusion

Custom experimental set-ups have been developed to measure different circuits of the H35DEMO, a pixel demonstrator for the silicon tracking layers of the ATLAS HL-LHC upgrade. The utilization of a Sr90 radioactive source has shown that the detector works well, with fast large amplitude induced signals. The characterization with an edge-TCT set-up of a 3×3 matrix of HV-CMOS pixels in a high resistivity substrate of $1\text{ k}\Omega \cdot \text{cm}$, thinned to $100\text{ }\mu\text{m}$ and backside processed to allow sensor biasing from the back has demonstrated that the sensor is fully depleted at low biasing voltages of -40 V .

Acknowledgments

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