Total Ionizing Dose Response of High-*k* Dielectrics on MOS Devices

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Abstract

As advanced Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) technology continues to minimize the gate oxide thickness, the exponential increase in gate leakage current poses a major challenge for silicon dioxide (SiO_2) based devices. In order to reduce the gate leakage current while maintaining the same gate capacitance, alternative gate insulator materials with higher dielectric constant (high-*k*) became the preferred replacement of SiO_2 gate dielectrics. Germanium (Ge) MOSFETs have been regarded as promising candidates for future high-speed applications because they possess higher carrier mobility when compared to silicon based devices. At present, advanced microelectronics devices and circuits are used in aerospace engineering, nuclear industry, and radiotherapy equipment. These applications are unavoidably exposed to space-like radiation, which has a relative low radiation dose rate at 10^{-2}-10^{-6} rad(Si)/s. For these reasons, it is necessary to understand the low-dose-rate radiation response of high-*k* materials based on Si and Ge MOS devices. The radiation response of high-*k* materials such as radiation-induced oxide and interface trap density have been typically examined by carrying out off-site capacitance-voltage (CV) measurements. However, the conventional and off-site radiation response measurements may underestimate the degradation of MOS devices. In this study, a semi-automated laboratory-scale real-time and on-site radiation response testing system was developed to evaluate the radiation

response. The system is capable of estimating the radiation response of MOS devices whilst the devices are continuously irradiated by γ-rays. Moreover, the complete CV characteristics of MOS capacitors were measured in a relatively short time. The pulse CV measurement reduces the impact of charge trapping behavior on the measurement results, when compared to conventional techniques. The total ionizing dose radiation effect on HfO_2 dielectric thin films prepared by atomic layer deposition (ALD) has been investigated by the proposed measurement system. The large bidirectional ΔV_{FB} of the irradiated HfO_2 capacitor was mainly attributed to the radiation-induced oxide trapped charges, which were not readily compensated by bias-induced charges produced over the measurement timescales of less than 5 ms. Radiation response of Ge MOS capacitors with HfO_2 and $Hf_xZr_{1-x}O_y$ gate dielectrics was also investigated. It was found that radiation-induced interface traps were the dominant factor for Flat-band Voltage shift (ΔV_{FB}) in HfO_2 thin films, whereas the radiation response for Zr-containing dielectrics under positive bias was mainly affected by oxide traps. Under positive biased irradiation, the Zr-doped $Hf_xZr_{1-x}O_y$ exhibited smaller ΔV_{FB} than that of HfO_2. This is attributed to the de-passivation of Ge-S bonds in capacitors incorporating HfO_2 thin films, resulting in the build-up of interface traps. Under negative biased irradiation, ΔV_{FB} was attributed to the combined effect of the net oxide trapped charges and the passivation of Ge dangling bonds at the Ge/high-*k* interface.

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List of Acronyms

Term	Initial components of the term
IC	Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
ΔV_{FB}	Flat-band voltage shift
CV	Capacitance-Voltage
Ge	Germanium
ALD	Atomic Layer Deposition
SiO_2	Silicon dioxide
high-*k*	High dielectric constants
EOT	Equivalent Oxide Thickness
Al_2O_3	Aluminum oxide
HfO_2	Hafnium oxide
ZrO_2	Zirconium oxide
Ta_2O_5	Tantalum pentoxide
TiO_2	Titanium dioxide
CeO_2	Cerium oxide
La_2O_3	Lanthanum oxide
Y_2O_3	Yttrium oxide
Tm_2O_3	Thulium oxide
Nd_2O_3	Neodymium oxide
γ–ray	Gamma-ray
EHPs	Electron/Hole Pairs
ΔV_{mg}	Mid-gap voltage shift
ΔV_{TH}	Threshold voltage shift

I-V	Current-Voltage
RCA	Radio Corporation of America
HF	Hydrofluoric acid
NH_3H_2O	Ammonium hydroxide
HCl	Hydrochloric acid
MOCVD	Metal Organic Chemical Vapor Deposition
$(CH_3)_2N]_4Hf$	Tetrakis (dimethylamido) hafnium (IV)
RTA	Rapid Thermal Annealing
EDS	Energy Dispersive Spectrometer
OTF	On-the-fly
ICRP	International Commission on Radiological Protection
NCRP	Radiation Protection and Measurements
NIST	National Institute of Standards and Technology
TLDs	Thermoluminescent dosimeters
PBI	Positive biased irradiation
NBI	Negative biased irradiation

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Chapter 1: Introduction

1.1 Review of High-*k* Materials

Over the past few decades, the improvement of integrated circuit (IC) performance was mainly due to the exponential increase in the number of complementary metal oxide semiconductor (CMOS) transistors on a silicon ship. This exponential increase is known as Moore's Law, which states the number of transistors on a chip would double every 2 years [1, 2]. For the past 50 years, the semiconductor industry has kept pace with this prediction, which requires the size of transistors to continuously decrease [3, 4].

In 2016, some semiconductor manufacturers at the leading edge have achieved 16-nm technology or even smaller gate length such as: Intel-14 nm, Qualcomm-10 nm, and TSMC-16 nm. Meanwhile, the gate oxide area of transistors has been scaled with the decreasing of gate length. To keep superior controllability of metal gate to the channel of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), it is necessary to maintain the capacitance density of gate oxide. Therefore, the gate oxide thickness has also continued to shrink since the gate capacitance of devices is inversely proportional to gate oxide thickness as shown in Eq.1.1:

$$C_{ox} = \frac{A \cdot \varepsilon_{ox}}{t_{ox}} \qquad (1.1)$$

where C_{ox} is the gate oxide capacitance, A is the gate area, ε_{ox} and t_{ox} are the dielectric constant and physical thickness of gate oxide.

Before 2007, silicon dioxide (SiO_2) has been employed as the gate oxide for commercial transistors as it has large band gap, good reliability, and high thermodynamic stability on silicon. To obtain the scaling of MOSFETs, the gate oxide layer has been continuously downscaled. However, the rate at which the thickness of gate oxide decreased was steady for years but started to slow at the 90-nm generation, which went into production in 2003 [5-7]. Devices with gate oxides thinner than 5 nm exhibit large gate leakage current because a part of carriers can directly tunnel between gate electrode and substrate. In other words, Metal-Oxide-Semiconductor Field-Effect Transistor are nearly approaching the physical scaling limitation with SiO_2 technology [8, 9].

Therefore, the gate oxide layer had to be physically thick enough to prevent electrons tunneling while maintaining relative high gate capacitance. As indicated in Eq.1.1, the gate capacitance of MOSFET is inversely proportional to the gate oxide thickness but proportional to the gate oxide dielectric constants (ε_{ox}). To meet the requirements of reducing the gate leakage currents and scaling down the transistor size with further increase in the gate capacitance for better channel control, alternative gate insulator materials with higher dielectric constants (high-*k* materials) are considered as a replacement for SiO_2 gate dielectric. By using high-*k* materials, the equivalent oxide thickness (EOT) of devices is less than 10 Å and significantly smaller leakage currents

are observed compared to that of SiO_2 [10-13]. Equivalent oxide thickness is used for representing the effect of high-*k* thin films to the decrease in gate oxide thickness, as indicate in Eq. 1.2:

$$\mathrm{EOT} = \frac{t_{ox(high-k)}\varepsilon_{SiO2}}{\varepsilon_{ox(high-k)}} \qquad (1.2)$$

Where $t_{ox(high-k)}$ is the physical thickness of high-*k* thin films, $\varepsilon_{ox(high-k)}$ is the permittivity of high-*k* thin films, and ε_{SiO2} is the dielectric constant of silicon dioxide (3.9). Several high-*k* candidates have been under consideration, such as Aluminum Oxide (Al_2O_3), Hafnium Oxide (HfO_2), Zirconium Oxide (ZrO_2), Tantalum Pentoxide (Ta_2O_5), Titanium Dioxide (TiO_2), Cerium Oxide (CeO_2), Lanthanum Oxide (La_2O_3), and their silicates [14-16]. Besides the permittivity requirements, gate oxides have to be thermally and chemically stable when in contact with Si in order to prevent reacting with Si. It is essential to avoid the formation of silicide during the deposition and other high temperature integration processes. Furthermore, the candidate material is required to have relative high bandgap to reduce the leakage current. Much effort has been expended to identify the most promising high-*k* dielectrics after considering the requirements mentioned above [17-19]. The permittivity and bandgap of several potential candidates has been demonstrated and listed in Table 1-1-1. It is a crucial requirement to identify with certainty the feasibility of these promising high-*k* candidates.

With regard to group III candidates, Al_2O_3 is the most widely investigated as it has relatively large bandgap (8.7 eV) and high thermodynamic stability on silicon.

Excellent reliability characteristics was found using Al_2O_3 as an interfacial layer in high-*k*/Al_2O_3/Si stacked MOSFET devices due to its large bandgap [20, 21]. However, a relative large density of negative fixed charges was observed in Al_2O_3 thin films. These negative fixed charges could induce high variations of threshold voltage and device degradation [22]. In addition, the relative permittivity of Al_2O_3 is only 2.3 times larger than that of SiO_2, which has a limited development prospect for the scaling of devices. Another group III candidate Y_2O_3 has attracted considerable attention. It has been reported that epitaxial crystalline Y_2O_3 on silicon could offer higher dielectric constant and better control of interfaces comparing to amorphous SiO_2. Besides, Y_2O_3 has exhibited high thermodynamic compatibility and high conduction band offset ~ 2.3

Table 1-1-1. Relative permittivity and band gap of several potential high-*k* materials [20, 21, 23-32].

Material	Relative Permittivity	Band Gap (eV)	Material	Relative Permittivity	Band Gap (eV)
Al_2O_3	9	8.7	TiO_2	50-80	3.5
Ta_2O_5	20-23	4	HfO_2	15-25	5.8
Y_2O_3	12-15	5.6	ZrO_2	15-25	5
La_2O_3	28-32	4.3	$HfAlO_x$	10-14	5.7-6
Tm_2O_3	12-18	5.8	$LaZrO_x$	15-39	3.5-4.5
Nd_2O_3	10-14	4.7	$Hf_xZr_{1-x}O_y$	20-37	3.7

eV with Si. In spite of these advantages, it was reported that Y_2O_3 deposited via various technologies have exhibited uncertain crystal structures, which is a potential source of gate leakage current and bulk traps in oxide [25, 33].

Rare-earth oxides such as La_2O_3 and Tm_2O_3 have been recently used in the development of MOSFETs. They have relative high effective permittivity and thermodynamic stability on Si. Moreover, superior dielectric integrity and lifetime longer than ten years at 2 V is achieved by the employment of La_2O_3 [26, 34]. The drawback of La_2O_3 and other rare-earth oxides is the lack of ambient stability. La-silicate films are susceptible to $La(OH)_3$ and LaO(OH) formation within minutes of air exposure, which resulting in the decrease of dielectric constant [27, 35].

Titanium dioxide (TiO_2) is a possible candidate due to its extremely high dielectric constant and good thermal stability on Si. The high dielectric constant of TiO_2 benefits from its rutile-type phase which leads to a dielectric constant of approximately 80. Rutile is the most common natural crystal form of TiO_2. Rutile has among the highest refractive indices at visible wavelengths of any known crystal, and also exhibits a particularly large dielectric constant and high dispersion [36, 37]. Another polymorph of TiO_2 is an anatase phase whose dielectric constant is approximately 30, smaller than that of the rutile phase. Enormous efforts have been devoted to the research of TiO_2, which has led to many promising applications, such as memory capacitors, photovoltaics, and photo-/electrochromics sensors. However, very high leakage current density and multi-leakage paths were observed in TiO_2 associated with its relative small

band gap and the presence of oxygen vacancies [28]. A relative thick interfacial layer (more than 2 nm) was required to insulate the gate oxide, which indicated that TiO_2 was difficult to be a long-term solution as an alternative gate insulator [38, 39].

Among the high-*k* materials mentioned in Table 1-1-1, the oxides of hafnium and zirconium dielectrics are most widely employed as they have relatively high dielectric constants of 15-25, relatively large band gap (5.8 eV) and high thermodynamic stability on silicon [29, 40-42]. In January 2007, Intel made the first working 45-nm micro-processors using Hf-based dielectrics with metal gate transistors. Compared with the previous SiO_2-based 65-nm transistors, 45-nm high-*k* plus metal gate transistors provide a 25 percent increase in drive current at the same subthreshold leakage current and greater than 10 times reduction in gate leakage currents [43]. The improvement in drive currents is due to the scaling of gate oxide thickness and increase in channel inversion charge.

There has been much recent research in Zr-based oxides since it has similar bandgap and band offset as HfO_2. ZrO_2 offers the benefit of a higher dielectric constant due to easier stabilization of its tetragonal higher-*k* phase as opposed to the monoclinic phase that is dominant in HfO_2 thin films [30, 44]. However, ZrO_2 did not receive as much attention as HfO_2 because of its poor thermal stability, which may induce chemical reactions within the channel region. To further increase the dielectric constants of Hf-based dielectrics while removing preexisting defects in HfO_2, crystallized HfO_2 in tetragonal phase have been proposed. It was also reported that

HfO_2 and ZrO_2 are almost identical chemically and thus fully miscible [31]. Therefore, $Hf_xZr_{1-x}O_y$ dielectric is introduced as an alternative candidate for advanced gate stack applications. Several studies indicate that $Hf_xZr_{1-x}O_y$ has been shown to be a superior gate dielectric due to its improved device performance and reliability comparing to HfO_2. Addition of ZrO_2 stabilizes the tetragonal phase and enhances the k value in $Hf_xZr_{1-x}O_y$ devices [45, 46]. Similarly, the tetragonal or cubic phases of HfO_2 and ZrO_2 can be stabilized by addition of rare earth elements, such as Lanthanum (La). The dielectric constants were hereby improved with lightly La doped films, with a doping level of around 10 percent. However, the significant enhancement of the dielectric constant for lightly doped films was also accompanied with significant dielectric relaxation. For example, a *k*-value of 40 was obtained at a frequency of 50 Hz for La_2O_3 MOS capacitors, but reduces substantially as the frequency is increased, dropping to 25 at 100 kHz. [32, 47, 48]. Since dielectric relaxation and associated losses impaired MOSFET performance, the larger dielectric relaxation of most La doped dielectrics compared with SiO_2 was a significant issue for their use.

1.2 Total Dose Radiation Effect

At present, advanced microelectronics devices and integrated circuits (ICs) are widely used in satellite communication systems, nuclear power plants and medical equipments. These applications are unavoidably exposed to space-like radiation, which has a relatively low radiation dose rate at 10^{-2}-10^{-6} rad(Si)/s [49-51]. When MOS devices are exposed to ionizing radiation environment, significant degradations would

be induced in their characteristics. Thus, it is a major reliability issue for devices used in radiation environment.

In the 1890s, the effects of X-rays and radioactivity on physical characteristics of solid-state materials were discovered. Meanwhile, the damages of radiation exposure on human tissues were also discovered, these damages were defined as biological radiation effects [50]. However, the need for mechanism study arose a matter of urgency only in the late 1950s, when semiconductor technology began to be used in space and military equipment. These two space-like environments provide radiation exposure to applications which leaves many active semiconductor devices severely damaged. In 1960s, the radiation effects on SiO_2 based semiconductor devices were investigated and reported. The radiation effects were classified into two different types: ionizing radiation and displacement damage. It was found that the major effect to gate dielectrics in MOS devices was ionizing radiation damage [52, 53]. Ionizing radiation degrades a CMOS integrated circuit by producing electron hole pairs in the gate and isolation dielectrics. The related mechanisms will be discussed later in this section.

To date, modern ICs and MOSFETs technologies based on silicon and silicon dioxide have been designed to have excellent radiation hardness [5, 54, 55]. On the other hand, alternative gate insulator materials with higher permittivity has become the preferred replacement of SiO_2 gate dielectrics as we discussed in previous part. However, the effects of radiation to advanced semiconductor devices with high-*k* materials are not completely understood and reported. Very few works have been done

regarding the radiation response of high-*k* materials or other advanced semiconductor technologies such as germanium substrate [56, 57]. Therefore, the charge trapping behavior and long-term reliability of advanced microelectronics devices need to be investigated in details.

The "radiation effects" are the processes of the interactions between high-energy particles and target materials. Various environments likely to have a degrading effect on electronic devices and system: such as space, nuclear reactors, weapons, and controlled fusion. In these radiation environments, there are various radiation sources associated with different types of high-energy particles: gamma rays, X-rays, alpha particles, beta particles, electrons, positrons, neutrons, protons [58]. Gamma rays and X-rays are short–wavelength forms of photon or electromagnetic radiation. A gamma photon has its origin in a nuclear interaction, whereas an X-ray originates from electronic or charged-particle collision. They are lightly ionizing and highly penetrating and leave no activity in the material irradiated [59, 60].

Alpha particles are the nuclei of helium atoms. They have low penetration power and travel in straight lines. Beta particles have the same mass as an electron but may be either negatively or positively charged. With their small size and charge they penetrate matter more easily than alpha particles but are more easily deflected. The proton is the nucleus of a hydrogen atom and carriers a charge of 1 unit. The proton has a mass of 1800 times larger than that of an electron, and has energy levels in the MeV range. A neutron has the same mass as a proton but has no charge and consequently is difficult

to stop. The neutron can be slowed down by hydrogenous materials. The capture of a neutron results in the emission of a gamma ray [61, 62].

The radiation environments present various high-energy particles as discussed above, these particles can pass through electronic applications and react with target materials. However, typical laboratory radiation measurements are commonly carried out by X-ray and gamma ray source [63, 64]. This is because that the other high-energy particles are difficult to produce, and the major radiation damage mechanisms of these high-energy particles to semiconductor devices are similar. Therefore, the radiation sources used in the investigation of radiation response of semiconductor devices are normally X-ray and gamma ray source. Moreover, the establishment of an X-ray testing platform is complex and expensive. Therefore, a Cs^{137} γ-ray radiation source is used to irradiate MOS devices in this study. The activity of the Cs^{137} γ-ray radiation source is 1.11 GBq which gives off 1.11×10^{9} γ-photons per second with energy of 662 keV.

γ-ray is an electromagnetic radiation with very short wavelength and extremely high energy (keV ~ MeV). There are three major effects when γ-ray exposures to a solid state materials: i) Photoelectric effect; ii) Compton effect; iii) Electron pair effect [65]. The photoelectric effect is the emission of electrons or other free carriers when γ photons exposure to a target material. The electrons overcome the bounding energies from the atomic nucleus and become photo electrons, while the energies of the γ photons are totally lost. The compton effect is the inelastic scattering between γ photons and the electron. Part of the energies of the photons are transferred to the electrons.

These electrons receive energies and become recoiling electrons, while the energies and motions of γ photons are changed. Electron pair effect is the transformation of incident high-energy γ photons. When an incident γ photon passes through the atomic nucleus of target materials, the γ photon is transferred to a positive and a negative electrons. The electron pair effect only dominates the γ-ray effect when the γ photon energy is higher than 5 MeV. Since the energy of γ photon in this study is 662 keV, the major effects to the high-*k* thin films are photoelectric effect and compton effect.

The effects of radiation exposure on materials are determined by the interactions between the emitted high-energy particles and the atoms in materials. Dose absorption is used to define the actual energy deposition or the effects of radiation exposure on target materials. In 1960s, rad and gray (Gy) were defined as universal units of energy deposition. A rad has been absorbed by the sample of interest when 100 ergs per gram, and a gray when a 1 joule per kilogram has been deposited. One rad thus equals 10^{-2} gray [62]. In this study, the unit for dose absorption is rad and dose absorption rate is rad per second (rad/s). On the other hand, the atomic structure and atomic mass are different for different materials. Therefore, the energy depositions of various materials have been calculated in section 3.1.3 according to their atomic mass and other element properties. In other words, the total dose absorption for each material has been defined and calculated using its specific dose absorption rate. In this study, the reference of energy depositions for different dielectrics is the total absorption dose, but not the radiation exposure time.

To verify the calculated dose rates, thermoluminescent dosimeters (TLDs) were employed to measure the dose rate at the same position as that of the irradiated high-*k* devices in the radiation response testing system set-up in section 3. Thermoluminescent dosimeters test method was developed by Winokur *et al*. and the preferred method was developed by Fleetwood *et al* [63]. Many crystalline materials exhibit thermoluminescence characteristics, such as lithium fluoride (LiF), calcium fluoride (CaF_2), calcium sulphate ($CaSO_4$) [62]. Electron and hole traps in the thermoluminescent materials are filled during radiation exposure. After the radiation exposure, these trapped electrons and holes are released by heating. Light is emitted when the electrons and holes recombine. In other words, light is emitted when the material is heated after exposure to radiation. In this study, LiF TLDs were used due to the advantages of high-sensitivity and low-cost.

The irradiated LiF TLDs were annealed by an annealing furnace at Soochow University to measure the actual total absorbed dose of the TLDs as a reference for calculated dose rates. Previous results in the literature support that the calibrated dosimetry system with short exposures, followed by a relatively long wait, represents appropriate use of TLDs in calibrating for dosimetry of low dose rates [63]. Hence, a calibrated dosimetry system is employed to perform accurate dosimetry for the low-dose-rate Cs^{137} exposures. The details of the calibrated dosimetry system have been presented in section 3.1.3. The average dose rate obtained from short TLDs exposures is 16% lower than the dose rate of LiF (0.0369 rad/s) calculated from the calculation model established in this study. The results indicated that the dose rate of high-*k*

materials calculated from the calculation model is acceptable.

Advanced semiconductor devices use high-atomic number metal (high-z) as the metal gate and the ohmic contact, such as gold, titanium, aluminum or nickel. If these devices are exposed to ionizing radiation, dose enhancement effects can lead to increased energy deposition in device regions with low-atomic number (low-z), such as gate oxide [66]. The dose enhancement effects are mainly due to the reflection of the high-energy particles from high-z materials that are nearby the gate dielectrics. The reflected particles would pass through the gate dielectric layers, and collide the atoms in gate oxide. Part of these reflected particles has been already passed through the gate dielectrics when they emitted from radiation source. Therefore, the reflected particles lead to an enhancement on total dose absorption of gate dielectrics. The dose enhancement effects on high-z materials are insignificant. In this study, the gate dielectrics used are HfO_2, ZrO_2 and $HfZrO_2$, the metal gate and back contact used is aluminum. Dasgupta *et al*. reported the dose enhancement factors for SiO_2 and HfO_2 under the 400-keV X-ray exposure. The energy of radiation source, thickness of dielectrics and high-z metal materials in this literature is comparable to those in this study. Therefore, the dose enhancement factors in the literature are roughly employed in out calculation model. The details of dose enhancement effects have been presented in section 3.1.3.

Semiconductor devices exposed to irradiation exposure, such as X-ray and Gamma (γ)–ray, typically suffer collisions of high-energy particles and photons. These particles

or photons are able to break atomic bonds and create electron/hole pairs (EHPs) in materials. The device failure and degradation caused by this bond-breaking process is defined as "ionizing radiation damage" [52, 67, 68]. The effects due to these bond-breaking events are to be contrasted with those that occur when atoms in a material structure are displaced from their original positions by the radiation (displacement damage) [69, 70]. Displacement damage causes a reduction in minority carrier lifetime in the substrate. Since the properties of most MOS devices are not significantly affected by minority carrier lifetime, they are relatively insensitive to displacement damage [71].

Ionizing damages can be classified into two types: total dose effects and single-event effects. The "total dose effects" affects device operational characteristics and performance by radiation-induced damage to the oxide layers in MOS circuits, whereas "single-event effects" is able to generate photocurrents in the substrate by relative high-dose-rate radiation [53, 72]. It was reported that single-event effects could only pose significant problems for COMS devices at the dose rate greater that 10^6-10^7 [73]. In consequence, the effects of total dose on oxide layer is of the major concern for MOS devices under irradiation exposure. The following paragraphs will provide a description and overview of total dose radiation effects.

The total ionizing radiation effects in gate oxide layers consist of three components: the build-up of oxide trapped charges, the formation of interface traps, and an increase in the number of bulk oxide traps. Electron/hole pairs (EHPs) are created initially within

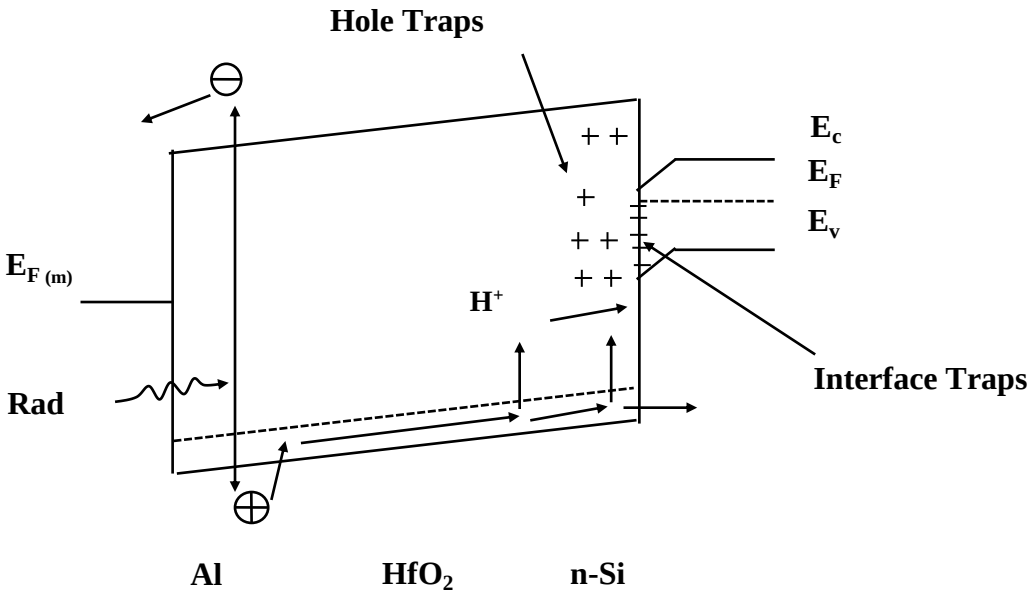

Figure 1-2-1. Energy band diagram demonstrated total ionizing-radiation-induced charge generation and charge trapping in high-k oxide layer under positive gate bias.

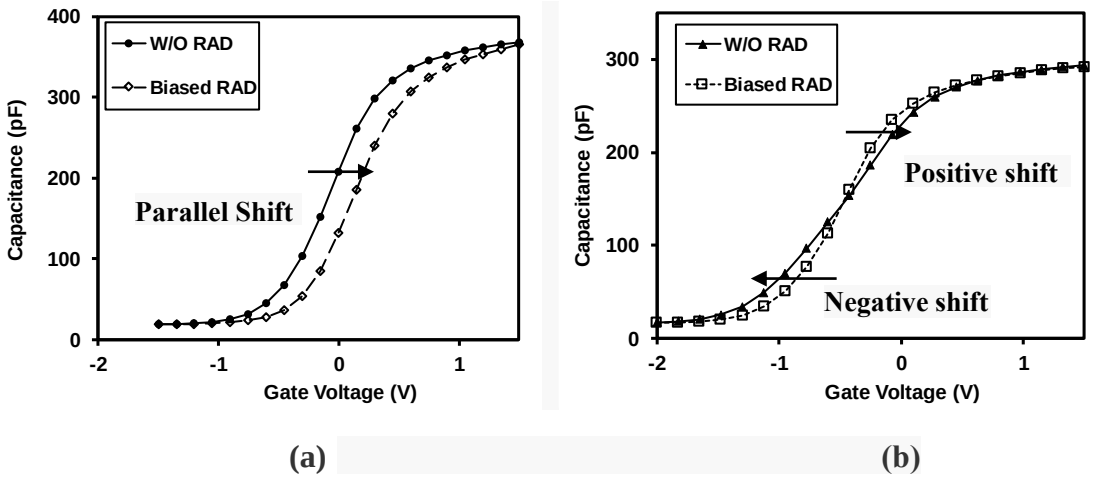

Figure 1-2-2. Capacitance-Voltage characteristics for (a) a n-Si SiO_2 MOS capacitor irradiated to 40 krad (SiO_2) with -0.5 MV/cm gate electric field. The capacitance in vertical axis is the capacitance of SiO_2 MOS capacitor. The oxide trapped charges lead to parallel shifts of CV curves; (b) a n-Ge $HfZrO_x$ MOS capacitor irradiated to 56 krad ($HfZrO_x$) with -0.5 MV/cm gate electric field. The build-up of Ge-H or Ge-S interface dangling bonds increase the slope of CV curves after irradiation exposure.

the oxide by ionizing radiation exposure. Some of these EHPs can recombined and do not affect the properties of devices. Conversely, the un-recombined electrons and holes are separated and drift to contacts under applied electric field[54, 74, 75]. It was reported that the EHPs would have no significant effect on the devices without an applied electric field [76]. In addition, most of the semiconductor devices in operation suffered from voltage bias. Therefore, it is more convincing to investigate the radiation response of gate dielectrics under biased irradiation exposure.

Fig.1-2-1 illustrates the radiation induced charge generation and charge trapping process in HfO_2 oxide layer of a MOS capacitor under positive gate bias. After the non-recombined carriers are separated by the positive bias, electrons are very mobile in the oxide region and quickly move to the gate electrode, and the holes are transported toward the oxide/Si interface via defect sites in HfO_2. Some of these holes will become trapped in oxide, forming positive oxide trapped charges. Meanwhile, few electrons are trapped near the interface of gate/oxide [77, 78]. The effect of trapped carriers on devices is more significant when the trapped charges are closer to oxide/Si interface, in other words, the electrons trapped near gate/oxide would have no distinct effect to the characteristics of devices, while the positive charges trapped near oxide/Si interface can lead to significant negative flat-band voltage shift (ΔV_{FB}) [79]. Conversely, under negative bias, radiation-induced electrons are transported toward the HfO_2/Si interface. Some of these electrons will become trapped in oxide, forming a negative oxide trapped charge and inducing positive ΔV_{FB}.

It was found that the oxide trapped charges only response for the mid-gap voltage shift (ΔV_{mg}), which shifts the C-V curves in parallel as indicated in Fig. 1-2-2 (a) [80]. A 0.22 V positive ΔV_{FB} was observed for a n-substrate SiO_2 MOS capacitor irradiated to 40 krad (SiO_2) with -0.5 MV/cm gate electric field. In this case, the ΔV_{FB} is due entirely to oxide trapped charges. It was because that a fix density of oxide trapped charges would induce a constant shift of C-V curves in whole gate voltage sweep range. However, it was reported that ΔV_{FB} can be attributed to the combination effects of oxide and interface traps [81, 82]. The effects of interface traps to device characteristics will introduced in the following parts.

The most widely accepted defects in high-*k* dielectrics include two trapping centers: i). O_2^- centers (O_2^- coupled to hafnium or other high-*k* ion) serve as electron traps; ii). oxygen vacancy (V^+/V^{2+}) serve as electron and/or hole traps [83, 84]. Alone with the EHPs generation and transportation process, chemical bonds (Hf-H, Hf-OH etc.) in high-*k* dielectrics may be broken. Some of these broken bonds may react with EHPs and reform chemical bonds, whereas others may form electrically active defects. These defects created by radiation can serve as trap sites for carriers near the oxide/Si interface. The bonds associated with hydrogen or hydroxyl groups can release impurities such as H, and OH which would result in the formation of interface traps [59].

Shown in Fig. 1-2-1, the protons can be released from the oxide, or be released from Hf-H or sub-oxide bounds during the transportation of EHPs. These protons can transport toward to oxide/Si interface under positive bias and react with Si dangling

bonds which result in interface traps of devices [85]. Interface states are located at the interface with energy levels that exist within the band gap of silicon, germanium or other substrate. Interface traps distributed in the lower half of band gap are donor-like traps, they can produce excess negative charges when empty and be neutral when filled upper half of band gap are acceptor-like traps which can react with negative chargeswith protons or hydrogen as indicates in Fig. 1-2-3 (a). Interface traps distributed in the and produce excess negative charges, whereas they are in neutral charge states when electrons are de-trapped as indicates in Fig. 1-2-3 (b) [86]. Therefore, the number of neutral and charged interface states is bias dependent since the energy level of interface states relative to Fermi level can be determined by the applied electric field.

Shown in Fig. 1-2-2 (b), under negative gate bias, interface states induce negative

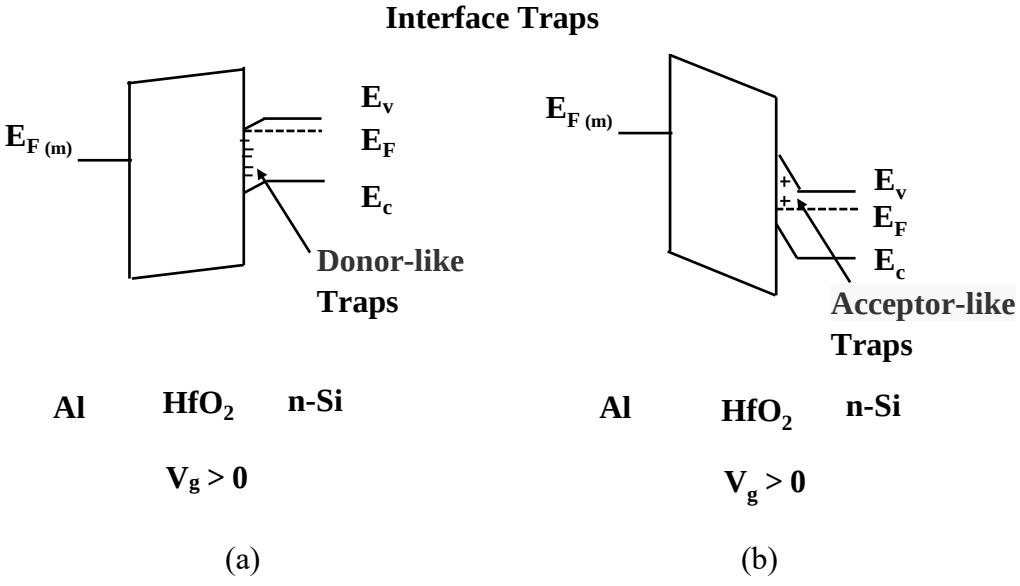

Figure 1-2-3. Energy band diagram showing interface traps located at the interface with energy levels that exist within (a) upper half of n-Si band gap; (b) lower half of n-Si band gap.

flat-band voltage shifts in MOS devices. When the gate bias sweeps from negative to positive, flat-band voltage shifts would change from negative to positive due to the variation of interface states at energy level. With regard to C-V characteristics of MOS devices, the presence of the interface states or dangling bonds has significant effect to the 'slope' of CV curves.

1.3 Objectives of Thesis

Gamma-ray radiation is known to induce degradation and failures to the electrical properties of a variety of materials and components thus degrading the device performance. The degradation and failures are caused by the charge trapping built-up in either gate dielectrics or interface leading to a shift in the flat-band voltage (V_{FB}) or the threshold voltage (V_{TH}) as discussed in previous section. There has been a substantial body of research on the physical mechanisms of high-dose-rate total ionizing dose response of high-*k* materials in recent years [57, 67, 87]. So far, total-dose irradiation testing of semiconductor devices was carried out by 10-KeV X-ray irradiators at the dose rate of 50 to 5600 rad (SiO_2)/s [63, 64]. However, the accumulation of total dose is a long process as the representative distribution of dose rate is $10^{-2} \sim 10^{-6}$ rad(Si)/s in space-like environments [49-51]. The total ionization dose effects to MOS devices are required to identify with certainty at the dose-rate level close to actual radiation conditions.

Conventional evaluation of radiation induced V_{TH}/V_{FB} shift has been carried out in

an off-site condition after the exposure due to radiation safety consideration. The conventional radiation response measurement processes are 1) a MOS device is irradiated by gamma-ray under certain voltage biasing condition using a radiation exposure facility, 2) the radiation exposure and voltage biasing are interrupted and the sample is taken out from the on-site irradiation chamber, and 3) electrical characterization of the irradiated devices is performed by traditional current-voltage (I-V) or/and capacitance-voltage (C-V) techniques [88]. According to the mechanism of radiation-induced defects or degradation in semiconductor materials, the interruption of irradiation and voltage biasing may cause a rapid recovery of the V_{TH}/V_{FB} shift. Moreover, the conventional measurement techniques may underestimate the defects or degradation in dielectrics because the measurements cannot be completed in a very short time [3, 75]. To precisely detect the effects of total ionizing dose on semiconductor devices, it is necessary to upgrade the conventional evaluation of radiation response to on-site and real-time measurement. The construction of a turnkey real-time and on-site radiation response testing system for semiconductor devices has been reported in Chapter 3 of the thesis. Analysis of ΔV_{FB} extracted from SiO_2 and high-*k* deposited MOS capacitors suggested that the on-site and real-time/pulse measurements can detect more serious degradation compared with the off-site irradiation and conventional measurement techniques.

In Chapter 4, low-dose-rate radiation response of Al-HfO_2/SiO_2–Si MOS devices has been reported, where the gate dielectric was formed by atomic layer deposition (ALD) with 4.7 nm equivalent oxide thickness. The degradation of the devices was

characterized by pulse capacitance-voltage (C-V) measurement system and an on-site radiation response technique under continuous gamma (γ) ray exposure at a relatively low-dose-rate of 0.116 rad(HfO_2)/s. A significant variation of the flat-band voltage shift, with the total dose of up to 40 krad (HfO_2) and an electric field of ~0.5 MV/cm has been measured for the HfO_2-based MOS devices using the proposed pulse CV techniques. The large flat-band voltage shift is mainly attributed to the radiation-induced oxide trapped charges, which are not readily compensated by bias-induced charges.

Analysis of the experimental results suggested that both hole and electron trapping can dominate the radiation response performance of the HfO_2-based MOS devices depending on the applied bias. No distinct hysteresis variation has been found with irradiation in all cases. The result was likely due to the fact that bias-induced electrons were injected into HfO_2 to neutralize the positive cyclic charges which are located in shallow traps in the HfO_2. In addition, a framework and measurement methodology have been proposed for better understanding mechanisms of radiation-induced charge trapping and compensation of bias-induced charges in HfO_2 stacks. It was suggested that the effect of the peak voltage time on the concentration of net oxide trapped charges was negligible. With regard to pulse magnitude effects, a higher pulse magnitude would cause larger ΔV_{FB} during the biased irradiation pulse CV measurements

The long-term radiation response of $Hf_xZr_{1-x}O_y$ thin films on germanium substrate will be discussed in Chapter 5. Prior to the irradiation exposure, the gate leakage

behavior for the devices has been investigated. Gate leakage density increases with the increasing of ZrO_2 content in gate oxide. In addition, CV measurements indicate that smaller interface trap density is exhibited for HfO_2 capacitors, while a higher dielectrics constant can be achieved by addition of ZrO_2 in HfO_2 thin films. The ΔV_{FB} of the proposed devices under positive or negative bias without irradiation-exposure has also been investigated. A smaller oxide and interface trap density has been observed for HfO_2 gate dielectrics under negative bias, whereas no significant difference of oxide and interface trap density was observed between $Hf_xZr_{1-x}O_y$ thin films with various Zr compositions. More interface traps were generated in Zr-doped $Hf_xZr_{1-x}O_y$ compared to HfO_2 under positive bias, which suggests that ZrO_2 presented more hydrogen-related species than HfO_2.

The total ionizing radiation effects to $Hf_xZr_{1-x}O_y$ thin films on germanium substrate were evaluated under both positive and negative biased gamma-ray irradiation exposures. The effects of biased-radiation induced oxide and interface traps to device characteristics will be presented separately. Under positive biased radiation, the Zr-doped $Hf_xZr_{1-x}O_y$ exhibited smaller ΔV_{FB} than that of HfO_2. This is attributed to the de-passivation of Ge-S bonds in capacitors incorporating HfO_2 thin films, resulting in the build-up of interface traps. Under negative biased radiation, ΔV_{FB} was dependent on the combined effect of the net oxide trapped charge and interface traps at the Ge/high-*k* interface. Analysis of the results obtained from biased radiation and pure bias measurements indicated that the interface traps build-up between Ge and oxide dominate the radiation response of $Hf_xZr_{1-x}O_y$ thin films. This can be explained by the

large number of interface traps between the dielectric and the Ge substrate. It is also suggested that the radiation exposure would induce more de-passivation of Ge-S passivated dangling bonds in HfO_2 / Ge interface compared with ZrO_2 containing gate dielectrics. This work demonstrated that $Hf_xZr_{1-x}O_y$ may be a promising candidate for space microelectronics in bias conditions. However, the biased radiation environment is quite challenging for Ge devices. However, the biased radiation environment is quite challenging for Ge devices due to the large number of interface traps between the dielectric and the Ge substrate.

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Chapter 2: Device Fabrication and Characterization Techniques

2.1 Thin Films Deposition and Process Treatment

As discussed in Chapter 1, to meet the requirements of reducing the gate leakage currents and scaling down the transistor size, high-*k* materials are employed to replace SiO_2 as the gate dielectrics [1-3]. Several high-*k* materials have been under consideration, such as hafnium oxide (HfO_2), zirconium oxide (ZrO_2), yttrium oxide (Y_2O_3), titanium oxide (TiO_2), and their silicates [4-7]. Among these materials, the oxides of hafnium and zirconium dielectrics emerged as the most promising high-*k* materials as they have relatively high dielectric constants of 15-25, relatively large band gap (5-5.8 eV). In particular, HfO_2 is more widely used than ZrO_2 because it is more stable with silicide formation [8-10]. However, ZrO_2 offers the benefit of a higher dielectric constant.

On the other hand, it has been reported that the addition of ZrO_2 into HfO_2 gate dielectric stabilizes the tetragonal phase and enhances the dielectric constant. $Hf_xZr_{1-x}O_y$ dielectric is thus an attractive candidate for advanced gate stack applications [11]. Therefore, it is necessary to understand the radiation response of HfO_2, ZrO_2, and $Hf_xZr_{1-x}O_y$ dielectrics before they can be used in space applications. Prior to irradiation exposure, these high-*k* materials were deposited on silicon (Si) or germanium (Ge)

substrates to form Metal-Oxide-Semiconductor (MOS) capacitors. The fabrication processes were carried out at the XJTLU clean room.

Si-based MOS capacitors were formed on single crystal n-type silicon <1 0 0> wafers with a doping concentration of ~10^{15} cm^{-3}. Before the wafers were deposited with high-*k* thin films, the wafers were subjected to standard Radio Corporation of America (RCA) cleaning to remove native oxide, organic and metallic contamination. The wafers were then etched in a hydrofluoric acid solution (HF: H_2O = 1:50) for 30 seconds to remove oxides created during the RCA clean, and finally dried by nitrogen gas. The related clean procedures are shown in Fig. 2-1-1 [12, 13]. Among these procedures, hydrofluoric acid treatment was carried out at room temperature, while ammonium hydroxide (NH_3H_2O) and hydrochloric acid (HCl) treatment were carried

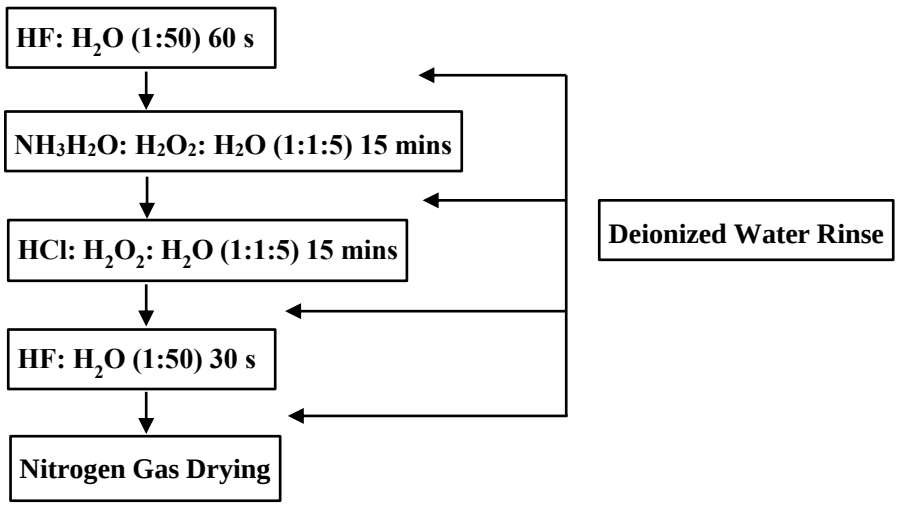


Figure 2-1-1. RCA clean procedures and post-HF treatment for Si wafers. Deionized water rinse was performed after each procedure to remove the solutions remained on the Si surface.

out at 80 ℃.

High-*k* thin films have been deposited by a number of techniques including RF magnetron sputtering, metal organic chemical vapor deposition (MOCVD), and atomic layer deposition (ALD). Among these techniques, ALD is one of the most reliable method, as it offers the advantages of large area deposition capability, good composition and doping control, high film uniformity, and superior conformal step coverage on non-planer substrates [14-16]. Therefore, after the cleaning processes of Si-wafers, HfO_2 thin films were deposited by ALD using an f-200 ALD fabrication machine.

To better understand the ALD principle, Fig. 2-1-2 illustrates the schematically mechanisms of possible reactions and atomic motions during deposition of HfO_2 thin films on Si substrate [17-19]. The deposition of HfO_2 thin films was carried out at a temperature of 200 ℃ using tetrakis (dimethylamido) hafnium (IV) $Hf[Me_2N]_4$ as the precursor for HfO_2 and deionized H_2O as the oxidant. There were 160 HfO_2 cycles grown with the following sequence: water / purge / precursor / purge (30 ms / 25 s / 150 ms / 25 s). Initially, water vapor was transported to Si surface and reacted with Si dangling bonds, producing hydroxyl groups (Si-O-H) as shown in Fig. 2-1-2 (a). After the formation of hydroxyl groups, precursor of $Hf[Me_2N]_4$ was applied into reaction chamber and reacted with the absorbed hydroxyl groups, forming Si-O-Hf bonds as indicated in Fig. 2-1-2 (b). Since $Hf[Me_2N]_4$ cannot react with itself or Si dangling bonds, the Hf-precursor can only deposit one-layer of hafnium atoms. The excess

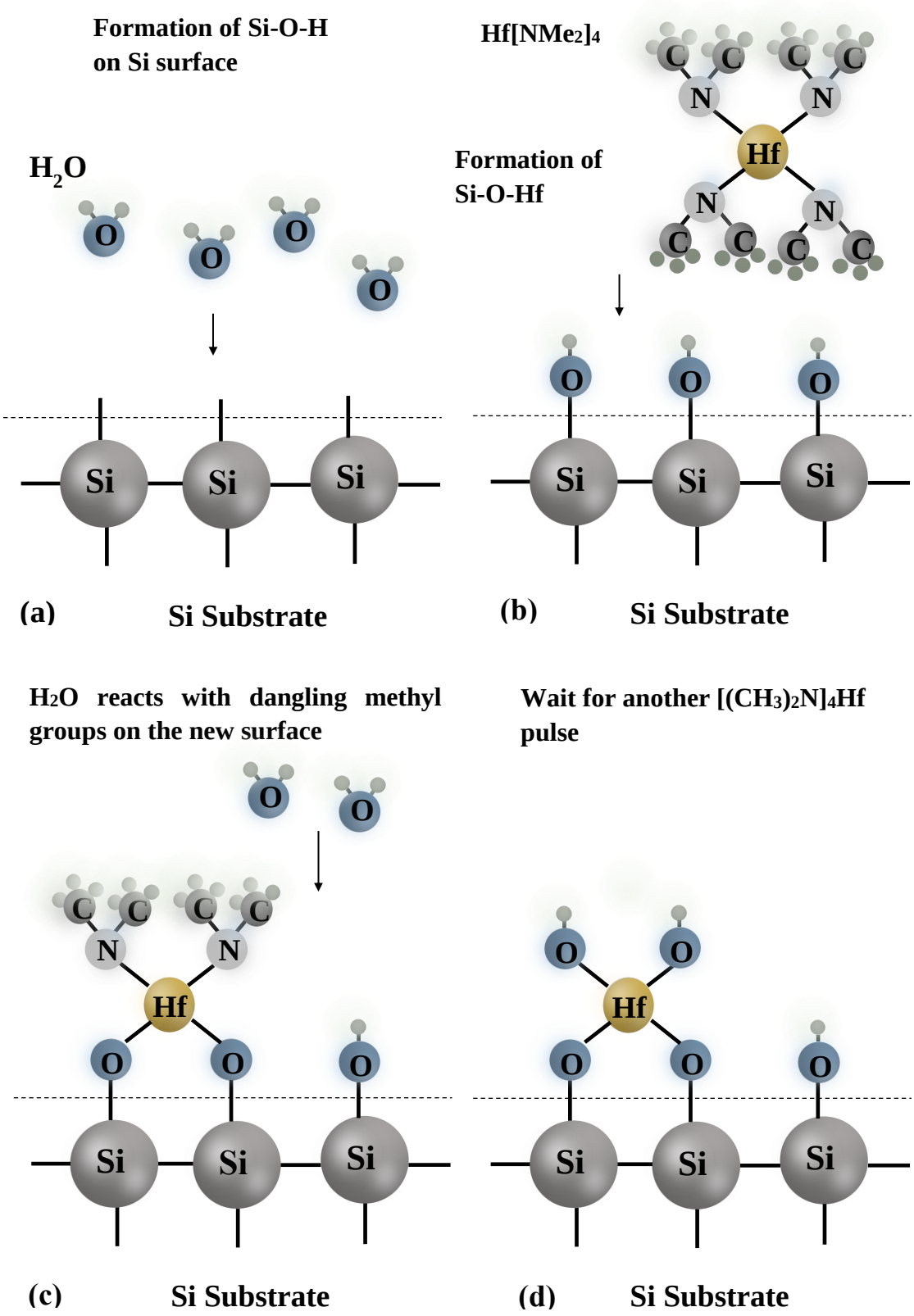


Figure 2-1-2. Schematic diagrams of ALD principle and reactions during deposition of HfO_2 thin films on Si substrate.

$[(CH_3)_2N]_4Hf$ and the methane reaction product was blown away by nitrogen. Similarly, another cycle of H_2O vapor was supplied to the chamber followed by the Hf-precursor. Water vapor can react with the dangling methyl groups ($[(CH_3)_2N]$-) produced in the previous procedure, forming Si-O-Hf-O bonds illustrated in Fig. 2-1-2 (c, d).

After high-*k* thin films deposition, the aluminum gate electrodes (500 nm thick and 0.07 mm^2 gate area) and back contact were formed by electron beam evaporation through a shadow mask. Solid aluminum was vaporized by electron beam with the accelerating voltage of 8 kV – 15 kV. The deposition chamber was evacuated to a pressure of 10^{-3} Pa to allow the gaseous aluminum evaporated on the silicon substrate. The deposition rate of aluminum layers is 10 nm/sec.

With regard to germanium substrate, the samples used in this study were n-type germanium <1 0 0> wafers with a doping concentration of ~10^{15} cm^{-3}. The n-type wafers were doped by antimony (Sb) using ion implantation technique. It has been reported that germanium substrate with Sb implanted dopant is expected to provide higher impurity concentration and less defect generation [20, 21]. Prior to gate stack fabrication, the germanium wafers were initially degreased for 10 minutes in acetone and isopropyl alcohol. The native oxides were then removed using a solution of HF: deionized water (1:50) for 30 seconds. The final treatment involved 15 minutes of $(NH_4)_2S$ solution (0.1 mol/L) soak and deionized water rinse in order to passivate the germanium interface [14, 15]. Similar to deposition of HfO_2, $Hf_xZr_{1-x}O_y$ ($0.4<X<1$) thin films with various Zr/Hf ratios, were prepared at a wafer temperature of 200 ºC using

ALD technique. $Hf[NMe_2]_4$, $Zr[NMe_2]_4$, and deionized water served as the precursor for hafnium, zirconium and oxygen. Composition and thickness of the thin films were controlled by varying the ratios of Zr:Hf precursor cycles. $Hf_xZr_{1-x}O_y$ dielectrics with different Zr compositions were deposited; sample A was grown with the Hf:Zr deposition ratio of 1:1, (i.e. every HfO_2-H_2O cycle followed by a ZrO_2 -H_2O cycle), while the deposition ratio for sample B was 3:1. Aluminum electrodes with 0.07 mm^2 gate area were deposited by electron beam evaporation. Finally, Al back contacts were evaporated at the back of the substrates.

During the fabrication processes of MOSFETs, the deposited samples unavoidably suffered high temperature thermal annealing treatments, such as ion implantation. Ion implantation is an important technique to dope ions into target materials. For MOSFET devices, each dopant atom can create a charge carrier in target semiconductor material after annealing. These carriers modify the conductivity of the semiconductor to form drain, source regions. In semiconductor manufacturing, ion implantation is also used to determine and adjust the threshold voltage of MOSFETs by controlling the channel length. In order to active the implanted ions, thermal annealing treatments are carried out flowed by the implantation processes at the temperature of 500 ~ 1000 °C. Prior to ion implantation, the high-*k* films have been deposited by atomic layer deposition at relative low temperature (<300°C) with an amorphous microstructure. However, the post-deposition annealing at higher temperature transforms the amorphous high-*k* films to either the cubic or tetragonal phases. These phases have higher *k*-values than the amorphous or monoclinic phase, but show an adverse increase in the leakage current.

Therefore, it is important to understand the effects of thermal annealing on crystalline structure of high-*k* thin films, which mimics the typical thermal budget of CMOS processes. After the thin film-deposition process, rapid thermal annealing (RTA) was carried out at 500 and 600 °C for 15 s under nitrogen gas flow by TP-600xp (Modular Process Technology Corp.).

2.2 Physical Characterization of MOS Capacitors

The investigation of the deposited high-*k* thin films on their physical properties was mainly focused on physical thickness and element-concentration. The physical properties were carried out by spectroscopic ellipsometry and energy dispersive spectrometer.

The physical thicknesses of the deposited thin films were measured by spectroscopic ellipsometry. Ellipsometry is an efficient method for determining optical constants, namely, the index of refraction and extinction coefficient. The permittivity and thickness of dielectrics can be obtained by analyzing the measured index of refraction and extinction coefficient. Fourier-modulated radiation is emitted from an interferometer and linearly polarized by a polarizer. When the radiation falls onto the sample with a specific incidence-angle, two reflected-light beams are generated at the surface of the dielectrics and the interface between the dielectrics and the substrate. These two reflected-light beams are then transmitted and passed to a second polarizer, and falls into the detector. The thickness of the dielectrics can be calculated from the

phase shift of the reflected-beams [22, 23].

Typically, spectroscopic ellipsometry measurements are carried out at the incident angles near 50°, because it was reported that the maximum test-precision of reflected-beams can be achieved at these angles [24]. This is particularly important for thin films with thickness less than 20 nm. Moreover, for dielectric films, the inferior sensitivity of a rotating analyzer makes the measurement of phase shifts of incident-light and reflected-light beams significant only near to the incident angle region from 50° to 70° [24]. In order to select an appropriate incident angle in this study, the incident beams with different angles from 50° to 70° were applied to SiO_2 thin films as reference. The results indicate that the most accurate thicknesses of the thin films were obtained from the measurements with the incident angles near 65 °. Therefore, the spectroscopic ellipsometry measurements in this study were carried out by an ELLIP-SR-1 ellipsometer with an incident angle of 65° and wavelengths from 300 nm to 800 nm with a step of 25 nm. The physical thickness of the HfO_2 films for Si-based capacitors was 24 nm. In addition, a very thin, ~2 nm, SiO_2 interfacial layer was formed between the HfO_2 layer and the Si substrate. For Ge-based MOS capacitors, the physical thicknesses of HfO_2, $Hf_{0.6}Zr_{0.4}Oy$, and $Hf_{0.43}Zr_{0.57}O_y$ were 20.5 nm, 21.3 nm, and 21.1 nm, respectively.

The analyses of the thin films of Ge-based capacitors were carried out by EDS measurements using an Oxford Instrument. EDS is applied to determine the concentration of chemical elements in a microscopic volume of a specimen. The

measurement relies on an interaction of some source of X-ray excitation and the materials. X-ray exposes to the surface of the thin films can result in the electromagnetic emission of each element in the dielectrics. Since each element has a unique atomic structure, the energy and numbers of emitted electrons for different element would offer a unique set of peaks on its electromagnetic emission spectrum [25]. The energy of incidence X-ray is 10-KeV, and the elevation degree is 35°. Fig. 2-2-1 shows the spectrum of the measured Ge capacitors. Elements of C, O, Ge, Hf, and Pt can be from the spectrum. Since HfO_2 is an insulator, Pt is induced by the surface-treatment before the EDS measurements to achieve the electric conductivity. Moreover, impurity element C can be attributed to the Ge surface passivation process by $(NH_4)_2S$ solution. Analysis of the results obtained from the spectrum is presented in Chapter 5.

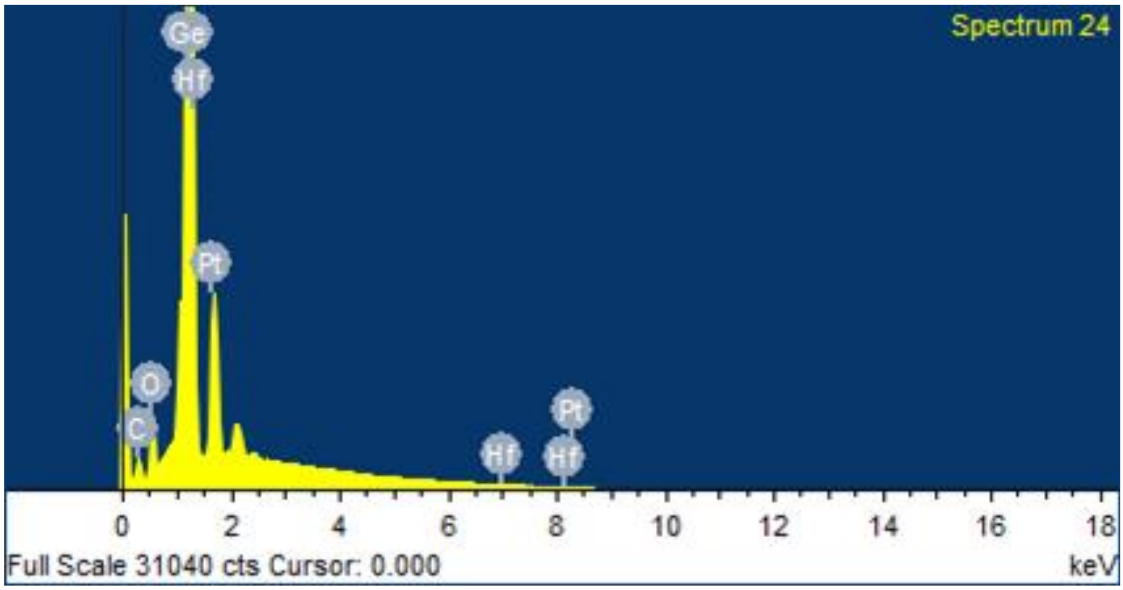


Figure 2-2-1. Measured 10-keV spectrum for Ge capacitors with HfO_2.

2.3 Electrical Characterization of MOS Capacitors

The investigation of the deposited MOS capacitors on their electrical properties was mainly focused on C-V and I-V characteristics. One of the major concerns in further reduction of oxide thickness is high gate leakage current which leads to issues regarding dielectric reliability and power consumption [26, 27]. Since devices with various gate dielectrics were expected to exhibit different current leakage behaviors. I-V measurements were performed before the biased-irradiation exposure to evaluate the gate leakage currents of the MOS capacitors. In this study, I-V measurements were carried out by using an Agilent B1500A Semiconductor Device Analyzer.

In Chapter 1.2, we discussed the irradiation exposure capable of inducing charge trapping in gate dielectrics, thus resulting in a shift in the flat band voltage (V_{FB}) of the C-V curves. Therefore, the C-V characteristics of the MOS capacitors were investigated during the biased radiation at various dose levels. In this work, a semi-automated laboratory-scale real-time and on-site radiation response testing system was developed to evaluate the ΔV_{FB} of the biased devices which was irradiated by a Cs^{137} γ-ray radiation source with an activity of 1.11 GBq and photon-energy of 662 keV. The testing setup is able to measure the C-V characteristics of MOS capacitors while the devices were irradiated by the gamma ray source. More details on the radiation response testing system are illustrated in Chapter 3. C-V measurements were carried out using a HP 4284 Precision inductance-capacitance-resistance (LCR) meter. During the C-V measurements, the LCR meter initially generated a small voltage signal to the gate of

MOS capacitor, and then measured the small signal current flowed through the capacitor. The measured capacitance (C_m) of the measured MOS capacitor can be calculated according to [28, 29]:

$$C_m = \frac{i_{ac}}{dV_{ac}/d_t} \qquad (2.1)$$

where i_{ac} is small signal current, dV_{ac} is the variation of the small gate signal voltage, and d_t is the variation of measuring time, dV_{ac}/d_t is the slope of V_{ac}(t). The whole C-V curves of MOS capacitors were obtained by applying a sweeping voltages to gate electrode. Fig. 2-3-1 shows the schematic diagrams of MOS capacitor under C-V measurements with parallel model. The equivalent circuit in left hand side illustrates the components present in actual measurements, while components of the equivalent

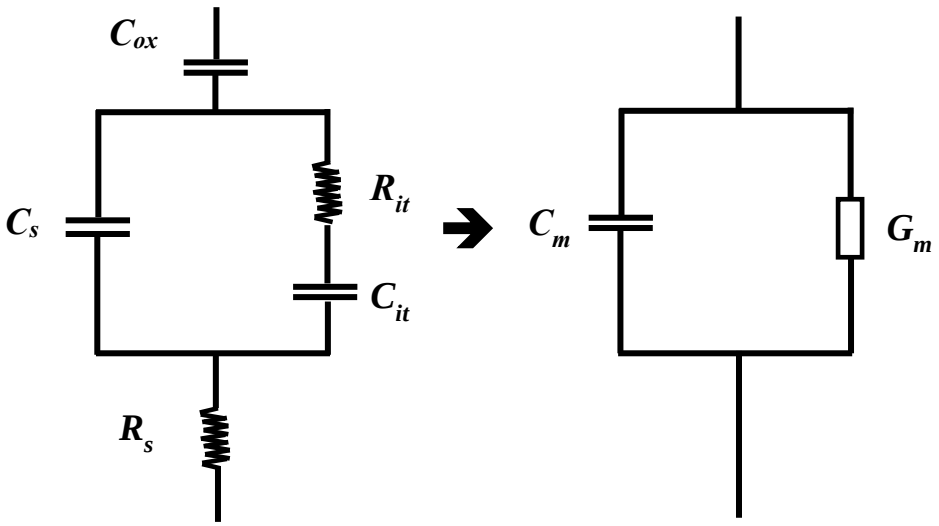


Figure 2-3-1. Schematic diagrams of C-V measurements with parallel model for MOS capacitors. The equivalent circuit in left hand side illustrates the components present in actual measurement environments, whereas components of the equivalent circuit in right hand side represent the equivalent capacitance (C_m) and conductance (G_m) measured by Agilent 4284 LCR meter.

circuit in right hand side represent the equivalent capacitance (C_m) and conductance (G_m) measured by HP 4284 LCR meter [30, 31]. C_{ox} is the capacitance of the oxide layer, C_s is the space charge capacitance or depletion capacitance of Si or Ge semiconductor substrate, R_s is the series resistance, R_{it} and C_{it} are the resistance and the capacitance related to the interface traps at oxide/substrate interface, respectively. Therefore, the measured capacitance C_m is not only determined by C_{ox} and C_s, but also effected by the interface traps. Meanwhile, the maximum capacitance (accumulation region) in measured C-V curves cannot fully represent C_{ox}. However, as the other components have very limited effects on the C-V curves of MOS capacitors at the accumulation region, the measured capacitance has been referred to C_{ox} in this study [32-34].

To investigate the reliability of semiconductor materials comprehensively, it is crucial to evaluate the effect of irradiation on the leakage behavior of MOS devices. DC I-V and stress measurements were performed by applying a sweeping voltage and a stress voltage to the MOS devices using a Keithley 487 ampere meter and an Agilent E3647A DC power supply. Fig. 2-3-2 shows a schematic diagram of the measurement set-up for a MOSFET device using the DC I-V and stress technique in the ionizing radiation probe station system. The inset of Fig. 2-3-2 shows a graph of the gate sweeping voltage and stress voltage(V_g) versus the sweeping/stress time in the conventional C-V and stress module. The stress voltage and the sweeping voltage are alternately applied to the MOS device under test by the Agilent 4284 LCR meter. The duration of the stress voltage is controlled by the PC. The DC power supply generates

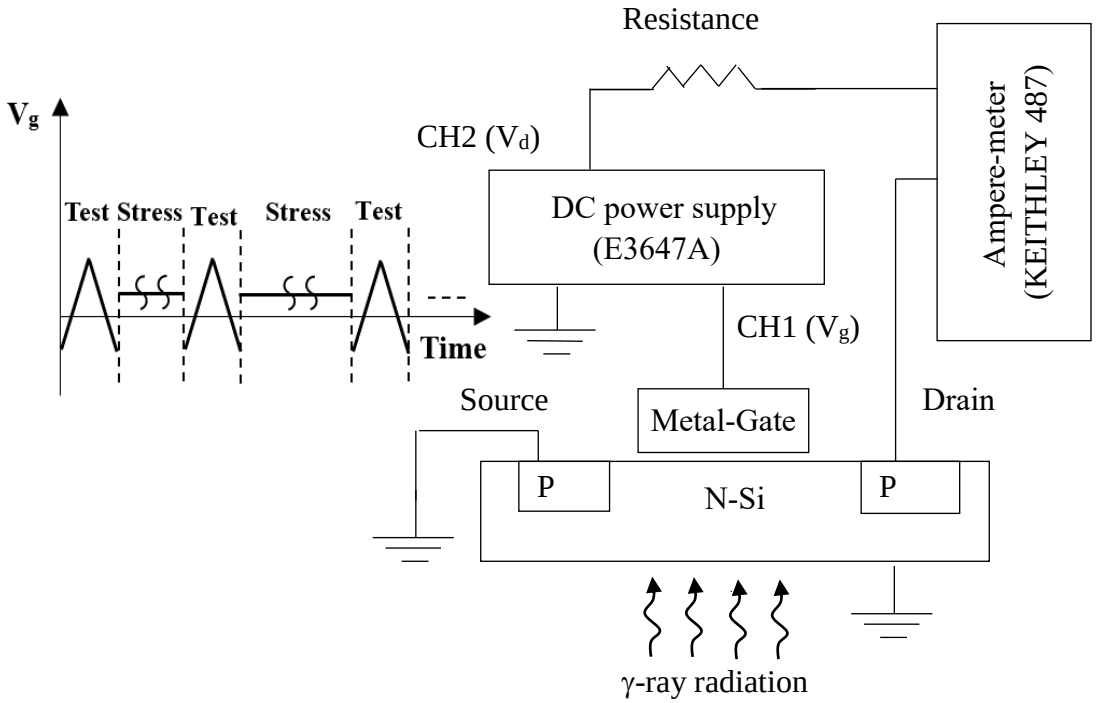


Figure 2-3-2. Schematic diagram of the measurement set-up for a MOSFET device using the DC I-V and stress technique under continuous γ-ray exposure in the ionizing radiation probe station system. The waveform of V_g is the same as the waveform shown in Fig. 3-2-2.

a sweeping voltage or bias voltage (V_g) with a range of $\pm$35 V to the gate of the MOSFET. A continuous voltage (V_d) is supplied to the drain of the MOSFET. Afterwards, the drain current (I_d) of the MOSFET is measured by the ampere-meter which has a measurement accuracy at the 1 μA level.

Fig. 2-3-3 presents the I-V curves of a MOSFET device using the DC I-V and stress technique with +1 V bias for a stress duration of 460 s. A sweeping voltage and a bias voltage of +1 V were alternately applied to the metal gate of the MOSFET for a stress duration of 460 s. The results indicate that the threshold voltage of the MOSFET is less

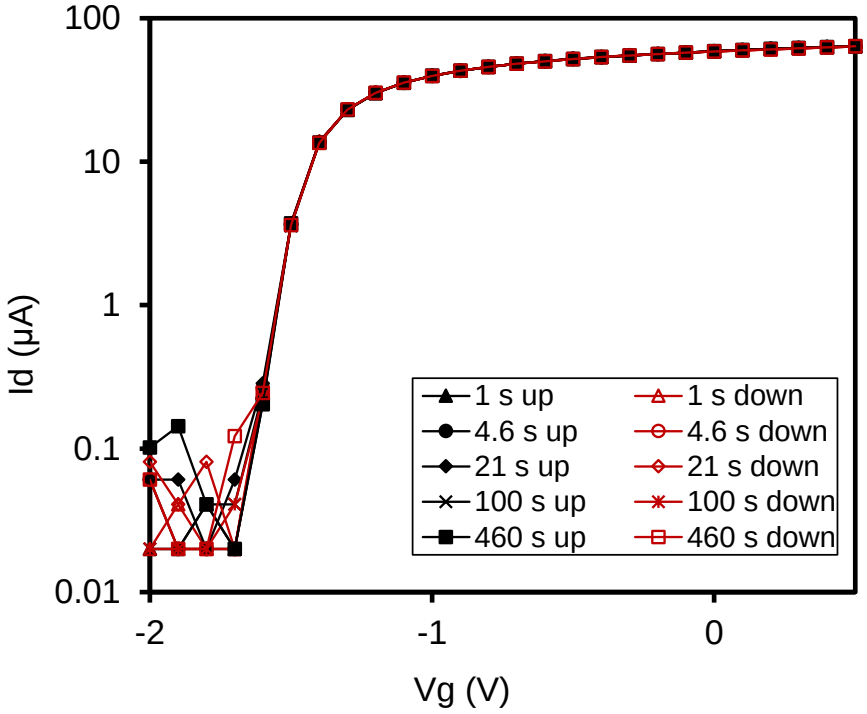


Figure 2-3-3. I-V curves of a MOSFET device from measurements using the DC I-V and stress technique with +1 V bias for a stress duration of 460 s.

than -1.7 V. Neither significant hysteresis nor threshold voltage shifts of each loop were observed. Due to the limitation of the measurement range of the ampere meter, the noise signals had significant effects to the measured drain current when the drain current was below 1 μA.

A pulse I-V measurement system is set up with a Rigol DS1302CA oscilloscope, a Rigol DG3061 function generator and an Agilent E3647A DC power supply. Fig. 2-3-4 shows a schematic diagram of such a set-up for a MOSFET measured using the pulse I-V technique under continuous γ-ray exposure in the ionizing radiation probe station system. Initially, a trapezoidal pulse signal (V_g) is applied to the gate of MOSFET and a continuous DC voltage (V_{DD}) is applied to the drain through a resistor.

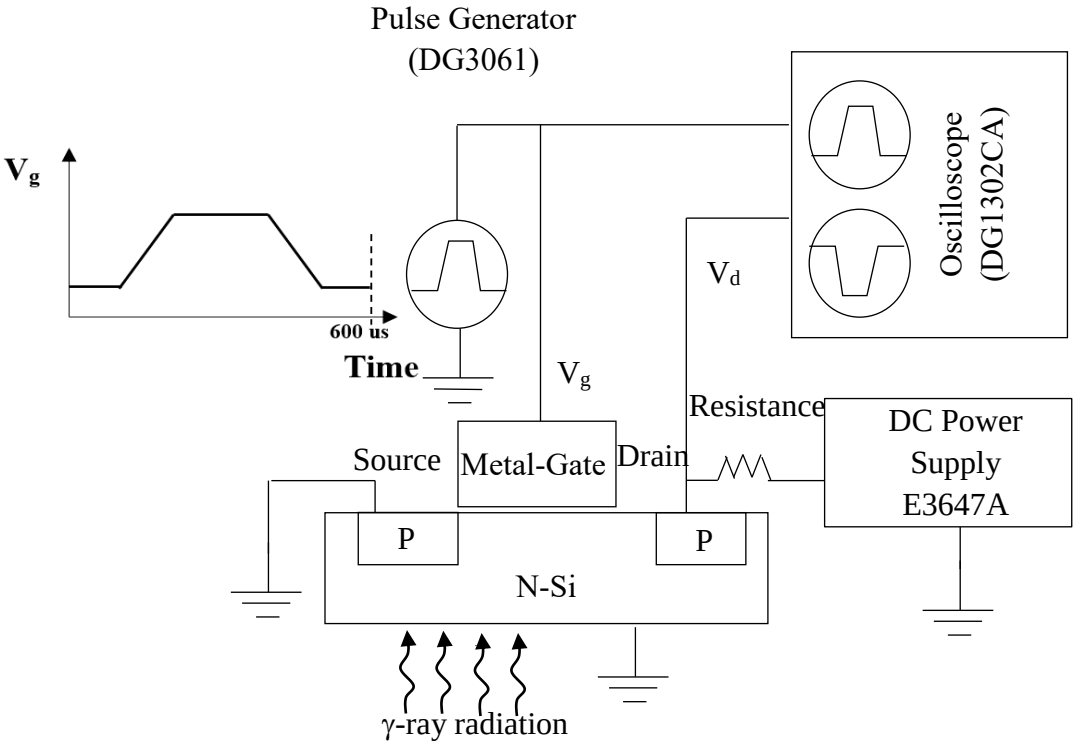


Figure 2-3-4. Schematic diagram of the measurement set-up for a MOSFET device using the pulse I-V technique under continuous γ-ray exposure in the ionizing radiation probe station system.

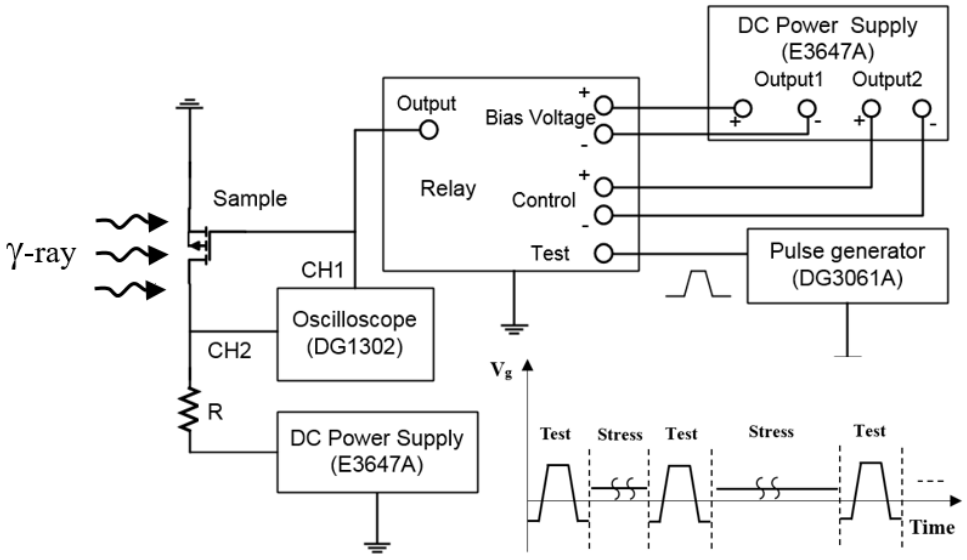


Figure 2-3-5. Schematic diagram of the measurement set up for a MOSFET device using the pulse I-V technique and stress technique under continuous γ-ray exposure in the ionizing radiation probe station system.

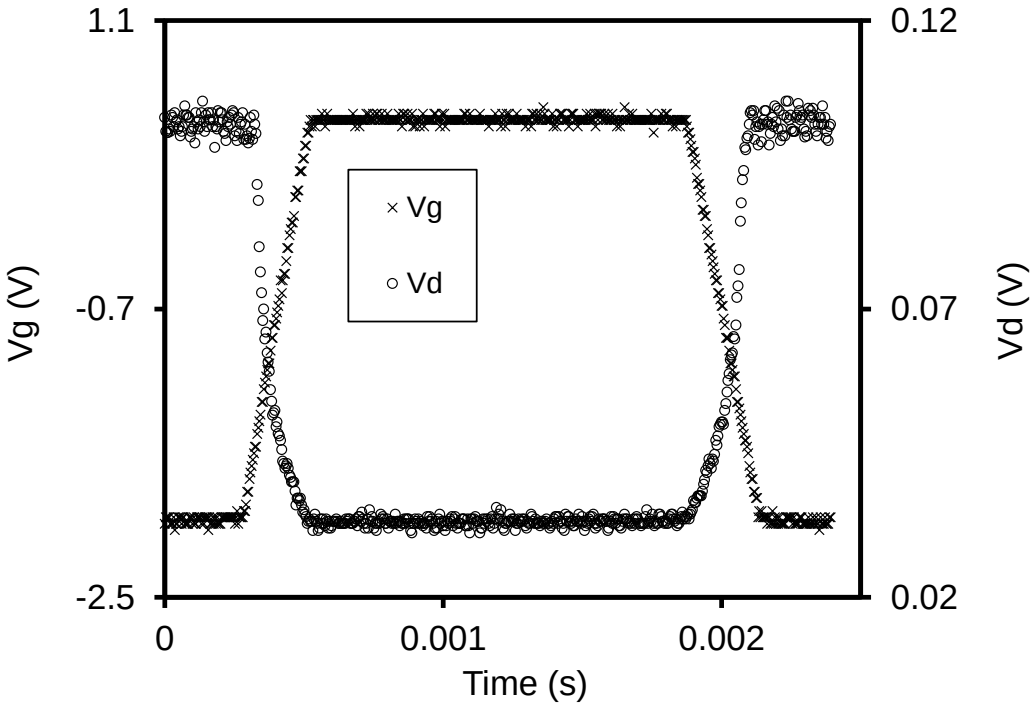
Afterwards, the drain voltage (V_d) is detected by the oscilloscope and is converted to drain current (I_d). The drain current of the MOSFET is expressed as:

$$I_d = \frac{V_{DD}}{V_d}\left(\frac{V_{DD}-V_d}{R}\right) \qquad (2.2)$$

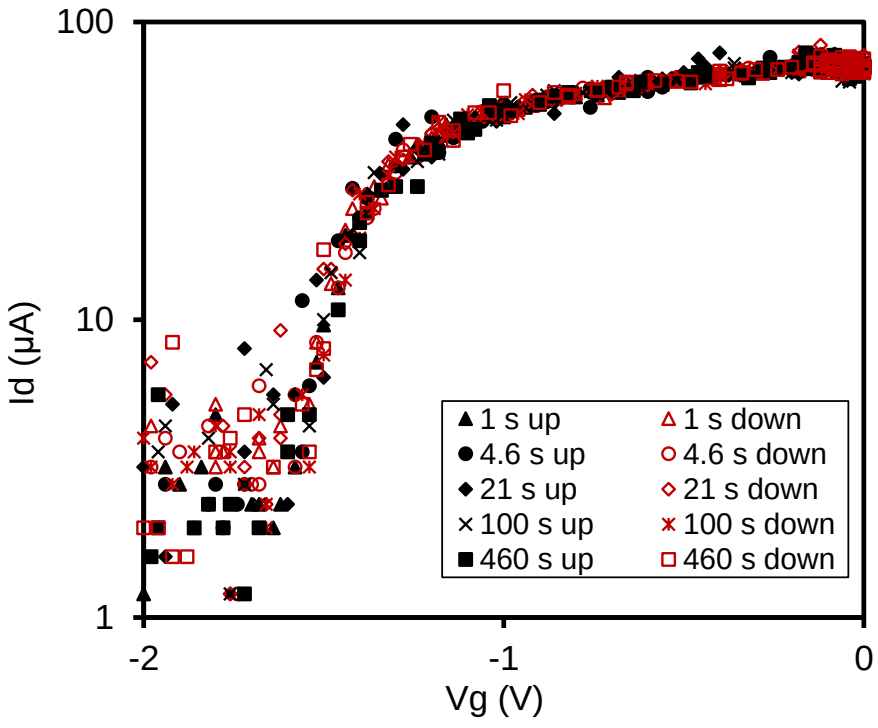
where V_{DD} is the continuous voltage applied to the drain; V_d is the drain voltage obtained from the oscilloscope and R is the resistance of the resistor between the DC power supply and the MOSFET.

Fig. 2-3-5 shows a schematic diagram of the measurement set-up for a MOSFET using the pulse I-V and stress technique under continuous γ-ray exposure in the ionizing radiation probe station system. A pulse I-V and stress measurement system is developed from a pulse I_d-V_g measurement system, an Agilent E3647A DC power supply and a relay. The DC power supply applies stress voltages to the gate of MOSFET in the "stress mode". After the DC power supply is switched to the "test mode" by the relay, the device is connected to the pulse I-V system and pulse I-V measurements are performed then.

Fig.2-3-6 (b) shows the I-V curves of a MOSFET from measurements using the pulse I-V and stress technique. A trapezoidal pulse signal V_g and a +1 V stress voltage are alternately applied to gate dielectrics for a stress duration of 460 s and a DC voltage of +0.1 V is continuously applied to the drain of the MOSFET. The trapezoidal pulse signal (V_g) and the drain voltage (V_d) as a function of time are shown in Fig. 2-3-6 (a). The results indicate that the threshold voltage of the MOSFET is about -1.6 V and the saturation current is 0.06 mA. There is no significant threshold voltage shift after each



(a)



(b)

Figure 2-3-6. (a) Gate and drain voltage versus time characteristics of a MOSFET device obtained by the pulse I-V and stress technique. (b) I-V curves of the MOSFET with +1 V bias for a stress duration of 460 s.

stress duration. The noise of drain current becomes non-negligible when the drain current is below 10 μA.

The pulse I-V technique can detect the trapped charges in the oxide of MOS devices. However, the rising edge and the falling edge of the trapezoidal signal are intensely sharp. As a result, the charging and discharging currents of parasitic capacitance would significantly affect the measurement of the I-V characteristics. For this reason, a multiple-pulse testing technique is more appropriate to detect the charging/discharging of defects instead of using one pulse waveform technique (pulse I-V and pulse C-V). On-the-fly (OTF) techniques are suitable for this purpose and the OTF techniques use a continuous stress voltage which contains periodic perturbations to the gate of the MOS device. Afterwards, the drain current is determined from the measurement to analyze the ΔV_{th} of the MOS device. Schematic diagrams illustrating the OTF techniques are similar to those of the pulse/DC I-V and stress techniques. However, the OTF techniques apply a continuous stress voltage to devices even the testing current is applied as shown in Figs. 2-3-7 and 2-3-8.

As indicated in the insets of Fig. 2-3-9 (b) and Fig. 2-3-10 (b), the OTF techniques measure three points of the drain current with respect to the gate voltage to calculate the shift of the threshold voltage in each testing period. During the DC OTF measurements, the DC power supply applies a continuous stress voltage and periodic perturbations to the gate. Afterwards, the ampere meter is used to measure the drain current. During the pulse OTF measurements, a function generator applies multiple

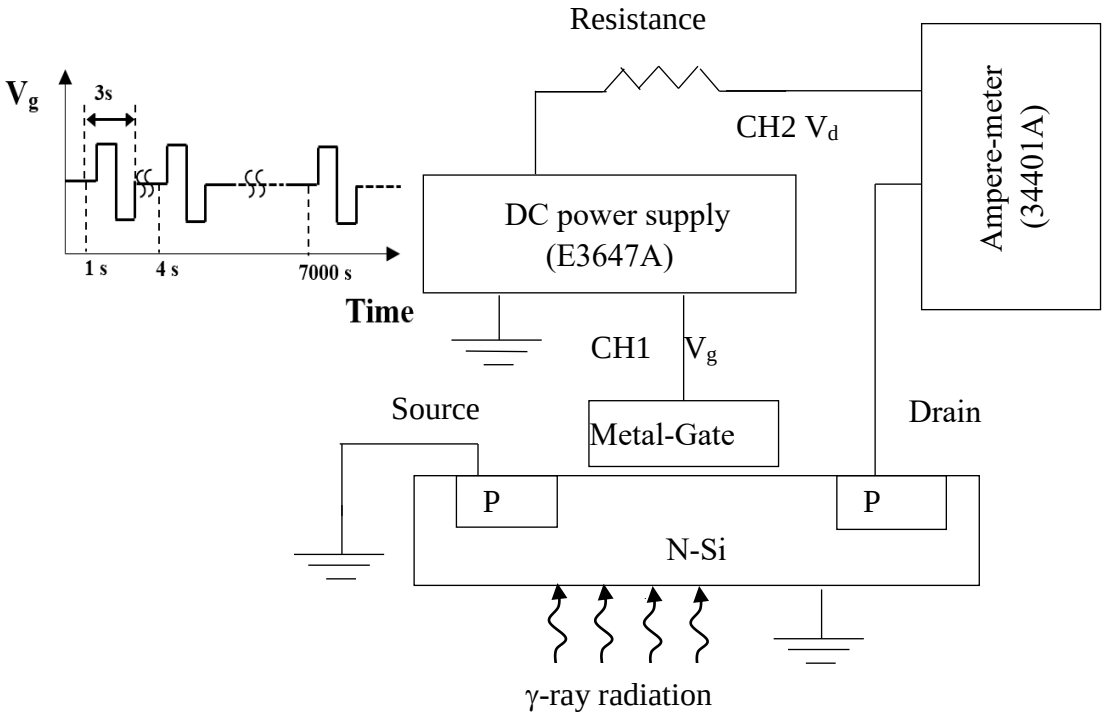


Figure 2-3-7. Schematic diagram of the measurement set-up for a MOSFET device using the DC on-the-fly technique under continuous γ-ray exposure in the ionizing radiation probe station system.

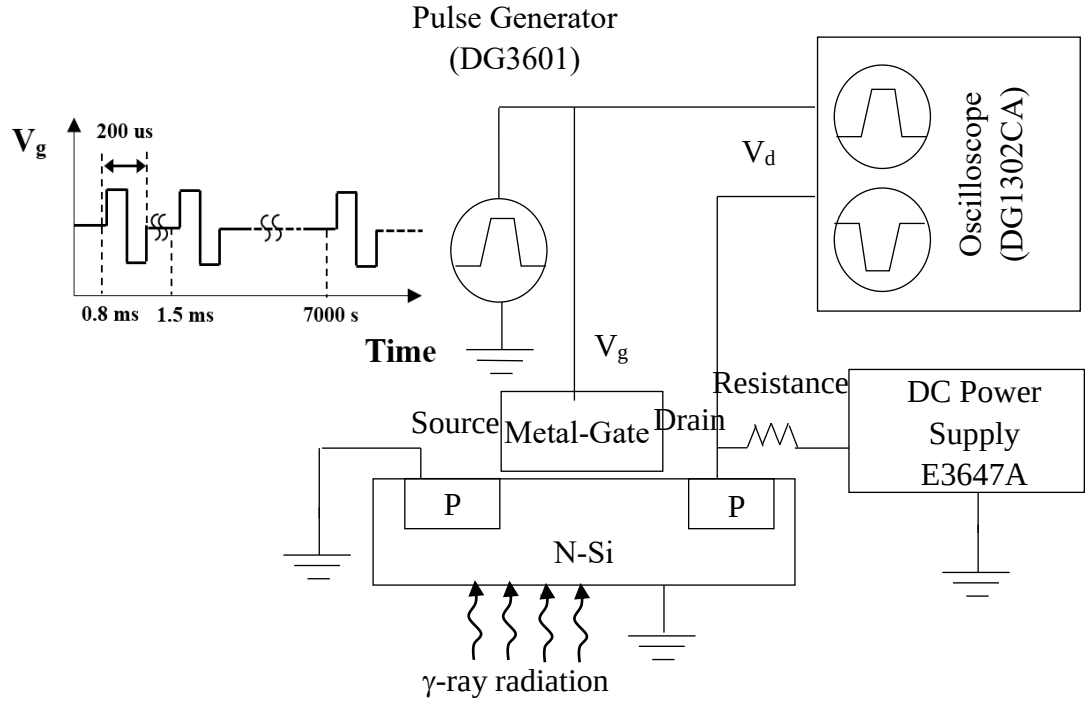


Figure 2-3-8. Schematic diagram of the measurement set-up for a MOSFET device using the pulse on-the-fly technique under continuous γ-ray exposure in the ionizing radiation probe station system.

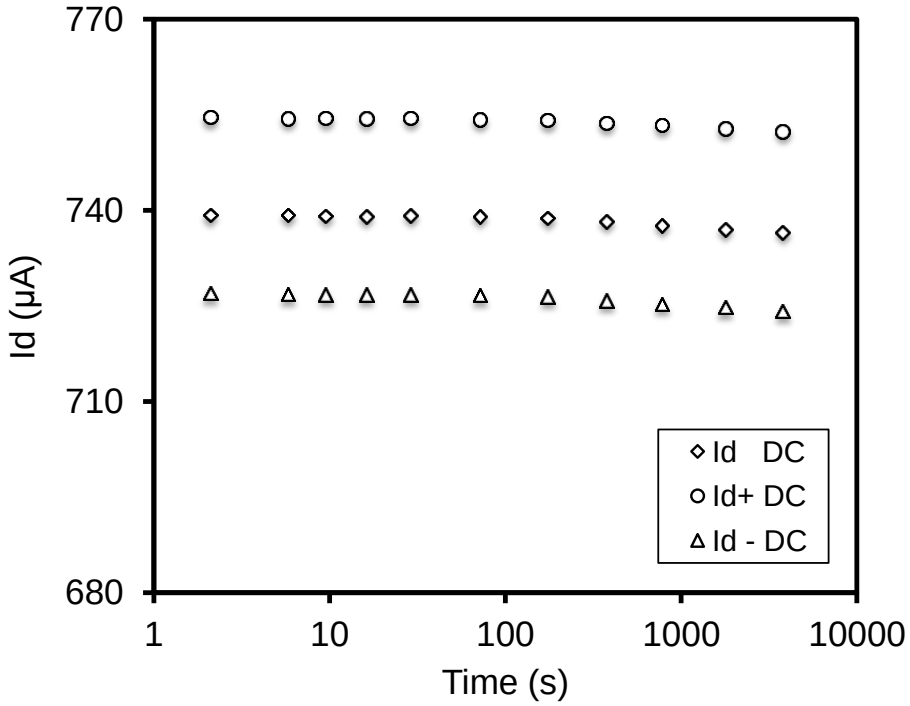
trapezoidal pulse signals to the gate of the MOSFET and the DC power supply applies a continuous voltage to the drain of the MOSFET. Meanwhile, the drain voltage is detected and converted to drain current using Eq. 2.2.

The inset of Fig. 2-3-9 (b) shows graphs of the gate and drain voltages versus the stress time characteristics. A continuous stress voltage of +0.5 V and periodic perturbations were applied to the gate dielectrics while a periodic stress voltage of +0.5 V was applied to the drain of a MOSFET. The amplitude of the periodic perturbation is ± 0.1 V and the pulse width is 3 s. The drain currents at different periodic perturbation levels (0 V, ± 0.1 V) were measured and more than 11 perturbations were applied. The drain current-time characteristics of the MOSFET are shown in Fig. 2-3-9 (a), with the leakage current of the MOSFET from 720 μA to 760 μA at different perturbation levels. Afterwards, the threshold voltage shift in each measurement point is calculated from the leakage current using Eqs. 2.3 to 2.7. For each perturbation, the transconductance of the MOS device is given by:

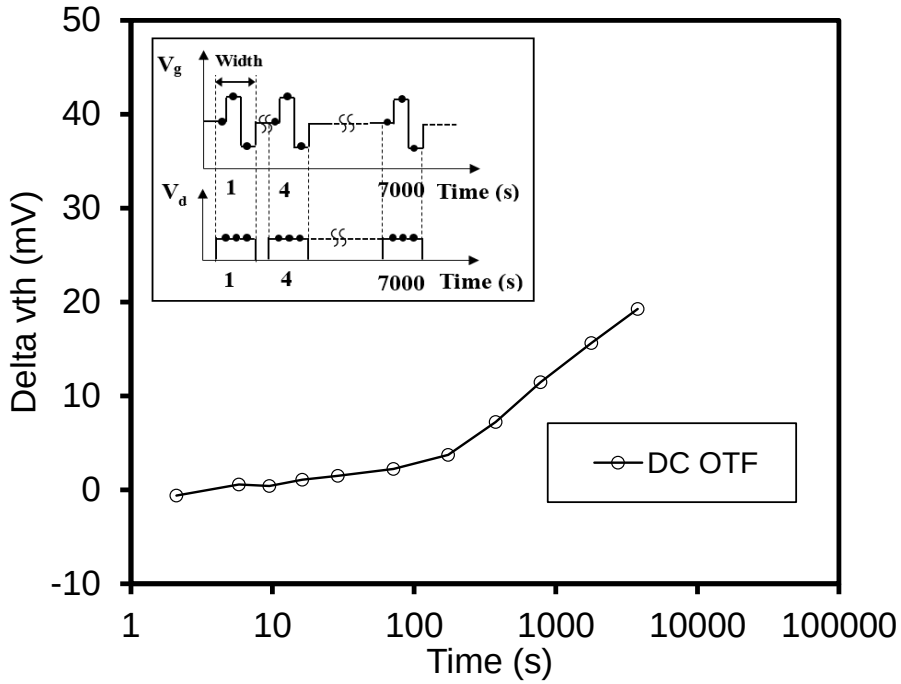
$$g_m \approx \frac{\Delta I_d}{\Delta V_g} = \frac{I_{d(V_g+D_v)} - I_{d(V_g-D_v)}}{2 \cdot D_v} \qquad (2.3)$$

where ΔI_d is the variation of the drain current in one perturbation; ΔV_g is the variation of the gate voltage; $I_{d(Vg+Dv)}$ and $I_{d(Vg-Dv)}$ are the drain currents with respect to the gate voltages of $V_g + D_v$ and $V_g - D_v$; D_v is the magnitude of the perturbations. For each continuous measurement period, the continuous stress voltages are constant. Hence, the ΔV_{th} (n) is given by:

$$\Delta V_{th}(n) = -\Delta\left[V_g - V_{th}(\mathrm{n})\right] = -\frac{\Delta I_d(n)}{g_m} \qquad (2.4)$$

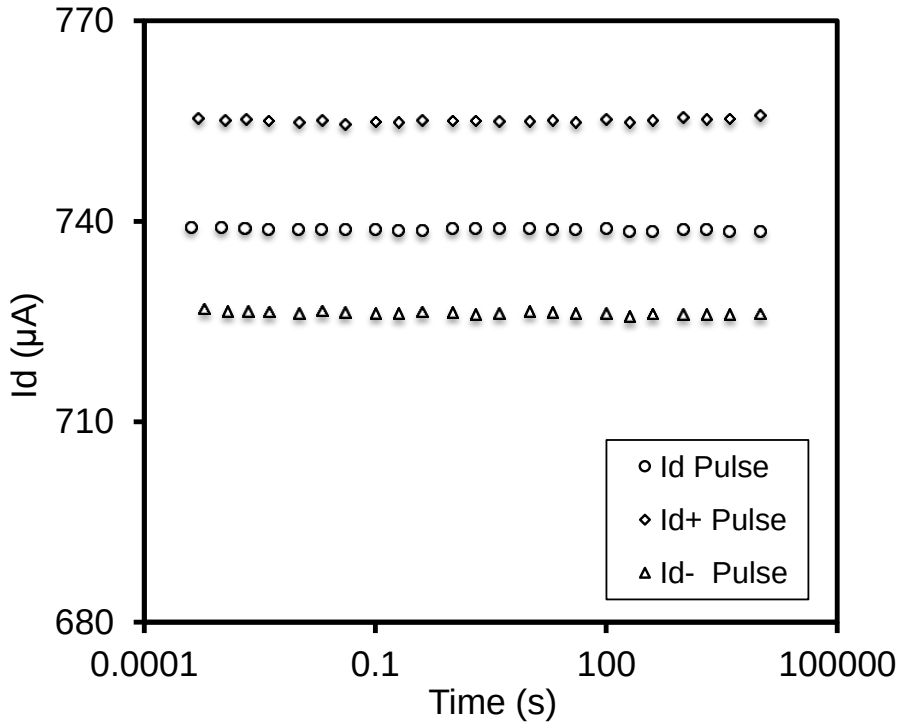


(a)

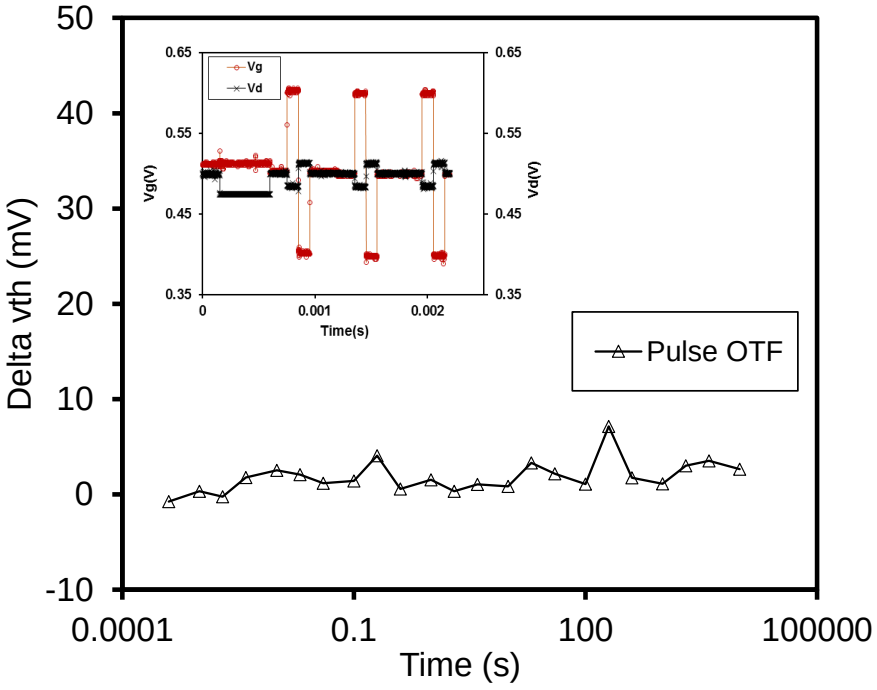


(b)

Figure 2-3-9. (a) Drain current versus stress time characteristics of a MOSFET, (b) Threshold voltage shift (ΔV_{th}) versus stress time characteristics of the MOSFET measured by the DC OTF technique. The inset shows the gate and drain voltage versus stress time characteristics at the periodic width of 3 s.



(a)



(b)

Figure 2-3-10. (a) Drain current versus time characteristics of the MOSFET, (b) Threshold voltage shift (ΔV_{th}) versus time curve of the MOSFET measured by the pulse OTF technique. The inset shows the gate and drain voltage versus time characteristics of the MOSFET with the pulse width of 200 μs.

where n is the number of measurement times. For each two adjacent measurement periods, the variation of the drain current ΔI_d (n) is given by:

$$\Delta I_d(n) = I_d(n) - I_d(n-1) \qquad (2.5)$$

and the average transconductance for each two continuous measurement periods follows the relation

$$g_m = \frac{g_m(n)+g_m(n-1)}{2} \qquad (2.6)$$

Hence, ΔV_{th} for N times of measurements using the OTF technique, namely ΔVth (n), can be expressed as

$$\Delta V_{th} \approx -\sum_{n=1}^{N} \frac{I_d(n)-I_d(n-1)}{[g_m(n)+g_m(n-1)]/2} \qquad (2.7)$$

ΔV_{th} is calculated and shown in Fig. 2-3-10 (b) by using Eq. 2.7. The result indicates that the ΔV_{th} is increased with the increasing of the stress time; 21 mV threshold voltage shift is measured after 7000 s at the applied bias voltage.

The inset of Fig. 2-3-10 (b) shows the first three pulse perturbations of the gate voltage and drain voltage-time characteristics of the MOSFET measured by the pulse on-the-fly technique. The pulse width of the perturbations is 200 μs. The continuous stress voltage of +0.5 V and $\pm$0.1 V periodic perturbations were applied to the gate; +0.5 V bias was periodically applied to drain of the MOSFET. The drain voltage V_d at different periodic perturbation level (0 V, $\pm$0.1 V) was measured. The drain current is calculated from the drain voltage using Eq. 2.2 as shown in Fig. 2-3-10 (a). The leakage current of the MOSFET is from 725 μA to 755 μA in each perturbation level. Afterwards, the threshold voltage shift in each measurement point is calculated from

the leakage current using Eqs. 2.3 to 2.7. The result indicates that the threshold voltage has no significant shift with the increase of the stress time as indicated in Fig. 2-3-10 (b). In addition, the first testing point of the pulse OTF technique is taken at time < 1 ms making the testing speed much faster than that of the DC OTF technique.

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Chapter 3: Development of Real-time and On-site Radiation Response Testing Techniques

The construction of a real-time and on-site radiation response testing system for semiconductor devices is reported in Chapter 3. Components of an on-site radiation response probe station, which contains a 1.11 GBq Cs^{137} gamma (γ)-ray source, and the dose absorbed rate of high-*k* materials are described in Section 3.1. For the sake of operators' safety, an equivalent dose rate of 70 nSv/h at a given operation distance is indicated by a dose attenuation model in the experimental environment. The real-time measurement system includes a conventional capacitance-voltage (C-V) and stress module, a pulse C-V and stress module, a conventional current-voltage (I-V) and stress module, a pulse I-V and stress module, a DC on-the-fly (OTF) module and a pulse OTF module.

Electrical characteristics of MOS capacitors or MOSFET devices are measured by each module integrated in the probe station under continuous γ-ray exposure and the measurement results are presented in section 3.2. To verify the reliability of the system, irradiation exposure of the sample is carried out with a dose rate of 0.175 rad/s and ± 1 V bias in section 3.3. Comparing with the on-site and real-time system, the conventional measurement in the literature exhibits smaller gate voltage shift of HfO_2 capacitors at

all total dose levels. Moreover, a large increase of gate voltage shifts up to 1 V is observed as measured using the pulse C-V and stress technique. Analysis of the gate voltage shifts (ΔV_g) of the MOS capacitors suggests that the on-site and real-time/pulse measurements detect more serious degradation of the HfO_2 thin films compared with the off-site irradiation and conventional measurement techniques.

In space environments, the accumulation of total dose is a long process as the representative distribution of dose rate is $10^{-2} \sim 10^{-6}$ rad/s (Si) [1]. Over the last thirty years, the effects of 10-keV X-rays irradiation on high-*k* materials at high dose rates (50 to 5600 rad (SiO_2)/s) have been investigated extensively [2-5]. However, up to now, very little research has been published on radiation effects on high-*k* thin film materials irradiated at low dose rates after either X-ray exposure or γ-ray irradiation.

γ-radiation is known to induce degradation of components thus degrading the device performance [6, 7]. The degradation and failures are caused by the charges built up in gate dielectrics leading to a ΔV_{FB} or threshold voltage shift (ΔV_{TH}). So far, total-dose irradiation testing of semiconductor devices exposed to X-ray has been demonstrated on a 10-keV ARACOR semiconductor X-ray irradiator which was developed by Palkuti and LePage in early 1980s [8, 9]. Cobalt-60 irradiations are performed on ceramic-lidded devices in Gammacell Blood Irradiator at a dose rate of ~200 rad (SiO_2)/s [9, 10]. These conventional evaluation of radiation induced V_{TH}/V_{FB} shift has been carried out in an off-site condition after the exposure due to radiation safety consideration. The conventional radiation response measurement processes are

i) a MOS device is irradiated by γ-ray under certain voltage biasing condition using a radiation exposure facility; ii) the radiation exposure and voltage biasing are interrupted and the sample is taken out from the on-site irradiation chamber; and iii) electrical characterization of the irradiated devices is performed by traditional current-voltage (I-V) or/and capacitance-voltage (C-V) techniques [4]. According to the mechanism of radiation-induced defects or degradation in semiconductor materials, the interruption of irradiation and voltage biasing may cause a rapid recovery of the ΔV_{TH} /ΔV_{FB} [11-13]. Moreover, the conventional measurement techniques may underestimate the defects or degradation in dielectrics because the measurements cannot be completed in a very short time in the order of a few micro-seconds. To precisely detect the effects of total ionizing dose on semiconductor devices, it is necessary to upgrade the conventional evaluation of radiation response to on-site measurement; meanwhile, pulse and stress techniques are used to monitor the evolution of the gate and drain voltage waveforms. The techniques can measure the characteristics of the semiconductor devices in milliseconds while the devices are continuously irradiated by γ-rays. The effects of total ionizing dose on ΔV_{FB} to HfO_2 capacitors with voltage biasing are re-examined by the proposed method.

3.1 On-Site Measurement System

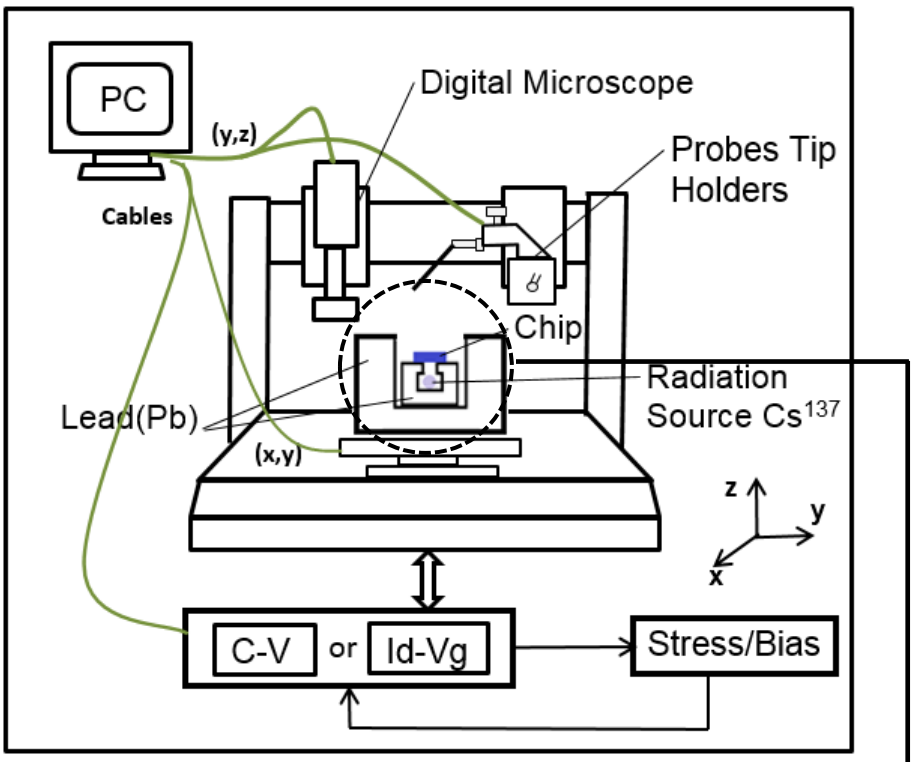
A novel radiation response testing system is developed in this section by integrating an on-site measurement probe station with a real-time testing system. A mathematical model has been established to calculate the dose rate absorbed by gate dielectrics tested

in the radiation response testing system. In addition, a lead protection application is proposed to obtain a safe operation environment. The system development and details of the aforementioned factors are described in each section.

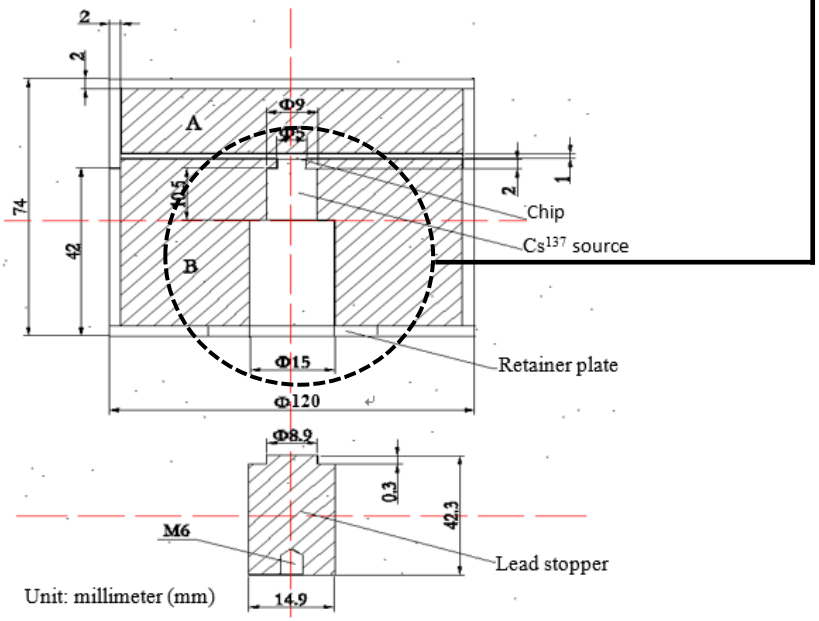
3.1.1 Gamma-Ray Wafer Probe Station Platform

A real-time and on-site radiation response testing system is composed of a program-controlled ionizing radiation probe station and a real-time testing system. The proposed probe station is developed from a conventional program-controlled probe station platform as shown in Fig. 3-1-1 (a) [14]. The probe station platform consists of a platform with an x-y adjustable stage, an optical microscope equipped with a digital camera, an on-wafer probe mounted on a precision positioner, a testing sample loading chuck mounted on a rail, and a lead container to keep the γ-ray radiation source at the center of the platform which is surrounded by an annular lead wall. Both the optical microscope and the probe positioner are mounted on robotic arms with the program-control PC placed outside the probe station. The robotic arms can move vertically along the z-axis and horizontally along the y-axis while the lead container mounted on a stage can move in a horizontal plane along the x-axis and the y-axis.

To design a desirable and safety-compliant real-time radiation response testing system, a lead container and an annular lead wall are employed to surround the radiation source as illustrated in Fig. 3-1-1 (a). The container itself is made of lead and the shield thickness of the lead container is designed to be 5 cm to attenuate the γ-ray. A lead cover and a bottom case are developed to preserve and transport the radiation source



(a)



(b)

Figure 3-1-1. (a) Real-time and on-site measurement system of γ-ray radiation with stress-and-sense pulse I-V, pulse C-V or/and pulse On-The-Fly measurement capabilities. (b) Schematic diagram of the lead container with a Cs^{137} γ-ray radiation source in the ionizing radiation probe station system.

when the irradiation exposure is in off time as shown in Fig. 3-1-1 (b). The lead container has a small opening on the top surface where the semiconductor chip under test is placed above. The γ-ray radiation source with an activity of 1.11 GBq is placed into the lead container. The lead wall with 3 cm lead surrounding the container is for blocking any possible γ-radiation leaking sideways from the source.

To perform radiation response measurements, a semiconductor chip needs to be first placed on the loading chuck which is outside the ionization probe station. Since the loading chuck is not in proximity of the radiation source when the semiconductor chip is mounted, the radiation risk to the human operator is negligible. Once the chip is mounted, the loading chuck can be controlled by a PC to move the chip into the ionization probe station and above the lead-walled container where the γ-ray source is kept. Initially, when the chip or wafer piece is settled on the lead-walled container, the robotic arm holding the microscope equipped with a digital camera can be controlled by the PC to move in the y-z direction to a position above the chip for digital imaging of the on-chip devices as shown in Fig. 3-1-1 (a).

For initial probe positioning, low magnification of the optical microscope should be used for a zoomed-out view of both the chip and nearby regions. Primary adjustments of the robotic arm hold the probe positioner to move the probe to the top of the chip in the y-z plane. The probe should be within the zoomed-out view of the microscope. With the digital imaging of the optical microscope, the probe can be positioned precisely as it is visible on the PC's screen which displays the real-time view

of the optical microscope. By gradual increase of the magnification of the optical microscope and the careful movement of the probe positioner, the devices in the chip can then be probed for electrical measurements while the chip is subjected to γ-ray radiation. The whole process is done through controlling the robotic arms and the optical microscope with digital imaging equipment which are all remote controlled by a PC. The human operator can stay at least one meter away from the radiation source for operating the PC which is outside the ionization radiation probe station. The radiation risk to the human operator is therefore much minimized.

3.1.2 Dose Attenuation in the Experimental Environment

To protect the operators around the system from radiation hazard, a lead container and an annular lead wall are employed to surround the radiation source. The thickness of the lead protection system is calculated to establish a safe experimental environment. In that respect, a calculation model of the dose attenuation in the experimental environment around the system is indicated as illustrated in Fig. 3-1-2. A Cs^{137} γ-ray

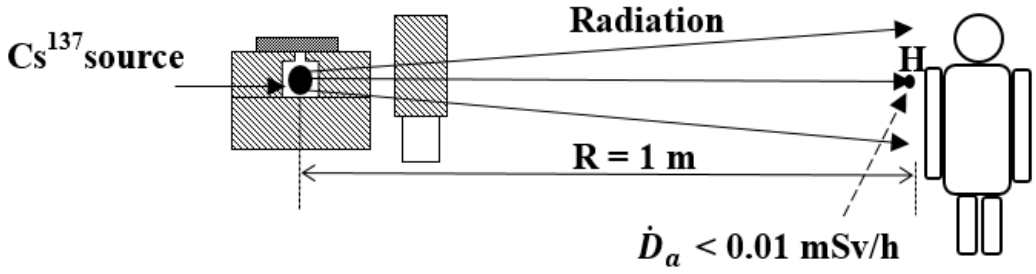


Figure 3-1-2. Calculation model of the dose attenuation from a Cs^{137} point-like radiation source to a technician who operates the ionizing radiation probe station system.

radiation source is used to irradiate MOS devices in the system. The activity of the Cs^{137} γ-ray radiation source is 1.11 GBq which gives off 1.11×10^{9} γ-photons per second with energy E = 662 keV. The irradiation dose rate in the air is given by [15]:

$$\dot{X} = \frac{A\cdot\ \Gamma}{R^2} \qquad (3.1)$$

where Γ is the exposure rate constant, R is the distance from the source to the operators near the system, A is the activity of the Cs^{137} γ-ray radiation source. Here, Γ = 6.312×10^{-19} $C\cdot m^2\cdot kg^{-1}\cdot Bq^{-1}\cdot S^{-1}$, R = 1 m. For the condition of charged ion balancing, the equivalent dose rate in the air under Cs^{137} γ-ray radiation source is indicated by [15]:

$$\dot{D}_a = \dot{X}\cdot\frac{W_a}{e} \qquad (3.2)$$

where $\dot{X}$ is the irradiation dose rate in the air, W_a is the average energy consumption of the generation of an ion by an electron in the air, e is the charge of an electron. Here, $W_a = 5.42\times10^{-18}$ J, 1 e = 1.602×10^{-19} C. For the 1.11 GBq Cs^{137} γ-ray radiation source, the equivalent dose rate is:

$$\dot{D}_a = \dot{X}\cdot 33.85 \qquad (3.3)$$

From Eqs. 3.1, 3.2, and 3.3, the equivalent dose rate at one meter (operation distance) away from the source without any protection system can be determined as $\dot{D}_a \approx 0.0854$ mSv/h. According to the International Commission on Radiological Protection (ICRP) in laboratory [16], both a lead wall and a lead container are required to be designed in such a way to attenuate the equivalent dose rate $\dot{D}_a$ to be less than 0.01 mSv/h at the operating distance. Hence, $\dot{D}_a$ at the operating distance should be reduced by more than 8.54 times. According to the National Council on Radiation Protection and

Measurements (NCRP) No. 46 1976 [17], the thickness of the lead container and the lead wall to reduce the dose equivalent rate to be a half of the initial value (0.0854 mSv/h) under Cs^{137} γ-ray radiation source is 0.78 cm. The thickness of the lead wall and the lead container to reduce the $\dot{D}_a$ to be 1/K of the initial value is given by [16]:

$$d = 0.78 \times \frac{\log K}{\log 2} \qquad (3.4)$$

where K is a multiple of the attenuation of $\dot{D}_a$. Here, K should be larger than 8.54 to attenuate $\dot{D}_a$ to be less than 0.01 mSv/h. From Eq. 3.4, the shield thickness of the lead wall or the lead container should be no less than 2.41 cm. In case of the operators carrying out the experiments within 1 m around the system, the shield thickness of the lead container is designed to be 5 cm and the lead wall 3 cm. The multiple of the attenuation of $\dot{D}_a$ equals to 1223.17 in this case. $\dot{D}_a$ at one meter away from the Cs^{137} source after the 8 cm lead protection (at point H as shown in Fig. 3-1-2) is decreased to 70 nSv/h. A CM7001EX real-time radiation detector is used to measure the actual equivalent dose rate at point H. The actual value of $\dot{D}_a$ in the horizontal direction at the operation distance (point H) is 140 nSv/h after taking the background (100 nSv/h) into account. So the actual measured $\dot{D}_a$ (140 nSv/h) is very close to the calculated one (70 nSv/h). Hence, the human operator can stay at least one meter away from the radiation source for operating the PC which is outside the ionization radiation probe station. The radiation risk to the human operator is therefore much minimized.

3.1.3 Dose Rate for High-*k* Dielectrics

A point source model has been established in previous work to calculate the dose

rate absorbed by gate dielectrics [4]. In the point source model, the volume of a radiation source is considered to be zero. High-energy photons are emitted from the point source. The photons emitted to target materials is calculated along the axis from the point source to capacitor surface. However, if the volume of the radiation source is relative large compare to the distance between radiation source and capacitor surface. The numbers of photons emitted to target materials will be overestimated. The point source model can only be used when the distance from the radiation source to the irradiated device is 5 times larger than the size of the radiation source [4].

In the ionizing radiation probe station system, the distance between the radiation source and the irradiated device is 0.3 cm and the length of the radiation source is 1 cm. Hence, a novel calculation model is established in this work to calculate the dose rate absorbed by the gate dielectrics under test in the system. The 1.11 GBq Cs^{137} γ-ray radiation source emits 1.11×10^{9} γ-photons per second with the energy E of 662 keV. The radiation source has a radius R of 0.4 cm and a length L of 1 cm. The distance from the top surface of the source to the device is d = 0.4 cm. It is assumed that the radiation source emits γ-photons uniformly. In the calculation model, as illustrated in Fig. 3-1-3, the number of particles emitted by the radiation source per unit time and unit volume is given by:

$$N_i = \frac{\mathrm{N(E)}}{L\pi R^2} \qquad (3.5)$$

where N(E) is the number of photons of energy E, emitted per unit time by the source. Here, N(E) = 1.11×10^{9} photons/s. Hence, the number of particles passing through the

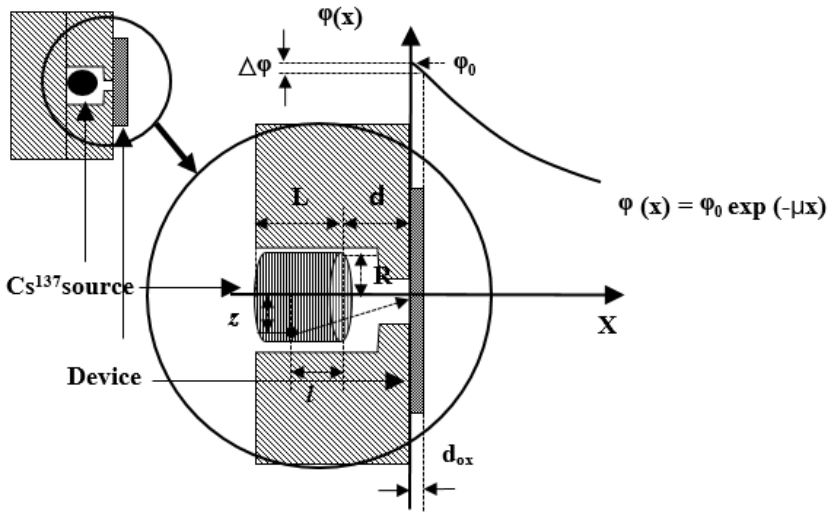


Figure 3-1-3. Calculation model of the dose rate attenuation of gate dielectrics under test in the ionizing radiation probe station system.

target dielectric irradiated by a unit volume of the radiation source per unit time, which has a distance of *z* to the center axis of the radiation source and a distance of *l* to the surface of the radiation source as shown in Fig. 3-1-3, is given by:

$$\varphi_0' = \frac{N_i 2\pi z}{4\pi((l+d)^2+z^2)} \qquad (3.6)$$

The total particle flux of the device is given by:

$$\varphi_0 = \int_0^L \int_0^R \frac{N_i 2\pi z}{4\pi((l+d)^2+z^2)} dz\, dl \qquad (3.7)$$

Here, $\varphi_0 \approx 1.316 \times 10^8$ photons/cm^2·s. The particle flux of the target dielectric is decreased compared with the point source model $\varphi_0 \approx 9.815 \times 10^8$ photons/cm^2·s [4]. The attenuation of the particle flux when γ-photons pass through the target dielectric or other materials, which has a thickness of *x*, is given by:

$$\varphi(x) = \varphi_0 \exp(-\mu_m \rho x) \qquad (3.8)$$

where μ_m is the total mass attenuation coefficient of the target material. Generally, μ_m is expressed as $\mu_m = \mu / \rho$, where μ is the linear attenuation coefficient and ρ is the density of the target material. The total mass attenuation coefficient indicates the probability of attenuation for a particle when it passes through the target materials of unit thickness. The energy absorbed by target material when a γ-photon passes through the target dielectrics or other materials is expressed as μ_{en}/ρ [18]. μ_{en} is the linear energy absorbed coefficient of the target material. The values of total mass attenuation coefficient and energy absorbed coefficient of single elemental materials of energy E = 662 keV are taken from Physical Reference Data of National Institute of Standards and Technology (NIST) as listed in Table 3-1-1 [19]. For example, the total mass attenuation coefficient and the mass energy absorbed coefficient of a compound material HfO_2 are given as follows [20]:

$$\mu_m(HfO_2) = \mu_m(Hf)\frac{M(Hf)}{M(Hf)+2M(O)} + \mu_m(O)\frac{2M(O)}{M(Hf)+2M(O)} \qquad (3.9)$$

$$\frac{\mu_{en}}{\rho}(HfO_2) = \frac{\mu_{en}}{\rho}(Hf)\frac{M(Hf)}{M(Hf)+2M(O)} + \frac{\mu_{en}}{\rho}(O)\frac{2M(O)}{M(Hf)+2M(O)} \qquad (3.10)$$

where M is the molar mass of the target elements. The mass attenuation coefficient and mass energy absorbed coefficient of six materials of energy E = 662 keV have been calculated using Eqs. 3.9 and 3.10 as shown in Table 3-1-2. The dose rate D_R of a thin film is given by:

$$D_R = \int_0^{d_{ox}} E \times \varphi_0 \exp(-\mu x) \times \frac{\mu_{en}}{\rho} \times \frac{1}{d_{ox}} dx. \qquad (3.11)$$

where d_{ox} is the thickness of the irradiated material. When the thickness of the irradiated material is very small, the dose rate D_R can be given by:

$$D_R \approx E \times \varphi_0 \times \frac{\mu_{en}}{\rho} \qquad (3.12)$$

In this work, the Cs^{137} γ-ray radiation source emits 1.11×10^9 γ-photons per second with energy E = 662 keV. The particle flux φ_0 and the mass energy absorbed coefficient

Table 3-1-1. Total mass attenuation coefficient (μ_m) and mass energy absorbed coefficient (μ_{en}/ρ) of single elemental materials for energy E = 662 keV.

Element	Li	O	F	Si	Hf	Zr	La
μ_m (cm^2/g)	0.0672	0.0777	0.0736	0.0776	0.0984	0.0739	0.0803
μ_{en}/ρ (cm^2/g)	0.0254	0.0294	0.0278	0.0293	0.0494	0.0293	0.0361

Table 3-1-2. Total mass attenuation coefficient (μ_m), mass energy absorbed coefficient (μ_{en}/ρ) and dose rate (D_R) of different materials for energy E = 662 keV.

Thin films	Si	LiF	SiO_2	HfO_2	ZrO_2	LaZrOx
μ_m (cm^2/g)	0.0776	0.0719	0.0777	0.0952	0.0749	0.0775
μ_{en}/ρ (cm^2/g)	0.0293	0.0272	0.0294	0.0432	0.0293	0.0329
D_R (rad/s)	0.0409	0.0369	0.041	0.0603	0.0409	0.0459

Table 3-1-3. TLD response to Cs^{137} irradiation and the dose rate of HfO_2 after taken into account the dose enhancement effect at the same position as that of the irradiated high-*k* devices in the system.

No. of TLDs	Exposure time (min)	Wait time (hour)	Average total ionizing dose (TLDs) (Rad)	Average Dose Rate (TLDs) (rad/s)	Dose Rate (HfO_2) (enhanced) (rad/s)
YQ-001-002	5	72 – 96	11.1	0.037	0.139
YQ-003-004	10	72 – 96	17.2	0.029	0.109
YQ-005-006	15	72 – 96	23.6	0.026	0.098
YQ-007-008	20	72 – 96	39.0	0.032	0.12

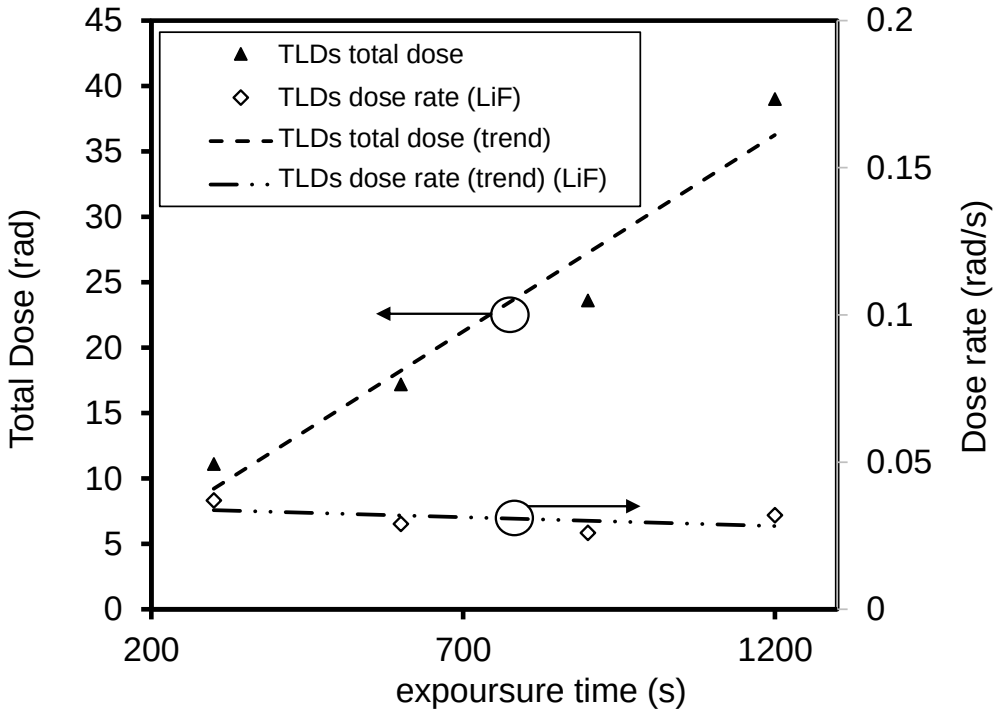


Figure 3-1-4. Total dose and dose rate of TLDs response to Cs^{137} irradiation at the same position as that of the irradiated high-κ devices in the system. The dash lines represent respectively the trend lines of the dose rate and total dose of LiF TLDs.

μ_{en}/ρ for each material have been calculated using Eqs. 3.7 and 3.10. Hence, from Eq. 3.12, the dose rate of the different materials is calculated and listed in Table 3-1-2.

As discussed in section 1.2, to verify the calculated dose rates, thermoluminescent dosimeters (TLDs) were employed to measure the dose rate at the same position as that of the irradiated high-*k* devices in the radiation response testing system. Four groups of TLDs have been used to calibrate the fading curves at different total dose levels of Cs^{137} γ-ray source as shown in Table 3-1-3. Each group includes two TLDs to improve the accuracy. A discrepancy of the dose rate of TLDs between each groups was observed as indicated in Table. 3-1-3 and Fig. 3-1-4. The results indicate that the dose rates of

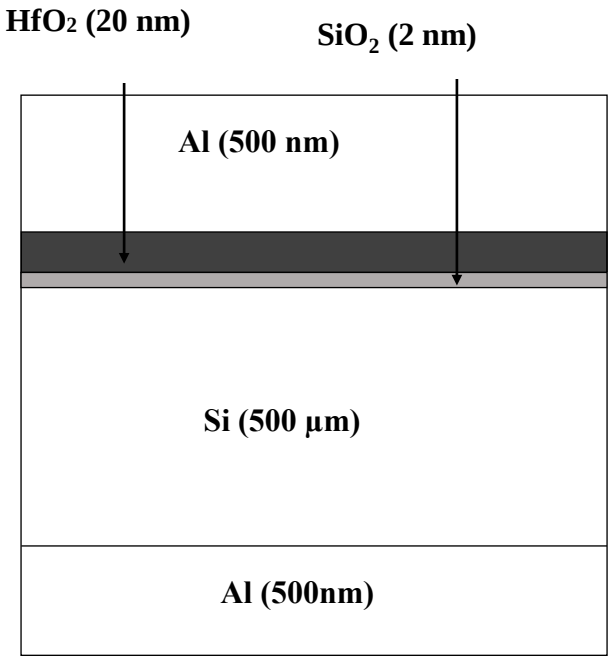


Figure 3-1-5. Schematic diagram showing the layered structure of the MOS capacitors under test; 20 nm-HfO_2 thin film layers were deposited on 500 μm n-type silicon; MOS capacitors were formed with aluminum as the top electrodes and back contact with a thickness of 500 nm.

TLDs measured by each groups are similar. In each case, the average dose rate obtained from short TLDs exposures is 16% lower than the dose rate of LiF (0.0369 rad/s) calculated from the calculation model.

Previous results in the literature demonstrated that high-*k* materials in metallization and packaging can lead to significant dose reduction and enhancement in low- and medium-energy X-ray environments [21]. The dose enhancement effects are mainly due to the reflection of the high-energy particles from high-z materials that are nearby the gate dielectrics. The reflected particles would pass through the gate dielectric layers, and collided the atoms in gate oxide. Part of these reflected particles has been already passed through the gate dielectrics when they emitted from radiation source. Therefore, the reflected particles lead to an enhancement on total dose absorption of gate dielectrics. The dose enhancement effects can lead to increased energy deposition in device regions with low-atomic number (low-z), such as gate oxide. Fig. 3-1-5 shows a schematic diagram of the MOS capacitor employed in this study which is similar to the structure discussed in the literature, as the HfO_2 is surrounded by lower atomic number materials (e.g. Si, Al).

In a medium-energy (400-keV) X-ray environment, the total dose absorbed in an HfO_2 based capacitor is approximately equals to 6.2 times of that in a SiO_2 capacitor after taken into account dose enhancement effect. As calculated from our calculation model, the dose rate for HfO_2 is approximately equals to 2.7 times of that for SiO_2 at the energy level of 400 keV [21]. Hence, the ratio of dose absorbed for HfO_2 relative

to SiO_2 obtained from the experiment is supposed to be enhanced by 2.3 times compared with that from the calculation which can be expressed as:

$$\frac{[D_{a(HfO_2)}/D_{a(SiO_2)}]_{measured}}{[D_{a(HfO_2)}/D_{a(SiO_2)}]_{calculated}} \approx 2.3 \qquad (3.13)$$

In this study, we use the Cs^{137} γ-ray source with energy of 662 keV, and only the total dose deposited in TLDs (LiF) have been measured instead of SiO_2. As compared to the results in the literature, we hence assume that the ratio of dose absorbed for HfO_2 relative to LiF obtained from experiment will be enhanced by 2.3 times compared to that obtained from the calculation model. In other words, the dose rate measured from TLDs and calculated dose rate of LiF were used instead of SiO_2 to calculated the actual dose rate of HfO_2. Moreover, the calculated dose rate of HfO_2 (0.0603 rad/s) is also used in Eq. 3.13. According to the dose rate measured from TLDs using the calibrated dosimetry system, the dose rates of HfO_2 in experiment in each case are shown in Table. 3-1-3 after taken into account the dose enhancement effect and the average value equals 0.116 rad(HfO_2)/s. Therefore, the dose rate of HfO_2 thin films in this study is 0.116 rad(HfO_2)/s.

3.2 Real-time and Conventional Characterizations

To date, the electrical characterization of high-*k* dielectrics has been mainly focusing on DC measurements and dynamic measurements [22-24]. In DC measurements, a sweeping voltage is applied to obtain the values of capacitance or leakage current of MOS devices in a few seconds. During the measurements, charges

injected from electrode or substrate can be trapped by defects in the oxide or Si/oxide interface under the positive or negative applied field. However, with the variation of the applied field (sweeping), these trapped charges can be compensated in a few milliseconds. On the other hand, the forward or reverse sweeping will take a few seconds. It is difficult to detect the progress of fast trapping and de-trapping by using DC measurements [25-27]. However, in dynamic measurements, trapezoidal pulse signals are applied to obtain the values of leakage currents in hundreds of microseconds. Meanwhile, the obtained values of leakage current can be amplified and converted into values of capacitance. Hence, dynamic measurements are employed to analyze the reliability of semiconductor due to the fact that it reduces the impact of charge trapping on the measurement results [25, 27].

In the radiation response measurements, ionizing radiation generates electron-hole pairs (EHPs) in the gate dielectrics under test. Some of the EHPs recombine in a short time and do not affect the device performance. If a positive electric field is applied to the gate dielectrics, the un-recombined EHPs will be separated by the electric field. The electrons will be swept out of the oxide in a picosecond. However, the surviving holes transport towards the cathode slowly via defect sites because they have a relatively low mobility [2, 28, 29]. Some of the surviving holes will recombine with the electrons injected from the silicon substrate, and other holes will be trapped by oxide traps during the transport, forming positive oxide trapped charges. These trapped charges will cause the radiation-induced threshold voltage shift. When the surviving holes approach the silicon-oxide interface, protons (H^+) are released and react with silicon-hydrogen (Si-

H) bonds to form radiation-induced interface traps [30-32]. Apart from hole trapping in the oxide, most gate dielectrics can also trap a significant density of electrons. Some high-*k* films are more prone to generation of negative oxide trapped charges than positive oxide trapped charges [7, 33]. On the other hand, if the applied electric field and the ionizing radiation are interrupted for a period of time, some of the trapped charges will be compensated and this gives rise to a recovery of radiation-induced threshold voltage shift. Hence, off-site radiation response measurements may underestimate the radiation induced degradation. It is therefore significantly important to apply on-site and pulse measurements in the experiments. In this study, conventional C-V and stress techniques are used to compare the results with dynamic measurements.

The characteristics analyzing equipment (and the controlling PC) are placed outside the probe station. A real-time measurement system is comprised of modules capable for conventional C-V, DC I-V, DC on-the-fly, pulse C-V, pulse I-V, and pulse on-the-fly measurements. In addition, a stress system is applied to each measurement technique and it will generate continuous stress voltage during irradiation or testing. All the electrical measurement instruments (except the digital oscilloscope Rigol DS1302CA) are connected using GPIB cables for programmable control and data acquisition. Together with the PC-controlled movement of the optical microscope, probe positioner and movable stage inside the ionization radiation probe station, the electrical measurement equipment connected to a controlling PC makes the real-time radiation response measurements semi-automated.

3.2.1 Conventional C-V and Stress

A conventional C-V and stress measurement system is set up with an Agilent 4284 LCR meter and a PC. Fig. 3-2-1 is a schematic diagram showing the measurement of a MOS capacitor using the conventional C-V and stress technique under continuous γ-ray exposure in the ionizing radiation probe station system. The LCR meter generates

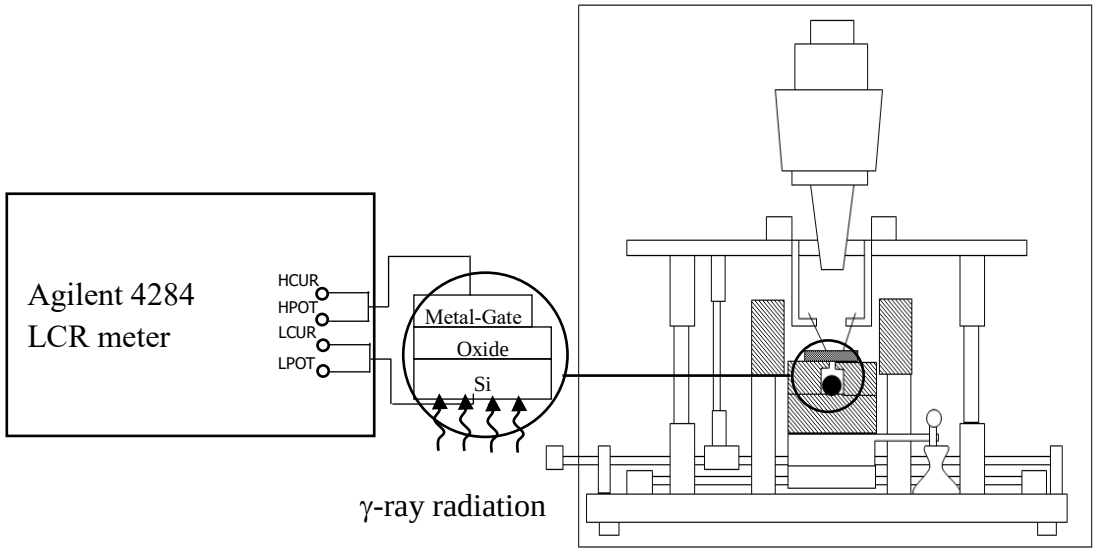


Figure 3-2-1. Schematic diagram showing the measurement set-up for a MOS capacitor using the conventional C-V and stress technique under continuous γ-ray exposure in the ionizing radiation probe station system.

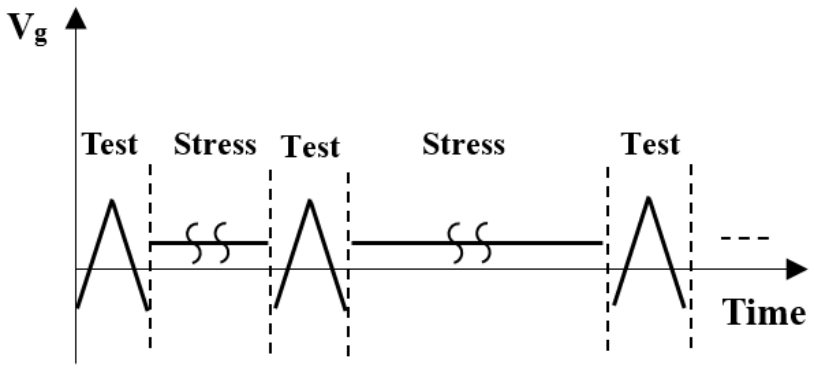
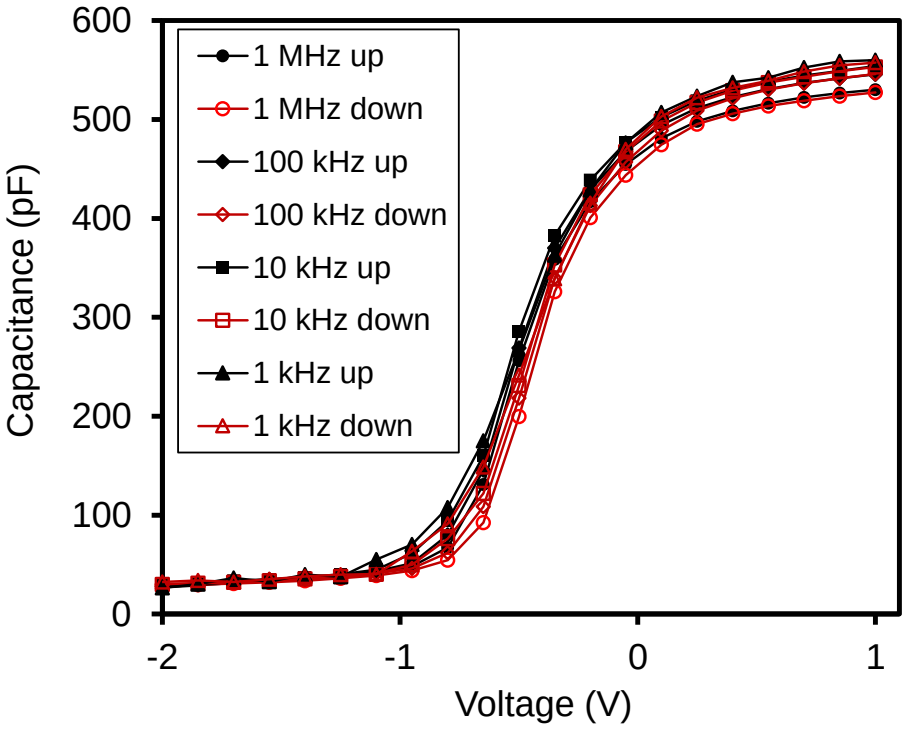


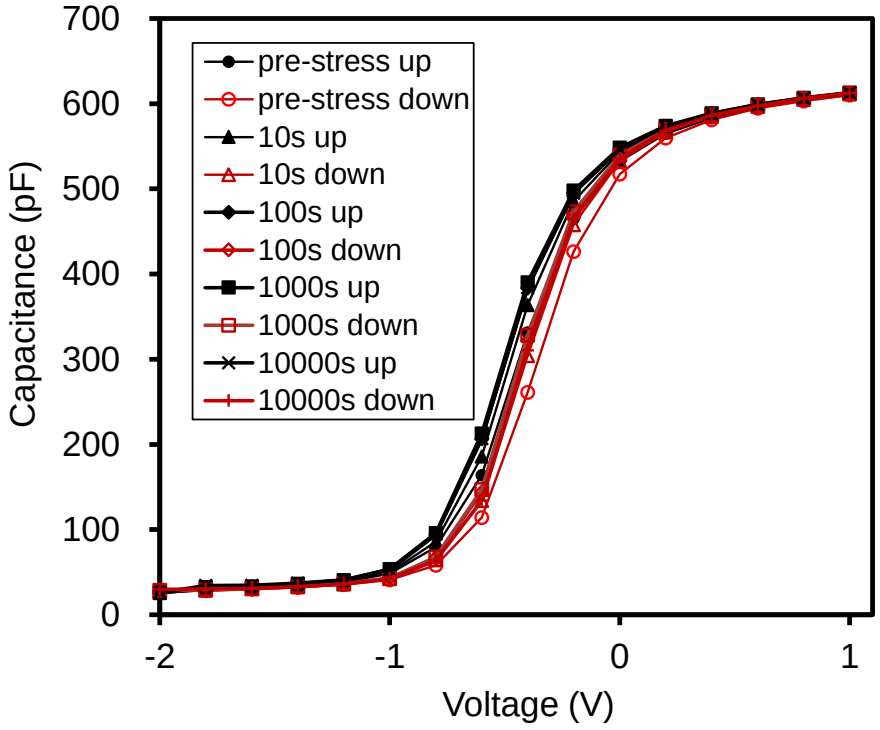
Figure 3-2-2. Graph of the gate sweeping voltage for C-V test and stress voltage versus time characteristics of the conventional C-V and stress technique.

a sweeping voltage for C-V test or a bias voltage to the gate of the MOS capacitor with a voltage range from -40 V to +40 V and a frequency range from 20 Hz to 1 MHz. Afterwards, the capacitance of the MOS capacitor is recorded and primary C-V curves are plotted by a MATLAB program. The PC controls the system using a GPIB connection cable. Fig. 3-2-2 shows a graph of the gate sweeping voltage and stress voltage(V_g) versus the sweeping/stress time in the conventional C-V and stress module. The stress voltage and the sweeping voltage are alternately applied to the MOS device under test by the Agilent 4284 LCR meter. The duration of the stress voltage is controlled by the PC.

In Fig. 3-2-3 (a), C-V curves of MOS capacitors with HfO_2 dielectrics were measured using the conventional C-V and stress technique from 1 kHz to 1 MHz. The C-V curves with different frequencies were measured by both forward and reverse sweeping voltages. The result of Fig. 3-2-3 (a) indicates that the MOS capacitor has appropriate C-V curves from -2 V to +1 V using the conventional C-V and stress technique. In Fig. 3-2-3 (b), C-V curves of the MOS capacitors with HfO_2 dielectrics were measured using the conventional C-V and stress technique at a frequency of 1 MHz and +1 V bias for a stress period of 10,000 seconds. It can be seen that there is very little negative shift of the flat band voltage under +1 V bias. The result illustrates that very few positive oxide-trapped charges and/or interface traps have been generated or observed in the oxide and/or silicon-oxide interface by the applied positive bias.



(a)



(b)

Figure 3-2-3. The conventional C-V and stress technique. (a) C-V curves of MOS capacitors with HfO_2 dielectrics from 1 kHz to 1 MHz, (b) C-V curves of the MOS capacitors with HfO_2 dielectrics at a frequency of 1 MHz and +1 V bias for a stress duration of 10,000 seconds.

3.2.2. Pulse C-V and Stress

A pulse C-V measurement system is set up with a Rigol DS1302CA oscilloscope, a Rigol DG3061A function generator, a Keithley 428 current amplifier and a PC. Fig. 3-2-4 shows a schematic diagram of the measurement of a MOS capacitor using the pulse C-V technique under continuous γ-ray exposure in the ionizing radiation probe station system. Initially, the function generator applies a trapezoidal pulse signal (V_g) to the gate of the MOS capacitor. Afterwards, the leakage current of the capacitor is detected and converted to an output voltage signal (V_{out}) by the current amplifier. Meanwhile, the output voltage signal is fed to the oscilloscope and data is recorded. These measurement processes can be completed in one millisecond. The capacitance of the MOS capacitor can be expressed as:

$$C(V_g) = \frac{V_{out} - V_{offset}}{A * dV_g/dt} \qquad (3.14)$$

where V_g is the applied gate voltage; V_{out} is the output voltage from the current amplifier, V_{offset} is the offset voltage to set the amplitude of the trapezoidal pulse signal V_g; dV_g is the variation of the gate voltage; dt is the variation of measuring time; and A is the amplification factor of the amplifier. The magnitude of offset voltage equals to the value of middle point of input pulse voltage.

Fig. 3-2-5. (a) shows a schematic diagram of the measurement of a MOS capacitor using the pulse C-V and stress technique under continuous γ-ray exposure in the ionizing radiation probe station system. A pulse C-V and stress measurement system is developed from a pulse C-V measurement system, an Agilent E3647A DC power

supply and a relay. As indicated in Fig. 3-2-5 (b), a trapezoidal pulse signal and a stress voltage (V_g) are alternately applied to the gate dielectrics. When the system is set to the "stress mode", the DC power supply will be switched by a relay to apply a continuous stress voltage to the MOS capacitor. Otherwise, the system is switched to the "test mode" and the device is connected to the pulse C-V system to perform pulse C-V measurement.

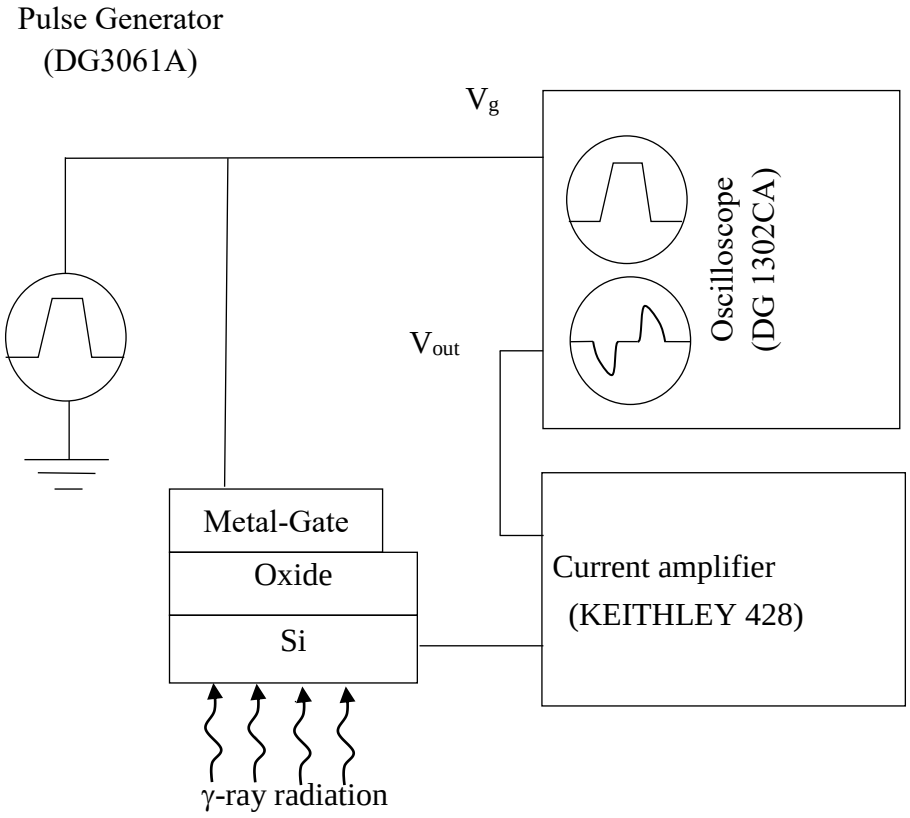
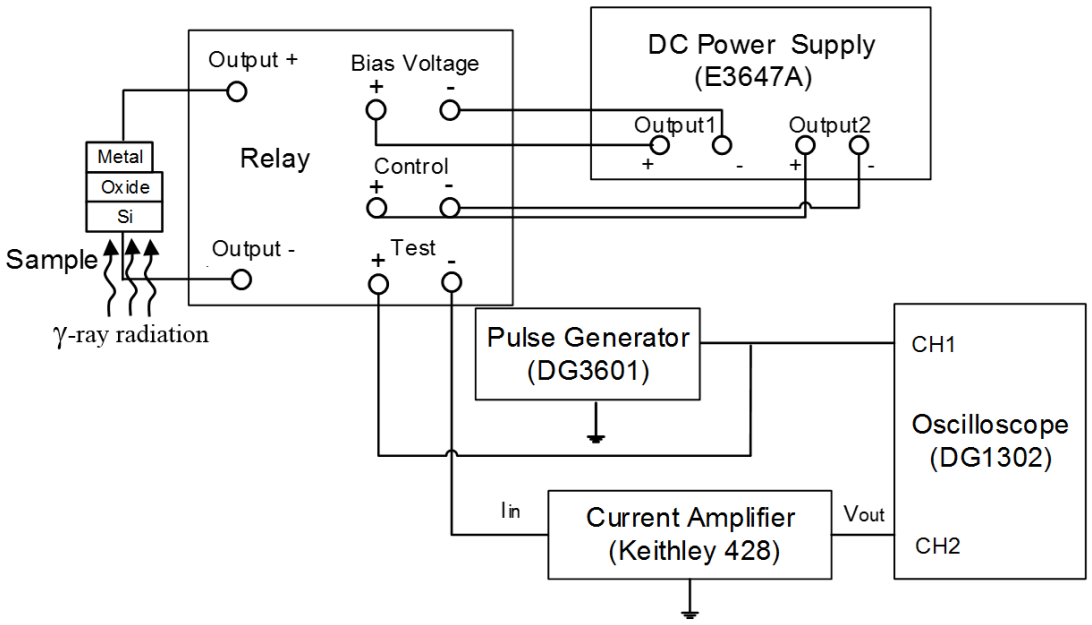
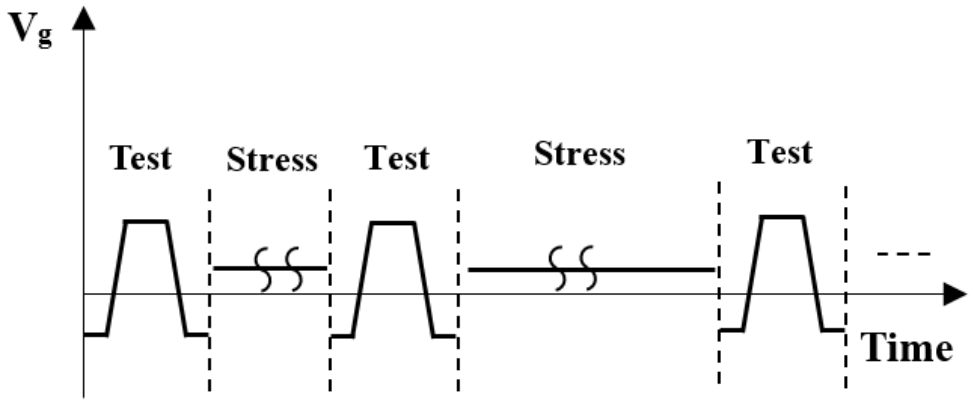


Figure 3-2-4. Schematic diagram of the measurement set-up for a MOS capacitor using the pulse C-V technique under continuous γ-ray exposure in the ionizing radiation probe station system.

The waveform of the applied gate pulse (V_g) and amplified output pulse (V_{out}) for pulse CV technique are shown in Fig. 3-2-6 (a), a trapezoidal pulse signal V_g is applied to the gate of the MOS capacitor with an amplitude of 4 V, an offset voltage V_{offset} of 0



(a)



(b)

Figure 3-2-5. (a) Schematic diagram of the measurement set-up for a MOS capacitor using the pulse C-V and stress technique under continuous γ-ray exposure in the ionizing radiation probe station system. (b) Graph of the gate voltage for the pulse C-V test and stress voltage versus time characteristics of the pulse C-V and stress technique.

V and an amplification factor "A" of 5. The gate waveform voltage was ramped up from -2 V to +2 V with an edge time of t_r and kept at +2 V for a time of t_w-t_r, then turned back to -2 V with the same edge time. The pulse magnitude is from -2 V to +2 V which

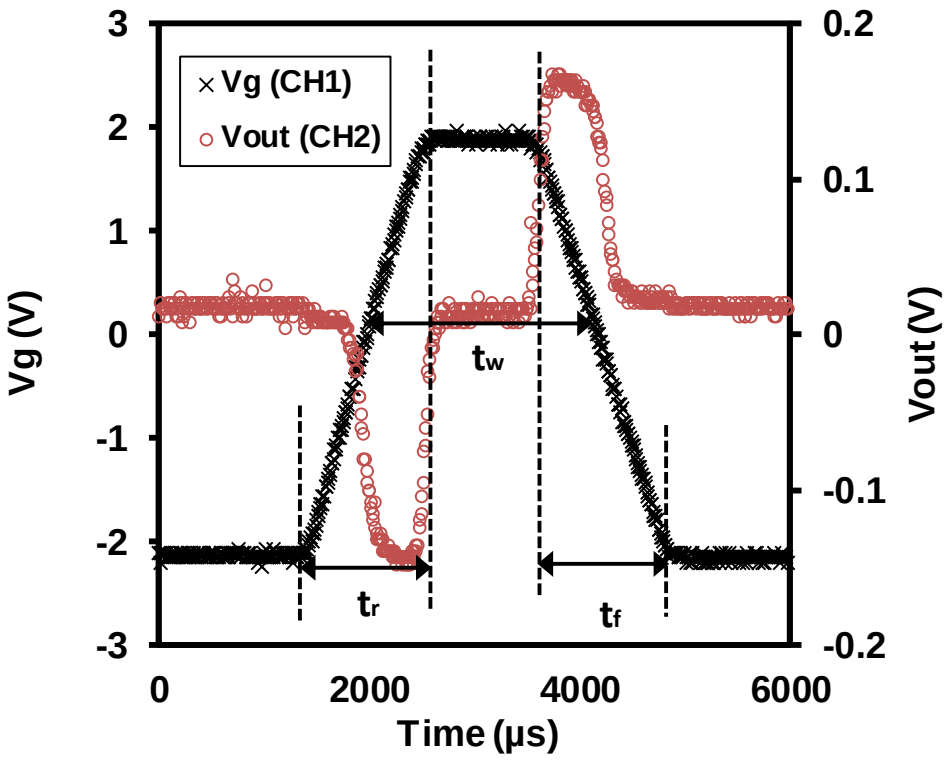
is same to the applied gate voltage range of conventional C-V measurements. The pulse width of t_w was also indicated in Fig. 3-2-6 (a). In the conventional C-V measurements, the edge time is 10 s and the peak voltage duration (t_w-t_r) is 400 ms. With regard to pulse C-V measurements, the edge time can be set to no less than 300 μs. The range of the edge time of the applied pulse waveform for the pulse C-V measurement is from 300 μs to 1000 μs due to the limitation of the function generator. Moreover, the range of the peak time of the applied pulse waveform for the pulse C-V measurement is from 100 μs to 3000 μs.

As discussed before, the trapped charges in oxide can be compensated in a few milliseconds during the measurements. In order to characterize the actual density of trapped charges, the edge time and the peak time are normally set to be as short as possible. However, the peak time is expected to significantly affect the loop width between ramped up and down C-V curves. During the biased irradiation measurements, the time of biased irradiation in the experiment is much longer than the pulse width time. It is suggested that the effect of the peak voltage time (t_w-t_r) on the concentration of net positive oxide trapped charges is negligible. The details of the effect of test time (t_r and t_f) and peak time (t_w-t_r) on pulse C-V measurements and radiation response is discussed in Section 4.3.

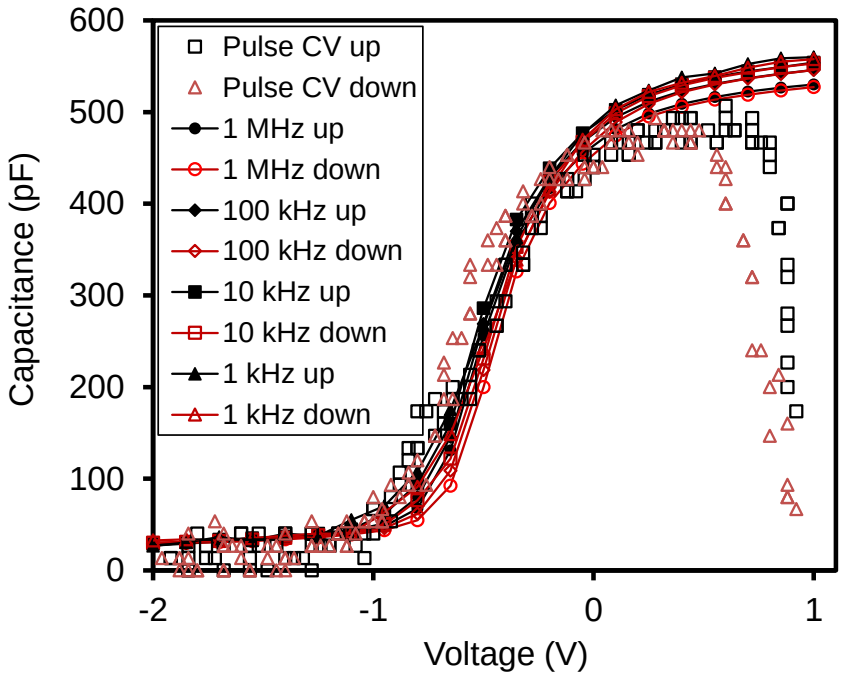
The comparison of C-V curves of the MOS capacitors with HfO_2 dielectrics obtained using the conventional C-V technique and the pulse C-V technique is presented in Fig. 3-2-6 (b). Since the accuracy of the KEITHLEY 428 current amplifier

is up to 1 mA, the accuracy of the amplified V_{out} signals is up to 1 mV. From Eq.3.14, the accuracy of the calculated capacitance is up to 0.1 pF. A fall from the true capacitance value of the pulse C-V measurement is observed within the range of 0.5 V to 1 V. The phenomenon is mainly due to the response time of the oscilloscope and the capacitance charging and discharging issues [34]. In consequence, the capacitance related to the gate voltage from -2 V to 0.5 V is the actual capacitance value of the MOS capacitor. The capacitance measured using the pulse C-V technique is approximately equal to that measured using the conventional C-V technique, while the conventional C-V technique has better stability.

Fig. 3-2-7 is a plot of C-V curves of the MOS capacitors with HfO_2 dielectrics. The C-V curves were obtained at a gate bias of +1 V for a stress duration of 10,000 seconds using the pulse C-V and stress technique. The pulse signal V_g and the +1 V bias voltage were alternately applied to the MOS capacitor. The trapezoidal pulse signal V_g has the same waveform as in Fig. 3-2-6 (a). The C-V curves indicate that there is a very small negative shift for both forward and reverse sweepings. This implies that very few positive oxide-trapped charges and/or interface traps have been generated in the oxide and silicon-oxide interface by the applied positive bias.



(a)



(b)

Figure 3-2-6. (a) Gate and output voltage versus time characteristics of the MOS capacitors with HfO_2 dielectrics obtained by the pulse C-V technique. (b) Comparison of the C-V curves of MOS capacitors with HfO_2 dielectrics measured using conventional C-V and pulse C-V techniques.

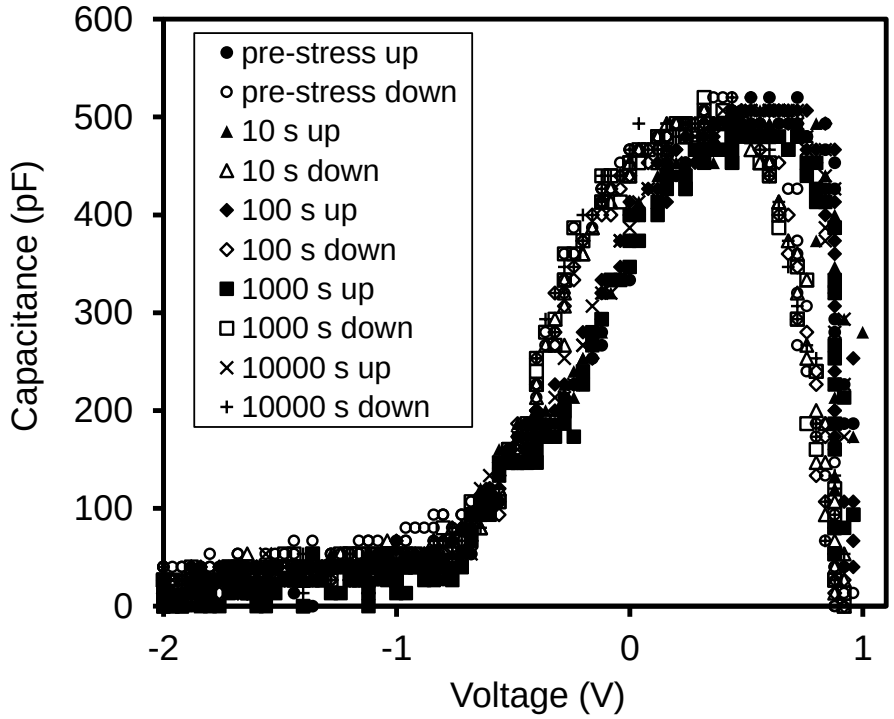
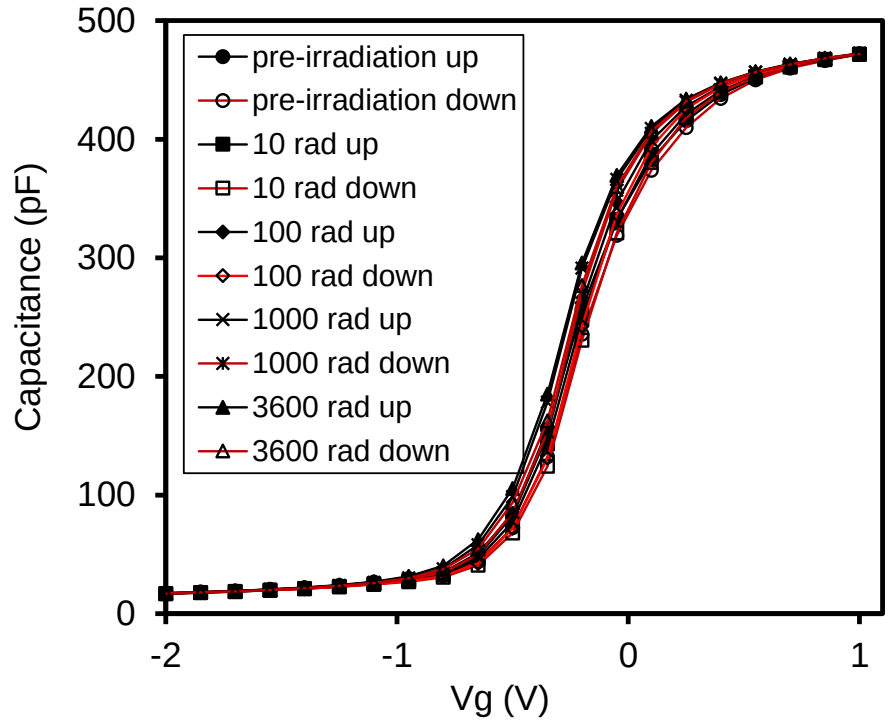


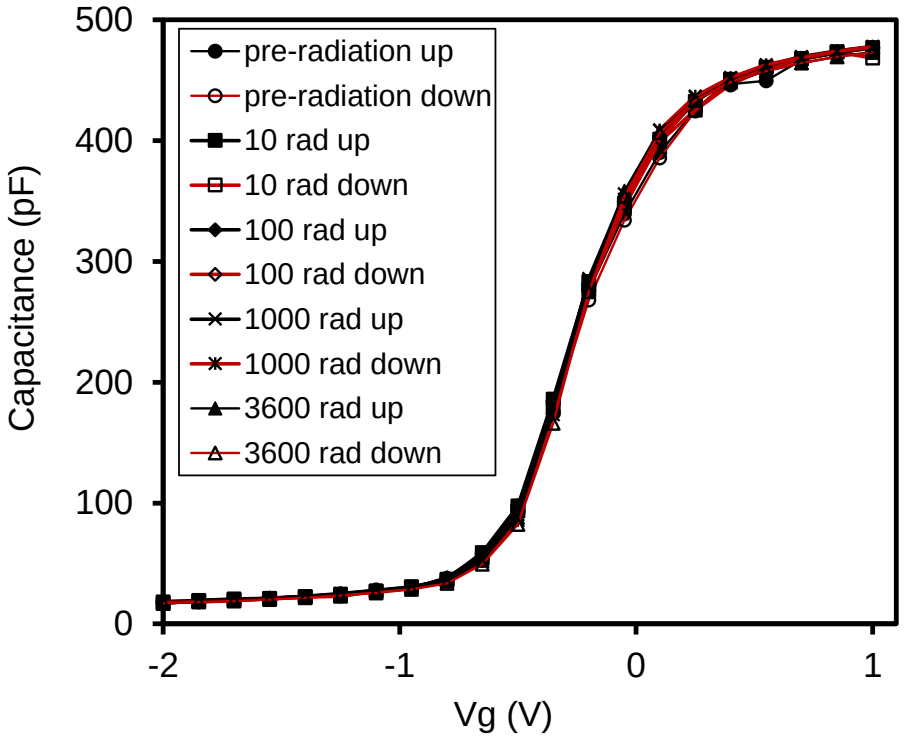
Figure 3-2-7. C-V curves of the MOS capacitors with HfO_2 dielectrics with +1 V bias for a stress duration of 10,000 seconds measured using the pulse C-V and stress technique.

3.3 Verification and Reliability of the Testing Techniques

Primary results of radiation response for capacitors with 20 nm thick HfO_2 dielectrics is determined by the conventional C-V and stress technique and the pulse C-V and stress technique using the ionizing radiation probe station system. The C-V measurement was performed with both forward and reverse swings from -2 V to 1 V at a frequency of 1 MHz. The pulse C-V measurements were carried out at V_{PP} of 4 V, V_{offset} of 0 V and a pulse edge of 400 μs. 1 V or -1 V bias was continuously applied to the gate dielectrics during the irradiation exposure.



(a)



(b)

Figure 3-3-1. C-V curves of a MOS capacitor deposited with 20 nm thick HfO_2 under the γ-ray exposure of 3600 rad measured by the conventional C-V and stress technique at 1 MHz: (a) +1 V bias, (b) -1 V bias.

Figs. 3-3-1 (a) and (b) illustrate a comparison between the pre-radiation and the post-radiation C-V curves for the HfO_2 deposited MOS capacitors which are measured using the conventional C-V and stress technique under 1 V or -1 V bias respectively. After radiation exposure up to 3600 rad, a negative shift up to -100 mV of the gate voltage (V_g) is observed under the positive bias condition as shown in Fig. 3-3-1 (a). Under negative bias, very little positive shift up to 40 mV is observed as shown in Fig. 3-3-1 (b). The results indicate that the HfO_2 sample exhibits more positive oxide trapped charges than negative oxide trapped charges after exposure and a very little concentration of negative oxide trapped charges has been generated to induce the positive shift of V_g [35]. In addition, there is no measurable interface trap built up with ionizing irradiation of these capacitors because the slope of the C-V curves is stabilized [36].

The comparisons between the pre-radiation and the post-radiation C-V curves for the MOS capacitors measured using the pulse C-V and stress technique under 1 V or -1 V bias are shown in Figs. 3-3-2 (a) and (b). A fall from the true capacitance value of the pulse C-V measurement is observed within the range of 1 V to 2 V. As illustrated before, the phenomenon is mainly due to the response time of the oscilloscope and the capacitance charging and discharging issues [34]. In consequence, the range of -2 V to 1 V of the full C-V curves is the actual capacitance value of the capacitor. Under the same total ionizing dose, a negative shift up to -0.96 V and a positive shift up to 0.8 V of the V_g are observed, respectively, with the continuous positive and negative gate potential. The results indicate the same conclusion from C-V measurements that more

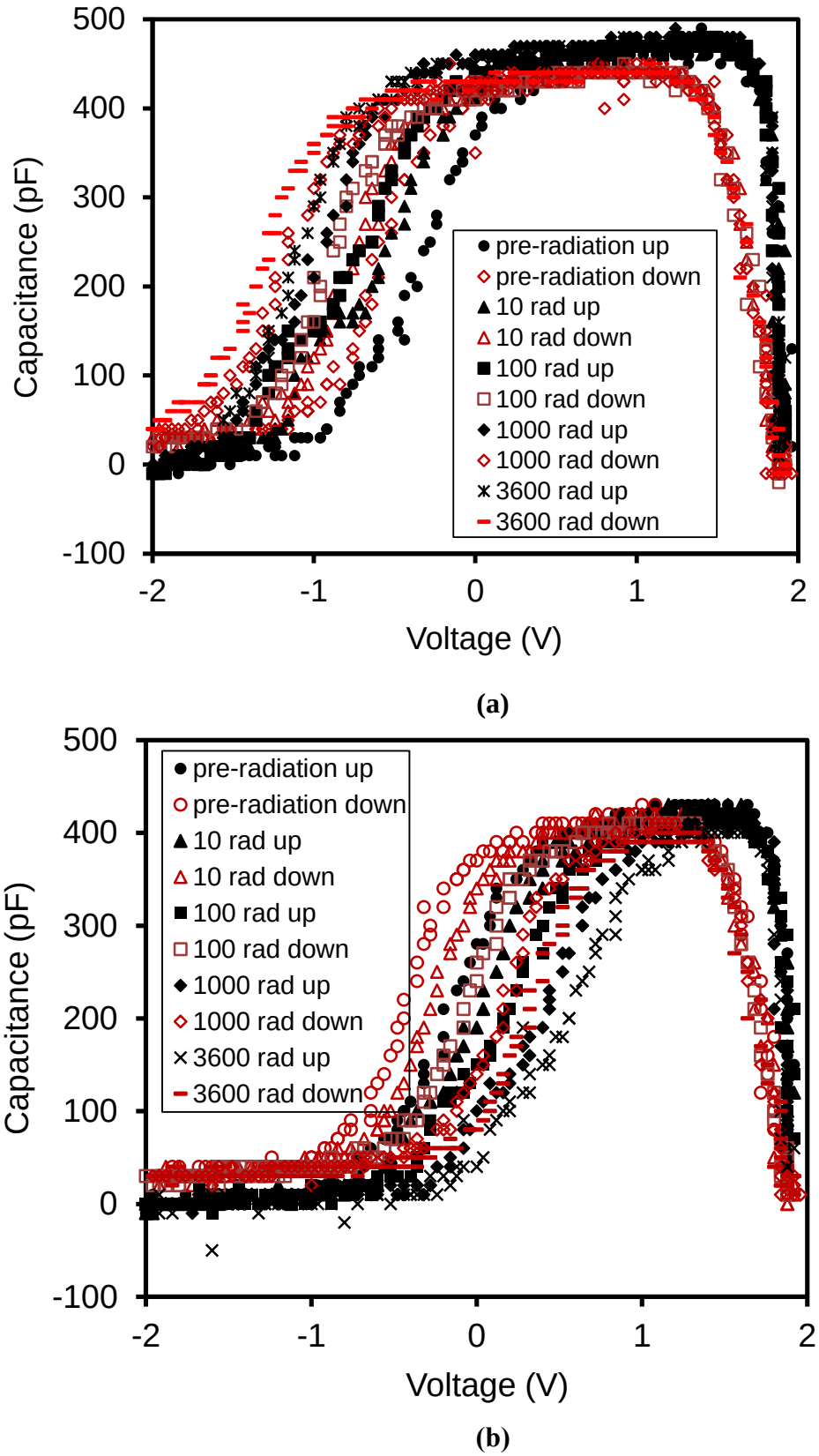


Figure 3-3-2. C-V curves of a MOS capacitor with the HfO_2 gate dielectric under the γ-ray exposure for 3600 rad measured by the pulse C-V and stress technique: (a) +1 V bias, (b) -1 V bias.

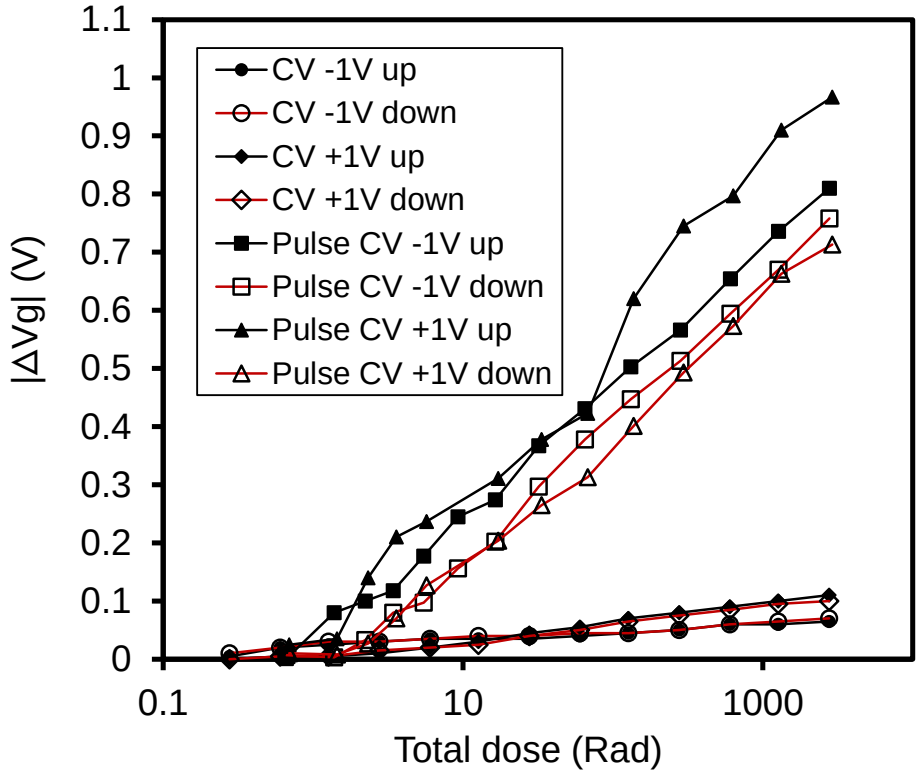


Figure 3-3-3. Comparison of γ-ray induced V_g shift measured using the developed real-time measurement technique and the conventional technique with the HfO_2 gate dielectric of the MOS capacitor irradiated at different total dose levels.

positive oxide trapped charges have been generated under positive bias, whereas a significant increase of V_g shift is observed at both positive and negative bias compared with C-V measurements.

A comparison of the radiation induced V_g shift of the capacitors extracted from the two different techniques under 1 V or -1 V bias is shown in Fig. 3-3-3. There is no significant difference of V_g shift between two different bias conditions measured by the conventional C-V technique. Meanwhile, a large increase of V_g shift up to 1 V is observed as measured using the pulse C-V and stress technique. The results indicate

that the pulse C-V technique evaluates precisely the radiation-induced degradation ofthe gate dielectrics as the gate voltage shift recovery can take place in microseconds. The V_g shift observed under +1 V is larger than that under -1 V bias at forward direction measured by the pulse C-V and stress technique. It is suggested that the HfO_2 oxide layer exhibits more hole traps than electron traps at a total dose of 3600 rad (HfO_2).

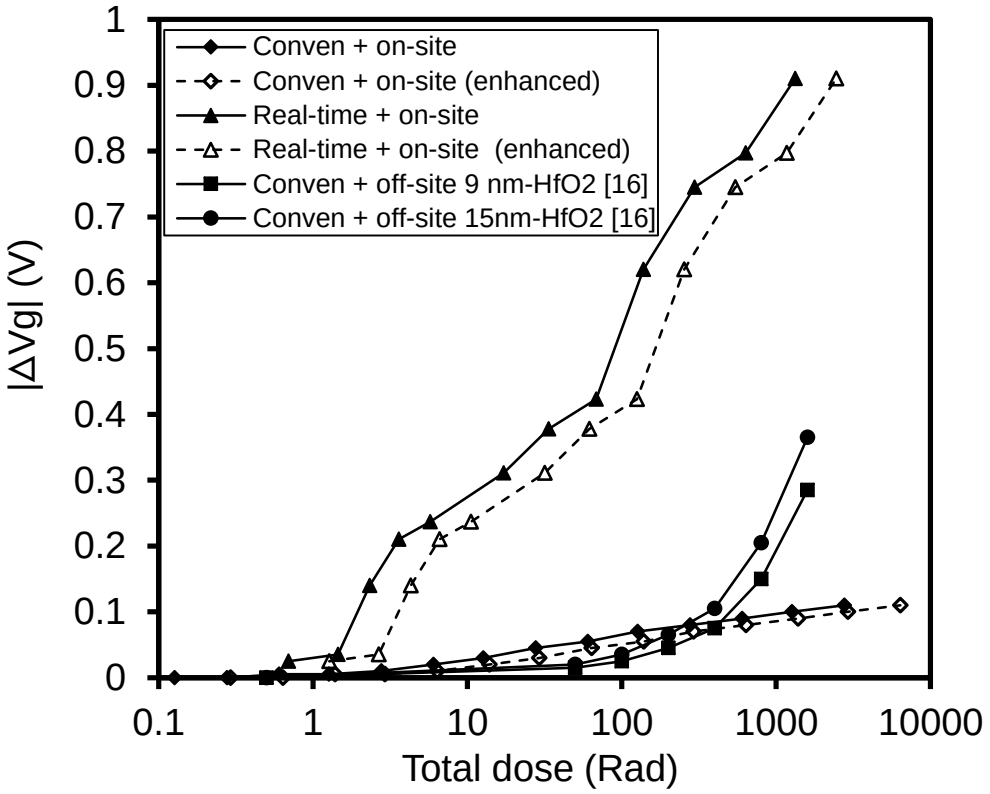


Figure 3-3-4. Comparison of γ-ray induced V_g shift of HfO_2-based capacitors irradiated at low dose rates measured using the developed real-time and on-site measurement system and the conventional measurement method (the data points in solid square and circles are from the literature [3]). The dash lines represent V_g shift of capacitors as a function of the dose rate calculated by taking into account the dose enhancement of HfO_2 effect. The gate biases during the irradiation are 1 V (0.5 MV/cm) for the proposed measurement and 4.5 V (3 MV/cm) for the conventional measurement.

To verify the reliability of the real-time and on-site measurement system, we also show data from the literature in Fig. 3-3-4 [3]. Aluminum-gate capacitors with 9-nm HfO_2 and 15-nm HfO_2 oxide were irradiated in a Co^{60} source at a dose rate of 1.8 rad/s (Si) under a 3 MV/cm positive bias. The sample and irradiation conditions in the literature are similar to those exhibited in this study. The V_g shift of C-V curves in the literature was measured by the conventional C-V and off-site measurement. Comparing with the on-site and real-time system, the conventional measurement in the literature exhibits smaller V_g shift of HfO_2 capacitors at all total dose levels. Meanwhile, the V_g shift measured by the on-site and off-site measurements is similar to that measured by the conventional C-V technique when the total dose is less than 200 rad. The results indicate that the real-time and on-site system evaluates more radiation-induced degradation of the gate dielectrics. After 200 rad irradiation exposure, the V_g shift obtained from the on-site and conventional C-V measurements is smaller than that from the off-site measurement in the literature. One possible explanation for this observation is that the HfO_2-based capacitors in the literature were grown using argon plasma and a sputtering method. As a result, inherent defects are prone to be generated at high sputtering power [37, 38]. The dash lines represent the V_g shift of HfO_2 as a function of total ionizing dose, which was calculated by taking into account the interface dose enhancement of HfO_2.

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Chapter 4: Radiation Response of Hafnium Oxide Dielectrics on Silicon

In order to reduce the gate leakage current while maintaining the same gate capacitance, alternative gate insulator materials with higher dielectric constant (high-*k*) have become the preferred replacement of SiO_2 gate dielectrics [1, 2]. Several high-*k* materials have been under consideration, such as hafnium oxide (HfO_2), zirconium oxide (ZrO_2), yttrium oxide (Y_2O_3), cerium oxide (CeO_2), and their silicates [3-5]. As discussed in Chapter 1, the oxides of hafnium and zirconium dielectrics are most widely employed as they have relatively high dielectric constants of 15-25, relatively large band gap (5.8 eV) and high thermodynamic stability on silicon [6, 7]. In particular, HfO_2 is more widely used than ZrO_2 because it is more stable with silicide formation [8]. At present, advanced microelectronics devices and circuits are used in aerospace engineering, nuclear industry and radiotherapy equipment. These applications are unavoidably exposed to space-like radiation, which has a relatively low radiation dose rate at 10^{-2}-10^{-6} rad(Si)/s [9, 10]. For this reason, it is necessary to understand the low-dose-rate radiation response of HfO_2 based MOS devices. Currently, gamma (γ)-ray radiation sources can be employed in the laboratory to accurately evaluate and predict the radiation response of MOS devices in space-radiation environment [11, 12].

On the other hand, The electrical characteristics of the materials such as flat-band voltage shift, electron trap density and interface trap density have been typically examined by carrying out off-site capacitance-voltage (CV) measurements [13, 14]. As discussed in Chapter 3, the conventional and off-site radiation response measurements may underestimate the degradation of MOS devices. Moreover, in MOSFETs technologies, there is a great interest in understanding the behavior of charge trapping in the oxide during and after pulse voltages [15]. For example, in flash memory technologies, program/erase pulse voltages are applied to the memory devices. It has been reported that the memory device performance is affected by defects in the bulk of oxide during the application of pulse voltages. These defects may lead to device charge trapping or charge leakage [16].

The pulse CV technique is suitable for observing the charge trapping behaviors in relatively short time, which is close to the actual conditions. Furthermore, it has also been found that the defects in HfO_2 induce charging and neutralization behaviors during the applied pulse waveform. These behaviors affect the threshold voltage V_{th} instability of MOSFETs or even lead to device degradation [17]. Therefore, to gain a better understanding of these defects, the pulse CV technique is developed to measure the complete CV characteristic of MOS capacitors in a relatively short time. It reduces the impact of charge trapping on the measurement results, as opposed to the conventional CV technique. As a consequence, our group has developed a novel radiation response testing system, which is capable of estimating the radiation response of MOS devices whilst the devices are continuously irradiated by γ-rays. The related electrical

characterization measurements can be completed in a few milliseconds. The principles and reliability of the system have been reported in Chapter 3. Using this novel testing technique, the degradation of devices can be precisely detected as very few radiation-induced oxide-trapped charges are compensated by bias-induced charges within the complete measurement cycle.

Despite the extent of ongoing research into the radiation response of high-k dielectrics, little work has been done on the fast charge trapping characteristics and long-term reliability of hafnium oxide under continuous low-dose-rate γ-rays exposure. In chapter 4, the mechanism of total ionizing dose radiation effect on HfO_2 dielectric thin films have been studied. The radiation response of HfO_2 gate dielectrics is evaluated by the pulse CV and on-site technique and compared to that extracted from conventional measurements. To further verify the radiation response of HfO_2 gate dielectrics obtained by the pulse technique, MOS capacitors with a silicon dioxide dielectric were also fabricated and tested. More radiation-induced oxide trapped charges were observed in both HfO_2 and SiO_2 dielectrics, via the proposed measurements. One possible explanation is that the fast characterization of pulse CV measurements induces less compensation of the trapped charges in HfO_2.

4.1 Biased Irradiation Effects of the MOS Capacitors

Al-HfO_2/SiO_2–Si MOS capacitors were employed in this study, where the gate dielectric was formed by atomic layer deposition with 24 nm gate-oxide thickness. The

physical thicknesses of SiO_2 interfacial layer was 1.8 nm. The reference SiO_2 thin films were grown in dry O_2 1000ºC to a thickness of 19 nm. The details related to the device information was presented in Chapter 2.

During the biased irradiation, the pulse CV or conventional CV measurements were employed to investigate the charge trapping mechanism of HfO_2 film at each total dose level. The stress voltage and the sweeping voltage are periodically applied to the MOS device during the biased irradiation tests. Conventional CV measurements were carried

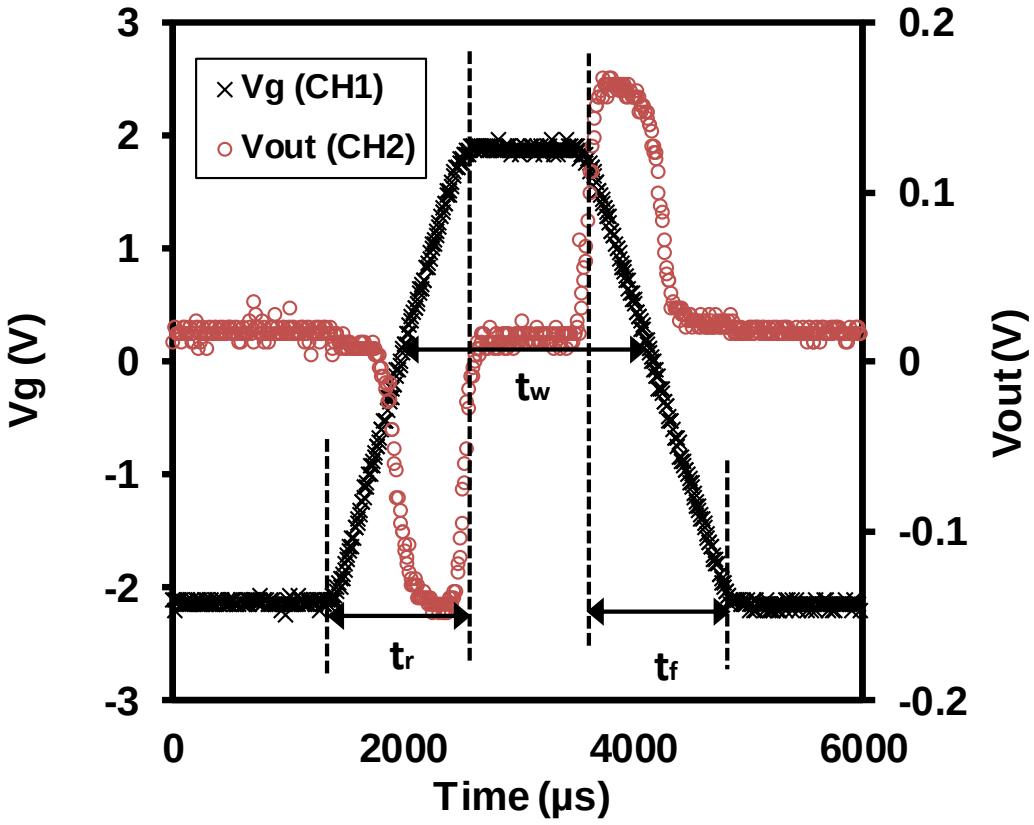


Figure 4-1-1. Voltage versus time characteristics of the pulse CV technique. An input pulse waveform (CH1) was applied to the gate of the HfO2 capacitor and an amplified output pulse waveform (CH2) was extracted. The input waveform was ramped up from -2 V to +2 V in an edge time of tr and kept for (t_w-t_r), then turned back to -2 V in the same edge time. The pulse width was indicated as t_w.

out at a frequency of 1 MHz. The waveform of the applied gate pulse (CH1) and the amplified output pulse (CH2) for pulse CV technique are shown in Fig. 4-1-1. The gate waveform voltage was ramped up from -2 V to +2 V with an edge time of t_r and kept at +2 V for a time of t_w-t_r, then turned back to -2 V with the same edge time. The pulse width of t_w was also indicated in Fig. 4-1-1. In the conventional CV measurements, the edge time is 10 s and the peak voltage duration (t_w-t_r) is 400 ms. Bias-induced degradation was also measured without irradiation at the same irradiation time and biases. All biased irradiation and electrical measurements were performed at room temperature.

Fig. 4-1-2 shows the CV curves extracted from pulse and conventional CV measurements before irradiation exposure. V_g was ramped up and turned back with an edge time of 900 μs with a pulse width of 1300 μs. The CV curves extracted from pulse technique overlap the results of high-frequency conventional CV data. The good agreement in the CV curves indicates that the two techniques measure the same pre-irradiation flat-band voltage, which provides a definite reference point for further investigation of radiation-induced oxide charge trapping. When V_g was ramped down followed by the rising edge in a short time, a small hysteresis between the two extracted CV curves was observed to form a "loop width" as shown in the inset of Fig. 4-1-2. Zhao *et al*. [18, 19] have reported that the loop width originates from part of the charges in HfO_2 dielectrics which can repeatedly be neutralized and recharged by charge injection from the substrate. It was also suggested that when the pulse width or stress time is longer than 1 s, the contribution of these cyclic charges to the ΔV_{FB} is negligible.

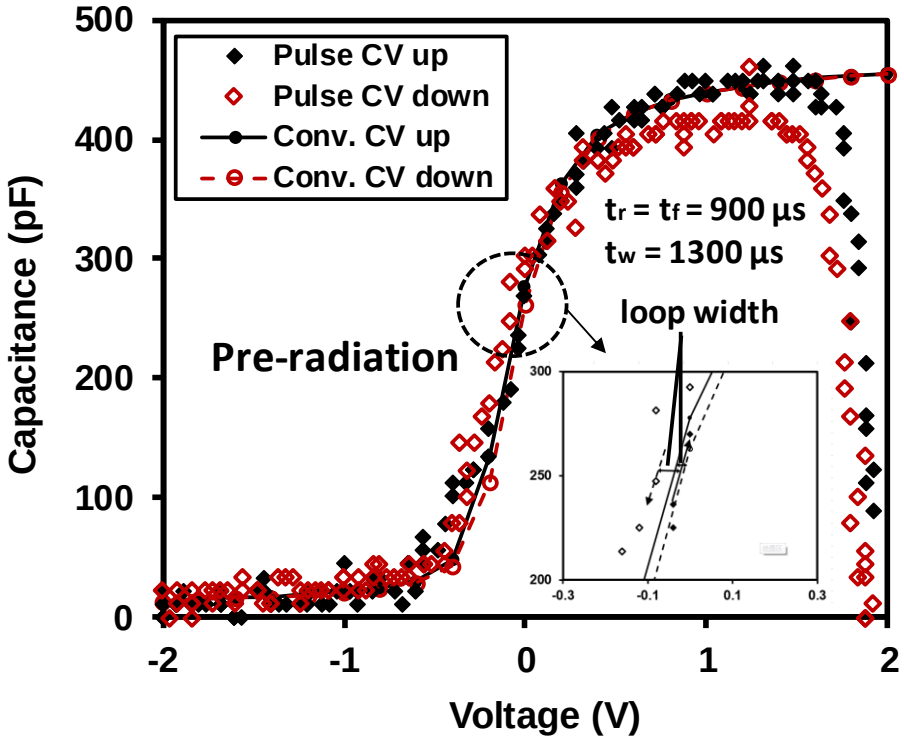


Figure 4-1-2. CV characteristics of the HfO_2/SiO_2-Si capacitor without irradiation exposure. The rising/falling edge time of gate pulse was 900 μs, and the pulse width was 1300 μs. The close similarity in the CV curves indicates that the same pre-irradiation flat-band voltage can be extracted from the two techniques and it provides a solid foundation for further investigation of radiation-induced oxide charge trapping. The corresponding loop width of the CV curves is shown in the inset.

The sensitivity of the loop width to biased irradiation is investigated in the following part by performing long-term pulse CV measurements.

To assess the radiation-induced charge trapping in HfO_2 dielectrics, we use both the high-frequency conventional CV and pulse CV measurements. Fig. 4-1-3 illustrates representative CV curves before and after radiation exposure of 1.1, 10.5, 15.2, and 45.5 krad (HfO_2) respectively with the electric field of 0.5 MV/cm measured by the conventional CV technique. After total dose up to 45.5 krad (HfO_2), it was observed

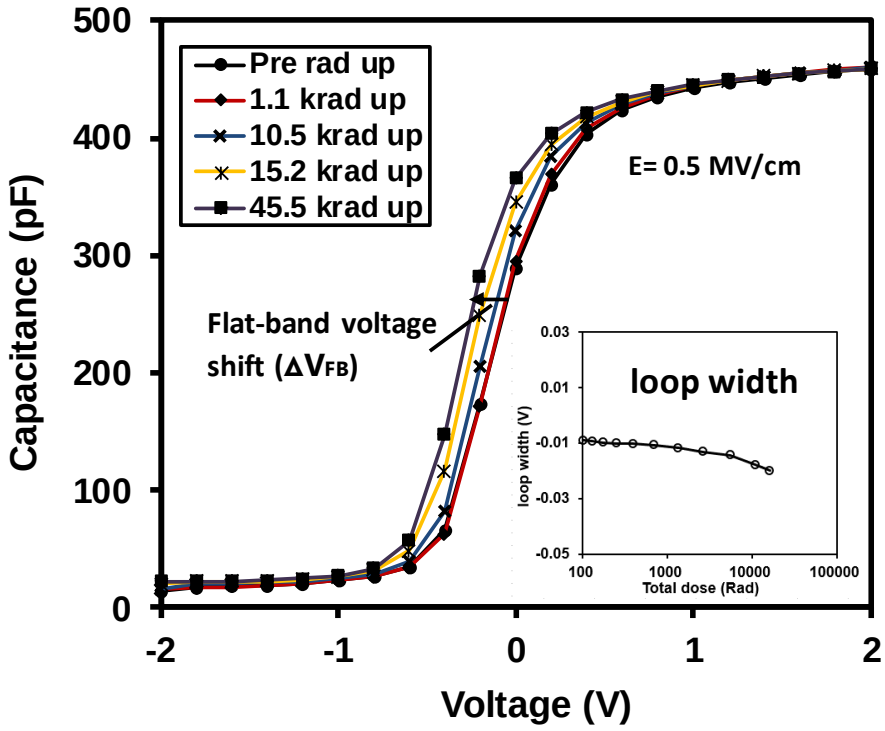


Figure 4-1-3. HfO_2/SiO_2-Si capacitor was irradiated with 662 keV γ-rays at a dose rate of 0.116 rad (HfO_2)/s and biased at an electric field of 0.5 MV/cm during the irradiation. The radiation response of the device was dominated by the flat-band voltage shift (ΔV_{FB}) as indicated, which was extracted from conventional CV measurement. The loop width versus the total dose of HfO_2/SiO_2 thin films is shown in the inset.

that the CV curves presented a negative ΔV_{FB} up to -0.15 V. Since the distribution of oxide trapped charges in the HfO_2/SiO_2 is not known, the trapped charges in the HfO_2 and SiO_2 layers can be considered as equivalent charges projected to the interface of HfO_2/SiO_2 and SiO_2/Si with effective charge densities of Q_{ox} and Q_{in}, respectively. As a result, the ΔV_{FB} due to the oxide trapped charges is calculated by Eq. 4.1:

$$\Delta V_{FB} = -qA\left(\frac{Q_{ox}}{C_{ox}} + \frac{Q_{in}}{C_{in}}\right) \qquad (4.1)$$

where A is the area of the capacitor; $-q$ is the electronic charge; C_{ox} and C_{in} are the

capacitances of HfO_2 and SiO_2 [20, 21]. Analysis of the result shows that the increase in the negative ΔV_{FB} consists of the enhancement of net positive oxide trapping density in HfO_2 and interfacial layers during irradiation. We tentatively attribute the hysteresis to the generation of net positive oxide trapped charges in HfO_2 because it is clear that the thickness of interfacial layer is relatively small (1.8 nm) [22]. Nevertheless, it is conceivable that the positive oxide trapping density in SiO_2 layer is high enough to affect the ΔV_{FB}. However, the needed amount of trapping is in contrast with the typical radiation-induced oxide trap-charge density in SiO_2 found previously [23].

Effective interface trapping efficiencies were calculated using the method of Felix *et al* [24]. It is also suggested that in all cases, there is no discernible interface trap build-up at both HfO_2/SiO_2 and SiO_2/Si interfaces with positive biased irradiation. The inset of Fig. 4-1-3 indicates the loop width versus the total dose of irradiated devices. It clearly shows that the loop width observed by conventional CV measurements is almost insensitive to the radiation exposure. As described earlier, the result in the inset of Fig. 4-1-3 supports the conclusion that the loop width originates from the cyclic charges in dielectrics and these cyclic charges can only be evaluated in a relatively short time.

To further determine the radiation response of HfO_2 dielectrics, irradiation pulse CV measurements are performed on the HfO_2/SiO_2-Si capacitor with the same electric field compared with conventional evaluation as indicated in Fig. 4-1-4. The rising/ falling edge time of gate pulse was 900 μs and the pulse width was 1300 μs in all cases.

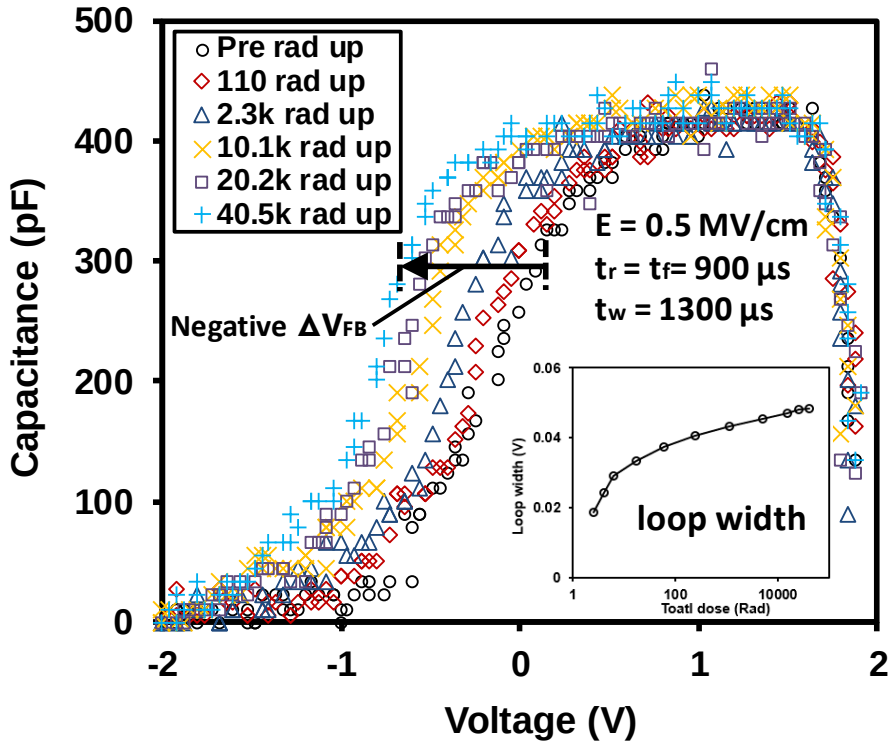


Figure 4-1-4. Pulse CV measurements from an irradiated HfO_2/SiO_2-Si capacitor with an electric field of 0.5 MV/cm applied to the gate. The rising/ falling edge time of gate pulse was 900 µs, and the pulse width was 1300 µs. A very large, -0.67 V, negative ΔV_{FB} was observed in the CV curves at total dose of 40.5 krad (HfO_2), which indicated a large concentration of positive charges being generated in the oxide. The inset shows the loop width versus the total dose, suggesting no significant variations of loop width.

A very large, -0.67 V, negative ΔV_{FB} is observed after a total dose of 40.5 krad (HfO_2). The result in Fig. 4-1-4 indicates that a large concentration of net positive charges was generated in the HfO_2/SiO_2 oxide layer. As mentioned above, it is suggested that the positive oxide trapped charges is primarily generated in HfO_2 dielectric layer, since no significant oxide trapping is expected in the ultrathin SiO_2[22]. The inset of Fig. 4-1-4 shows the loop width versus the total dose of the irradiated devices as observed by pulse

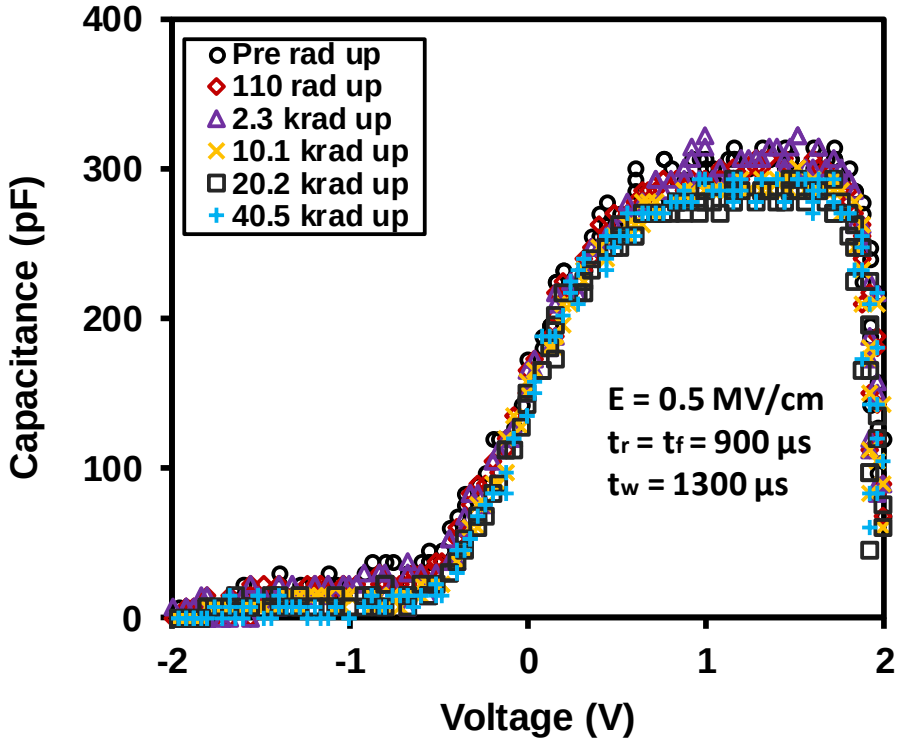


Figure 4-1-5. Pulse CV measurements of an HfO_2/SiO_2-Si capacitor under electric field of 0.5 MV/cm without irradiation exposure. The edge time and pulse width of the measurements were identical with the measurements in Fig. 4-1-4. Positive ΔV_{FB} up to 66 mV was observed at total dose of 40.5 krad (HfO_2).

CV measurements. The small increase in loop width is likely due to the fact that more bias-induced electrons are injected into HfO_2 to neutralize the positive cyclic charges which are located in shallow traps in the HfO_2 [18]. It is also suggested that the generation of these positive cyclic charges is consistent with some radiation-induced holes which are generated and trapped in HfO_2 during the positive biased irradiation.

In order to separate the bias-instability and radiation-caused shifts, the ΔV_{FB} of the devices under positive bias without radiation exposure was also observed by using the pulse technique. The edge time and pulse width of the measurements were identical with the measurements under irradiation exposure. Positive electric field on the device

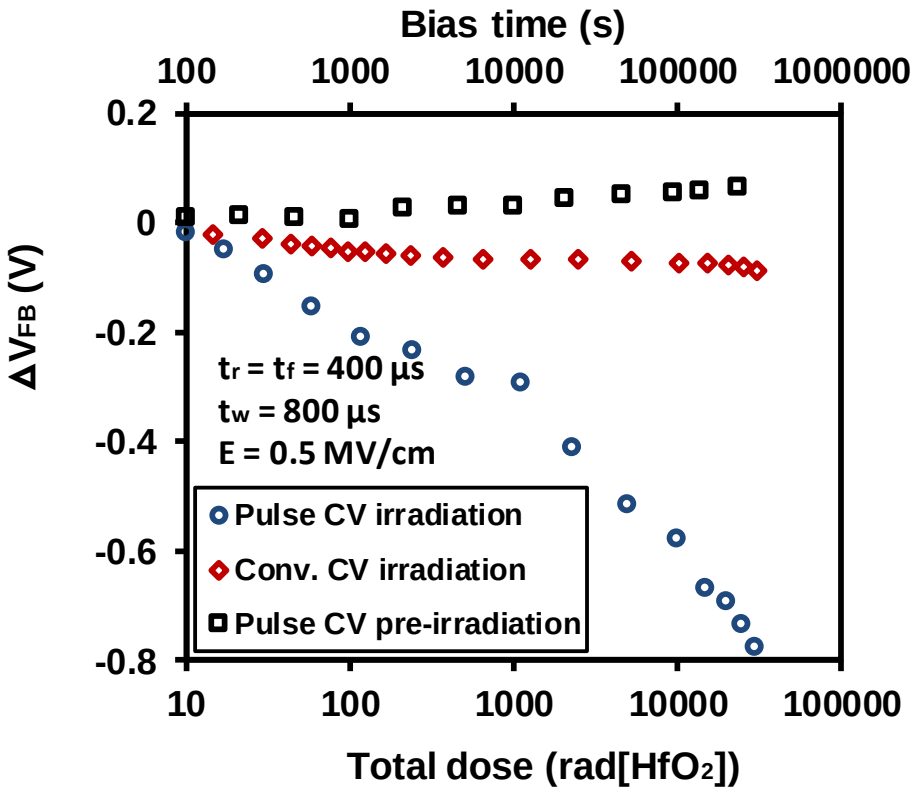


Figure 4-1-6. Comparison of ΔV_{FB} for the HfO_2/SiO_2-Si capacitors measured by pulse CV and conventional CV technique, in which the pulse CV measurements were carried out under irradiation up to 40.5 krad (HfO_2) and without irradiation. In all cases, the electric field applied to the gate was 0.5 MV/cm. The rising/falling edge time of the gate pulse was 400 μs, and the pulse width was 800 μs. A large density of positive radiation-induced charges was extracted by pulse CV under biased irradiation.

for more than 105 hours without irradiation results in a maximum ΔV_{FB} of 66 mV as shown in Fig. 4-1-5. The small hysteresis is attributed to the bias-induced electrons which are tunneling from the silicon substrate and are trapped into HfO_2 with the energy level below the bottom edge of the Si conduction band [19, 25, 26]. The result indicates that only very few bias-induced electrons which exist in the deeper energy level can be extracted from the pulse technique

Fig. 4-1-6 summarizes the flat-band voltage shifts of the stacked HfO_2/SiO_2-Si capacitors, which are extracted from pulse and conventional CV measurements at each total dose level with 1 V gate bias. The rising and falling edge times of the gate pulse were 400 μs and the pulse width was 800 μs. The time scale of the top axis is matched to the bias time when performing pulse CV measurements without irradiation. The devices exposed to gamma radiation show a negative ΔV_{FB} of up to -793 mV and -80 mV, respectively from pulse and conventional CV measurements.

The differences between the ΔV_{FB} with and without irradiation clarify the effects of gamma radiation on HfO_2 film. Therefore, the negative ΔV_{FB} in Fig. 4-1-6 could be due to radiation-induced positive charge trapping and compensation of bias-induced electrons in HfO_2 layers. Analysis of these data shows that a large concentration of radiation-induced positive oxide trapped charges is generated in the oxide. However, the conventional measurement can only extract very few net positive charges. One possible explanation is that the recovery of ΔV_{FB} observed by conventional method may be due to the trapping process of the biased-induced tunneling electrons in the oxide during the long duration of the measurement. Conversely, a large density of the negative oxide trapped charges would be de-trapped with less trapping occurring before the completion of pulse CV measurement. This also explains the relatively small hysteresis observed in pulse CV measurements without irradiation. In this case, a large concentration of the bias-induced negative oxide trapped charges were de-trapped and only the charges trapped in deep energy levels were extracted [19, 27, 28].

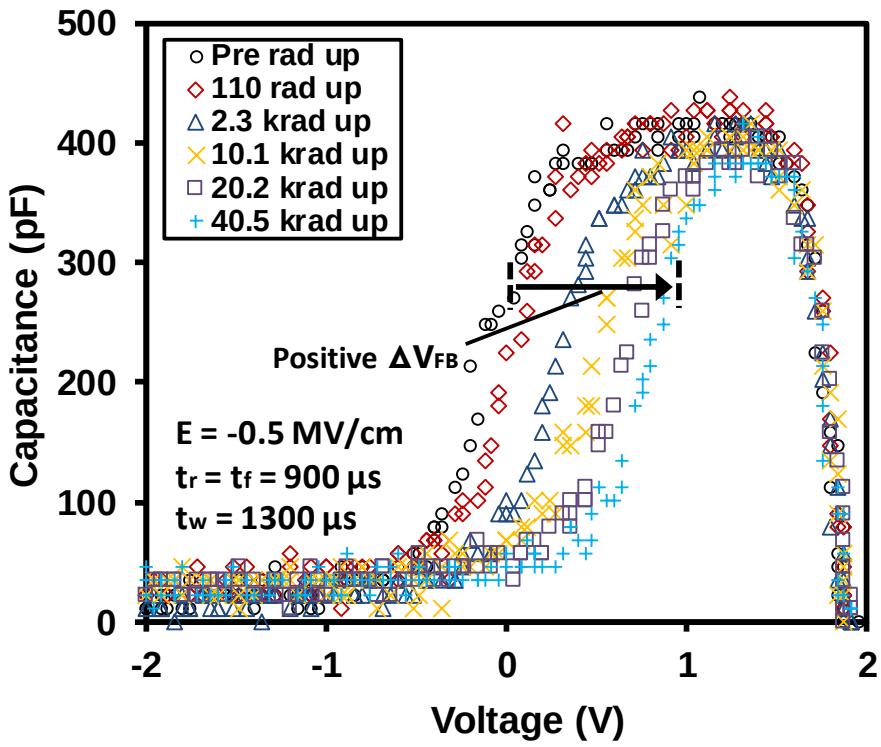


Figure 4-1-7. CV plot of the HfO_2/SiO_2-Si capacitor irradiated at different doses with an electric field of -0.5 MV/cm applied to the gate. The measurements were carried out by pulse CV technique. The rising/ falling edge time of gate pulse was 900 µs, and the pulse width was 1300 µs. Positive flat-band voltage shifts up to 0.89 V were observed after irradiation to 40.5 krad (HfO_2).

Fig. 4-1-7 is a plot of representative CV curves of a HfO_2/SiO_2-Si capacitor obtained from pulse CV measurements. The capacitor was irradiated at total doses of 0.11, 10.5, 15.2, and 45.5 krad (HfO_2) with a gate bias of -1 V. The rising/ falling edge time of gate pulse was identical with the same conditions as in the positive biased irradiation experiment in Fig. 4-1-4. The results in Fig. 4-1-7 indicate that a large concentration of net negative charges has been generated in the HfO_2 layer under negative biased irradiation. A positive ΔV_{FB} of 0.99 V is comparable to the negative ΔV_{FB} observed in Fig. 4-1-4 in terms of the magnitude for the same total dose. This confirms the existence of a large density of electron traps in HfO_2 as suggested in the

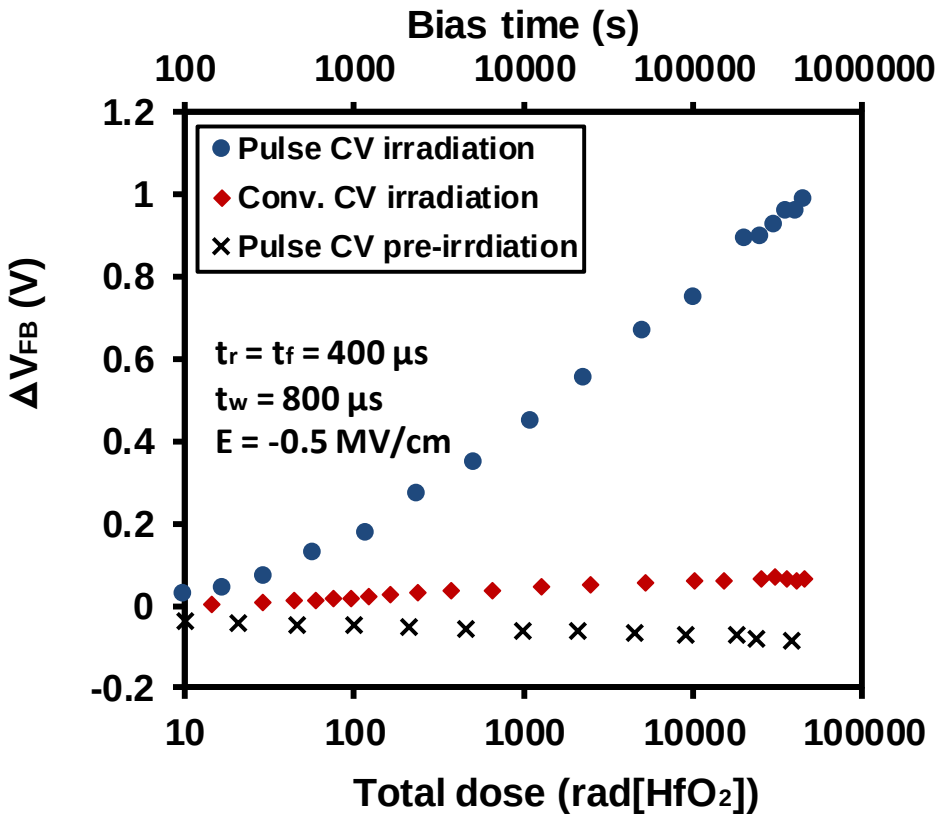


Figure 4-1-8. Comparison of ΔV_{FB} for the HfO_2/SiO_2-Si capacitors measured by the pulse CV and conventional CV techniques, in which the pulse CV measurements were carried out under irradiation up to 40.5 krad (HfO_2) and without irradiation. In all cases, the electric field applied to the gate was -0.5 MV/cm. The rising/falling edge time of the gate pulse was 400 µs, and the pulse width was 800 µs. The time scale on the top axis is matched to the bias time when performing the pulse CV measurements without irradiation.

explanation for the recovery of V_{FB} in conventional positive biased irradiation experiment. The bidirectional flat-band voltage shifts observed under opposite-biased irradiation indicate that both positive and negative trapped charges dominate the radiation response of the HfO_2/SiO_2 capacitors [29].

To further verify that the bias-induced charge trapping and de-trapping in HfO_2 are

responsible for the recovery of radiation-induced ΔV_{FB} by using conventional evaluation, we examine the radiation response for the HfO_2/SiO_2 capacitors by using both pulse and conventional CV measurements at -1 V gate bias as shown in Fig. 4-1-8. Similar to positive biased radiation, the pulse CV measurements were carried out with and without irradiation exposure. The applied gate pulse was identical with the conditions in the positive biased irradiation experiment as presented in Fig. 4-1-6. The dark crosses in Fig. 4-1-8 represent the ΔV_{FB} of the capacitors under negative bias without radiation exposure. ΔV_{FB} up to -80 mV was observed in the negative biased device without irradiation. This small negative hysteresis is likely due to the fact that the bias-induced positive charges are tunneling from the silicon substrate and are trapped into HfO_2 with the energy level above the top edge of the Si valence band [18, 30].

After a total dose exposure up to 40.5 krad (HfO_2), we observed positive ΔV_{FB} of 986 mV and 67 mV respectively obtained using the pulse and conventional techniques. The result has a good agreement with the ΔV_{FB} extracted from positive biased irradiation. As mentioned earlier, this ΔV_{FB} is mainly due to the radiation-induced charge trapping and the compensation of bias-induced charges in HfO_2 layers. Similarly, we attribute the recovery of ΔV_{FB} measured by the conventional measurement to the trapping of the bias-induced substrate hole injection (SHI) in HfO_2 oxide during the measurement.

4.2 Physical Mechanism for Biased Irradiation-Induced Charge trapping

To better understand the mechanisms of radiation-induced charge trapping and the compensation of bias-induced charges in HfO_2, Fig. 4-2-1 shows the energy band diagrams of the stacked HfO_2/SiO_2-Si capacitor during positive biased irradiation and CV measurements. Under the +1 V biased irradiation as shown in Fig. 4-2-1 (a), radiation-induced positive charges will transport toward HfO_2/SiO_2 interface via defects and then trapped in the bulk of HfO_2 to form positive oxide trapped charges, while most of the radiation-induced electrons are swept out of oxide to the gate electrode [31]. As the SiO_2 layer is very thin, the accumulation of radiation-induced charges at the interface due to the barrier of HfO_2/SiO_2 is negligible [44]. Meanwhile, the bias-induced electrons tunnel from the Si substrate and are trapped in the HfO_2 as indicated in Fig. 4-2-1 (a). These bias-induced electrons significantly compensate the radiation-induced hole trapping in either shallow and/or deep energy levels generated during positive biased irradiation (see Fig 4-2-1(a)) [32, 38, 39]. As a result, the concentration of net positive charges in HfO_2 is determined by the generation of radiation-induced positive charges and the compensation of bias-induced electrons.

During the ramp-up process of CV measurements, the gate sweeping voltage is ramped up from -2 V to +2 V. Initially at electric field of -2 V, a large concentration of bias-induced electrons, which are generated during positive biased irradiation, are de-trapped and forced out of HfO_2 as illustrated in Fig. 4-2-1 (b). This suggests that a

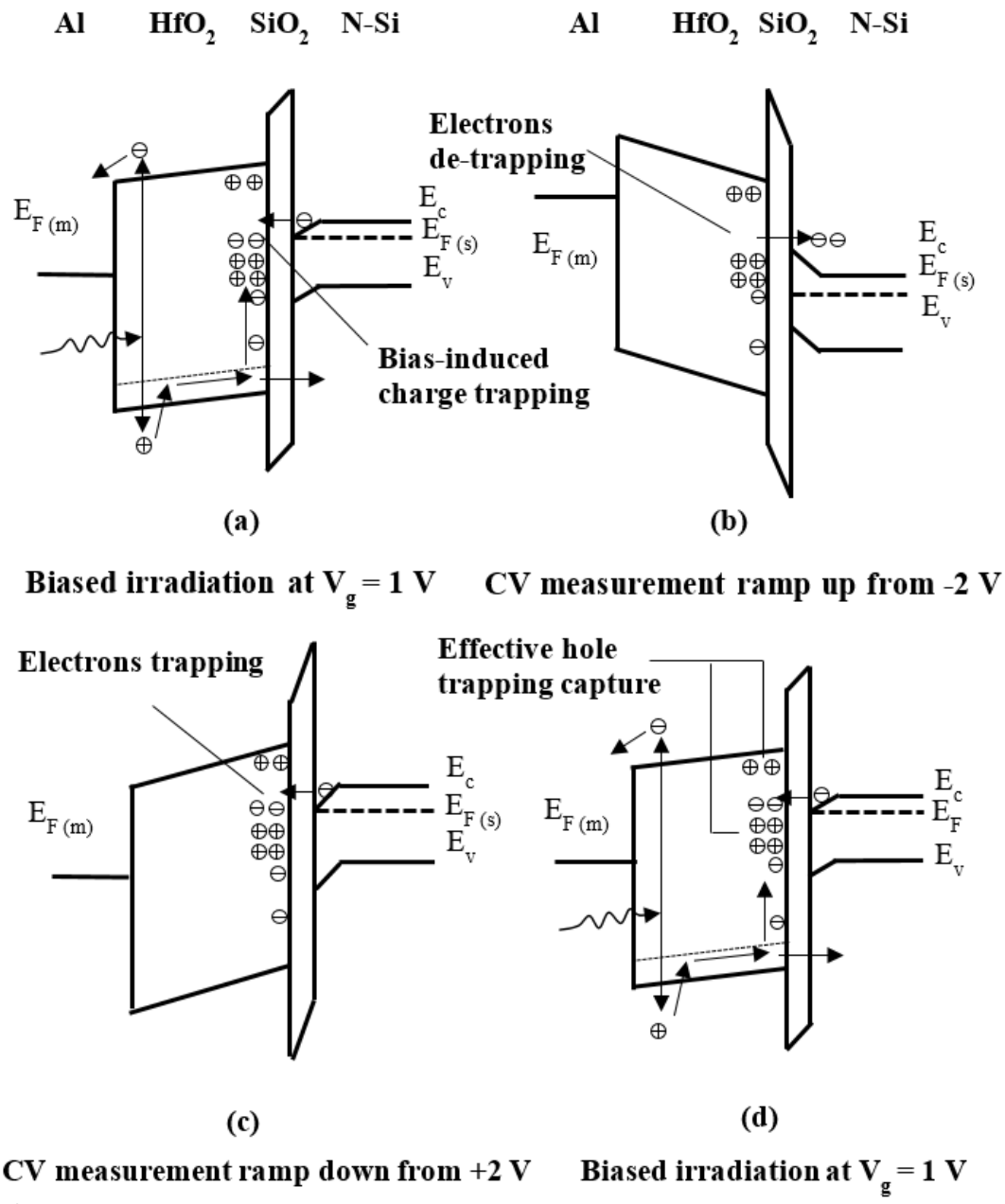


Figure 4-2-1. Energy band diagrams of a HfO_2/SiO_2-Si capacitor during biased irradiation and CV measurements: (a) +1 V biased irradiation. Radiation-induced positive charges transported to HfO_2/SiO_2 interface and trapped in the HfO_2 to induce negative ΔV_{FB}. Meanwhile, electrons were injected from Si and trapped in HfO_2 to compensate holes trapping. (b) CV measurements ramped up from -2 V. Initially, the negative oxide trapped charges were de-trapped and a relatively large negative ΔV_{FB} can be extracted at E = -0.5 MV/cm. Conventional measurements completed the process of ramp up from -2 V to +2 V in a relatively long time, in which de-trapped electrons were tunneling to HfO_2 again inducing strong

recovery of ΔV_{FB}. (c) CV measurements ramped down from +2 V, the de-trapped electrons were tunneling to HfO_2 again. (d) +1 V biased irradiation.

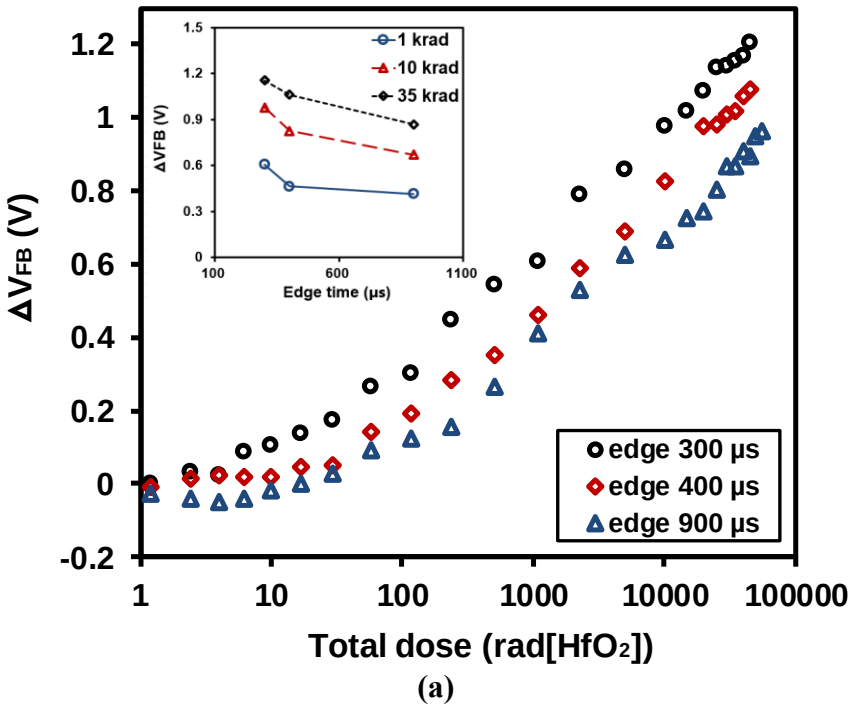
relatively large density of net positive charges can be extracted at this stage. Only very few bias-induced anti-neutralization electrons at deep energy level would affect the density of net positive charges. In other words, a large value of ΔV_{FB} would be also observed at –2 V during the ramp-up process. A similar mechanism was also indicated by Zhou *et al.* [32]. It was reported that the significant densities of dipolar defects were created during irradiation in the gate stacks. During positive bias, electrons compensated the trapped positive charges, while for negative bias, electrons were forced out of oxide. These defects may impact MOS device radiation response significantly. When the gate sweeping voltage is ramped to +2 V, the de-trapped electrons are tunneling back to HfO_2 again to compensate the positive oxide trapped charges as shown in Fig. 4-2-1 (c). This compensation would induce strong recovery of the initial ΔV_{FB} which is observed at V_g = -2 V. Since the ramp-up of the pulse CV measurement completes within 1 ms, the fast characterization will complete the whole measurement process before most of the de-trapped electrons tunnel back to HfO_2 [18].

In general, the pulse CV technique completes an evaluation with very little recovery of ΔV_{FB}. However, the conventional technique completes the process of ramp-up in a relatively long period. Thus, the radiation-induced positive charges will be compensated by the bias-induced electrons during the measurements and these processes will induce the recovery of ΔV_{FB}. As a result, the ΔV_{FB} with strong recovery

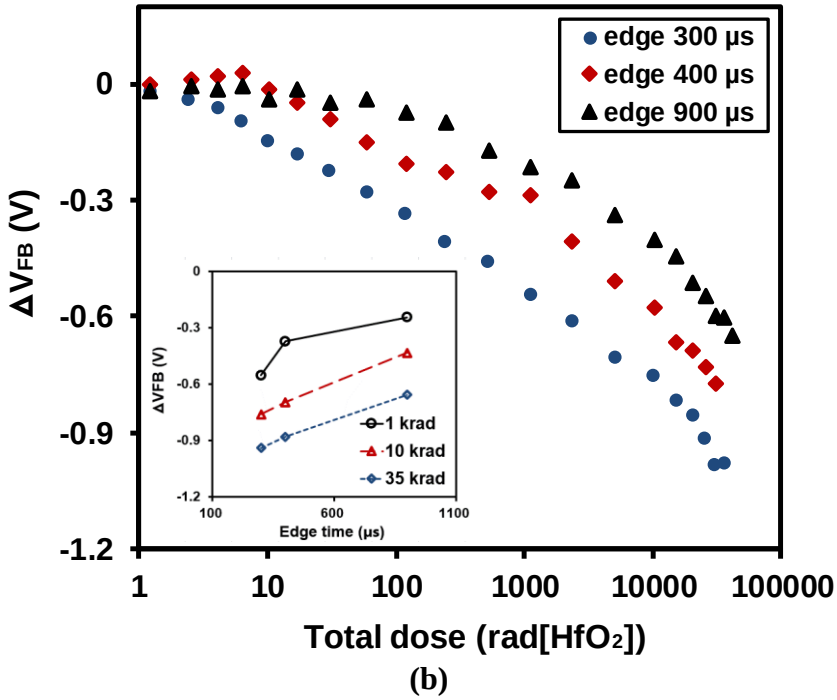
would be extracted by conventional technique. Similarly, the recovery of radiation-induced ΔV_{FB} obtained by the conventional measurement under negative biased irradiation is likely to be due to the compensation of bias-induced positive charges as a result of the relatively long test time.

4.3 Test Time Dependence

The analysis in section 4.2 indicates that increasing the test time leads to less net oxide trapped charges in the oxide. Furthermore, the test time during pulse CV measurements is mainly affected by the edge time (t_r and t_f). In order to observe the significant effect of the test time on the radiation response of the devices, ΔV_{FB} as a function of the total dose measured by pulse CV measurements with various edge time of the gate pulse are illustrated in Fig. 4-3-1. The electric field applied to the gate was -0.5 MV/cm and 0.5 MV/cm as shown in Fig. 4-3-1 (a) and Fig 4-3-1 (b) respectively. The results of Fig. 4-3-1 (a) indicate that the density of net negative charges decreases with the increase of the edge time in a range of 300 μs ~ 900 μs. From the trend of ΔV_{FB} summarized in the inset, we tentatively suggest that the radiation response extracted from pulse CV measurements would be identical to that of the conventional CV measurements if the edge time is large enough. Similarly, the results of Fig. 4-3-1 (b) indicate that the density of net positive charges decreases with the increase of the edge time. It can be concluded that both the positive and negative time-dependent fast charge trapping/de-trapping dominate the radiation response of HfO_2 dielectrics.



(a)



(b)

Figure 4-3-1. ΔV_{FB} as a function of the total dose obtained from pulse CV measurements with different edge time of the gate pulse. The electric fields applied to the gate were (a) -0.5 MV/cm and (b) 0.5 MV/cm. The inset in each figure was a plot of ΔV_{FB} versus the edge time for the HfO_2/SiO_2-Si capacitor at different dose levels. The magnitude of ΔV_{FB} was observed to increase with the decrease of the edge time under both positive and negative bias at all total dose levels.

In addition to edge time, the peak voltage time (t_w-t_r) of the input pulse waveform also affects the test time of CV measurements. The effects of the peak voltage time on the loop width without irradiation have been discussed in our previous work [33]. It was observed that with a longer peak voltage time, the loop width remained at a lower level. The result suggested that the longer peak voltage time leads to more electron charge trapping in oxide. Similarly, in this study, the increase of the peak voltage duration may induce more neutralization of positive cyclic charges. In general, a larger loop width may be extracted with longer peak voltage duration. On the other hand, increasing the pulse width time would also generate more radiation-induced positive charges. However, the time of biased irradiation in the experiment is much longer than the pulse width time. We hence tentatively suggest that the effect of the peak voltage time (t_w-t_r) on the concentration of net positive oxide trapped charges is negligible.

The impact of pulse magnitude on the loop width and flat-band voltage shift is also considered. It has been reported that the pulse magnitude will affect the loop width of CV curves without irradiation as indicated in the previous research [34]. The results showed that the loop width of $LaAlO_3$ was increased with an increase of pulse magnitude. This has been attributed to the positive cyclic charges with deeper energy levels that may exist in the bulk of high-*k* oxide, which can only be neutralized with larger electric field. In this study, it has been indicated that more positive cyclic charges, which are located in shallow traps of HfO_2, are generated during the biased irradiation. These results suggest that increasing the pulse magnitude may lead to more neutralization and recharging of positive cyclic charges with deeper energy levels. As a

result, a higher pulse magnitude would cause a larger loop width during biased irradiation pulse CV measurements. Similar to the loop width, when the pulse magnitude is increased, it is suggested that the bias-induced negative oxide trapped charges with deeper energy levels may be de-trapped during the pulse CV measurements. The stronger de-trapping process denotes the decrease in compensation of the radiation-induced positive charges. Hence, a larger concentration of net positive oxide trapped charges would be extracted, resulting in an increase of the flat-band voltage shift.

There is one more benefit to perform the pulse CV technique for evaluating the biased irradiation response of high-*k* dielectrics. The radiation response obtained from pulse CV measurements is closer to the way devices would behave in actual operating conditions. As indicated in Fig. 3-2-5, the biased irradiation measurements can be divided into two parts: testing and biasing. During both of these two processes, the irradiation exposure is uninterruptedly applied to the devices. The values of the gate voltages remain constant during the biasing processes. While during the testing processes, the gate voltages are swept between the positive and negative polarity. As a consequence, the reversed gate voltages with irradiation would lead to the decrease of net oxide trapped charges in HfO_2. For example, positive charges are trapped in the oxide during the +1 V biased irradiation. During the sense process, the gate voltages are swept from -2 V to +2 V. Negative radiation-induced charges are trapped in the oxide during -2V to 0 V, which induces a recovery of ΔV_{FB}.

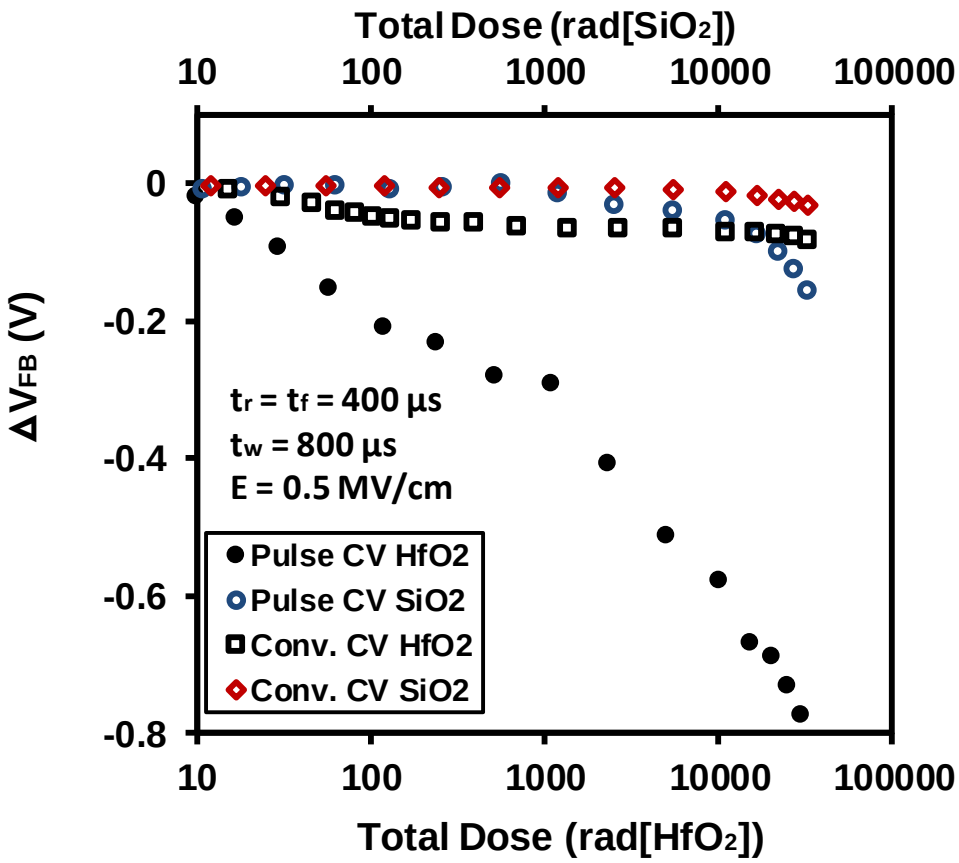


Figure 4-3-2. Comparison of ΔV_{FB} for the SiO_2 and HfO_2 based capacitors measured by the pulse CV and conventional CV techniques, respectively under the irradiation of up to 32.8 krad (SiO_2) and 40.5 krad (HfO_2). In all cases, the electric field applied to the gate was 0.5 MV/cm. The rising/falling edge time of the gate pulse was 400 µs, and the pulse width was 800 µs.

Therefore, a longer test process (i.e. a longer interruption of bias) would cause a stronger recovery of ΔV_{FB}. A conventional CV test normally takes several seconds or even longer. However, a pulse CV test completes the whole measurement process in relatively short time (just 1 millisecond) which allows data extraction of ΔV_{FB} with less recovery. Moreover, in actual operating conditions, an operating MOS circuit will not be interrupted by any test processes. Therefore, the test process is desired to be as short

as possible.

To probe further the radiation response of HfO_2 gate dielectrics evaluated by the pulse technique, MOS capacitors with a silicon dioxide (SiO_2) dielectric were employed. Previous results in the literature demonstrated that the radiation response of SiO_2 was dominated by the positive charge trapping[23]. Hence, only the positive biased irradiation effect on SiO_2 was measured. Fig. 4-3-2 shows the flat-band voltage shifts of the SiO_2-based capacitors, which are extracted from pulse and conventional CV measurements at each total dose level with positive bias. The dose scale of the top axis is matched to the total dose of SiO_2 when performing positive biased irradiation. A total dose of up to 32.8 krad (SiO_2) was applied to the irradiated SiO_2 samples. The devices exposed to gamma radiation show a negative ΔV_{FB} of up to -224 mV and -31 mV from pulse and conventional CV measurements, respectively.

Similar to HfO_2, the negative ΔV_{FB} could be due to radiation-induced positive charge trapping and compensation of bias-induced electrons in SiO_2 layers. The results indicate that the pulse CV technique extracts a lager flat-band voltage shift as compared to the conventional CV technique. As explained above, the recovery of ΔV_{FB} measured by the conventional method may take place due to a large density of biased-induced electrons trapped in the oxide. Conversely, most of these negative oxide-trapped charges would be de-trapped and less trapping occurred before the completion of the pulse CV measurement. As indicated in Fig. 4-3-2, the two dielectrics have similar difference of ΔV_{FB} obtained from the pulse and conventional CV measurements. The

results extracted from SiO_2 identify the reliability of the proposed measurement system. At all total dose levels, the value of ΔV_{FB} of HfO_2 remains at a higher level for both the pulse and conventional technique. This is because the positive oxide-trapped charge density in HfO_2 is much larger than that in SiO_2 [35, 36].

The annealing effects do exist in real cases, especially in low-dose-rate irradiation exposure. There are two kinds of annealing effects: annealing during irradiation and post-irradiation annealing. During irradiation, the main cause of annealing is the sense process, as discussed above. As for the post-irradiation annealing, the bias-induced charges would tunnel to the oxide and be trapped in both deep and shallow energy levels of the oxide to compensate the radiation-induced charges. With regard to conventional CV measurements, the accumulation of these bias-induced oxide trapped charges would cause significant recovery of ΔV_{FB} as indicated by Dixit *et al* [36]. However, this study has been focused only on the on-site radiation-induced charge trapping behaviors in HfO_2. We have not done the post-irradiation annealing study of HfO_2. We recognize it as a crucial issue to be extensively discussed in our future work.

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Chapter 5: Radiation response of Ge MOS Capacitors with $Hf_xZr_{1-x}O_y$ Gate Dielectrics

As the scaling of complementary metal oxide semiconductor (CMOS) devices requires the increase in gate capacitance for better channel control, while maintaining low leakage current, the high-*k* gate dielectric has been used to replace SiO_2 for nanoscale CMOS device applications [1-3]. Because of its relative high band gap and compatibility in contact with channel region, HfO_2 has been considered as a promising candidate for high-*k* gate dielectrics in COMS technology [4, 5]. However, the dielectric constant of HfO_2 is not high enough to obtain the continued scaling of advanced metal oxide semiconductor field effect transistors (MOSFETs). ZrO_2 offers the benefit of a higher dielectric constant due to easier stabilization of its tetragonal phase as opposed to the monoclinic phase in crystallized HfO_2. In addition, HfO_2 and ZrO_2 are chemical similar and thus completely miscible in solid state [6, 7]. It has been reported that the addition of ZrO_2 into HfO_2 gate dielectric stabilizes the tetragonal phase and enhances the dielectric constant [8]. $Hf_xZr_{1-x}O_y$ dielectric is thus an attractive candidate for advanced gate stack applications.

On the other hand, germanium (Ge) is of great interest as a promising channel material for future MOSFETs because it processes higher intrinsic carrier mobility (four times for hole and two times for electron mobility) compared with that of silicon (Si).

Likewise, Ge applications can offer high compatibility with conventional Si integration technologies [9, 10]. However, a fundamental issue of the application of Ge in CMOS technology is that Ge easily forms unstable oxides GeO_x on the surfaces, which can result in a poor quality interface between the Ge channel and high-*k* dielectrics and low carrier mobility in the channel. This technological issue has been overcome by the passivation of Ge surface, which can prevent oxidation formation during device processing [11-13]. It has been reported that sulfur passivation of germanium is very effective in preventing the formation of the GeO_x at the interface, which can lead to superior Ge gate stack [14, 15]. The reduction of interface defects is attributed to the formation of Ge-S bonds and GeS species at the Ge/high-*k* surface. The electrical characteristics of Ge MOS devices with $Hf_xZr_{1-x}O_y$ gate dielectric have been investigated in recent studies [16]. It has been reported that the interface trap density and sub-threshold swing of Ge MOSFETs are clearly improved by the addition of ZrO_2 into HfO_2 gate dielectric. Therefore, Ge devices with $Hf_xZr_{1-x}O_y$ gates could be promising candidates for advanced CMOS technologies and integrated circuits.

Advanced MOS devices employed in space applications are subjected to radiation exposure which can lead to device degradation and circuit failures. Several studies suggest that, unlike conventional Si/SiO_2 case, a significant density of trapped charges can be observed in high-*k* dielectrics under long-term radiation and bias conditions [17-21]. Qualification of high-*k* dielectrics for space applications needs far more studies to identify the charge trapping behaviors and reliability performance. Consequently, it is important to characterize the radiation response of Ge MOS devices with $Hf_xZr_{1-x}O_y$.

However, very little research has been done on the total dose effects of these devices. In this work, we have investigated the total ionizing dose radiation effect on $Hf_xZr_{1-x}O_y$ thin films prepared by atomic layer deposition (ALD) deposited on $(NH_4)_2S$ passivated Ge substrate. The measurements were carried out under continuous gamma-ray exposure with positive and negative bias. The bias instability of the $Hf_xZr_{1-x}O_y$ gate dielectric with various ZrO_2 content are also studied.

To investigate their radiation response, devices were irradiated at an on-site radiation response probe station system with a 662-KeV Cs^{137} γ-ray radiation source [22]. After taking into account the dose enhancement effect, the dose rate of HfO_2 and $HfZrO_2$ thin films was 0.116 rad(HfO_2)/s and 0.079 rad(ZrO_2)/s. A total dose up to 45 krad (HfO_2) was applied to devices with a constant gate bias of 0.5 V or -0.5 V. During the biased irradiation, oxide and interface charge trapping behaviors of $Hf_xZr_{1-x}O_y$ thin films were demonstrated by analysis of Capacitance-Voltage (C-V) curves at the frequency of 1 MHz. The C-V and Current-Voltage (I-V) measurements were carried out by a HP 4284 Precision LCR meter and an Agilent B1500A Semiconductor Device Analyzer.

The atomic ratios of the $Hf_xZr_{1-x}O_y$ thin films investigated are shown in Table. 5-1. Sample A was grown with the Hf:Zr deposition ratio of 1:1, (i.e. every HfO_2-H_2O cycle followed by a ZrO_2 -H_2O cycle), while the deposition ratio for sample B was 3:1. It can be observed that the atomic ratios of the thin films are 0.43:0.57 and 0.6:0.4 (Hf:Zr) for sample A and sample B, respectively. The indicates that the deposition rate of ZrO_2 is

Table 5-1. Energy Dispersive Spectrometer measurements of $Hf_xZr_{1-x}O_y$ thin films on Ge (100) substrates. For ALD deposition sequence, A: Hf:Zr =1:1, B: Hf:Zr= 3:1.

Element	Weight %		Atomic %	
Sample	A	B	A	B
O	4.12	4.22	16.94	17.59
Ge	86.06	83.65	78.04	76.89
Zr	3.95	2.76	2.85	2.02
Hf	5.88	9.37	2.17	3.05

higher than that of HfO_2. Moreover, no measurable impurity has been observed in the deposited films.

The impact of Zr composition in $Hf_xZr_{1-x}O_y$ gate dielectrics on their leakage behavior are exhibited in Fig.5-1. It is shown that the gate leakage density is increased with the increasing of Zr composition in gate oxide. This can be explained by the smaller band gap and lower band offset of ZrO_2 compared with HfO_2. The higher leakage current density of ZrO_2 is identical to previous reports for $Hf_xZr_{1-x}O_y$ dielectric deposited on Si substrate [6]. The effects of the surface passivation of Ge on the leakage behavior in $Hf_xZr_{1-x}O_y$ MOS capacitors is also shown in Fig.5-1. It can be observed that the leakage current is decreased after the sulfur treatment of Ge surface. Mao *et al*. have reported that the density and location of interface traps at dielectric/Si surface have significant effects to gate leakage current [23]. It was also reported that the passivation

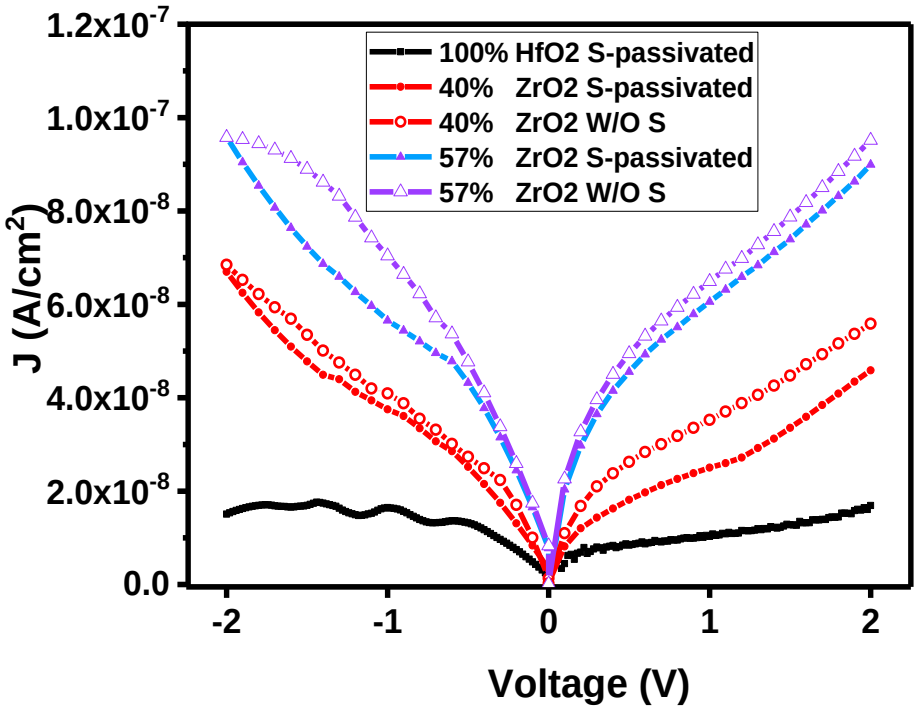


Figure 5-1. Current Density-Voltage (J-V) Characteristics for $Hf_xZr_{1-x}O_y$ dielectrics on Ge MOS devices. The gate leakage density is increased with the increasing of Zr compositions in $Hf_xZr_{1-x}O_y$ gate oxide.

of Ge surface can result in the formation of high-*k*/S/Ge stack and thus decreasing the interface traps [14]. Therefore, the improved leakage characteristics in sulfur passivated samples can be attributed to the reduction of interface trap density. However, the leakage behavior of the MOS capacitors cannot fully identify the impacts of sulfur treatment and Zr composition to Ge interface states. It is necessary to investigate the interface defects by evaluating bias instability of the MOS capacitors via their C-V characteristics.

In section 3, the radiation response measurements of Si based MOS capacitors were carried out by both conventional C-V and pulse C-V techniques. However, for Ge based MOS capacitors, only conventional C-V measurements were performed. The complete

C-V curves of Ge MOS capacitors cannot be measured by pulse C-V measurements. One of the possible explanation is that the interface trap density of Ge/high-*k* interface is very large compared to that of Si surface. The dangling bonds at the interface is able to combine with the electrons and holes from high-*k* oxide. When the C-V testing gate voltage is in the range of strong inversion region, and the testing frequency is very low (i.e. pulse C-V measurements), the electrons and holes which combined with dangling bonds have significant effects to space charge region in semiconductor. If the interface trap density is very large, the capacitance of MOS capacitor in strong inversion region equals to the oxide capacitance. When the testing frequency is very large (i.e. conventional C-V measurements), the frequency of combination and generation of electrons and holes in strong inversion region is much lower than the testing frequency. The capacitance of MOS capacitor in strong inversion region is determined by the oxide capacitance connected in series with capacitance of semiconductor.

5.1 Bias Instability

Fig. 5-1-1 shows the C-V characteristics of Ge MOS capacitors with various Zr-compositions of $Hf_xZr_{1-x}O_y$ gate dielectrics. The result indicates that higher dielectric constants can be observed in Zr-doped $Hf_xZr_{1-x}O_y$ thin films. It can be understood that the addition of ZrO_2 into HfO_2 gate oxide stabilizes the tetragonal phase and shows higher dielectric constant, whereas the HfO_2 exhibits monoclinic phase as opposite to ZrO_2 [6, 7]. Smaller hysteresis was extracted from the C-V curves of MOS capacitors with $Hf_{0.43}Zr_{0.57}O_2$ and $Hf_{0.6}Zr_{0.4}O_2$ dielectrics. The hysteresis between the ramped up

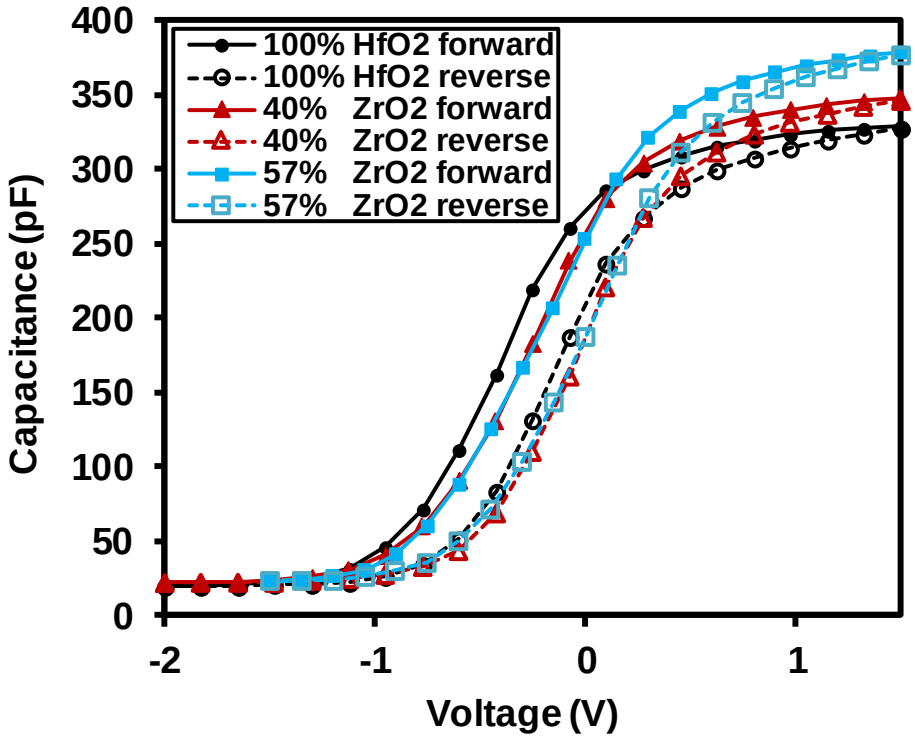


Figure 5-1-1. Capacitance-Voltage (C-V) characteristics of Ge MOS capacitors with HfO_2, $Hf_{0.6}Zr_{0.4}O_2$, and $Hf_{0.43}Zr_{0.57}O_2$ gate dielectrics. The permittivity of gate oxide increase with the increasing of ZrO_2 compositions in $Hf_xZr_{1-x}O_y$ dielectrics.

and ramped down of C-V curves was originated from part of the defects in high-*k* oxide which can be repeatedly neutralized and recharged by charge injection from the substrate [24, 25]. Therefore, the results imply that Zr-containing HfO_2 gate dielectrics has fewer cyclic charged traps or border traps compared with HfO_2. In addition, the gate ZrO_2 doped dielectrics shows a positive flat-band voltage shift (ΔV_{FB}) compared with HfO_2, which may be attributable to the presence of pre-existing electron traps or the lack of positive charges in ZrO_2.

As discussed in our Charter 4, the ΔV_{FB} of irradiated devices under electric field is attributed to the combined effect of radiation-induced and bias-induced charge trapping

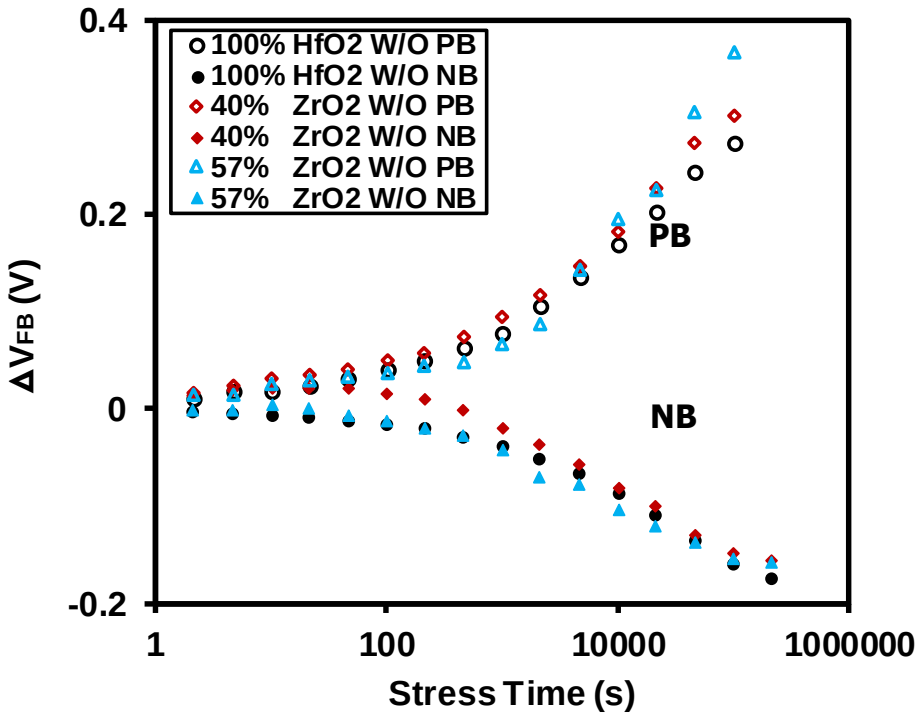


Figure 5-1-2. Flat-band voltage shifts (ΔV_{FB}) induced by -0.5 V or 0.5 V bias without irradiation as a function of stress time for Ge MOS capacitors with $Hf_xZr_{1-x}O_y$ gate dielectrics. Under positive bias (PB), larger ΔV_{FB} were obtained from Zr-containing devices after a stress time of 130 hours. Under negative bias (NB), no significant discrepancy of ΔV_{FB} can be observed.

in dielectrics [26]. In order to separate the bias-instability and radiation-caused shifts, the ΔV_{FB} of the devices under electric field without radiation exposure was observed [20, 27, 28]. Fig. 5-1-2 illustrated the ΔV_{FB} of Ge MOS capacitors with various Zr-containing $Hf_xZr_{1-x}O_y$ gate dielectrics. The ΔV_{FB} were estimated by C-V measurements of HfO_2, $Hf_{0.6}Zr_{0.4}O_2$ and $Hf_{0.6}Zr_{0.4}O_2$ respectively before and after pure positive or negative bias as illustrated in Fig. 5-1-3 (a), (b) and (c). Under positive bias (PB), $Hf_xZr_{1-x}O_y$ with various Zr compositions all exhibited positive ΔV_{FB} up to 0.38 V. As the ΔV_{FB} was attributed to the combined effect of net oxide trapped charges and

interface traps at the Ge/high-*k* interface, this positive ΔV_{FB} of $Hf_xZr_{1-x}O_y$ gate dielectrics was induced by electron tunneling from the Ge substrate to form negatively charge states and/or the build-up of interface traps. In addition, ΔV_{FB} of the capacitors increases with the increase of Zr composition in $Hf_xZr_{1-x}O_y$. This result indicates that HfO_2 dielectrics exhibits relative low electron trap density or interface trap density compared with that of ZrO_2. Negative bias (NB) applied on the $Hf_xZr_{1-x}O_y$ capacitors for more than 130 hours without irradiation resulted in negative ΔV_{FB} up to -0.18 V. No significant discrepancy of ΔV_{FB} was observed for $Hf_xZr_{1-x}O_y$ thin films with various Zr compositions. This can be explained by an approximately equal density of both net positive oxide trapped charges and interface charges for HfO_2 and ZrO_2. However, as shown in the following results (Fig. 5-1-4), it seems more probable that the combined

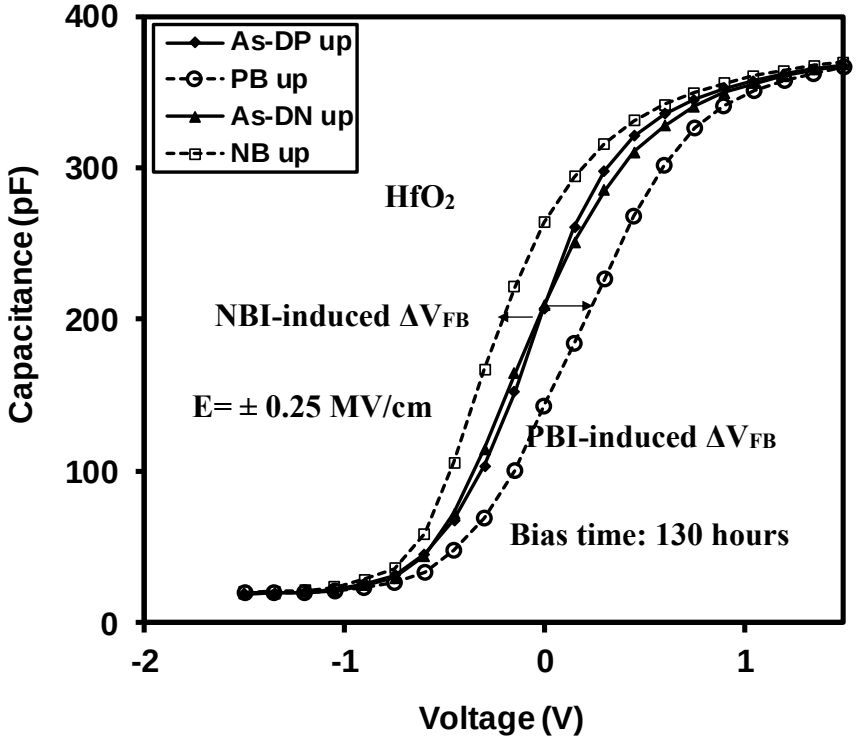
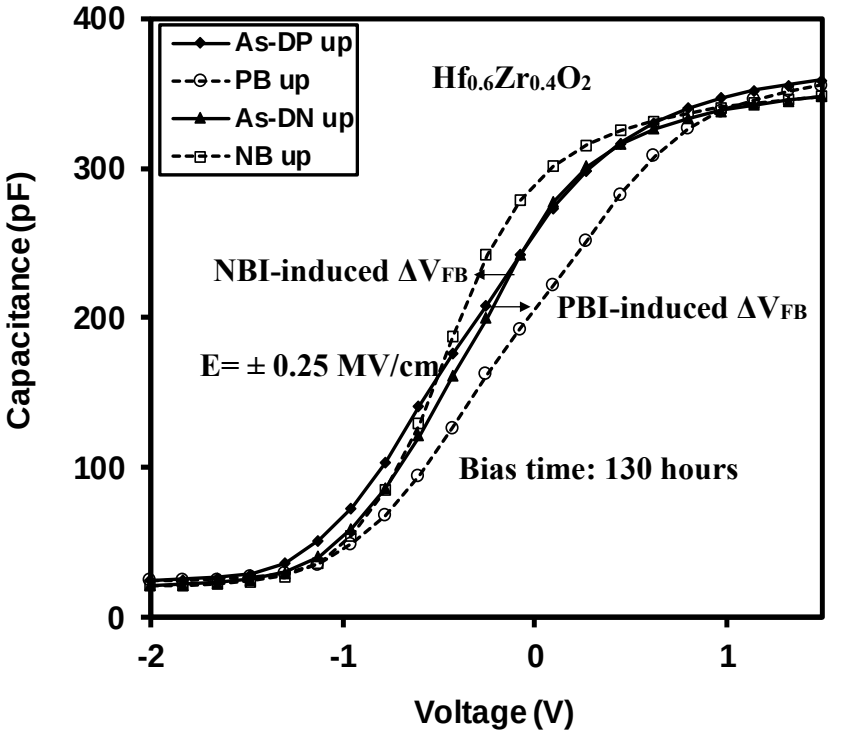
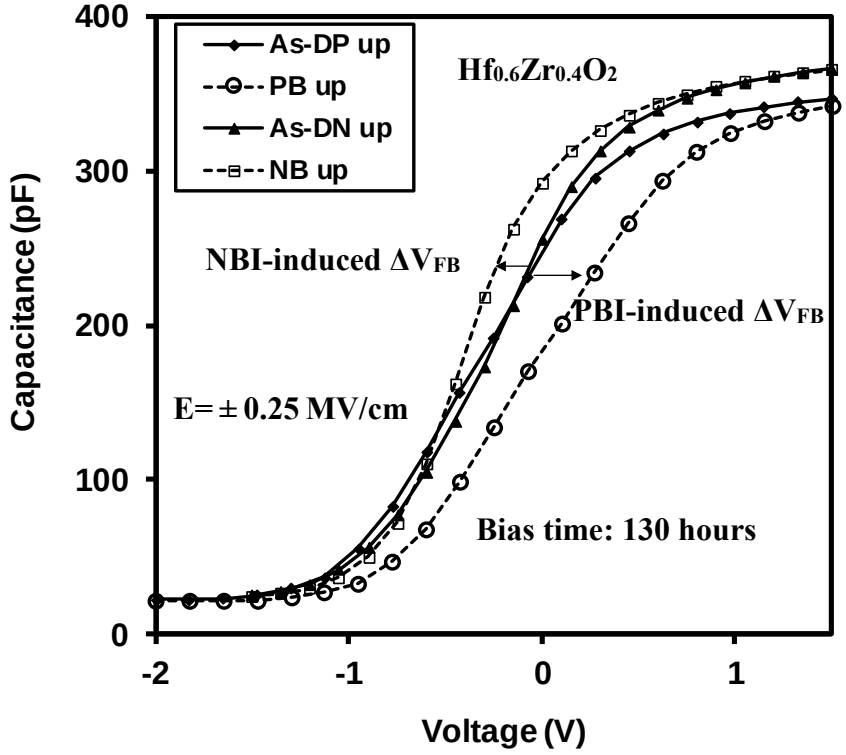


Figure. 5-1-3 (a)



(b)



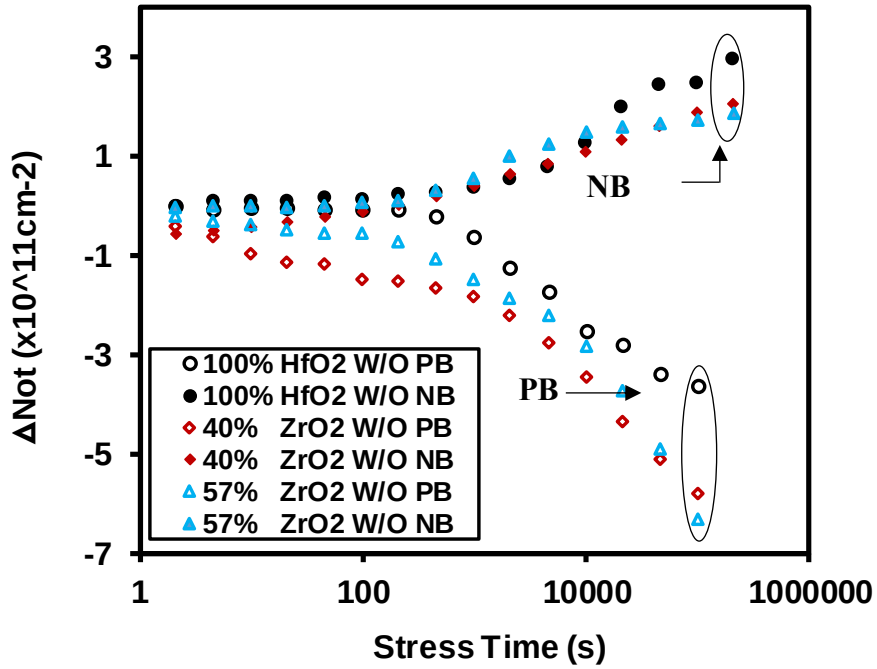
(c)

Figure 5-1-3. C-V curves for (a) HfO_2, (b) $Hf_{0.6}Zr_{0.4}O_2$ and (c) $Hf_{0.43}Zr_{0.57}O_2$ gate dielectrics before and after positive or negative gate bias for 130 hours at an electric field of 0.25 MV/cm. The effects were dominated by ΔV_{FB} as indicated.

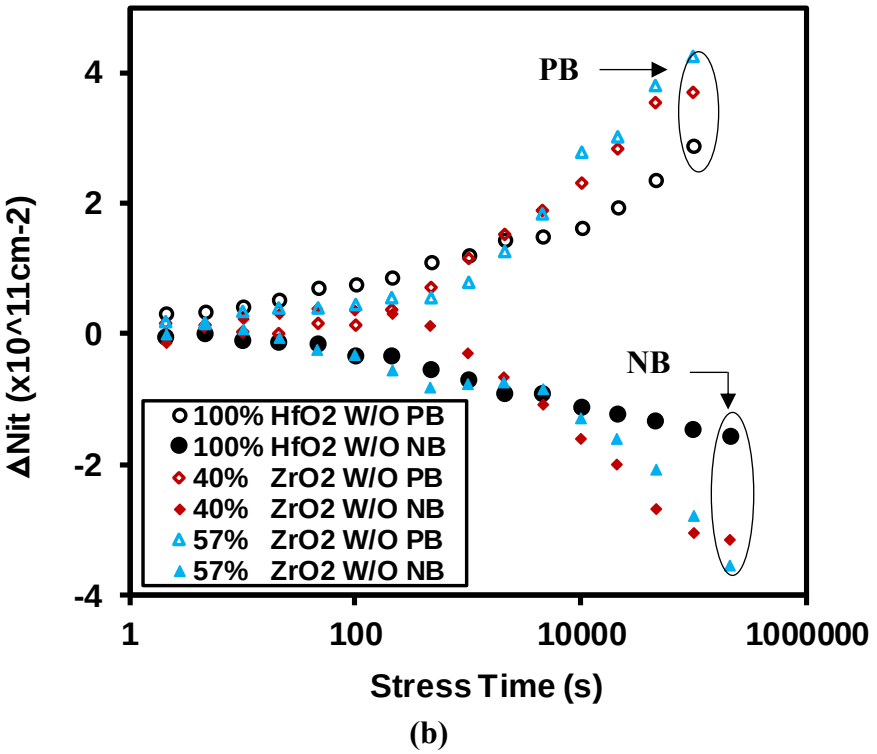
effect of oxide and interface charge trapping is the dominant cause for the identical ΔV_{FB} obtained under NB.

In order to determine the charge trapping behavior in $Hf_xZr_{1-x}O_y$ gate dielectrics under pure bias conditions, oxide trap density (ΔN_{ot}) and interface trap density (ΔN_{it}) was calculated from the C-V curves used in the extraction of ΔV_{FB} in Fig. 5-1-3. The calculated ΔN_{ot} as a function of stress time for both PB and NB is shown in Fig. 5-1-4 (a). The density of negative oxide trapped charges increases in magnitude with increasing Zr composition in $Hf_xZr_{1-x}O_y$ during PB. It was reported that the possible oxide trap centers in HfO_2 and ZrO_2 are related to oxygen vacancies and interstitials (O^0/O^-) [29]. Since the oxygen vacancies in high-*k* dielectrics behave as negative oxide traps, the larger ΔN_{ot} of Zr-containing dielectrics under PB suggests that the oxygen-vacancy concentration in $Hf_xZr_{1-x}O_y$ is increased by the addition of Zr [16]. Under NB, ΔN_{ot} of HfO_2 was larger than that of Zr-containing $Hf_xZr_{1-x}O_y$ when the stress time was longer than 6 hours. The result may indicate that more pre-existing hole traps are located in HfO_2 compared with ZrO_2. It is notable that the difference of oxygen vacancy and hole trap density between $Hf_{0.43}Zr_{0.57}O_2$ and $Hf_{0.6}Zr_{0.4}O_2$ is negligible. It can be tentatively suggested that the concentration of oxide traps in Zr-doped $Hf_xZr_{1-x}Oy$ is not strongly dependent on Zr composition.

Fig. 5-1-4 (b) shows the ΔN_{it} for Ge MOS capacitors with $Hf_xZr_{1-x}O_y$ gate dielectrics under PB and NB. The interface trap density of $Hf_xZr_{1-x}O_y$ with various Zr compositions was all increased during PB. This can be attributed to the build-up of Ge



(a)



(b)

Figure 5-1-4. (a) ΔN_{ot} and (b) ΔN_{it} as a function of stress time for Ge MOS capacitors with HfO_2, $Hf_{0.6}Zr_{0.4}O_2$, and $Hf_{0.43}Zr_{0.57}O_2$ gate dielectrics under -0.5 V or 0.5 V bias without irradiation exposure. ΔN_{ot} was extracted from the mid-gap voltage shift of C-V curves of Ge devices. ΔN_{it} was calculated from ΔV_{FB} and mid-gap voltage shift of Ge devices.

dangling bonds at Ge/dielectrics interface. It has been reported that the passivation of Ge surface by sulfide can result in Ge-S bonds and thus decrease the interface traps [11, 15]. Moreover, it is suggested that H^+ protons generated at the anode by positive bias can drift to the Ge interface and break the passivated Ge-S bonds as shown in Fig. 5-1-5 [27, 30]. One possible reaction of the formation of an interface trap is shown in (5.1):

$$Ge - S + 2\ H^+ \rightarrow Ge^+ + H_2S \qquad (5.1)$$

Therefore, the depassivation of passivated Ge-S bonds under positive bias can lead to an increase in interface trap density for Ge MOS capacitors. In addition, more interface traps were generated in Zr-doped $Hf_xZr_{1-x}O_y$ compared to HfO_2. The lager ΔN_{it} of Zr containing $Hf_xZr_{1-x}O_y$ suggested that ZrO_2 tended to present more hydrogen-related species than HfO_2. With regard to NB, ΔN_{it} of $Hf_xZr_{1-x}O_y$ with various Zr compositions are negatively increased. In this case, Ge dangling bonds at the interface were passivated. Moreover, it can be observed that more passivated dangling bonds are generated in Zr-doped $Hf_xZr_{1-x}O_y$. However, the source for passivation and related mechanisms are not fully understood yet. The difference of ΔNit between the different devices suggested that the source for passivation of dangling bonds was likely from the oxide, but not hydrogen in Ge.

5.2 Biased Irradiation Effects

Fig. 5-2-1 shows the ΔV_{FB} for Ge MOS capacitors with various $Hf_xZr_{1-x}O_y$ dielectrics irradiated to 45 krad(HfO_2) total dose at 0.5 V and -0.5 V. The ΔV_{FB} were

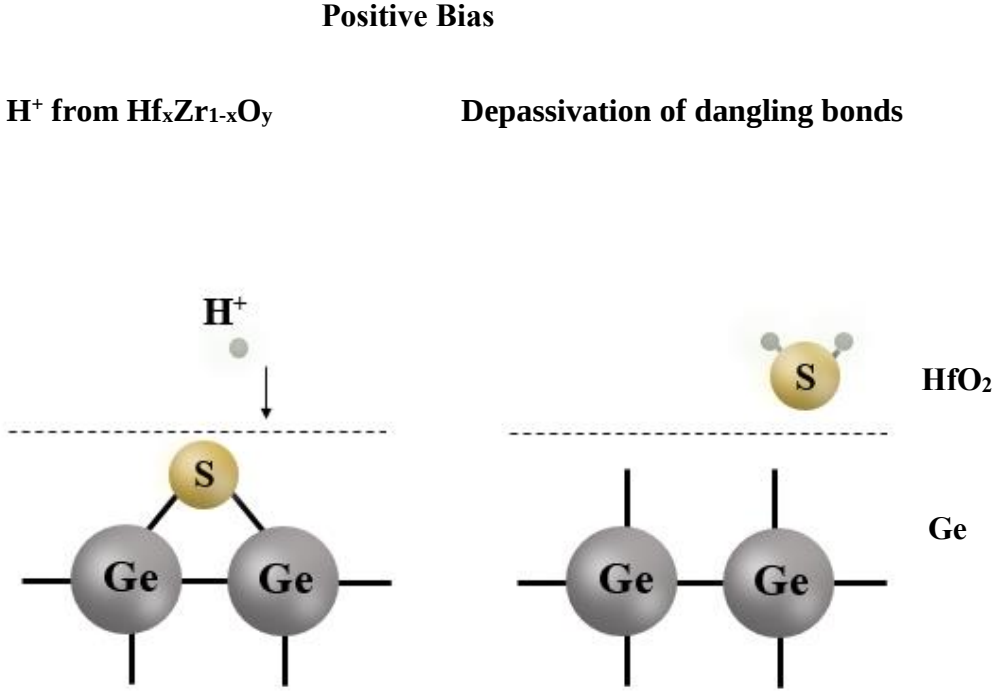


Figure 5-1-5. The Schematic diagram of Ge MOS capacitors with $Hf_xZr_{1-x}O_y$ dielectrics showing depassivation process of Ge-S bonds. Under positive bias, H^+ ions can be generated at the anode and drift to the Ge interface to break the passivated Ge-S bonds [27, 30].

estimated by C-V measurements of HfO_2, $Hf_{0.6}Zr_{0.4}O_2$ and $Hf_{0.6}Zr_{0.4}O_2$ respectively before and after positive or negative biased irradiation as illustrated in Fig. 5-2-2 (a), (b) and (c). Positive biased irradiation (PBI) on the devices for more than 130 hours resulted in positive ΔV_{FB} up to 0.58 V. Comparing to the result obtained from Fig. 5-1-2, larger ΔV_{FB} was extracted under radiation exposure for HfO_2 and $Hf_{0.6}Zr_{0.4}O_2$. However, no significant discrepancy of ΔV_{FB} can be observed for $Hf_{0.43}Zr_{0.57}O_2$ thin films with and without radiation. In addition, the ΔV_{FB} of the irradiated capacitors under PBI decreased with the increasing of Zr composition in $Hf_xZr_{1-x}O_y$, which has an opposite trend compared with that of un-irradiated capacitors. Since the radiation-

induced ΔV_{FB} of $Hf_xZr_{1-x}O_y$ dielectrics is determined by the density of oxide traps and interface states, the related charge trapping behaviors are investigated and shown in Fig. 5-2-3 (a) and (b), respectively.

Under PBI, $Hf_xZr_{1-x}O_y$ with various Zr compositions all exhibited the presence of net negative oxide trapped charges as indicated in Fig. 5-2-3 (a). Values of these ΔN_{ot} were larger than the pure PB results in Fig. 5-1-4 (a). This enhancement was mainly caused by the net radiation-induced negative trapped charges in $Hf_xZr_{1-x}O_y$. However, the effect of oxide trapped charges to devices is more significant when the location of these charges are closer to the high-*k*/Ge interface, and the radiation-induced holes are

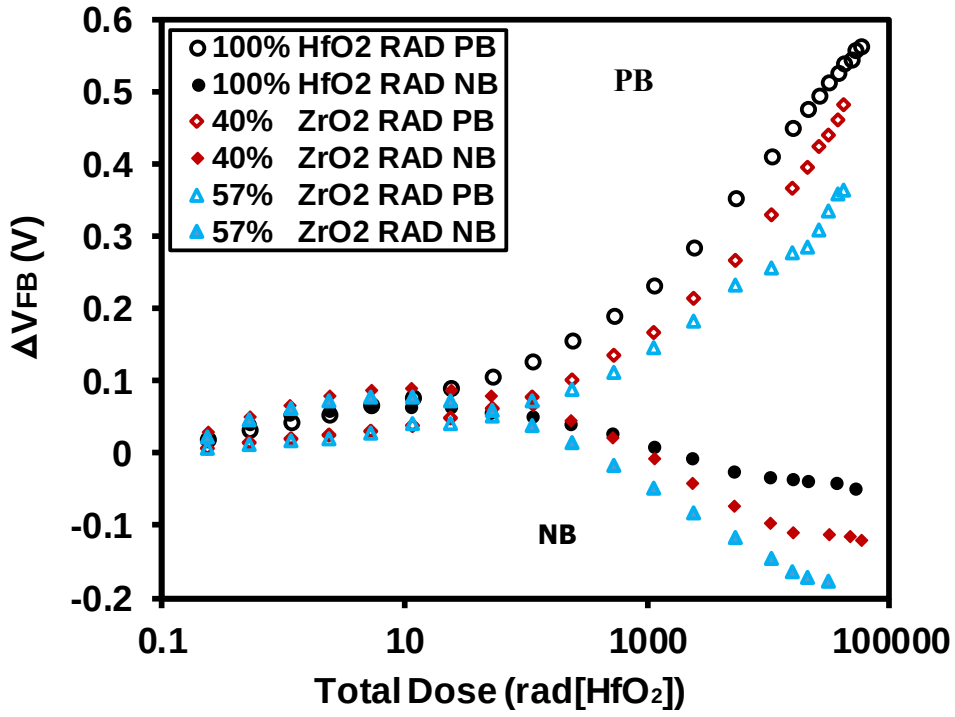


Figure 5-2-1. ΔV_{FB} as a function of total dose for Ge MOS capacitors with $Hf_xZr_{1-x}O_y$ gate dielectrics under -0.5 V or 0.5 V biased irradiation. ΔV_{FB} were extracted from the flat-band voltage shift of C-V curves in Fig. 5-2-2.

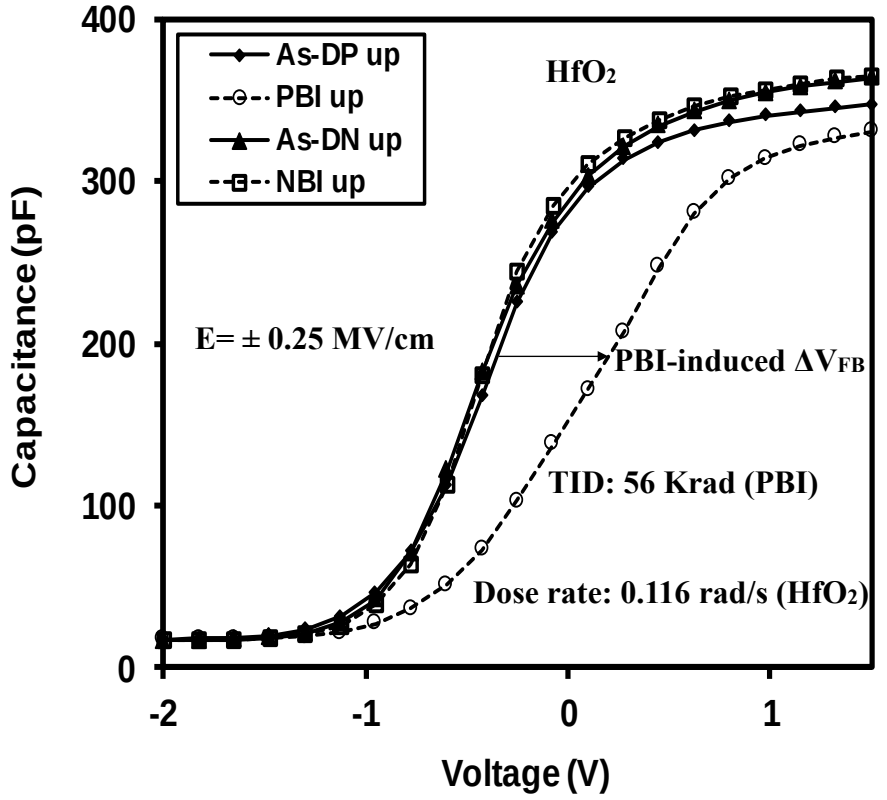


Figure 5-2-2 (a)

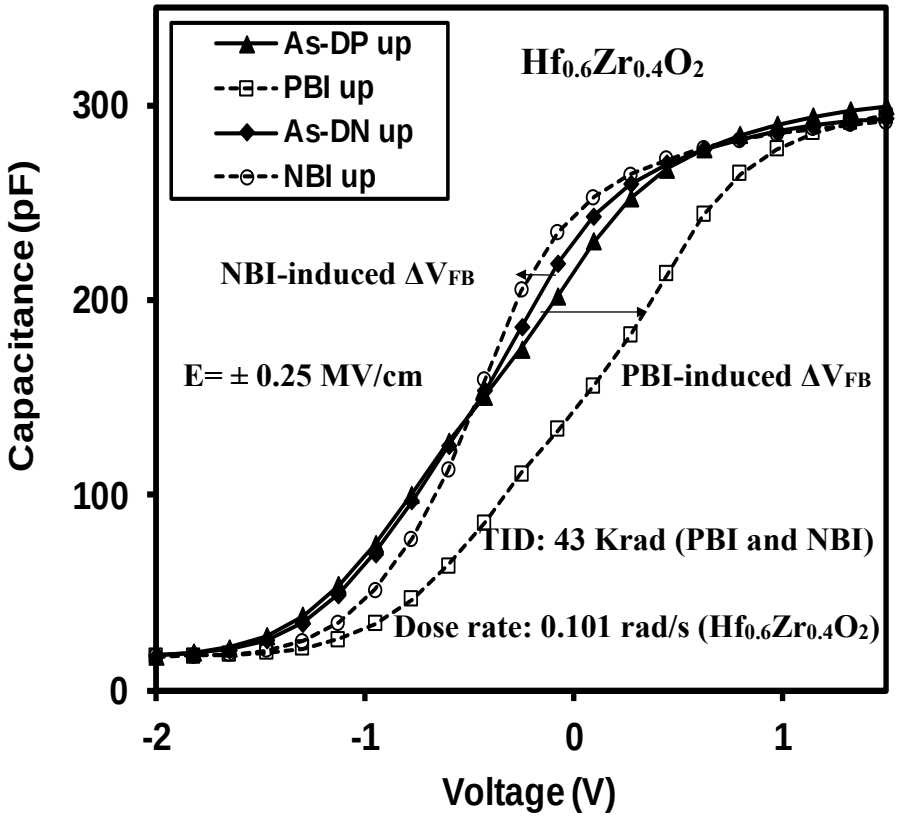
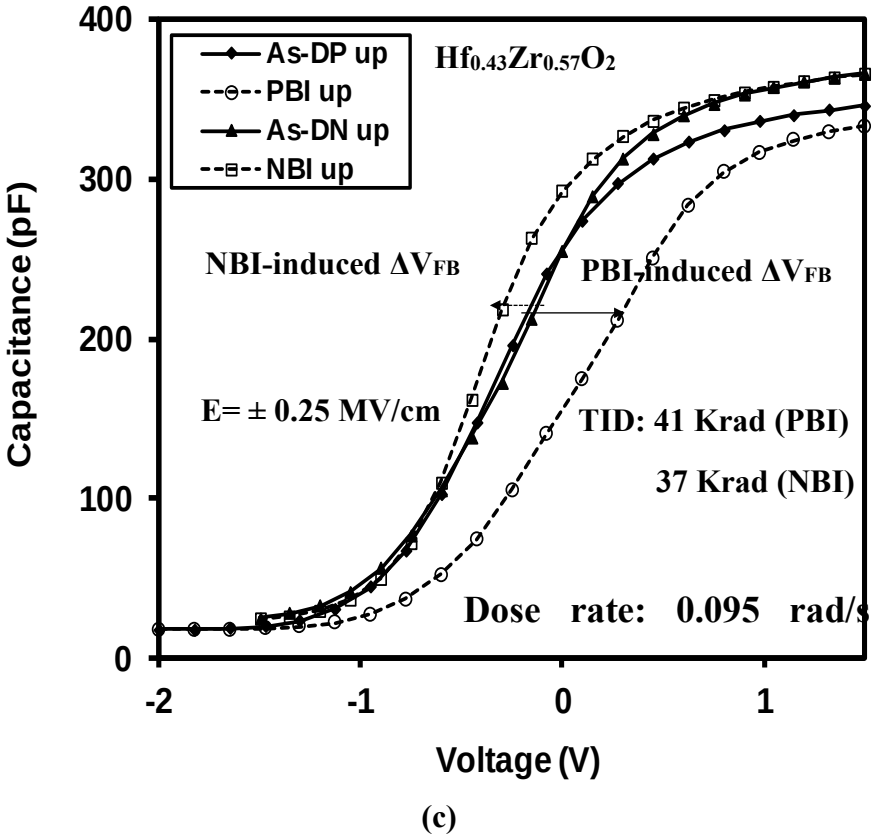


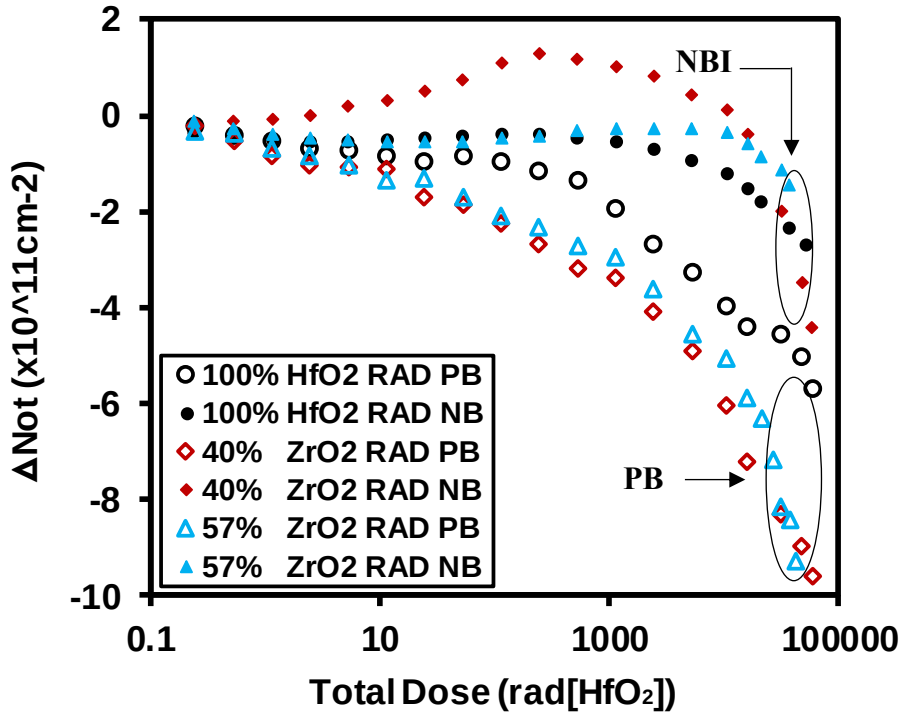
Figure 5-2-2 (b)



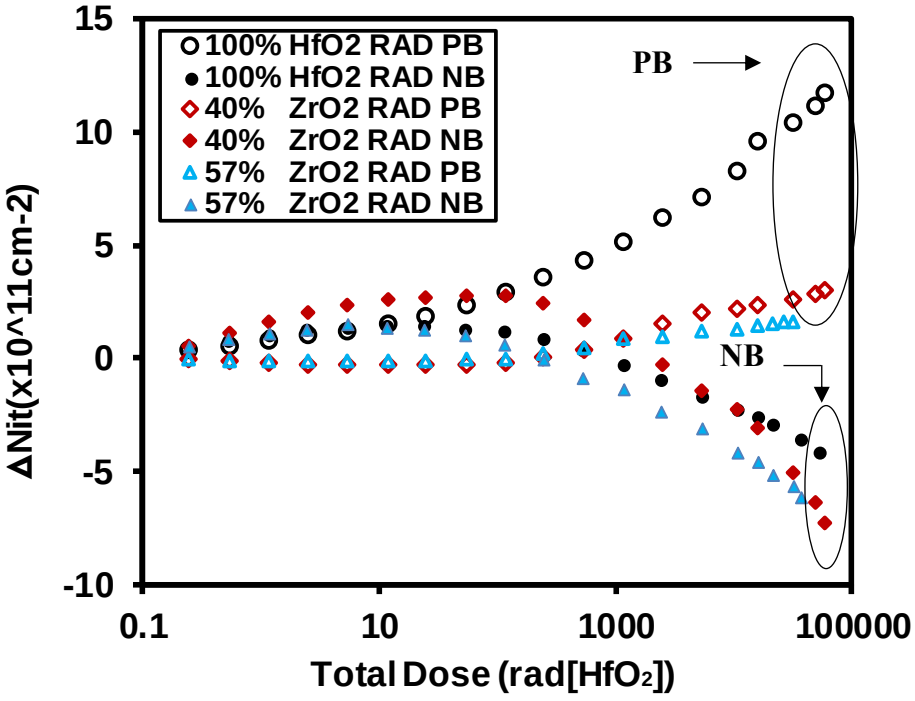
(c)

Figure 5-2-2. C-V curves for (a) HfO_2, (b) $Hf_{0.6}Zr_{0.4}O_2$ and (c) $Hf_{0.43}Zr_{0.57}O_2$ gate dielectrics before and after biased radiation at an electric field of 0.25 MV/cm. The effects were dominated by ΔV_{FB} as indicated.

likely to transport to high-*k*/Ge interface under positive bias [31]. The PBI exposed to $Hf_xZr_{1-x}O_y$ dielectrics is expected to induce more holes trapping. Therefore, the presence of net negative trapped charges during PBI suggests that the density of electron traps in $Hf_xZr_{1-x}O_y$ was much larger than hole traps. On the other hand, similar to the results in Fig. 5-1-4 (a), the density of negative oxide trapped charges increases with increasing Zr composition in $Hf_xZr_{1-x}O_y$. These results support that more oxygen-vacancies are located in ZrO_2 compared with HfO_2, which was observed in Fig. 5-1-4 (a).



(a)



(b)

Figure 5-2-3. (a) ΔN_{ot} and (b) ΔN_{it} as a function of total dose for Ge MOS capacitors with $Hf_xZr_{1-x}O_y$ gate dielectrics under -0.5 V or 0.5 V biased irradiation. ΔN_{ot} were extracted from the mid-gap voltage shift of C-V curves. ΔNit was calculated from the ΔV_{FB} and mid-gap voltage shift of irradiated Ge devices.

The ΔN_{it} of the Ge MOS capacitors under PBI is shown in Fig. 5-2-3 (b). $Hf_xZr_{1-x}O_y$ with various Zr compositions all exhibited the build-up of Ge dangling bonds. Under PBI, electron-hole pairs (EHPs) can be generated and transported toward to Ge substrate. During the transportation of radiation-induced holes, H^+ protons can be released from the $Hf_xZr_{1-x}O_y$ dielectrics, Hf-H, Zr-H bonds, and sub-oxide bonds [27]. As discussed in Fig. 5-1-4 (b), these H^+ transport to the Ge interface and break the passivated Ge-S bonds, forming Ge dangling bonds. Besides, the irradiation exposure can also directly break the Hf-H, Zr-H bonds, or other bonds associated with hydrogen. The ΔN_{it} of HfO_2 in Fig. 5-2-3 (b) is larger than it is observed without irradiation, whereas no significant discrepancy can be found for Zr-doped $Hf_xZr_{1-x}O_y$.

The results indicated that more H^+ ions were generated in HfO_2 during PBI than that of ZrO_2, which was in contrast to the pure PB results. The results also suggested that more radiation-induced holes were generated in HfO_2, leading to higher concentration of H^+ ions during the transportation of holes. Another possible explanation is that Zr-H bond has a higher bond energy, meaning that the Zr-H bonds in ZrO_2 are less susceptible to breaking by irradiation exposure and exhibited a lower density of H^+ protons. Considering the results obtained in Fig.5-2-2 and Fig.5-2-3, the large radiation-induced ΔNit under PBI, is the dominate cause for ΔV_{FB} in Ge MOS capacitors with HfO_2. Conversely, the radiation response for Zr-containing dielectrics under positive bias is mostly affected by oxide traps. Comparing to the results evaluated in our previous study, the ΔV_{FB} evaluated in HfO_2 Ge devices is 7~8 times larger than that of Si devices, which is attributable to the large density of interface traps at the

$Hf_xZr_{1-x}O_y$ / Ge interface, that can result in significant effect to ΔV_{FB}.

ΔV_{FB}, ΔN_{ot}, and ΔN_{it} of the Ge MOS capacitors under negative biased irradiation (NBI) was also presented in Fig.5-2-2 and Fig.5-2-3. After a total dose exposure up to 45 krad (HfO_2), a maximum ΔV_{FB} of -0.19 V was observed, which was comparable to the results extracted in Fig. 5-1-2. The ΔV_{FB} of the irradiated capacitors increased in terms of magnitude with the increasing of Zr composition in $Hf_xZr_{1-x}O_y$. As discussed above, this trend is likely associated with the combined effect of oxide and interface traps. In contrast to bias effects alone, the ΔN_{ot} of $Hf_xZr_{1-x}O_y$ dielectrics under NBI, indicated the presence of net negative oxide trapped charges after the total dose of 10 krad.

For $Hf_{0.6}Zr_{0.4}O_2$ thin films, the accumulation of net positive charges was observed at the total dose less than 1 krad. Therefore, it is suggested that both bias-induced hole traps and radiation-induced electron traps dominated the oxide charge trapping of $Hf_xZr_{1-x}O_y$ under NBI at low dose level. At the total dose larger than 10 krad, the radiation response is mainly affected by radiation-induced negative oxide trapped charges. Similarly, ΔN_{it} of $Hf_xZr_{1-x}O_y$ under NBI increase negatively at high does level, which is explained by the passivation of Ge dangling bonds at interface. However, more passivated Ge-H or Ge-S bonds can be observed in irradiated devices than the pure negative-biased capacitors. This result may indicate that more electrons are transported to Ge interface to suppress the de-passivation reaction (reaction (1)) during NBI.

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Charter 6: Conclusion

In summary, the development of an on-site and real-time radiation response measurement system has been presented for electrical characterization of semiconductor devices and thin films subjected to γ-ray exposure. The real-time radiation response measurements of semiconductor devices and components during continuous γ-ray irradiation can give a new insight into the electrical characteristics of the devices and materials used in real radiation environments. The system has been successfully used to measure the electrical characteristics of semiconductor devices with pulse and stress techniques with a 1.11 GBq Cs^{137} γ-ray source at low dose rates. The C-V and I-V results of MOS capacitors as well as MOSFET devices measured by each technique have been reported and compared.

A reliable measurement system for radiation response studies while maintaining radiation safety of the operator has been demonstrated by establishing a dose attenuation model in the experimental environment. A dose rate of 0.0603 rad/s for HfO_2 has been calculated by a novel dose rate calculation model presented in this work. The average dose rate obtained from short TLDs exposures was 16% lower than the dose rate of LiF (0.0369 rad/s) calculated from the dose rate model. The average dose rates of HfO_2 in the experiment after taken into account the dose enhancement effect was 0.116 rad/s. It was also suggested that the real-time and on-site measurements

assess more precisely the radiation-induced degradation of gate dielectrics in HfO_2 thin films compared with the conventional measurement technique.

Detailed investigations of the low-dose-rate radiation responses of HfO_2/SiO_2–Si capacitors were characterized by pulse and conventional CV measurements under continuous γ-ray exposure. We have found that a very large concentration of radiation-induced oxide trapped charges is generated in the oxide. However, the conventional measurement extracts very small values of ΔV_{FB}. This has been attributed to the compensation of radiation-induced oxide trapped charges by bias-induced charges for measurements completed in a relatively long time (more than 7 seconds). It has also been demonstrated that both the positive and negative trapping/de-trapping dominate the radiation response of HfO_2 dielectrics.

Consequently, a framework and measurement methodology has been proposed for better understanding the mechanisms of radiation-induced charge trapping and compensation of bias-induced charges in HfO_2 stacks. During the measurements, the bias-induced oxide trapped charges tunnel into HfO_2 again to cause recovery of radiation-induced ΔV_{FB}. Fast characterization using pulse CV can measure these effects and avoid the compensation of the bias-induced charges. Moreover, the density of effective trapped charges decreases with the increase of the edge time. According to the results in this work and our previous study, we tentatively suggest that the effect of the peak voltage time on the concentration of net oxide trapped charges is negligible. A higher pulse magnitude would cause larger ΔV_{FB} during the biased irradiation pulse CV

measurements. Similar to HfO_2, the SiO_2-based capacitors exposed to gamma radiation show a negative ΔV_{FB} of up to -224 mV and -31 mV, respectively from pulse and conventional CV measurements. These results further support that the radiation response of HfO_2 was correctly estimated by using the proposed measurement system. The significant ΔV_{FB} suggests that it is quite challenging for HfO_2 to replace SiO_2 in combined radiation and bias environment. However, the large bidirectional radiation-induced ΔV_{FB} of HfO_2-based capacitors was only extracted from pulse CV and on-site measurements. On the other hand, the discussions in this study were focused only on the radiation response of ~ 24 nm HfO_2 dielectrics instead of considering real devices, with thinner dielectrics of most commercial interest. Such a thickness is relevant for investigation of the failure mechanisms of hafnium oxide. Since the HfO_2-based devices are less sensitive to irradiation or bias with thinner dielectrics, the present study is, as yet, unable to precisely estimate the irradiation effect for real applications devices having thinner gate dielectrics. Therefore, more future work will be needed to identify with certainty the radiation-induced charge trapping behavior in HfO_2 gate dielectrics and its dependence on the dielectric thickness.

The radiation response of Ge MOS capacitors with $Hf_xZr_{1-x}O_y$ ($0.43<x<1$) gate dielectrics under positive and negative bias was also examined. Gate leakage current density increased with the increasing of Zr composition in gate oxide, and decreased with the sulfur treatment of Ge surface. The density of negative oxide trapped charges increases in magnitude with increasing Zr composition in $Hf_xZr_{1-x}O_y$ during PB. Under NB, ΔN_{ot} of HfO_2 was larger than that of Zr-containing $Hf_xZr_{1-x}O_y$. In addition, the

difference of ΔN_{ot} between $Hf_{0.43}Zr_{0.57}O_2$ and $Hf_{0.6}Zr_{0.4}O_2$ was negligible. This implies that the concentration of oxygen vacancies and hole traps in Zr-containing $Hf_xZr_{1-x}O_y$ is not strongly dependent on Zr composition. More interface traps were generated in Zr-doped $Hf_xZr_{1-x}O_y$ compared to HfO_2 under PB, which suggests that ZrO_2 presented more hydrogen-related species than HfO_2. Under PBI, the Zr-doped $Hf_xZr_{1-x}O_y$ exhibited smaller ΔV_{FB} than that of HfO_2. This is attributed to the de-passivation of Ge-S bonds in capacitors incorporating HfO_2 thin films, resulting in the build-up of interface traps. Under NBI, ΔV_{FB} was dependent on the combined effect of the net oxide trapped charge and interface traps at the Ge/high-k interface. The ΔV_{FB} evaluated in HfO_2 Ge devices is much larger than that of the Si devices evaluated in our previous study. This can be explained by the large number of interface traps between the dielectric and the Ge substrate. This work demonstrated that $Hf_xZr_{1-x}O_y$ may be a promising candidate for space microelectronics under specific bias conditions. However, it is quite challenging for Ge devices in the biased radiation environment, future work will be required to identify the radiation hardness of these devices.