Atomic Layer Deposition of Tantalum Doped Aluminium Oxide as a Gate Dielectric for GaN-based Power Transistors

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Conferences and publications

- T. Partida-Manzanera, T.N. Bhat, Z. Zhang, H.R. Tan, S.B. Dolmanan, S. Tripathy and R.J. Potter. **Atomic Layer Deposition of high-κ Ta-doped Al_2O_3 layers as Gate Dielectric for AlGaN/GaN High Electron Mobility Transistors on 8-inch Si(111) Substrate.** Oral presentation in the AVS Topical Conference on Atomic Layer Deposition 2014, Kyoto (Japan), June 2014.

- T. Partida-Manzanera, T.N. Bhat, Z. Zhang, H.R. Tan, S.B. Dolmanan, S. Tripathy and R.J. Potter. **Atomic Layer Deposition of high-κ $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ Gate Dielectrics for InAlN/GaN High-Electron-Mobility Transistors on 8-inch Si(111) Substrate.** Poster presentation in the AVS Topical Conference on Atomic Layer Deposition 2015, Portland, Oregon (USA), June 2015.

- T. Partida-Manzanera, J.W. Roberts, T.N. Bhat, Z. Zhang, H.R. Tan, S.B. Dolmanan, N. Sedghi, S. Tripathy and R.J. Potter. **Comparative analysis of the effects of tantalum doping and annealing on atomic layer deposited $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ as potential gate dielectrics for $GaN/Al_xGa_{1-x}N/GaN$ high electron mobility transistors.** Journal of Applied Physics, Vol. 119 Issue 2, p.025303 (2016).

Abstract

The motivation for this research is to combine wide bandgap Al_2O_3 with high dielectric constant (high-κ) Ta_2O_5 for the development of a novel wide bandgap/high-κ gate dielectric material for next generation GaN-based high electron mobility power transistors (HEMTs). In this work, $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ thin films were deposited using atomic layer deposition (ALD) of Al_2O_3 with Ta modulation doping. Ellipsometry and scanning transmission electron microscopy (STEM) were used to analyse the films growth rates. X-ray diffraction (XRD) analysis shows that the films crystallisation temperature decreases with the Ta content, with a minimum crystallisation temperature of 750 ºC obtained for pure Ta_2O_5. X-ray photoelectron spectroscopy (XPS) reveals that the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers have good stoichiometry and their composition varies linearly with the ALD dopant cycle fraction. The bandgap of the oxide films obtained from XPS decreases linearly from 6.5 eV for Al_2O_3 to 4.6 eV for Ta_2O_5, while the dielectric constant calculated from capacitance-voltage (CV) measurements increases linearly from 7.8 to 25.6. The $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films are not affected by the post-deposition annealing step in N_2 at 600 ºC used for source/drain contact formation during HEMT processing, which gives the thermal and chemical stability needed for gate dielectrics applications.

A comparative analysis of the impact of Ta doping and annealing has been carried out for Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films grown on GaN/AlGaN/GaN and InAlN/GaN HEMTs. XPS shows a reduction of oxygen-related defects at the oxide/HEMT interface for all samples after annealing in N_2 at 600 ºC. As a result, the conduction band offsets (CBOs) of the Al_2O_3/GaN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT samples increase by ~ 1.1 eV to 2.8 eV and 2.6 eV, respectively, and the CBOs of the Al_2O_3/InAlN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT samples increase by ~ 0.7 eV and ~ 0.4 eV to

1.5 eV and 1.1 eV, respectively. AFM shows that the samples surface remains smooth after annealing. Cross-sectional STEM and high resolution transmission electron microscopy (HR-TEM) show uniform oxide film thickness with continuous and sharp oxide/HEMT interfaces before and after annealing and confirm that the introduction of Ta does not affect the thermal stability of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ film. Thus, the annealing step improves the samples interfacial properties by increasing the oxides barrier height to the HEMTs.

Finally, the electrical characteristics of GaN/AlGaN/GaN HEMTs have been analysed before and after the deposition of the ALD Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics. CV measurements show that, compared to the Schottky HEMT, the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs gate-source capacitance decreases and the threshold voltage absolute value increases, which results in a higher two-dimensional electron gas (2DEG) carrier concentration. Compared to the Al_2O_3 MOSHEMT, the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT achieves a higher capacitance and smaller threshold voltage absolute value, improving channel control and reducing switching losses, together with a higher 2DEG concentration. Superior direct current (DC) current-voltage (IV) and gate transfer characteristics are also observed for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT. From OFF-state measurements, the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT shows a smaller increase of the breakdown voltage and a bigger reduction of the gate leakage current in comparison to the Al_2O_3 MOSHEMT. The results demonstrate that ALD can be used to control the properties of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ as gate dielectric to achieve both a higher-κ compared to Al_2O_3 and a sufficient CBO to the GaN-based HEMT structure, providing superior electrical performance and lower gate leakage current while still improving the breakdown voltage with respect to Schottky HEMTs.

Contents

Notation

Symbol	Description	Units
a_0, a	Material lattice constants	
A	Area	(m^2)
A_i	Adjusted photoelectron intensity	(CPS.eV)
c_{13}, c_{33}	Material structure elastic constants	
C_{AlGaN}	AlGaN barrier capacitance	(F)
C_{AlN}	AlN spacer capacitance	(F)
C_{GaN}	GaN cap capacitance	(F)
C_{GS}	Gate-source capacitance	(F)
C_{ox}	Oxide film capacitance	(F)
D	Grain size	(Å)
d_{hkl}	Atomic spacing of the (*hkl*) planes	(Å)
D_{it}	Interface trap density	($cm^{-2}eV^{-1}$)
e_{31}, e_{33}	Material piezoelectric coefficients	(C/m^2)
E	Energy	(eV)
E_B	Binding energy	(eV)
E_{BR}	Breakdown electric field	(V/m)
E_{CNL}	Charge neutrality level	(eV)
E_{cr}	Critical electric field	(V/m)
E_F	Fermi level	(eV)
E_g	Bandgap	(eV)
E_i	Electrons recorded energy	(eV)
E_K	Kinetic energy	(eV)
E_p	Electric field component parallel to the plane of incidence	(V/m)
Es	Electric field component perpendicular to the plane of incidence	(V/m)
g_m	Transconductance	(S/m)
h	Plank constant	
I	Photo threshold energy	(eV)
I_D	Drain current	(A)
$I_{D,sat}$	Drain saturation current	(A)
I_G	Gate current	(A)
I_i	Measured photoelectron intensity	(CPS.eV)
I_S	Current between the source and the drain terminals	(A)
K	Shape factor	
k	Boltzmann's constant (in chapter 2)	
k	Material extinction coefficient (in chapter 3)	
N	Density of states	($charges/m^3$)
n	Material refractive index (in chapter 3)	

Symbol	Description	Units
n	Escape depth compensation exponent (in chapter 4)	
n	Number of ALD cycles (in chapters 4-6)	
N_d	Doping density	(charges/m^3)
N_{DIGS}	Volume density of DIGS	(charges/m^3)
n_{PDMAT}	Number of PDMAT based ALD cycles	
n_s	2DEG sheet carrier concentration	(cm^{-2})
N_{ss}	Net surface charge	(charges/m^2)
n_{TMA}	Number of TMA based ALD cycles	
$\boldsymbol{P}$	Polarisation along the (0001) direction	(C/m^2)
$\boldsymbol{P_{PE}}$	Piezoelectric polarisation along the (0001) direction	(C/m^2)
$\boldsymbol{P_{SP}}$	Spontaneous polarisation along the (0001) direction	(C/m^2)
Q	Charge	(C)
q	Thermal conductivity (in section 2.1.1)	(W/m^2K)
q	Electron charge (in section 2.1.4 and chapter 7)	(C)
R_a	Arithmetic average root mean square roughness	m
R_{ON}	ON-resistance	(Ω)
$R_{ON,sp}$	Specific ON resistance for a given area	(Ω·m^2)
r_p	Fresnel coefficient parallel to the plane of incidence	
r_s	Fresnel coefficient perpendicular to the plane of incidence	
S	Schottky pinning factor	
T	Absolute temperature	(K)
t_{ox}	Oxide film thickness	(m)
V_B	Breakdown voltage	(V)
V_{cr}	Critical voltage	(V)
V_{DS}	Drain-source voltage	(V)
$V_{DS,sat}$	Drain source saturation voltage	(V)
V_{fb}	Flatband voltage	(V)
V_{GS}	Gate-source voltage	(V)
V_S	Electron saturation velocity	(m/s)
V_{th}	Threshold voltage	(V)
W_G	Gate width	(m)
X_i	Percentage of atomic concentration	(at. %)
X_S	Semiconductor electron affinity	(eV)
β	Line broadening at peak FWHM	
Δ	Interfacial dipole (in chapter 2)	(eV)
Δ	Phase shift upon reflection (in chapter 3)	
ΔE_V	Valence band offset	(eV)
δ	Thickness of the disorder layer	(m)
ε	Permittivity	(F/m)
ε_o	Electric constant	(F/m)

Symbol	Description	Units
ε_r	Relative permittivity	(F/m)
ε_s	Semiconductor permittivity	(F/m)
θ	Diffraction or Bragg angle	(º)
κ	Dielectric constant	
λ	X-ray wavelength	(Å)
μ_n	Mobility of the electrons	(m^2/Vs)
μ_o	2DEG carriers field mobility	(m^2/Vs)
ν	Frequency of the radiation (in chapter 3)	(Hz)
ν	2DEG charge carrier velocity (in chapter 7)	(m/s)
ν_{sat}	2DEG charge carrier saturation velocity	(m/s)
σ_b	Positive bound polarisation charge	(charges/m^3)
Φ_B	Schottky barrier height	(eV)
Φ_s	Density of internal screening charge	(charges/m^3)
$\Phi_{S,CNL}$	Charge neutrality point with respect to the vacuum level	(eV)
ϕ	Work function	(eV)
ϕ_M	Metal work function	(eV)
Ψ	Amplitude shift upon reflection	

Acronyms

Acronym	Description
2DEG	Two-dimensional electron gas
AC	Alternating current
AFM	Atomic force microscope
ALD	Atomic layer deposition
Å	Angstrom
BE	Binding energy
BFTEM	Bright-field TEM
BJT	Bipolar junction transistor
C	Collector
CI	Confidence interval
CMOS	Complimentary metal-oxide-semiconductor
CNL	Charge neutrality level
CV	Capacitance-voltage
D	Drain
DC	Direct current
DI	De-ionised
DIGS	Disorder induced gap defect states
E	Emitter
EOT	Equivalent oxide thickness
FN	Fowler-Nordheim
FPE	Frenkel-Poole emission
FWHM	Full width at half maximum
G	Gate
HAADF-STEM	High-angle annular dark field STEM
HEMT	High electron mobility transistor
HR-BFTEM	High resolution cross-sectional bright-field TEM
HRXRD	High resolution XRD
IC	Integrated circuit
ICP	Inductively coupled plasma
IGBT	Insulated gate bipolar transistor
IV	Current-voltage
JCPDS-ICDD	Joint Committee on Powder Diffraction Standard-International Center for Diffraction Data
LDA	Local density approximation
LED	Light-emitting diodes
MFC	Mass flow controllers
MIGS	Metal-induced gap states
MOCVD	Metal-organic chemical vapor deposition
MOS	Metal-oxide-semiconductor

Acronym	Description
MOSFET	Metal-oxide-semiconductor field effect transistor
NIR	Near infrared
PL	Photoluminescence
PZT	Piezoelectric transducers
RF	Radio frequency
RIE	Reactive ion etching
RMS	Root mean square
RTA	Rapid thermal annealing
RTP	Rapid thermal processing
S	Source
SBH	Schottky barrier height
SE	Spectroscopic ellipsometry
SSF	Scofield sensitivity factors
STEM	Scanning transmission electron microscopy
TAT	Trap-assisted tunnelling
TE	Thermionic emission
TEM	Transmission electron microscopy
TFE	Thermionic field emission
TFEL	Thin film electroluminescence flat panel displays
TLM	Transmission Line Model
TMA	Trimethylaluminium
TSB	Thin Schottky barrier
TXFN	Transmission functions
UV	Ultraviolet
V	Voltage
VBO	Valence band offset
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction analysis

1. Introduction

1.1. Motivation for this thesis

Due to their superior material properties, group III-nitride semiconductors have attracted much attention in the past few years as candidates for next generation high-frequency, high-power and high-temperature power switching devices. Power transistors are used in almost all consumer electronics today, with applications ranging from power generation and transmission to the conversion of mains voltages down to end-user low voltages. The efficiency of current Silicon (Si)-based devices shows limitations related to Si voltage blocking capability, operation temperature and switching frequency. Gallium Nitride (GaN)-based devices have the potential to overcome these limitations due to the wide bandgap, high breakdown voltage, high electron saturation velocity, high electron mobility and high thermal conductivity of GaN.[1, 2] Furthermore, GaN-on-Si technology offers a cost effective route towards commercially viable high-performance GaN-based power electronics. Recent advances are now allowing the successful growth of high quality GaN-based epitaxial layers on top of large area Si substrates despite the large lattice mismatch and thermal expansion coefficient mismatch between GaN and Si.[3-7]

Among GaN devices, AlGaN/GaN high electron mobility transistors (HEMTs) are the most prevalent for power device applications due to the superior transport properties provided by the highly conductive two-dimensional electron gas (2DEG) formed below the AlGaN/GaN interface. This is a result of the difference in bandgap of the two materials and spontaneous and piezoelectric polarisation effects.[8, 9] The second structure of interest for power devices applications are the InAlN/GaN HEMTs. InAlN/GaN HEMTs have become

a new research topic of interest in the last decade as alternative to AlGaN/GaN HEMTs due to their superior power capabilities.[10, 11] InAlN/GaN heterostructures have two main advantages over AlGaN/GaN heterostructures. Firstly, the larger bandgap difference and larger spontaneous polarisation charge at the InAlN/GaN interface allow higher 2DEG sheet current densities.[12] Secondly, $In_{0.17}Al_{0.83}N$ and GaN are lattice matched and therefore there are no mechanical constrains in the epitaxial structures, which are believed to be the origin of trapping centres that strongly affect device performance.[13, 14] One of the main limitations of these GaN-based HEMT structures is the high gate leakage current caused by a low Schottky barrier height,[15] and/or poor interface quality between the gate metal and the nitride.[16] To address this problem, wide bandgap/high dielectric constant (high-κ) materials have been investigated as gate dielectrics for metal-oxide-semiconductor HEMT (MOSHEMT) structures.

Due to its self-limiting behaviour, atomic layer deposition (ALD) meets the needs for the deposition of very thin, conformal and highly insulating high-quality gate oxides in the sub-nanometre range for power electronic devices. In addition to this, the ALD process is not limited by the substrate area size and it can be integrated with GaN-based device processing of 200 mm GaN-on-Si wafers in a standard Si complimentary metal-oxide-semiconductor (CMOS) foundry. In literature, wide bandgap high-κ oxides such as Al_2O_3,[17-20] HfO_2,[21-23], ZrO_2[23, 24] and Ta_2O_5[25] deposited by ALD have been used to mitigate high gate leakage currents in GaN-based MOSHEMTs. Among these, ALD Al_2O_3 is one of the most widely investigated candidates as gate dielectrics for GaN-based devices due to its large bandgap (6.5 eV),[26] large breakdown electric field (5-10 MV/cm)[27] and ease of deposition. However, its dielectric constant (κ~9)[28] is relatively low compared to other high-κ oxides. For this reason, the introduction of a higher dielectric material such as Ta_2O_5, with a dielectric constant typically around 25 for amorphous Ta_2O_5,[29] may allow a further

reduction of the gate leakage while maintaining or enhancing the device gate capacitance. Compared to traditional dielectric materials such as HfO_2 and ZrO_2, Ta_2O_5 has shown better device performance due to its higher dielectric constant, as well as comparable gate leakage current despite its lower bandgap.[24, 25] Ta_2O_5 is a key high-κ material for next generation MOS due to its high breakdown electric field (4.5 MV), low leakage current (< 10^{-8} A/cm^2 at 1 MV/cm) and good step coverage.[30-32] Moreover, Ta_2O_5 used as gate dielectric in capacitors fabricated on GaN has shown low fixed oxide charge density and low midgap interface trap density.[33] However, the higher κ value of Ta_2O_5 compared with Al_2O_3 comes at the expense of a smaller bandgap (~ 4.4 eV)[34, 35] and hence lower band offsets which can reduce the barrier height with GaN, which is necessary for the prevention of carrier leakage. To achieve a high driving current capability, the gate dielectric must have a sufficient conduction band offset (for n-type MOS devices) or valence band offset (for p-type MOS devices) to the underlying semiconductor in order to ensure a significant barrier height for low leakage currents. Small band offsets can result in high leakage due to Schottky emission over the barrier and due to enhanced Fowler-Nordheim tunnelling at high voltages. Furthermore, from a device application point of view, one of the most challenging requirements for the integration of high-κ oxides as gate dielectrics is the chemical and thermal stability of the oxide film at the interface with the underlying semiconductor and the control of interface trap defects. In the case of gate-first HEMT technology where high temperature annealing steps are required for source/drain contact formation during device processing, it is important to understand the effects of post-deposition annealing in the gate oxide and its interfacial properties at the nitride surface. Band offsets are important parameters to understand the properties of the gate oxide/semiconductor interface. Changes in the band offsets between high-κ oxides and GaN due to band bending after annealing have been reported.[36] These changes can affect device performance especially if the

resultant band offsets are smaller than 1 eV.[37] In addition, the lower crystallisation temperature of Ta_2O_5 can result in the re-crystallisation of the gate oxide during post-deposition annealing processing at temperatures above 600 ºC,[37, 38] inducing high leakage currents due to grain boundary conduction. Previous research has been carried out on the band offsets of Al_2O_3 and Ta_2O_5 on GaN,[36, 39, 40] and between Al_2O_3 and InAlN.[41] However, there are no reports on the characteristics of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films on GaN/AlGaN/GaN HEMT or InAlN/GaN HEMT structures. To optimally combine the complementary characteristics of Al_2O_3 and Ta_2O_5, ALD with delta doping is used in this thesis to grow $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers as a novel gate oxide for GaN-based HEMTs.

1.2. Contribution of this thesis

This thesis presents for the first time a systematic study on the growth of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers as a new gate dielectric material for GaN-based MOSHEMTs. ALD of Al_2O_3 with Ta modulation doping is used for the deposition of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers in order to control key material parameters such as bandgap and dielectric constant as a function of the Ta content.

A detailed study on the correlation between the ALD doping ratio and the crystallisation temperature, thickness, refractive index and composition of the oxide layers is presented, together with the impact of post-deposition annealing on these properties. This is followed by an investigation of key materials parameters such as bandgap, dielectric constant and band offsets of the oxide films on GaN as a function of the Ta_2O_5 molar fraction before and after post-deposition annealing. This investigation is used to optimally combine the wide bandgap of Al_2O_3 with the high dielectric constant of Ta_2O_5 and study the effects of Ta doping and annealing on the surface, interface, band alignment and thermal stability of

undoped Al_2O_3 and Ta-doped $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films grown on GaN/AlGaN/GaN and InAlN/GaN HEMT structures. Finally, the electrical characteristics of GaN/AlGaN/GaN HEMTs are analysed before and after deposition of ALD Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films as gate dielectrics to evaluate the effect of the introduction of the gate oxides on the performance of the devices.

The results demonstrate that ALD with modulation doping can be used to optimise the properties of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ gate dielectrics to achieve both a high-κ and a sufficient conduction band offset to the GaN-based HEMTs for low leakage currents, high breakdown voltages and superior electrical performance.

1.3. Overview of this thesis

In order to provide the context and motivation for the work presented in this thesis, the first section of the literature review in chapter 2 covers the theory related to power electronics and power semiconductor switching devices, including the requirements for power switching devices and the benefits of the use of GaN as a new semiconductor material to enhance the efficiency of power electronic systems. The second section summarises the state of the art research on GaN-based power electronic devices and the current understanding of the role of oxide/GaN interface electronic states on the gate leakage current and current collapse mechanisms that affect the performance of these devices. Finally, the last section gives an overview on the ALD process and the advantages of the use of ALD for the growth of gate oxides, together with a review of current research on high-κ oxides grown by ALD as gate dielectrics for GaN-based power devices.

Chapter 3 covers the experimental techniques and equipment used during the present project. Due to the joint nature of this PhD, the experimental work was conducted at two different places: the University of Liverpool in the UK and the A*STAR Institute of Materials, Research and Engineering (IMRE) in Singapore. The ALD of the oxide films and the post-deposition annealing treatments were carried out at the University of Liverpool during the first year and a half and the fourth year of this PhD, together with some of the characterisation techniques such as ellipsometry, x-ray diffraction analysis, photoluminescence spectroscopy and capacitance-voltage and current-voltage measurements. Other techniques such as rapid thermal annealing processing, x-ray photoelectron spectroscopy, atomic force microscopy and transmission electron microscopy were performed at IMRE during the second half of the second year and the third year of this PhD. On the other hand, the fabrication and electrical measurements of the MOSHEMTs analysed in this thesis were carried out at the University of Sheffield during the fourth year. Unless otherwise specified, all the experimental data collection and analysis was performed by myself.

Chapters 4-7 cover the experimental work conducted for this thesis. Chapter 4 investigates the growth of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ thin films deposited by thermal ALD of Al_2O_3 with Ta modulation doping as potential gate dielectrics for GaN-based power electronics. The crystalline structure, optical properties and composition of the oxide layers are studied as a function of the ALD dopant cycle fraction, together with the impact of post-deposition annealing on these properties. Chapter 5 analyses the electronic and dielectric properties of the ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films as a function of the x molar fraction, before and after the post-deposition rapid thermal annealing in N_2 at 600 ºC used during gate-first HEMT technology processing. Chapter 6 presents a comparative analysis of the effects of annealing in N_2 at 600 ºC on the interfacial properties and thermal stability of undoped

Al_2O_3 and Ta-doped $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ grown on GaN/AlGaN/GaN HEMT and InAlN/GaN HEMT structures. Chapter 7 evaluates the electrical characteristics of GaN/AlGaN/GaN HEMTs before and after the introduction of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics.

Finally, chapter 8 outlines possible further experimental work required to achieve a better understanding of the oxide/HEMT interface and its role on MOSHEMT device performance.

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2. Literature Review

2.1. Power electronics

2.1.1. Introduction to power electronics

Power electronics technology is associated with the control and conversion of electric power using solid-state electronic devices. Power electronic systems are present in almost all the electrical and electromechanical equipment today and their applications cover all stages of power supply: generation, transmission, distribution and end-user power consumption. For example:

- AC/DC converters (or rectifiers) are used to transform the high voltage alternating current (AC) power from the grid to low voltage direct current (DC) power needed in consumer electronics (computer, mobile phones, television, etc.) by adjusting voltage and current whenever an electronic device is connected to the mains.[1]
- DC/AC converters (or inverters) are used to convert DC electricity (such as the power generated by solar cells) into AC power to be connected to electrical appliances or to the power grid.[2] They are also used to produce AC electricity at mains voltage from the DC battery in uninterruptible power supply (or UPS) or renewable energy systems if the mains fails.[3]
- AC/AC converters are used to control the voltage, frequency and phase of the waveform applied from a supplied AC system to a load. They can be classified into two main categories depending on whether the frequency is changed. AC/AC voltage controllers (or AC regulators) control the heating loads or speed of motors with increasing torque load (industrial fans, winding machines, etc.) without changing the

frequency. AC/AC frequency converters change the AC frequency, phase, magnitude or power in international power adapters.[4]

- DC/DC converters are used to maximise the energy collected from solar photovoltaic or wind turbine systems. They are also used in most mobile devices (mobile phones, personal digital assistant (or PDA), etc.) to maintain the voltage at a fixed value independently of the level of battery.[5]

The key element of the electronic circuits used for power electronics is the power transistor, which is a semiconductor-based device used as a switch. Current power semiconductor switching devices are based on silicon (Si) technology. Si-based power devices have been used for the last five decades since the introduction of the first solid-state power switch in 1957: the silicon controlled rectifier (SCR).[6] However, they are reaching their theoretical limits of performance in terms of efficiency, as determined from intrinsic material properties such as bandgap, critical field, electron mobility and thermal conductivity. According to the latest report by the International Energy Agency (IEA), 'end use efficiency' is intended to be responsible for 49 % of the total worldwide CO_2 emission reduction by 2030.[7] Hence, high efficiency power electronic devices will play a major role in improving 'end use efficiency' and reducing energy loss and energy usage worldwide in the 21st century. For this reason, there is great commercial interest that motivates the research and development of power transistors using new semiconductors that would enhance their performance for higher energy efficiency systems.

Semiconductors such as gallium nitride (GaN), silicon carbide (SiC) and diamond are currently under research to replace Si due to superior material properties such as high breakdown voltages provided by their wide bandgaps.[8-11] Table 2.1 below shows a comparison of the material properties for Si, SiC, GaN and diamond. GaN and SiC present the better trade-off between theoretical characteristics and maturity of their technological

processes as they are currently undergoing a transition from research to commercial release.[12] The high critical field of both GaN and SiC relative to Si is a property that allows these devices to operate at higher voltages and lower leakage currents. In addition, the higher electron mobility and electron saturation velocity of GaN compared to SiC allow higher operation frequency which means that GaN devices are better for very high frequencies, whereas the higher thermal conductivity of SiC compared to GaN means that the material is superior in conducting heat more efficiently and that SiC devices can theoretically operate at higher power densities. The relationship between semiconductor properties and device performance will be explained in more detail in section 2.1.4. On the other hand, diamond is the ultimate candidate for next generation power devices due to unrivalled properties such as high breakdown voltage, high thermal conductivity and high electron mobility, which can potentially push the performance of the devices even further in terms of operating frequency, power handling capacity, operating voltage, and operating environment.[13] However, diamond technology is still in its early stages of research. There are still several challenges to overcome before diamond power devices can contribute to the global CO_2 reduction plan, such as the fabrication of large diameter wafers with low dislocation density and low resistivity.[14]

TABLE 2.1. Material properties of Si, SiC, GaN and diamond.[8-11]

Material property	**Si**	**SiC**	**GaN**	**Diamond**
Bandgap, E_g (eV)	1.1	3.3	3.4	5.5
Breakdown electric field, E_{BR} (MV/cm)	0.3	3.5	3.3	10
Electron mobility, μ_n (cm^2/Vs)	1500	650	2000	2200
Electron saturation velocity, V_S ($x10^6$ cm/s)	10	20	25	8
Thermal conductivity, q (W/cm K)	1.5	5	1.3	20

2.1.2. Semiconductor theory

Bandgap

According to quantum mechanical theory, the atomic orbitals of the outermost electrons in a solid form energy bands that consist of a series of closely spaced discrete energy levels with allowed energy states for electrons wherein electrons may move.[15] Due to the finite widths of the energy bands, there are ranges of energy not covered by any band with forbidden energy states for electrons called bandgaps.[15] Depending on the distribution of the energy bands and the bandgap between them, solids will have different conduction properties. According to this, they can be classified as: conductors or metals, semiconductors and insulators.[15]

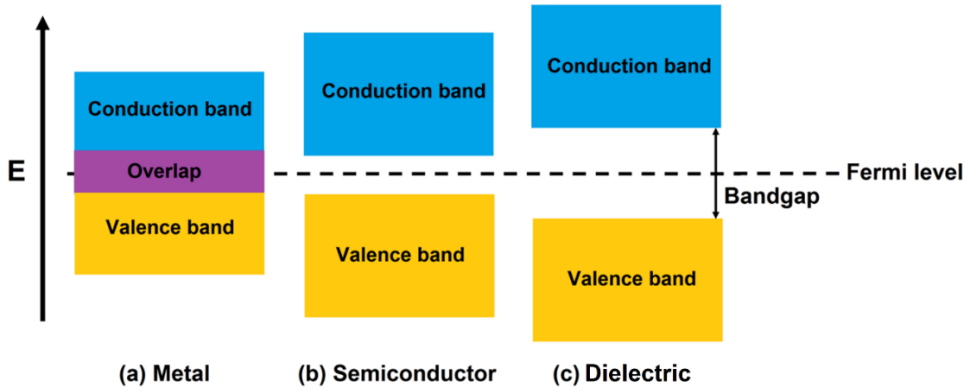

FIG. 2.1: Energy bands in solids.

Figure 2.1 shows a plot of the valence and conduction bands of available energies for electrons in metal, semiconductor and dielectric materials. According to the Pauli exclusion principle,[15] electrons fill energy levels in order from the lowest to the highest level of the valence band. Valence electrons can move from atom to atom by swapping places with other valence electrons in neighbouring atoms. The availability of conduction electrons determines the conductivity of the material. In conductors like metals, the valence band overlaps with the conduction band and valence electrons are free to move to the conduction

band with no additional energy provided. In semiconductors and insulators, the valence band is separated from the conduction band by an energy gap. For semiconductors the gap between the valence and conduction bands is narrow, whereas for insulators the bandgap is relatively wide. Electrons in the valence band require an energy equal or bigger than the bandgap energy to be promoted into the conduction band. This energy can be provided by different mechanisms such as thermal energy (phonons). Thus, the smaller the bandgap, the higher the probability that a valence electron will be promoted into an energy state within the conduction band at a given temperature, giving rise to an enhanced conductivity.[15]

Fermi level

In quantum mechanics,[15] the Fermi level (E_F) defines the highest energy level that an electron can reach or occupy in a material at absolute zero. At higher temperatures, the thermal energy is continuously exciting electrons within the band and a fraction of the electrons will exist above the Fermi level. The position of the Fermi level in relation to the conduction band is a crucial factor in determining the electrical properties of a material. At higher temperatures, a larger fraction of electrons have energies above the Fermi level and the gap between the Fermi level and the conduction band is smaller. Consequently, a larger number of electrons can bridge this gap participating in electrical conduction.

Conduction in semiconductors

If enough electrons are excited into the semiconductor conduction band at room temperature, they can be accelerated in the presence of an electric field, participating in the conduction process.[15] Electric current arises from the flow of these electrons with energies greater than the Fermi energy (named free electrons) in response to the forces that act on them from an externally applied electric field. Since electrons are negatively charged particles, they move in a direction opposite to that of the field. The electrical conductivity

is a direct function of the number of free electrons. According to quantum mechanics, there is no interaction between an accelerating electron and atoms in a perfect crystal lattice and thus all the free electrons should accelerate as long as the electric field is applied, which would give rise to a continuously increasing electric current with time. However, imperfections in the crystal lattice cause the scattering of electrons. Each scattering event causes an electron to lose kinetic energy and to change direction. The resultant net electron motion in the direction opposite to the field is the electric current, which reaches a constant value when a field is applied.[15]

2.1.3. Power semiconductor devices

Power semiconductor devices are used in power electronics as an ON/OFF switches. A power electronic switch can be represented as a three terminals device: the input, the output and a control terminal which imposes the ON/OFF conditions on the switch. The characteristics of an ideal switch are:[16]

- When the switch is in ON-state (forward-biased), the voltage across the end terminals of the switch is zero and it can carry infinite current flowing through.
- When the switch is in OFF-state (reverse-biased), it has zero current through and it can handle infinite voltage.
- The transition between the ON-state and the OFF-state (or switching) takes zero time.

In practice, power switches are not ideal and have limitations in all these characteristics. For example, when a switch is in ON-state it has some voltage across known as the ON voltage, carrying only a finite current. When the switch is in OFF-state, it also carries a small current known as the leakage current while supporting a finite voltage. The transition between ON/OFF and OFF/ON takes time and does not happen instantaneously. As a

consequence, there is voltage and current across the switch at all times. This results in two types of losses: (1) conduction losses which occur during the ON and OFF-states and (2) switching losses which occur just as the switch changes state as either opening or closing.[16]

Switches with the capability of handling high voltage and current operations at high frequency are needed for power electronics. Therefore, the design of a power switch is a trade-off between performance in the ON-state, OFF-state and switching. As the requirements for the ON and OFF-states are completely opposite (i.e. the same area of the device must sustain the OFF-state blocking voltage and allow current flow in the ON-state) a power switch has to be optimised to minimise the conduction losses. In addition to this, any increase in switching speed is also desirable to reduce the switching losses.

As power switch technology advances to reduce the total power loss and to enhance the efficiency of power systems, next generation power semiconductors switching devices have two strong Si competitors: the metal-oxide-semiconductor field effect transistor (MOSFET)[17] and the insulated gate bipolar transistor (IGBT).[18]

Enhancement mode power MOSFET

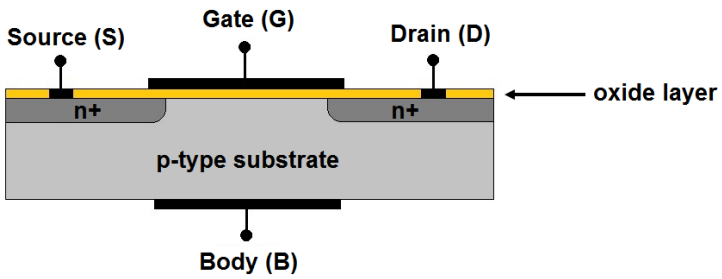

FIG. 2.2: Schematic of the cross section of an n-type MOSFET.

A power MOSFET is a four terminal device which operates by applying a signal to the gate (G) terminal that controls current conduction between the source (S) and the drain (D) terminals.[17] According to the carrier involved in the channel flow, there are two varieties

of MOSFETs: n-type MOSFET composed of a p-type substrate and n+ doped source and drain (Fig. 2.2) and p-type MOSFET with the reverse polarity scheme.[17]

The basic structure of a conventional silicon MOSFET[17] consists of a layer of silicon dioxide (SiO_2) on top of a doped silicon substrate with two highly conductive regions at its opposite ends (the source and the drain terminals). The region between the source and the drain is where the current flows and is known as the transistor channel, allowing the current to pass close to the substrate surface. A third electrode (the gate terminal), which consists of an electrical metal contact usually made from polysilicon, is sitting on top of the SiO_2 film, which electrically insulates the transistor body from the gate terminal to which the input signal is applied. The MOSFET therefore operates as a conducting semiconductor channel between the source and the drain in which the current flow is modulated by the MOS capacitor formed between the body and the gate. Due to the high isolation between input and output, the MOSFET is a nearly ideal switch element in which the voltage on the gate terminal turns ON or OFF the flow of current through the transistor channel.

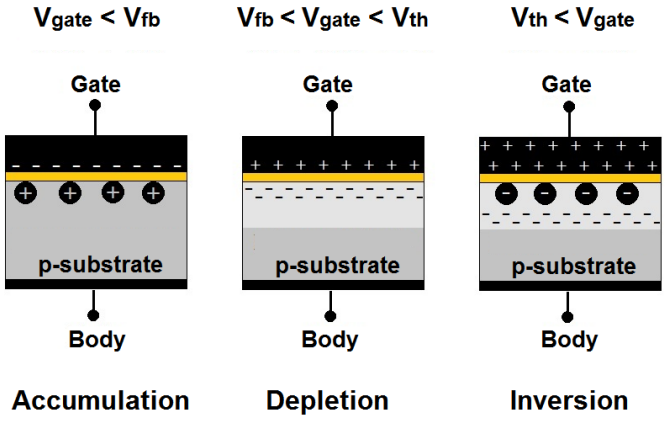

FIG. 2.3: MOSFET operation modes.

There are three distinct voltage regions in the MOSFET operation: accumulation, depletion and inversion (Fig. 2.3).[17] In an n-type MOSFET, the p-type substrate is very lightly doped, and so it has a very high electrical resistance and current cannot pass between

the source and drain if there is zero voltage on the gate. When a bias voltage is applied to the drain without a gate bias, the junction between the n^+ drain and p-substrate becomes reverse biased and no current flow transpires between the source and the drain. If a negative voltage is applied to the gate (smaller than the flatband voltage, V_{fb}, or voltage at which there is no electrical charge in the semiconductor) positively charged holes in the substrate are attracted creating a positive charge accumulation region under the gate insulator. The dielectric oxide layer prevents the holes from reaching the gate and hence they build up at the oxide-semiconductor interface. When a positive voltage is applied on the gate (bigger than the V_{fb}) a strong electric field is set up across the oxide layer. Since the gate electrode is positively charged, the holes in the semiconductor nearest the gate area are repelled into the p-substrate, creating a depletion region with fixed negative charges under the oxide layer. At even more positive voltages, a negative charge inversion layer starts forming at the top of the depletion region by the minority carriers (electrons) that are attracted to the surface. The gate voltage that corresponds with the transition between the depletion and the inversion regime is called the threshold voltage, V_{th}. When a bias voltage is then applied between source and drain, current is allowed to flow through the inversion layer. The V_{th} therefore separates the OFF-state and ON-state of the transistor. A p-type MOSFET works in the opposite manner: a positive voltage on the gate cuts off the flow of current.

IGBT

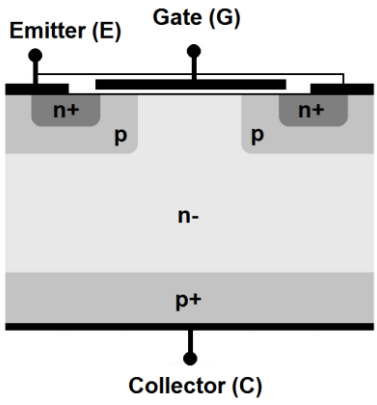

FIG. 2.4: Schematic of the cross section of an n-channel IGBT.

The IGBT is a three terminal device which combines the insulated gate input technology of the power MOSFET with the output performance characteristics of the conventional bipolar junction transistor (BJT).[18] The BJT is a transistor that uses both electron and hole charge carriers by using two junctions between n-type and p-type semiconductors and forming PNP or NPN semiconductor structures.[18] Bipolar transistors work as current-controlled current regulators in which a small current controls the main current (or controlled current) that goes from collector to emitter (in PNP-type transistors) or from emitter to collector (in NPN-type transistors).[18]

The basic structure of an IGBT[18] is similar to an n-channel vertical power MOSFET, but the n^+ drain is replaced with a p^+ collector layer which forms a vertical PNP BJT with the surface n-channel MOSFET (Fig. 2.4). The n^+ layer at the top is the source or emitter and the p^+ layer at the bottom is the drain or collector. The gate terminal controls the current path between the emitter (E) and collector (C) terminals. As a result, the IGBT has the output switching and conduction characteristics of a bipolar transistor but is voltage-controlled like a MOSFET.

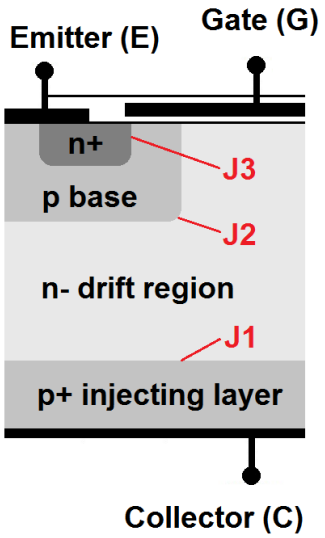

FIG. 2.5: Structure of an n-channel IGBT.

The principle of operation for the IGBT[18] is very similar to that of the n-channel power MOSFET. The basic difference is due to the p^+ collector layer which is responsible for the minority carrier injection into the n^- region and for the resulting conductivity modulation (Fig. 2.5). When the gate is externally shorted to the emitter, if a positive voltage is applied across the collector-to-emitter, the device enters into forward-blocking mode, and junctions J1 and J3 are forward-biased whereas junction J2 is reverse-biased. Under this condition a depletion layer is formed on both sides of junction J2 between the p base and the n^- drift region. When the gate-emitter shorting is removed, if a positive voltage big enough to invert the Si in the p base region below the gate is applied, the transition from the forward-blocking regime to the forward-conducting regime is achieved and a conducting channel through which electrons flow from the n^+ emitter to the n^- drift region is formed. This flow of electrons into the n^- drift lowers the potential of the n^- drift region, and junction J1 between the p^+ collector and the n^- drift becomes forward-biased. Under forward-bias, a high density of minority carrier (holes) is injected from the p^+ collector into the n^- drift region. When the injected carrier concentration is much larger than the background concentration, a condition defined as a plasma of holes builds up in the n^- drift region. This plasma of holes attracts electrons from the emitter contact to maintain local charge neutrality. As a result, approximately equal excess concentrations of holes and electrons are gathered in the n^- drift region. This excess concentration of electrons and holes drastically enhance the conductivity of n^- drift region, which is known as the n^- drift region conductivity modulation mechanism. Finally, if a negative voltage is applied across the collector-to-emitter terminal, junction J1 between the p^+ collector and n^- drift region becomes reverse-biased and its depletion layer extends into the n^- drift region.

IGBT vs MOSFET

The IGBT combines the fast switching of a MOSFET and the low power conduction loss of a BJT. The flow of electrons in IGBTs draws positive charges from the p-type substrate into the drift region, increasing the conductivity of the drift region significantly and enabling a dramatic reduction in the ON-state voltage. This conductivity modulation mechanism gives the IGBT a higher current density and capability compared to an equivalent MOSFET. As a result, the resistance of the main conduction channel when the current flows through the IGBT in the ON-state is significantly smaller and the ON-state voltage drop is much lower in higher blocking voltage ratings. On the other hand, in MOSFETs only electrons flow during forward conduction and the switching speed is only limited by the rate of charge. The MOSFET can change to the ON-state faster than the IGBT. Therefore, MOSFETs are ideal for use in applications where high switching speeds are required. Historically speaking, IGBTs are usually preferred for high voltage, high current and low switching applications, whereas MOSFETs are preferred for low voltage, low current and high switching frequencies.[19]

2.1.4. Requirements for power switching devices

The key application requirements for power switching devices are: high-blocking voltage, high-power efficiency, high-switching speed and normally OFF operation. These application requirements are related to the device semiconductor material properties such as bandgap, breakdown field, carrier saturation velocity, carrier mobility or thermal conductivity, which have a major impact on the performance characteristics of the devices.

High-blocking voltage

The blocking voltage of a switch is the maximum voltage that can be applied across the switch in OFF mode. It corresponds to the breakdown voltage in a transistor, which is the voltage at which the semiconductor suffers irreversible damage, changing from insulating to conducting. The breakdown voltage is determined by the critical field of the semiconductor. The relationship between the breakdown voltage and the critical or breakdown field can be defined by the following equation:[20]

$$V_B = \frac{\varepsilon_s E_{cr}^2}{2qN_d} \tag{2.1}$$

where V_B is the breakdown voltage, E_{cr} is the critical or breakdown electric field, N_d is the n-type semiconductor doping density, ε_s is the semiconductor permittivity and q is the value of electron charge.

The critical field of a material is related to the strength of the atomic bonds, which is further related to the bandgap (materials with small atoms and strong atomic bonds are associated with wide bandgaps). For this reason, the critical field of Si is the limiting factor for applications that require high blocking voltages due to its lower bandgap, whereas the wider bandgaps of GaN and SiC correspond to higher critical fields which allow these devices to operate at higher voltages.[21]

High-power efficiency

One of the two main sources of power loss in power transistors is the switching loss when the device transitions between the ON and OFF states. The ON resistance offered for a given area when the device is turned ON determines the power loss and heating of the

device. However, this ON resistance is necessary to achieve high breakdown voltages, as given by the following relationship:[22]

$$R_{ON,sp} = \frac{4V_B^2}{\varepsilon_s \mu_n E_{cr}^3} \tag{2.2}$$

where $R_{ON,sp}$ is the specific ON resistance for a given area and μ_n is the mobility of the electrons.

Therefore, the relationship between the specific ON resistance and the maximum achievable breakdown voltage defines the limit of the material theoretical performance. The relative theoretical performance for Si, SiC and GaN is shown in Figure 2.6.

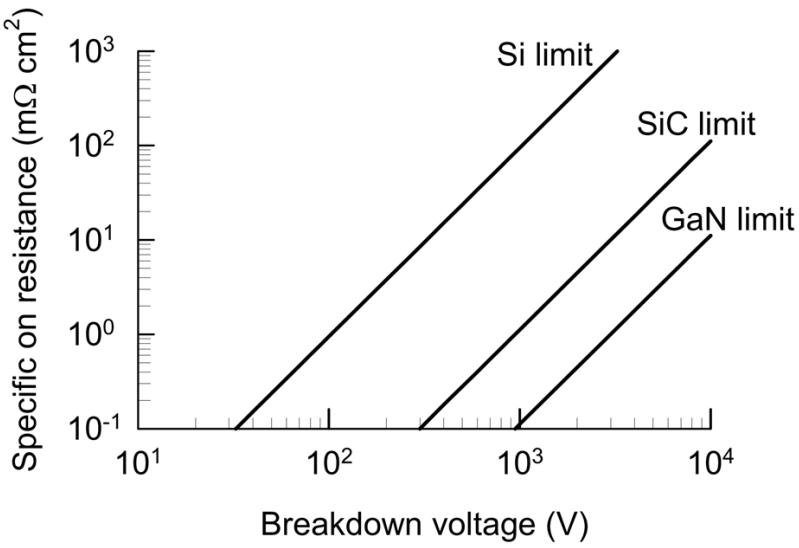

FIG. 2.6: Relationship between specific on resistance and the maximum achievable breakdown voltage for Si, SiC and GaN. Reprinted from Niiyama et al.[21]

It can be observed that, compared to Si, SiC and GaN have a superior relationship between the specific ON resistance and the breakdown voltage. For a given specific ON resistance, the breakdown voltages for SiC are ten times higher than for Si, and even higher in the case of GaN. This is due to their higher critical electric field, which demonstrates

that the critical field of Si limits the practical breakdown voltages that can be achieved by Si devices.

The second main source of power loss in power devices is the conduction loss that result from energy dissipation across the resistance of the conduction path as charge moves through the circuit when the device is in ON state. The ON resistance of the power device is inversely proportional to the cube of the electrical breakdown (Eq.2.2). Thus, higher critical electric fields provide a significant reduction of the device specific ON resistance for a given breakdown voltage, leading to a reduction in conduction losses. It is expected that SiC and GaN devices will have an ON resistance two and three orders of magnitude lower that the theoretical limit of Si devices, respectively.

High-switching speed

High breakdown voltages and low ON resistances allow high-speed switching and miniaturisation of the devices, which can significantly reduce the size and cost of power systems.[22] Due to their inferior relationship between the specific ON resistance and the breakdown voltage (Fig. 2.6), Si transistors require a bigger chip area to reduce the ON resistance for a given breakdown voltage requirement. On the other hand, the higher breakdown fields of SiC and GaN allow the use of smaller devices for a given breakdown voltage and ON resistance. This miniaturisation increases the transistor speed as the charges do not need to travel as far in smaller devices. Furthermore, the use of smaller devices reduces the transistor parasitic capacitance, which is the unwanted internal capacitance present in all circuit elements that causes their behaviour to differ from ideal circuit element behaviour, such as the junction capacitances created between the source or drain and the underlying substrate. This reduction in the parasitic capacitance improves the transistor switching speed causing lower switching losses.

In addition to the smaller device size, the higher electron saturation velocity of SiC and GaN (or maximum velocity an electron attains in a semiconductor in the presence of very high electric fields),[23] makes SiC and GaN devices more suitable for high-speed applications. Furthermore, GaN is characterised by a high electron mobility, which is the velocity an electron can move through a semiconductor when pulled by an electric field, making possible for GaN transistors to switch even faster.

Normally OFF operation

Power electronics rely on normally OFF devices to provide additional protection for the equipment and its users. A normally OFF operation switch is in OFF mode when no voltage is applied at the transistor gate electrode and it is turned ON when a voltage above the V_{th} is applied. If there is a failure in the circuit controlling the power device, a normally ON device could turn ON damaging the equipment and possibly injuring the user. Normally OFF transistors in which no current flows at 0 V are strongly desired for fail-safe operation as well as reduced power consumption.[21] Historically, the only device structure that could achieve this requirement is the enhancement mode MOSFET.[20] For this reason, MOSFETs are the dominating semiconductor device for power switching applications and complimentary metal-oxide-semiconductor (CMOS) technology for digital electronics.

2.1.5. Relative advantages of GaN vs SiC for power switching devices

GaN is particularly attractive over SiC in applications in the medium voltage market for voltage stresses below 1200 V.[24-26] The main advantage of GaN versus SiC at lower voltages is that GaN transistors are extremely cost effective when GaN is grown on a Si wafer and the wafer can be processed into active transistors in a standard Si CMOS foundry at a very low cost.[24] In addition to this, GaN has a significant advantage versus SiC in terms

of switching speed due to its superior relationship between specific ON resistance and breakdown voltage.[23] GaN has made inroads in power conversion applications requiring 600 V and below due to the higher conversion efficiency provided by the smaller size and higher switching speed of GaN devices compared to Si power MOSFETs (which are the dominant type of Si transistor at these voltages).[27, 28] These commercial power transistors using GaN are based on a structure that is known as the high electron mobility transistor (HEMT).[29] A review of GaN-based HEMTs will be presented in section 2.2.2.

The advantage of SiC over GaN at higher voltages comes from the structure of the device. At high voltages the transistor is more efficient when the current is conducted through the wafer, which requires the entire wafer to be made of a single crystal type. Since the cost of SiC crystals is much lower than the cost of GaN crystals today, SiC devices are fabricated on SiC substrates.[30] This is called a vertical device, in contrast to the lower voltage GaN HEMT transistor grown on other substrates which is a lateral device. SiC devices are finding success at voltages of 1200 V or higher. At high voltages, the switching frequency of a SiC MOSFET for the same power rating can be increased by around 10 times as compared to a Si IGBT (which is the dominant type of Si transistor at these voltages).[31] This can reduce the overall system cost by reducing the size of the passive elements, which makes a significant difference in industrial applications requiring high voltages.

2.2. GaN material for power devices

2.2.1. The potential of GaN for power electronics

The wide bandgap of GaN yields a significantly higher breakdown field which makes it very attractive for high-frequency, high-power and high-temperature power electronic

applications.[32, 33] GaN has been used in bright-light-emitting diodes (LED) since the 1990s. In 1991, Nakamura et al. presented the first high brightness GaN-based blue LED with an output power ten times higher than the conventional SiC blue LED.[34] Since then, GaN technology rapidly spread to electronic applications. However, its use in commercial power electronic devices has until recently been limited due to lack of commercially available large area GaN substrates and due to the costs of using GaN wafers as substrates for GaN-based devices.[35] For this reasons, GaN has usually been produced on SiC,[36] sapphire[37] or Si.[38] Table 2.2 compares the properties of these three substrates for GaN growth.

TABLE 2.2. Comparison of GaN epitaxy on common substrate materials.[39]

Material property	**SiC**	**Sapphire**	**Si**
Lattice constant mismatch (%)	3.1	15	17
Linear thermal expansion coefficient (10^{-6} K^{-1}) (GaN value = 5.6)	4.16 (*c*-axis)	7.5	2.6
Thermal conductivity (W/cm K)	3.8-4.9	0.25	1.56
Typical epitaxial GaN dislocation density (cm^{-2})	$< 10^8$	$< 10^8$	$< 10^9$
Cost	Expensive	Less expensive	Cheap

The production of high quality epitaxial GaN is challenging due to the difference in lattice parameters and thermal properties with respect to the substrates, which leads to high dislocation density and film stress issues. An ideal substrate material should have minimal lattice constant mismatch and thermal expansion coefficient mismatch with GaN as well as high thermal conductivity. Based on these desirable characteristics, SiC is the superior choice. However, when GaN is grown on SiC it exhibits a high density of defects and higher cost compared to the other substrates. For this reason, GaN-on-SiC is used for the fabrication of LEDs rather than for power electronic devices. The fact that the high density of defects did not seem to degrade the operation of GaN LEDs grown on SiC encouraged the development of power transistors for microwave applications. GaN-based HEMTs

grown on SiC appeared in 2004 and were successfully produced for the radio frequency (RF) market.[40] Sapphire substrates cost less than SiC but have larger lattice constant and thermal expansion coefficient mismatch, which set limits on the quality of the epitaxial GaN film.[39] Furthermore, sapphire has a much lower thermal conductivity, which can be a significant concern for high power devices.[39] For cost-sensitive applications, Si is the most attractive substrate among all options as GaN grown on SiC or sapphire may never reach device prices comparable to the Si products. Although the defect density of GaN grown on Si is higher due to the large lattice mismatch, the availability of large diameter Si substrates and the possible integration of GaN device processing in Si fabrication facilities significantly reduce the fabrication cost of a GaN epitaxial wafer.[41] In 2005, the first depletion mode RF-HEMT made with GaN on Si wafers was introduced.[42] GaN-based HEMTs grown on Si substrates have been developed and commercialised for various wireless RF applications since 2006, but their acceptance outside this market has been limited by device cost.[43]

With the successful growth of GaN on top of Si despite the large lattice mismatch and the thermal expansion coefficient mismatch, GaN-on-Si technology has emerged as the best alternative to the well-established but aged Si technology.[44] One of the main challenges for GaN-on-Si technology is the significant mechanical strain that epitaxial GaN films suffer due to the large lattice and thermal expansion coefficient mismatch between the substrate and the epilayers. This results in a high density of misfit and threading dislocations in the GaN layers, causing several types of electrically active defects that affect the device performance.[45] For example, defects such as edge and mixed type threading dislocations propagating from the bottom up to the surface can influence the buffer leakage current by creating parasitic conducting paths which lower the breakdown voltage.[46] These problems can be mitigated by precisely controlling the grading, composition and thickness of

intermediate aluminium gallium nitride (AlGaN) and aluminium nitride (AlN) buffer layers, which has enabled the growth of high quality GaN on Si wafers.[34, 47] In 2010, the first enhancement mode GaN transistors (eGaN FET) on silicon substrate were demonstrated.[38] The devices consisted of a thin layer of GaN grown on top of a silicon wafer and were designed as power MOSFET replacements to be produced in high volume at low cost using standard Si manufacturing technology and facilities, which allows GaN superior electrical performance while maintaining costs similar to Si MOSFETs.

Although the quality of GaN grown on Si is not yet as good as that on SiC and sapphire, large diameter Si substrates reduce dramatically the manufacturing costs for GaN devices making GaN-on-Si technology potentially competitive with existing Si and SiC technologies. Recent advances are now allowing the realisation of high quality GaN-based epitaxial layers on top of large area Si substrates.[48-50] In addition to the mechanical strain of epitaxial GaN, the growth of GaN on large area Si substrates is quite challenging due to thermal gradients across the wafer that lead to problems such as high wafer bowing, which causes non-uniform material properties and makes further device processing difficult.[51] However, the growth of GaN epitaxial layers with reduced bowing on cost effective Si substrates has recently been demonstrated using AlGaN/AlN buffer layers.[52-56] Although there are still challenges that need to be addressed for GaN-based HEMT structures on Si such as the presence of a high density of point and line defects and wafer bowing induced electrical inhomogeneities, the realisation of GaN-based HEMT structures on 8-inch Si wafers has been reported very recently.[57-61] 8-inch GaN-on-Si technology has emerged as a cost effective route towards the commercially viable high-performance GaN-based power electronics, offering the advantages of low-cost, large diameter wafers together with the integration of GaN heterostructures with the well-developed 8-inch Si microelectronics technology.

2.2.2. GaN-based power electronic devices

There are two specific GaN power switching device structures that have been investigated in the past fifteen years: the GaN MOSFET and the GaN HEMT (Figs. 2.7a and 2.7b, respectively). As previously mentioned in section 2.1.5, most of the commercial GaN devices available today are HEMTs (Fig. 2.7.b).[62] The HEMT is a field-effect-transistor that incorporates a heterojunction between two materials with different bandgaps as the conducting channel. The term 'high electron mobility' refers to the superior transport properties provided by the highly conductive two-dimensional electron gas (2DEG) induced at the heterojunction between GaN and a wider bandgap material such as AlGaN.

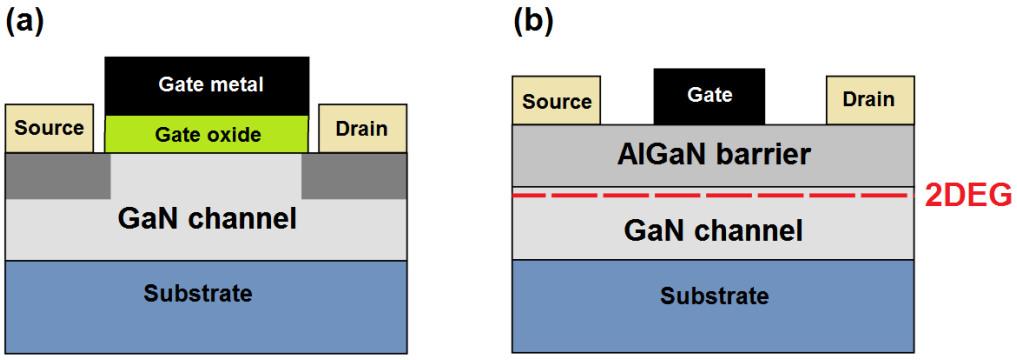

FIG.2.7: Cross-section of (a) GaN MOSFET and (b) AlGaN/GaN HEMT structures.

2.2.2.1. GaN HEMT

AlGaN/GaN HEMTs

Currently, the most prevalent HEMT structure is the AlGaN/GaN HEMT. The transition from GaN to AlGaN creates fixed and positive polarisation charge which attracts the electrons that create the channel,[63, 64] inducing a 2DEG at the GaN side of the heterojunction (Fig. 2.8c). The polarisation charge that forms the 2DEG in AlGaN/GaN HEMTs include spontaneous and piezoelectric polarisation (Fig. 2.8a). The spontaneous

polarisation refers to the built-in polarisation field present in Wurtzite III-V materials due to the intrinsic asymmetry of the bonding in this crystal structure. This results in a strong macroscopic polarisation along the [0001] direction, which makes the crystals 'naturally' distorted. This occurs in AlGaN and GaN crystals because both semiconductors have polar Wurtzite structure, but their spontaneous polarisations are not identical as a consequence of their different compositions. The piezoelectric polarisation results from mechanical stress due to the difference in lattice constant between AlGaN and GaN. Since the GaN lattice is 2.4% larger than the AlN lattice at room temperature,[65] the AlGaN layer is grown on a relaxed GaN buffer layer and therefore is biaxially strained, which contributes to a sheet charge on the two faces of the AlGaN layer.

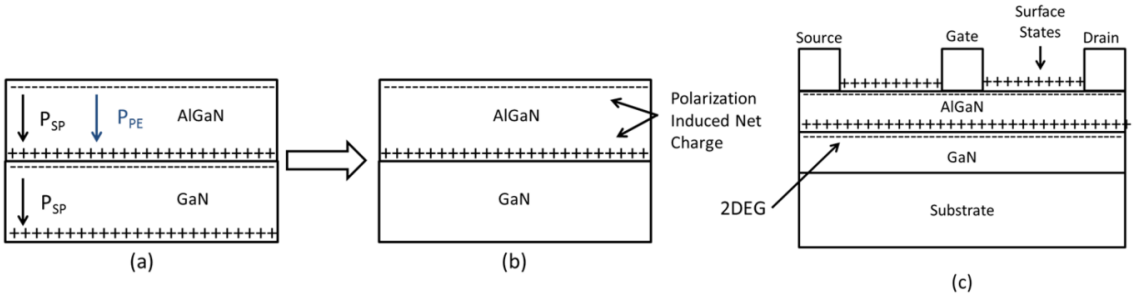

FIG.2.8: Structure of AlGaN/GaN showing (a) individual polarisation charge contributions, (b) polarisation induced net charge and (c) AlGaN/GaN HEMT with polarisation induced net charge and surface contributions. Reprinted from Jarndal et al.[66]

Figure 2.9. shows the band edge diagram of an AlGaN/GaN HEMT with Schottky gate. The net charge induced by polarisation alters the band diagram and the electron distribution at the heterojunction between the wide-bandgap AlGaN layer and the narrower bandgap GaN layer,[67] forming a sharp dip in the GaN conduction band. Electrons generated in the highly doped n-type AlGaN layer drop into the non-doped GaN channel forming a depleted AlGaN layer. The wider bandgap of AlGaN prevents the electrons from the channel leaking into the gate of the device. This results in a very high carrier concentration in a narrow

region (or quantum well) parallel to the surface under the AlGaN layer. The distribution of electrons in the quantum well is essentially two dimensional due to its very small thickness in comparison to the width and length of the channel. This is why it is known as two-dimensional electron gas or 2DEG.

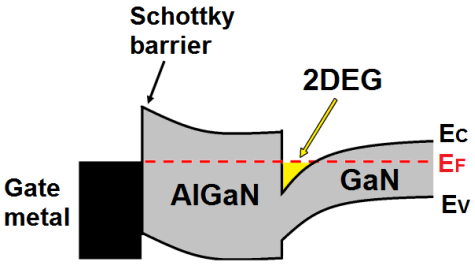

FIG.2.9: Band structure of an AlGaN/GaN HEMT with Schottky gate at equilibrium.

The basic principle of operation of the HEMT is similar to that of the MOSFET.[17] When a voltage is applied to the drain electrode with the source electrode grounded (V_{DS}), the current flowing between the drain and the source (I_D) is controlled by the signal applied to the gate terminal (V_{GS}). The majority of HEMTs are normally ON devices and thus, the V_{th} is negative and the current flows through the device without an external gate biasing ($V_{GS} = 0$). If a negative voltage is applied to the gate ($V_{GS} < V_{th}$), the depletion region starts to penetrate into the 2DEG, stopping the current flow. When the channel is completely depleted the device is in the pinch-off state. The drain current plotted over the drain voltage at a given gate voltage is known as the HEMT output characteristic (Fig. 2.10). When the drain and source contacts are biased at low voltages ($V_{DS} < V_{GS} - V_{th}$), the HEMT operates in a linear regime where the electron velocity is linearly related to the electric field strength (Fig. 2.10a). The drain current in the linear regime is dependent of the drain bias and the device's current-voltage characteristics can be modulated by the gate bias.[17] At high drain bias voltages ($V_{DS} > V_{GS} - V_{th}$), the effective electron velocity saturates and becomes independent of the drain bias or the electric field strength (Fig. 2.10b). As a result, the drain

current saturates. The gate voltage-controlled current saturation in power devices is a useful behaviour when switching because it allows limiting the current flow by the device and thus the power dissipation during switching.[17] For this reason, AlGaN/GaN HEMTs are typically operated in the saturation regime. Parameters such as the device's maximum drain current, ON-resistance and breakdown voltage can be extracted from the output characteristics. The HEMT transfer characteristic describes the drain current dependence on the gate voltage at a fixed drain voltage, usually in the saturation regime. An important parameter that can be obtained from the transfer characteristic is the transconductance. The transconductance is defined as the rate of change in drain current with incremental gate voltage,[17] and thus quantifies the ability to control the 2DEG channel. A large transconductance is desirable to obtain a high drain current with a small gate bias voltage.[17]

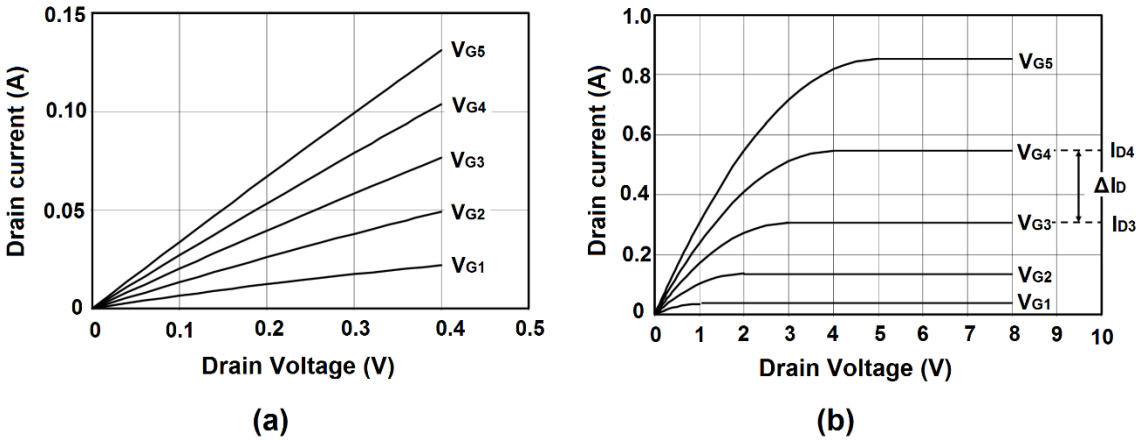

FIG.2.10: HEMT ideal characteristics at (a) low drain bias voltages and (b) high drain bias voltages.[17]

AlGaN/GaN HEMTs with low ON resistance and high breakdown voltage that break the Si limit have recently been fabricated.[68-72] The mobility in the channel of the transistor is almost 100 times higher than the mobility in the channel of SiC MOSFETs, which is a huge advantage in terms of the ability to achieve low ON resistance with much smaller area devices.[73] Extremely fast switching transients and low losses with a high conversion

efficiency of 97.8 % have been achieved with a high speed and low ON resistance GaN HEMT.[74]

InAlN/GaN HEMTs

Lately, InAlN/GaN HEMTs have become a new research topic of interest as alternative to AlGaN/GaN HEMTs for high-frequency power applications. The main advantage of the InAlN/GaN heterostructure is that the $In_xAl_{1-x}N$ alloy is lattice-matched with GaN when the In content is 17-18 %.[75, 76] This offers a strain-free barrier layer on GaN with a larger bandgap difference and larger polarisation-induced charge between the barrier and channel, which results in higher 2DEG carrier density.[77] Furthermore, compared to AlGaN/GaN HEMTs, lattice-matched InAlN/GaN HEMTs present reduced strain induced reliability issues, which are believed to be the origin of poor device reliability at high drive currents.[78] In addition, a high 2DEG electron density can be achieved with a thinner barrier layer, which can reduce the distance between the gate and the channel improving the gate modulation efficiency. This enables transistors to operate at higher frequencies for millimetre-wave applications.[79] Moreover, InAlN HEMTs have shown thermal stability at high operation temperatures.[80] Thus, strain-free InAlN/GaN HEMTs offer an alternative platform suitable for high current, high frequency and high temperature operations.

Limitations of GaN-based HEMTs

One of the main limitations of HEMTs is that they intrinsically show a negative threshold voltage that separates the ON and OFF states, which results in a normally ON type transistor. Since a negative gate voltage needs to be applied to turn the switch OFF, they need a drive circuit to control the gate bias. To solve this problem, commercial GaN HEMTs are connected with a Si MOSFET that provides the normally OFF operation whereas the GaN HEMT provides high-blocking voltage and low ON resistance.[27, 28] This

can result in increased circuit complexity and higher costs. The other major problem of GaN HEMTs is the high gate leakage current through the Schottky gate caused by a low Schottky barrier height and/or poor interface quality, which is the most limiting factor in the device performance of Schottky gate HEMTs.[81-87] To solve this problem, high dielectric constant materials such as high-κ oxides are currently being investigated as gate dielectric for metal-oxide-semiconductor HEMT (MOSHEMT) structures (Fig. 2.11).

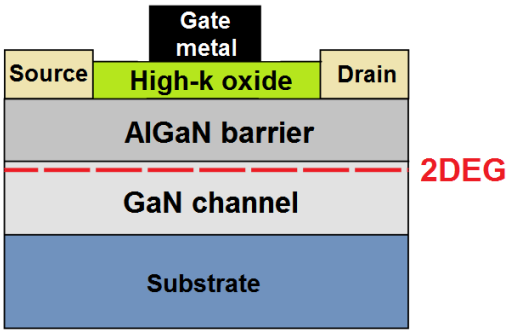

FIG. 2.11: Cross-section of the AlGaN/GaN MOSHEMT basic structure.

With the successful development of normally OFF GaN MOSHEMTs, GaN-based power devices have the potential to become the dominant device for power electronics due to their significant advantages in terms of power dissipation and cost.[88-91] However, there are still some issues that need to be addressed before GaN-based power electronics replace Si technology. In addition to the development of methods for the epitaxial growth of high-quality GaN on large area Si substrates, there is a need to minimise the interface states between the gate dielectric and the GaN substrate. The high density of defects at the dielectric/GaN interface results in a large leakage current and current collapse that can degrade device performance and reliability.[92-97] The nature of these states and their role in GaN-based devices are not yet fully established due to their complexity and therefore, an increased understanding of the mechanisms responsible for these reliability issues is required.

2.2.2.2. GaN MOSFET

Although GaN MOSFETs do not benefit from enhanced electron mobility due to quantum confinement in a 2DEG, they provide the capability of fabricating normally OFF devices with low gate leakage current and simple structure.[98] Compared to conventional Si MOSFETs, GaN MOSFETs can operate at much higher temperatures, provide lower ON resistance, lower leakage current and reduced power consumption.[99] However, the electron mobility of the GaN MOSFET channel is dramatically lower than that of the GaN HEMT, which increases the ON resistance and creates a challenge to achieve low conduction losses.[100] In order to compete with SiC MOSFET technology, significant efforts need to be done to fabricate GaN MOSFETs with high field-effect mobility and high breakdown voltages.[101] Very recently, GaN MOSFETs with the potential to rival state of the art GaN HEMTs have been reported. Improvement in the electron mobility has been obtained in GaN MOSFETs with aluminium oxide (Al_2O_3) gate dielectric by engineering the Al_2O_3/GaN positive interface fixed charges using post-dielectric annealing in nitrogen.[102] The high performance of GaN MOSFETs has been related to the good surface morphology and high Al_2O_3/GaN interface quality achieved using a wet etching-based gate recess technique.[103] Excellent device performance has also been demonstrated due to the high conduction band offset at the interface between the silicon oxide (SiO_2) gate oxide and the GaN channel.[104] Furthermore, due to the small capacitance equivalent thickness obtained using high-κ gate dielectrics and recessed-gate etching, enhancement mode n-channel GaN MOSFETs have been reported with dual dielectric composed of Al_2O_3 and hafnium oxide (HfO_2),[105] magnesium oxide (MgO) and hybrid MgO and titanium oxide (TiO_2) stacked gate dielectrics,[106] and lanthanum $LaAlO_3/SiO_2$ gate dielectric.[107] Therefore, the fabrication of candidates for switching devices in high-power applications can be achieved by engineering the gate dielectric and the dielectric/GaN interface charge of GaN MOSFETs.

2.2.2.3. Gate dielectrics for GaN-based devices

Dielectrics can be used in two ways to improve device reliability: as gate dielectric material under the metal gate to reduce gate leakage,[108, 109] and as passivation layer between the gate and the drain to attenuate current collapse.[105, 110] The two most important characteristics of a dielectric material are the dielectric constant, which refers to the ability of the material to concentrate an electric field when a voltage is applied, and the bandgap, which determines the confinement characteristics of the carriers.

When a dielectric material is placed in an electric field it reduces the field by becoming polarised: positive charges are displaced towards the field and negative charges shift in the opposite direction creating an internal electric field within the dielectric. The permittivity of the material expresses the ability to polarise in response to an applied field. The dielectric constant, or relative permittivity of a material to the permittivity of vacuum, represents the increase in charge storing capacity in a capacitor by insertion of the dielectric.[15] This is also related to the capacitance provided for a certain dielectric thickness, which in a MOS structure is given by the following equation:

$$C_{ox} = \frac{\varepsilon_r \varepsilon_o A}{t_{ox}} \tag{2.3}$$

where C_{ox} is the oxide capacitance, A is the area of overlap of the metal and the semiconductor, ε_r is the relative static permittivity or dielectric constant of the oxide material, ε_o is the electric constant and t_{ox} is the oxide thickness. Therefore, if a gate oxide has a higher dielectric constant, for a given voltage it will accumulate a bigger amount of charge drawing more charge into the transistor channel. As a result, materials with higher dielectric constant allow the physical thickness of the gate dielectric to be increased, reducing the current lost through the gate by electron tunnelling (or gate leakage current)

while maintaining or enhancing the capacitance density and increasing the device current driving capability.

In addition to the high dielectric constant, the gate dielectric material must have a sufficient conduction band offset (CBO) (for n-type devices) or valence band offset (VBO) (for p-type devices) with the semiconductor in order to allow carrier confinement. Larger bandgaps can give higher energy band offsets at the oxide/semiconductor interface, which results in reduced gate leakage current for the same dielectric thickness. Furthermore, there are other parameters to consider such as the crystal structure of the dielectric material. Amorphous materials are generally preferred to crystalline materials. Grain boundaries in polycrystalline materials serve as high-leakage paths,[111] reducing the effectiveness of the dielectric. On the other hand, single crystal materials often require high deposition temperature, which can cause interface reactions due to the thermodynamic instability, as well as consideration of the lattice mismatch between the semiconductor and insulator, which can result in a high concentration of structural defects at the interface.[111] Additionally, other properties that must be considered when selecting a dielectric material are: interface quality, thermodynamic stability, film morphology, compatibility with the materials used during device processing, process compatibility and reliability.[111]

Table 2.3 below summarises the dielectric constant, bandgap and interface trap density (D_{it}) obtained for several dielectrics considered as gate dielectrics and/or passivation layers for GaN-based devices. It should be noted that D_{it} is very sensitive to the processing and deposition conditions and thus the reported values vary. Additionally, comparing the performance of these dielectrics can be difficult due to the different surface pretreatments, dielectric deposition, device fabrication and post-deposition treatments used. In general, the studies demonstrate that oxides with larger bandgap are more effective in reducing the

leakage current. On the other hand, nitrides are the most effective dielectrics to mitigate current collapse. This is because current collapse is associated with defects at the GaN surface that are likely caused by either nitrogen vacancies or electric field driven oxidation from the atmosphere.[146]

TABLE 2.3. Comparison between the dielectric constant, bandgap and interface trap density (D_{it}) on GaN of several dielectrics.

Material	Ref.	κ	E_g (eV)	Use	D_{it} on GaN (cm^{-2} eV^{-1})	Comments
SiO_2	105, 112-116	3.9	8.9	Passivation	$(2.5\text{-}5.3)\cdot10^{11}$	Reduction of leakage and current collapse
SiN_x	110, 113-117	7.5	5.0	Passivation	$(0.5\text{-}9)\ 10^{11}$	Reduction of leakage and current collapse
AlN	110, 118, 119	8.5	6.2	Passivation	$< 1\cdot10^{11}$	Reduction of current collapse
GaN	120, 121	9.5	3.4	Passivation/ gate dielectric	-	Reduction of current collapse but not effective gate dielectric
Ga_2O_3	122, 123	4.8	10.2-14.2	Gate dielectric	$2.5\cdot10^{11}$	Not effective
Al_2O_3	124-126	10	7.0	Passivation/ gate dielectric	$(4\text{-}9)\cdot10^{11}$	Reduction of leakage and current collapse
HfO_2	127, 128	20-25	5.8	Gate dielectric	$2\cdot10^{11}$	Reduction of leakage and current collapse
ZrO_2	129	20	5.8	Gate dielectric	-	Low leakage current
TiO_2	108	24-96	3.2	Passivation/ gate dielectric	$6.4\cdot10^{11}$	Reduction of leakage and current collapse
Sc_2O_3	130-135	14	6.3	Passivation	$5\cdot10^{11}$	Reduction of current collapse
MgO	135, 136	10	8.0	Passivation/ gate dielectric	$2\cdot10^{11}$	Reduction of current collapse
La_2O_3	137	18-27	4.3-6.4	Gate dielectric	-	Not effective
Gd_2O_3	138-141	11.4	5.3	Gate dielectric	$(1\text{-}3)\cdot10^{11}$	Small reduction of leakage current
Ta_2O_5	142, 143	25	4.4	Gate dielectric	$(2\text{-}4)\cdot10^{13}$	Low leakage current
ZnO	144	8.5	3.4	Passivation/ gate dielectric	-	Reduction of current collapse but not effective gate dielectric
Pr_2O_3	145	14	6.3	Gate dielectric	-	Low leakage current

In terms of future integration into device manufacturing it is convenient to use a deposition method for the adopted dielectric that allows low-cost or high-yield processes. Among the established dielectric deposition methods, atomic layer deposition (ALD) has been demonstrated as a robust and highly manufacturable technique widely implemented by the semiconductor industry for the deposition of high quality dielectrics in ultra-scaled conventional and novel microelectronic devices.[147] As previously mentioned in the introduction chapter, this thesis will focus on the ALD of high-κ oxides as gate dielectrics for GaN-based MOSHEMTs. Section 2.3.3 will give a more detailed review on ALD high-κ gate oxides on GaN and GaN-based devices.

2.2.3. Electronic state theory

2.2.3.1. GaN surface polarisation and band bending

GaN and other III-V nitrides with hexagonal Wurtzite crystal structure are characterised by a macroscopic polarisation along the (0001) direction. This polarisation (***P***) is the sum of the spontaneous polarisation ($\boldsymbol{P_{SP}}$) inherent to the equilibrium lattice and the piezoelectric polarisation induced by strain ($\boldsymbol{P_{PE}}$). Wurtzite GaN can have two distinct surface polarities depending on the growth conditions: the Ga-face, when the film is grown with (0001) orientation, and the N-face, when the film is grown with (000-1) orientation.[73] These polarities have different properties that affect both device technology and performance.[73] The Ga-face crystals are of most interest for device work due to their superior electron transport properties.[148] Therefore, Ga-face Wurtzite GaN is the relevant surface polarity for this review.

Since polarisation is inherent to the material, each component can be determined using *ab initio* calculations. The polarisation along the c-axis induced by the piezoelectric effects can be determined using the material constants:

$$\boldsymbol{P_{PE}} = 2\frac{a - a_0}{a_0}\left(e_{31} - \frac{c_{13}}{c_{33}}e_{33}\right)\hat{c} \tag{2.4}$$

where c_{13} and c_{33} are elastic constants, e_{31} and e_{33} are piezoelectric coefficients, and a_0 and a are lattice constants.[149-154] For unstrained GaN crystals, the piezoelectric polarisation is negligible,[73] whereas the spontaneous polarisation is large and negative.[153] Calculations using the Berry-phase approach and local density or generalised gradient approximations have determined that the spontaneous polarisation of Ga-face Wurtzite GaN is – 0.029 C/m^2.[155-157] This spontaneous polarisation gives rise to a negative bound surface charge of ~ 1.81 x 10^{13} charges/cm^2.[146] Consequently, an equivalent positive bound polarisation charge exists on the N-face of GaN given by:

$$\sigma_b = \boldsymbol{P} \cdot \hat{c} \tag{2.5}$$

According to the charge neutrality condition, the overall charge of a system must be neutral and therefore the large bound polarisation charge at the interface which arises from the polarisation in GaN must be compensated.[158] In order to satisfy surface conditions of charge neutrality, the material system adjusts and gives rise to a distribution of inherent electronic states. There are two forms of compensation charges in semiconductors: (1) the formation of an internal space-charge layer that consists of ionised donors and defects near the surface or (2) external charged surface or interface states (Fig. 2.12).[158] These internal and external screening mechanisms are inversely related: the larger the compensation from the internal space-charge layer, the smaller the net concentration of surface states. The

nature and distribution of the compensation charge affect the internal electric field of the materials and ultimately device performance.[158]

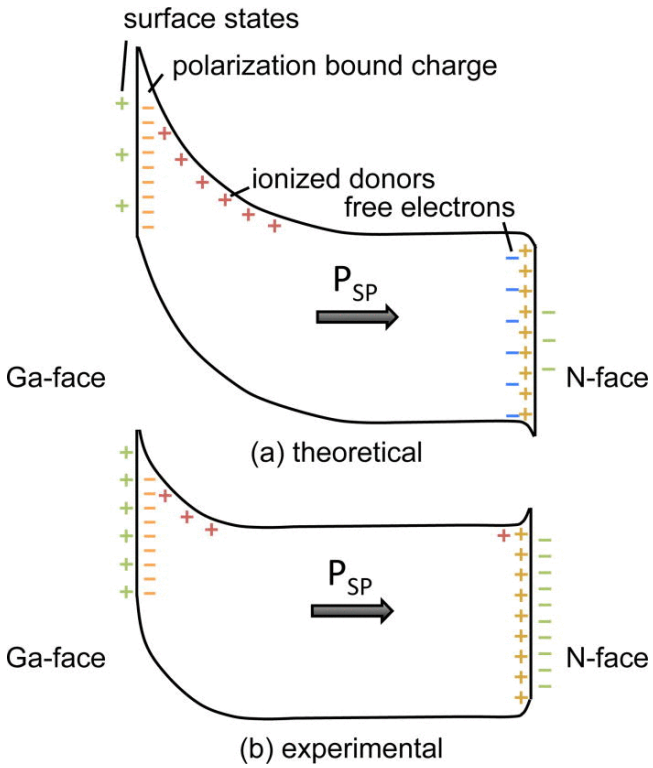

FIG.2.12: (a) Theoretical and (b) experimental band bending schematic for Ga- and N-face GaN. Both surfaces are screened by 10^{13} charges/cm^2 (the position of the ionised donors and electrons corresponds to their physical position rather than their energy level within the bandgap). Reprinted from Eller et al.[158]

Surface band bending is directly related to the space charge region and is an important device characteristic which describes the energy profile of electronic states at the interface: downward band bending favours the accumulation of electrons and upward band bending results in the depletion of electrons. Band bending can be calculated from the density of internal screening charge:[158]

$$\Phi_s = -\frac{qN_{ss}^2}{2\varepsilon\varepsilon_0 N_d}\hat{c} \tag{2.6}$$

where N_{ss} is the net surface charge. Assuming a Ga-face n-type GaN with doping density of 10^{17} charges/cm^3 and a net polarisation charge of ~ 1.81 x 10^{13} charges/cm^2 compensated internally by positive ionised donors, the calculation gives a surface potential of – 420 V.[158] This corresponds to 420 eV of upwards band bending and an average electric field of 200 MV/m at the surface of GaN. In equilibrium, this large internal field results in inversion or accumulation, which would limit the band bending to approximately the bandgap of the material, 3.4 eV (Fig. 2.12a.).[159, 160] Therefore, the polarisation bound charge cannot be entirely compensated internally by positive ionised donors.

Experimental band bending measurements indicate the band bending is well below the bandgap. In fact, most experimental band bending experiments for n-type Ga-face GaN typically report measurements between 0.3 eV and 1.5 eV.[161-163] These measurements can then determine the concentration of charged surface states from the band bending:

$$N_{SS} = \sqrt{-\frac{2\Phi_s \varepsilon \varepsilon_0 N_d}{q}} \quad (2.7)$$

This equation suggests that a 0.1 eV change in band bending corresponds to a 3.2 x 10^{11} charges/cm^2 change in the concentration of surface states. In order to achieve the experimental band bending, the depletion region is reduced to 56–126 nm for the doping density mentioned, which corresponds to ~ 5.6 x 10^{11}–1.3 x 10^{12} ionised donors/cm^2.[158] Since the polarisation charge will be fully compensated, the surface must be compensated by an additional ~ 1.7 x 10^{13} charges/cm^2. This compensation must therefore take place externally by charged electronic surface states (Fig. 2.12b).

2.2.3.2. GaN surface states

As previously mentioned, the total concentration of electronic surface states in Wurtzite Ga-N based structures is on the order of ~ 10^{13} charges/cm^2. The nature of these defects depends on the growth and processing conditions. They can be classified into two types: intrinsic and extrinsic.

Intrinsic surface states

Intrinsic surface states are associated with an ordered surface reconstruction that occurs at the termination of the crystal structure. For GaN, the hexagonal reconstruction has found to be the most likely surface reconstruction, which leads to vacancies and dangling bonds states in the bandgap.[164] The reconstructed surface determines the electronic surface states on GaN and may contribute to the interface state density of MOS devices.

Extrinsic surface states

Extrinsic surface states are associated with variations in the surface reconstruction. These defects include: grain boundaries, dislocation defects, structural defects, native oxides and adsorbates such as oxygen, carbon, and hydrogen.[158] Each defect has its own energy and charge state. Experimental research has shown that the band bending on GaN is upwards regardless of the crystal orientation, which indicates positively charged states on the Ga face and negatively charged states on the N face.[158] It has been reported that the most likely states in GaN are structural defects, Ga termination, surface contamination (such as absorbed oxygen atoms), surface states, adsorbates, or additional charge compensation.[165] Thus, these states depend on the deposition, cleaning, and processing methods and conditions.

2.2.3.3. Oxide/GaN interface states

The formation of the oxide/GaN interface generates defect states which are part of the overall interface electronic states. Various band alignment models have been explored over the last decades to describe the semiconductor interface.[166-172] However, a unified theoretical model has not yet been developed due to the complexity of the interface electronic states.

The band offsets at an oxide/semiconductor interface are related to the theoretical band alignment modelling of metal/semiconductor interfaces. The original interface model was presented independently by Mott[166] and Schottky[167] in 1938 and 1940, respectively:

$$\Phi_B = \phi_M - X_S \tag{2.8}$$

The Schottky-Mott model defines the Schottky barrier height (SBH) as the difference between the work function of the metal (ϕ_M) and the electron affinity of the semiconductor (X_S), assuming that the metal and semiconductor are in equilibrium and that there is no charge transfer or direct interaction (and therefore no dipole) across the interface (Fig. 2.13a).

In 1947, acknowledging the fact that a low density of interface states energetically located in the semiconductor gap could sufficiently 'pin' the Fermi level, Bardeen adapted the model to include interface states:[168]

$$\Phi_B = \phi_M - X_S - \Delta \tag{2.9}$$

This model assumes that when the semiconductor makes contact with the metal, charge can flow across the interface to fill or deplete the surface states in the semiconductor. This surface states charge transfer results in an interfacial dipole (Δ) which can compensate the difference between the metal and semiconductor work functions (Fig. 2.13b).

In 1965, Heine elaborated on the nature of the surface defects in the Bardeen model.[169] The Bardeen–Heine model points out that localised states cannot exist at the interface when the metal conduction band overlaps with the semiconductor energy gap, but rather the tailing of the metal electron wave functions will decay into the semiconductor and induce states within the bandgap. These states are known as metal-induced gap states (MIGS). In 1977, Flores and Tejedor discussed that the behaviour responsible for the MIGS in metal/semiconductor heterostructures is also applicable to semiconductor/semiconductor heterostructures.[170] They showed that the interface dipole is induced when the charge neutrality points of the two semiconductors are not aligned.[171] Finally, Tersoff further refined this concept by arguing that the most important property at a semiconductor heterostructure is the band 'line up', which occurs to minimise the interface dipole (Fig. 2.13c).[172] This means that the semiconductors will align at the charge neutrality point rather than at the electron affinity. The resulting SBH is given by:

$$\Phi_B = S(\phi_M - \Phi_{S,CNL}) + (\Phi_{S,CNL} - X_S) \tag{2.10}$$

where $\Phi_{S,CNL}$ is the charge neutrality point with respect to the vacuum level, and S is the Schottky pinning factor which determines the strength of the Fermi pinning. There are two limits for the Schottky pinning: (1) the Schottky-Mott limit characterised by the absence of a dipole or pinning (S=1), where the change of barrier height equals the change of metal work function, and (2) the Bardeen-limit or strong pinning limit (S=0), in which charge transfer pins the barrier height at the charge neutrality level (CNL) of the semiconductor.[173] The CNL is the energy of the highest occupied state for the neutral surface. At a semiconductor interface, corresponds to the Fermi level of the MIGS or where the gap states change from donor-like to acceptor-like.[173]

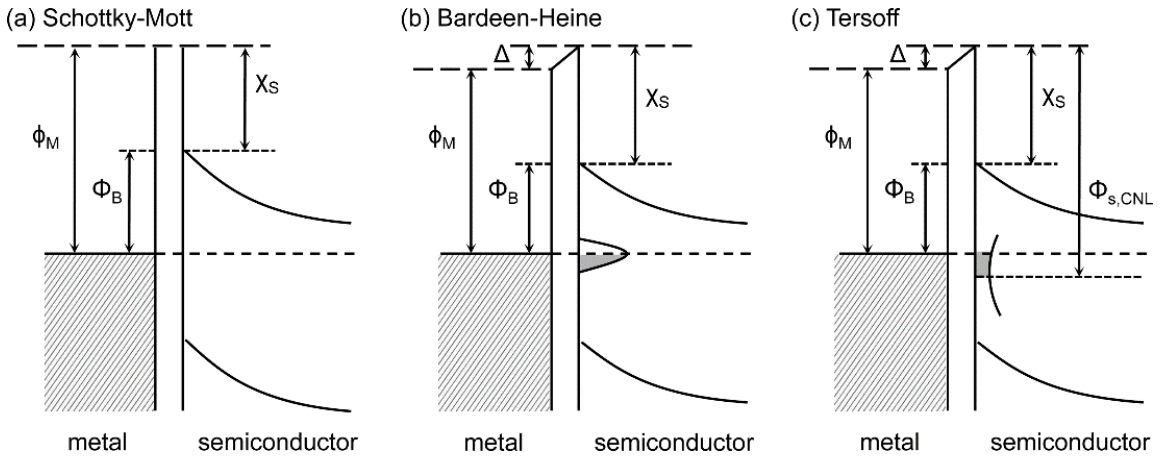

FIG.2.13: Schematic of the metal–semiconductor interface models according to (a) Schottky–Mott, (b) Bardeen–Heine, and (c) Tersoff**.** Reprinted from Eller et al.[158]

Schottky pinning

Various models explain the Schottky pinning factor linked to the interface defects density. Currently, there is a need for better understanding of these models and the interface defects that could explain the origin of Schottky pinning factor.

Based on the previously mentioned MIGS theory that assumes that there are intrinsic states within the energy gap of the semiconductor, Monch found an empirical relationship for the Schottky pinning factor at metal/semiconductor interfaces and the dielectric constant of the semiconductor:[174]

$$S = \frac{1}{1 + 0.1\,(\varepsilon_s - 1)^2} \tag{2.11}$$

This model has also been used to describe insulator/semiconductor interfaces. However, it is unclear where the MIGS would originate in such a system.[158]

Spicer *et al.* noticed that for III-V compounds the pinning phenomenon occurs at both metal/semiconductor and oxide/bulk semiconductor interfaces.[175, 176] They suggest that the Fermi level stabilises after a fraction of a monolayer of metal or oxide is added to the

surface and thus, the states responsible for pinning result from interaction between the adatoms and the semiconductor regardless of the electronic configuration of the adatom. This results in a unified defect model for pinning based on interface defect states, where defect formation is caused by the energy released when the atom is adsorbed. The thermal energy produced by chemisorption of an adatom can excite a constituent atom from the semiconductor generating a vacancy, and the vacancy states characterise Fermi level pinning. However, this model requires explicit identification of defect states on an atomic level.[158]

Hasegawa *et al.* proposed a similar model where the disorder induced at the surface region of the semiconductor is responsible for pinning, where departure from the crystalline structure generates 'Anderson localised states'.[177] These disorder induced gap defect states (DIGS) are assumed to be several monolayers thick and energetically distributed within the energy bandgap, giving the following Schottky pinning factor:[178]

$$S = \text{sech}\,(\delta/\lambda) \tag{2.12}$$

where

$$\lambda = \sqrt{\varepsilon\varepsilon_0/N_{DIGS}(E_0)} \tag{2.13}$$

where δ is the thickness of the disorder layer and $N_{DIGS}(E_0)$ is the volume density of DIGS at E_0.

On the other hand, the chemical reaction model by Andrews and Phillips suggests that the chemical reactivity may affect the interface states and SBH.[179] They noticed a linear correlation between the heat of formation and the SBH. However, the model does not give rise to an explicit microscopic explanation of the Fermi level pinning.

Band line-up

In addition to the nature of Schottky pinning, a better understanding of the alignment point at a heterojunction is necessary. While the electron affinity model assumes no charge transfer at the interface, the charge neutrality level model focusses on Fermi level pinning and charge transfer. The value of the CNL represents the weighted average of the density of states and it can be calculated as the energy at which the Green's function is zero:[180, 181]

$$\mathrm{G}(E) = \int_{BZ} \int_{-\infty}^{\infty} \frac{N(E')dE'}{E - E'} = 0 \tag{2.14}$$

where the density of states $N(E')$ can be calculated from either the local density approximation (LDA)[172, 180, 181] or the tight binding (TB) model.[182] These methods find the band offsets in terms of the semiconductor bulk properties for a wide range of bonding types without the need to characterise each bond explicitly, which is particularly useful for amorphous structures where specific bonding structures may be difficult to characterise.[158]

2.2.3.4. Band offsets

The band offsets at an oxide-semiconductor interface are related to the band alignment models. They depend on the charge transfer across the interface which would create an interface dipole. Robertson and Falabretti carried out theoretical studies of the band offsets between various dielectrics and GaN using the MIGS pinning factor and CNL alignment as determined by the LDA.[183] From this model, the VBO at an oxide/GaN interface can be determined as given by the following equation:[183]

$$\Delta E_V = E_{CNL,oxide} - E_{CNL,GaN} - S\left[I_{GaN} - I_{oxide} - \left(E_{CNL,GaN} - E_{CNL,oxide}\right)\right] \tag{2.15}$$

where I is the photo threshold energy, and E_{CNL} is the charge neutrality level with respect to the valence band maximum for GaN and the respective oxide.

TABLE 2.4. Comparison between the theoretical band offset calculations and experimental measurements for dielectrics on GaN.[158]

	Theoretical values			**Experimental values**	
Material	**VBO**	**CBO**	**Deposition**	**VBO**	**CBO**
AlN	0.4	2.4	ECR MBD	0.8	
			Reactive MBD	1.4	
Al_2O_3	3.0	2.4	PEALD	1.8	
			ALD	0.1	
			ALD	1.2	2.0
			ALD		2.1
Ga_2O_3	0.7	0.5	Dry therm. ox.	1.4	
HfO_2	1.6	1.1	PEALD	1.4	
			ALD	−1.9	
			ALD	0.5	1.5
			MBD	0.3	
			Sputtering	0.6	1.7
La_2O_3	0.7	2.0	MBD	1.9	
MgO	2.0	2.6	MBD	1.2	
			PEMBD	1.1	
Sc_2O_3	0.7	2.0	MBD	0.8	
			PEMBD	0.4	
			Pulsed laser	0.8	
Si_3N_4	0.8	1.3	MBD	−0.6	
			PEMBD	−0.4	
			ECR-PECVD	1.0-1.2	
SiO_2	3.1	2.6	ALD	2.4	3.0
			MBD	2.0	
$SrTiO_3$	0.2	−0.1	MBD	0.1	
ZnO	0.9	−0.7	PEMBD	0.8	−0.8
			Sputtering	0.5	−0.6
			Sputtering		−0.6
			Sputtering	0.7	−0.7

Table 2.4 shows a comparison between some oxide/GaN band offsets calculated using the theoretical model and the values measured experimentally.[158] From the experimental studies of band alignments for oxides on GaN summarised in Table 2.4, it can be concluded that the model provides a good approximation for some interfaces. However, it is not very reliable for all the interfaces. The differences between theoretical and experimental values are usually attributed to variations in the oxides bandgap, stoichiometry or crystal structure. They can also be a consequence of the presence of an interfacial oxide layer as well as unaccounted band bending during the measurements, which can alter the band offsets values dramatically.[183] In some cases, a large range of experimental values can be observed, which can be a consequence of inconsistent processing methods such as cleaning and deposition technique. This can result in variations in oxygen coverage, dielectric stoichiometry and interfacial bonding, affecting the band offsets.

2.2.4. Device reliability

2.2.4.1. Gate Leakage mechanisms in GaN HEMTs

The large concentration of electronic defect states on GaN-based devices causes device performance and reliability issues such as large leakage current and current collapse. As mentioned before, gate leakage is one of the major issues that needs to be addressed before GaN-based power electronic devices replace existing Si technology. In a HEMT, the Schottky gate diode controls the 2DEG in the channel. Because GaN-based HEMTs are normally ON devices with high 2DEG concentration, they need a large negative bias applied to the gate to turn the device OFF. Therefore, gate leakage significantly degrades the standby power dissipation and the power efficiency and reliability of the device.[92]

A wide range of gate leakage mechanisms have been discussed for AlGaN/GaN HEMTs including Schottky or thermionic emission (TE),[184] thermionic field emission (TFE),[185-189] trap-assisted tunnelling (TAT),[184, 185] dislocation-assisted tunnelling,[95, 188, 190] defect hopping,[115, 185, 186] Fowler-Nordheim (FN) tunnelling,[191] Frenkel-Poole emission (FPE),[188, 192] and space charged limited current[193] (Fig. 2.14). In forward bias, the gate leakage at Schottky interfaces is usually attributed to thermionic emission and thermionic field emission.[184, 185, 187-189] However, research has shown that this mechanism only describes a fraction of the experimental gate leakage and that the total gate leakage must be enlarged by a trap-related mechanism such as deep-level bulk states that act as trapping states within tunnelling distance of the interface,[194] defects near the surface region,[195] and deep traps below the conduction band minimum that are likely to be trapping centres.[196] In reverse-bias, the leakage current is assumed to consist of two temperature dependent mechanisms. As in forward bias, thermionic emission and thermionic field emission is believed to be the dominant mechanism.[186] However, lateral tunnelling from the edge of the gate to the drain (hopping) or trap-assisted tunnelling are also believed to contribute to the total leakage current.[185, 197] Temperature-dependent studies have shown that thermionic field emission is the dominant leakage mechanism at high temperatures while trap-assisted tunnelling dominates at low temperatures.[186] Other studies have suggested that Frenkel-Poole emission is the dominant mechanism at high temperatures,[188, 190] while Fowler-Nordheim tunnelling is also observed at low temperatures.[188] Also, at large reverse bias, trap-assisted tunnelling at higher temperatures, hopping conduction along the surface at moderate temperatures and impact ionisation at lower temperatures have been reported.[80] Finally, studies on leakage mechanisms for InAlN/GaN HEMTs have reported tunnelling current via dislocations in the forward bias[95] and Frenkel-Poole emission in the reverse bias.[93, 94] Therefore, the dominant mechanism responsible for large leakage current in

Schottky HEMT devices has not yet been fully established, as it is believed to be dependent on temperature, bias and the specifics of each device.

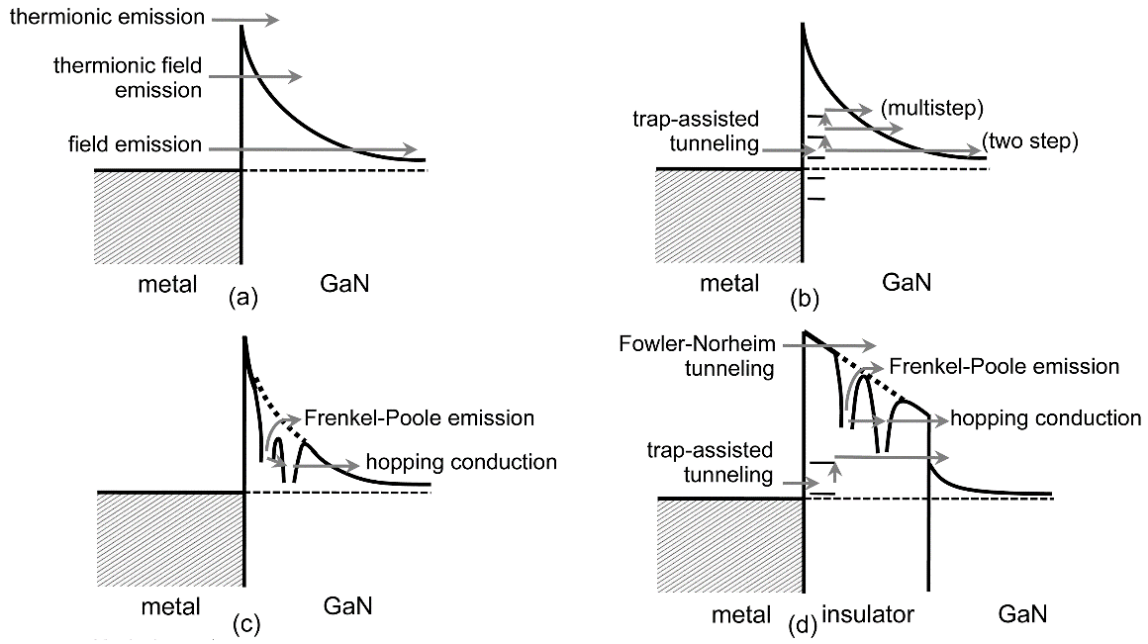

FIG. 2.14: Possible gate leakage mechanisms at (a)-(c) metal/GaN and (d) metal/insulator/GaN interfaces. Reprinted from Eller et al.[158]

Polarisation is also believed to have an important role in the reverse bias gate leakage mechanism, determining device behaviour in AlGaN/GaN and InAlN/GaN HEMTs.[192, 198] It has been observed that increases in polarisation and internal electric field at the Schottky barrier occur with a simultaneous increase of gate leakage, which suggests that the leakage current mechanism must be related to defect states that also increase with polarisation.[199] It has been reported that stress-induced defects caused by the lattice mismatch between the AlGaN barrier and GaN are related to pits and grain boundaries near the gate edge where the electric field is the highest.[193, 196, 200-205] However, it has been observed that gate edge defects provide only a partial explanation for device failure and thus, other defects may also be associated with the increase in post-electrical stressed devices.[206] It has been proposed the existence of a failure mechanism accelerated by the electric field only, resulting in trap generation and charge trapping, with consequent increase in the gate

leakage current.[207] According to Joh and del Alamo,[45] the electric field in the gate-drain region would increase the strain in the AlGaN/GaN heterojunction (inverse piezoelectric effect) eventually resulting in strain relaxation and crystallographic defect formation. It has been found that under high voltage these defects introduced by the inverse piezoelectric effect produce an increase in the gate leakage current.[207] If the voltage exceeds a critical value, this increase in the leakage current is non-reversible, resulting in device degradation.[45]

An alternative model proposed by Hasegawa *et al.*,[208] suggests that the electronic states act as pinning states rather than tunnel-assisting traps. In this model, the previously discussed DIGS model and additional empirical results explain the mechanisms of gate leakage in AlGaN/GaN (Fig. 2.15.a). The near-surface electronic states are described by a U-shaped continuum common to III-V semiconductors defined by:[209]

$$N_{SS}(E) = N_{SS0} \exp\left(\frac{|E - E_{CNL}|}{E_{CNL}}\right)^{n_j} \tag{2.16}$$

where N_{SSO} is the minimum surface state density, E_{CNL} is the energy position of the charge neutrality level with respect to the valence band maximum, E_{0j} and n_j determine the distribution shape of the continuum ($j = a$ for acceptor-like states above E_{CNL}, and $j = d$ for donor-donor like states below E_{CNL}). The U-shaped continuum pins the surface Fermi level near the E_{CNL}. In addition to the U-shaped continuum, high-density deep donors are created near the surface, resulting in an additional discrete peak at $E_c = 0.37$ eV (Fig. 2.15.b). This discrete peak is related to N-vacancies and thus its density depends on the individual sample processing treatments. Due to Fermi level pinning near E_{CNL}, these deep donors are ionised, supplying electrons to the 2DEG. This produces a thin Schottky barrier (TSB) region that allows for electron tunnelling (Fig. 2.15.c), generating the

thermionic field emission path responsible for the large leakage current in both forward and reverse directions. Hashizume *et al.*[210] later applied this model to experimental work, showing that it gives excellent fitting for current-voltage (IV) curves in both forward and reverse bias.

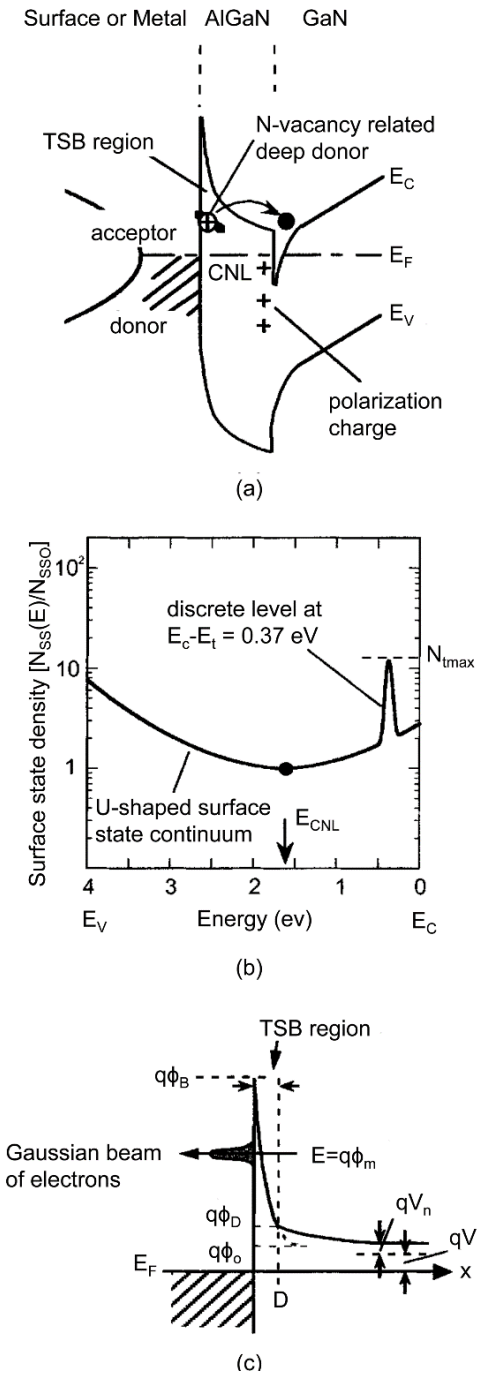

FIG. 2.15: (a) Unified model for near-surface electronic states of AlGaN, (b) a combined distribution of state density, and (c) the TSB model for current transport at the Schottky interface. Reprinted from Hasegawa et al.[158]

2.2.4.2. Current collapse in GaN HEMTs

Drain current collapse is another major limiting factor in the performance of GaN-based power electronics. A reduction of the output power is observed based on IV measurements (Fig. 2.16a), caused by a decrease of the maximum drain current and an increase of the ON voltage.[211]

In III-V HEMTs, the drain stress in the ON-state it is expected to cause the capture of electrons from the 2DEG by deep-level traps ultimately decreasing the drain current, whereas the gate stress in the OFF-state condition should inject electrons back into the channel resulting in an increase in drain current. However, this increase in the OFF-state drain current under gate stress is not observed experimentally for AlGaN/GaN HEMTs. A reduction in drain current has been observed under drain stress when the saturation region is in the ON-state and also under gate stress when the channel region is pinched OFF in the OFF-state condition.[212]

A model proposed by Hasegawa *et al.*,[208] explains this behaviour of AlGaN/GaN HEMTs under drain and gate stress (Figs. 2.16b and 2.16c, respectively). This model uses the density of states distribution shown in Figure 2.15a (in the previous section) and assumes that under drain stress electrons are injected from the 2DEG to the surface states of AlGaN near the drain, reducing the drain current and expanding the depletion width. When the voltage is switched to the OFF-state, the electrons are emitted from these states leading to recovery transients, according to:

$$N_{emit}(t) = \int N_{SS}(E)\left[1 - \exp\left(-\frac{1}{\tau(E)}\right)\right] dE \qquad (2.17)$$

where:

$$\tau(E) = \frac{1}{N_c \, \sigma_n \, \vartheta_{thin}} \exp\left(\frac{E_c - E}{kT}\right) \tag{2.18}$$

The model fits experimental data, where the total density of the discrete peak at 0.37 eV is 5×10^{11} defects/cm^{-2}.[208] Once the voltage is switched back to the OFF-state, the electrons from the discrete peak are quickly emitted, giving rise to a fast transient.[208] There is also another slower transient associated with the emission of electrons from the continuum of surface states, which have a wider range of time constants and cause the formation of a virtual gate.[208]

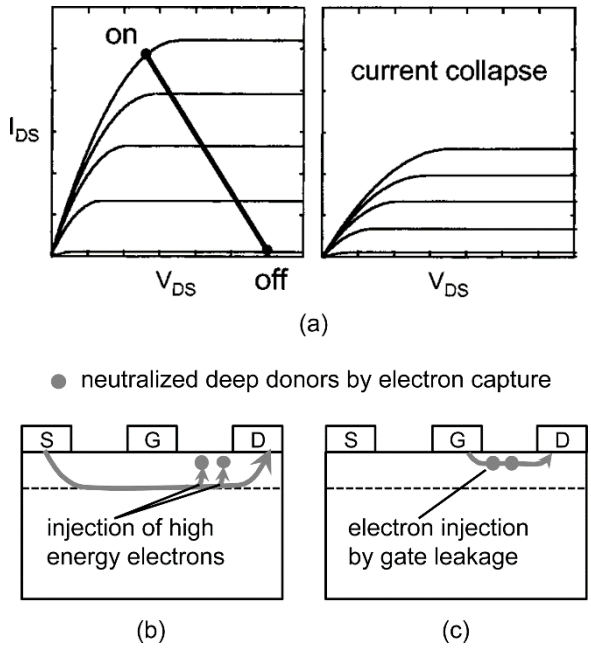

FIG. 2.16: (a) Schematic representation of drain current collapse. Models for current collapse (b) under drain stress and (c) under gate stress. Reprinted from Hasegawa et al.[158]

Virtual gate

The concept of 'virtual gate' was proposed in 2001 by Vetury *et al.*.[211] If a negative charge exists on the AlGaN layer surface, the surface potential is made negative, depleting the channel of electrons and leading to extension of the gate depletion region (Fig. 2.17a). The effect of this surface negative charge is to act like a negatively biased metal gate.

Therefore, there are two gates on the surface which are connected in series between the source and drain (as shown in Fig. 2.17b). The potential on the metal gate, V_G, is controlled by the applied gate bias while the potential on the second gate, V_{VG}, is controlled by the total amount of trapped charge in the gate drain access region. The output drain current is now controlled by the mechanism that supplies charge to and removes charge from the virtual gate, in addition to the applied gate bias. The current collapse is thus a consequence of the creation of this virtual gate, which results from accumulation of negative charge on the surface. In order to restore the current, the net positive surface charge on the device surface must be replaced either by the removal of electrons trapped in the surface when the gate is forward biased, or by the accumulation of holes at the surface, eliminating the virtual gate. Koudymov *et al.*[213] and Morardi *et al.*,[214] further developed this model based on a simple and more precise model that uses a set of assumptions and a minimal number of fitting parameters. The implementation of this analytical model closely agree with experimental measurements in AlGaN/GaN HFETs.[213, 214]

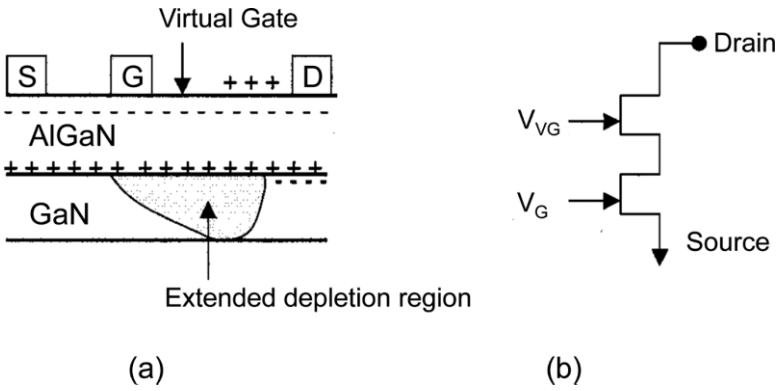

FIG. 2.17: Model of device showing (a) the location of the virtual gate and (b) schematic representation of the device including the virtual gate. Reprinted from Vetury et al.[176]

The formation of a virtual gate as the cause of the current collapse phenomenon has been confirmed experimentally.[215, 216] However, it is still unclear which states play a role

in the creation of the virtual gate or the location of these defects in the AlGaN/GaN heterostructures. Defects have been measured at the surface close to the gate edge,[217, 218] in the AlGaN layer,[217, 219] at the AlGaN/GaN interface,[218, 220] and in the GaN buffer.[217] Processing conditions and device design are believed to be the cause of these discrepancies. For example, it has been reported that current collapse is proportional to carbon contamination,[221] and therefore dependent on the cleaning process used during device fabrication. In addition, it has been demonstrated that there is a linear relationship between the critical degradation voltage and the gate length, which suggests that the electric field is the main cause of degradation.[222] This proves that device design has an effect on the concentration and distribution of defects.

2.3. Atomic layer deposition of high-κ gate oxides for GaN-based devices

2.3.1. Overview of atomic layer deposition

The atomic layer deposition growth method was introduced and patented in 1977 by Suntola and Antson in Finland, under the name of atomic layer epitaxy or ALE.[223] ALD technology was originally developed to meet the needs for a deposition method of high-quality and large-area thin-films for the fabrication of thin film electroluminescence (TFEL) flat panel displays. ALD was used commercially for the first time in the mid-1980s for the fabrication of TFEL displays.[224, 225] The devices consisted of a large bandgap doped semiconducting layer of polycrystalline luminescent ZnS:Mn, surrounded from both sides by insulated oxide layers of amorphous Al_2O_3. At that time, the applicability of ALD to epitaxial growth of II-IV and III-V compound semiconductors was demonstrated.[226, 227] Great efforts were made in the preparation of III-V compounds in the late-1980s.[228, 229] However, due to the complicated surface chemistry between group III alkyl compounds

and group V hydrides no real breakthrough was achieved in this area, with no reported commercial applications.

The resurgence of ALD in the mid-1990s was motivated by the microelectronics industry, where the decrease of device dimensions and increase of aspect ratios and complexity in ICs required the introduction of new materials and thin film deposition techniques.[230] The interest in ALD increased dramatically in the 2000s with the transition of the industry to the use of high-κ dielectrics for the transistor gate stack as a consequence of the high leakage currents present in Si MOSFETs with SiO_2-based gate dielectrics. To solve the oxide thickness reduction challenges, the high-κ oxides needed to be highly uniform and pinhole-free on Si to prevent leakage current through the gate oxide. In 2007, Intel introduced a new generation of ICs with thin films of HfO_2 used as gate dielectric layers deposited by ALD.[231] This allowed them to advance to a new technology without creating transistors with significantly higher power consumption. Afterwards, ALD was established as an important technique for the deposition of high-κ dielectric gate oxides in these and subsequent ICs.[232-234] Currently, the International Technology Roadmap for Semiconductors (ITRS)[235] includes ALD for the deposition of high-κ dielectric gate oxides in next generations MOS structures, and ALD-related research is being conducted in a large number of universities, research centres and companies.

2.3.2. Atomic layer deposition process

Atomic layer deposition uses sequential, self-limiting and surface controlled gas phase reactions for the deposition of ultrathin, uniform and conformal thin layers of material. During the ALD growth process, the sample surface is exposed to two or more precursor chemicals which contain the different elements of the material being deposited.[230] The precursors are kept separated from each other in the gas phase and introduced alternatively

into the reactor chamber, where they react with the sample surface one at a time through a self-limiting surface reaction. The growth of the desired material is achieved by repeating the ALD-growth cycle, which normally involves four steps: precursor dose, precursor purge, co-reactant dose and co-reactant purge (Fig. 2.18).[230]

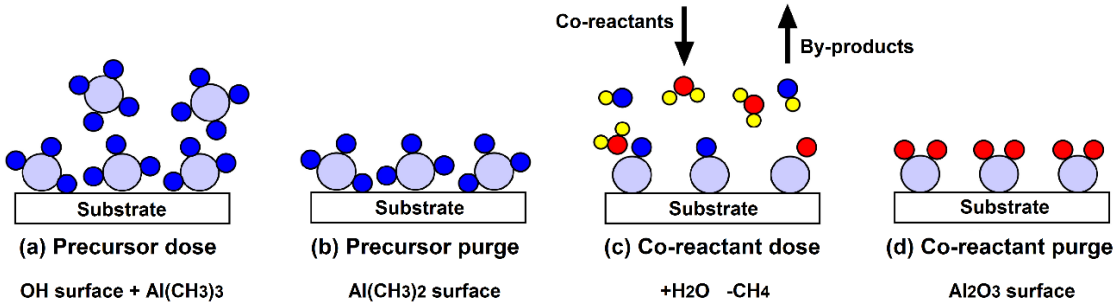

FIG.2.18: Schematic illustration of the ALD cycle with the $(CH_3)_3Al$-H_2O process as an example.

Figure 2.18 shows a schematic diagram of the ALD process. The growth of Al_2O_3 from trimethylaluminium (TMA or $(CH_3)_3Al$) and water (H_2O) is used as an example. When the TMA precursor is dosed onto the surface terminated with hydroxyl (OH) functional groups, the precursor molecules are chemisorbed by reacting with these groups and releasing some of their ligands (Fig. 2.18a). Due to the finite number of reaction or chemisorption sites on the substrate surface, only an atomic layer of the precursor (or monolayer) can be bonded to the surface. The excess precursor molecules and the volatile reaction by-products are removed by an inert gas such as Argon (Ar) during the precursor purge leaving only a saturated monolayer of the precursor (Fig. 2.18b). The H_2O co-reactant is then dosed and reacts with the precursor monolayer liberating the ligands and producing Al_2O_3 (Fig. 2.18c). At this point the surface is converted back to its original state and the newly deposited layer of Al_2O_3 acts as new OH terminated surface. The co-reactant purge removes all excess co-reactants and by-products, completing the ALD cycle (Fig. 2.18d). A common misconception is that a monolayer is deposited in each ALD cycle, but often the growth

per ALD cycle is much smaller than one monolayer. For example, the growth per cycle of Al_2O_3 is typically 1.0-1.1 Å/cycle whereas its monolayer thickness is 3.8 Å.[230] Reasons for this are the limited number of reactive surface sites and the steric hindrance between bulky ligands in the chemisorption layer, so even if the chemisorption layer is saturated it may contain too few metal atoms for forming a full monolayer of the film material.[236]

2.3.2.1. Advantages of ALD for the growth of gate oxides

Thickness control

If the times for the precursor and co-reactant doses are high enough to achieve saturation, the material deposited on the substrate surface per cycle is constant, and therefore the film thickness can be accurately controlled at the Angstrom (Å) or monolayer level by the number of deposition cycles applied.[230]

Conformality

Due to the self-limited nature of the surface reactions in ALD, if the precursor flow is large enough so that the chemisorption layer becomes saturated, the deposited films remain extremely smooth, uniform and conformal to the substrate.[237] As a result, ALD provides excellent step coverage and conformal deposition on high aspect ratio structures.[236] This ability is one of the most desirable characteristics of ALD as the miniaturisation of semiconductor devices has led to the increasing need for high quality conformal coating of high aspect ratio structures (Fig. 2.19).[236]

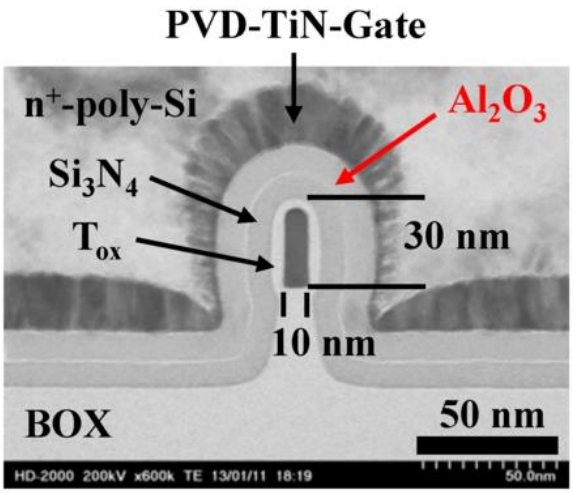

FIG.2.19: Cross-sectional STEM image of a fabricated MANOS type SOI-FinFET flash memory with an ALD Al_2O_3 blocking layer. Reprinted from Liu et al.[238]

Pinhole free films

If the reactions are driven to completion during every reaction cycle, no surface sites are left behind during film growth and the films tend to be very continuous and pin-hole free, which is a very important factor for the deposition of high quality dielectric films.[239]

Scalability

Other advantage of the ALD process is that the ALD precursors are gas phase molecules and thus the surface chemistry involved is independent of the substrate area. As a result, the ALD process can easily be scaled-up to large substrates and to parallel processing of multiple substrates providing large area capability. ALD is only limited by the size of the reactor chamber.[236]

Effective material utilisation

Because the surface reactions in ALD are performed sequentially, the two gas phase reactants are not in contact in the gas phase.[236] This separation of the two reactions

eliminates all possible detrimental gas phase reactions and favours the use of precursors highly reactive toward each other, enabling the effective utilisation of the precursor materials.[230]

Relatively low processing temperatures

For the same growth temperature, films grown by ALD often show superior quality compared with films made by other methods. This is related to the fact that in ALD each monomolecular layer reaction step is given enough time to reach completion, while in other methods the continuous growth may prevent this by covering the unreacted species with new deposits. As a result, high quality materials are obtained at relatively low ALD processing temperatures.[230]

Relatively wide processing temperature range

Many ALD processes can be performed over a relatively wide temperature range. Thus, a common growth temperature can be found for different materials, which gives the capability to deposit multilayer structures in a continuous process. This is utilised in manufacturing of the TFEL displays where the insulator-luminescent material-insulator three-layer structure is grown in one continuous process.[230]

Delta doping in atomic layer deposition

Another advantage of ALD is doping control. Doping in ALD can be achieved by the inclusion of additional precursors within the ALD recipe. The doping of ALD films can be easily tailored using the ‘delta doping’ method,[240] which consists in adding a dopant cycle in a series of ALD cycles. By controlling the number of dopant cycles added, the properties of the doped ALD films can be tuned to meet specific requirements. In the case of gate

oxides, the electronic or optical properties of the undoped material can be improved by adding a dopant with higher dielectric constant or wider bandgap, respectively.

Therefore, due to its excellent thickness control, uniformity, conformality, low thermal budget and the ability to layer multi-compositional films to combine different material properties, ALD is the most promising deposition technique to produce high-κ gate oxides for power electronic devices, where the deposition of very thin, conformal and highly insulating high-quality oxide layers in the sub-nanometre range is needed.

2.3.2.2. Requirements for ALD

The key factors that must be taken into account during an ALD reaction are: the volatility and thermal stability of the precursors, their pulsing into the reactor and their interaction with the substrate surface and each other.[241]

Precursor volatility and thermal stability

High volatility and adequate thermal stability are essential for ALD precursors in order to ensure an efficient transportation into the reaction chamber and to avoid self-decomposition at the deposition temperature. For highly volatile precursors with vapour pressures of ~ 10 Torr at 20 °C such as TMA,[241] precursor transportation can be achieved by vapour draw. If the precursor volatility is insufficient at room temperature, heating is required to achieve an adequate vapour pressure. For example, in the industrial ALD process of HfO_2 using $HfCl_4$, the precursor needs to be heated at ~ 200 °C to achieve good vapour pressure that is suitable for deposition.[242] The increase of temperature to enhance the vapour pressure can cause problems such as decomposition of the precursor or change of phase, which can result in poor stability and short life-time for precursors.[241] Thermal decomposition also affects the self-limiting film growth and leads to non-uniform

thickness and contaminated films.[241] Additionally, if the precursor vapour pressure up to the decomposition temperature is insufficient, a bubbling technique can be used for liquid or solid precursors.[243] Bubblers with internal dip tubes that go beneath the surface of the precursor in a liquid state are utilised in this case. The bubbler contains valves to allow an inert carrier gas to flow into the bubbler through the dip-leg and pick up the material for transportation. The vapours are then transported into the reaction chamber.

Precursor dose

Due to the self-limited nature of the surface reactions in ALD, an exact precursor dosage is not needed. The only requirement is that the number of precursor molecules introduced into the chamber during each dose must be large enough to cover the available surface reaction sites, including the sample surface as well as all the inside exposed surfaces of the reactor chamber. In addition to this, the dose of each reactant must be long enough so that the reactant reacts with the entire sample surface and reaches saturation coverage.[244]

Precursor interaction with the substrate surface and each other

During the precursors dose, each precursor must undergo a self-limiting reaction with the substrate surface groups. These reactions must be fast, complete and irreversible within the time scale of one precursor dose step in order to ensure a fast saturation with short cycle times, complete reactions with high film purity and avoid gas phase reactions, and thereby a rapid formation of the desired material.[245] After each reaction is complete, no further reaction must occur between any excess reactant and its own reaction products on the surface. The reactants and by-products must be sufficiently volatile at the deposition temperature so that they can be efficiently removed during the purge step.[245] Furthermore, reactants and volatile reaction by-products should not etch and/or dissolve into the substrate

or the growing film, preventing the self-limiting film growth or even the growth of the desired material.[245]

Therefore, precursors chemistry is the key to a successful ALD process. The essential requirements for ALD precursors are: high volatility and thermal stability at the deposition temperature, sufficient reactivity towards the substrate surface and the co-reactant, 'clean' reaction with the co-reactant to avoid film contamination and no etching and/or dissolution into the substrate or the growing film.[230] Other desirable properties for the precursors include: easy synthesis, availability, low cost, high purity, safe-handing and non-toxicity.[245]

2.3.2.3. The ALD reactor

ALD processes can be performed over a large range of pressures from atmospheric[246] to ultrahigh vacuum.[247] According to the pumping and use of carrier gas, ALD reactors can be divided into two groups:[236] (1) inert gas flow reactors operating at pressures higher than ~ 1 mTorr under viscous or transition flow conditions, where the reactants are exposed with a carrier gas in viscous flow which flows continuously through the reactor to the pump,[248] and (2) high or ultrahigh vacuum reactors with molecular flow conditions, where the reactants are exposed without carrier gas and are removed by opening up completely to the pump and evacuating the reactor after the exposures.[249]

Commercial ALD reactors are generally designed to minimise the pulse and purge times and to maximise the efficiency of precursor use. For this reason, most ALD reactors operate in viscous flow mode with an inert carrier gas. The ALD cycle times of viscous flow reactors are much shorter because the carrier gas entrains the reactants and products, making the residence times in the reactor shorter compared to high-vacuum reactors which employ no carrier gas during reaction exposure.[236] Additionally, the purge times of viscous

flow reactors are faster than the evacuation times of high-vacuum chambers.[236] Finally, precursor utilisation efficiency in viscous flow reactors is larger due to the fact that precursor molecules undergo multiple collisions while being carried along the reactor.[236] This increases reaction probability and accelerates the saturation of the chemisorption layer, which makes the process faster. On the other hand, high-vacuum reactors precursor molecules make only a few collisions with the substrate surface before being pumped out and therefore have a limited probability to react.[230] Figure 2.20 shows the main features of a typical viscous flow ALD reactor:

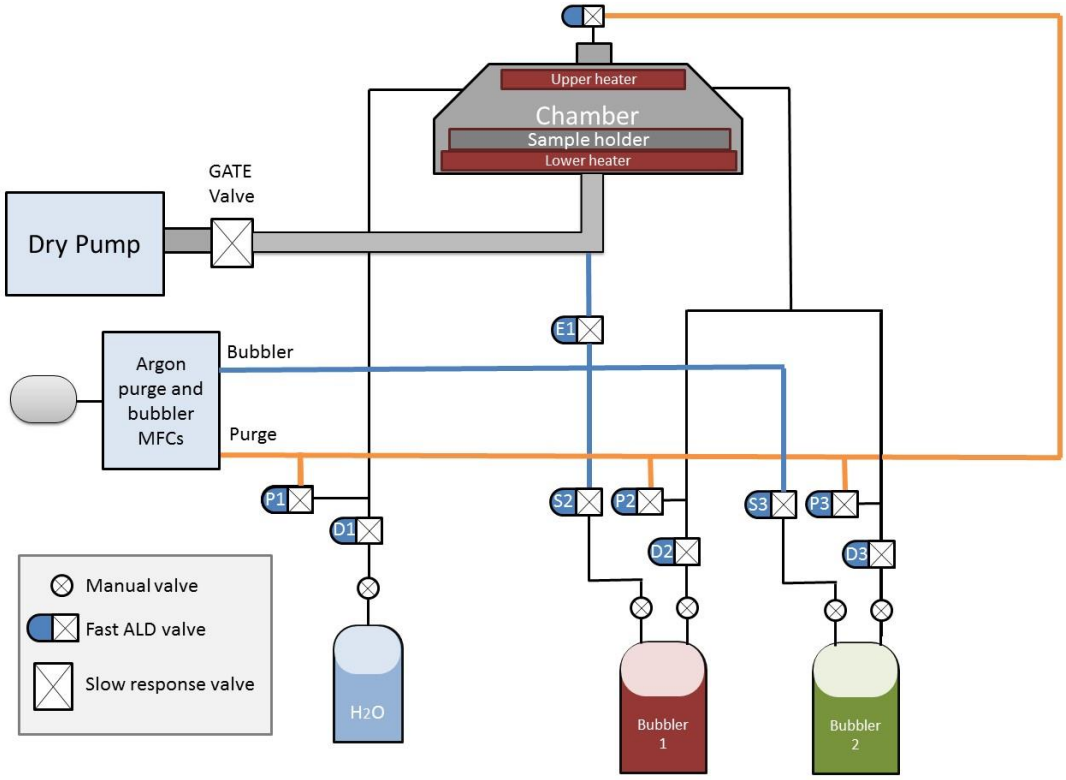

FIG.2.20: Schematic illustration of an ALD reactor.

Pump

Mechanical pumps are used to form a partial vacuum by removing gas molecules from the reactor chamber and moving them to the exhaust. The pumps customised for ALD normally achieve pressures in the order of 10^{-3} Torr.[250]

Carrier and purge gas

An inert gas (often nitrogen or argon) is used to carry along the precursor vapours and to purge the reactor chamber. Each source tube is connected both to the inert gas and the reaction chamber (Fig. 2.20). A continuous flow of the inert gas enters the source tube between the source and the reaction chamber. When the source valve is OPEN, the carrier gas flow transports the precursor to the reactor chamber. When the source is CLOSED, the gas flow purges the reaction chamber and the source tube.

The continuous flow of the inert gas is regulated with mass flow controllers (MFCs). The optimum operating pressure for viscous flow reactors is about 0.1-10 Torr.[251] The flow rate of the carrier gas is optimised together with the total pressure and the reactor geometry to obtain the optimum combination of process speed, precursor transportation, precursor use efficiency and inert gas valving and consumption. Carrier gas purity is very important because it can be a source of impurities in the ALD process. A minimum of 99.999 % purity is recommended.[230]

Sources

Depending on their vapour pressure, the source chemicals can be classified into two groups. If their vapour pressure at room temperature is higher than the total pressure inside the reactor (gases and high volatile liquids) the sources are dosed into the reactor from their external cylinders via vapour draw. The precursor vapour is drawn from the bubbler to the

chamber by opening a fast valve and once it enters into the reactor it is further transported by the carrier gas flow. The dose is determined by the valve opening times. If the source chemicals have lower vapour pressures, they need bubblers or additional carrier gases to lead them into the reactor. The dose in this case is determined by the bubbling time, the bubbler temperature and the carrier gas flow rate.

Precursor dosing is controlled by MFCs to achieve the desired flow rate. They need to be heated together with the source lines and the valving system to ensure effective transportation. It is very important to avoid 'cold spots' and hot spots' on the walls which can lead to precursor molecules condensation or decomposition, respectively.[230] For example, in the growth of oxides where water is used as oxygen source, long purge periods may be required to desorb precursor molecules adsorbed on 'cold spots'.

Reaction chamber

When precursor molecules are pulsed into the reaction chamber and transported by the carrier gas along the substrate surface, they diffuse by a succession of random collisions with other molecules, the reactor walls and with the substrate. Lower process pressures favour the diffusion of reactants in the carrier gas but reduce the carrier gas precursor transport capability. The optimal operation pressure is a trade-off between these two factors and the pumping speed.[236]

Since most ALD precursors are air sensitive,[230] the reactor chamber must ensure a clean deposition environment. It is also important for the chamber and the lines that are purged or evacuated to have small volume and uniformly heated walls in order to avoid long purge times. The substrate holder is used to provide a uniform temperature for the substrate surface. Resistance based heating coils are often used embedded in the substrate holder to

achieve uniform heating, and thermocouples are generally used to measure and provide active feedback of temperatures at multiple locations in ALD reactors.

2.3.3. High-κ gate oxides for GaN-based materials by ALD

As previously mentioned in section 2.2.2.3, ALD has been used to deposit high-κ oxides as gate dielectrics to improve the properties of GaN-based MOSHEMTs. Due to their high dielectric constant and sufficient bandgap with respect GaN, the most promising oxide materials include: Al_2O_3, HfO_2, ZrO_2, and Ta_2O_5.[124-129, 142, 143] A significant reduction of the gate leakage current of the HEMTs has been reported for all of these dielectrics.

ALD Al_2O_3 ($\kappa \sim 9$)[252] is the most widely investigated candidate as high-κ gate dielectric for GaN-based HEMTs.[126, 253] This is due to its considerably larger bandgap (6.4 eV)[159] with respect other high-κ materials, large breakdown electric field (5–10 MV/cm),[254] high chemical and thermal stability,[255] and ease of deposition.[254] Al_2O_3 grown by ALD was first reported in the late-80s and early-90s.[256, 257] The ALD process of Al_2O_3 has been developed as a model ALD system because its surface reactions are very efficient and self-limiting due to the formation of a very strong Al-O bond. The excellent electrical properties of ALD Al_2O_3 make it currently one of the best candidates as high-κ gate oxide and for the passivation of semiconductor surfaces.[258, 259] In recent years, Al_2O_3 deposited by ALD on GaN surfaces has been the subject of several studies.[162, 260-262] ALD-Al_2O_3/GaN has shown promising results and reduced interface trap states when compared to other deposition techniques such as metal-organic chemical vapour deposition (MOCVD)-Al_2O_3 or oxidation of a thin Al surface layer to form Al_2O_3.[263] Some reports suggest that the Al_2O_3/GaN interface has reduced trap states as compared to the Al_2O_3/AlGaN interface.[263-265] Since AlGaN/GaN HEMT structures normally have GaN capping layers on

the top of the AlGaN barrier to improve the device characteristics,[266, 267] the learning obtained from GaN MOS devices can also be used for the improvement of AlGaN/GaN MOSHEMT devices. Therefore, Al_2O_3 shows excellent performance in suppressing gate leakage and current collapse in GaN-based devices.[125, 126, 258] However, its dielectric constant is relatively low compared to other high-κ oxides. For this reason, other ALD materials with higher dielectric constant and sufficient bandgaps such as HfO_2, ZrO_2 and Ta_2O_5 have also been investigated as gate dielectrics for GaN-based HEMTs.

HfO_2 has also been studied as a gate dielectric for GaN-based devices.[127, 268] Although it has a smaller bandgap (5.8 eV)[159] compared to Al_2O_3, HfO_2 has been applied in Si CMOS technology and intensively studied in III–V MOS devices due to its high dielectric constant (κ ~ 18–20).[252] The valence band and conduction band offsets of Al_2O_3 and HfO_2 deposited by ALD on GaN have experimentally been determined to be 1.8 eV and 1.3 eV for ALD-Al_2O_3 on GaN and 1.4 eV and 1.0 eV for ALD-HfO_2 on GaN, respectively.[159] This values demonstrate that energy-band offsets of both ALD-Al_2O_3 and ALD-HfO_2 from GaN are large enough (≥ 1eV) in order to ensure a significant barrier height for low gate leakage currents. Excellent electrical properties such as low interfacial density of defects, low leakage current density and negligible current collapse have been observed with ALD-HfO_2/GaN HEMTs. These devices have shown a reduction in leakage current of six orders of magnitude.[127, 269] However, HfO_2 is less chemically and thermally stable than Al_2O_3. Studies on Si have shown that amorphous HfO_2 starts crystallising at only 300-500 °C,[128, 270] which is a huge disadvantage since grain boundaries can enhance leakage. Furthermore, in a systematic study of ALD Al_2O_3/GaN, HfO_2/GaN and HfO_2/Al_2O_3/GaN capacitors, the formation of an interfacial layer between the ALD-HfO_2 and the GaN surface has been observed whereas the absence of an interfacial layer at the ALD-Al_2O_3/GaN interface has been confirmed.[252] A high quality interface has been

achieved in an AlGaN/GaN MOSHEMT fabricated using a stacked ALD-HfO_2/Al_2O_3 structure together with a good surface passivation effect of the Al_2O_3 layer and a reduction of the gate leakage current.[269] In addition to the HfO_2/Al_2O_3 stack, research has been carried out into ALD-HfAlO alloys as gate dielectric for AlGaN/GaN HEMTs in order to combine the thermal stability and larger bandgap of Al_2O_3 with the higher dielectric constant of HfO_2.[271, 272]

ZrO_2 is comparable to HfO_2 due to its dielectric constant of $\kappa \sim 20$ and bandgap of 5.8 eV.[273] MOSHEMTs fabricated with ALD-ZrO_2/Al_2O_3 gate dielectric stack have shown that the use of the ZrO_2 results in a suppressed reverse gate leakage current.[108] Recent studies of HfO_2 and ZrO_2 films deposited by ALD on GaN showed an improvement on the oxide/GaN interface for the ZrO_2 samples over the HfO_2 samples.[274] However, ALD-ZrO_2/GaN HEMTs devices have shown a reduction in leakage current of four orders of magnitude,[275] which is smaller than the reduction observed with HfO_2. Therefore, ZrO_2 is less effective than HfO_2 as gate dielectric.

Ta_2O_5 is a transparent oxide also considered as gate dielectric for GaN-based devices due to its large dielectric constant of $\kappa \sim 25$,[276] and its sufficient bandgap of ~ 4.4 eV.[277] Ta_2O_5 has shown advantages compared to traditional dielectric materials. In a comparative study of ALD Ta_2O_5 and HfO_2 on AlN/GaN HEMTs, Ta_2O_5 showed better device performance than HfO_2, which is likely related to its higher dielectric constant.[143] In addition to this, Ta_2O_5 is characterised by a comparable gate leakage current despite its lower bandgap.[143] This study suggests that the use ALD-Ta_2O_5 as gate dielectric for GaN-based devices could be advantageous.

In summary, GaN-based MOSHEMT transistors have shown great potential as a substitute for Si technology for next-generation power electronics. However, it is believed

that defect states on the GaN surface and at the dielectric/GaN interface play a critical role in gate leakage either through a trap-based tunnelling/emission mechanism or Schottky barrier pinning, degrading device performance and reliability. Research has been carried out to mitigate the effects of these states using gate dielectrics that generate an additional barrier for tunnelling and emission processes. Al_2O_3 deposited by ALD is currently one of the most competitive high-κ gate dielectrics for GaN-based MOSHEMTs despite its lower dielectric constant due to its large bandgap, chemical and thermal stability and ease of deposition. On the other hand, higher dielectric constant materials such as HfO_2, ZrO_2, and Ta_2O_5 are also promising. However, in addition to lower bandgap and stability, these oxides have negative bulk charge attributed to oxygen-related defects, which could affect the 2DEG carrier concentration and facilitate the leakage current.[158] Compared to HfO_2 and ZrO_2, Ta_2O_5 has shown better device performance due to its higher dielectric constant, as well as comparable gate leakage current despite its lower bandgap. The optimal combination of the complementary characteristics of Al_2O_3 and Ta_2O_5 could achieve a higher dielectric constant with respect Al_2O_3 together with larger bandgap and higher chemical and thermal stability with respect Ta_2O_5. This thesis investigates for the first time the optimal combination of the complementary characteristics of Al_2O_3 and Ta_2O_5. ALD of Al_2O_3 with Ta modulation doping is used to grow $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ as a novel gate oxide for GaN-based MOSHEMTs.

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3. Experimental Methods

3.1. Atomic layer deposition growth system

The oxide layers studied in this thesis were deposited at the University of Liverpool using an Oxford Instruments OpAL thermal ALD reactor. Figure 3.1 represents a schematic of the reactor. The OpAL is an open-load reactor composed of a 200 mm sample holder with a temperature range of 25-400 °C, two vapour draw precursor lines (connected to bubblers 1 and 3), two bubbling lines with maximum source temperature of 200 °C (connected to bubblers 2 and 4), and a perpendicular flow chamber. The reactor uses three different gas lines for precursor dosing (blue line), precursor purging (orange line) and ammonia (red line), respectively. Argon (BOC 99.998 %) is used for both dosing and purging, whereas Ammonia (Air products, electronic grade) is used as a nitrogen containing co-reactant. Each line has a Mass Flow Controller (MFC) with a maximum flow rate of 500 sccm for the argon lines and 20 sccm for the ammonia line. An Adixen A103P dry pump that achieves a base pressure of about 3 mTorr is used to evacuate the reactor.

For the deposition of the Ta-doped Al_2O_3 oxide layers during the present project, the aluminium source was connected to one of the vapour draw lines and the tantalum source was connected to one of the bubbling lines. The other vapour draw line was connected to the water source and used as the co-reactant line. Electronic grade trimethylaluminium (TMA) and pentakis(dimethylamino)tantalum (PDMAT) (supplied by SAFC Hitech®) were used as the aluminium and tantalum sources, respectively, whereas de-ionised (DI) water was used as the oxygen containing co-reactant. The TMA and H_2O were both held at room temperature and delivered using vapor draw, whereas the PDMAT was heated to 75 ºC using a heat jacket and transported with the assistance of 100 sccm of argon using a dip-leg bubbler. The line between the PDMAT bubbler and the chamber was heated at

90 ºC to avoid condensation of the precursor vapour during transport. Finally, in order to avoid cold spots in the reactor walls, the sample holder was heated at the deposition temperature (which ranged from 100 ºC to 375 ºC), the upper and lower chamber were heated to temperatures between 100 ºC and 150 ºC (depending on the deposition temperature) and the exhaust line was heated to 100 ºC. The reactor temperatures, gas flows and dosing were all controlled by the ALD reactor software.

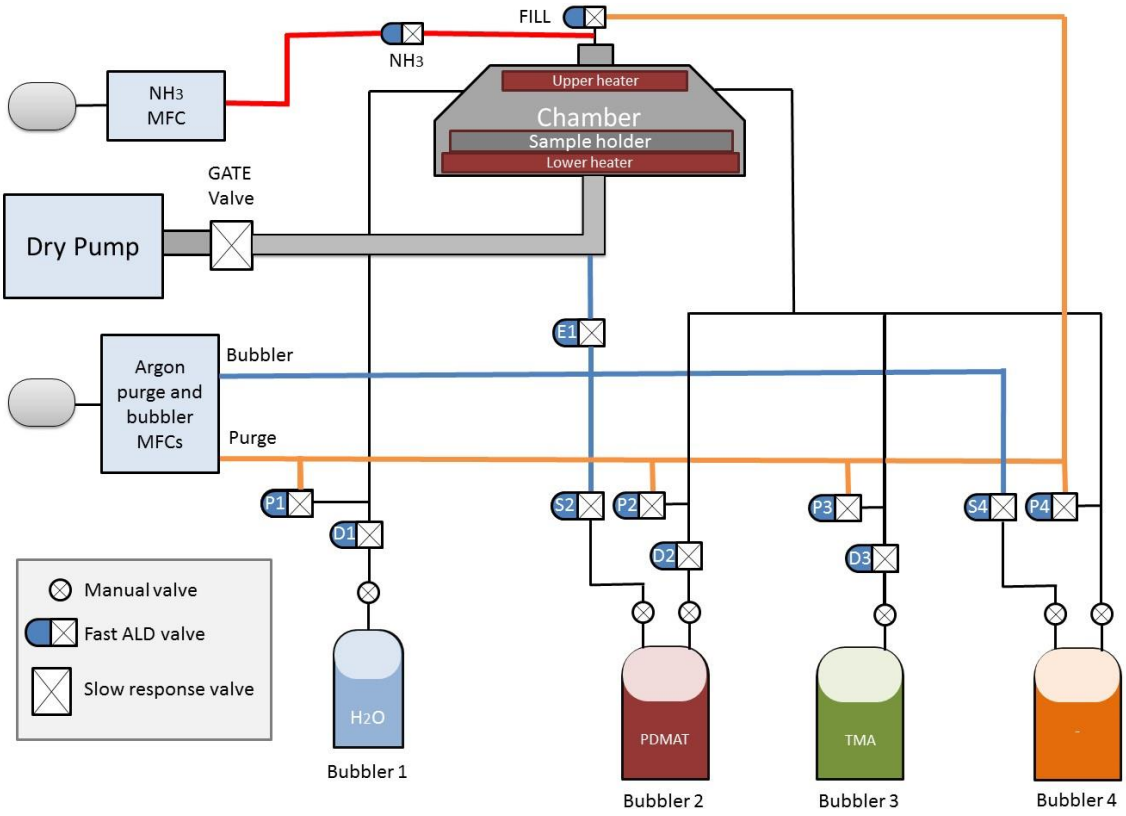

FIG.3.1: Schematic illustration of the OpAL thermal ALD reactor.

Tables 3.1 and 3.2 below show a summary of the growth parameters used during the present project for the TMA and PDMAT based ALD cycles. The flow rates as well as the pulse and purge times used in this thesis were selected based on previous work carried out in the same reactor.[1-3] Throughout the process, the overall argon flow into the reactor was

maintained at 200 sccm, giving a chamber pressure of approximately 200 mTorr. An initial step was included at the beginning of each process to stabilise the gas flow into the reactor. This flow set step consisted of an Ar purge flow of 200 sccm through the FILL valve for 10 s. The TMA precursor was dosed for 20 ms into the reactor chamber through D3 valve alongside an Ar purge of 200 sccm via the FILL valve to avoid the injected precursor getting trapped within the top part of the chamber. The TMA precursor purge was carried out for 5 s using an Ar purge of 200 sccm through the FILL valve. The PDMAT precursor dose was carried out through D2 valve for 4 s by bubbling 100 sccm of Ar through S2 while an additional Ar purge of 100 sccm was fed into FILL valve. An additional step was used to compensate for any slight delay when closing D2 after bubbling PDMAT in order to avoid the precursor going up the dip-leg of the bubbler. An Ar flow of 20 sccm through S2 and a simultaneous Ar purge of 180 sccm through FILL valve were used during 0.01 s in this step. The PDMAT precursor purge was carried out using an Ar purge of 200 sccm through P2 and FILL valves. For the H_2O co-reactant dose through D1 valve, a simultaneous Ar purge of 200 sccm through P1 valve was used. For the co-reactant purge, an Ar purge of 200 sccm through P1 was used for 5 s. Each TMA ALD cycle (n_{TMA}) consisted of a TMA precursor dose followed by a precursor purge and then a H_2O co-reactant dose followed by a co-reactant purge, whereas each PDMAT ALD cycle (n_{PDMAT}) consisted on a PDMAT precursor dose followed by a purge and then a H_2O co-reactant dose followed by a purge. Tantalum doping of Al_2O_3 was realised using delta doping where TMA based ALD cycles were periodically interspersed with PDMAT ALD cycles.

TABLE 3.1. Summary of the growth parameters of the TMA based ALD cycles used to deposit Al_2O_3.

TMA ALD cycle			
Step	**Time**	**OPEN valves**	**Ar purge**
TMA dose	20 ms	D3 FILL	200 sccm
TMA purge	5 s	FILL	200 sccm
H_2O dose	20 ms	D1 P1	200 sccm
H_2O purge	5 s	P1	200 sccm

TABLE 3.2. Summary of the growth parameters of the PDMAT based ALD cycles used to deposit Ta_2O_5.

PDMAT ALD cycle				
Step	**Time**	**OPEN valves**	**Ar bubbler**	**Ar purge**
PDMAT dose	4 s	S2,D2 FILL	100 sccm	100 sccm
Close D2 delay	0.01 s	S2 FILL	20 sccm	180 sccm
PDMAT purge	5 s	P2 FILL	-	200 sccm
H_2O dose	20 ms	D1 P1	-	200 sccm
H_2O purge	5 s	P1	-	200 sccm

3.2. Post-deposition thermal annealing processing

Two types of post-deposition annealing processes were performed during the present project. Firstly, ALD oxide films deposited on Si(100) substrates were annealed at the University of Liverpool to investigate their crystallisation temperature using a carbolite tube furnace 12/65/550 with maximum temperature of 1200 ºC and maximum ramping rate of 5 ºC/min. The carbolite tube furnace uses a resistive heating element around the ceramic work tube of ~ 5 cm inner diameter and ~ 1 m length, and a thermocouple for temperature control. The work tube heated length is divided into 3 zones. An extended uniform zone in

the mid-section is achieved with the use of end zone controllers that track the temperature in the centre and compensate for the loss of heat from the tube furnace ends. The samples were annealed in nitrogen ambient for 30 min at temperatures ranging from 600 ºC to 1000 ºC. The process was carried out with zero grade Nitrogen (supplied by BOC) to replicate the annealing gas as used for HEMT processing.[4] The range of temperatures was selected to cover the annealing temperatures typically used for HEMT processing, which are normally under 800 ºC as higher temperatures result in device degradation.[5-7] For each process, once the work tube was heated up to the desired temperate, the tube was evacuated of atmospheric gases by purging the tube with nitrogen. This was achieved by setting the output pressure at the regulator to 2 atmospheres and setting the flow regulator to its most open setting. As the regulator was used for several gas types with different molecular masses, it was not possible to determine the precise gas flow. Once the tube was evacuated the end cap was removed and the samples were inserted into the middle of the tube within an alumina boat, while continuing the high flow nitrogen purge. The end cap was then replaced and the nitrogen flow was reduced to approximately half its maximum value. After annealing for the required time, the nitrogen flow was set to its highest value and the end cap was removed, allowing the sample to be positioned at the cooler end of the tube. The end cap was replaced and the samples were allowed to cool down for ~ 5 min before they were taken out to reduce thermal internal stress in the samples. To unload the samples, the loading process was repeated in reverse.

Rapid thermal annealing (RTA) was performed at IMRE (Singapore) after ALD of the oxide films on top of GaN-based HEMT samples. The instrument used was a Jipelec JetFirst 150 rapid thermal processing (RTP) system for III-V materials with capability up to 150 mm diameter wafers. The RTP features a temperature measurement and control system to provide accurate and repeatable thermal behaviour. The system is heated with

halogen lamps and uses cold wall chamber technology. The maximum operation temperature is 1200 ºC, with a maximum ramp rate of 150 ºC/s. For temperature control the system uses a thermocouple for annealing temperatures up to 600 ºC, and a pyrometer for temperatures between 600-1200 ºC. The temperature stability is about ± 2 ºC. The system is connected to N_2, O_2 and Ar process gases and to a N_2 purge gas line. The RTA process can be carried out at atmospheric pressure or under vacuum. Figure 3.2 shows a diagram of the RTA process used in this project. The samples were annealed in nitrogen at 600 ºC for 60 s. This RTA condition is the same as used for the purpose of forming the source and drain ohmic contacts on the HEMT structures using an Au-free CMOS-compatible Ta/Al/Ta metallisation scheme.[4] Once the samples were loaded, the chamber was evacuated before the nitrogen flow was set to 1500 sccm, giving a chamber pressure of approximately 1 bar. The temperature was then ramped up to 600 ºC over 90 s. After annealing at 600 ºC for 60 s, the temperature was ramped down to room temperature over 60 s in N_2. Finally, the samples were left to cool down for 5 min before unloading.

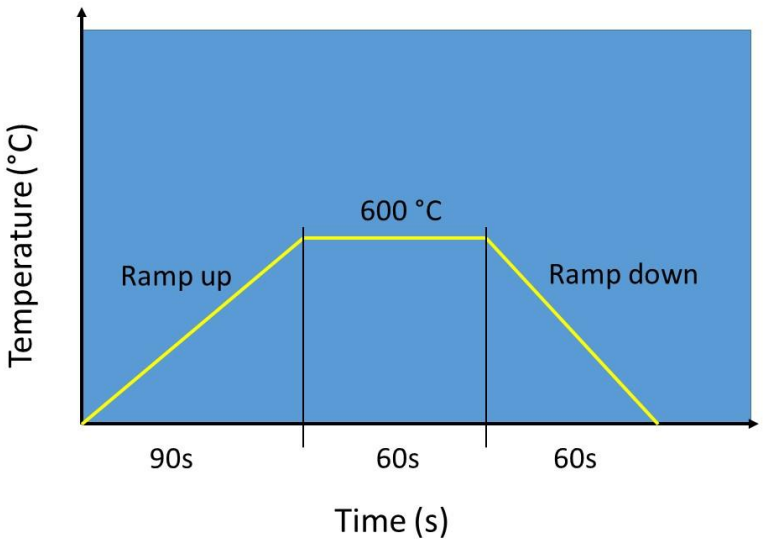

FIG.3.2: Diagram of the RTA process used in this project.

3.3. Characterisation tools

3.3.1. Ellipsometry

Spectroscopic ellipsometry (SE) was used routinely during the project to analyse the thickness and refractive index of the ALD oxide layers. Ellipsometry is an optical technique that can be used to characterise thin film properties such as thickness, refractive index, composition and roughness, by measuring the change in state of polarisation of a light beam that interacts with the sample.

Light can be described as an electromagnetic wave consisting of an electric field vector and a magnetic field vector, both perpendicular to the direction of propagation of light and mutually perpendicular. The electric field vector is the quantity which describes the light wave. When a light beam hits an interface between two media, it slows down if the refractive index of the second medium is higher, changes direction and can be absorbed and/or reflected by the second medium. Polarisation refers to the behaviour of the electric field vector observed at a fixed point in space and time.

When the light wave arrives at the sample surface, one part of that wave is reflected and the other part is transmitted (Fig. 3.3). Reflection leads to a modification of the polarised light. The components of the reflected polarised light can be described by the Fresnel coefficients, r_p and r_s, defined by the Fresnel equations:[8]

$$r_p = \frac{E_p^r}{E_p^i} = |r_p|\exp(i\delta_p) \tag{3.1}$$

$$r_s = \frac{E_s^r}{E_s^i} = |r_s|\exp(i\delta_s) \tag{3.2}$$

where E_s and E_p are the components of the incident (i) and the reflected (r) electric field, perpendicular and parallel to the plane of incidence, respectively, and δ_p and δ_s are the relative phase before and after the reflection, respectively.

The ratio ρ of these two coefficients is defined by the fundamental equation of ellipsometry:

$$\rho = \frac{r_p}{r_s} = \tan(\Psi)e^{i\Delta} \tag{3.3}$$

where Ψ and Δ are the ellipsometric angles that represent the amplitude and the phase shift caused by the reflection respectively:

$$\tan(\Psi) = \frac{|r_p|}{|r_s|} \tag{3.4}$$

$$\Delta = \delta_p - \delta_s \tag{3.5}$$

Therefore, the Ψ and Δ values can be calculated by measuring the change in state of polarisation of a light beam caused by the reflection on the material surface.

Ellipsometry is an indirect method which converts the measured Ψ and Δ values into the optical constants of the material by performing a model analysis. Direct conversion of Ψ and Δ is only possible for isotropic, homogeneous and infinitely thick films. In the rest of cases, a model considering the optical constants and thickness parameters of all individual layers of the sample needs to be set. The model uses an iterative procedure where the unknown parameters are varied to calculate Ψ and Δ using the Fresnel equations. The values of Ψ and Δ that are closest to the measured data give the optical constants and thickness parameters of the sample. Therefore, ellipsometer measurements can be used to describe a model that uses mathematical relations (called dispersion formulae) to evaluate the thickness and the optical properties of the material by adjusting specific fit parameters.

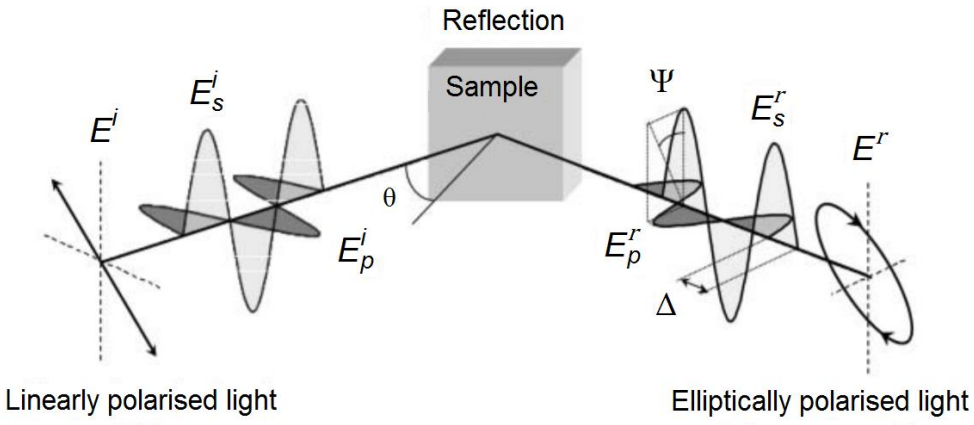

FIG.3.3: Schematic illustration of spectroscopic ellipsometry.

The ellipsometer used during the present project was a Horiba Jobin Yvon Spectroscopic Ellipsometer (located at the University of Liverpool). SE utilises broad band light sources that cover a specific range in the infrared, visible or ultraviolet spectral region. The ellipsometer includes a light source, a polariser, an analyser, a monochromator and optical fibres used to couple the light beam from the output light source to the input of the polariser and from the output of the analyser to the input of the monochromator, respectively (Fig. 3.4). The unpolarised light becomes linearly polarised when it travels through the polariser, which defines the state of polarisation before the light strikes the sample. After reflection on the material surface, the light becomes elliptically polarised. The modulator induces a modulation of the state of polarisation that makes the ellipticity of the polarisation to vary as a function of time. An analyser similar to the polariser is located after the sample and the photoelastic modulator. Finally, the monochromator separates the light into its various components before it reaches the detector.

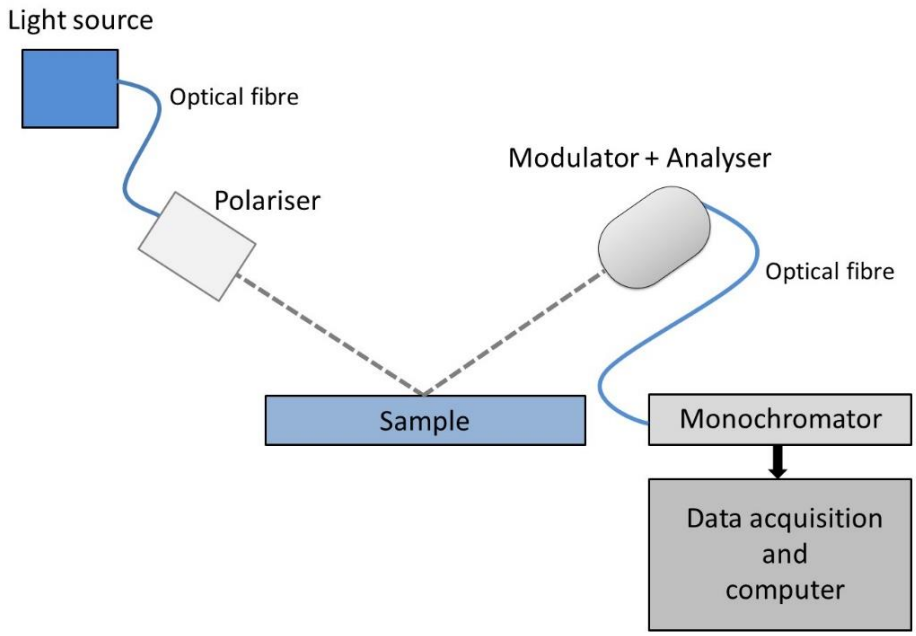

FIG.3.4: Schematic of spectroscopic ellipsometer.

The light source used by the ellipsometer was a blue LED and a Xenon arc lamp of 75 W with a spectral range from 430 nm to 850 nm and an angle of incidence of ~ 70 °. The modulator used in the spectroscopic ellipsometer was a photoelastic modulator. The ellipsometer was controlled by DeltaPsi2 software, which provides a complete measurement and modelling package for accurate and flexible characterisation of thin film structures, with features including calculation of thickness, alloy composition and optical constants. DeltaPsi2 integrates a materials database with references and dispersion relations required for accurate characterisation of the different material optical constants.

Dispersion model

The model used to define the ALD oxide films in this project was the 'New Amorphous' mathematical model, which showed the best fitting results within the wavelength range used by the Horiba Jobin Yvon Spectroscopic Ellipsometer. The New Amorphous dispersion formula has been derived by Horiba Jobin Yvon in order to give a Lorentzian

shape to the expressions of the extinction coefficient and refractive index of the material (Figs. 3.5 and 3.6):[9]

$$k(\omega) = \begin{cases} \frac{f_j(\omega-\omega_g)^2}{(\omega-\omega_g)^2+\Gamma_j^2} & \text{for } \omega > \omega_g \\ 0 & \text{for } \omega \leq \omega_g \end{cases} \tag{3.6}$$

$$n(\omega) = n_\infty + \frac{B(\omega-\omega_j)+C}{(\omega-\omega_j)^2+\Gamma_j^2} \tag{3.7}$$

where

$$\begin{cases} B_j = \frac{f_j}{\Gamma_j}\left(\Gamma_j^2 - (\omega_j - \omega_g)^2\right) \\ C_j = 2f_j\Gamma_j(\omega_j - \omega_g) \end{cases} \tag{3.8}$$

- n_∞ is a parameter which is bigger than one and equal to the value of the refractive index when $\omega \to \infty$.
- f_j is related to the strength (or amplitude) of the extinction coefficient peak. Generally, $0 < f_j < 1$.
- Γ_j is the broadening term of the peak of absorption. Generally, $0.2 < \Gamma_j < 8$
- ω_j is approximately the energy at which the extinction coefficient is maximum (peak of absorption). Generally, $1.5 < \omega_j < 10$
- ω_g is the energy bandgap or energy from which the absorption starts to be non-zero: $k(E \geq E_g) \geq 0$ and $\omega_g < \omega_j$

Figures 3.5 and 3.6 show the refractive index and extinction coefficient parameters given by the New Amorphous function for amorphous Al_2O_3 and Ta_2O_5, respectively.[9]

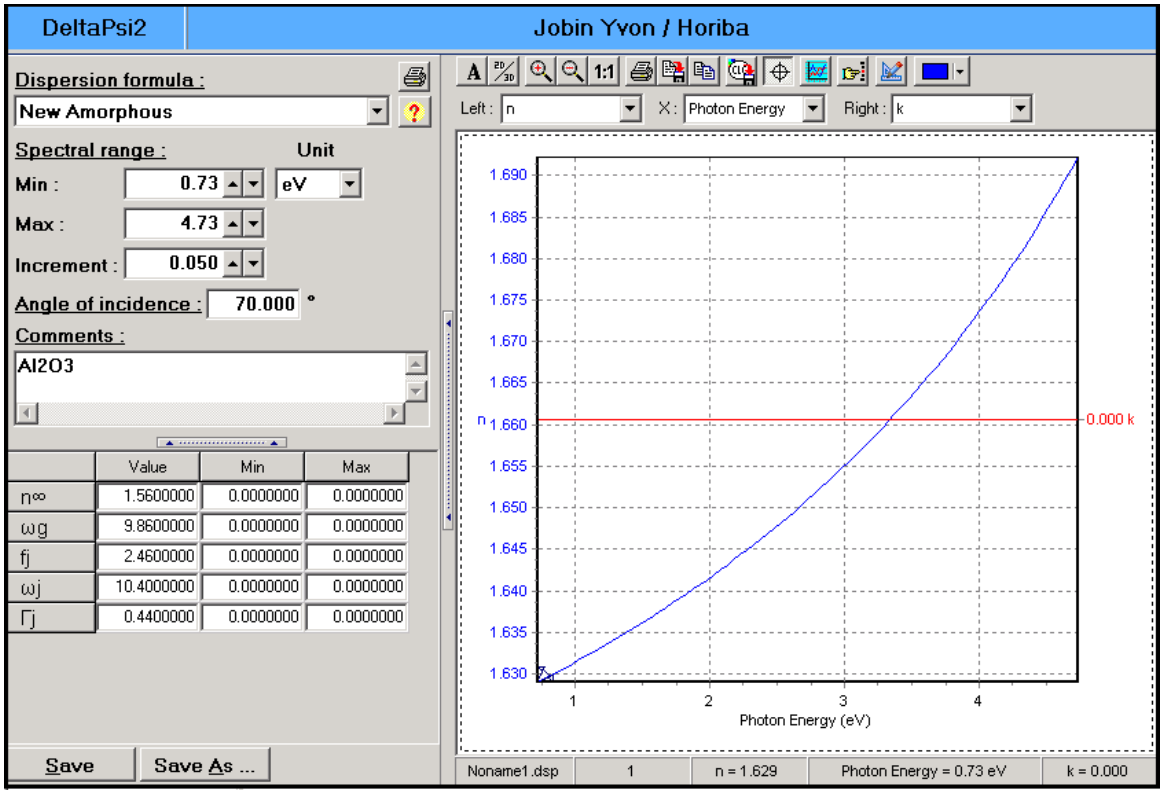

FIG.3.5: Optical properties of amorphous aluminium oxide given by the New Amorphous function.[9]

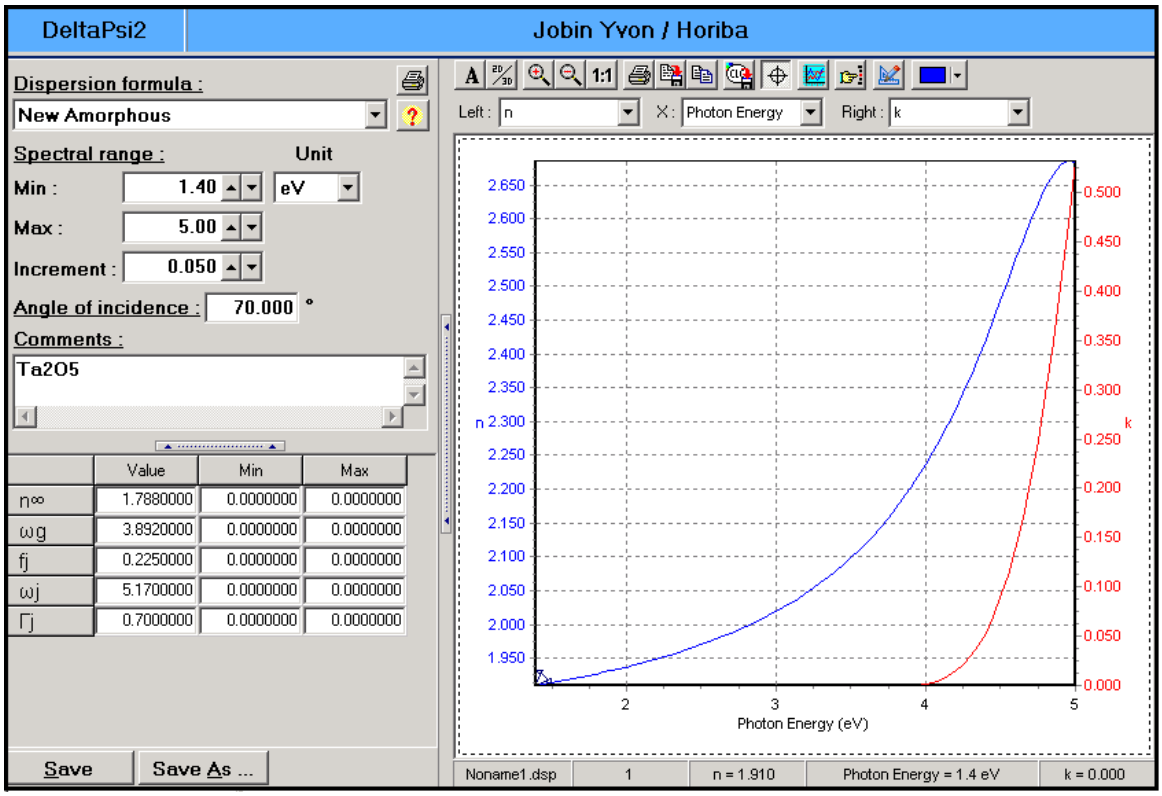

FIG.3.6: Optical properties of amorphous tantalum oxide given by the New Amorphous function.[9]

The New Amorphous model shows good results for amorphous materials exhibiting an absorption in the visible and/or FUV range such as absorbing dielectrics (i.e. Al_2O_3 and Ta_2O_5). However, following the recommendations made by Horiba,[9] in order to determine the validity of the New Amorphous model, the results obtained were compared between the New Amorphous dispersion formula and the Tauc-Lorentz dispersion formula as the Tauc-Lorentz model may fit better the absorption part of the experimental spectrum.[10]

Figure 3.7 shows an example of the thickness (Fig. 3.7.a) and refractive index (Fig. 3.7.b) values determined for the ALD Ta-doped Al_2O_3 films as a function of the PDMAT cycle fraction ($n_{PDMAT}/n_{TMA+PDMAT}$) using both the New Amorphous (blue) and Tauc-Lorentz (red) ellipsometry models. The difference in the values obtained experimentally is < 5 % for thickness and < 7 % for refractive index, which indicates that the parameters calculated using the Tauc-Lorentz dispersion formula do not significantly differ from the ones obtained using the New Amorphous dispersion formula. In addition to the better mathematical fit observed for the New Amorphous model (with fitting errors <1 Å), the thickness and refractive index values obtained using the New Amorphous dispersion formula are closer to the expected theoretical values (dashed lines) and the thickness measured for selected samples using transmission electron microscopy (TEM), which is a more accurate direct measurement technique (see section 3.3.5). Thus, the values of thickness and refractive index utilised during the present thesis were the values obtained using the New Amorphous model.

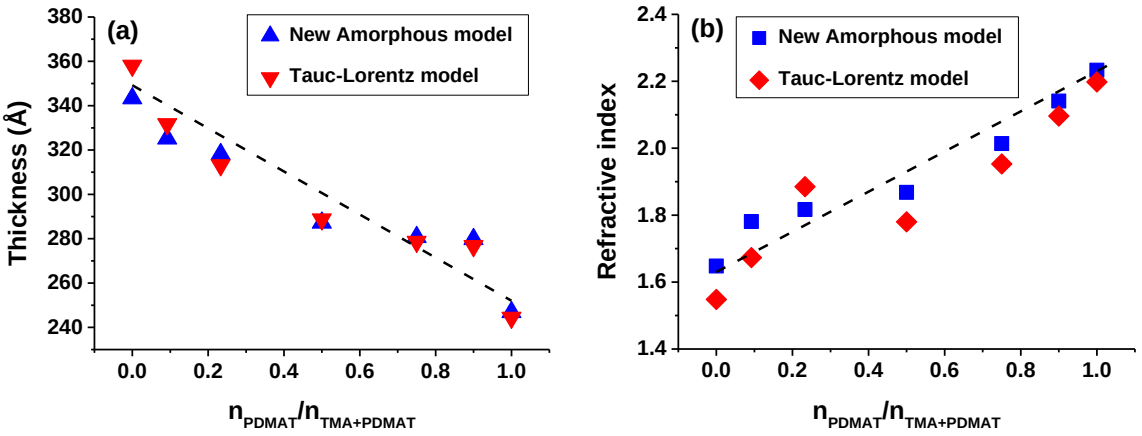

FIG.3.7: (a) Thickness and (b) refractive index of the ALD Ta-doped Al_2O_3 oxide films grown on Si(100) at 250 ºC using n = 360 ALD cycles as a function of the PDMAT precursor ALD cycle fraction.

It should be noticed that the errors of the thickness and refractive index values obtained in this project have not been estimated. This is due to the large number of factors that contribute to the error in the ellipsometry method, which makes it very difficult to compare the simulation with the experimental data in a quantitative way. The goodness of fit of the spectra as a function of the wavelength in SE can be assessed both quantitatively and qualitatively. Quantitatively, fitting errors are calculated based on the least-squares method,[11] whereas the qualitative assessment is performed by comparing on the same graph the experimental spectra together with the simulated spectra to examine how well the model fits the experimental data. However, in addition to the calculation errors there are other sources of errors such as sample dependent errors and system dependent errors. Sample dependent errors are a function of the angle of incidence, the ambient refractive index, the film refractive index, the substrate refractive index and the film thickness.[12] System dependent errors include systematic errors and calibration constants. Systematic errors arise from inaccurate system parameters such as the monochromator resolution or the angle of incidence, and calibration constants include the attenuation constant that accounts for the fractional attenuation of the signal by the electronic circuitry of the detector, the polariser

starting angle and the analyser starting angle.[12] For this reason, ellipsometry studies typically do not report an error for the obtained values of the parameters in the optical model and the derived parameters.[13]

3.3.2. X-ray diffraction

X-ray diffraction analysis (XRD) was performed to study the microstructure of the ALD oxide films before and after post-deposition annealing. XRD is a technique used to analyse the crystallographic structure of materials and layers. X-rays are waves of electromagnetic radiation with wavelengths of the same order of magnitude than the interatomic distances in a crystal (between 0.1 Å and 100 Å approximately),[14] which allows crystal structures to diffract x-rays.

When an x-ray strikes the crystallographic planes (*hkl*) of a sample with an angle of θ (Fig. 3.8), it can either be transmitted along its original direction or it can be scattered by the atoms in the material. When scattered x-rays add constructively, a new wave with larger amplitude is created and peaks are formed. According to Bragg's law, the constructive wave occurs when the path difference of the two x-ray waves ($2d_{hkl}\sin\theta$) equals an integer multiple of the wavelength (λ) of the incident x-ray. The distance between two or more parallel (*hkl*) crystallographic planes can be calculated with the relation described by the Bragg's law:[15]

$$n\lambda = 2d_{hkl}\sin\theta \tag{3.9}$$

where n is the integer, d_{hkl} is the atomic spacing of the (*hkl*) planes, λ is the x-ray wavelength and θ is the diffraction angle.

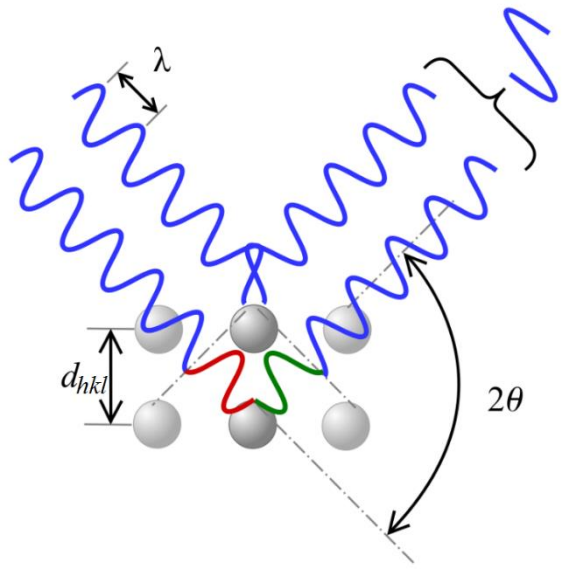

FIG.3.8: Reflection of x-rays by planes of atoms in a crystal.

The x-ray diffractometer used in this project to perform the analysis of the ALD oxide films was a Rigaku Miniflex diffractometer with a Cu $K\alpha$ source ($\lambda_{K\alpha}$ = 1.5405 Å) and a θ/2θ Bragg Brentano configuration (at the University of Liverpool). The angular range set for data collection was from 2θ = 20° to 2θ = 60° to cover the main x-ray diffraction angles of Al_2O_3 and Ta_2O_5 and to avoid a very strong diffraction peak from the Si(100) substrates at ~ 2θ = 70°. The scans were carried out using the 'Fourier transform' method, with scan steps of 0.05° and scan time of 20 s per step. The Fourier transform represents a function in terms of a set of sine-waves. The diffracted x-ray signal is a function that contains a superposition of different waves with different amplitudes, frequency and phase. By performing an inverse Fourier transform, the individual frequencies of the diffracted x-ray waves and their relative strengths can be determined. Since different lattice spacings will diffract x-rays differently, each decomposed sine-wave will give a characteristic of the crystal structure. Therefore, the Fourier transform method is used to isolate the different waves of x-rays that overlap during diffraction. By reconstructing the frequency spectrum from the inverse Fourier transform, the lattice structure can be determined. Finally, the

diffraction patterns obtained experimentally were processed using Peak search 4.0 software licenced from Rigaku, which was utilised to remove the background and noise from the XRD signals.

3.3.3. X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS), also known as electron spectroscopy for chemical analysis (ESCA), was utilised during this project to study the composition, bandgap and band offsets of the ALD oxide films. XPS is a non-destructive quantitative surface analysis technique which provides elemental composition and chemical state information of the surface of solids with a depth resolution up to 10 nm.[16]

Figure 3.9 shows a schematic of the excitation process in photoelectron spectroscopy. XPS uses monochromatic sources of soft x-rays (with a fixed photon energy of 200-2000 eV) to irradiate the area of the sample being analysed using a focused beam with diameter ranging from few mm down to 20 μm. Photoelectron spectroscopy is based on the process that occurs when a photon is absorbed by an atom in a molecule or solid, leading to ionisation and the emission of a core (or inner-shell) electron. If the binding energy of the sample atoms (or energy required to disassemble an atom into free electrons and nucleus) is lower than the x-ray energy that excites the electrons, they will be emitted as photoelectrons. The majority of these electrons will be reabsorbed by the sample, but the electrons emitted from atoms near the sample surface (approximately twenty atomic layers depth)[16] can escape the sample surface. The number of electrons emitted (or photoelectrons) and their kinetic energy distribution can be measured using an electron energy analyser, producing a spectrum of photoelectron intensity versus electron binding energy. Since the binding energies of the photoelectrons are characteristic of the elements from which they are emanated, the identification of the elements in a sample can be made

directly from the kinetic energies of the emitted photoelectrons. In addition, the relative concentrations of elements can be determined from the photoelectron intensities.

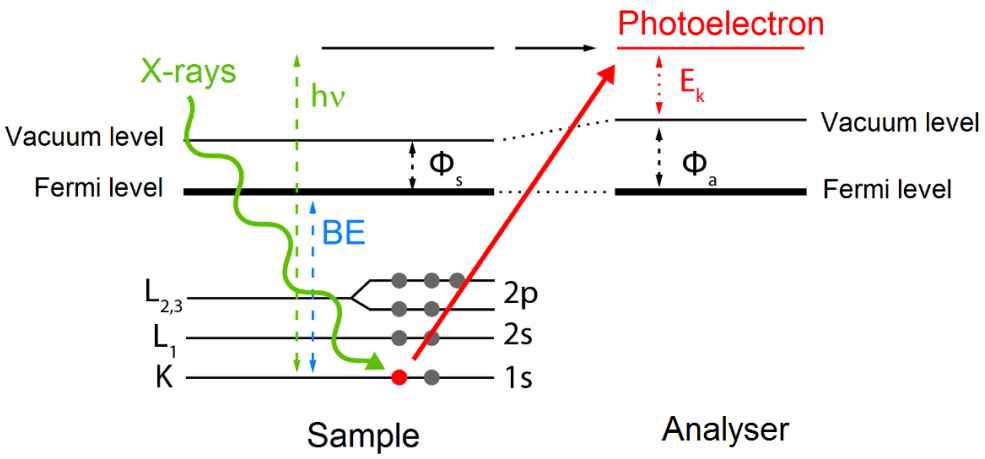

FIG. 3.9: Schematic of XPS excitation process.

The energy of a photon is given by the Einstein relation:[17]

$$E = h\nu \tag{3.9}$$

where h is the Plank constant and ν is the frequency of the radiation.

The process of photoionisation of an atom A can be considered as:

$$A + h\nu = A^{+} + e^{-} \tag{3.10}$$

The conservation of energy requires that:

$$E(A) + h\nu = E(A^{+}) + E(e^{-}) \tag{3.11}$$

Since the electron energy is present as kinetic energy, the equation can be arranged as:

$$E_K = h\nu - (E(A^{+}) - E(A)) \tag{3.12}$$

Where the final term in brackets represents the difference in energy between the ionised and the neutral atoms (also called binding energy or BE) of the electron, which leads to the following equation:

$$E_K = h\nu - E_B \quad (3.13)$$

Since the binding energies of the energy levels in a solid are conventionally measured with respect to the Fermi level of the solid rather than the vacuum level, a small correction is needed in the equation given above in order to account for the work function (ϕ), or energy needed to remove an electron from a solid to a point in the vacuum outside the solid surface:

$$E_K = h\nu - (E_B + \phi) \quad (3.14)$$

In practise the work function ϕ is an adjustable instrumental correction factor which depends of both the spectrometer and the material, and accounts for the kinetic energy given up by the photoelectron as it becomes absorbed by the instrument detector. Therefore, if the kinetic energy of the emitted electrons is measured, the corresponding binding energy can be calculated through a subtraction and the elements of the sample can be determined. For a given element, there will be a characteristic binging energy associated with each core atomic orbital. This will give rise to a characteristic set of peaks in the photoelectron spectrum at kinetic energies determined by the photon energy and the respective binding energies.

XPS measurements during the present project were carried out by Dr. Zhang Zheng (IMRE, Singapore) using a high energy resolution VG ESCALAB 200i-XL system. A monochromatic Al Kα x-rays source (1486.7 eV) was used to obtain the core level spectra and the valence band spectra of the samples. All peak binding energies were referenced to the C 1s peak at 285.0 eV to compensate for any variations in the peak core level positions due to binding energy shift caused by surface charging. Finally, the XPS data processing was carried out by myself using Thermo Scientific™ Avantage software in order to obtain quantitative information on composition and chemical states of the samples.

Figure 3.10 shows the XPS spectrum obtained for one of the ALD oxide films. An XPS spectrum is a combination of the number of electrons leaving the sample when irradiated with x-rays and the ability of the instrumentation to record these electrons. Not all the electrons emitted from the sample are recorded by the instrument, and the efficiency with which emitted electrons are recorded depends on the kinetic energy of the electrons which in turn depends on the operating mode of the instrument. As a consequence of this, a direct comparison of peak areas and intensities is not recommended when comparing samples in XPS. A change in the experimental conditions between measurements (such as the x-ray gun power output) will result in a change in the absolute value of the peak intensities. However, if the rest of the parameters are equal, the peak intensities will remain constant in relative terms. For this reason, the best way to compare XPS intensities is via percentage atomic concentrations, which represent the ratio of the intensity to the total intensity of electrons in the measurement.[18]

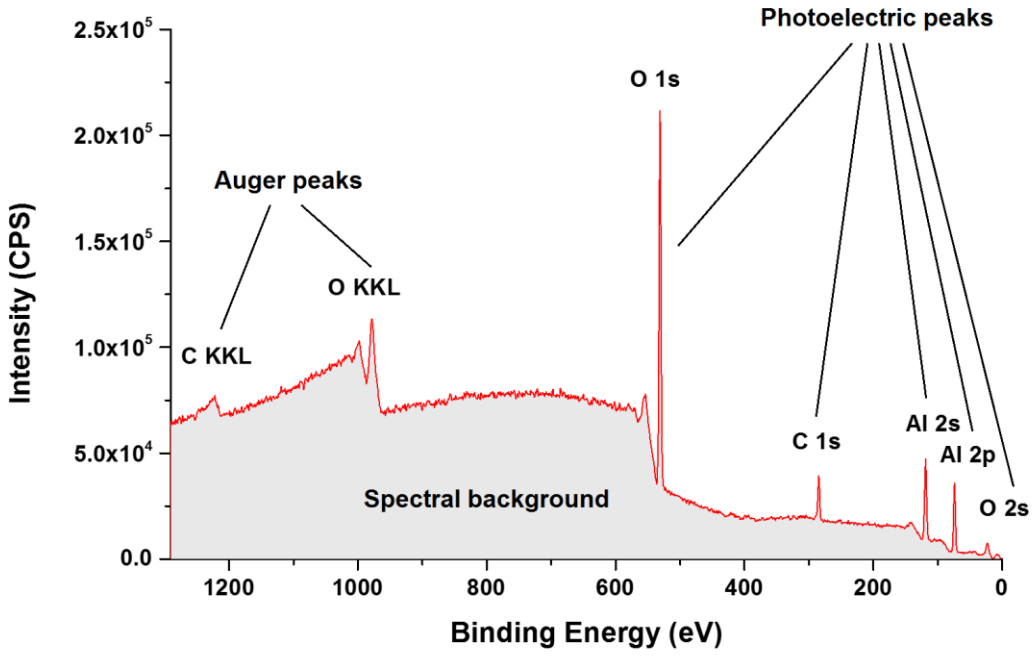

FIG. 3.10: XPS spectrum showing Auger and XPS peaks above the background of scattered electrons.

XPS spectra represent the number of electrons recorded for a given transition, including the background signal and resonance peaks characteristic of the bound states of the electrons in the surface atoms. The resonance peaks above the background are the significant features in XPS spectra. During the quantification of XPS spectra, it is assumed that the number of electrons recorded is proportional to the number of atoms in a given state. The basic tool for measuring the number of electrons recorded for an atomic state is the quantification region, which defines the range of energies over which the signal can be attributed to the transition of interest.[18] Once this range of energies is defined, the background signal not belonging to the peak can be identified and removed. This background results from scattering events that cause photoelectron energy losses prior to emission from the sample. XPS spectra are then quantified in terms of peak intensities and peak positions. The peak intensities measure how much of a material is at the surface, while the peak positions indicate the elemental and chemical composition. Other values such as the peak full width at half maximum (FWHM) are useful indicators of chemical state changes and physical influences. For example, broadening of a peak may indicate a change in the number of chemical bonds contributing to a peak shape, a change in the sample condition (x-ray damage) and/or differential charging of the surface (localised differences in the charge-state of the surface).[18]

3.3.4. Photoluminescence spectroscopy

Photoluminescence (PL) spectroscopy was utilised to analyse the bandgap of the GaN substrates used during the present project. PL is a technique used for the characterisation of the optical and electronic properties of semiconductors or molecules, by measuring the energy of the light emitted by a sample (or photoluminescence) after the absorption of photons.[19]

Figure 3.11 shows a diagram of the PL process for a semiconductor. PL occurs when light photons are absorbed by the semiconductor material, causing electrons to promote into permissible excited energy states in a process called photoexcitation. In PL spectroscopy, the semiconductor is excited with a monochromatic light source that provides photons with an energy larger than the bandgap. When the photons are absorbed, electrons from the valence band are excited to the conduction band and holes are formed in the valence band. The electrons then undergo energy relaxation towards the conduction band minimum. Finally, electrons and holes recombine under either radiative emission of photons with lower energy than the absorbed photons or non-radiation emission generating heat. This emitted light is called PL. The semiconductor bandgap can be determined from the spectral distribution of PL.[20] PL measurements provide an emission intensity versus wavelength spectrum. The higher intensity represents the optical bandgap, and lower intensity emissions are associated to defect states such as impurities.[20]

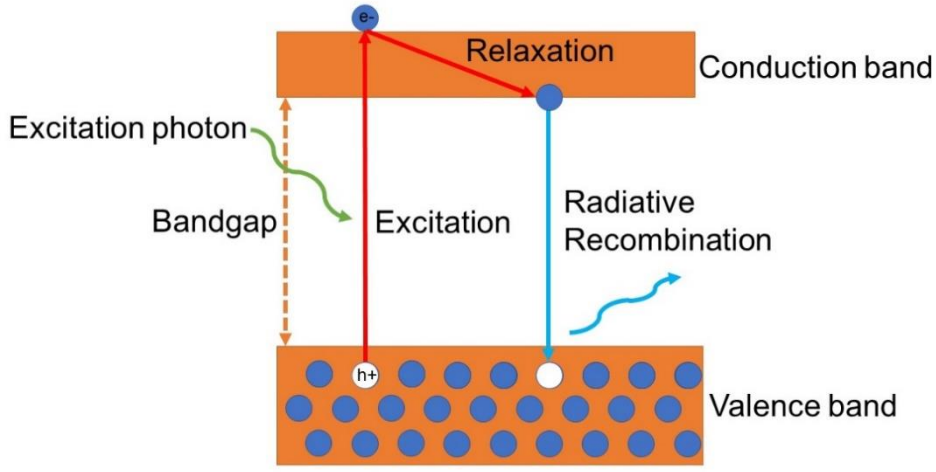

FIG. 3.11: Diagram of the photoluminescence process for a semiconductor.

The PL measurements in this project were performed at room temperature using a Horiba Jobin-Yvon HR-800 UV confocal Raman microscope. A He-Cd ultraviolet (UV) laser with a wavelength of 325 nm (3.841 eV) was used as the excitation source. The

microscope objective utilised was a x40NUV objective with a confocal pinhole of 1000 μm. Prior to the measurements, the system was calibrated using the zero-order diffraction of a white light source to set the zero of the spectrometer, and using the 520 cm^{-1} Raman emission of a silicon calibration sample to calibrate the linear coefficient. LabSpec software was used to adjust the confocal hole (100-1000 μm), the filter controlling the incident light intensity from 0.01-100 %, and the acquisition parameters related to the duration of the scan. The PL signal was collected for a range of wavelengths between 350 nm and 700 nm.

3.3.5. Atomic force microscopy

Atomic force microscopy (AFM) was used to study the surface morphology of the GaN-based HEMT structures before and after the deposition of the ALD oxide layers. AFM is a material characterisation technique that provides 3-dimensional surface profiles with a sub-nanometre vertical resolution by measuring the atomic interactions between a scanning probe and the samples surface.

Figure 3.12 shows a schematic of an AFM. The AFM probe consists of a sharp tip micromachined from Si at the end of a cantilever, with a tip radius of less than 10 nm that gives good resolution and reproducibility. The AFM operates by scanning the tip across the sample surface. A precisely controlled motion of the tip is achieved by controlling the voltages applied to a three axis (x, y, z) piezoelectric transducers (PZT) fitted to the sample holder. When the tip is brought into proximity of the sample surface, the interactive force between the tip and the sample atoms leads to a deflection of the cantilever. The deflection of the cantilever is transmitted to a four-segmented photodiode that detects the position and movement of a laser beam that is reflected at the back of the cantilever. The AFM keeps

the laser beam in the middle of the photodiode by controlling the voltage applied to the PZT and the recorded voltage is converted to the sample height.

The AFM images obtained in this thesis were recorded in tapping mode, in which the tip is attached to the end of an oscillating cantilever (Fig. 3.12). During tapping mode operation, the 'Drive Signal' applied to the 'Tapping Piezo', mechanically oscillates the probe at or near its resonance frequency with an amplitude ranging typically from 20 nm to 100 nm. The tip lightly taps on the sample surface during scanning contacting the surface at the bottom of its swing. The feedback loop maintains a constant oscillation amplitude by maintaining a constant root mean square (RMS) of the oscillation signal acquired by the split photodiode detector. By maintaining a constant oscillation amplitude, a constant tip-sample interaction is maintained during imaging. The vertical position of the PZT scanner at each (x, y) data point is stored by the computer to form the topographic image of the sample surface.

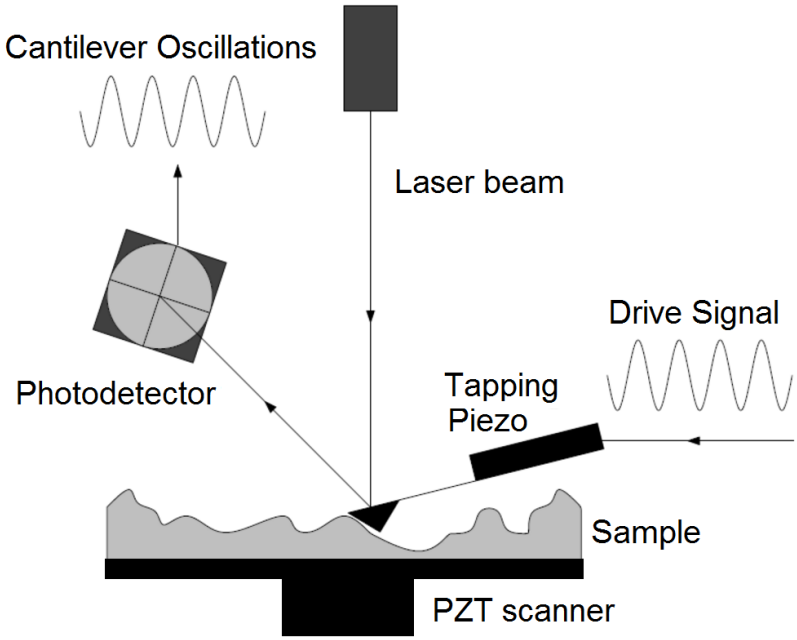

FIG. 3.12: Schematic of an Atomic Force Microscope working in tapping mode.

AFM measurements were performed using a Bruker Dimension ICON AFM system which can accommodate large wafer samples up to 8-inch diameter. AFM images were recorded in tapping mode using a silicon tip with resonance frequency between 204-497 kHz. Areas of 5x5 μm^2 were scanned with scan frequency of 0.992 Hz and 512 lines per sample. The technique was used in the present project to assess the films topography and to calculate the roughness of the films surface using NanoScope Analysis software. The roughness of the samples was assessed using the arithmetic average root mean square roughness (R_a), which is the arithmetic average of the absolute values of the height of the surface profile.

3.3.6. Transmission electron microscopy

High resolution transmission electron microscopy (TEM) and scanning transmission electron microscopy (STEM) experiments were performed to investigate the thickness and microstructure of selected ALD oxide films deposited on HEMT structures.

TEM is a microscopy technique in which an electron beam is transmitted through a very thin sample (< 100 nm), interacting with the sample and forming an image. TEM has a high resolution capability due to the small wavelength of the electron beam, which enables the observation of even a small column of atoms. The most common mode of operation for a TEM is the bright-field imaging in which the image contrast is formed by occlusion and absorption of electrons in the material. In this mode, regions of the sample with a higher atomic number will appear dark, whereas regions with no sample in the beam path will appear bright.

The capabilities of TEM can be extended into a STEM by adding a system that rasters the beam across the sample combined with detectors to form the image. Scanning coils are used to deflect the beam which is collected using a current detector that acts as an electron

counter. By correlating the electron count to the position of the scanning beam, the beam transmitted component can be measured and the non-transmitted components can be obtained by the use of annular dark field detectors. Annular dark field imaging has the ability to image atoms.[21]

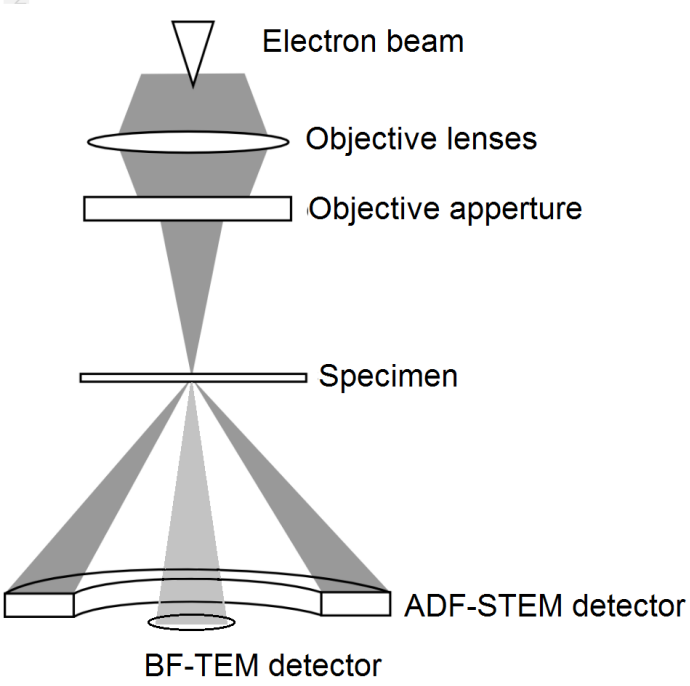

FIG. 3.13: Schematic diagram of annular dark field (ADF) and bright field (BF) spectrum modes in a STEM.

Cross-sectional TEM and STEM were conducted to characterise the thickness and the interfacial properties between the ALD films and the nitride top layers in the HEMT heterostructures. The TEM images were acquired by Dr. Hui Ru (IMRE, Singapore) using a FEI Titan 80-300 kV Scanning Transmission Electron Microscope operating at 200 kV in bright-field TEM (BFTEM) and high-angle annular dark field STEM (HAADF-STEM) modes (Fig. 3.13). This high-resolution STEM instrument is capable of atomic resolutions of ~ 0.12 nm for BFTEM and ~ 0.17 nm for STEM.

3.3.7. Electrical measurements

Capacitance-voltage (CV) and current-voltage (IV) measurements were used to investigate the ALD oxide films dielectric properties. The CV response of a MOS capacitor is a key technique for the characterisation of a MOS system. CV characteristics can be measured by superimposing a small AC signal of amplitude δV on the DC gate voltage. During CV measurements, the voltage bias applied to a MOS capacitor is swept from positive to negative voltages through zero bias so that the surface of the semiconductor changes from accumulation to depletion and then to inversion (or/and vice versa). Displacement current is measured as a function of time, which results in a measurement of the charge stored in the MOS capacitor. Stored charge equals to the product of capacitance and voltage (i.e. Q = CV) and thus, the capacitance as a function of voltage can be calculated. The typical characteristic for an ideal MOS capacitor with n-type substrate at high and low frequencies is shown in Figure 3.14. In the accumulation layer, the charge is modulated by the measuring signal. The charge is formed by majority carriers (in this case, electrons) beneath the oxide layer that react easily to the signal. Therefore, the measured capacitance in the accumulation region of the CV plot is the capacitance of the oxide layer. The depletion region forms when gate voltage becomes smaller than the flatband voltage and the majority carriers are forced away from the surface of the semiconductor. The majority carriers are present underneath the depletion region and there is no layer of mobile carriers under the oxide. The modulated charge is at the edge of the depletion region and the majority carriers are pushed and pulled backwards and forwards by the AC field. Therefore, the measured capacitance in depletion consists of the series combination of the oxide capacitance and the capacitance of the depletion layer. Thus, during depletion the capacitance decreases to the minimum capacitance. Inversion occurs when the threshold voltage is reached and the semiconductor surface starts to fill up with minority carriers (in

this case, holes). At low frequency, the substrate carriers are at thermal equilibrium and minority carrier generation can follow the measuring signal and the DC voltage sweep, and the capacitance increases back to the maximum value. At high frequency, for an applied AC voltage the response of the inversion layer is too slow to follow the signal and the inversion layer appears fixed with respect to the AC component of the bias. The minority carrier generation process cannot follow the measuring signal but can follow the 'slow' DC sweep, and the capacitance reaches a minimum value.

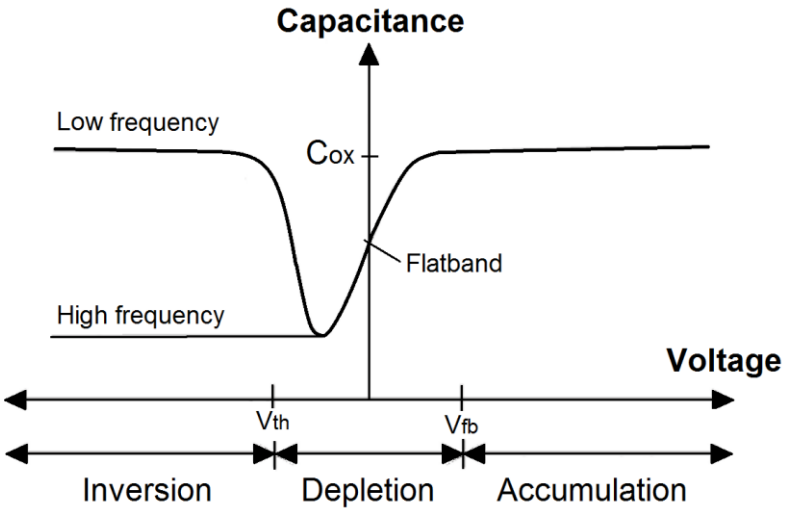

FIG. 3.14: Capacitance-voltage characteristics for an ideal MOS capacitor with n-type substrate.

In addition to the CV characteristics, the IV characteristics of a MOS capacitor can provide information about the quality of the gate oxide. IV measurements can be carried out using the same MOS capacitors as fabricated for CV measurements. IV measurements are performed by sweeping voltage bias slowly from zero towards either positive or negative values and measuring the resultant current. The typical IV response for an ideal gate oxide is shown in Figure 3.15. For relatively thick oxides, very little current flows at voltages below the breakdown voltage. Once the breakdown occurs, the current rises very rapidly. On a semilogarithmic plot as the one shown in Figure 3.15 (with current density plotted on a logarithmic scale versus voltage plotted on a linear scale) the IV response

appears as a flat or slowly rising curve until it reaches the breakdown voltage, at which point the plot becomes essentially vertical. The breakdown voltage must be directly dependent on the oxide film thickness. For thin oxides, the IV response is affected by the phenomenon of quantum mechanical tunnelling. Particles such as electrons cannot be completely confined by a finite potential barrier such as the one provided by the oxide layer and therefore some current can always be expected to leak through the gate oxide. This tunnelling current appears in the IV plot as a rising characteristic in the region just below breakdown. As particle confinement substantially depends on barrier thickness, tunnelling current is significant only for very thin oxide layers.

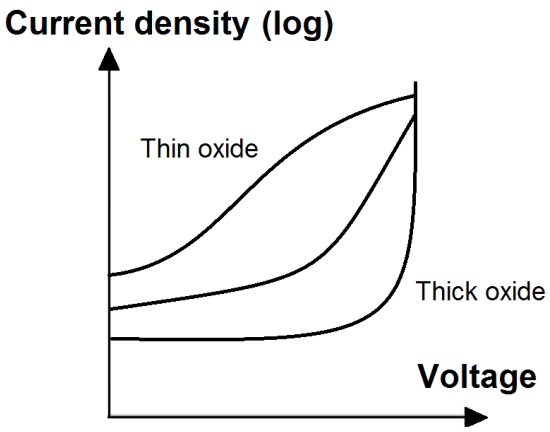

FIG. 3.15: Ideal current-voltage characteristics for thin and thick oxide films.

CV-IV measurements were performed on Au/oxide/Si(100) MOS capacitors fabricated at the University of Liverpool. The ALD oxide films were grown on n-type Si(100) substrates (supplied by PI-KEM, test grade). Gold top electrodes were then deposited by sputtering through two different shadow masks with holes of ~ 1 mm and ~ 300 µm diameter, respectively. The samples were annealed using the carbolite tube furnace at 600 ºC for 60 s in nitrogen (BOC Zero grade). The back metal contact was formed by evaporation of Al on the backside of the Si substrate using an Edwards E306A cating system. Finally, the capacitors received a forming gas (10 % hydrogen/nitrogen supplied

by BOC) anneal at 430 ºC for 30 min in the carbolite tube furnace to reduce the density of interface states (D_{it}).[22]

CV measurements were carried out in dark on the ~ 1 mm diameter MOS capacitors using an E4980A precision LCR meter (Fig. 3.16). The CV analyser applies a high frequency drive signal (which is superimposed on a relatively slow DC bias sweep) to the backside of the substrate via a probe chuck. The probe station used was a Karl Süss KSM SOM 4. The signal was measured at the gate via a probe needle. The CV measurements were carried out to calculate the dielectric constant of the ALD oxide films. The measurements were performed at different frequencies ranging from 1kHz to 500kHz, and for voltages between -3 V and positive voltages under the breakdown voltage (which depends on the oxide film), and steps of 0.1 V.

IV measurements were carried out using an Agilent B1500A semiconductor device analyser on the ~ 300 µm diameter MOS capacitors. MOS with smaller area were fabricated in this case to reduce the chance of including areal defects in the measurements, which can potentially affect the capacitors current leakage. The absolute value of the devices current was recorded for a voltage range from – 4 V to + 4 V and steps of 0.04 V. In contrast to CV measurements, the bias voltage in IV measurements is generally carried to values for which the oxide layer breaks down (i.e. fails as an insulator).

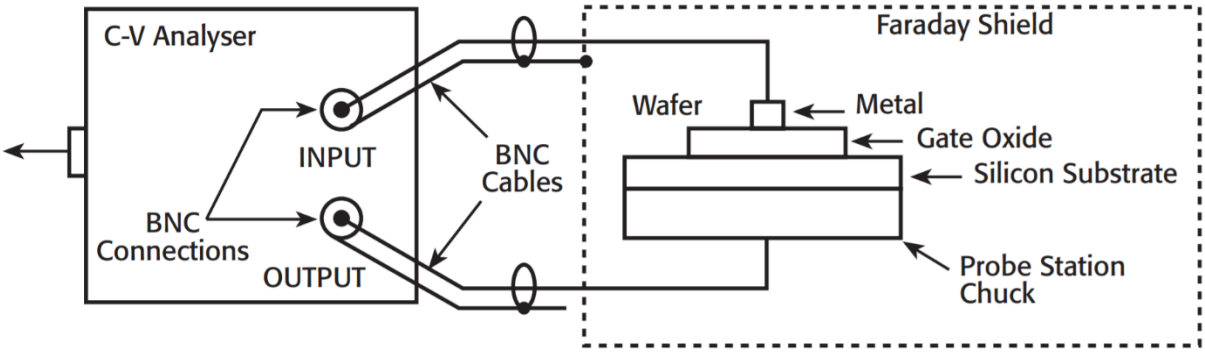

FIG. 3.16: Schematic of CV and IV characterisation using an analyser.

3.4. MOSHEMTs fabrication and characterisation

3.4.1. MOSHEMTs fabrication process

The fabrication and electrical measurements of the MOSHEMTs studied in this thesis were carried out at the University of Sheffield by Dr.Zaffar H.Zaidi. In a preparatory step, the wafers with the HEMT stack were cut manually into pieces of approximately 2 x 2 cm^2. After the cutting, a standard cleaning procedure was used. Each sample was placed sequentially in beakers containing acetone and isopropanol and sonicated in an ultrasonic water bath to remove any organic contaminants from the sample surface. The cleaning procedure was completed with a DI water rinse of the sample in an ultrasonic water bath. Finally, the sample was blown dry with an N_2 gun and subsequently baked on a hot plate to evaporate remaining solvents. This cleaning procedure was used several times during the fabrication of the devices.

Mesa etching

The first step in the MOSHEMTs processing was the mesa etching, which was performed to isolate regions of the sample where individual devices will be fabricated. To obtain a good electrical isolation, GaN-based HEMTs were etched down to the GaN buffer layer so the conducting 2DEG cannot form (Fig. 3.17). Due to the chemical stability of group III-nitride semiconductors, it is difficult to etch the materials using wet etch techniques and thus dry etching techniques such as reactive ion etch (RIE) and inductively coupled plasma (ICP) etching are normally used for the mesa structure process.[23] Compared to the RIE, ICP etching offers low damage etch, high etching rates and anisotropic profiles.[24, 25] Consequently, mesa etching of the HEMT structures analysed in this thesis was carried out using ICP etching with a Cl_2-based plasma.

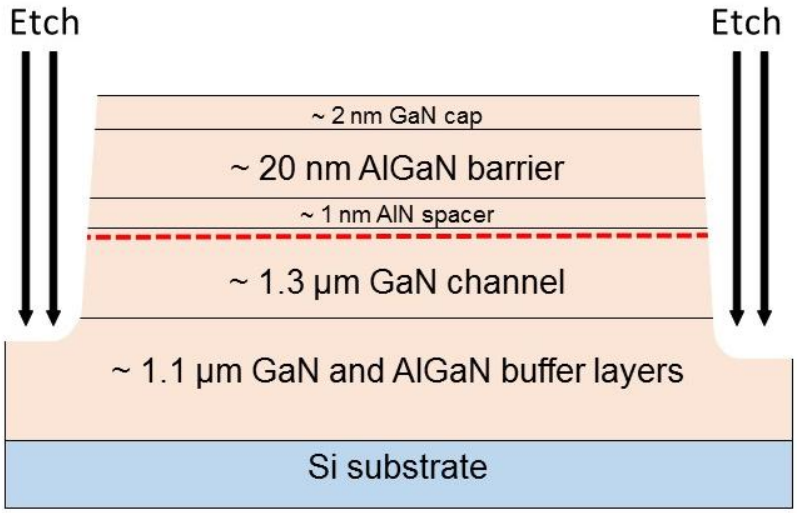

FIG.3.17: Schematic cross section of an AlGaN/GaN HEMT after mesa etching.

Prior to mesa etching a standard lithography process was carried out. Lithography is the process of creating patterns on samples using a photosensitive material (or photoresist) and an UV light exposure system to transfer the patterns on a mask to the sample surface. Depending on how the photoresists respond to the UV light/radiation, they can be classified as positive or negative.[26] For positive photoresists, the exposed regions become more soluble in developer solutions and thus more easily removed during the development process. As a result, the patterns formed in the positive resist are the same as those on the mask. For negative photoresists, the exposed regions become less soluble in developer solutions and thus more difficult to be removed during the development process. The patterns formed in the negative resist are the reverse of the mask patterns.

Mesa fabrication in this project started with the sample standard cleaning procedure prior to lithography processing. After cleaning, positive photoresist was spun on the sample surface to ensure a uniform coating (Fig. 3.18a). Following the spinning step the sample was baked on a hotplate to remove the solvent from the resist film and to increase resist adhesion to the wafer. The sample was then aligned and brought into contact with the mesa

pattern on the mask and the photoresist was exposed to the UV light (Fig. 3.18b). The exposed resist was dissolved in a developer solution and the sample was then rinsed with DI water and dried with N_2 gun. After the lithography process the mesa patterns were defined on the samples surface and the areas of the samples in which the photoresist had been cleared were etched around 350 nm (Fig. 3.18c). After etching the photoresist was removed with acetone (Fig. 3.18d). Finally, the sample was cleaned using the standard cleaning procedure.

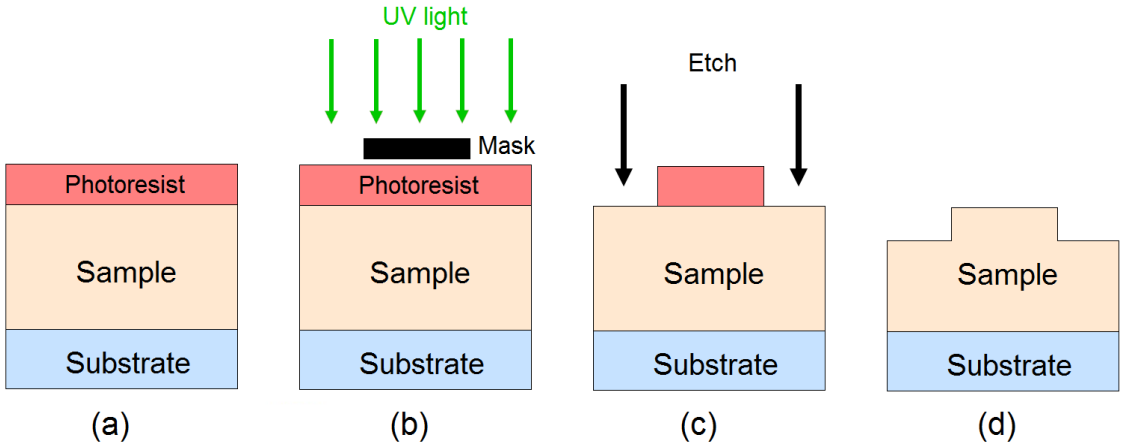

FIG.3.18: Schematic of the fundamental mesa processing steps: (a) photoresist coating, (b) selective photoresist exposure to UV light using a mask, (c) mesa etching and (d) photoresist removal.

Ohmic contacts fabrication

The second step in the MOSHEMTs fabrication process was the source and drain ohmic contacts fabrication. Optimal performance of GaN-based HEMT devices requires the use of ohmic contacts with low resistance and smooth surface morphology in order to reduce the ON-resistance, minimise the power dissipation in the ohmic contacts and to maximise RF power output and power-added efficiency of the devices.[27]

To fabricate ohmic contacts, the standard lithography process used for mesa fabrication was performed utilising a mask with the source and drain patterns negative (Fig. 3.19b). After the ohmic contacts lithography process the negative of the source and drain patterns

was defined on the samples surface (Fig. 3.19c). The metal stack was then blanket-deposited all over the sample surface substrate covering both the photoresist and the areas where the photoresist had been cleared. After metal deposition a liftoff process was utilised for patterning the deposited metals. During liftoff the photoresist under the metal was removed with acetone, taking the metal with it and leaving only the metal that was deposited directly on the sample surface (Fig. 3.19d). After liftoff the sample was rinsed with DI water and dried with N_2 gun. In this work, a Ti/Al//Ni/Au (20/120/20/45 nm) metal stack was deposited by thermal evaporation. After the metal liftoff the samples were annealed in a CTB at 830 °C under N_2 ambient to form the source and drain ohmic contacts.

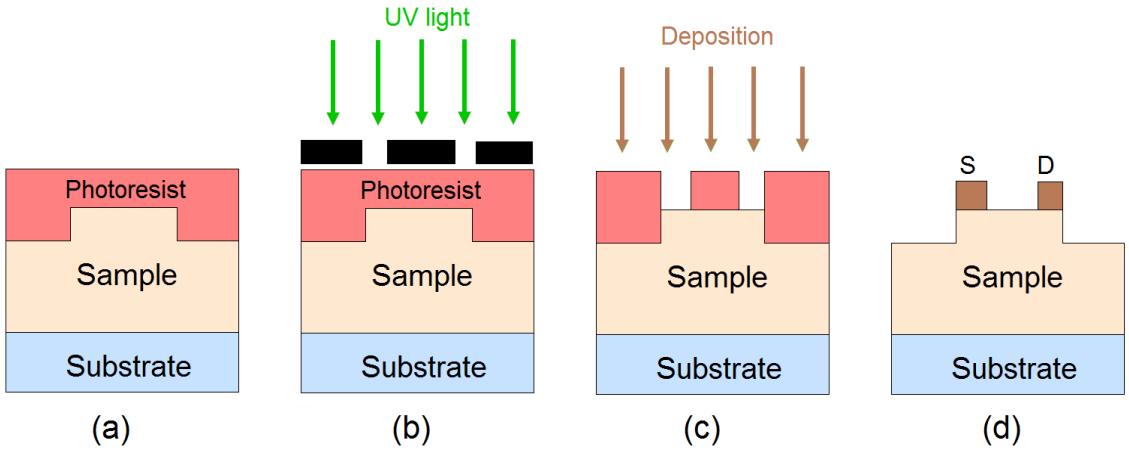

FIG.3.19: Schematic of the fundamental source and drain ohmic contacts processing steps: (a) photoresist coating, (b) selective photoresist exposure to UV light using a mask, (c) metal deposition and (d) photoresist removal.

Gate fabrication

After the ohmic contacts processing the whole sample surface was passivated to minimise the carrier trap concentration at the interface with the semiconductor.[28] A ~ 80 nm thick SiN_x passivation layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) (Fig. 3.20a). A 1.5 µm gate window was then etched through the SiN_x layer using ICP (Fig. 3.20b). Prior to gate window etching the standard lithography process was carried

out using a mask with the negative of the gate window pattern. After gate etching a ~10 nm thick gate dielectric layer was deposited by ALD (Fig. 3.20c). The samples were then annealed at 600 ºC for 60 s under nitrogen ambient to improve the interface between the gate dielectric and the semiconductor surface.[29] The same lithography process used for ohmic contacts processing was carried out to etch an additional window through the insulating layers in order to access the source and drain contacts (Fig. 3.20d). RIE was used to etch both the gate dielectric and the passivation layers.

Prior to the deposition of the gate metal the standard lithography process was carried out utilising a mask with the gate pattern negative. A T-shape Ni/Au (20/180 nm) gate metal with 100 µm gate width and 1.5 µm gate length was deposited by thermal metal evaporation. T-shaped gates are used to improve the device characteristics by minimising the effective gate length and by reducing the gate resistance.[30] A liftoff process followed by the sample standard cleaning procedure completed the MOSHEMTs processing (Fig. 3.20e).

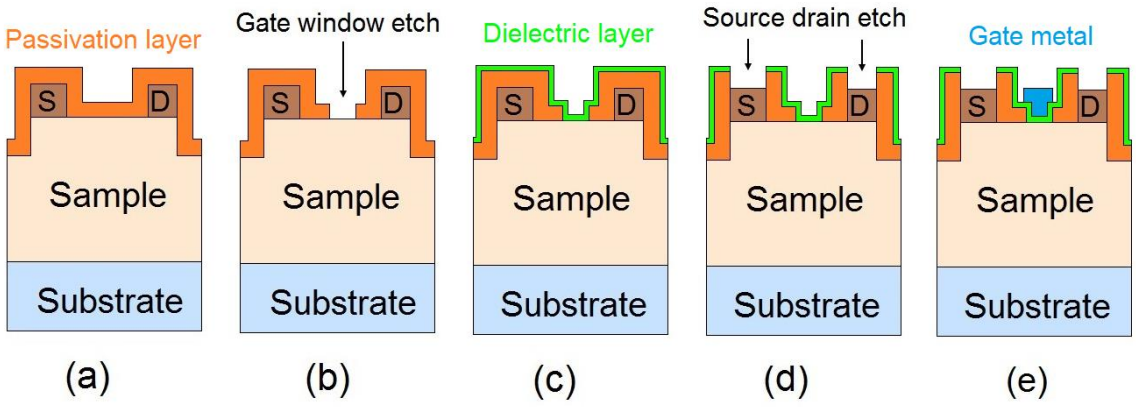

FIG.3.19: Schematic of the gate processing steps: (a) surface passivation layer deposition, (b) gate window etching, (c) gate dielectric deposition, (d) source and drain etching and (e) gate metal deposition.

3.4.2. MOSHEMTs characterisation methods

To determine the output DC characteristics of the transistors, the gate source and drain source electrodes were biased with gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}), respectively (Fig. 3.20). The ON-state transistor characteristics can be defined as the drain current (I_D) as a function of the V_{DS} and V_{GS}. Before I_D was monitored, the transistor working point was determined by sweeping V_{GS} from some volts beyond 0 V down to a level slightly underneath the threshold voltage whereas V_{DS} was swept from 0 V up to several tens of volts below the breakdown voltage. During measurements, the working point for a given V_{GS} or V_{DS} value was swept through and I_D was monitored.

The device's OFF-state characteristic is given by the OFF-state leakage currents as a function of the V_{DS}. To measure the OFF-state characteristics, V_{GS} was set under the threshold voltage in order to put the device in the OFF-state. The V_{DS} was then swept from 0V to 300 V. To avoid the permanent damage of the samples, the maximum I_D was set to a value of 1 µA/mm so that the voltage sweep would stop in case this value was reached. The voltage at which I_D reached 1 µA/mm was taken as the breakdown voltage. This is a standard value for the OFF-state leakage current in MOSHEMT devices.[31]

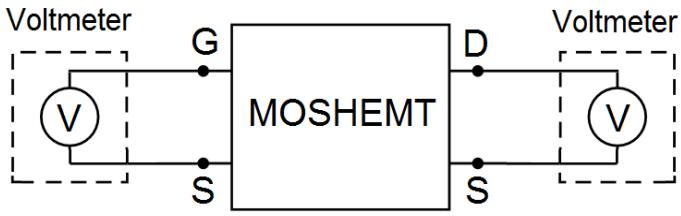

FIG.3.20: Setup used to characterise the output of the fabricated MOSHEMTs.

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4. Growth and characterisation of ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ thin films

4.1. Introduction

This chapter describes a method to grow $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ thin films as potential gate dielectrics for next-generation GaN-based power transistors. The microstructure, optical properties and composition of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films grown by thermal ALD at 250 °C have been studied as a function of the Ta precursor ALD cycle fraction, together with the impact of post-deposition annealing on these properties. This deposition temperature has been selected based on preliminary growth studies where the growth rates of Al_2O_3 and Ta_2O_5 have been analysed as a function of the deposition temperature using ellipsometry. XRD analysis shows that the crystallisation temperature of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers decreases with the introduction of Ta. The oxide films optical properties obtained from spectroscopic ellipsometry change significantly with the Ta content: the thickness decreases, while the refractive index increases. After annealing, a slight decrease in thickness together with an increase in the refractive index is observed. This is attributed to a densification of the oxide films, which can be beneficial for their dielectric properties. XPS measurements show that the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers composition has very good stoichiometry and varies linearly with the Ta precursor ALD cycle fraction. The effect of post-deposition annealing in N_2 at 600 ºC on the composition of the oxide films has also been investigated. These conditions are analogous to the conditions used for source/drain contact formation in gate-first GaN-based HEMT technology.[1] The oxide films microstructure and composition are not affected by this post-deposition annealing process, which is promising for their use as gate dielectrics. The results demonstrate that ALD with modulation doping can be used to control the composition of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers for gate dielectric applications.

4.2. Growth rate of ALD Al_2O_3 and Ta_2O_5 layers as a function of the deposition temperature

In order to investigate the self-saturation growth characteristics for the Al_2O_3 and Ta_2O_5 ALD processes, the growth rate of Al_2O_3 and Ta_2O_5 films was analysed as a function of the deposition temperature. Al_2O_3 and Ta_2O_5 layers were deposited on Si(100) substrates at different temperatures ranging from 100 ºC to 375 ºC and using a constant number of ALD cycles (n = 300). The ALD growth parameters used to deposit the Al_2O_3 and Ta_2O_5 layers are specified in section 3.1. The oxide film thickness and refractive index were determined by spectroscopic ellipsometry (SE). The measurements were performed at an angle of incidence of ~ 70 º using a spectral range of 430–850 nm. The accumulated spectra were characterised using a model comprising the Si(100) substrate, a ~ 15 Å SiO_2 native layer on top of the substrate and the deposited ALD Al_2O_3 or Ta_2O_5 film. The thickness of the SiO_2 interlayer was determined from SE measurements performed on the Si(100) substrates prior to the deposition of the ALD oxides. These experimental measurements were utilised to define the Si(100) substrate and the SiO_2 interfacial layer in the ellipsometry model, whereas the Al_2O_3 and Ta_2O_5 films were defined using the New Amorphous theoretical model described in section 3.3.1. The oxide film thickness, angle of incidence, refractive index and extinction coefficient were set as parameters to be fit. The growth rates for the Al_2O_3 and Ta_2O_5 films were calculated by dividing the film thickness by the total number of ALD cycles. The refractive index values were obtained at 632.8 nm wavelength.

4.2.1. Spectroscopic ellipsometry of ALD Al_2O_3 on Si(100)

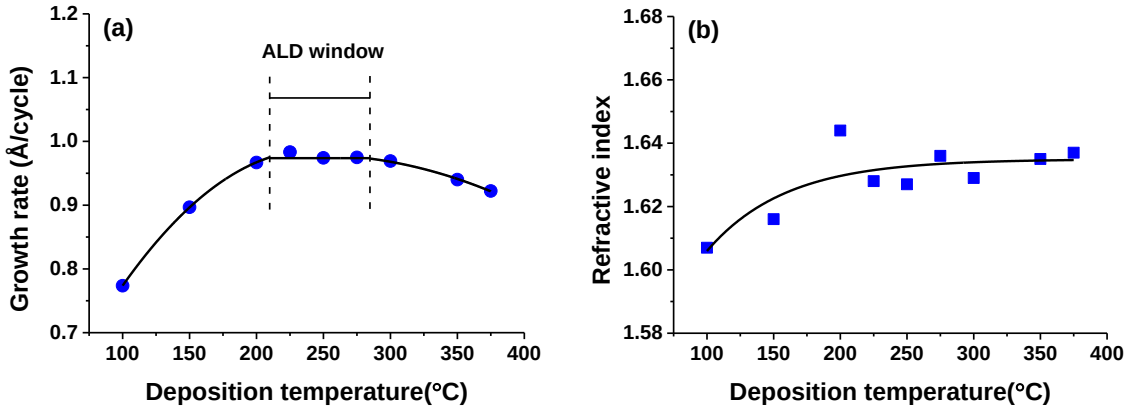

FIG. 4.1: Temperature dependence of the (a) growth rate and (b) refractive index at 632.8 nm wavelength of thermal ALD Al_2O_3 films deposited on Si(100) using n=300 ALD cycles.

Figures 4.1a and 4.1b show the growth rate and refractive index of Al_2O_3 as a function of the deposition temperature. The results show three distinct growth regions in the Al_2O_3 ALD process (Fig. 4.1a). The middle one is where the growth per cycle appears to be independent of substrate temperature, which indicates the existence of an ALD process window where the growth of the oxide layers occurs in a self-limiting manner. The ALD window for Al_2O_3 is found to be between approximately 210 ºC and 285 ºC. The experimental self-limiting growth rate calculated for this temperature range is 0.97 Å/cycle, which is in good agreement with typical values of 1.0-1.1 Å/cycle reported in literature for Al_2O_3 grown by ALD using TMA and H_2O precursors.[2-4] Figure 4.1b shows that the refractive index of the Al_2O_3 films decreases slightly with decreasing growth temperatures. This trend has been previously reported and was attributed to decreased density and to increased impurity levels in films grown at lower temperatures.[5-7] The refractive index value decreases from about 1.63 for temperatures higher than 150 ºC to 1.61 when the substrate temperature is 100 ºC. The refractive index value of 1.63 obtained within the ALD window is very similar to the value of 1.64 reported for Al_2O_3 in other published work.[8, 9]

Outside the ALD window, the Al_2O_3 growth rate decreases for both, lower and higher temperatures. At temperatures below the ALD window, the growth rate is often found to decrease due to insufficient thermal energy to drive forward the surface reactions.[10] The refractive index also decreases with temperature below the ALD window. This trend of the refractive index has been reported for temperatures under 200 ºC.[8, 11, 12] The decrease of the refractive index is expected to be caused by a reduction of the Al_2O_3 films mass density.[7] This could be attributed to an increase of carbonate species (with lower atomic mass than Al)[13] incorporated by the precursor side groups due to incomplete metal precursor interaction with the substrate. However, further XPS experiments on the film composition would be required to analyse the C content in the oxide films and confirm this assumption. The decrease of the Al_2O_3 growth rate at temperatures above the ALD window has been reported in literature.[14, 15] This decrease can be caused by desorption of AlOH* and $AlCH_3$* surface species prior to their respective reaction with TMA and H_2O precursors. The decrease can also be attributed to a lower OH surface coverage at higher temperature due to thermally activated dehydroxylation reactions where two OH groups combine to form an oxygen bridge and release water.[16] The fact that the refractive index does not significantly change above the ALD window indicates that the oxide film density does not vary with the deposition temperature in this region. This agrees with the desorption mechanism accounting for the lower growth rate, but further studies such as XPS, secondary ion mass spectrometry (SIMS) or low-energy ion scattering spectroscopy (LEIS) would be required to support this hypothesis.

4.2.2. Spectroscopic ellipsometry of ALD Ta_2O_5 on Si(100)

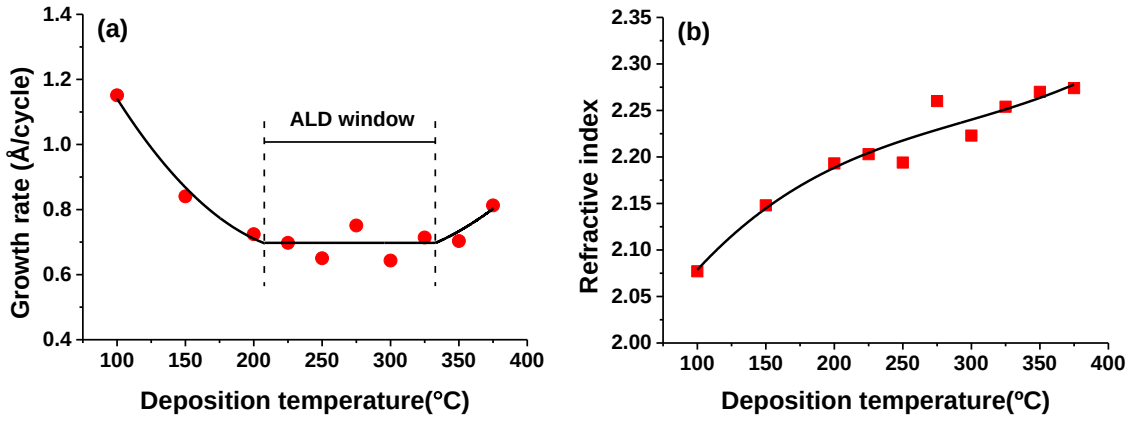

FIG. 4.2: Temperature dependence of the (a) growth rate and (b) refractive index at 632.8 nm wavelength of thermal ALD Ta_2O_5 films deposited on Si(100) using n=300 ALD cycles.

The growth rate and refractive index of Ta_2O_5 as a function of the deposition temperature are shown in Figures 4.2a and 4.2b. As occurred with Al_2O_3 in the previous section, the results show three distinct growth regions in the Ta_2O_5 ALD process (Fig. 4.2a). The ALD window for Ta_2O_5 is found to be between around 210 ºC and 330 ºC. The self-limiting growth rate of Ta_2O_5 in this temperature range is 0.70 Å/cycle, which is within the range of values reported in other published work for Ta_2O_5 deposited by ALD using PDMAT and H_2O (~ 0.6 - 0.85 Å/cycle).[17-19] The value of the refractive index increases with temperature from 2.1 to 2.3 (Fig. 4.2b). This indicates that there is a positive correlation between the growth temperature and the Ta_2O_5 films density, which agrees with published work.[20] The refractive index within the ALD window slightly varies from 2.2 to 2.3, which is in agreement with experimental values of about 2.2 reported in literature for Ta_2O_5.[21, 22]

The growth rate of Ta_2O_5 increases outside the ALD window. This behaviour has previously been reported for Ta_2O_5 grown by ALD on Si substrates.[19] At lower temperatures, the increase of the growth rate can result from precursor condensation.[20] This

would explain the decrease of the refractive index at low temperatures due to the incorporation of lower density species from the metal precursor. At temperatures above the ALD window, the growth rate of Ta_2O_5 increases due to thermal decomposition of the metal precursor which leads to a 'CVD-like' growth contribution to the overall growth rate.[23] Thermal decomposition of PDMAT has been reported to produce Ta_2O_5 with large C contamination during CVD Ta_2O_5 of at 400 ºC.[24] Again, further XPS experiments on the films composition would be required to confirm these assumptions.

Therefore, the temperature regions where the Al_2O_3 and Ta_2O_5 ALD processes occur in a self-limiting manner overlap between approximately 210 °C and 285 ºC. This range defines the ALD temperature window for the deposition of the Ta-doped Al_2O_3 layers, which is the region in which the growth of the films is saturated. Based on the results, the deposition temperature selected for the growth of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films during the present project was 250 ºC.

4.2.3. Cross section of Al_2O_3 and Ta_2O_5 on a GaN/AlGaN/GaN HEMT structure

High-resolution scanning transmission electron microscopy was used to confirm the self-limiting growth rates of ~ 10 nm thick Al_2O_3 and Ta_2O_5 films deposited on an GaN-capped AlGaN/GaN HEMT structure at 250 ºC and using n = 120 ALD cycles. Figure 4.3 shows the cross-sectional HAADF-STEM images of the as-deposited Al_2O_3 and Ta_2O_5 layers. Prior to ALD of the oxide films, the thickness of the HEMT nitride epilayers was investigated by high resolution XRD (HRXRD). From HRXRD, the HEMT structure consists of a thin AlN spacer of about ~ 1-2 nm, an AlGaN barrier layer of ~ 21-22 nm and a top undoped GaN cap layer of ~ 4-5 nm. These measurements are in agreement with the thicknesses observed by STEM. As the HEMT structure is grown on a 200 mm diameter Si(111) substrate, a small variation in the AlGaN barrier and GaN cap thicknesses is

expected across the wafer. HAADF-STEM imaging shows that the Al_2O_3 and Ta_2O_5 film thicknesses are uniform for both samples, with a continuous and sharp interface between the ALD oxide films and the GaN cap layer.

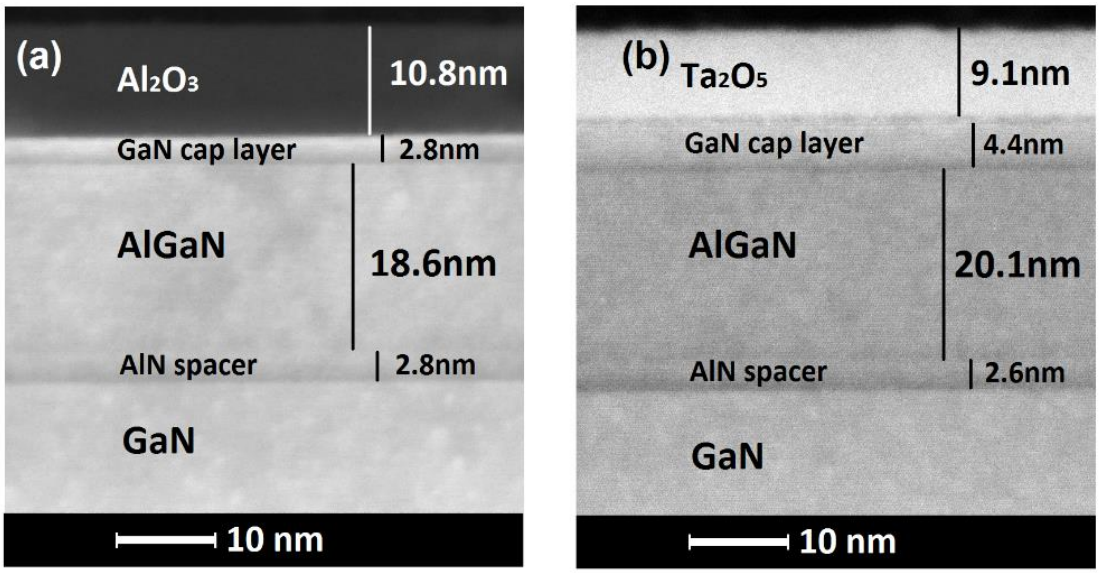

FIG. 4.3. Cross-sectional HAADF-STEM of (a) Al_2O_3 and (b) Ta_2O_5 layers grown on an AlGaN/GaN HEMT structure highlighting the top ALD oxide, GaN cap, AlGaN barrier, and AlN spacer on GaN buffer layers.

The deposition rates calculated for the Al_2O_3 and Ta_2O_5 layers are 0.90 Å/cycle and 0.76 Å/cycle, respectively. The values slightly differ from the growth rates of 0.97 Å/cycle and 0.70 Å/cycle obtained using ellipsometry. This difference is expected because in ellipsometry the thickness of the films is not measured directly. The ellipsometry method uses a model that evaluates the optical properties of the material by adjusting specific fit parameters and therefore the reliability of the extracted film parameters such as thickness depends on the model. As ellipsometry models calculate the thickness assuming that the film is homogeneous and the refractive index is constant within the film, ellipsometry measurements can be affected by surface roughness, film defects and/or bonding state changes at the oxide/substrate interface (i.e. deviation from homogeneity). Furthermore, ellipsometry calculates the film thickness using predetermined values for the refractive

index. The refractive index values used in the models are obtained from literature or from measuring bulk and high-purity samples, which may cause inaccuracy in the calculated thickness and therefore the ellipsometry results need to be independently validated.

Since the film thickness from TEM is measured directly and calculated as a function of the electron microscope magnification, the value of the thickness obtained using TEM is more reliable and can be used to assess the validity of the ellipsometry model. The results show that the growth rates obtained using ellipsometry differ less than 10 % from the TEM values. This indicates that the thicknesses calculated using ellipsometry can be used to calculate the ALD growth rates of Al_2O_3 and Ta_2O_5 to within 10 % of their true values.

4.3. Crystallisation temperature and optical properties of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ $(0 \leq x \leq 1)$ films

The microstructure, thickness and refractive index of ~ 30 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples with different compositions $(0 \leq x \leq 1)$ were analysed as a function of the Ta precursor ALD cycle fraction in order to study the effects of the introduction of Ta on the crystallisation temperature and optical properties of the oxide films. The films were deposited at 250 ºC on Si(100) substrates using a total of 360 ALD cycles (n = 360). After deposition, the samples were annealed in N_2 ambient for 30 min at temperatures ranging from 600 ºC to 1000 ºC. The oxide films microstructure as well as the thickness and the refractive index were analysed using XRD and SE.

4.3.1. Al_2O_3

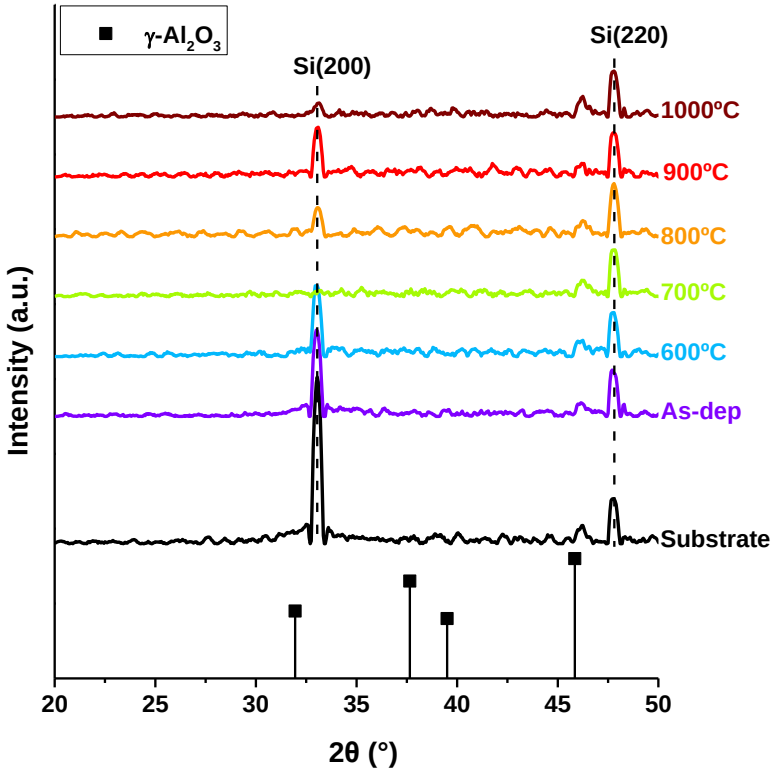

FIG. 4.4: XRD patterns of ~ 30 nm ALD Al_2O_3 samples grown on Si(100) as-deposited and annealed for 30 min in N_2 at temperatures ranging from 600°C to 1000°C.

Figure 4.4 shows the XRD patterns measured for the as-deposited and annealed Al_2O_3 samples. The XRD spectra of the coated samples were compared with the spectrum obtained for the uncoated Si(100) substrate and with the standard diffraction lines of the γ-Al_2O_3 phase from the Joint Committee on Powder Diffraction Standard-International Center for Diffraction Data (JCPDS-ICDD).[25] The peaks observed at 2θ ~ 33º and 2θ ~ 47º correspond to the (200) and (220) planes of the Si(100) substrate, respectively.[26] It can be observed that the Si(200) peak does not appear in all the scans and its intensity differs significantly from measurement to measurement. This is due to the fact that the Si(200) reflection is known as a basis-forbidden reflection and it is only visible when multiple diffraction occurs, which depends on the in-plane orientation of the sample.[27] Thus, the experimental diffraction patterns obtained indicate that the Al_2O_3 films are amorphous

before and after annealing at all temperatures analysed. A small peak at $2\theta \sim 46^{o}$ is also observed for all samples and the uncoated substrate, which could be assigned to the (201) plane of α-SiO_2 from a thin layer of native oxide.[28] Since this peak is not affected by the deposition of the oxide films or by the annealing treatments, it is not relevant in the following discussion. The absence of diffraction peaks, except for those from the substrate, indicate that no crystalline phases of Al_2O_3 are detected for any of the samples. This means that annealing in N_2 for 30 min at temperatures up to 1000 ºC causes no changes in the Al_2O_3 films crystal structure. These results differ from published work which has reported the crystallisation of Al_2O_3 in γ-phase between 700 ºC and 850 ºC.[29, 30] However, in other work Al_2O_3 films grown on Si remained amorphous after annealing at 900 °C.[31] It has also been reported that the transition from amorphous to crystalline α-Al_2O_3 phase occurs after annealing at temperatures ranging from 1050 ºC to 1150 ºC,[32] which is in agreement with the results obtained in this study.

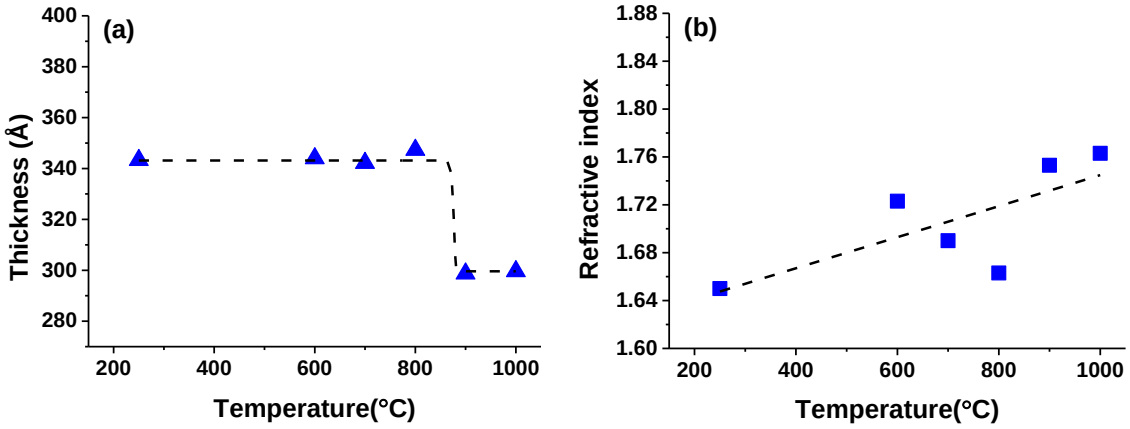

FIG. 4.5: (a) Thickness and (b) refractive index of ALD Al_2O_3 films grown on Si(100) using n=360 ALD cycles as-deposited and annealed for 30 min in N_2 at temperatures ranging from 600°C to 1000°C.

The Al_2O_3 samples were analysed by SE to determine the thickness and refractive index of the films before and after annealing (Figs. 4.5a and 4.5b). It is observed that annealing at temperatures above 800 ºC leads to a significant decrease in thickness. The thickness of

the as-deposited Al_2O_3 sample is calculated to be approximately 34 nm. No significant changes in thickness are observed after annealing at temperatures between 600 ºC and 800 ºC. However, after annealing at 900 ºC and 1000 ºC the thickness of the oxide films decreases to ~ 30 nm. This can be attributed to a densification of the Al_2O_3 films as suggested by the increase of the refractive index from ~ 1.64 to ~ 1.74 after annealing at temperatures up to 1000 ºC (Fig. 4.5b).[33] It has been shown that densification after annealing at temperatures up to crystallisation can improve the electric properties of Al_2O_3 films, increasing their dielectric constant.[34]

4.3.2. Ta_2O_5

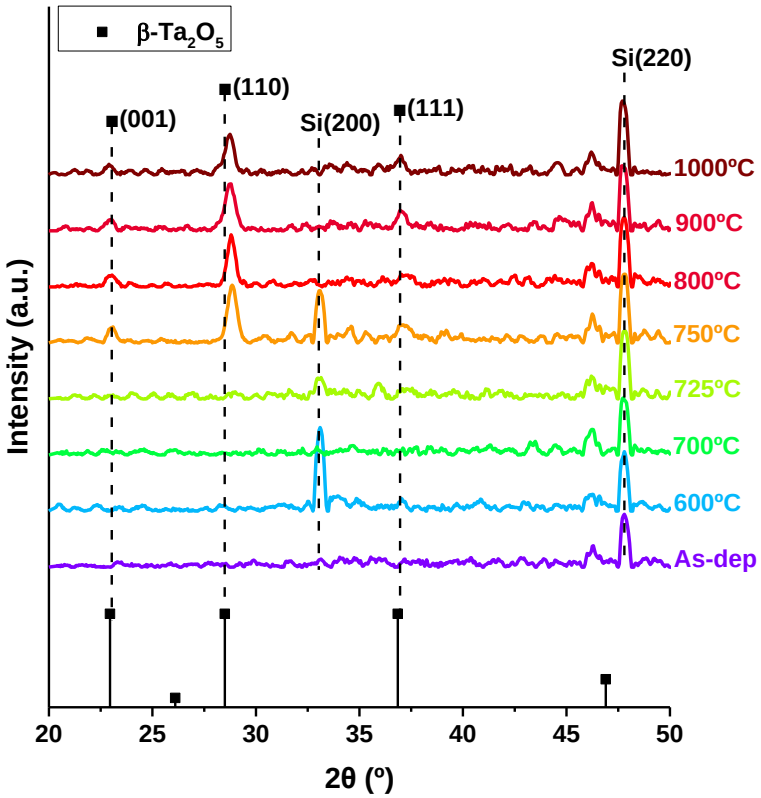

FIG. 4.6: XRD patterns of ~ 30 nm ALD Ta_2O_5 samples grown on Si(100) as-deposited and annealed for 30 min in N_2 at temperatures ranging from 600°C to 1000°C.

Figure 4.6 shows the XRD patterns obtained for the Ta_2O_5 samples as-deposited and after annealing. The standard diffraction lines of β-Ta_2O_5 (JCPDS-ICDD) are given at the

bottom.[35] XRD analysis shows that, according to the derived powder diffraction file, the Ta_2O_5 films develop a highly (110) oriented orthorhombic Ta_2O_5 structure after annealing at temperatures above 725 ºC. Three peaks which correspond to crystalline orthorhombic β-Ta_2O_5 can be observed for the samples annealed between 750 ºC and 1000 ºC.[36] The (110) peak with the highest intensity is detected at 2θ ~ 29º, and the (001) and (111) peaks with lower intensities are observed at 2θ ~ 23º and 2θ ~ 37º, respectively. The offset of the XRD peak positions with respect that of the powder diffraction file suggests a highly strained lattice in the *a* and *b* directions parallel to the substrate. According to Bragg's law, the shift of all peaks to higher 2θ values reflects the lattice parameter compression (Eq. 3.9). In literature, lower crystallisation temperatures of 600 ºC and 700 ºC have been reported for Ta_2O_5 films.[37, 38] However, Ta_2O_5 films which only showed polycrystalline peaks after annealing at 750–850 ºC have also been reported.[39] This is in agreement with the results obtained in this study. The re-crystallisation of the gate oxide during annealing can affect their dielectric properties inducing high leakage currents due to grain boundary conduction.[40, 41] Therefore, the results give an upper limit on the thermal budget for device processing when using Ta_2O_5 as gate dielectric.

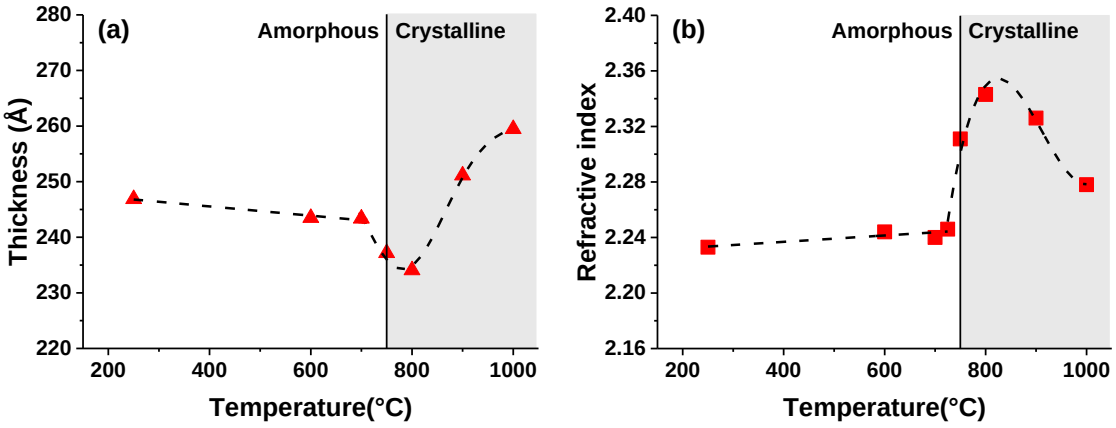

FIG. 4.7: (a) Thickness and (b) refractive index of ALD Ta_2O_5 films grown on Si(100) using n=360 ALD cycles as-deposited and annealed for 30 min in N_2 at temperatures ranging from 600°C to 1000°C.

Figures 4.7a and 4.7b show the thickness and refractive index calculated for the as-deposited and annealed Ta_2O_5 samples using SE. The results show a significant change in both thickness and refractive index after annealing at temperatures above the crystallisation temperature. The thickness and refractive index values obtained for the as-deposited Ta_2O_5 film are about 24.7 nm and 2.23, respectively. After annealing at temperatures up to 700 ºC, a slightly decrease in the thickness together with a small increase in the refractive index can be observed, which is associated with film densification.[33] The largest change is observed at the crystallisation temperature. After annealing at 750 ºC, the thickness decreases to ~ 23.7 nm and the refractive index increases to ~ 2.31, which indicates densification of the Ta_2O_5 film after crystallisation.[33] After annealing at 800 ºC, the thickness further decreases to ~ 23.4 nm and the refractive index increases to ~ 2.34. However, for higher annealing temperatures, the thickness increases up to ~ 25.9 nm after annealing at 1000 ºC and the refractive index decreases to ~ 2.28. One possible explanation for this is the formation of a thin $TaSiO_x$ interfacial layer as the annealing temperature increases over 800 °C, causing the increase of the total oxide thickness and the decrease of the refractive index.[42] However, this could not be confirmed by SE. A more accurate technique such as XPS depth profiling would be required to confirm this hypothesis.

4.3.3. $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 < x < 1$) films

$(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films with different compositions ($0 < x < 1$) were grown using Ta precursor ALD cycle fractions ($n_{PDMAT}/(n_{TMA}+n_{PDMAT})$) of approximately 1/10, 1/4, 1/2 , 3/4 and 9/10. The respective samples are denoted as 10%Ta-Al_2O_3, 25%Ta-Al_2O_3, 50%Ta-Al_2O_3, 75%Ta-Al_2O_3 and 90%Ta-Al_2O_3. For the 10%Ta-Al_2O_3 and 25%Ta-Al_2O_3 samples with the lowest Ta content, the PDMAT ALD cycle fractions are not exactly 1/10 and 1/4 because the ALD recipes where designed so that the initial set of cycles were

entirely TMA-based in order to have Al_2O_3 layers at the top and the bottom of the oxide film. As a consequence, the Ta precursor ALD fraction is slightly smaller than quoted. For the rest of the samples this was not possible due to their high Ta content. The sequence of ALD cycles used in the ALD recipes to grow the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples are summarised in Table 4.1:

TABLE 4.1. Sequence of Al precursor (TMA) and Ta precursor (PDMAT) ALD cycles used in the ALD recipes for the growth of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples.

Sample	Initial TMA cycles (n_{TMA})	Rest of cycles (n_{PDMAT}:n_{TMA})	Repeat (n_{PDMAT}:n_{TMA})	PDMAT cycles percentage
10%Ta-Al_2O_3	10	1:9	35	9.7 %
25%Ta-Al_2O_3	4	1:3	89	24.7 %
50%Ta-Al_2O_3	-	1:1	180	50 %
75%Ta-Al_2O_3	-	3:1	90	75 %
90%Ta-Al_2O_3	-	9:1	36	90 %

Figures 4.8a-e show the XRD patterns obtained for the Ta-Al_2O_3 samples before and after annealing between 600 °C and 1000 °C. The results show that the crystallisation temperature of the oxide films decreases with the PDMAT ALD cycle fraction. The films with lower Ta content (10%, 25% and 50%Ta-Al_2O_3) show no crystalline structure after annealing at temperatures up to 1000 °C (Figs. 4.8a-c), whereas the crystallisation of the 75%Ta-Al_2O_3 and 90%Ta-Al_2O_3 samples is observed after annealing at 875 °C and 850 °C, respectively (Figs. 4.8d and 4.8e).

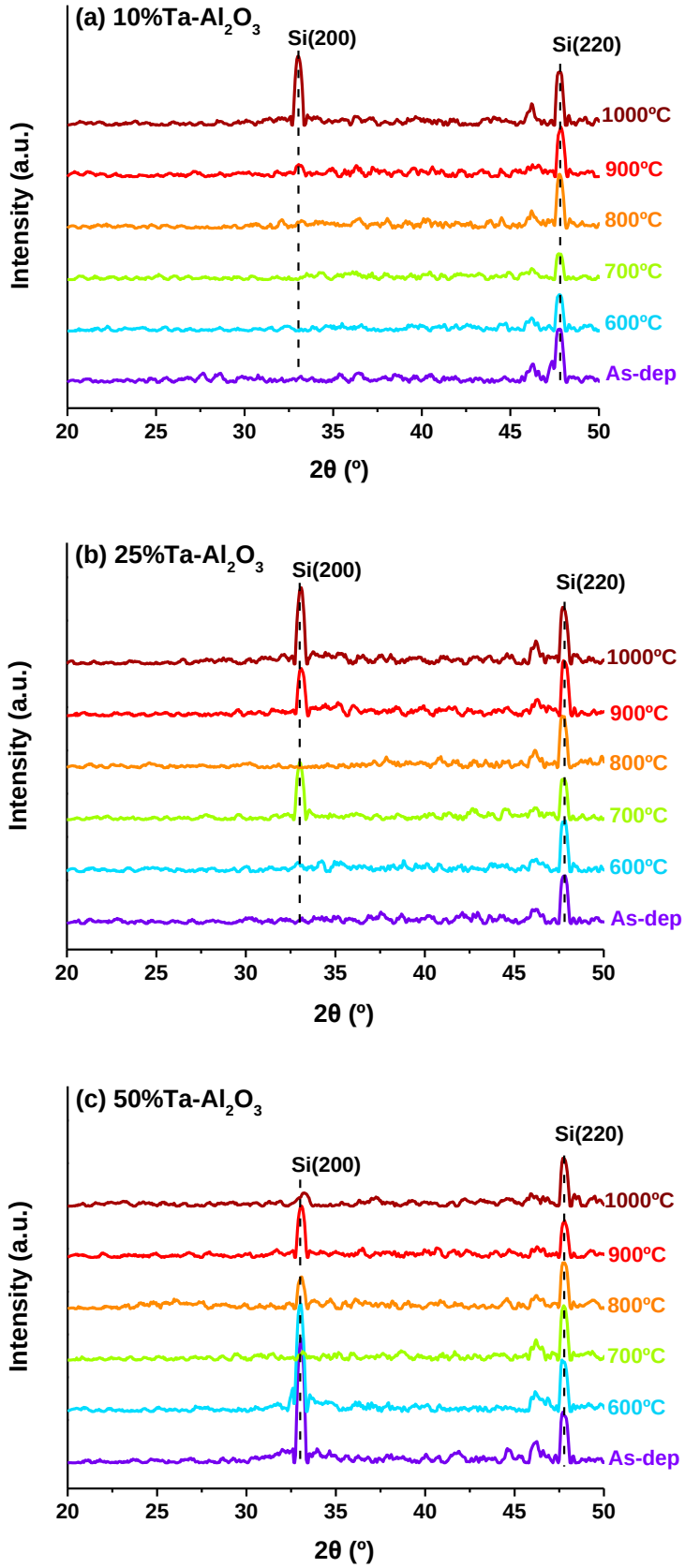

FIG. 4.8: XRD patterns of ~ 30 nm ALD (a) 10%Ta-Al_2O_3, (b) 25%Ta-Al_2O_3 and (c) 50%Ta-Al_2O_3 samples grown on Si(100) as-deposited and annealed at temperatures ranging from 600°C to 1000°C.

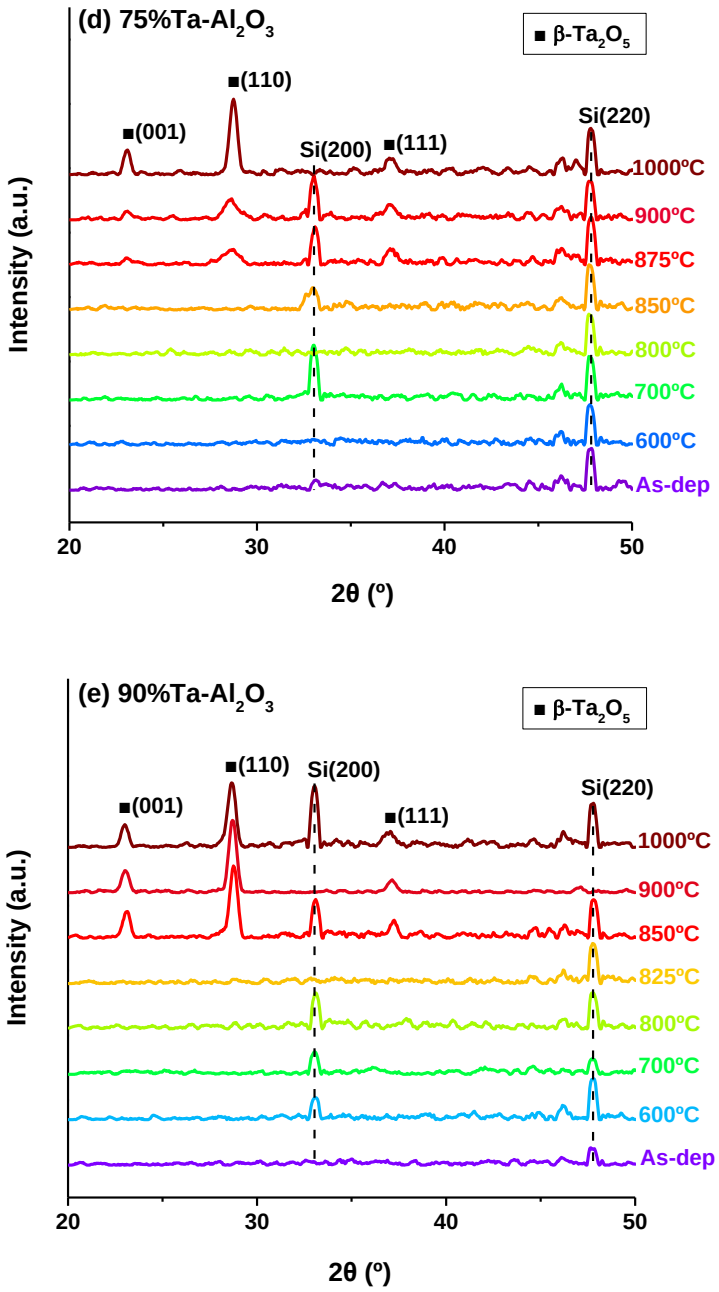

FIG. 4.8(cont.): XRD patterns of ~ 30 nm ALD (d) 75%Ta-Al_2O_3 and (e) 90%Ta-Al_2O_3 samples grown on Si(100) as-deposited and annealed at temperatures ranging from 600°C to 1000°C.

For the 75%Ta-Al_2O_3 sample, it can be observed that the β-Ta_2O_5 peak intensities after annealing at 875 °C and 900 °C are smaller compared to the maximum peak intensities obtained after annealing at 1000 °C (Fig. 4.8d). This increase in intensity with temperature can be attributed to an increase in the size of the crystallites, which is given by the Scherrer equation:[43]

$$D = \frac{K\lambda}{\beta \cos\theta} \tag{4.1}$$

where D is the grain size, K is the shape factor (typically 0.9), λ is the x-ray wavelength, β is the line broadening at FWHM after subtracting the instrumental broadening (in radians) and θ is the Bragg angle.

Table 4.2 below shows the FWHM calculated for the β-Ta_2O_5 (110) peak after applying a Gaussian curve fitting to the diffraction patterns obtained for the 75%Ta-Al_2O_3 sample. It can be observed that the FWHM values decrease with temperature, which according to Eq. 4.1 indicates that the Ta_2O_5 crystallite grain size in the oxide film increases significantly from 7.5 nm after annealing at 875 °C to 16.4 nm after annealing at 1000 °C.

TABLE 4.2. FWHM, 2θ and D values obtained for the crystalline β-Ta_2O_5 (110) peak of sample 75%Ta-Al_2O_3 annealed at different temperatures.

Annealing temperature	FWHM (°)	2θ	D (nm)
875 °C	1.1	28.6 °	7.5
900 °C	1.0	28.6 °	8.2
1000 °C	0.5	28.7 °	16.4

On the other hand, the β-Ta_2O_5 peak intensities for the 90%Ta-Al_2O_3 sample appear to reach the maximum intensity after annealing at 850 °C, which means that the size of the crystallites does not vary significantly after annealing at temperatures between 850 °C and 1000 °C. This behaviour is similar to the one observed for the Ta_2O_5 sample in section 4.3.2, where the β-Ta_2O_5 peak intensities reached the maximum intensity values after annealing at 725 ºC.

In summary, the XRD results suggest that the introduction of Ta is correlated with the decrease of the crystallisation temperature of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers, which can adversely affect device performance if the gate oxide crystallises during post-deposition annealing processing by inducing grain-boundary leakage current.

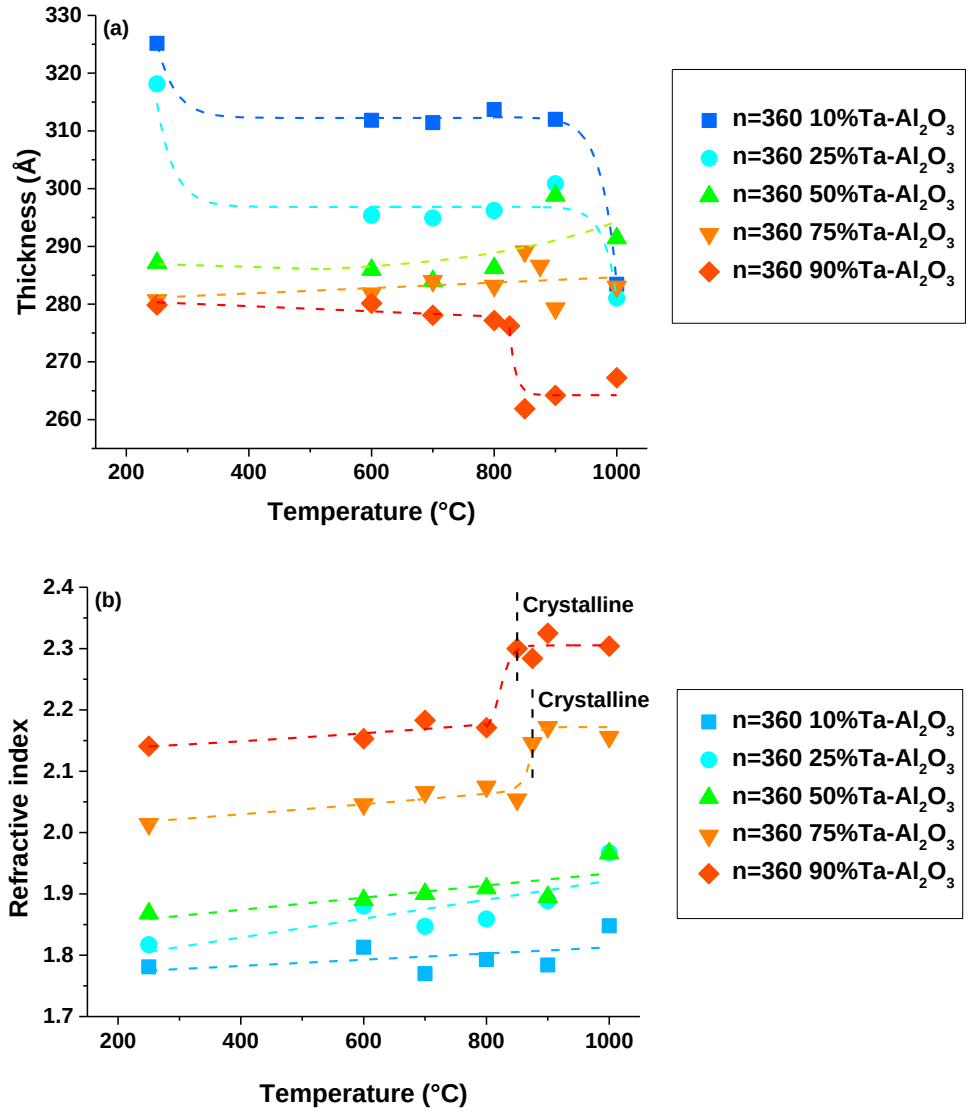

FIG. 4.10: (a) Thickness and (b) refractive index of ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films grown on Si(100) at 250 ºC using n=360 ALD cycles as a function of the annealing temperature.

The $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples were analysed using SE to examine the thickness and refractive index of the oxide films before and after annealing at different temperatures (Figs. 4.10a and 4.10b). In general, it can be observed that the increase of the PDMAT cycle fraction results in the reduction of the oxide films thickness and the increase of the refractive index. After annealing, a decrease in thickness together with an increase in the refractive index can be observed for the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples. This is in agreement with the results obtained for the Al_2O_3 and Ta_2O_5 samples in the previous sections, which

is attributed to a densification of the oxide films.[33] Additionally, as previously observed for the Ta_2O_5 sample in the previous section, the most significant refractive index change is observed for the 75%Ta-Al_2O_3 and 90%Ta-Al_2O_3 samples after crystallisation (Fig. 4.10b). No further changes are observed with temperatures above the crystallisation point, which suggests that the densification process saturates above the crystallisation temperature.[33] As previously mentioned, densification after annealing at temperatures up to crystallisation can increase the oxide films dielectric constant,[34] which could be advantageous for their use as gate dielectrics.

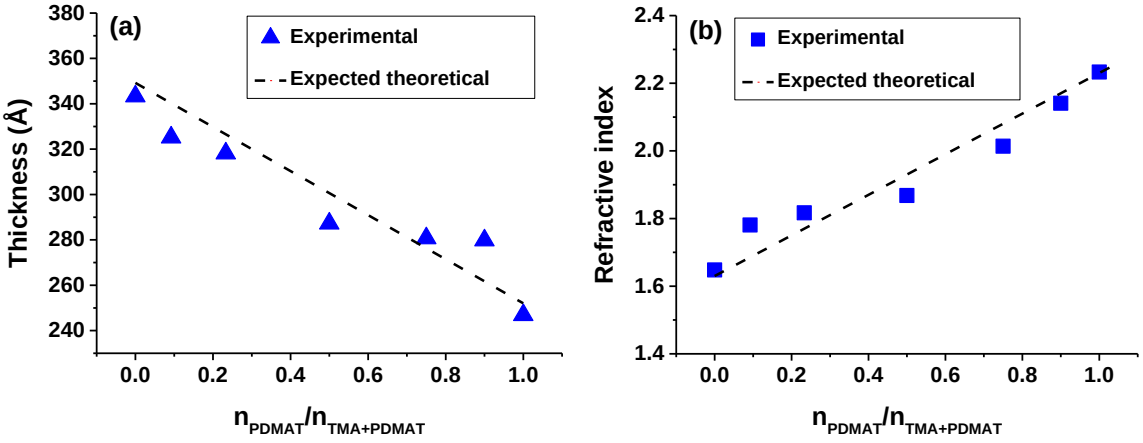

FIG. 4.11: (a) Thickness and (b) refractive index of ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films grown on Si(100) at 250 ºC using n=360 ALD cycles as a function of the Ta precursor ALD cycle fraction.

Figures 4.11a and 4.11b show the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films thickness and refractive index determined as a function of the PDMAT cycle fraction. It can be observed that the addition of Ta results in the decrease of the oxide films thickness and the increase of the refractive index. The thickness decreases from about 34 nm for pure Al_2O_3 to 25 nm for pure Ta_2O_5, whereas the refractive index increases from ~ 1.65 for Al_2O_3 to ~ 2.23 for pure Ta_2O_5. The experimental values obtained for the oxide films are close to the linear relationship with the PDMAT ALD cycle fraction expected based on the growth rate studies

carried out in section 4.2 for the pure oxides and the error of ≤10% estimated for the obtained thickness values.

4.4. Composition

The composition of ~ 10 nm thick ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ $(0 \leq x \leq 1)$ films was investigated by XPS analysis of the O 1s, Al 2p and Ta 4f core level spectra obtained for the samples before and after RTA at 600 ºC for 60 s under nitrogen ambient. The samples were deposited on GaN-capped AlGaN/GaN HEMT structures using different PDMAT ALD cycle fractions and a constant number of total ALD cycles (n = 120). The XPS measurements were performed without in situ sample cleaning treatment. The oxide composition was determined using the XPS peak area values obtained from experimental measurements of the sample surface and the Scofield sensitivity factors (SSF) and transmission functions (TXFN) provided by the instrument manufacturer for the O 1s, Al 2p and Ta 4f peaks.

The percentage atomic concentration of each element in a film, X_i, can be calculated using the following formula:[44]

$$X_i = 100\frac{A_i}{\sum_{j=1}^{m} A_i} \tag{4.2}$$

where:

$$A_i = \frac{I_i}{\mathrm{TXFN}(E_i)\mathrm{SSF}_i {E_i}^n} \tag{4.3}$$

A_i is the adjusted intensity determined from the measured intensity I_i in counts per second eV, the TXFN evaluated for electrons of recorded energy E_i, the SSF for the transition i and the escape depth compensation exponent n. The SSF corrects the raw intensity for sample and transition specific intensity variations, whereas the transmission and escape

depth correction terms are generally fixed for all samples and correct the measured intensity for instrumental influences.

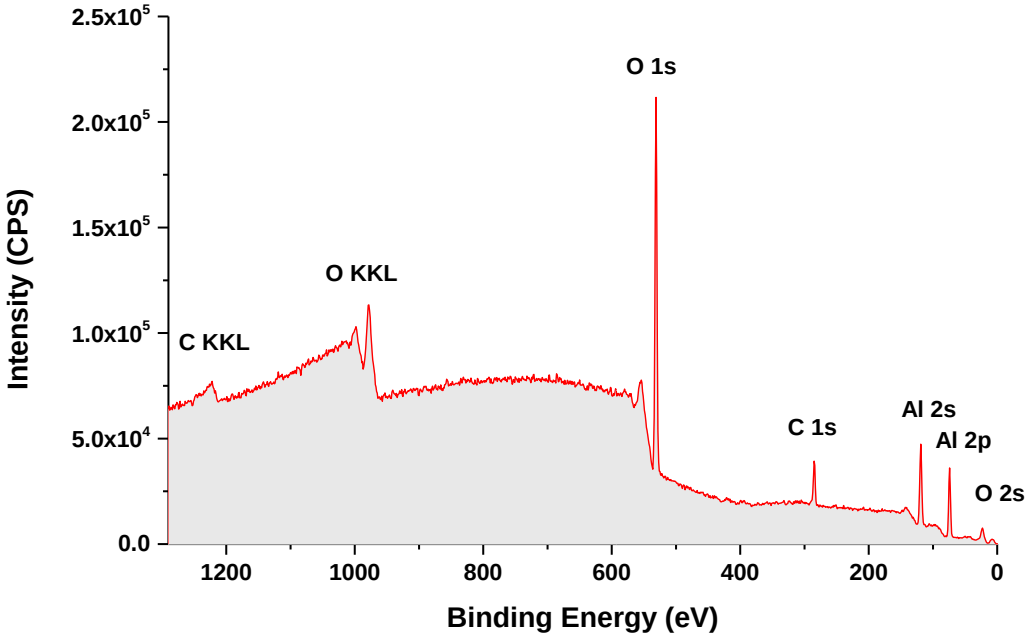

FIG. 4.12: XPS survey spectrum of as deposited ~ 10 nm thick ALD Al_2O_3 sample.

Figure 4.12 shows an example of the survey spectrum obtained for the as-deposited Al_2O_3 sample. Once the survey scan shows all the elements present on the sample surface, the quantification region for each selected peak can be defined and the acquisition of the high resolution XPS spectra for those peaks can be set up.

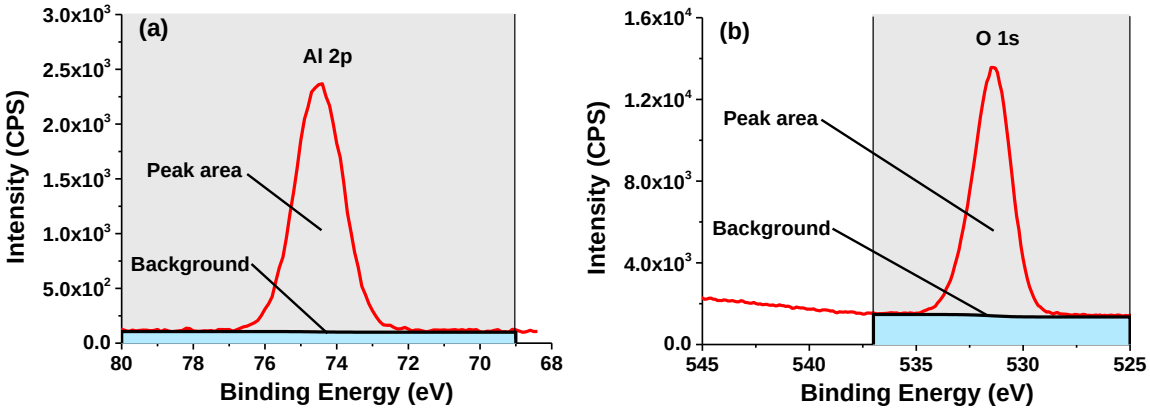

FIG. 4.13: XPS high resolution spectra of as-deposited Al_2O_3 (a) Al 2p peak and (b) O 1s peak.

Figure 4.13 shows the high resolution spectra obtained for the Al 2p and O 1s peaks. The standard approach to quantify the XPS spectra is to define the background signal. Once the background is removed, the parameters of the quantification regions such as peak position, intensity, FWHM and area can be measured. The quantification table is then computed using parameters which include the background type and the range of energies over which the background subtracted data is integrated to obtain the value for I_i and the SSF.

TABLE 4.3. Al 2p and O 1s peak BE, height, FWHM, area, area correction factor, transmission function, Scofield sensitivity factors and atomic percentages obtained for the as-deposited Al_2O_3 sample.

Peak	Al2p	O1s
Background	Shirley	Shirley
BE (eV)	74.5	531.4
Height (CPS)	2240.7	12168.8
FWHM (eV)	1.5	1.9
Area (CPS.eV)	3670.1	27754.0
Area (KE^0.6)	0.16	0.22
TXFN	566.81	686.3
SSF	0.537	2.93
Atomic %	40.9	59.1

Table 4.3 shows the quantification parameters generated used in the computation of the atomic concentrations. The XPS peaks binding energy (BE), height, FWHM and area are determined by Gaussian curve fitting after referencing all peak binding energies to the C 1s peak at 285.0 eV and subtracting the Shirley background from the spectra. The Area (CPS.eV) value in the quantification table corresponds to the raw intensity value, I_i, in

counts per second eV. The Area (KE^0.6) value is the energy dependent correction, E_i^n, calculated from the energy exponent with an assigned default value of – 0.6. It should be noticed that the exponent value in the quantification table is given a positive value of 0.6. This is because the correction to the area is made by the software using the expression $I_i \cdot E_i^{-n}$ rather than I_i/E_i^n. Finally, the atomic concentrations are computed by dividing the raw background subtracted area by the TXFN and the SSF and applying the energy dependent correction for each peak assigned a quantification region.

4.4.1. Al_2O_3

The composition of as-deposited and annealed Al_2O_3 samples was investigated from the Al 2p and O 1s photoelectron spectra obtained for the samples grown using TMA and water (Figs. 4.14a-d). The data points represent the measured experimental data and the solid lines represent the Gaussian peak fitting results. In both cases, the XPS Al 2p peaks are symmetric and can be fitted with a single peak attributed to the Al-O chemical bond in Al_2O_3.[45] (Figs. 4.14a and 4.14b). A common value reported in literature for the Al 2p peak position is 74.6 eV.[46] The XPS O 1s spectra can be de-convoluted into two components: a main O 1s peak located at lower binding energy, attributed to the Al-O chemical bond in Al_2O_3,[45] and a small peak at higher binding energy, assigned to surface contamination (S.C) such as carboxyl groups or hydroxyl groups in aluminium hydroxide,[47, 48] (Figs. 4.14c and 4.14d). The typical position for the O 1s peak in literature is 531.3 eV,[46] and the difference between the O 1s and S.C. component binding energies for oxides is reported to be within the range of 1.3–1.4 eV.[49, 50]

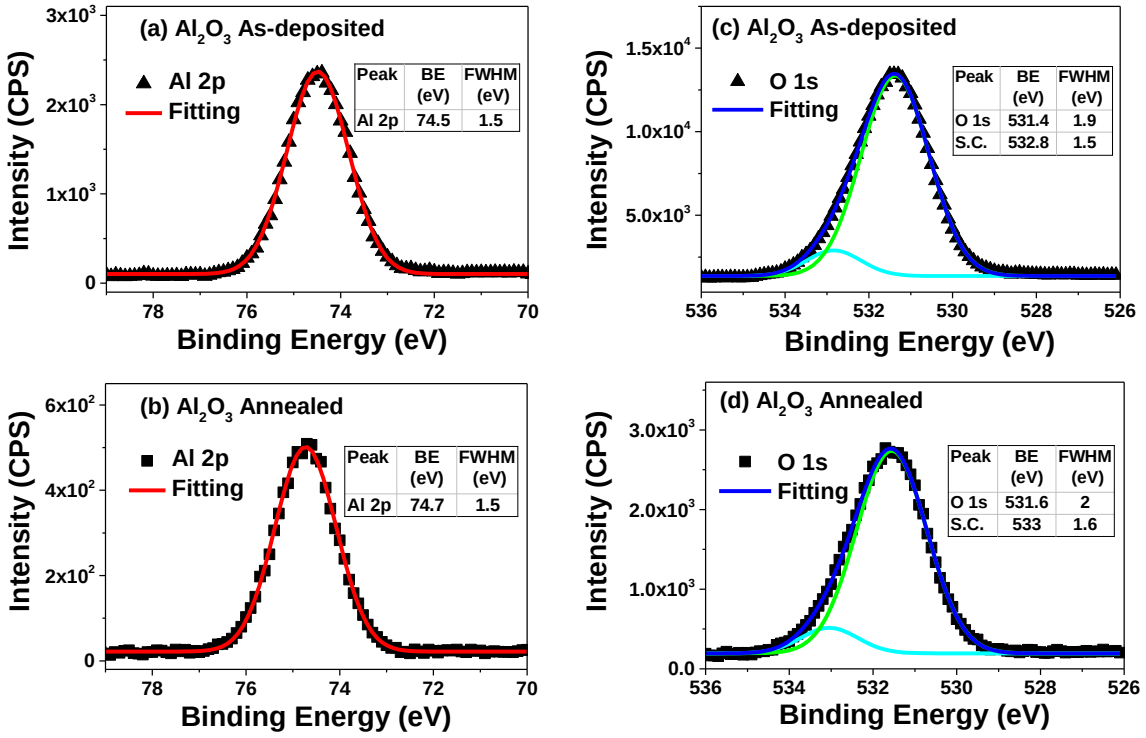

FIG. 4.14: XPS spectra of ~ 10 nm thick ALD Al_2O_3 showing (a) Al 2p core level of as-deposited sample, (b) O 1s core level of as-deposited sample; (c) Al 2p core level of annealed sample and (d) O 1s core level of annealed sample.

All the peak positions obtained experimentally are in good agreement with literature values reported for stoichiometric Al_2O_3, and the XPS spectra show no significant changes after the annealing process used. For the as-deposited sample, the Al 2p peak is located at 74.5 eV with FWHM of 1.5 (Fig.4.14a) and the O 1s peak is located at 531.4 eV with FWHM of 1.9 (Fig.4.14b). For the annealed sample, the Al 2p peak is located at 74.7 eV with FWHM of 1.5 eV (Fig.4.14c) and the O 1s peak is located at 531.6 eV with FWHM of 2.0 eV (Fig.4.14d). The peak positions of the annealed sample show a shift of 0.2 eV to higher binding energies. This shift is observed for all the core levels analysed and thus it can be attributed to the error range of ± 0.1-0.2 eV associated with the use of the C 1s spectrum as charge reference to correct surface charge in the oxide films due to their insulating nature.[51] A slight variation in the Al 2p and O 1s peaks FWHM values of 0.1 eV can also be observed after annealing, but this variation is significantly smaller than the

minimum energy broadening resolution of about ~ 0.25 eV achievable in monochromatic electron energy analysers.[52] Therefore, no significant changes are observed for the Al 2p and O 1s peaks associated with the oxide films after annealing.

TABLE 4.4. Al 2p and O 1s peak BE, height, FWHM, area, area correction factor, transmission function, Scofield sensitivity factors and atomic percentages obtained for the as-deposited and annealed Al_2O_3 samples.

Sample	As-deposited Al_2O_3		Annealed Al_2O_3	
Peak	Al2p	O1s	Al2p	O1s
Background	Shirley	Shirley	Shirley	Shirley
BE (eV)	74.5	531.4	74.7	531.6
Height (CPS)	2240.7	12168.8	481.7	2544.7
FWHM (eV)	1.5	1.9	1.5	2.0
Area (CPS.eV)	3670.1	27754.0	802.1	5933.8
Area (KE^0.6)	0.16	0.22	10.74	15.9
TXFN	566.81	686.3	1.79	2.07
SSF	0.537	2.93	0.537	2.93
Atomic %	40.9	59.1	40.3	59.7

Table 4.4 shows the quantification parameters obtained for the as-deposited and annealed Al_2O_3 samples. The atomic percentages of aluminium and oxygen calculated from XPS are very close to stoichiometric Al_2O_3 and confirm that the annealing process used has no significant effects in the films composition. The aluminium to oxygen atomic percentage ratios (Al/O) determined for the as-deposited and annealed samples are 40.9/59.1 and 40.3/59.7, respectively. These values are in very good agreement with the 40/60 stoichiometric value of Al_2O_3 considering the quantitative error of 5-10% of the value reported associated with the atomic percentage (at.%) calculation for major XPS peaks.[53] Thus, it can be concluded that no significant effects in terms of composition of the ALD Al_2O_3 films are observed after annealing.

4.4.2. Ta_2O_5

The composition of as-deposited and annealed Ta_2O_5 samples was determined from the Ta 4f and O 1s XPS spectra obtained for the samples grown from PDMAT and water (Figs.4.15a-d). The XPS Ta 4f spectra of both samples are fitted with a doublet of peaks, $4f_{7/2}$ and $4f_{5/2}$, with energy separation of 1.91 eV and $4f_{7/2}$ to $4f_{5/2}$ peak area ratio of 4:3 (Figs. 4.15a and 4.15b).[54] The literature average value of the Ta $4f_{7/2}$ peak BE in Ta_2O_5 is 26.56 eV.[55] The O 1s spectra are fitted to two Gaussian curve peaks (Figs. 4.15c and 4.15d). The main O 1s peak at lower binding energy corresponds to the Ta-O chemical bond in Ta_2O_5,[56] of which values found in literature range from 530.5 eV to 531.3 eV,[57, 58] and the small peak located at higher binding energy is attributed carboxyl and/or hydroxyl groups absorbed at the surface (S.C.).[58-60]

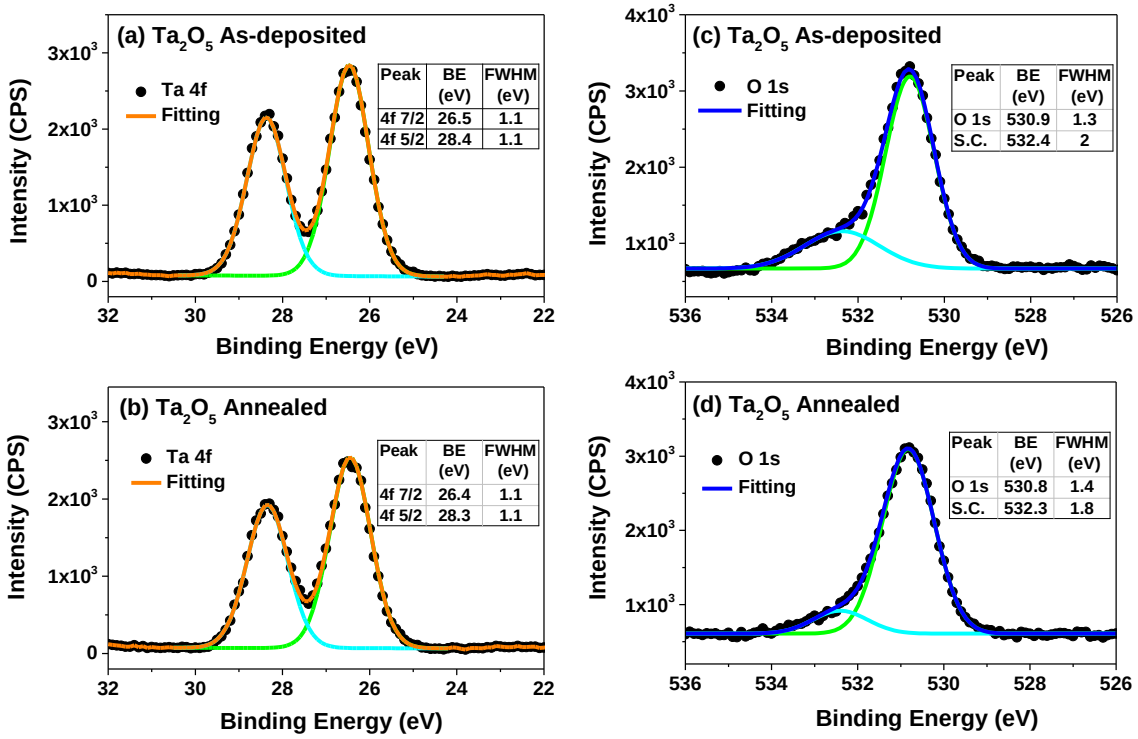

FIG. 4.15: XPS spectra of ~ 10 nm thick ALD Ta_2O_5 showing (a) Ta 4f core level of as-deposited sample, (b) O 1s core level of as-deposited sample; (c) Ta 4f core level of annealed sample and (d) O 1s core level of annealed sample.

The experimental values obtained for the Ta 4f and O 1s peak positions are consistent with the literature values of stoichiometric Ta_2O_5, and the measured XPS spectra show no significant changes after the annealing process. For the as-deposited sample, the Ta $4f_{7/2}$ and Ta $4f_{5/2}$ peaks core levels are located at 26.5 eV and 28.4 eV respectively, with a FWHM value of 1.1 eV for both peaks (Fig. 4.15a). The O 1s peak is located at 530.9 eV with FWHM of 1.3 (Fig. 4.15c). The Ta $4f_{7/2}$ and Ta $4f_{5/2}$ core levels for the annealed sample are located at 26.4 eV and 28.3 eV with FWHM of 1.1 eV (Fig. 4.15b) and the O 1s peak is located at 530.8 eV with FWHM of 1.4 eV (Fig. 4.15d). The only significant change observed after annealing is a reduction of the S.C. peak in the O 1s spectrum. However, no significant changes are observed for the Ta 4f and O 1s peaks associated to the annealed oxide film. This reduction of the S.C. peak of annealed Ta_2O_5 is attributed to the removal of the surface OC and OH bonds by the annealing process.[61] This is in agreement with published work that has reported that heating in N_2 is beneficial for Ta_2O_5 films.[58]

TABLE 4.5. Ta 4f and O 1s peak BE, height, FWHM, area, area correction factor, transmission function, Scofield sensitivity factors and atomic percentages obtained for the as-deposited and annealed Ta_2O_5 samples.

Sample	As-deposited Ta_2O_5		Annealed Ta_2O_5	
Peak	$Ta4f_{7/2}$	O1s	Ta4f	O1s
Background	Shirley	Shirley	Shirley	Shirley
BE (eV)	26.5	530.9	26.4	530.8
Height (CPS)	2777.1	2593.9	2475.3	2483.3
FWHM (eV)	1.1	1.3	1.1	1.4
Area (CPS.eV)	3185.3	4432.7	2946.6	4077.6
Area (KE^0.6)	4.72	11.88	4.36	10.93
TXFN	1.77	2.07	1.77	2.07
SSF	4.82	2.93	4.82	2.93
Atomic %	28.4	71.6	28.5	71.5

Table 4.5 shows the quantification parameters obtained for the as-deposited and annealed Ta_2O_5 samples. The tantalum and oxygen atomic percentages calculated for the samples are very close to stoichiometric Ta_2O_5 and no significant changes are observed in the oxide layers composition after annealing. The tantalum to oxygen atomic percentage ratios (Ta/O) obtained for the as-deposited and annealed Ta_2O_5 samples are 28.4/71.6 and 28.5/71.5, respectively, which are very close to the 28.6/71.4 stoichiometric value of Ta_2O_5. Therefore, annealing has no significant effect on the ALD Ta_2O_5 films composition.

4.4.3. $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 < x < 1$) films

$(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples with three selected compositions were grown to investigate the variation of the elemental atomic percentages in the ALD oxide films as a function of the Ta precursor ALD cycle fraction. The three oxide films were grown using Ta precursor ALD cycle fractions of approximately 1/10, 1/4 and 1/2 and are denoted as 10%Ta-Al_2O_3, 25%Ta-Al_2O_3 and 50%Ta-Al_2O_3, respectively (see section 4.3.3 for more details). The XPS Ta 4f, Al 2p and O 1s spectra used to calculate the composition of the samples are shown in Figures 4.16-4.18.

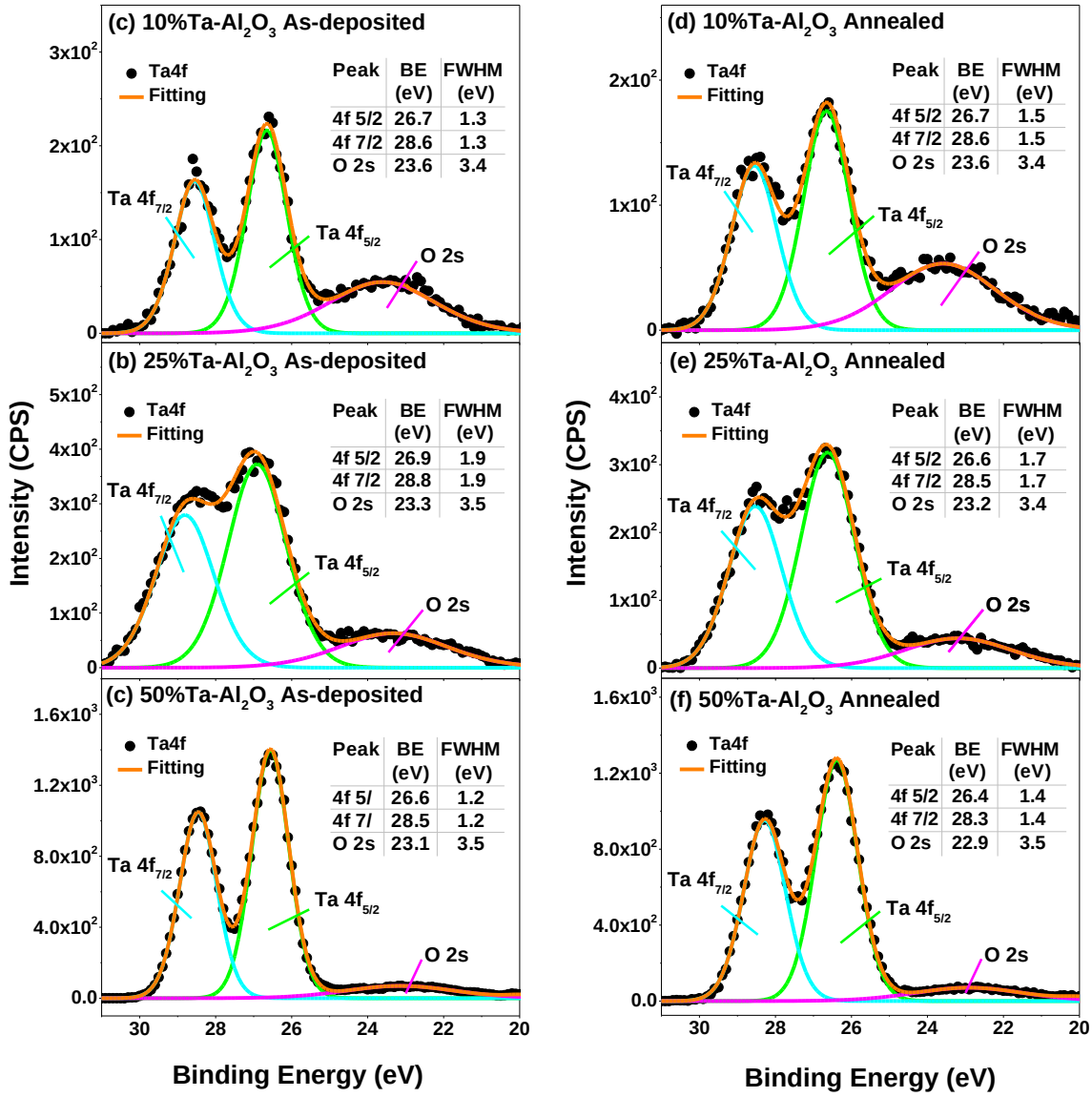

FIG. 4.16: XPS Ta 4f spectra of ~ 10 nm thick as-deposited (a) 10%Ta-Al_2O_3, (b) 25%Ta-Al_2O_3 and (c) 50%Ta-Al_2O_3; and annealed (d) 10%Ta-Al_2O_3, (e) 25%Ta-Al_2O_3 and (f) 50%Ta-Al_2O_3.

Figures 4.16a-f show the Ta 4f spectra of the as-deposited and annealed 10%Ta-Al_2O_3, 25%Ta-Al_2O_3 and 50%Ta-Al_2O_3 samples. The spectra are fitted with three peaks. The doublet of peaks at higher BE corresponds to the Ta $4f_{7/2}$ and Ta $4f_{5/2}$ peaks and the third peak at lower BE is associated with O 2s.[62] It can be observed that the relative intensity of the O 2s peak shows a reduction with the increase of the Ta content. This is the reason why the Ta 4f spectra obtained for the Ta_2O_5 samples in the previous section were dominated by the Ta $4f_{7/2}$ and Ta $4f_{5/2}$ peaks and the O 2s peak was not visible.

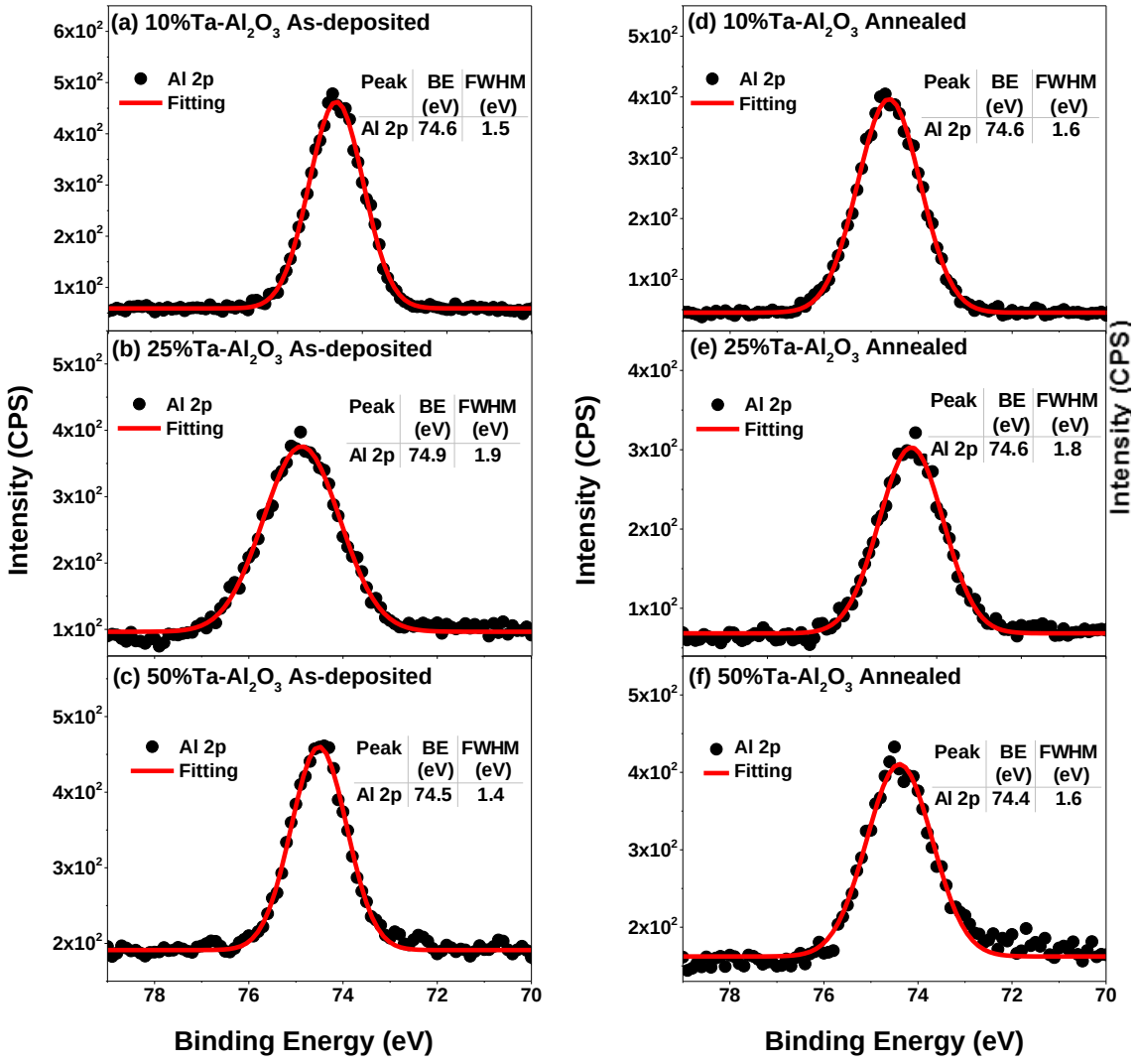

FIG. 4.17: XPS Al 2p spectra of ~ 10 nm thick as-deposited (a) 10%Ta-Al_2O_3, (b) 25%Ta-Al_2O_3 and (c) 50%Ta-Al_2O_3; and annealed (d) 10%Ta-Al_2O_3, (e) 25%Ta-Al_2O_3 and (f) 50%Ta-Al_2O_3.

Figures 4.17a-f show the XPS Al 2p spectra of the as-deposited and annealed 10%Ta-Al_2O_3, 25%Ta-Al_2O_3 and 50%Ta-Al_2O_3 samples. The Al 2p spectra are symmetric and fitted to one single peak, consistent with the spectra obtained for the Al_2O_3 samples.

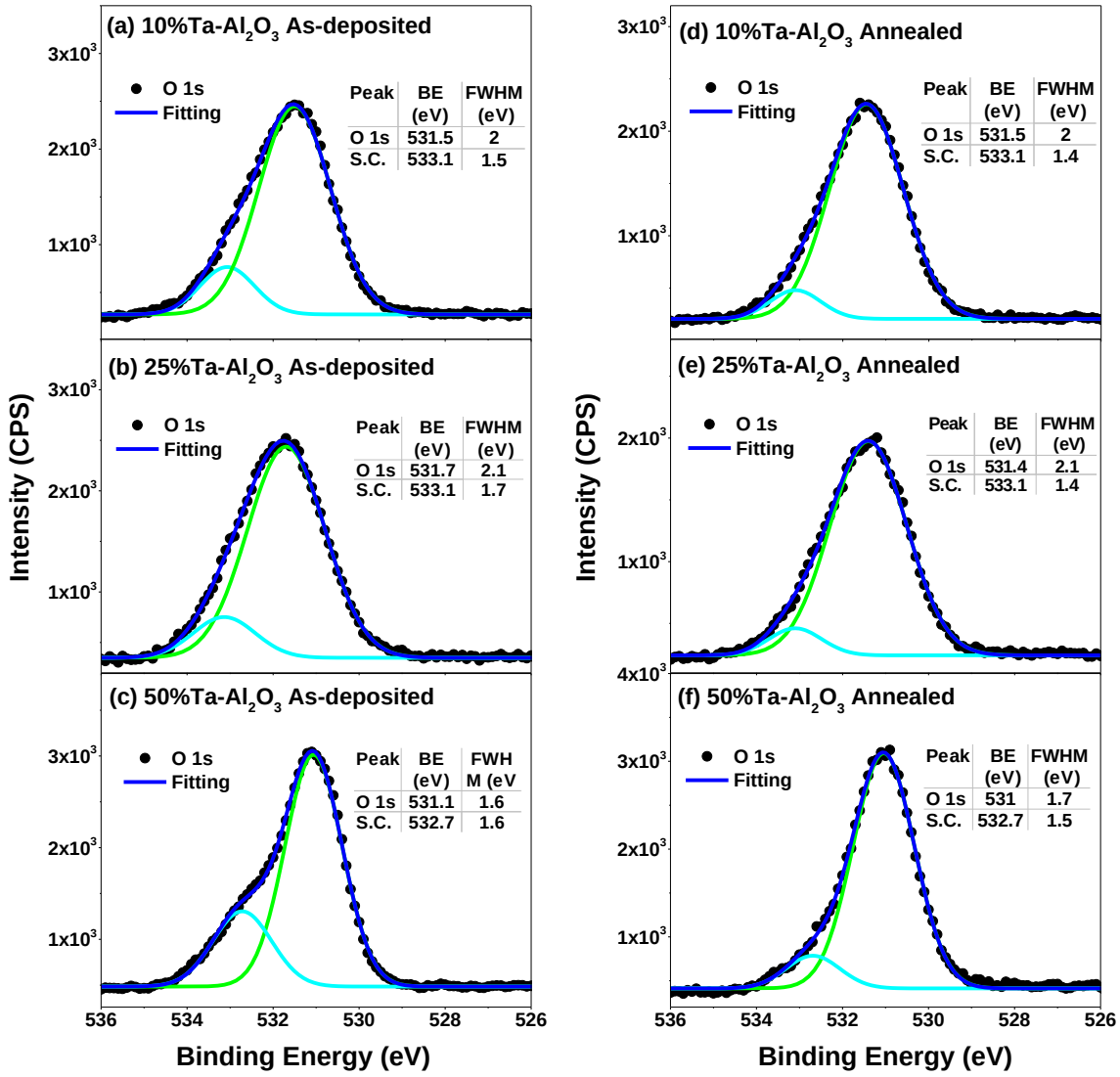

FIG. 4.18: XPS O 1s spectra of ~ 10 nm thick as-deposited (a) 10%Ta-Al_2O_3, (b) 25%Ta-Al_2O_3 and (c) 50%Ta-Al_2O_3; and annealed (d) 10%Ta-Al_2O_3, (e) 25%Ta-Al_2O_3 and (f) 50%Ta-Al_2O_3.

Figures 4.18a-f show the experimental O 1s spectra of the as-deposited and annealed 10%Ta-Al_2O_3, 25%Ta-Al_2O_3 and 50%Ta-Al_2O_3 samples. As occurred with the spectra obtained for the pure Al_2O_3 and Ta_2O_5 samples, the O 1s signals can be deconvoluted into two Gaussian components corresponding to the O 1s peak and to S.C.

The experimental Ta 4f, Al 2p and O 1s spectra of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples can be compared to the spectra obtained for the pure Al_2O_3 and Ta_2O_5 samples, and no significant changes are observed after the annealing process. Only a shift of 0.3eV to higher BEs is observed in the Ta 4f, Al 2p and O 1s core levels of the as-deposited 25%Ta-doped Al_2O_3 sample with respect the annealed one. However, although the shift is slightly bigger than the typical error of ~ 0.1-0.2 eV associated to surface charge correction, it is universal for all the peak core levels and it can still be attributed to the use of the C 1s spectrum as reference charge.[63, 64] Thus, the results show that the Ta 4f and Al 2p peak core levels measured for the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples are in very good agreement with the Ta 4f and Al 2p core levels obtained for pure Ta_2O_5 and Al_2O_3, respectively. On the other hand, a shift of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples O 1s core level to lower BEs is observed with the increase of the Ta ALD cycle fraction. This shift is consistent with the reduction of the O 1s BE reported in literature for $(HfO_2)_x(Al_2O_3)_{1-x}$ with the increase of the HfO_2 concentration.[65] The decrease in the O 1s BE with the Ta content is due to the fact that Ta is a more ionic cation than Al in $(Ta_2O_5)_x(Al_2O_3)_{1-x}$, and thus the charge transfer contribution changes with the increase of the Ta_2O_5 concentration.[66, 67] As a result, the experimental O 1s spectra BEs of the 10%Ta-Al_2O_3 and 25%Ta-Al_2O_3 samples are very close to the O 1s BE obtained for pure Al_2O_3 due to their relatively low Ta content, whereas the O 1s core level of the 50%Ta-Al_2O_3 samples is found to be closer to the value obtained for Ta_2O_5 as a consequence of their higher percentage of Ta in the samples. Finally, the O 1s spectra of the three $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples show a consistent reduction of the S.C. peak after annealing. This confirms that the annealing process can remove OC or OH bonds at the oxide films surface.[61]

TABLE 4.6a. Ta 4f, Al 2p and O 1s peak BE, height, FWHM, area, area correction factor, transmission function, Scofield sensitivity factors and atomic percentages obtained for the as-deposited and annealed 10%Ta-Al_2O_3 samples.

Sample	As-deposited 10%Ta-Al_2O_3			Annealed 10%Ta-Al_2O_3		
Peak	$Ta4f_{7/2}$	Al2p	O1s	Ta4f	Al2p	O1s
Background	Shirley	Shirley	Shirley	Shirley	Shirley	Shirley
BE (eV)	26.7	74.6	531.5	26.7	74.6	531.5
Height (CPS)	217.3	408.5	2193.1	175.9	358.9	2060.4
FWHM (eV)	1.3	1.5	2.0	1.5	1.6	2.0
Area (CPS.eV)	294.6	677.7	5507.1	269.1	607.9	49224
Area (KE^0.6)	0.44	9.07	14.76	0.4	8.14	13.19
TXFN	1.77	1.79	2.07	1.77	1.79	2.07
SSF	4.82	0.537	2.93	4.82	0.537	2.93
Atomic %	1.8	37.4	60.8	1.8	37.5	60.7

TABLE 4.6b. Ta 4f, Al 2p and O 1s BE, height, FWHM, area, area correction factor, transmission function, Scofield sensitivity factors and atomic percentages obtained for the as-deposited and annealed 25%Ta-Al_2O_3 samples.

Sample	As-deposited 25%Ta-Al_2O_3			Annealed 25%Ta-Al_2O_3		
Peak	$Ta4f_{7/2}$	Al2p	O1s	Ta4f	Al2p	O1s
Background	Shirley	Shirley	Shirley	Shirley	Shirley	Shirley
BE (eV)	26.9	74.9	531.7	26.6	74.6	531.4
Height (CPS)	373.8	290.6	2131.5	319.1	237.7	1748.6
FWHM (eV)	1.9	1.9	2.1	1.7	1.8	2.1
Area (CPS.eV)	729.9	603.6	5484.1	577.9	473.7	4333.1
Area (KE^0.6)	1.08	8.08	14.7	0.86	6.34	11.61
TXFN	1.77	1.79	2.07	1.77	1.79	2.07
SSF	4.82	0.537	2.93	4.82	0.537	2.93
Atomic %	4.5	33.9	61.6	4.6	33.7	61.7

TABLE 4.6c. Ta 4f, Al 2p and O 1s peak BE, height, FWHM, area, area correction factor, transmission function, Scofield sensitivity factors and atomic percentages obtained for the as-deposited and annealed 50%Ta-Al_2O_3 samples.

Sample	As-deposited 50%Ta-Al_2O_3			Annealed 50%Ta-Al_2O_3		
Peak	Ta4f$_{7/2}$	Al2p	O1s	Ta4f	Al2p	O1s
Background	Shirley	Shirley	Shirley	Shirley	Shirley	Shirley
BE (eV)	26.6	74.5	531.1	26.4	74.4	531.0
Height (CPS)	1402.2	275.9	2560.4	1246.7	254.5	2708.0
FWHM (eV)	1.2	1.4	1.6	1.4	1.6	1.7
Area (CPS.eV)	1744.9	441.9	5704.6	1735.8	434.8	5645.3
Area (KE^0.6)	2.58	5.92	15.29	2.57	5.82	15.13
TXFN	1.77	1.79	2.07	1.77	1.79	2.07
SSF	4.82	0.537	2.93	4.82	0.537	2.93
Atomic %	10.9	24.9	64.3	10.9	24.8	64.3

The quantification parameters obtained for the as-deposited and annealed 10%Ta-Al_2O_3, 25%Ta-Al_2O_3 and 50%Ta-Al_2O_3 samples are given in Tables 4.6a-c. The calculated ratios of tantalum, aluminium and oxygen (Ta/Al/O) have very good stoichiometry and confirm that the oxide films composition is not affected by the annealing process. The (Ta/Al/O) values obtained for the as-deposited and annealed 10%Ta-Al_2O_3, 25%Ta-Al_2O_3 and 50%Ta-Al_2O_3 samples are very close to the stoichiometric values of (2.0/37.3/60.8), (4.6/33.6/61.8) and (4.6/33.6/61.8), which correspond to Ta_2O_5 mole fractions of $x = 0.05$, $x = 0.12$ and of $x = 0.31$, respectively. Thus, the composition of the samples can be expressed as $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$, $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ and $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$, respectively. In addition to this, the results demonstrate that the annealing process has no significant effect on the oxide films composition. This is expected as there are previous studies that show that the chemical composition of ALD Al_2O_3 and Ta_2O_5 films is not affected by annealing processing.[35, 68] Post-deposition annealing is normally used during device processing and the chemical stability of the oxide films is one

of the requirements for their integration as high-κ gate dielectrics. Therefore, the XPS results obtained in this study demonstrate that the deposited $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films fulfil this requirement.

TABLE 4.7. Atomic percentage of the Ta 4f, Al 2p and O 1s core level spectra obtained by XPS for the ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples as-deposited and after annealing in N_2 at 600 °C 60 s.

	As-deposited			Annealed			
$n_{PDMAT}/(n_{TMA+PDMAT})$	Ta 4f 7/2 (at.%)	Al 2p (at.%)	O 1s (at.%)	Ta 4f 7/2 (at.%)	Al 2p (at.%)	O 1s (at.%)	Ta_2O_5 mole fraction value, *x*, as in $(Ta_2O_5)_x(Al_2O_3)_{1-x}$
0	-	40.9	59.1	-	40.3	59.7	0
0.09	1.8	37.4	60.8	1.8	37.5	60.7	0.05
0.23	4.5	33.9	61.6	4.6	33.7	61.7	0.12
0.50	10.9	24.9	64.3	10.9	24.8	64.3	0.30
1	28.4	-	71.6	28.5	-	71.5	1

The atomic percentages of tantalum, aluminium and oxygen obtained for the as-deposited and annealed $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples, together with their corresponding Ta_2O_5 molar fraction value, *x*, are summarised in Table 4.7.

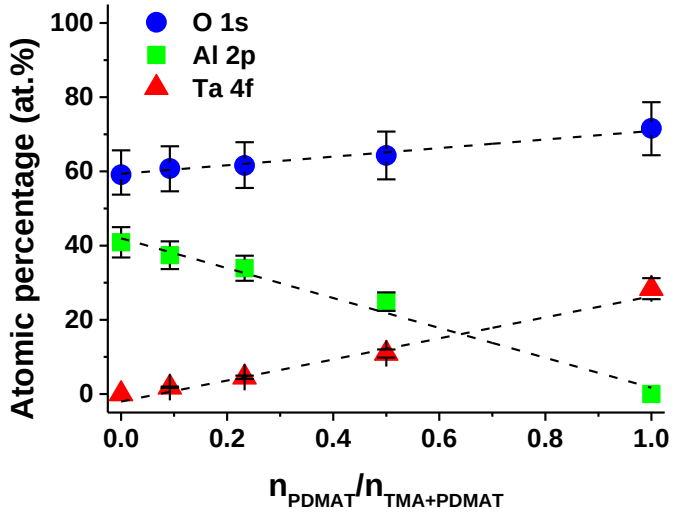

FIG. 4.19: Atomic percentage of the O 1s, Al 2p and Ta 4f core level spectra obtained by XPS for the ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples as-deposited and after annealing in N_2 at 600 °C 60 s, as a function of the PDMAT precursor ALD cycle fraction.

Figure 4.19 shows the atomic percentage of tantalum, aluminium and oxygen of the samples as a function of the Ta ALD cycle fraction. XPS results show that the percentage of the different elements in the samples varies linearly with the PDMAT cycle fraction. The fact that the Ta concentration is smaller that the fraction of PDMAT cycles added to the deposition process means that the proportion of dopant incorporated per cycle is likely to be dominated by steric hindrance.[69] This relationship between the PDMAT cycle fraction and the doping concentration is most probably determined by a combination of precursor reactivity and molecule size.[70] The bulkier precursor ligands in the PDMAT are likely to cause steric hindrance on the film surface, resulting in a more sparse distribution of the dopants, therefore a lower doping fraction.[71]

4.5. Conclusions

ALD with modulation doping has been used to grow $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ as a novel gate dielectric for GaN-based HEMT structures. XRD analysis shows that the crystallisation temperature of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers decreases with the introduction of Ta, with a minimum crystallisation temperature of 750 ºC obtained for pure Ta_2O_5. XPS measurements show that the composition of the ALD-$(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films has good stoichiometry and varies linearly with the Ta-dopant precursor ALD cycle fraction. $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers grown on HEMT structures have been analysed before and after annealing in N_2 at 600 ºC for 60 s. This post-deposition annealing step used during HEMT processing does not affect the microstructure and composition of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films, which gives the thermal and chemical stability needed for their application as gate dielectrics. These results demonstrate that ALD with modulation doping can be used to optimally control the composition of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ as gate dielectric to achieve low leakage currents in next generation GaN-based power devices.

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5. Electronic and dielectric properties of ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films

5.1. Introduction

This chapter describes a method to optimally combine wide bandgap Al_2O_3 with high-κ Ta_2O_5 for gate dielectric applications. The electronic and dielectric properties of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ thin films deposited by thermal ALD have been studied as a function of the Ta_2O_5 molar fraction, *x*, together with the impact of post-deposition annealing in N_2 at 600 ºC on these properties. XPS shows that the bandgap of the oxide films linearly decreases from 6.5 eV for pure Al_2O_3 to 4.6 eV for pure Ta_2O_5. The dielectric constant calculated from CV measurements at 100 kHz also increases linearly from 7.8 for Al_2O_3 up to 25.6 for Ta_2O_5. These values are in good agreement with literature values reported for Al_2O_3 and Ta_2O_5.[1-4] The VBO and CBO of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers grown on GaN-on-Si substrates investigated from XPS also decrease linearly with the *x* molar fraction. The VBO decreases from 1.0 eV for Al_2O_3/GaN to 0.3 eV for Ta_2O_5/GaN, whereas the CBO decreases from 1.9 eV for Al_2O_3/GaN to 0.8 eV for Ta_2O_5/GaN. After annealing, the band offsets shift and the VBO decreases from 1.2 eV for Al_2O_3/GaN to – 0.1 eV for Ta_2O_5/GaN, whereas the CBO decreases from 1.8 eV for Al_2O_3/GaN to 1.2 eV for Ta_2O_5/GaN. This change in the interfacial properties of the samples caused by the post-deposition annealing step used during device processing can affect the performance of the gate oxide if the resultant band offsets are < 1 eV.[5] The results demonstrate that ALD of Ta-doped Al_2O_3 can be used to control the properties of the gate dielectric, allowing the κ value to be increased, while still maintaining a sufficient CBO to GaN for low leakage currents.

5.2. Bandgap of ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers

The bandgap of the ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 \leq x \leq 1$) samples used in the previous chapter for composition studies was investigated as a function of the *x* molar fraction before and after RTA in N_2 at 600 ºC for 60 s. The bandgap energies of the oxide films were calculated by measuring the difference between the core level peak and the onset of inelastic loss from the XPS O 1s core level energy-loss spectra.[6]

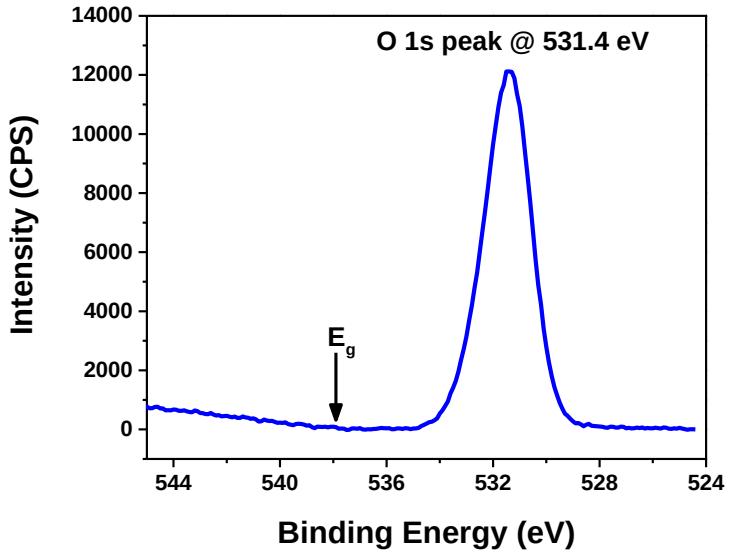

FIG. 5.1: XPS O 1s spectra of as-deposited ~ 10 nm thick Al_2O_3 sample.

Figure 5.1 shows an example of a high-resolution scan of the O 1s spectrum obtained for the as-deposited Al_2O_3 sample. The lower limit of inelastic loss is equal to the bandgap energy of insulators or wide bandgap intrinsic semiconductors. Although in principle any core-level spectra will exhibit the same inelastic losses, the measured photoelectron intensity must be large enough so that a sufficient signal-to-noise ratio can be achieved with suitably high resolution.[6] Consequently, the O 1s core level is usually chosen in oxides due to its high intensity.[6]

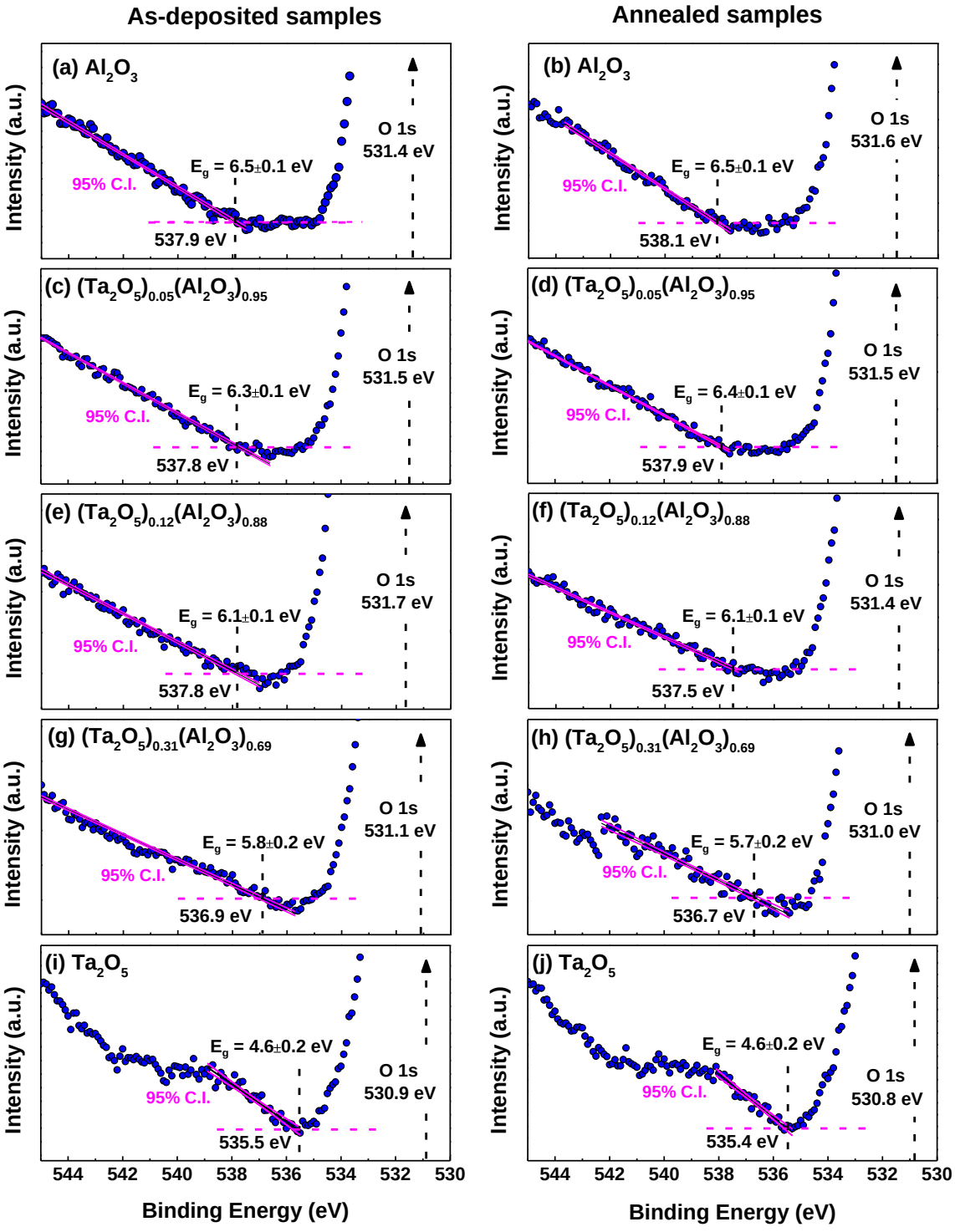

FIG. 5.2: XPS O 1s energy-loss spectra used to calculate the bandgap of ~ 10 nm thick ALD (a) Al_2O_3 as-deposited, (b) Al_2O_3 annealed, (c) $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ as-deposited, (d) $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ annealed, (e) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as-deposited, (f) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ annealed, (g) $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ as-deposited, (h) $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ annealed, (i) Ta_2O_5 as-deposited and (j) Ta_2O_5 annealed. The circular points represent the experimental data, the onsets of energy loss is indicated with dashed lines and the O 1s core level is indicated with dashed arrows.

Figures 5.2a-j show the experimental onset of inelastic losses near the O 1s core level measured for the as-deposited and annealed $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples. In order to determine the bandgap energy of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films, a Shirley background fitting was subtracted from the O 1s spectra and the resulting background level was used as the zero-intensity reference.[7] The O 1s peak BE was determined using Gaussian curve fitting (as shown in section 4.4). Finally, the onsets of inelastic losses energy was found by extrapolating a linear fit with 95% confidence interval (C.I.) applied to the loss spectra curve near the location of onset of inelastic losses (solid lines) and calculating its intersection with the 'zero' background level (dashed horizontal line).

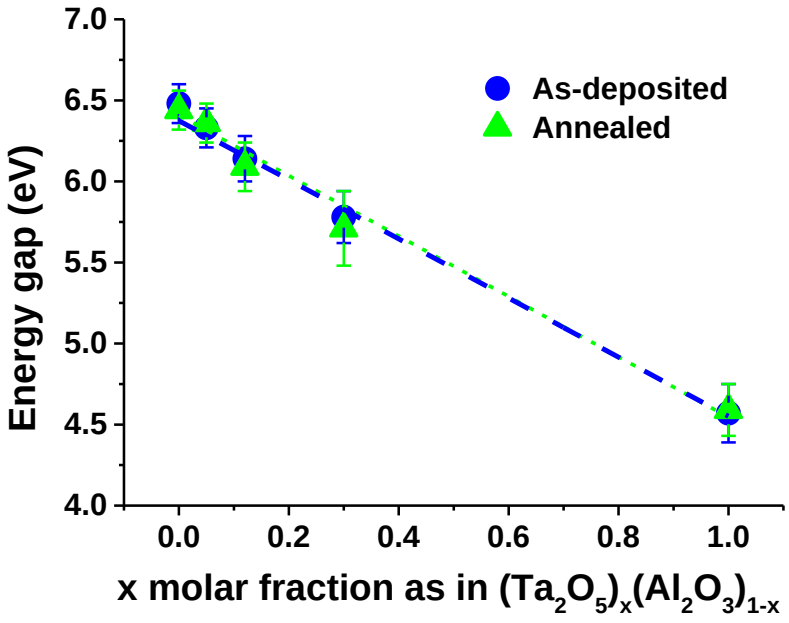

FIG. 5.3: Bandgap of as-deposited and annealed ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers as a function of the molar fraction, *x*.

Figure 5.3 shows the bandgap values determined with a 95% reliability for the as-deposited and annealed $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films as a function of the Ta_2O_5 mole fraction. The results show that the bandgap of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples decreases linearly with the Ta_2O_5 fraction and no significant changes are observed after the annealing process. The bandgap value of pure Al_2O_3 is calculated to be 6.5 ± 0.1 eV for both the as-deposited and

the annealed samples (Figs. 5.1a-b), which is in good agreement with literature values of 6.5 eV reported for amorphous Al_2O_3 grown by ALD.[1, 2] The bandgap of Al_2O_3 strongly depends on the crystallographic phases and synthesis method, with experimental values reported including 8.8 eV for α-Al_2O_3,[8] 8.7–7.1 eV for γ-Al_2O_3[9-11] and 7.0–5.1 eV for amorphous Al_2O_3.[12-15] This reduction in bandgap for amorphous Al_2O_3 is attributed to the lower coordination number of Al atoms and density with respect to crystalline Al_2O_3, which causes changes in the charge transfer from the Al to the O atom leading to shifts at the bottom of the conduction band edge.[16, 17] The value obtained for the Ta_2O_5 films before and after annealing is 4.6 ± 0.2 eV (Figs. 5.2i-j), which is close to previously reported values of ~ 4.5 eV for amorphous Ta_2O_5 deposited by ALD.[3] This value is within the range of experimental bandgap values reported for Ta_2O_5, which include 3.9-4.5 eV[3, 18-20] for crystalline Ta_2O_5 and 4.2-5.3 eV[18, 20, 21] for amorphous Ta_2O_5. These values are very dependent on the crystal structure and fabrication method, with an observed reduction in the bandgap of Ta_2O_5 caused by the transition from the amorphous to the crystalline phase.[18] From linear fitting, the value of the bandgap (E_g) of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films can be expressed as:

$$E_g = 6.45 - 1.80\,x \qquad (5.1)$$

A linear dependence between the bandgap and the x molar fraction has also been reported for other oxides such as ALD $(HfO_2)_x(Al_2O_3)_{1-x}$[2] as well as for $Zn_{1-x}Mg_xO$ and $Cd_{1-x}Mg_xO$ alloys.[22, 23] This means that the Ta_2O_5 concentration and the bandgap energy of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ gate dielectric can be tuned by ALD modulation doping.

5.3. Dielectric constant of ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers

To investigate the electrical properties of the ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers as a function of the Ta_2O_5 molar fraction, CV and IV measurements were carried out on 1 ± 0.1 mm and 300 ± 15 µm diameter Au/oxide/Si(100) MOS capacitors. The variance for the top contacts size were estimated based on optical microscopy measurements. These variations arise from not perfect contact between the shadow mask and the samples surface during Au sputtering.

The dielectric constant of the oxide films was calculated from the CV measurements using the following relationship:

$$\kappa = \frac{C_{ox}\, t_{ox}}{\varepsilon_0\, A} \tag{5.2}$$

where C_{ox} is the oxide capacitance in F, t_{ox} is the gate oxide thickness in m, $\varepsilon_0 = 8.85\times10^{-12}$ F/m and A is the device area in m^2.

C_{ox} was calculated using a series capacitance model considering a 15 ± 1 Å SiO_2 interlayer between the oxide films and the Si substrate, as given by equation 5.3 below. The parameters of the SiO_2 interfacial layer were determined based on the thickness and fitting errors obtained from ellipsometry measurements performed on the Si(100) substrates prior to the deposition of the ALD oxide films.

$$\frac{1}{C} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{ox}} \tag{5.3}$$

where C is the MOS capacitance measured in the accumulation region and C_{SiO_2} is the capacitance of the SiO_2 interfacial layer.

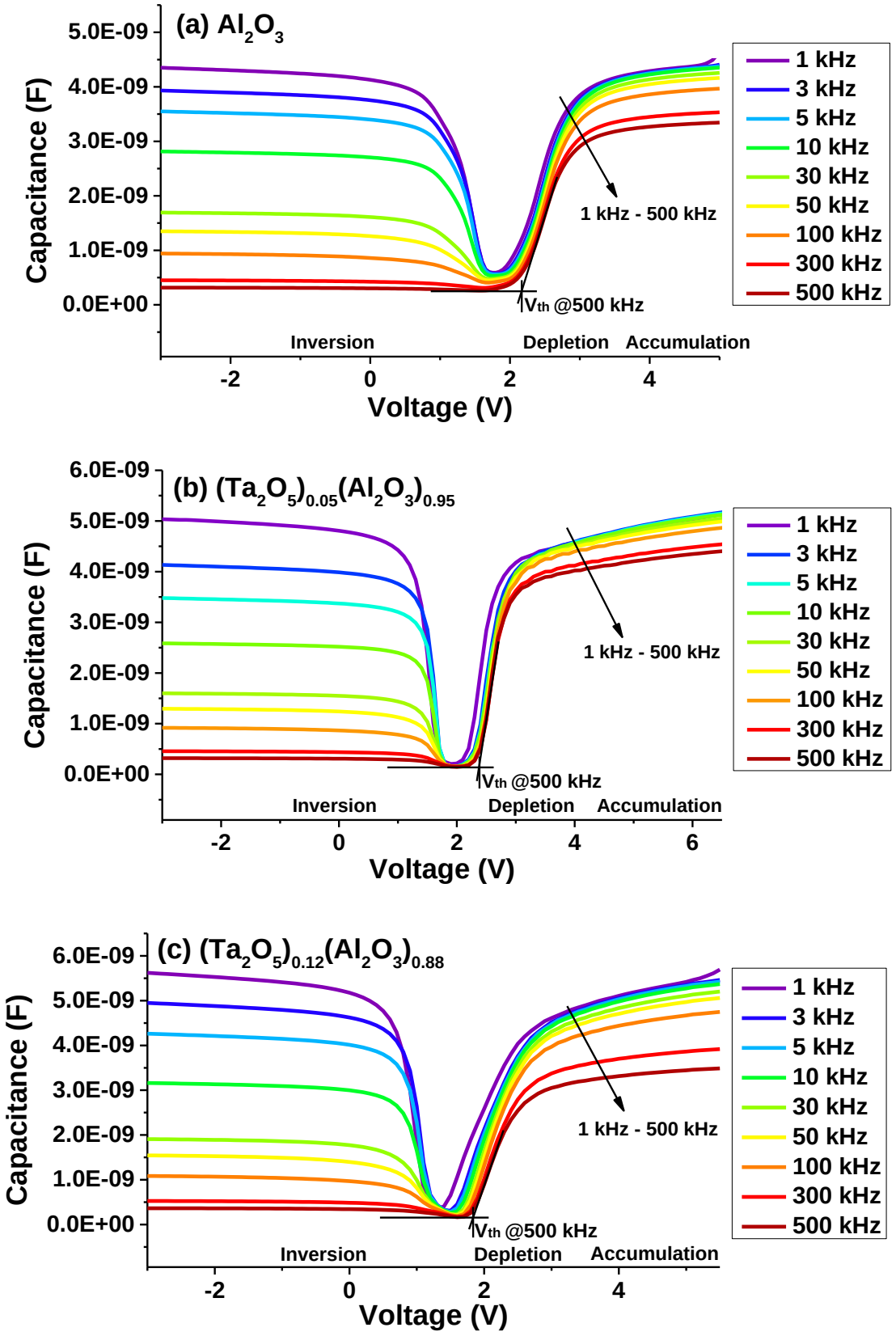

FIG. 5.4: CV measurements at frequencies ranging from 1 kHz to 500 kHz for the ~ 1 mm diameter Si(100) MOS capacitors fabricated with ~ 10 nm thick (a) Al_2O_3, (b) $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ and (c) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate oxides.

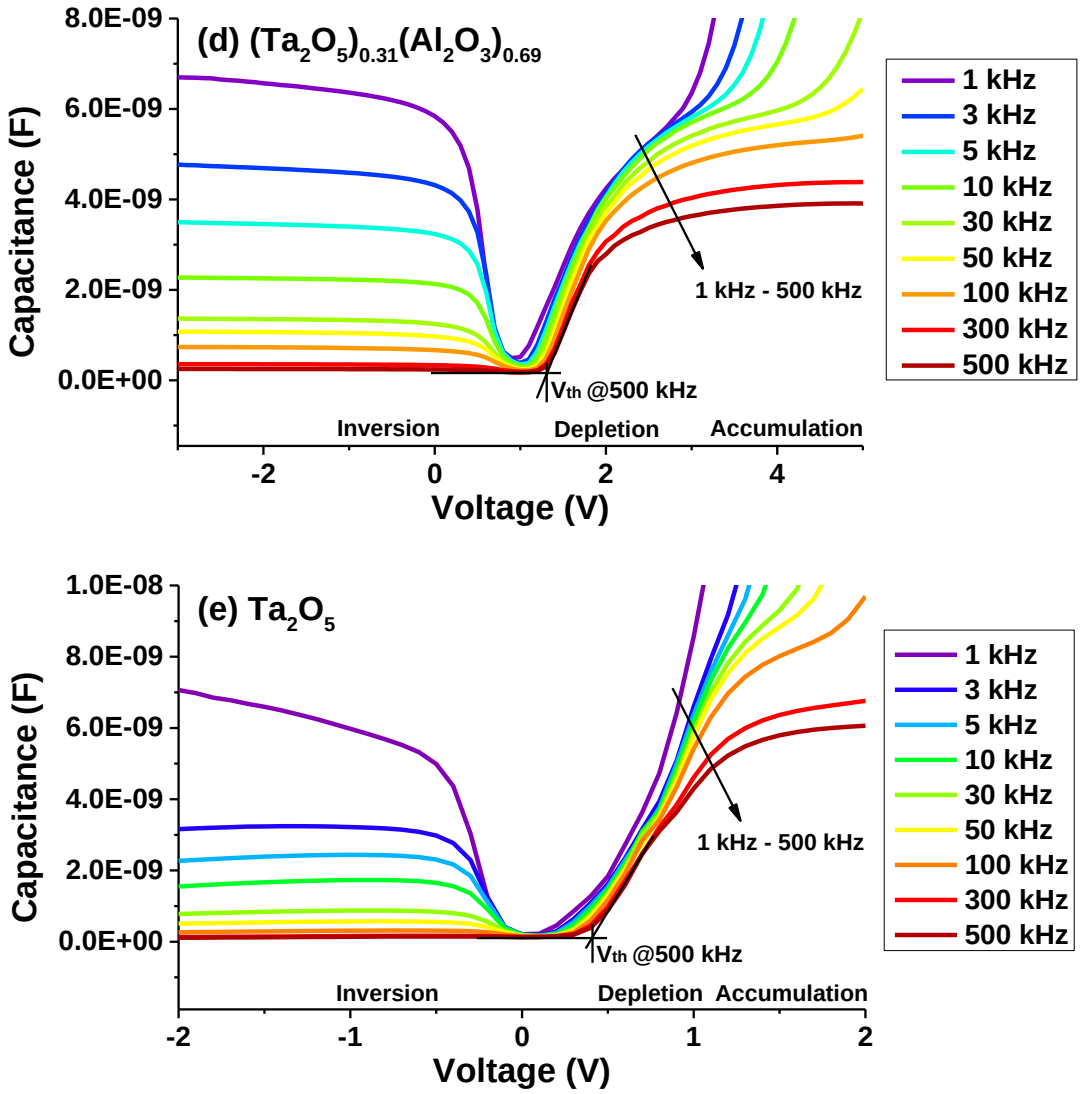

FIG. 5.4 (cont.): CV measurements at frequencies ranging from 1 kHz to 500 kHz for the ~ 1 mm diameter Si(100) MOS capacitors fabricated with ~ 10 nm thick (d) $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ and (e) Ta_2O_5 gate oxides.

Figures 5.4a-e show the CV characteristics at room temperature of the 1 mm diameter Au/$(Ta_2O_5)_x(Al_2O_3)_{1-x}$/Si(100) capacitors in the frequency range of 1 kHz to 500 kHz. As the MOS Si substrates are n-type, the inversion region of the CV curves occurs at voltages below the threshold voltage and the accumulation region is observed when positive voltages are applied. The inversion charge of the samples is frequency dependent. It reaches its maximum at low frequencies, when the capacitor is in thermal equilibrium and there is sufficient time for the inversion layer carrier concentration to respond to any changes in the

applied gate voltage, and decreases at high frequencies, when the inversion layer cannot build up fast enough and the capacitance is reduced. The maximum capacitance in the accumulation region also shows a reduction with frequency for all the samples. This frequency dispersion associated with the frequency dependence of the κ value is often observed in CV measurements for high-κ materials.[24] This is an indicator of the presence of interface states at the semiconductor/oxide interface.[25] The oxide film capacitance can be extracted from the CV curves when the MOS capacitance is in accumulation. It should be noted that, for the $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ and Ta_2O_5 samples with higher Ta content (Figs. 5.4d-e), the CV curves show a non-ideal behaviour at low frequencies in accumulation and thus the oxide capacitance cannot be effectively measured for these frequencies. This is attributed to high leakage current, where electrons from the n-type silicon conduction band tunnel through the oxide into the gate electrode.[26] The higher leakage current through the gate oxide with the increase of the Ta_2O_5 mole fraction could be a result of the lower barrier height of Ta_2O_5 on Si (measured to be 0.77 eV)[27] compared to the barrier height of Al_2O_3 on Si (3.5 eV).[28]

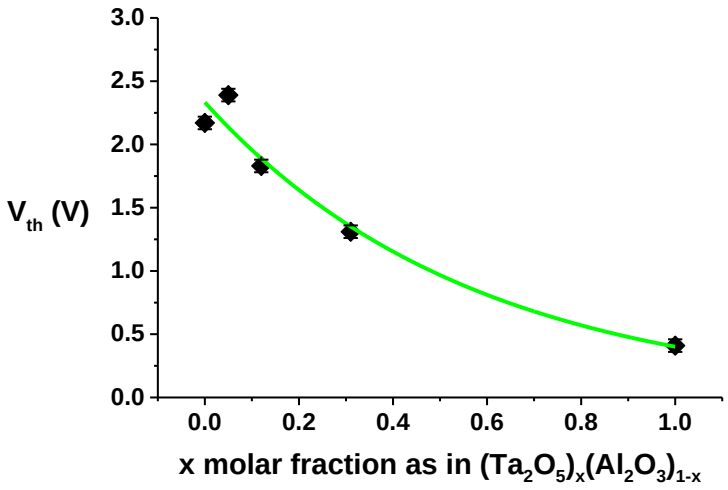

FIG. 5.5: V_{th} values calculated for the ~ 1 mm diameter Si(100) MOS capacitors fabricated with ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ gate oxides, as a function of the Ta_2O_5 *x* molar fraction at frequency of 500 kHz.

Figure 5.5 shows the threshold voltage values calculated for the Au/$(Ta_2O_5)_x(Al_2O_3)_{1-x}$/Si capacitors as a function of the oxides *x* molar fraction at 500 kHz. The threshold voltage is determined for each CV curve by linearly extrapolating the CV profile around the inflection point to zero capacitance (Fig. 5.4).[26] The errors shown are estimated from fitting errors after applying a 95% C.I. to the linear fit. The threshold voltage of the samples shows a reduction with the increase of the Ta_2O_5 mole fraction (Fig. 5.5). The threshold voltage shift towards negative values can be caused by an increase in the number of positive oxide fixed charges or a reduction in the number of negative oxide fixed charges, which is unwanted for power electronics due to fact that the gate oxide negative charge in GaN-based MOS-HEMTs can enhance the shift of threshold voltage towards positive voltages for the realisation of normally-OFF transistors.[30] It has been reported that Al_2O_3 shows negative fixed oxide charge when in contact with Si, AlGaN and GaN.[30-32] Therefore, the results indicate that there is a reduction of the Al_2O_3 negative charge with the introduction of Ta, which could be an issue when using $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ gate dielectrics with high Ta_2O_5 concentration for GaN-based power devices.

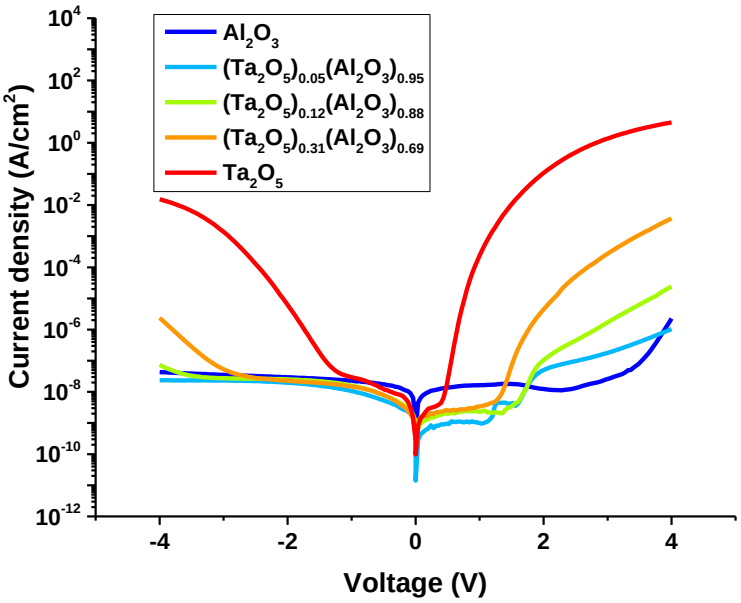

FIG. 5.6: IV measurements carried out for the ~ 300 µm diameter Si(100) MOS capacitors fabricated with ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ gate oxides.

Figure 5.6 shows the IV characteristics (in log-linear scale) of the 300 µm diameter Au/$(Ta_2O_5)_x(Al_2O_3)_{1-x}$/Si MOS capacitors. When a positive bias voltage is applied, the results show an increase in the leakage current density of several orders of magnitude for Ta_2O_5 with respect Al_2O_3. For negative applied voltage, a rapid increase in the current of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$, $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ and Ta_2O_5 samples is observed from about – 3.3 eV – 2.5 eV and – 1.1 eV, respectively, whereas for the $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ and Al_2O_3 samples this current increase is not observed for the range of voltages measured. As previously mentioned, this increase in the leakage current with the Ta_2O_5 molar fraction can be attributed to the decrease of the oxide barrier height on Si due to the smaller bandgap of Ta_2O_5, causing the observed change in the CV curves from near-ideal behaviour to a regime where the CV behaviour is highly non-ideal (Fig. 5.4). As the barrier height of Ta_2O_5 on GaN is < 1 eV,[33] the use of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ gate dielectrics with high Ta_2O_5 concentration for GaN-based devices could result in high gate leakage currents. This low barrier height issue could be mitigated by introducing an Al_2O_3 interlayer in a bi-layer $Al_2O_3/(Ta_2O_5)_x(Al_2O_3)_{1-x}$ or a 'sandwich' $Al_2O_3/(Ta_2O_5)_x(Al_2O_3)_{1-x}/Al_2O_3$ structure. Reports on HfO_2/Al_2O_3, TiO_2/Al_2O_3 and AlO_xN_y/Al_2O_3 gate insulators on GaN have shown that the use of the bi-layers stacks with Al_2O_3 as an interfacial layer improves the oxide/GaN interface as well as the electrical properties of the GaN MOS devices compared to the singe-layer gate insulators.[4, 34, 35] An $Al_2O_3/TiO_2/Al_2O_3$ stack has also been investigated showing improved IV and CV characteristics while maintaining low leakage current.[36] Alternatively, a graded layer (i.e. Al_2O_3 to $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ with increasing Ta_2O_5 molar fraction with increasing distance from the GaN interface) could also be used due to the composition control demonstrated with ALD in the previous chapter.

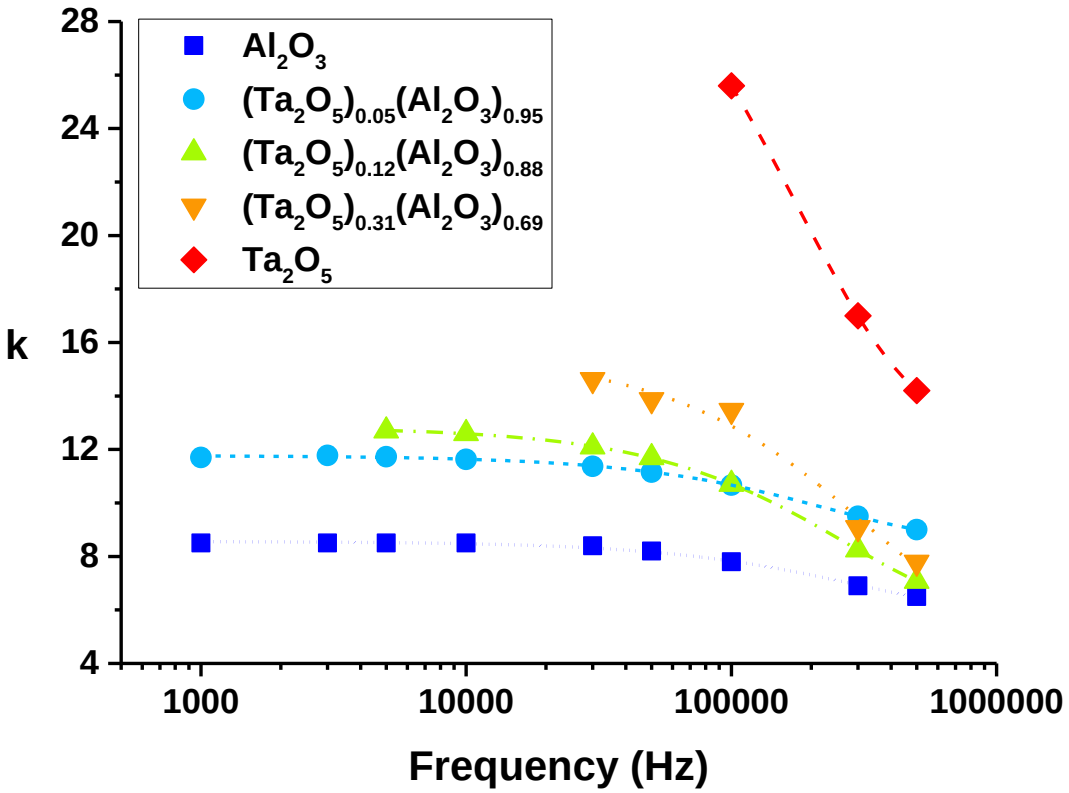

FIG. 5.7: Dielectric constant values calculated for the ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films grown on Si(100) at frequencies ranging from 1 kHz to 500 kHz.

Figure 5.7 shows the κ values obtained as a function of frequency for the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples. It can be observed that the dielectric constant of the oxide films decreases with frequency, which is attributed to the reduction of the interfacial, ionic and dipolar polarisation contributions to the dielectric constant with increasing frequency. This is due to the fact that the dipole moment can follow the changes in the electric field easily at low frequencies whereas at higher frequencies the interfacial dipoles have less time to orient themselves in the direction of the field.[37-39] At low frequencies, the dielectric constant value increases with the Ta_2O_5 molar fraction for all the samples. At high frequencies, the Al_2O_3 sample and the $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ sample with the lowest Ta_2O_5 molar fraction show a smaller variation of the dielectric constant with frequency. This behaviour is comparable to the frequency dispersion reported for Al_2O_3.[39] On the other hand, the Ta_2O_5

and $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples with a higher Ta content show bigger changes in the dielectric constant value with frequency. These variations of dielectric constant due to structural differences in the doped oxide films have been reported in literature.[40, 41] These structural differences are expected to be caused by the addition of Ta dopant to amorphous alumina, which can have an effect on the oxide local structure (i.e. Al coordination number, the distribution of bond distances and angles, etc.).[42] Therefore, if the dopant concentration affects the structural properties of the material, this will affect the magnitude of polarisation achievable by the oxide and ultimately will determine the oxide dielectric properties, and hence the dielectric constant.

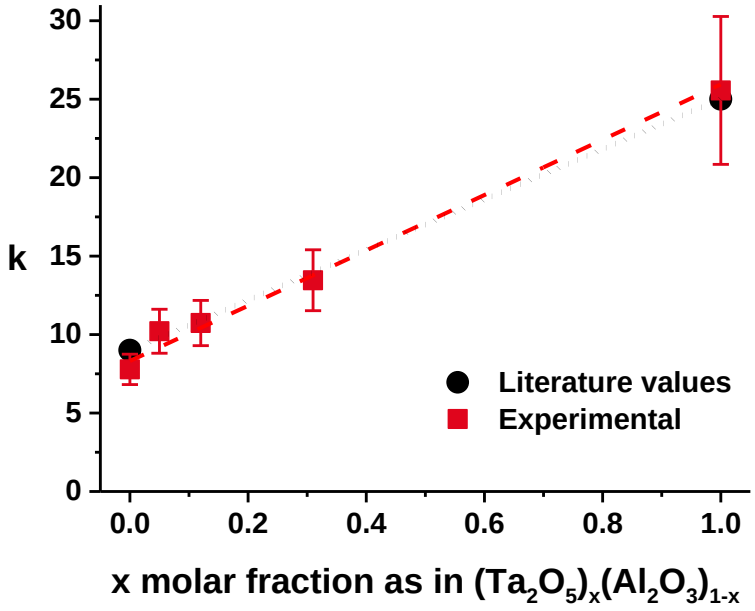

FIG. 5.8: Dielectric constant values calculated as a function of the Ta_2O_5 molar fraction, *x*, for the ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films grown on Si(100) at frequency of 100 kHz.

Figure 5.8 shows the κ value calculated for the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films at 100 kHz as a function of the *x* molar fraction. The results show that the dielectric constant increases linearly with the Ta_2O_5 molar fraction. The calculated dielectric constant values determined for the $x = 0$ and $x = 1$ samples are 7.8 and 25.6, respectively, which are close to the

literature values of ~ 9 and ~ 25 known for Al_2O_3 and Ta_2O_5, respectively.[3, 4] The results suggest a significant increase in the dielectric constant of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers with the introduction of Ta, which is very important for their application as gate dielectrics in power devices.

5.4. Band alignment of ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films on GaN-on-Si(111)

The band alignment at the interface between the ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 \leq x \leq 1$) films and GaN-on-Si was studied as a function of the *x* molar fraction before and after RTA at 600 ºC for 60 s in N_2. Interface samples were grown using an overall number of ALD cycles n = 30 to deposit ~ 2.5 nm thick films on the GaN-on-Si substrate. The valence band offset of the oxide films grown on the GaN-on-Si substrate was determined by XPS using the method proposed by Grant[43] and Kraut *et al.*[44]

$$\Delta E_V = (E_{CL,GaN} - E_{V,GaN}) - (E_{CL,oxide} - E_{V,oxide}) + \Delta E_{CL} \quad (5.4)$$

where E_{CL} represents the binding energy of the core levels (CL) and E_V is the binding energy of the valence band maximum (VBM). $E_{CL,GaN}$ and $E_{V,GaN}$ are the CL and the VBM binding energies of the GaN-on-Si substrate, $E_{CL,oxide}$ and $E_{V,oxide}$ are the CL and the VBM binding energies of the bulk oxide film, and ΔE_{CL} is the difference between the CL binding energies of the GaN-on-Si substrate and the oxide in the oxide/GaN-on-Si interface. In this analysis, the XPS binding energy of the Ga-N bond is used as the core level of bulk GaN-on-Si substrate, the Al 2p binding energy is used as the core level of bulk Al_2O_3 and $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 < x < 1$) oxides and the Ta 4f binding energy is used as the core level of bulk Ta_2O_5.

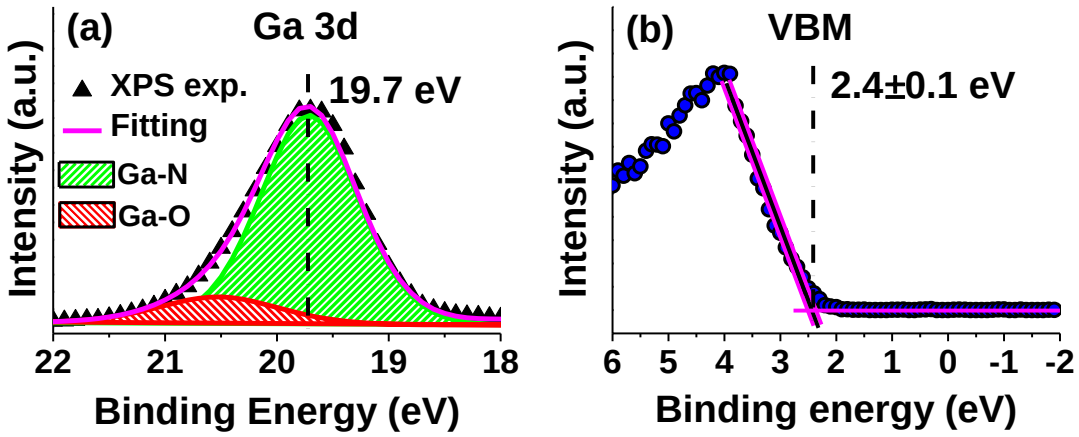

FIG.5.9: XPS spectra of (a) Ga 3d core level and (b) VBM obtained for the uncoated GaN-on-Si(111) substrate. The core level of the GaN peak and the VBM are indicated with dot dashed lines.

The difference between the binding energy of the Ga-N bond and the VBM in the GaN-on-Si substrate, $E_{CL,GaN} - E_{V,GaN}$, is investigated from the Ga 3d and VBM spectra obtained for the uncoated substrate as shown in Figure 5.9. The Ga 3d core level XPS spectrum has been deconvoluted into two components corresponding to Ga-N and Ga-O bonds (Fig. 5.9a). The Ga-O component can be attributed to oxidation of the GaN surface when the epilayers are exposed to air due to the vacuum break following MOCVD.[45] The VBM is determined by extrapolating the linear fit with 95% C.I. applied to the leading edge of the valence band spectrum and calculating its intersection with the base line (Fig. 5.8b).[46] The binding energy difference between the Ga-N bond and the VBM in the GaN-on-Si substrate is 17.3 eV. This value is smaller than the values obtained from the electronic-state studies of bulk GaN, where the Ga 3d core level is found to be 17.7-17.8 eV below the VBM.[47, 48] This reduction is attributed to the presence of growth induced in-plane stress in the GaN epilayers due to the difference in lattice parameters and thermal expansion coefficients between the GaN and the underlying Si(111) substrate.[49] This stress can have a significant influence on the electronic band structure leading to a variation in the VBM.[50]

The difference between the binding energy of the core level and the VBM in the oxide layers, $E_{CL,oxide} - E_{V,oxide}$, is investigated from the spectra of the ~ 10 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ $(0 \leq x \leq 1)$ layers used for composition and bandgap studies in sections 4.4 and 5.2, respectively. For the Al_2O_3 and $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ $(0 < x < 1)$ samples the $E_{CL,oxide} - E_{V,oxide}$ value is investigated from the Al 2p and VBM spectra, whereas for the Ta_2O_5 samples the $E_{CL,oxide} - E_{V,oxide}$ value is investigated from the Ta 4f and VBM spectra. The respective Al 2p and Ta 4f spectra used in this section are the same as used in the previous chapter for the analysis of the composition of the oxide films (section 4.4). The VBM spectra of the as-deposited and annealed samples are shown in Figure 5.10.

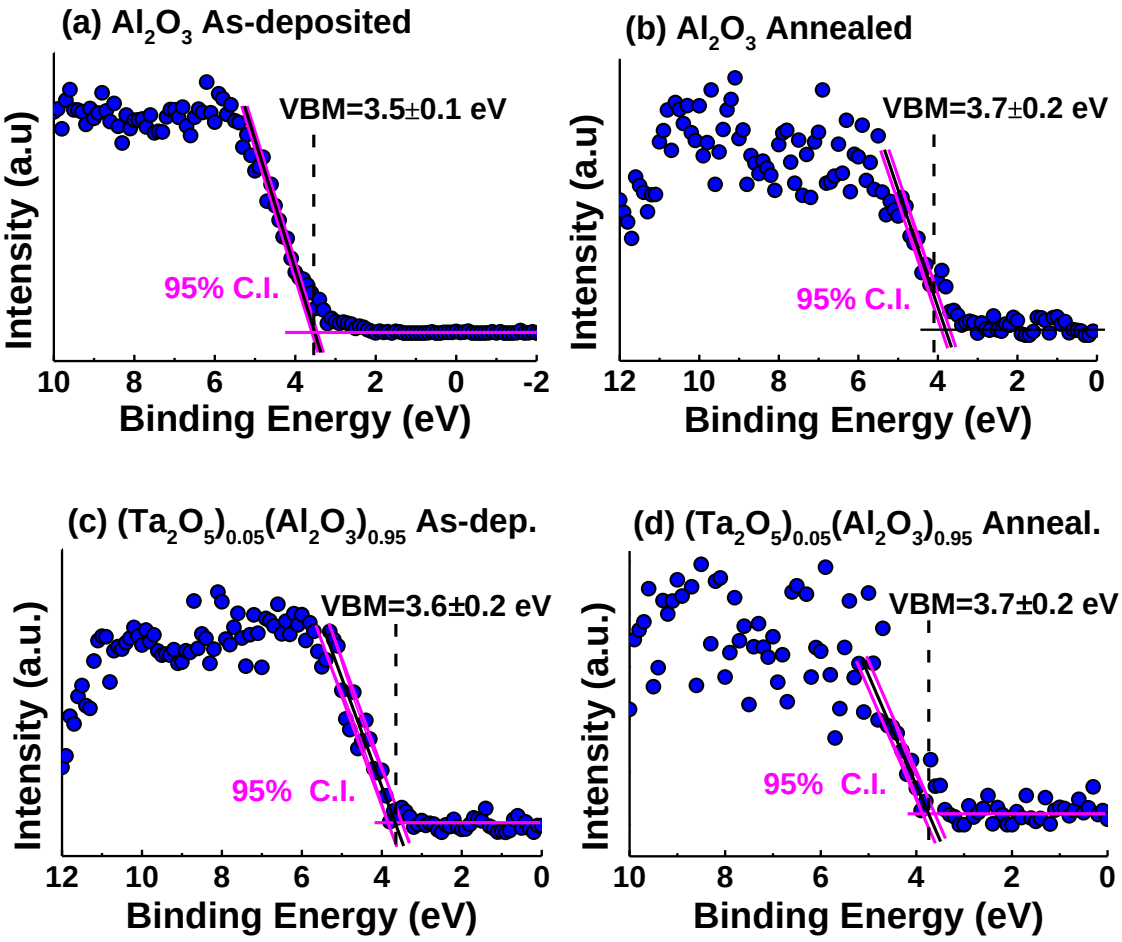

FIG. 5.10: XPS spectra of VBM obtained for the ~ 10 nm thick ALD: (a) Al_2O_3 as-deposited, (b) Al_2O_3 annealed, (c) $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ as-deposited and (d) $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ annealed samples.

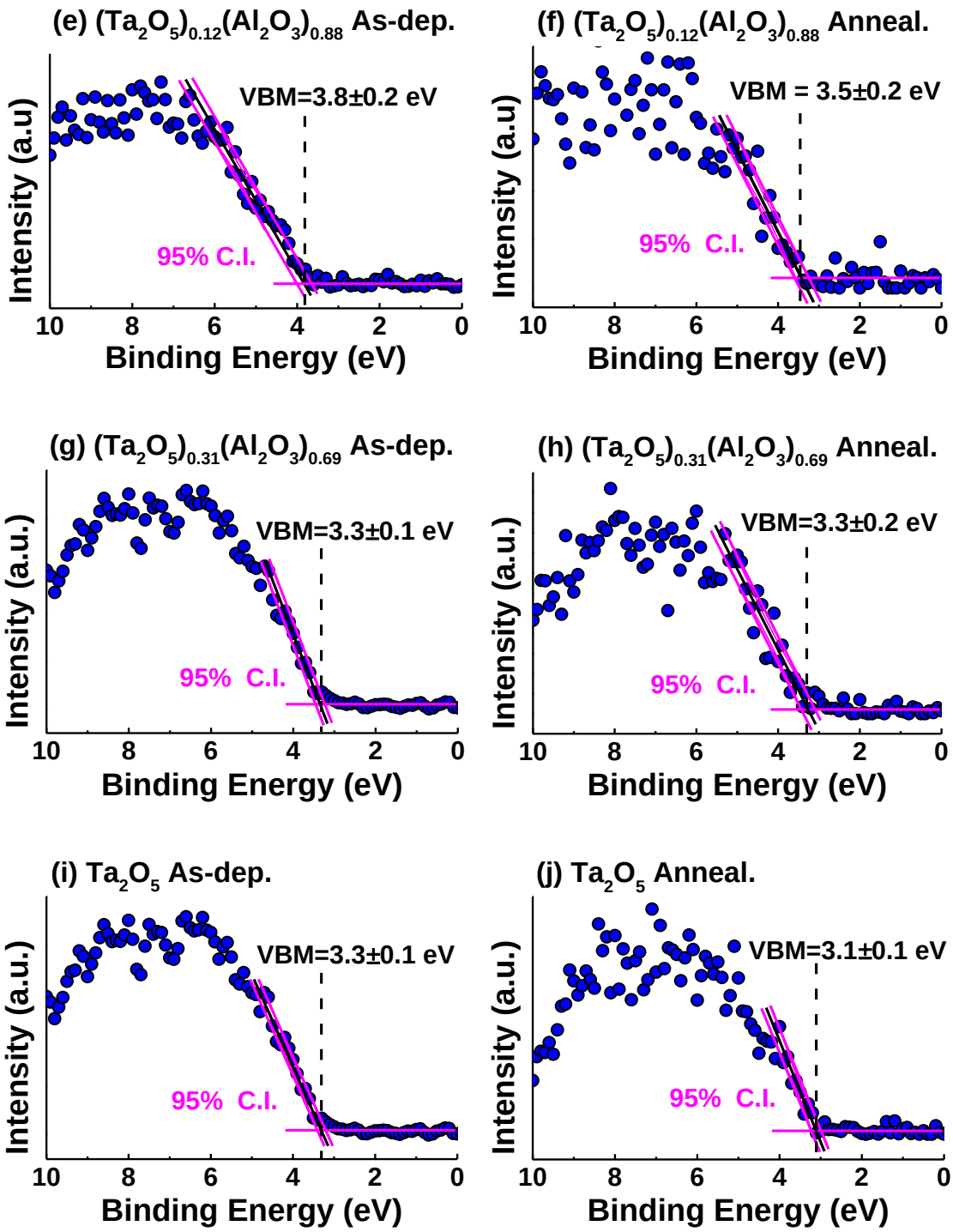

FIG. 5.10 (cont.): XPS spectra of VBM obtained for the ~ 10 nm thick ALD: (e) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as-deposited, (f) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ annealed, (g) $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ as-deposited, (h) $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ annealed, (i) Ta_2O_5 as-deposited and (j) Ta_2O_5 annealed samples.

The $E_{CL,oxide} - E_{V,oxide}$ values determined for the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 \leq x \leq 1$) layers before and after annealing in N_2 at 600 ºC for 60 s are summarised in Tables 5.1a and 5.1b. For the Al_2O_3 sample the binding energy of the Al 2p core level is found to be 71.0 eV below the VBM. This value is within the range of values of 70.4 eV to 71.8 eV reported in other studies for bulk Al_2O_3.[1, 51, 52] The value obtained for the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples varies from 71.0 eV to 71.2 eV with the increase of the Ta_2O_5 molar fraction, showing that the addition of Ta has little effect on the difference between the core levels of Al 2p and VBM. For the Ta_2O_5 sample the binding energy of the Ta 4f core level is 23.2 eV below the VBM. This value is close to the value of 23.4 eV reported in literature for sputtered Ta_2O_5.[50] After annealing the $(E_{CL} - E_V)_{oxide}$ value does not vary significantly for any of the samples. This is in agreement with Poisson's equation, which states that band bending is caused by the spatially varying electrostatic potential which bends all of the bands or energy levels by an amount that depends only on the distance from the interface.[53] As a result, the $(E_{CL} - E_V)$ values should be independent of band bending because the VBM and CL bands are affected equally and thus, the only parameter that is influenced by band bending and polarisation effect is ΔE_{CL}.

TABLE 5.1a. Summary of the Al 2p core level, VBM and $(E_{CL} - E_V)_{oxide}$ values for the ~ 10 nm $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 \leq x < 1$) 'bulk' samples before and after annealing in N_2 at 600 ºC for 60 s.

Sample	Al 2p (eV)	VBM (eV)	$(E_{CL}\text{-}E_V)_{oxide}$ (eV)
Al_2O_3 as-deposited	74.5	3.5	71.0
Al_2O_3 annealed	74.7	3.7	71.0
$(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ as-deposited	74.6	3.6	71.0
$(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ annealed	74.6	3.7	70.9
$(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as-deposited	74.9	3.8	71.1
$(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ annealed	74.6	3.5	71.1
$(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ as-deposited	74.5	3.3	71.2
$(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ annealed	74.4	3.3	71.1

TABLE 5.1b. Summary of the Ta 4f core level, VBM and $(E_{CL} - E_V)_{oxide}$ values for the ~ 10 nm Ta_2O_5 'bulk' samples before and after annealing in N_2 at 600 ºC for 60 s.

Sample	Ta 4f (eV)	VBM (eV)	$(E_{CL}-E_V)_{oxide}$ (eV)
Ta_2O_5 as-deposited	26.5	3.3	23.2
Ta_2O_5 annealed	26.4	3.1	23.3

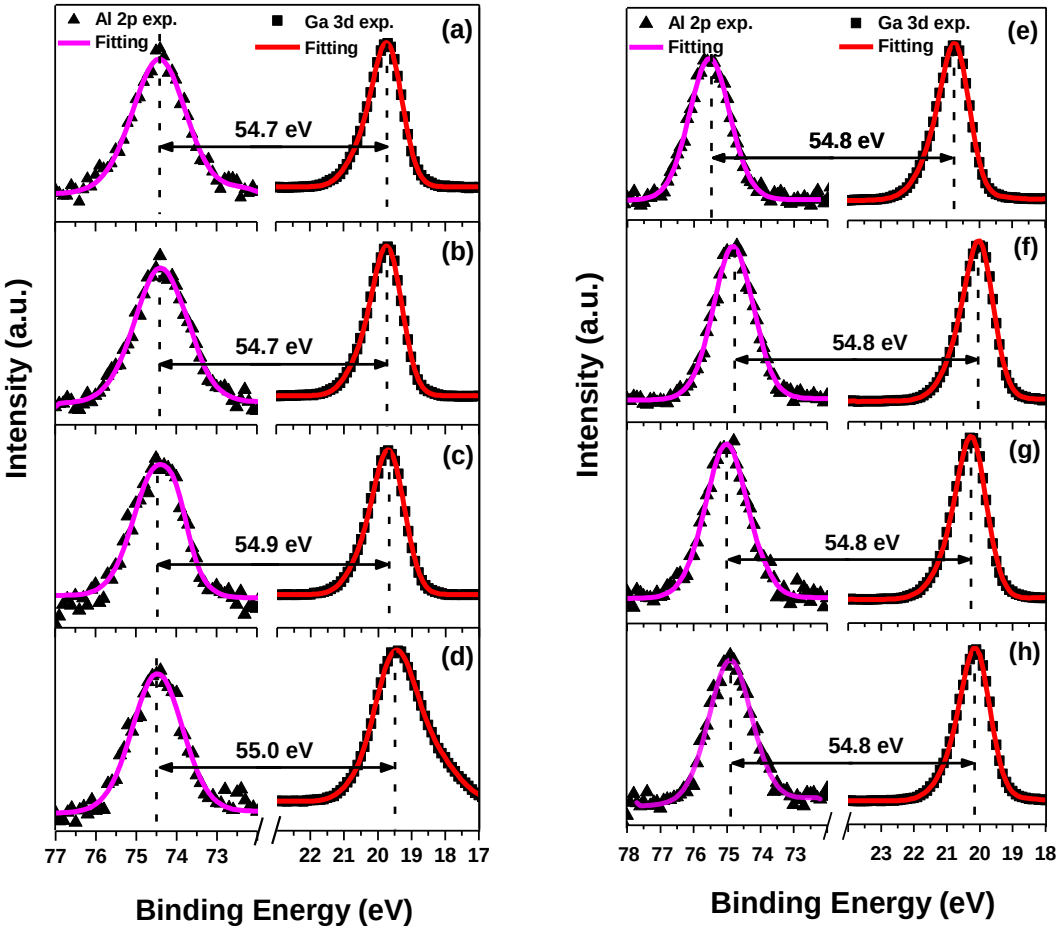

FIG. 5.11: XPS Al 2p and Ga 3d spectra of as-deposited: (a) ~ 2.5 nm Al_2O_3/GaN, (b) ~ 2.5 nm $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$/GaN, (c) ~ 2.5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN, and (d) ~ 2.5 nm $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$/GaN; and annealed (e) ~ 2.5 nm Al_2O_3/GaN, (f) ~ 2.5 nm $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$/GaN, (g) ~ 2.5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN, and (h) ~ 2.5 nm $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$/GaN. The values of the core level of the peaks are indicated with dash lines.

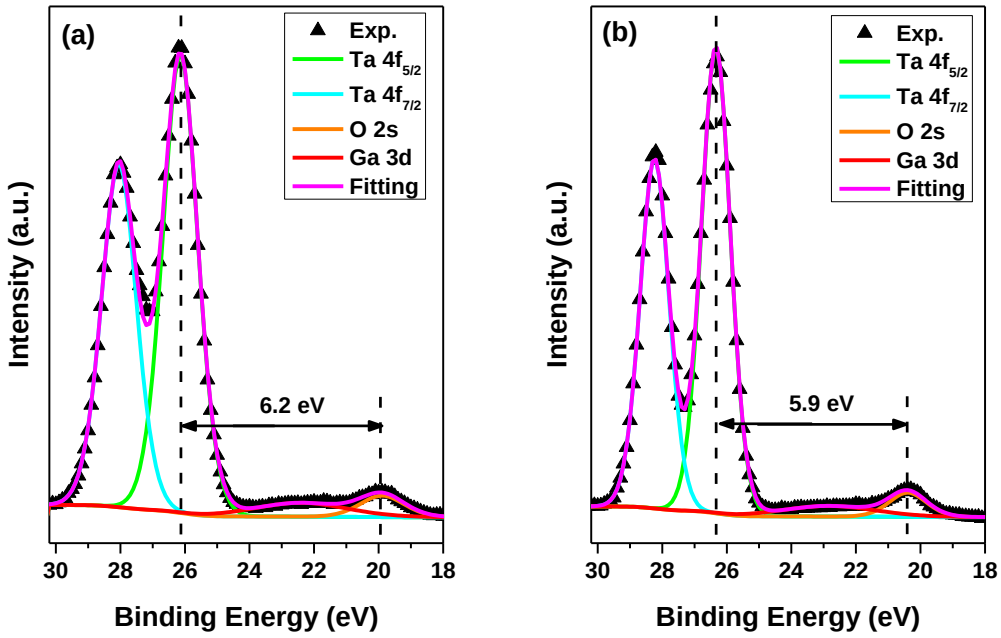

FIG. 5.12: XPS Ta 4f and Ga 3d spectra of (a) as-deposited ~ 2.5 nm Ta_2O_5/GaN and (b) annealed ~ 2.5 nm Ta_2O_5/GaN. The values of the core level of the peaks are indicated with dash lines.

The difference between the binding energies of the core levels at the interface, ΔE_{CL}, is obtained for the ~ 2.5 nm thick $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films grown on the GaN-on-Si substrate. For the Al_2O_3 and $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 < x < 1$) layers on GaN-on-Si, the value of ΔE_{CL} is calculated from the Al 2p and Ga 3d core level spectra obtained for the as-deposited and annealed samples (Fig 5.11). For the Ta_2O_5 layers on GaN-on-Si, ΔE_{CL} is calculated from the Ta 4f and Ga 3d core level spectra of the as-deposited and annealed samples (Fig 5.12). The ΔE_{CL} value obtained for the interface samples before and after annealing in N_2 at 600 ºC for 60 s are summarised in Tables 5.2a and 5.2b. The results indicate that the band bending is altered during post-deposition annealing. The Al 2p, Ta 4f and Ga 3d core levels shift to higher BEs after annealing in N_2 at 600 ºC for 60 s. As a consequence, the ΔE_{CL} values at the interface vary, which demonstrates that the annealing process can change significantly the band bending conditions at the oxide/GaN interface. Polarisation in Wurtzite Ga-face GaN produces a negative surface charge that is partially compensated by positive ionised donors, leading to band bending at the surface.[54] Experimental upward band bending

between 0.3 and 1.5 eV has been reported for Ga-face GaN.[55-57] In order to achieve this experimental band bending the surface needs to be compensated with ionised donors such as structural defects, Ga termination, oxidation of the surface, surface states or adsorbates causing Fermi level pinning or additional charge compensation.[58] Annealing can change the screening of the polarisation surface bound charge and alter the band bending conditions at the oxide/GaN interfaces,[1] causing variations in the ΔE_{CL} values, which is in agreement with the results obtained in this study.

TABLE 5.2a. Summary of the Al 2p core level, Ga 3d core level and $(E_{CL} - E_V)_{oxide}$ value for the ~ 2.5 nm $(Ta_2O_5)_x(Al_2O_3)_{1-x}$/GaN ($0 \leq x < 1$) 'interface' samples before and after annealing in N_2 at 600 ºC for 60 s.

As-deposited	Al 2p (eV)	Ga 3d (eV)	ΔE_{CL} (eV)	Annealed	Al 2p (eV)	Ga 3d (eV)	ΔE_{CL} (eV)
Al_2O_3	74.4	19.7	54.7	Al_2O_3	75.5	20.7	54.8
$(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$	74.4	19.7	54.7	$(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$	74.8	20.0	54.8
$(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$	74.5	19.6	54.9	$(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$	75.0	20.2	54.8
$(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$	74.5	19.5	55.0	$(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$	74.9	20.1	54.8

TABLE 5.2b. Summary of the Ta 4f core level, Ga 3d core level and $(E_{CL} - E_V)_{oxide}$ value for the ~ 2.5 nm Ta_2O_5/GaN ($0 \leq x < 1$) 'interface' samples before and after annealing in N_2 at 600 ºC for 60 s.

As-deposited	Ta 4f (eV)	Ga 3d (eV)	ΔE_{CL} (eV)	Annealed	Ta 4f (eV)	Ga 3d (eV)	ΔE_{CL} (eV)
Ta_2O_5	26.1	19.9	6.2	Ta_2O_5	26.3	20.4	5.9

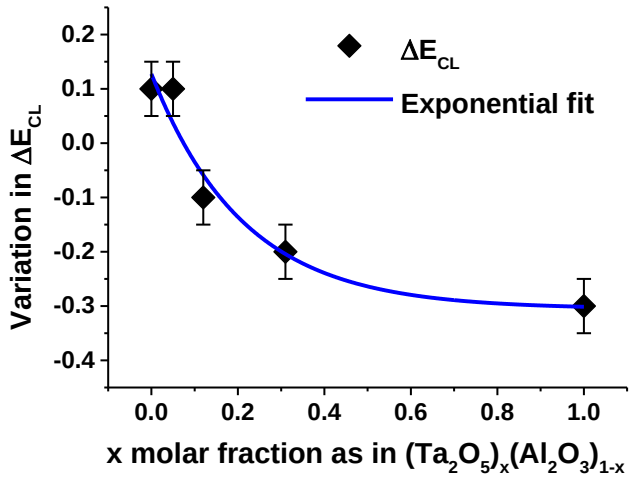

FIG. 5.13: Variation in ΔE_{CL} value calculated for the ~ 2.5 nm thick ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$/GaN-on-Si interface samples after annealing in N_2 at 600ºC for 60s, as a function of the Ta_2O_5 *x* molar fraction.

Figure 5.13 shows the variation in the ΔE_{CL} value for the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ samples as a function of the x molar fraction. The errors shown correspond to the energy resolution of the XPS spectrometer (0.05 eV). This variation in the difference between the E_{CL} of the oxide films and the GaN-on-Si substrate at the interface changes exponentially with the Ta_2O_5 content. The ΔE_{CL} increases by 0.1 eV for both the Al_2O_3 and $(Ta_2O_5)_{0.05}(Al_2O_3)_{0.95}$ samples and decreases by 0.1 eV and 0.2 eV for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ and $(Ta_2O_5)_{0.31}(Al_2O_3)_{0.69}$ samples, respectively. Finally, the ΔE_{CL} decreases by 0.3 eV for the Ta_2O_5 sample. According to equation 5.4, since the value of the terms $(E_{CL} - E_V)_{GaN}$ and $(E_{CL} - E_V)_{oxide}$ remains constant after the annealing process, a variation of the ΔE_{CL} value implies a change in the VBO at the interface. Therefore, the results indicate that the band alignment between the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers and GaN changes differently after annealing depending on the oxide film composition. This can be explained by the fact that, as previously mentioned, annealing can change the interface charges and alter the electric field in the oxide and the band bending at the oxide/GaN interface. Since the properties of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films vary with the x molar fraction, it is expected that the changes in band bending after annealing will depend on the oxide film composition and its interface with GaN.

According to equation 5.4, the VBO value obtained for as-deposited Al_2O_3 on GaN-on-Si is 1.0 eV. This value is significantly smaller than the experimental value of 1.8 eV reported by other authors for Al_2O_3 on GaN,[1] which is similar to the theoretical value of 1.7 eV calculated from the electron affinity model[59] and the charge neutrality level (CNL) model when the Al_2O_3 and GaN CNLs are calculated by local density approximation (LDA).[52] However, smaller experimental values of 0.7 eV and 0.9 eV have also been reported for Al_2O_3 on GaN,[51] which are closer to the value obtained in this study. The differences in the experimental values reported in literature are attributed to the processing

methods utilised in each case such as cleaning and deposition technique, which can result in variations in oxygen coverage, dielectric stoichiometry and interfacial bonding, affecting the band offsets significantly.[60] The VBO value obtained for the as-deposited Ta_2O_5 sample is 0.3 eV, which implies a reduction of 0.7 eV with respect the VBO of the Al_2O_3 sample. This reduction is expected considering the smaller theoretical VBO value of 1.1 eV calculated for Ta_2O_5 on GaN using the LDA and CNL model.[60] After annealing, the VBO value obtained for Al_2O_3 increases by 0.1 eV to 1.1 eV, whereas the VBO of Ta_2O_5 decreases by 0.4 eV to – 0.1 eV. The results confirm that the variations in the band offsets between the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films and the GaN-on-Si substrate after annealing processing vary with the oxide film composition. These variations have been attributed to changes in the interface charges and alterations in the oxides electric field and the band bending at the GaN interface after annealing.[1]

The CBOs between the oxide films and the GaN-on-Si substrate can be derived by the following equation:

$$\Delta E_C = E_g - \Delta E_V - 3.4 \text{ (eV)} \quad (5.5)$$

where 3.4 eV is the bandgap of GaN,[61] confirmed experimentally by photoluminescence (PL) spectroscopy as shown in Figure 5.14.

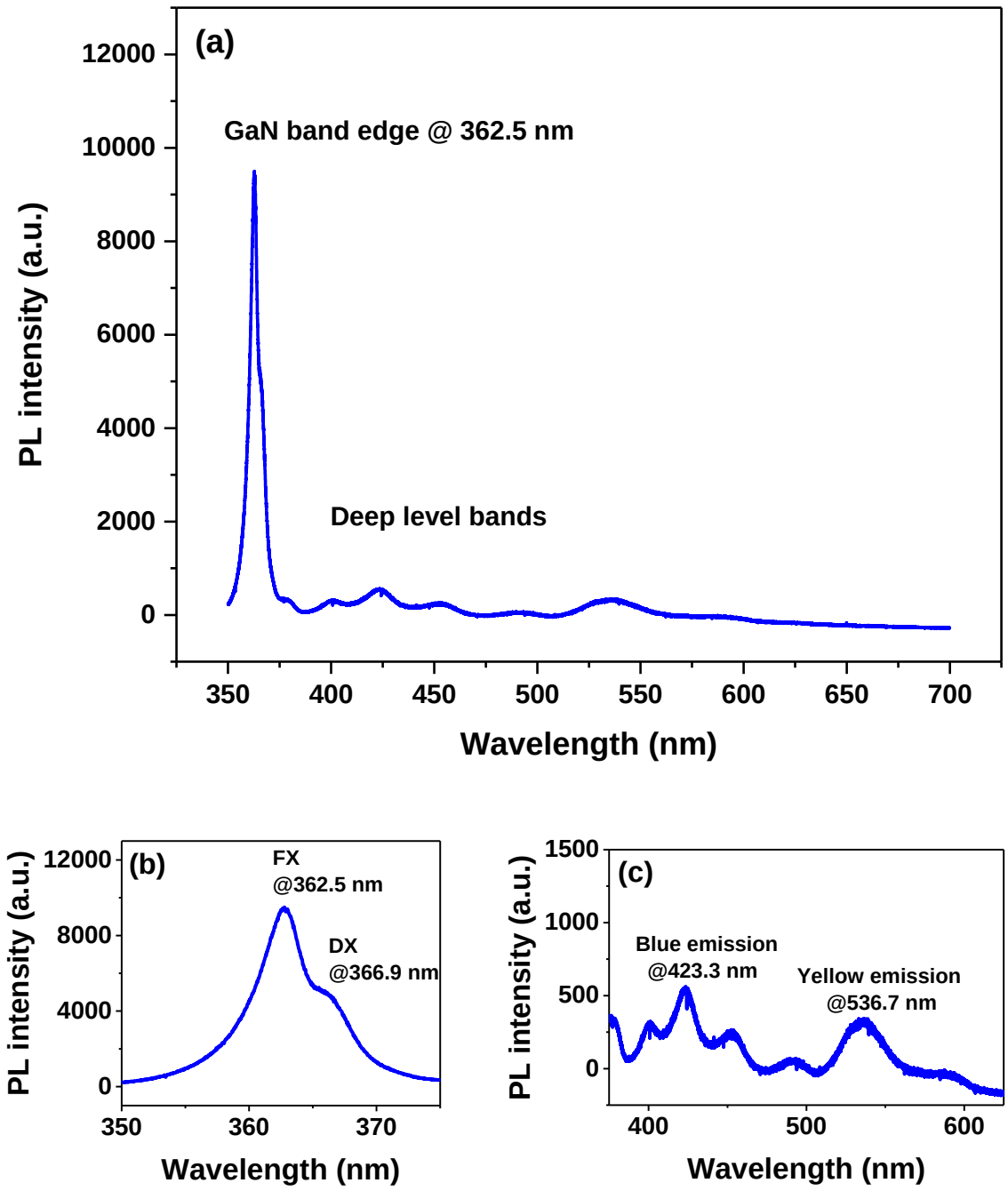

FIG. 5.14: Room temperature ultraviolet 325 nm excitation photoluminescence spectra obtained from the GaN-on-Si(111) substrate (a) for wavelength range between 350 nm and 700 nm, (b) detailed spectrum between 350 nm and 375 nm and (c) detailed spectrum between 375 nm and 625 nm.

Figure 5.14a shows that the room temperature PL spectrum obtained for the GaN substrate is dominated by a large peak at 362.5 nm which corresponds to 3.42 eV as given by the following equation, attributed to the band edge emission of GaN.

$$E = \frac{1239.84}{\lambda} \tag{5.6}$$

where E is the energy in eV and λ is the wavelength in nm.

Figure 5.14b shows the detailed PL spectrum corresponding to the range of wavelengths from 350 nm to 375 nm. The spectrum can be fitted with two peaks, the main peak at 362.5 nm (3.42 eV) is considered to be from free excitons (FX) and the shoulder at 366.9 nm (3.38 eV) is attributed to residual neutral donor-bound excitons (DX) generated from oxygen impurities.[62] The detailed PL spectrum of the small peaks found at higher wavelengths is shown Figure 5.14c. Two optical transitions are observed at 423.36 nm (2.93 eV) and 534.7 nm (2.31 eV), which correspond to blue luminescence (BL) and yellow luminescence (YL) emission bands, respectively.[63] The BL band is believed to be due to a C_{Ga}-C_N deep donor-deep acceptor recombination mechanism,[64] whereas the YL has been found to be related to Ga vacancies in GaN.[65] The very low relative intensity of these defect-related peaks is an indicative of the good quality and high purity of the GaN substrate used in this study.

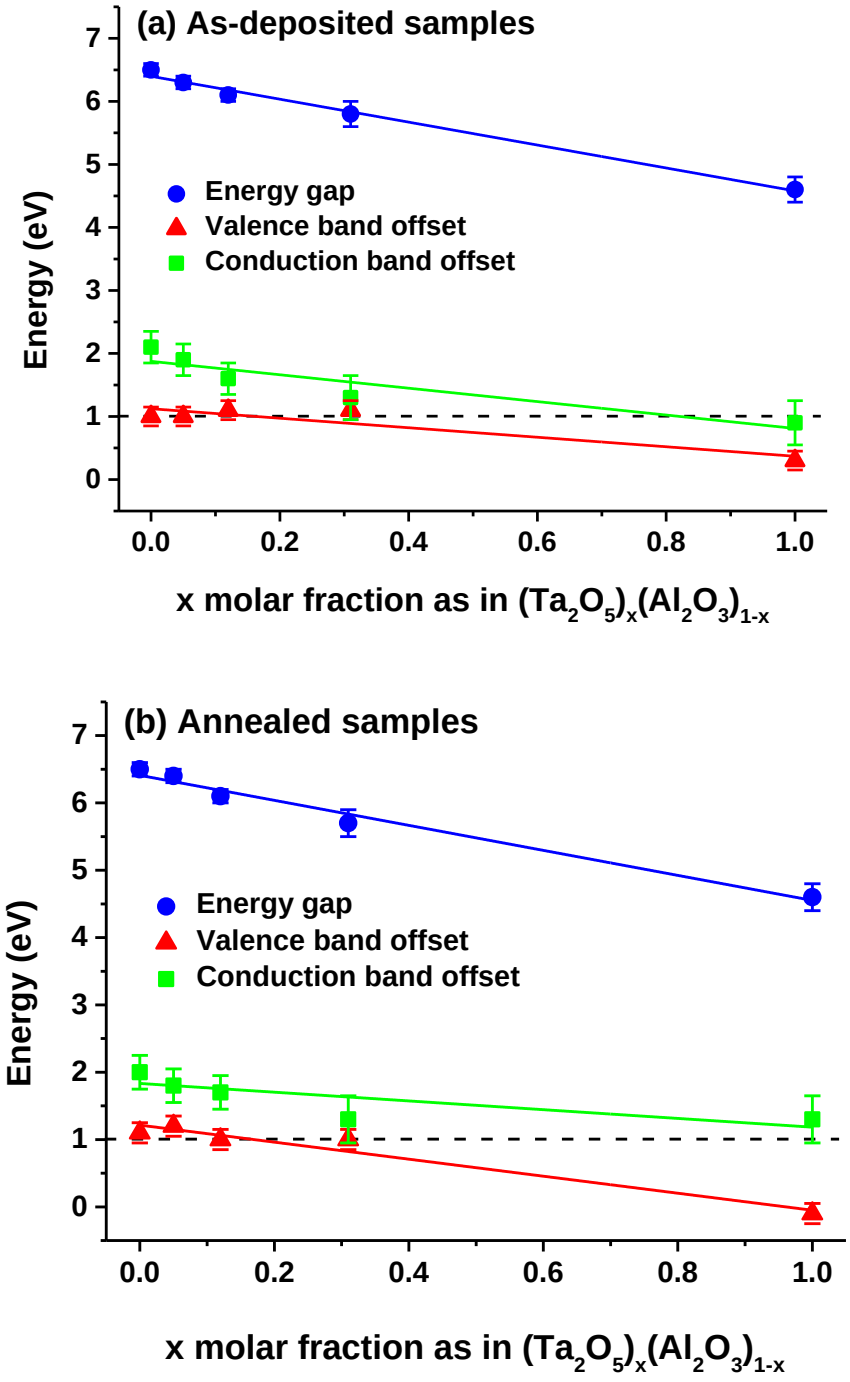

FIG. 5.15: Bandgap, valence band offset and conduction band offset of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers deposited on GaN-on-Si as a function of the molar fraction (x) for the samples (a) as-deposited and (b) annealed. The dashed lines indicate the minimum band offset value of 1 eV required for gate dielectric applications.

Figures 5.15a and 5.15b show the bandgap values determined for the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers as well as their VBOs and CBOs with the GaN-on-Si substrate as a function of the Ta_2O_5 molar fraction, before and after annealing in N_2 at 600 ºC for 60 s respectively. As previously observed for the bandgap of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films in section 5.2, the results show that the VBO and CBO values also decrease linearly with the Ta_2O_5 molar fraction. A linear dependence between the band offsets and the oxides composition has previously been reported in literature for $(HfO_2)_x(Al_2O_3)_{1-x}$ films on Si and $Zn_{1-x}Mg_xO$ on ZnO interfaces.[2, 66] From linear fit, the VBO and CBO of the as-deposited $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films can be derived as a function of the x molar fraction by equations 5.7 and 5.8 below. The results indicate that the reduction of the ΔE_V with the Ta_2O_5 molar fraction is smaller compared to the reduction of ΔE_C. The ΔE_V decreases by ~ 0.7 eV from 1.0 eV for Al_2O_3 to 0.3 eV for Ta_2O_5, whereas the ΔE_C decreases by ~ 1.1 eV from 1.9 eV for Al_2O_3 to 0.8 eV for Ta_2O_5.

$$\Delta E_V = 1.12 - 0.75\,x \tag{5.7}$$

$$\Delta E_C = 1.88 - 1.07\,x \tag{5.8}$$

For the annealed samples, a shift of the band offsets is observed and equations 5.9 and 5.10 are obtained for the VBO and CBO, respectively. Figure 5.15 shows that the VBO and CBO variations increase with the x molar fraction. The results reveal that the VBO of the annealed samples decreases significantly with respect the as-deposited samples for films with a Ta_2O_5 molar fraction $x > 0.4$, whereas the CBO significantly increases for films with a Ta_2O_5 molar fraction $x > 0.3$. As a result, the reduction of the ΔE_V with the Ta_2O_5 molar fraction is bigger compared to the reduction of ΔE_C. The ΔE_V decreases by ~ 1.3 eV from 1.2 eV for Al_2O_3 to – 0.1 eV for Ta_2O_5, whereas the ΔE_C decreases by ~ 0.6 eV from 1.8 eV for Al_2O_3 to 1.2 eV for Ta_2O_5. This demonstrates that the annealing process step alters the

band alignments between the oxides and GaN, with different changes observed depending on the oxide films composition. The characterisation of the band offsets of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers on GaN before and after annealing is very important to understand the effects of post-deposition annealing processing on the oxide films and their interface with the semiconductor, as these changes can affect the use of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers as gate dielectrics for GaN-based devices if the resultant band offsets are < 1 eV. The gate oxide must have a conduction band (for n-type devices) or valence band (for p-type devices) of at least 1 eV to ensure a significant barrier to the semiconductor in order to ensure a sufficiently low leakage current due to Schottky emission of carriers into the band states.[67]

$$\Delta E_V = 1.21 - 1.26\,x \tag{5.9}$$

$$\Delta E_C = 1.83 - 0.65\,x \tag{5.10}$$

5.5. Conclusions

Ta doping has been used to improve the dielectric constant of Al_2O_3 as a gate dielectric for GaN-based HEMT structures. XPS measurements show that the bandgap of the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers decreases linearly with the Ta_2O_5 molar fraction, *x*, from 6.5 eV for pure Al_2O_3 to 4.6 eV for pure Ta_2O_5. The dielectric constant value calculated from CV measurements also varies linearly with the *x* molar fraction, increasing from 7.8 for Al_2O_3 up to 25.6 for Ta_2O_5 at 100 kHz. The band alignment at the interface between the oxide layers and the GaN-on-Si substrate has been analysed using XPS before and after annealing in N_2 at 600 ºC. The band offsets between the $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ films and GaN also show linear variations with the *x* molar fraction. For the as-deposited samples, the VBO decreases from 1.0 eV for Al_2O_3 to 0.3 eV for Ta_2O_5, whereas the CBO decreases from 1.9 eV for Al_2O_3 to 0.8 eV for Ta_2O_5. After annealing, the band offsets shift and the VBO decreases

from 1.2 eV for Al_2O_3 to – 0.1 eV for Ta_2O_5, whereas the CBO decreases from 1.8 eV for Al_2O_3 to 1.2 eV for Ta_2O_5. Therefore, the post-deposition annealing step used during device processing changes the interface characteristics of the samples, which can affect the use of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers as gate dielectrics if the resultant band offsets are < 1 eV. The results demonstrate that ALD with modulation doping can be used to optimally control the properties of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ as gate dielectric by changing the Ta_2O_5 mole fraction, to achieve both a high-κ and a sufficient band offset to GaN for low leakage currents in GaN-based devices.

5.6. References

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6. Effects of Ta doping and annealing on ALD $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ as potential gate dielectric for GaN-based HEMTs

6.1. Introduction

This chapter presents a comparative analysis of the impact of Ta doping and annealing on the interfacial properties of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films deposited by thermal ALD on GaN-capped AlGaN/GaN and InAlN/GaN HEMT structures. These samples were selected based on the band alignment studies carried out in the previous chapter for $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 \leq x \leq 1$) films grown on GaN-on-Si substrate to ensure a sufficient conduction band offset between the oxide films and the n-type GaN-based HEMT structures (> 1 eV). The surface morphology, band offsets and thermal stability of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films grown on the HEMT structures have been investigated before and after annealing in N_2 at 600 ºC. AFM shows uniform nucleation and smooth surface of the oxides deposited on the HEMT structures before and after annealing. Cross-sectional STEM shows uniform oxide film thickness with continuous and sharp oxide/HEMT interfaces for the samples before and after annealing. XPS measurements show that, for both the GaN-HEMT and InAlN-HEMT interfaces, the CBO of the Ta-doped oxide decreases by 0.1 eV compared to pure Al_2O_3. The CBOs of as-deposited Al_2O_3/GaN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT are 1.6 eV and 1.5 eV, respectively, and the CBOs of Al_2O_3/InAlN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT are 0.8 eV and 0.7 eV, respectively. For the samples deposited on the GaN/AlGaN/GaN HEMTs, a reduction of the Ga-O to Ga-N bond ratios at the oxide/GaN-HEMT interfaces is observed after annealing, which is attributed to a reduction of interstitial oxygen-related defects. As a result, the CBOs of the Al_2O_3/GaN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT samples increase to 2.8 eV and

2.6 eV, respectively. For the samples grown on the InAlN-HEMTs, the results show a reduction of the Al-O-Al/Al-OH bond ratios after annealing associated to a reduction of OH defects that lead to excess of oxygen at the oxide/InAlN interface. As a result, the CBOs of the annealed Al_2O_3/InAlN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT samples increase to 1.5 eV and 1.1 eV, respectively. HR-TEM confirms that the introduction of Ta does not affect the thermal stability of the doped $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ film. The results demonstrate that the annealing step used during HEMT processing significantly increases the CBO between the oxides and the HEMT structures, which is advantageous for n-type HEMTs. Furthermore, all the CBOs obtained after annealing are > 1 eV, which indicates that the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films analysed in this chapter are suitable as gate dielectrics for GaN/AlGaN/GaN and InAlN/GaN HEMT devices.

6.2. Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics on a GaN/AlGaN/GaN HEMT structure

A comparative analysis of the impact of annealing on the gate oxides and their interface with a GaN-capped AlGaN/GaN HEMT structure has been carried out in this section for two samples: undoped Al_2O_3 and Ta-doped $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$. As previously mentioned in the introduction, these samples were selected based on the band alignment studies carried out in section 5.4 in order to ensure sufficient CBOs between the oxide films and GaN (> 1 eV). The GaN/AlGaN/GaN HEMT structure was grown by MOCVD on a 1.0 nm thick 200 mm diameter Si(111) substrate. Prior to the ALD of the oxide films, the uncoated HEMT samples were treated with an ex situ wet-chemical cleaning process. The samples were sonicated in separate acetone and isopropanol for 10 min each to remove organic contaminants and then rinsed in DI water for 2 min and dried with compressed nitrogen. ~ 5 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films were then deposited on the HEMT

structures using an overall number of ALD cycles n = 60. The total number of ALD cycles was doubled with respect the samples studied in section 5.4 to ensure that the total thickness of the oxide film and the GaN cap layer in each sample was bigger than the XPS analysis depth, which was estimated to be slightly under 10 nm based on XPS measurements. After deposition, the samples were annealed by RTA at 600 ºC for 60 s under nitrogen ambient, which is analogous to the conditions used for the formation of ohmic contacts in the GaN-based HEMT structures using an Au-free Ta/Al/Ta metallisation scheme.[1]

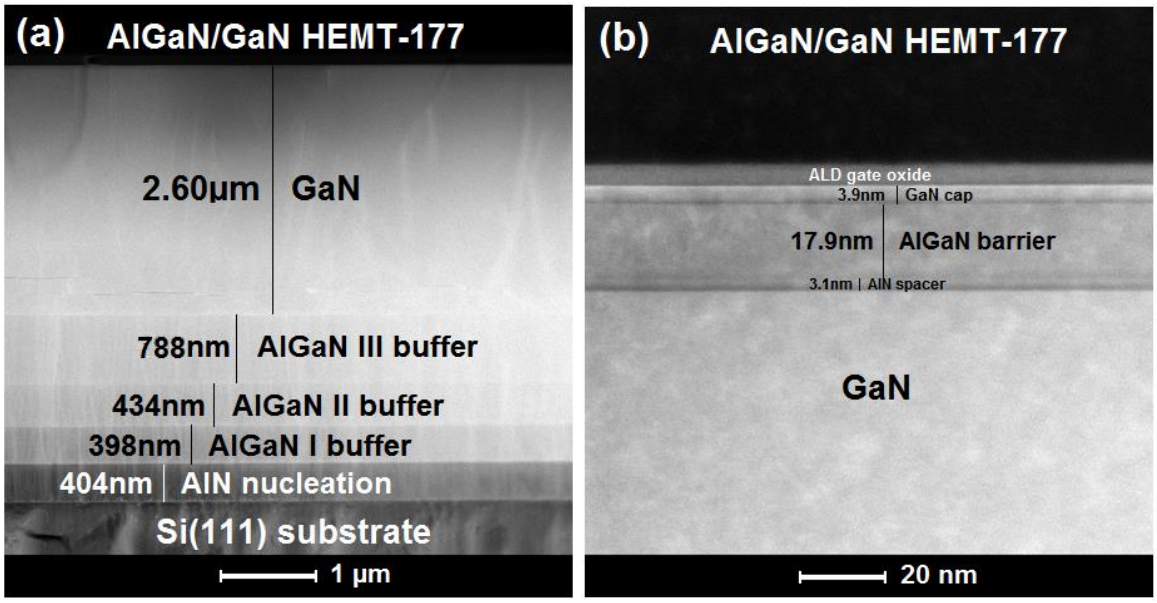

FIG.6.1: Cross-sectional HAADF-STEM images of (a) overall AlGaN/GaN HEMT structure grown on Si(111) substrate and (b) top ALD oxide, GaN cap, AlGaN barrier and AlN spacer layers on GaN.

The composition and thickness of the HEMT nitride epilayers was investigated by HRXRD and STEM. The total thickness of the nitride stack is about 4.6 µm (Fig. 6.1a). It includes a ~ 400 nm thick AlN nucleation layer, three step-graded $Al_xGa_{1-x}N$ intermediate layers with a total thickness of approximately 1.6 µm and Al composition ranging from approximately 60 to 20% (AlGaN/GaN I-III), and a ~ 2.6 µm thick GaN layer which includes a carbon-doped GaN buffer layer at the interface with the AlGaN III layer and an undoped GaN channel grown uninterruptedly without any interlayer. The top HEMT

structure consists of a thin AlN spacer, a ~ 18-19 nm $Al_{0.24}Ga_{0.76}N$ barrier layer and a ~ 4.0 nm top undoped thin GaN cap (Fig. 6.1b).

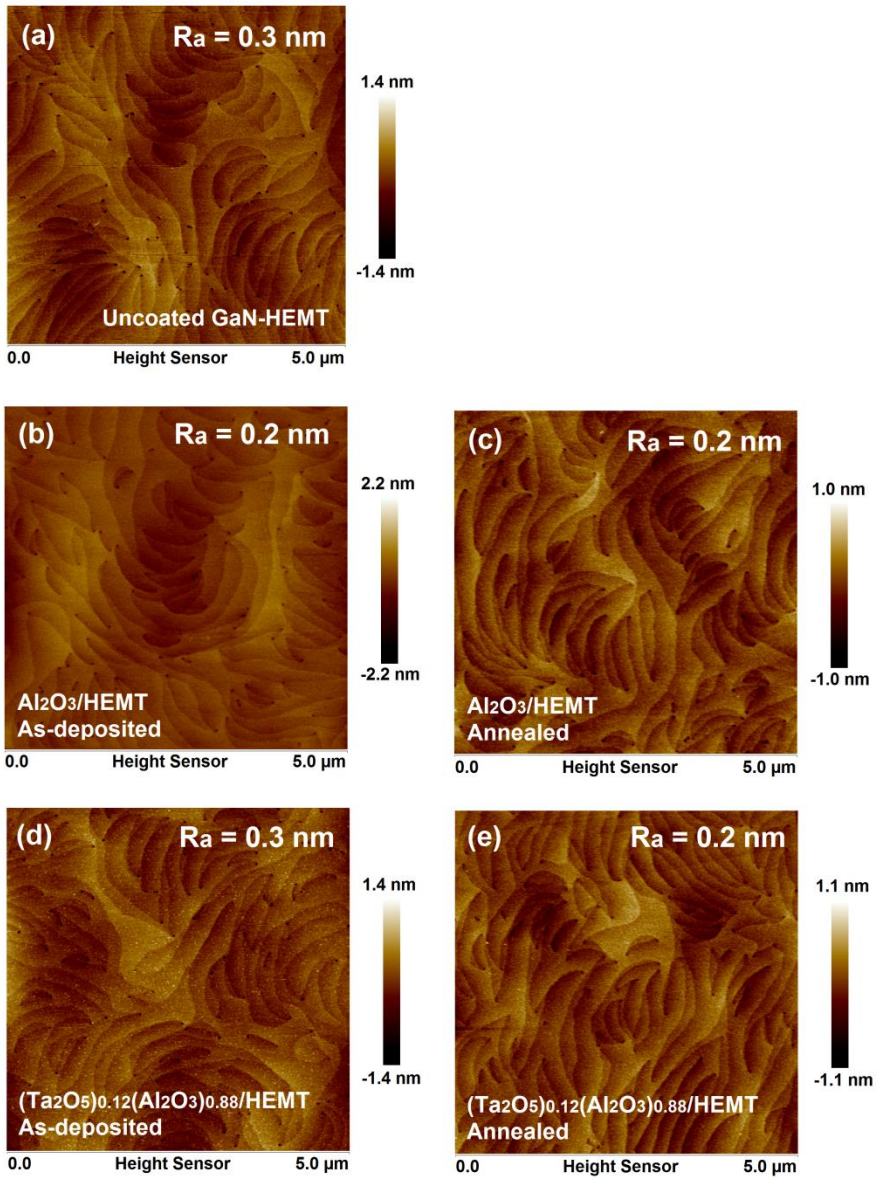

FIG. 6.2: 5.0 µm × 5.0 µm AFM images of the surface of: (a) uncoated GaN/AlGaN/GaN HEMT structure, (b) ~ 5 nm Al_2O_3/GaN-HEMT as deposited, (c) ~ 5 nm Al_2O_3/GaN-HEMT annealed, (d) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT as deposited and (e) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT annealed.

The morphology and roughness of the sample surfaces was analysed by AFM. Figure 6.2a shows the AFM image of the GaN/AlGaN/GaN HEMT structure grown on 8-inch Si(111) substrate. The uncoated sample shows a smooth surface with steps and mixed dislocation pits, typical from a 2D step-flow growth of the nitride epilayers.[2] The

arithmetic average root mean square roughness (R_a) obtained for a 5 x 5 μm^2 area scan is about ~ 0.3 nm, which is in agreement with literature.[3, 4] The surface roughness of the GaN/AlGaN/GaN HEMT before oxide deposition is a critical factor for the electrical performance of the fabricated device as it can affect the nucleation of the oxide and the interface trap density. Smother surface morphologies cause uniform nucleation of the deposited oxide and result in a smooth oxide layer and less available oxygen trapping states and therefore lower density of oxide and interface states, which results in a better electrical performance.[5] After the deposition of the ~ 5 nm thick ALD layers (Fig. 6.2b-e), the R_a of the samples remained within the range of ~ 0.2-0.3 nm, with no changes observed in terms of surface quality after RTA at 600 ºC for 60 s under nitrogen ambient. These results indicate uniform nucleation and smooth surface of the oxides deposited on the GaN surface before and after annealing, which is very promising for their use as potential gate oxides for MOSHEMTs.

6.2.1. Band offsets of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ on GaN/AlGaN/GaN HEMTs

The VBO between the ~ 5 nm thick oxide layers and the GaN-capped AlGaN/GaN HEMT structure were determined using the Grant[6] and Kraut *et al.*[7] method previously used in section 5.4:

$$\Delta E_V = (E_{CL,GaN} - E_{V,GaN}) - (E_{CL,oxide} - E_{V,oxide}) + \Delta E_{CL} \quad (6.1)$$

where $E_{CL,GaN}$ and $E_{V,GaN}$ are the CL and the VBM binding energies of the GaN/AlGaN/GaN HEMT substrate, $E_{CL,oxide}$ and $E_{V,oxide}$ are the CL and the VBM binding energies of the bulk oxide film, and ΔE_{CL} is the difference between the CL binding energies of the GaN/AlGaN/GaN HEMT substrate and the oxide in the oxide/GaN-HEMT interface.

The XPS binding energies of the Ga-N bond and Al 2p are used in this study as the core levels of bulk GaN/AlGaN/GaN HEMT substrate and oxides, respectively.

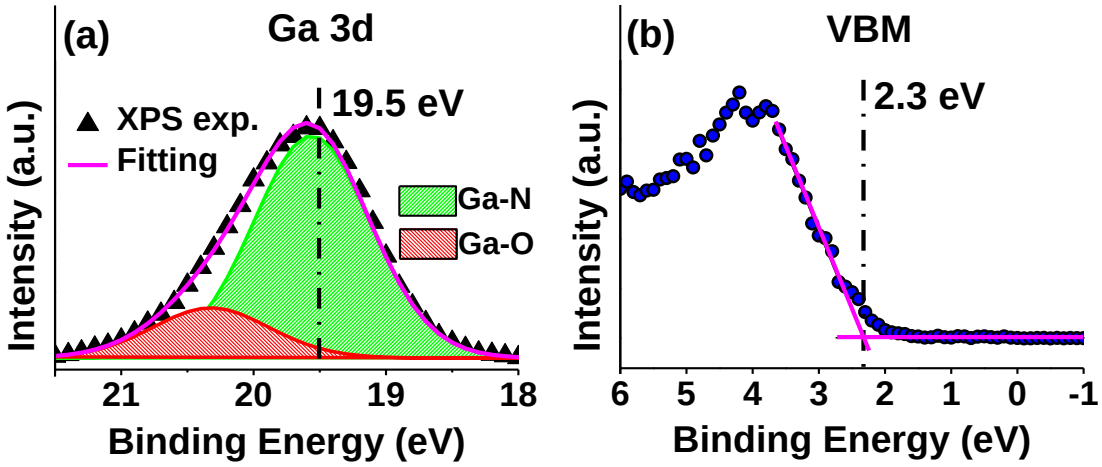

FIG. 6.3: XPS spectra of (a) Ga 3d core level and (b) VBM obtained for the uncoated GaN/AlGaN/GaN HEMT structure. The core level of the Ga-N peak and the VBM are indicated with dashed lines.

Figure 6.3 shows the Ga 3d and VBM spectra obtained for the uncoated GaN/AlGaN/GaN HEMT substrate. As carried out for the XPS spectra obtained in the previous chapter for the GaN-on-Si substrate, the Ga 3d spectrum has been deconvoluted into two components corresponding to Ga-N bonds from the GaN cap and Ga-O bonds from oxidation of the GaN surface after air exposure (Fig. 6.3a),[8] and the VBM has been determined by extrapolating the linear fit with 95% C.I. applied to the leading edge of the valence band spectrum and calculating its intersection with the base line (Fig. 6.3b).[9] The $E_{CL,GaN} - E_{V,GaN}$ calculated from the difference between the binding energy of the Ga-N bond and the VBM is 17.2 eV, which is very close to the value of 17.3 eV obtained for the GaN-on-Si substrate analysed in the previous chapter. As previously mentioned, these values are smaller than the values of 17.7-17.8 eV obtained from the electronic-state studies of bulk GaN samples.[10, 11] This is due to the presence of in-plane stress in the nitride epilayers caused by lattice parameters and thermal expansion coefficients mismatch with the underlying Si(111) substrate, which has a significant influence on the electronic band

structure leading to a variation in the VBM.[12] This has been demonstrated in a study carried out on a similar GaN-cap AlGaN/GaN HEMT structure also grown on a 200 mm diameter Si(111) substrate using the same MOCVD reactor, where the nitride epilayers exhibited in-plane stress values in the range of 0.1 - 0.3 GPa from the centre to the edges of the wafer.[13]

The $E_{CL,oxide} - E_{V,oxide}$ value is calculated from the binding energy difference between the Al 2p core level and the VBM of the ~ 10 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films before and after annealing (section 5.4). These values are summarised in Table 6.1.

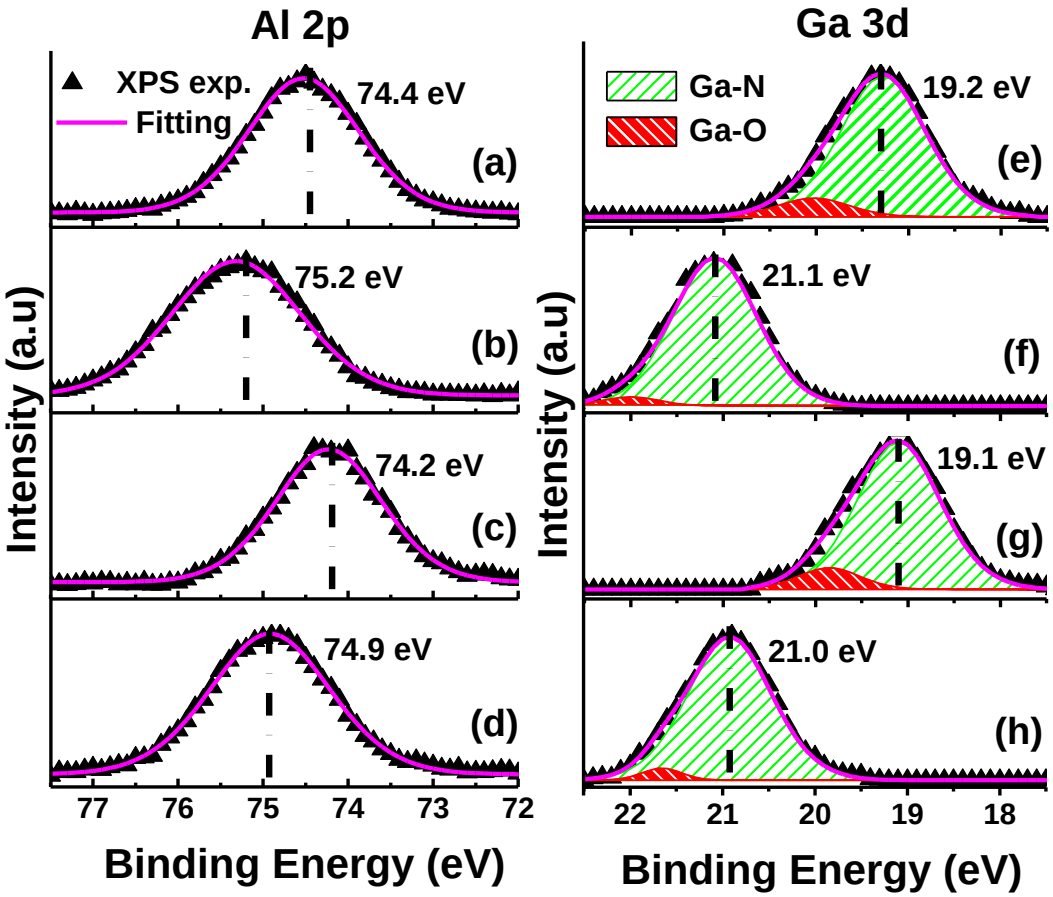

FIG. 6.4: XPS Al 2p spectra of: (a) ~ 5 nm Al_2O_3/GaN-HEMT as deposited, (b) ~ 5 nm Al_2O_3/GaN-HEMT annealed, (c) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT as deposited and (d) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT annealed; and Ga 3d spectra of: (e) ~ 5 nm Al_2O_3/GaN-HEMT as deposited, (f) ~ 5 nm Al_2O_3/GaN-HEMT annealed, (g) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT as deposited, and (g) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT annealed.

Figure 6.4 shows the Ga 3d and Al 2p core level spectra of the as-deposited and annealed ~ 5 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers grown on the GaN/AlGaN/GaN HEMT. The ΔE_{CL} values calculated from the difference between the binding energy of the Ga-N bond and the Al 2p core level of the oxide/GaN-HEMT interfaces before and after annealing are summarised in Table 6.1. The results indicate that the band bending is altered during post-deposition annealing. The Al 2p and Ga 3d core levels shift to higher energies after annealing by ~ 0.8 eV and ~ 1.9 eV, respectively. The value of ΔE_{CL} for the as-deposited Al_2O_3/GaN-HEMT sample is measured to be 55.2 eV, which according to equation 6.1 gives a VBO of 1.5 eV. This value is smaller than the experimental value of 1.8 eV reported by other authors,[14] which is similar to the theoretical value of 1.7 eV calculated from the electron affinity model[15] and the charge neutrality level (CNL) model when the Al_2O_3 and GaN CNLs are calculated by local density approximation (LDA).[16] However, the Al_2O_3/GaN VBO calculated using CNLs values for GaN and Al_2O_3 determined empirically is 1.4 eV,[17] which is closer to the value obtained experimentally in this study. The value of ΔE_{CL} measured for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT sample as-deposited is 55.1 eV, corresponding to a VBO of 1.2 eV, which implies that the addition of Ta to Al_2O_3 results in a reduction of 0.3 eV with respect the VBO of undoped Al_2O_3 on the GaN/AlGaN/GaN HEMT. This reduction is within the expected limits considering the smaller theoretical VBO value of 1.1 eV calculated for Ta_2O_5 on GaN using the LDA and CNL model.[18] It should be noted that, the VBOs obtained in the present study for the as-deposited Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films on the GaN-based HEMT structure are bigger than the values obtained in the previous chapter for the same oxides deposited on GaN. The VBOs of the ~ 2.5 nm thick Al_2O_3/GaN and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN samples are 1.1 eV and 1.0 eV, respectively, whereas the VBOs of the ~ 5 nm thick Al_2O_3/GaN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT samples are 1.5 eV and 1.2 eV,

respectively. This could be due to the different substrates used and/or due to the difference in the thickness of the deposited oxide films. Since there is not a significant variation in the Ga 3d and the VBM binding energies of the GaN/AlGaN/GaN HEMT with respect the GaN substrate, this change in the VBO values is attributed to the difference in the oxide film thicknesses. In literature, the VBO of Al_2O_3 on GaN has been found to increase with the thickness of the deposited oxide film, with values of 0.7 eV and 0.9 eV reported for 1.3 nm thick and 4 nm thick Al_2O_3 on GaN, respectively.[19] This is due to the fact that the upward band bending of the GaN energy bands occurs near the surface and thus, the difference between the Fermi level and the Ga 3d core level and the VBM in GaN decreases towards the surface. Since the x-ray penetration depth in XPS measurements is approximately constant, the probe depth in the GaN layer depends on the oxide film thickness. Therefore, if the top oxide film is thicker, the GaN photoelectrons scanned will come mainly from nearer the surface region where the difference between Fermi level and the Ga 3d core level and VBM is smaller. Hence, the resultant XPS spectra determined from the photoelectrons emitted from a certain depth in the sample will be shifted towards smaller energies and the extracted VBO will be larger, which is in agreement with the results. This brings out a limitation of the XPS method used for the calculation of VBOs. After annealing, the binding energy difference between Al 2p and Ga 3d core levels decreases by ~ 1.1 eV, resulting in VBOs of 0.3 eV and 0.1 eV for the annealed Al_2O_3/GaN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT interfaces, respectively. This reduction in the VBOs indicates that the annealing process used significantly changes the band alignment between the dielectrics and the GaN/AlGaN/GaN HEMT.

The CBOs between the oxide films and the GaN-based heterostructure are derived by the following equation:

$$\Delta E_C = E_g - \Delta E_V - 3.4 \text{ (eV)} \quad (6.2)$$

where 3.4 eV is the bandgap of GaN.[20] The bandgap values of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers (section 5.2), as well as their valence and conduction band offsets with the GaN/AlGaN/GaN HEMT structure before and after annealing in N_2 at 600 ºC for 60 s are listed in Table 6.1. The results show a reduction of 0.1 eV in the CBO of the Ta-doped sample with respect to the undoped Al_2O_3, which indicates that the reduction of the CBO due to the introduction of Ta-dopant is smaller compared to the reduction of 0.3 eV observed for the VBO. Figure 6.5 shows a schematic of the energy band diagrams determined by XPS for the as-deposited and annealed Al_2O_3/GaN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT interfaces. The results demonstrate that the annealing process step significantly alters the band offsets at the dielectric/nitride interfaces, reducing the VBOs and increasing the CBOs. This means that the post-deposition annealing step using for HEMT processing improves the interface characteristics of the samples analysed, giving higher barrier heights to the n-type HEMTs and therefore potentially lower gate leakage currents.

TABLE 6.1. Summary of the $(E_{CL} - E_V)_{oxide}$, ΔE_{CL}, ΔE_v, E_g and ΔE_C values for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers and the GaN/AlGaN/GaN HEMT structure, before and after annealing in N_2 at 600 ºC for 60 s.

Samples	$(E_{CL}$-$E_V)_{oxide}$ (eV)	ΔE_{CL} (eV)	ΔE_V (eV)	E_g (eV)	ΔE_C (eV)
As-deposited Al_2O_3	71.0	55.2	1.5	6.5	1.6
Annealed Al_2O_3	71.0	54.1	0.3	6.5	2.8
As-deposited $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$	71.1	55.1	1.2	6.1	1.5
Annealed $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$	71.1	54.0	0.1	6.1	2.6

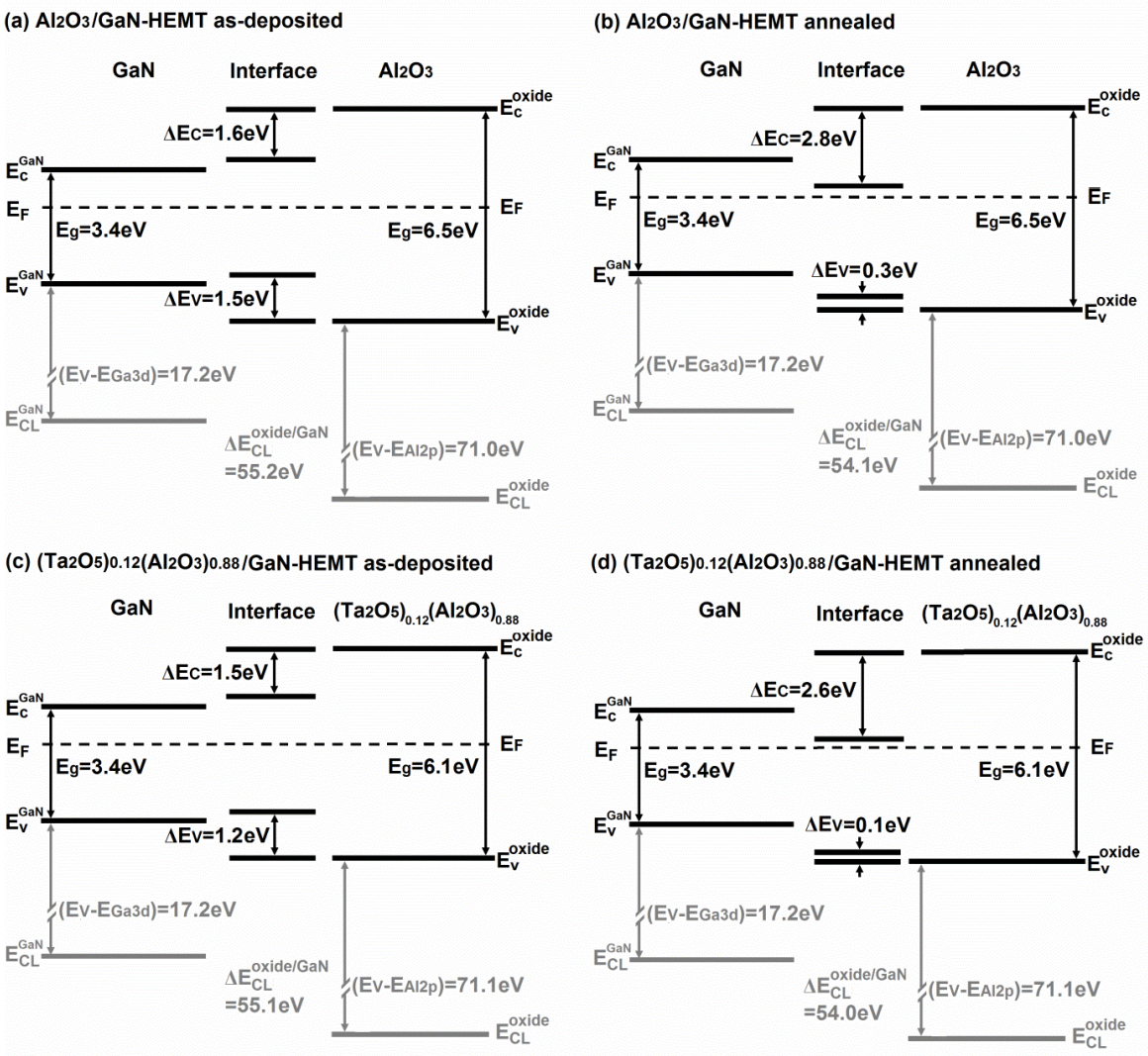

FIG. 6.5: Energy band diagrams determined by XPS for (a) Al_2O_3/GaN-HEMT interface as deposited, (b) Al_2O_3/GaN-HEMT interface annealed, (c) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT interface as deposited and (d) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT interface annealed. The valence band offset (ΔE_V), conduction band offset (ΔE_C), GaN-HEMT core level (E_{CL}^{GaN}), oxide core level (E_{CL}^{oxide}) and the core level separation across the interface (ΔE_{CL}) are represented.

6.2.2. Ga-O to Ga-N ratio at the GaN surface

A reduction in the Ga-O to Ga-N peak area ratio is observed for the interface samples with respect to the uncoated GaN/AlGaN/GaN HEMT substrate (Figs. 6.3 and 6.4). The Ga-O/Ga-N peak area ratio calculated for the uncoated GaN/AlGaN/GaN HEMT sample is 0.23, whereas the Ga-O/Ga-N area ratios of as-deposited Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$

films grown on the GaN/AlGaN/GaN HEMT structure are 0.11 and 0.10 respectively. This reduction in the Ga-O bond concentration is consistent with the 'self-cleaning' effect previously observed when Al_2O_3 is grown by ALD on GaAs,[21] InGaAs[22] and AlGaN,[23, 24] which suggests the passivation of the oxide surface by the metal precursor during deposition and a possible decrease in the concentration of gallium oxide states upon interaction with TMA during the first ALD cycles.[24] Al_2O_3 surface passivation in GaN-based MOSHEMTs is expected to reduce the number of negative electronic surface states. In addition to reducing the gate leakage current, this decrease in surface states can mitigate current collapse caused by the formation of a virtual gate arising from negative charge injection from the gate edges.[25] Additionally, the Ga-O/Ga-N peak area ratios of the annealed Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ samples further reduce to 0.04 for both samples. This 'clean up' effect after annealing has previously been reported on ALD ZrO_2 grown on GaN.[26] The decrease in the Ga-O to Ga-N peak area after annealing appears to lead to an increase of the Ga-N bond binding energy (Fig. 6.4b) which suggests that the Fermi-Level position at the GaN surface is affected by surface-related defects states associated with GaO_x. Oxygen interstitial defects have been shown to act as deep acceptors in Al_2O_3/GaN structures.[27] Spontaneous polarisation in GaN leads to a negative bound polarisation charge at the GaN surface and ionised donors to compensate these defects,[28] which results in upward band bending at the GaN surface and lower Ga-N bond binding energy. The shifts of the Ga-N bond to higher binding energies after annealing can therefore be attributed to a reduction of the upward band bending at the oxide/GaN interface as a consequence of the reduction of the defects or excess interstitial oxygen by the annealing process, which is confirmed by the results.

6.2.3. Cross section and thermal stability of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics on GaN/AlGaN/GaN HEMT structures

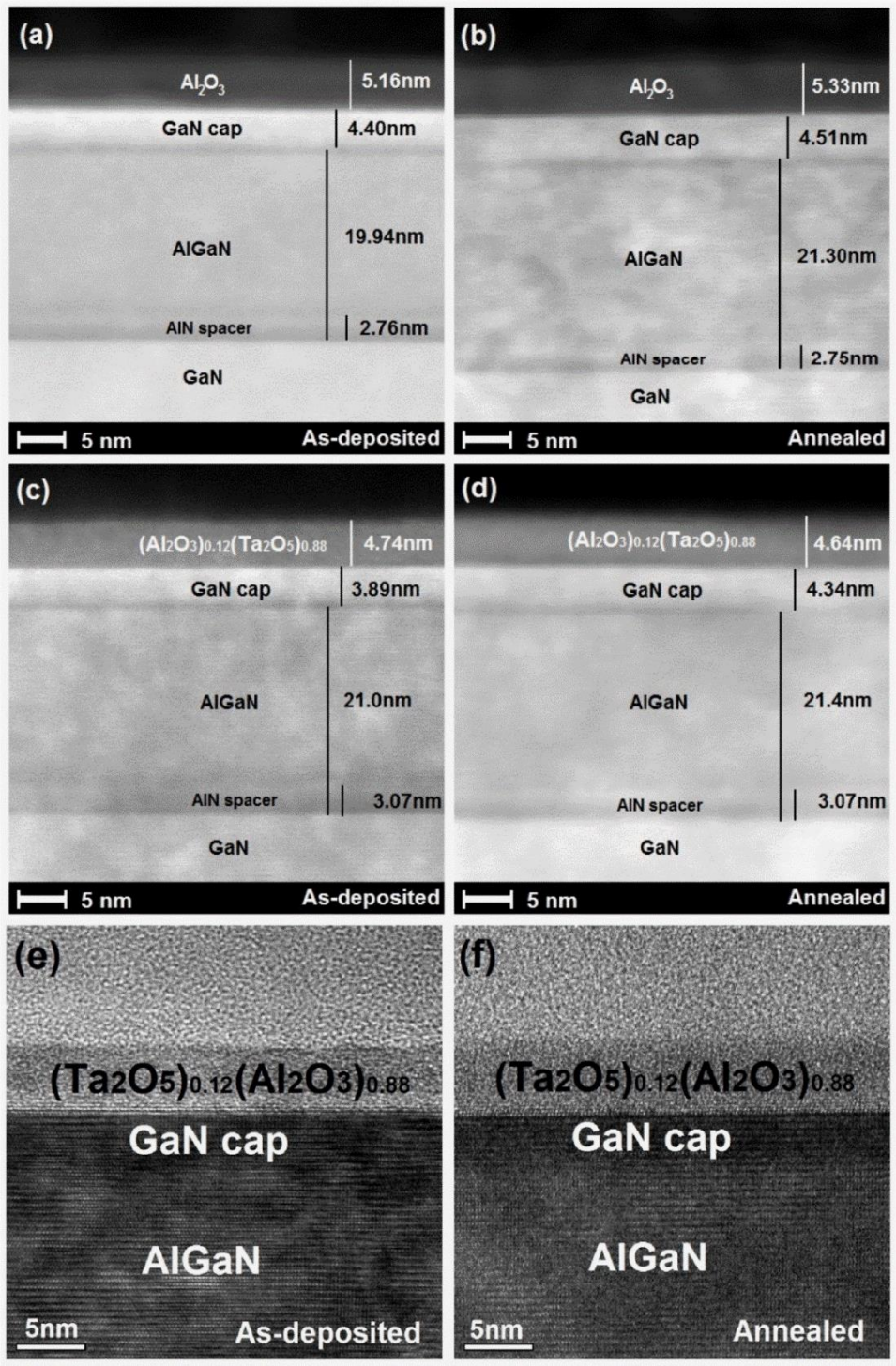

FIG. 6.6: (a)-(d) Cross-sectional HAADF-STEM of as-deposited and annealed Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers grown on the GaN/AlGaN/GaN HEMT structure highlighting the top ALD oxide, GaN cap, AlGaN barrier, and AlN spacer on GaN buffer layers. (e) and (f) represent cross-sectional HR-BFTEM of the as-deposited and annealed $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers grown on top of such HEMT structures.

The cross-sectional high-angle annular dark field STEM (HAADF-STEM) images of the ~ 5 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers grown on the GaN/AlGaN/GaN HEMT structure before and after annealing are shown in Figures 6.6a-d. As the HEMT structure is grown on a 200 mm diameter Si(111) substrate, a small variation in AlGaN barrier and GaN cap thicknesses is expected across the wafer. HAADF-STEM imaging shows a continuous and sharp interface of the ALD oxide films and the GaN cap layer. The oxide film thickness is uniform for both the as-grown and annealed sets of samples. In order to further investigate any Ta-doping induced inhomogeneity at the interfaces, high-resolution bright-field TEM (HR-BFTEM) was performed for the HEMT samples coated with the ~ 5 nm thick $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers before and after annealing (Figs. 6.6e and 6.6f). The as-deposited and annealed samples show a similar morphology in terms of the amorphous nature of the oxide layers. The interfaces show good thermal stability after RTA at 600 ºC in N_2, with a sharp and very flat transition from crystalline GaN to amorphous oxide with no obvious interfacial layer. There appears to be a slight improvement in the interface abruptness of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ oxide layers and the GaN/AlGaN/GaN HEMT structure after RTA. The TEM results therefore prove that the introduction of Ta does not affect the thermal stability of the investigated $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ oxide film during the annealing process used in the present study.

6.3. Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics on InAlN/GaN HEMT structure

In this section, the interfacial properties of ~ 5 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers deposited on an InAlN/GaN HEMT have been analysed before and after annealing. The samples fabrication steps are the same than the ones used in the

previous section. The InAlN/GaN HEMT structure was grown by MOCVD on a 1.0 mm thick 200 mm diameter Si(111) substrate. Prior to ALD, the HEMT samples were sonicated in separate acetone and isopropanol for 10 min each to remove organic contaminants and then rinsed in DI water for 2 min and dried with compressed nitrogen. The ~ 5 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films were deposited on the InAlN/GaN HEMTs using and total number of ALD cycles n = 60, and post-deposition RTA was performed at 600 ºC for 60 s under N_2 ambient.

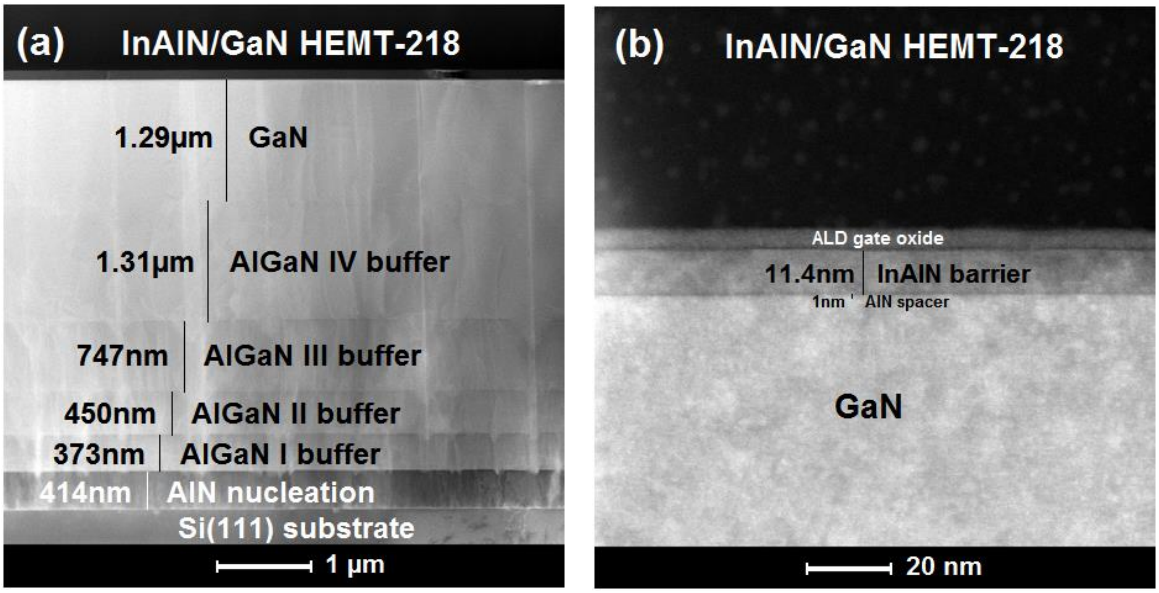

FIG. 6.7: Cross-sectional HAADF-STEM images of (a) overall InAlN/GaN HEMT structure grown on Si(111) substrate and (b) top ALD oxide, InAlN barrier and AlN spacer layers on GaN.

From STEM, the total thickness of the nitrides stack is about 4.6 µm and it includes a ~ 400 nm thick AlN nucleation layer, four step-graded $Al_xGa_{1-x}N$ intermediate buffer layers (AlGaN I-IV) with total thickness of about 2.9 µm and a GaN layer with thickness of about 1.3 µm (Fig. 6.7a). The Al composition obtained from HRXRD for the four step-graded $Al_xGa_{1-x}N$ intermediate buffer layers ranges from approximately 60 % to 4 %. The top HEMT structure consists of a thin AlN spacer of about ~ 1 nm and an $In_{0.18}Al_{0.82}N$ barrier layer of ~ 11-12 nm (Fig. 6.7b).

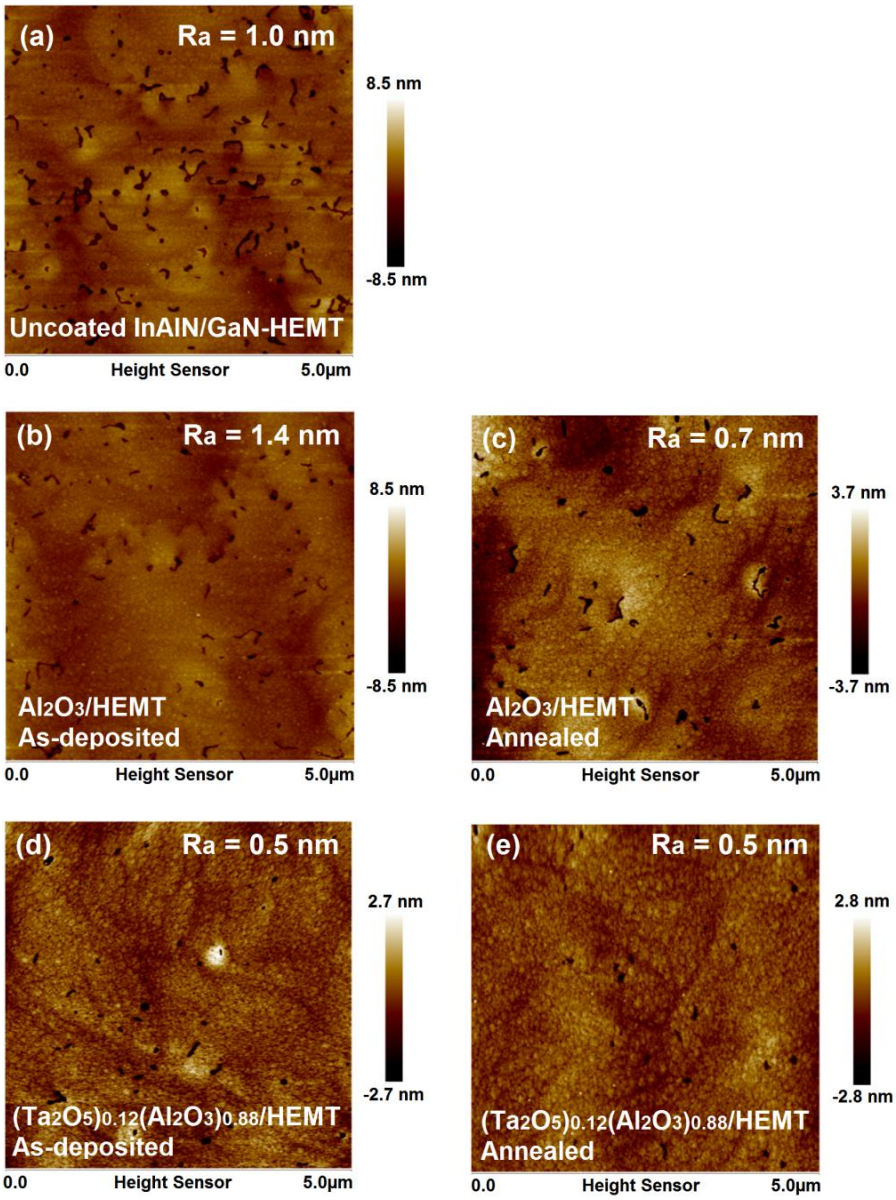

FIG.6.8: 5.0 µm × 5.0 µm AFM images of the samples surface obtained for: (a) uncoated InAlN/GaN HEMT structure, (b) ~ 5 nm Al_2O_3/InAlN/GaN-HEMT as deposited, (c) ~ 5 nm Al_2O_3/InAlN/GaN-HEMT annealed, (d) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN/GaN-HEMT as deposited and (e) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN/GaN-HEMT annealed

AFM was used to assess the morphology and roughness of the sample surfaces. The surface of the uncoated InAlN/GaN HEMT grown on 8-inch Si(111) substrate shows atomic steps and large pits characteristic of InAlN/GaN heterostructures grown by MOCVD (Fig. 6.8a).[29] These pits correspond to dislocations generated during the growth of the AlN spacer due to the large lattice mismatch with the underlying GaN buffer layers,

propagated through the InAlN layer during growth.[30] The R_a obtained for a 5 x 5 μm^2 area scan for the uncoated InAlN/GaN-HEMT is 1.0 nm. This surface roughness is in agreement with the values reported in literature for high-quality InAlN/GaN HEMTs grown by MOCVD, which are in the range of ~0.8 nm-1.2 nm depending on the growth temperature.[31, 32] After the deposition of the ~ 5 nm thick ALD oxide films, the R_a of as deposited and annealed samples decreases to 0.5-0.7 nm, with the exception of the as-deposited Al_2O_3 sample which shows a higher surface roughness of 1.4 nm (Fig. 6.8b-e). This could be a consequence of the higher density of dislocation pits present in the scanned sample surface together with a limited choice of scan area due to the small sample size, which results in larger surface roughness. The results show that after post-deposition annealing the surface of the coated samples is smoother than the InAlN/GaN sample surface and has lower density of dislocation pits, which is beneficial for their use as potential gate oxides for MOSHEMTs.

6.3.1. Band offsets of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ on InAlN/GaN HEMTs

The VBOs of the ALD oxide layers on the InAlN/GaN HEMT structure were calculated using the Grant and Kraut method as discussed in Ref.7, given by the following equation:

$$\Delta E_V = (E_{CL,InAlN} - E_{V,InAlN}) - (E_{CL,oxide} - E_{V,oxide}) - \Delta E_{CL} \quad (6.3)$$

where $E_{CL,InAlN}$ and $E_{V,InAlN}$ are the CL and the VBM binding energies of the InAlN/GaN-HEMT substrate, $E_{CL,oxide}$ and $E_{V,oxide}$ are the CL and the VBM binding energies of the bulk oxide film and ΔE_{CL} is the difference between the CL binding energies of the InAlN/GaN HEMT substrate and the oxide in the oxide/InAlN interface. In this study, the XPS binding energies of N 1s and Al 2p are used as the core levels of bulk InAlN/GaN HEMT substrate and oxides, respectively.

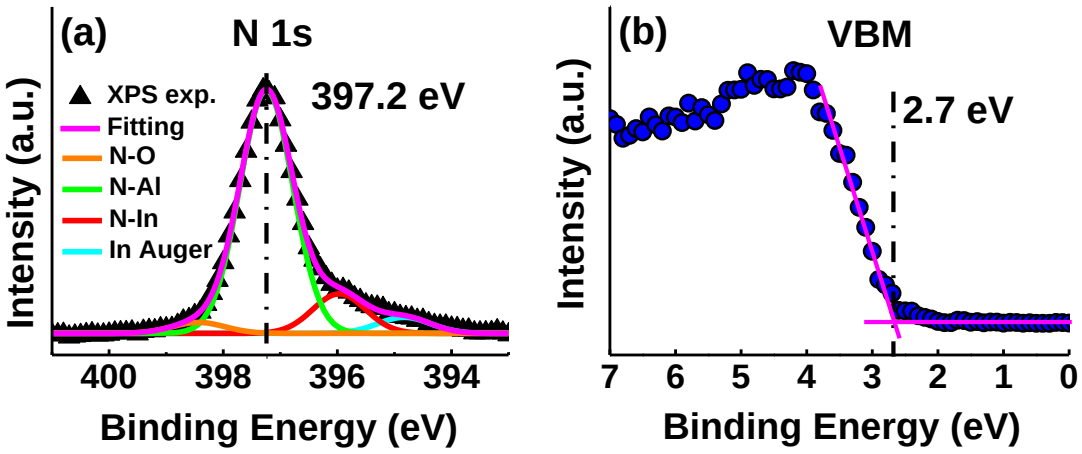

FIG. 6.9: XPS spectra of (a) N 1s core level and (b) VBM obtained for the uncoated InAlN/GaN HEMT structure. The core level of the N 1s peak and the VBM are indicated with dashed lines.

Figure 6.9 shows the N 1s and VBM spectra obtained for the uncoated HEMT substrate. The N 1s spectrum obtained for the InAlN/GaN HEMT sample has been fitted with four subpeaks (Fig. 6.9a). The main peak with a binding energy of 397.2 eV is assigned to the N-Al bond,[33] and the second main peak with a binding energy of 396.0 eV is assigned to the N-In bond.[34] The shoulder peak at lower binding energy is attributed to the Indium Auger peak.[35] Finally, the shoulder peak at higher binding energy is attributed to N-O bonds from the formation of oxynitride on the InAlN film surface after exposure with atmosphere.[36] The $E_{CL,InAlN} - E_{V,InAlN}$ value calculated from the difference between the binding energy of the N 1s core level and the VBM in the InAlN/GaN HEMT substrate is 394.5 eV, which is very good agreement with the value of 394.46 eV found in literature for an $In_{0.18}Al_{0.82}N$/GaN HEMT grown on sapphire substrate.[37]

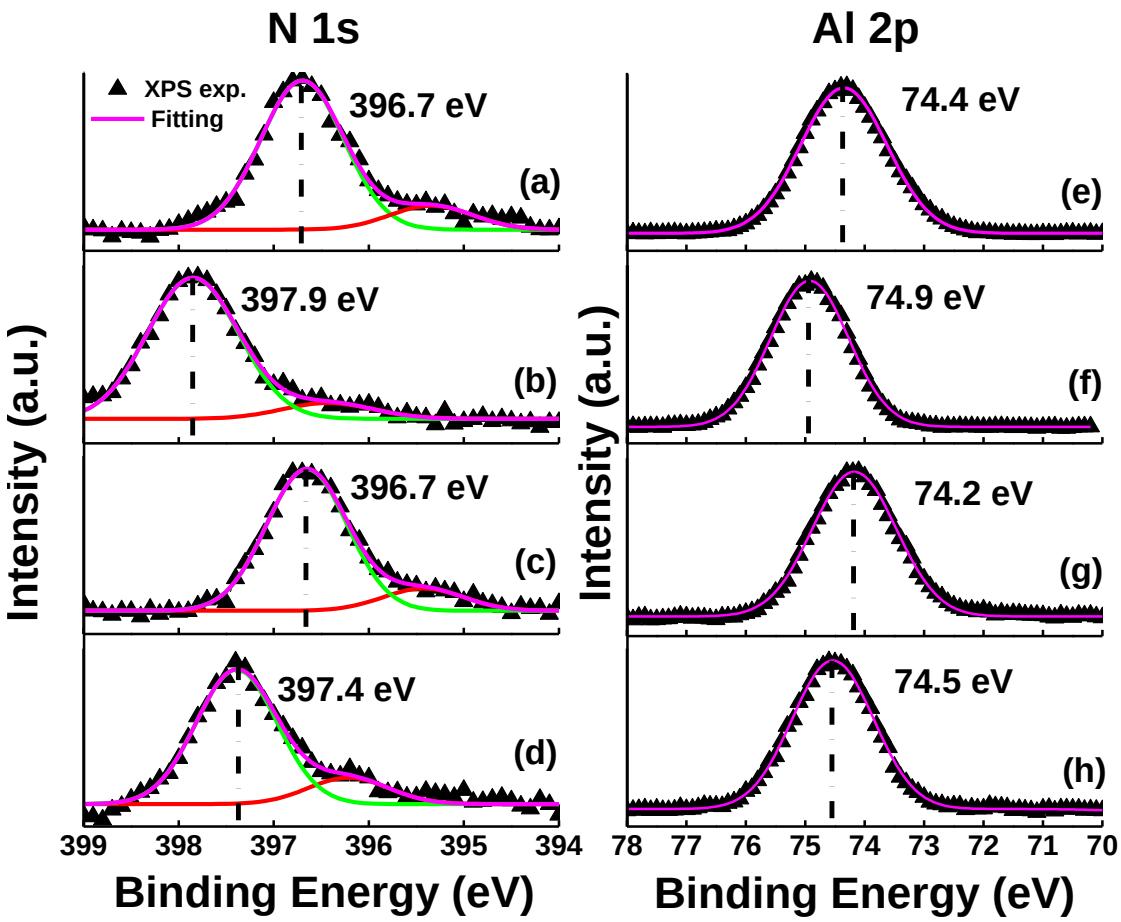

FIG. 6.10: XPS N 1s spectra of: (a) ~ 5 nm Al_2O_3/InAlN-HEMT as deposited, (b) ~ 5 nm Al_2O_3/InAlN-HEMT annealed, (c) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT as deposited, and (d) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT annealed; and Al 2p spectra of: (e) ~ 5 nm Al_2O_3/InAlN-HEMT as deposited, (f) ~ 5 nm Al_2O_3/InAlN-HEMT annealed, (g) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT as deposited, and (h) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT annealed.

Figure 6.10 shows the N 1s and Al 2p core level spectra obtained for the as-deposited and annealed ~ 5 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers grown on the InAlN/GaN HEMT. The ΔE_{CL} values calculated from the difference between the binding energies of the of the N 1s and the Al 2p core levels of the oxide/InAlN interfaces before and after annealing are summarised in Table 6.2. The results show that the band bending at the oxide/InAlN interfaces is altered during post-deposition annealing. After annealing, the N 1s and Al 2p core levels shift to higher energies by ~ 1.1 eV and ~ 0.5 eV for the

Al_2O_3/InAlN-HEMT sample and by ~ 0.7 eV and ~ 0.3 eV for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT sample, respectively. The value of ΔE_{CL} for the as-deposited Al_2O_3/InAlN-HEMT sample is measured to be 322.3 eV, which according to equation 6.3 gives a VBO of 1.2 eV. This value agrees with the VBO of 1.2 eV reported in literature for ALD Al_2O_3 grown on an $In_{0.17}Al_{0.83}N$/GaN heterostructure.[38] The value of ΔE_{CL} measured for the as-deposited $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT sample is 322.5 eV, which corresponds to a VBO of 0.9 eV. This implies a reduction of 0.3 eV in the VBO of the Ta-doped $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ film with respect the undoped Al_2O_3 film on the InAlN/GaN HEMT. This reduction is the same as the one observed in section 6.2.1 for the same oxides deposited on a GaN/AlGaN/GaN HEMT. As a result, the VBOs determined for the Al_2O_3/InAlN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT interfaces are ~ 0.3 eV smaller than the VBOs obtained for the Al_2O_3/GaN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/Ga-HEMT interfaces. This reduction is expected considering the VBO of 0.2 ± 0.2 eV for $In_{0.17}Al_{0.83}N$ on GaN reported in literature.[39] After annealing, the binding energy difference between of the N 1s and the Al 2p core levels for the Al_2O_3/InAlN/GaN HEMT sample increases by ~ 0.7 eV, resulting in a VBO of 0.5 eV. For the annealed $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN/GaN HEMT sample, the binding energy difference between of the N 1s and the Al 2p core levels increases by ~ 0.4 eV, which results in a VBO of 0.5 eV. The results indicate that the annealing process significantly varies the band alignment between the oxide films and the InAlN/GaN HEMT, with a bigger change observed for the Al_2O_3/InAlN/GaN HEMT sample. This can be explained by the fact that, as previously observed in section 6.2, the post-deposition annealing step used in this study can remove the defects or excess interstitial oxygen from the oxide/InAlN interface reducing the upward band bending and shifting the core levels at the interface to higher binding energies. Since the oxygen coordination numbers of Al_2O_3 and Ta_2O_5 are

different, the amount of oxygen defects per metal atom varies with the oxide film composition and therefore the reduction of oxygen defects and changes in band bending after annealing it is expected to depend on the oxide film composition and its interface with the InAlN-HEMT.

The CBOs between the oxide films and the InAlN/GaN heterostructure can be derived by the following equation:

$$\Delta E_C = E_g - \Delta E_V - 4.5 \text{ (eV)} \quad (6.4)$$

where 4.5 eV is the bandgap of the $In_{0.18}Al_{0.82}N$ layer, calculated using the standard bowing equation as obtained from a study of $In_{1-x}Al_xN$ samples:[40]

$$E_g^{InAlN}(x) = (1-x)\, E_g^{InN} + x\, E_g^{AlN} - 4.7x\,(1-x) \quad (6.5)$$

where E_g^{InN} and E_g^{AlN} are the bandgaps of InN and AlN, assumed to be 0.78 eV and 6.2 eV,[41] respectively.

The bandgap values of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers (section 5.2), as well as their valence and conduction band offsets with the InAlN/GaN HEMT structure before and after annealing in N_2 at 600 ºC for 60 s are listed in Table 6.2. The results show a reduction of 0.1 eV in the CBO of the as-deposited $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT sample with respect the as-deposited Al_2O_3/InAlN-HEMT sample. As previously observed for the VBOs, the reduction in CBO of the Ta-doped $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ film with respect the undoped Al_2O_3 film is the same than the one obtained for the same oxide films deposited on a GaN/AlGaN/GaN HEMT structure in section 6.2.1. Therefore, it can be concluded that the variations observed in the VBO and CBO due to the introduction of Ta dopant in the as-deposited oxide films do not depend on the underlying nitride layer. This means that the differences between the band offsets of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films with

the HEMT structure are due to the oxide films properties such as composition and bandgap. Figure 6.11 shows a schematic of the energy band diagrams determined by XPS for the as-deposited and annealed Al_2O_3/InAlN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT interfaces. After annealing, the band offsets at the oxide/InAlN interfaces change significantly. As occurred with the oxide/GaN-HEMT samples in section 6.2.1, The annealing process step reduces the VBOs and increases the CBOs, improving the interface characteristics of the samples by giving higher barrier heights to the n-type InAlN/GaN HEMTs. Furthermore, the resultant CBOs obtained after RTA are > 1 eV, which indicates that both Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ are suitable as gate dielectrics for InAlN/GaN HEMT devices.[1]

TABLE 6.2. Summary of the $(E_{CL} - E_V)_{oxide}$, ΔE_{CL}, ΔE_v, E_g and ΔE_C values for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers and the InAlN/GaN HEMT structure, before and after annealing in N_2 at 600 ºC for 60 s.

Samples	$(E_{CL}$-$E_V)_{oxide}$ (eV)	ΔE_{CL} (eV)	ΔE_V (eV)	E_g (eV)	ΔE_C (eV)
As-deposited Al_2O_3	71.0	322.3	1.2	6.5	0.8
Annealed Al_2O_3	71.0	323.0	0.5	6.5	1.5
As-deposited $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$	71.1	322.5	0.9	6.1	0.7
Annealed $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$	71.1	322.9	0.5	6.1	1.1

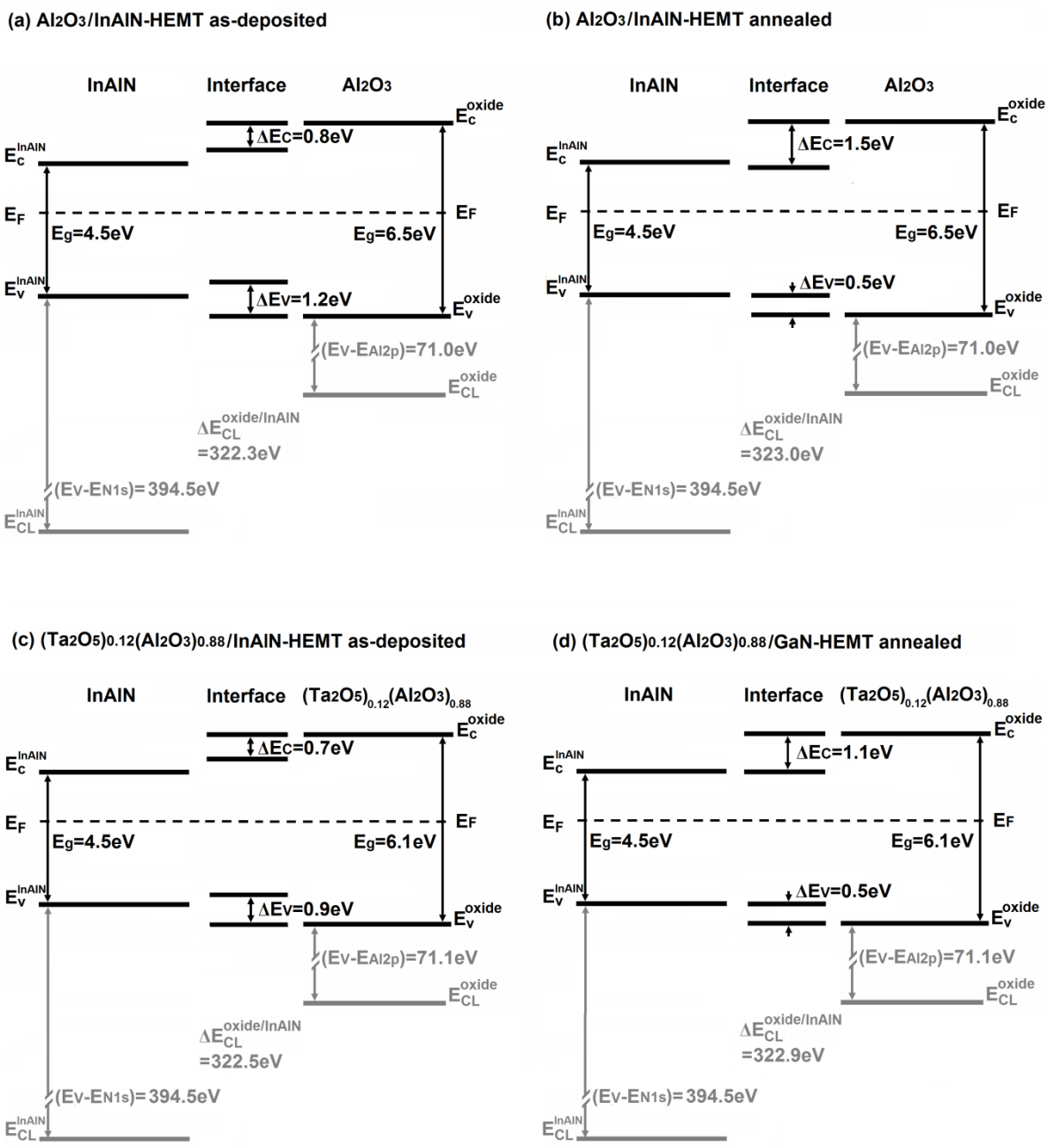

FIG. 6.11: Energy band diagrams determined by XPS for (a) Al_2O_3/InAlN-HEMT interface as deposited, (b) Al_2O_3/InAlN-HEMT interface annealed, (c) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT interface as deposited and (d) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT interface annealed. The valence band offset (ΔE_V), conduction band offset (ΔE_C), InAlN-HEMT core level (E_{CL}^{InAlN}), oxide core level (E_{CL}^{oxide}) and the core level separation across the interface (ΔE_{CL}) are represented.

6.3.2. O_{II} to O_I ratio at the InAlN surface

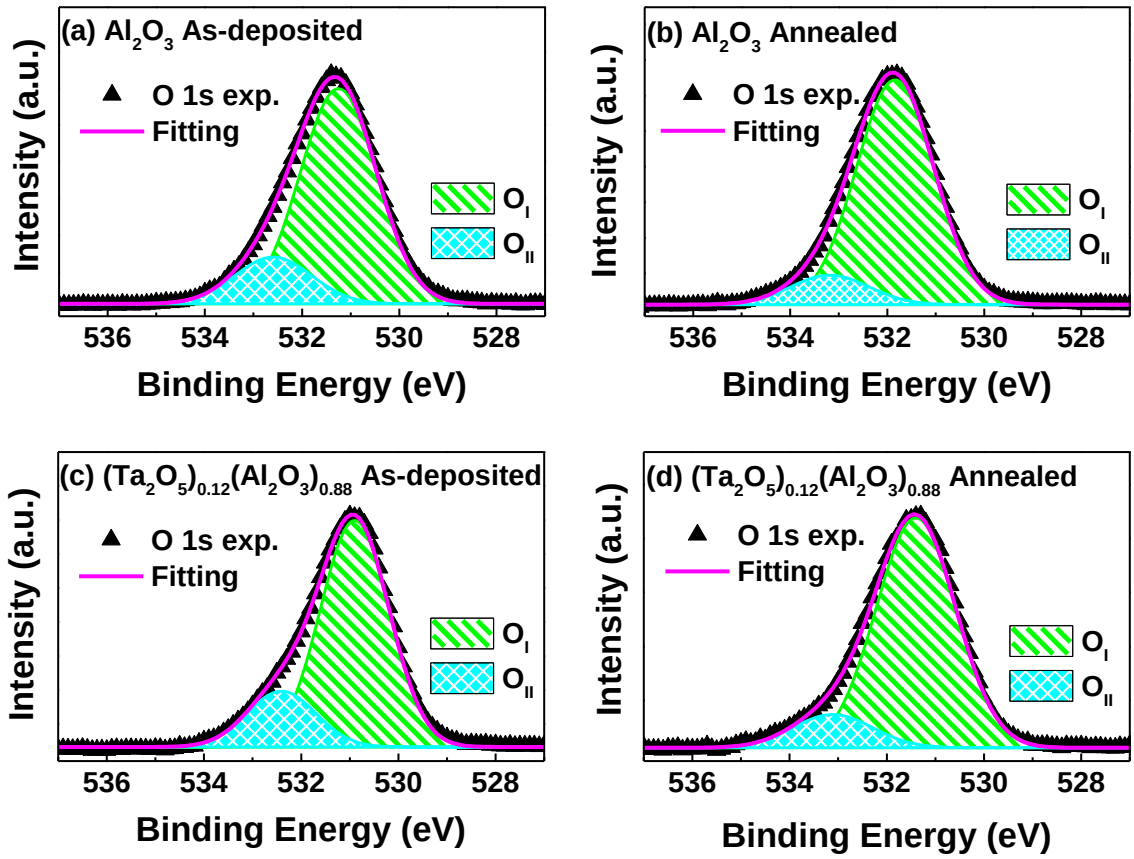

FIG. 6.12: XPS O 1s spectra of: (a) ~ 5 nm Al_2O_3/InAlN-HEMT as deposited, (b) ~ 5 nm Al_2O_3/InAlN-HEMT annealed, (c) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT as deposited, and (d) ~ 5 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT annealed.

Figure 6.12 shows the XPS O 1s spectra obtained for the ~ 5nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films on the InAlN/GaN HEMT samples before and after RTA. The O 1s spectrum has been decomposed into two components: O_I and O_{II}. The major O_I peak of lower binding energy is attributed to the Al-O-Al bonds from the oxide films, whereas the minor O_{II} peak located at higher binding energy is associated to Al-OH hydroxyl groups or oxygen absorbed species.[42] It has been reported that the presence of OH bonds associated with the O_{II} peak lead to excess oxygen and OH defects mainly located near the interface.[43] The results show a reduction of the O_{II}/O_I peak ratios for the annealed samples. The O_{II}/O_I area ratios calculated for the as-deposited Al_2O_3/InAlN/GaN HEMT and

$(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN/GaN HEMT samples are 0.22 and 0.25, respectively. After annealing, the O_{II}/O_I area ratios of the Al_2O_3/InAlN/GaN HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN/GaN HEMT samples decrease to 0.13 and 0.14, respectively. Therefore, the decrease in the O_{II}/O_I ratio at the oxide/InAlN interfaces can be attributed to a removal of excess oxygen and OH states during the annealing process,[14] which is consistent with the 'clean up' effect previously observed for ALD Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ samples grown on GaN-HEMTs after annealing.[44] This explains the shift to higher binding energies of the N 1s and Al 2p core levels and the reduction of the upward band bending at the oxide/InAlN interface observed in the previous section for the Al_2O_3/InAlN/GaN HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN/GaN HEMT samples.

6.3.3. Cross section and thermal stability of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics on InAlN/GaN HEMT structures

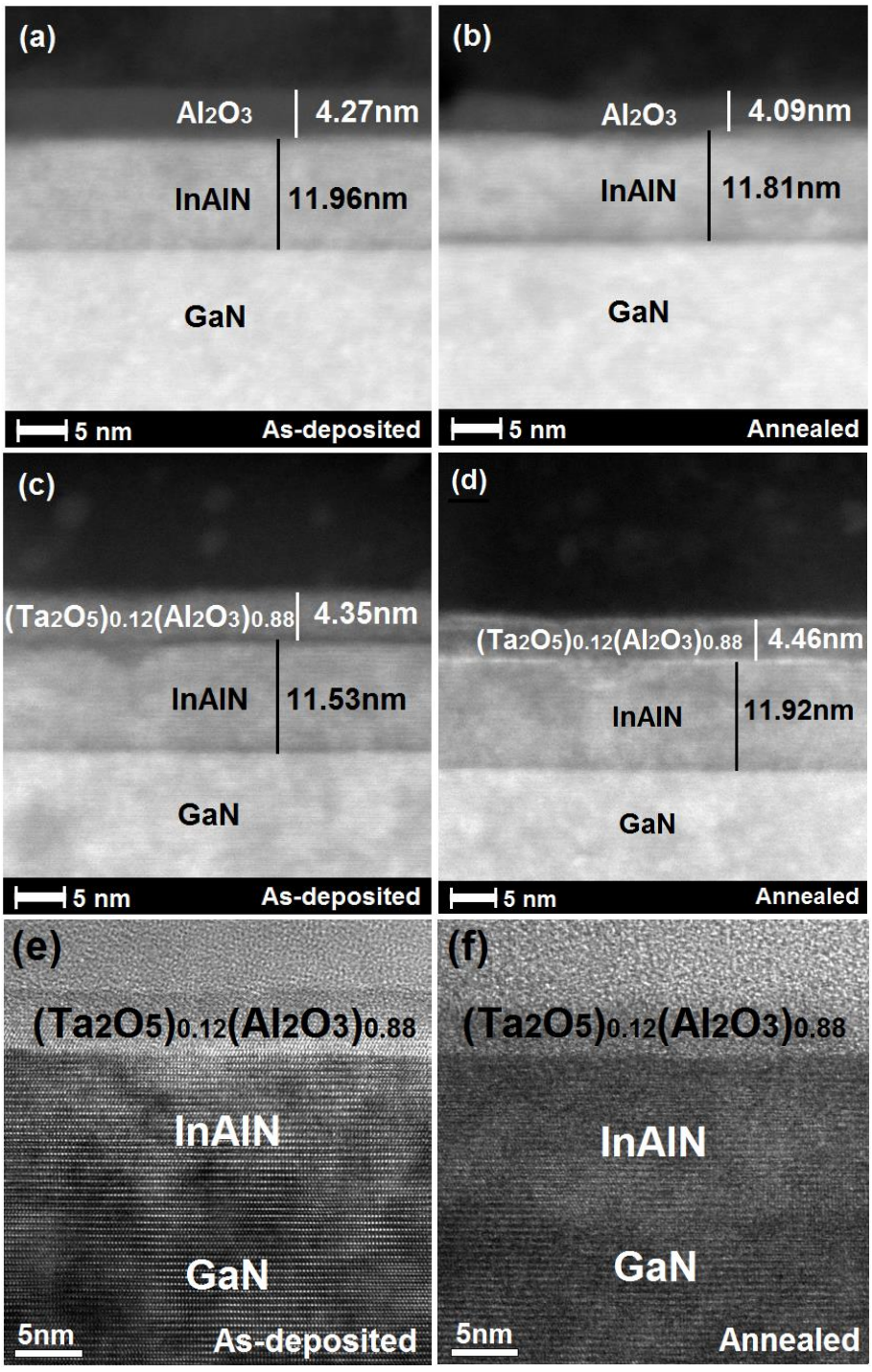

FIG. 6.13: (a)-(d) Cross-sectional HAADF-STEM of as-deposited and annealed Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers grown on the InAlN/GaN HEMT structure highlighting the top ALD oxide, InAlN barrier and GaN buffer layers; (e) and (f) represent cross-sectional HR-BFTEM of the as-deposited and annealed $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers grown on top of such HEMT structures.

Figures 6.13a-d show the cross-sectional HAADF-STEM images of the ~ 5 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers grown on the InAlN/GaN HEMT structure before and after annealing. The oxide films show uniform thickness within the samples, with a continuous and sharp interface with the InAlN barrier and no significant changes observed after annealing. Furthermore, HR-BFTEM performed for the HEMT samples coated with the ~ 5 nm thick $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers before and after annealing (Figs. 6.13e and 6.13f) shows that the interface between the amorphous oxide film and the crystalline InAlN/GaN structure shows good thermal stability with no interfacial layer observed. Therefore, the results demonstrate that the introduction of Ta does not affect the thermal stability of the investigated $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ oxide film after RTA at 600 ºC in N_2.

6.4. Conclusions

Post-deposition annealing in N_2 at 600 ºC can be used to improve the CBO of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as gate dielectrics for GaN-based HEMTs. The interfacial properties of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers grown on GaN-capped AlGaN/GaN and InAlN/GaN HEMT structures have been analysed before and after annealing in N_2 at 600 ºC. AFM shows that the surface morphology of the oxides deposited on the HEMT structures remains smooth after annealing. Cross-sectional STEM shows uniform oxide film thickness with continuous and sharp oxide/HEMT interfaces for all the samples before and after annealing. XPS results show that, for both the oxide/GaN-HEMT and oxide/InAlN-HEMT interfaces, the VBO and CBO of the as-deposited Ta-doped oxide decrease by 0.3 eV and 0.1 eV respectively compared to pure Al_2O_3. The VBOs of as-deposited Al_2O_3/GaN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT are 1.5 eV and 1.2 eV, respectively, with corresponding CBOs of 1.6 eV and 1.5 eV. The VBOs of

as-deposited Al_2O_3/InAlN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT are 1.2 eV and 0.9 eV, respectively, with corresponding CBOs of 0.8 eV and 0.7 eV. After annealing, all the samples are characterised by a reduction of excess interstitial oxygen defects at the oxide/nitride interface. This results in the decrease of the Al_2O_3/GaN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/GaN-HEMT VBOs to 0.3 eV and 0.1 eV, respectively, and the increase of the corresponding CBOs to 2.8 eV and 2.6 eV. For the Al_2O_3/InAlN-HEMT and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$/InAlN-HEMT samples, the VBOs decrease to 0.5 eV and 0.5 eV, respectively, and the corresponding CBOs increase to 1.5 eV and 1.1 eV. Furthermore, HR-TEM confirms that the introduction of Ta does not affect the thermal stability of the doped $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ film. Therefore, the post-deposition annealing step used during HEMT processing improves the interfacial characteristics of the samples by increasing the barrier height to the n-type HEMTs, giving potentially lower leakage currents. These results demonstrate that ALD of Al_2O_3 with Ta modulation doping can be used to achieve both a higher-κ and a sufficient CBO to the GaN-based HEMT structure for low leakage currents.

6.5. References

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7. Effect of ALD Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics on the characteristics of GaN/AlGaN/GaN MOSHEMTs

7.1. Introduction

This chapter presents a comparative study of the electrical characteristics of GaN-capped AlGaN/GaN HEMTs before and after the deposition of ~ 10 nm thick ALD Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films as gate dielectrics. Schottky gate HEMTs, Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs were fabricated using the same GaN/AlGaN/GaN structure to evaluate the effect of the introduction of the gate oxides on the performance of the devices.

CV measurements were carried out to investigate the effect of the gate oxides on the devices input characteristics. Compared to the Schottky HEMT, the gate-source capacitance of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs decreases due to the larger gate-to-channel separation, which is equivalent to a loss of channel control. This increase in the gate-to-channel separation together with the charge density created at the oxide/GaN interface after the deposition of the gate dielectrics cause an increase in the threshold voltage absolute value, increasing the power consumed during switching. This results in the increase in the 2DEG sheet carrier concentration in the active region of the MOSHEMTs, which is attributed to the oxides passivation effect that reduces the density of surface states. The impact of the use of the gate dielectrics on the devices output characteristics was also investigated. An improvement of the DC performance is observed for the MOSHEMTs from DC IV measurements: the maximum drain current, the saturation drain current and the saturation drain-source voltage increase, whereas the ON-resistance decreases. Gate transfer measurements show that, compared to the Schottky HEMT, the transconductance of the Al_2O_3 MOSHEMT decreases whereas the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$

MOSHEMT transconductance stays constant, which quantifies the devices ability to control the 2DEG. Although the MOSHEMTs ON-OFF drain current ratio decreases by one order of magnitude, the ON-state gate current is reduced by two orders of magnitude, which is attributed to the effective substitution of the gate Schottky barrier by a MOS structure. From OFF-state measurements, an increase of the breakdown voltage and a reduction of the gate leakage current is achieved for the MOSHEMTs structures compared to the Schottky HEMT. Furthermore, compared to the Al_2O_3 MOSHEMT, the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT can achieve a higher capacitance and a smaller threshold voltage absolute value, which is advantageous to improve the gate modulation efficiency and to reduce power consumption during switching. Higher maximum and saturation drain currents and lower ON-resistance values are obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT, which are associated with superior DC performance. In addition, its bigger maximum transconductance is directly related to the RF performance quality. Finally, although the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT shows a smaller breakdown voltage than the Al_2O_3 MOSHEMT, the OFF-state gate leakage current is reduced. Thus, the results demonstrate that the use of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ to increase the κ of Al_2O_3 as gate dielectric can achieve a lower OFF-state gate leakage current and a superior electrical performance, while still improving the OFF-state breakdown voltage with respect to the Schottky HEMT.

7.2. Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs fabricated on a GaN/AlGaN/GaN HEMT structure

The electrical characteristics of MOSHEMTs fabricated using ALD Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as gate dielectrics were compared to Schottky gate HEMTs manufactured using the same GaN/AlGaN/GaN HEMT structure. Figure 7.1 illustrates a

schematic of the Schottky gate GaN/AlGaN/GaN HEMT and the GaN/AlGaN/GaN MOSHEMT device structures used in the present study (Figs. 7.1a and 7.1b, respectively).

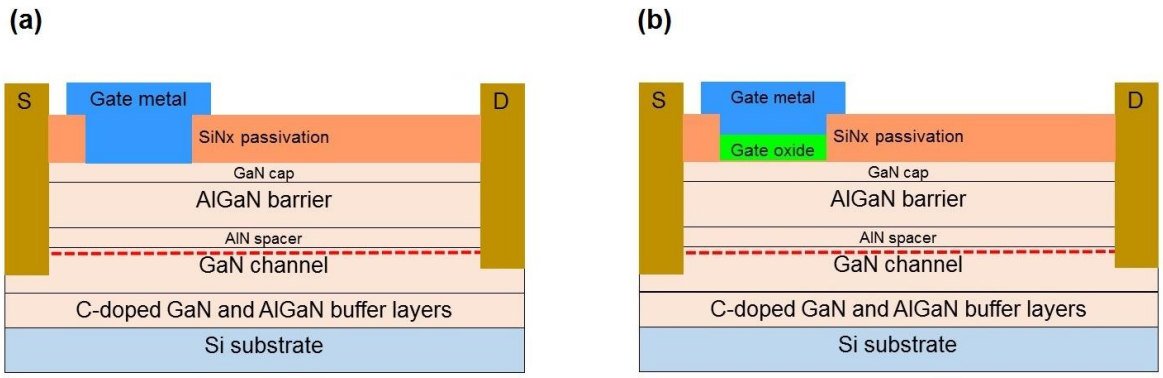

FIG. 7.1: Schematic of the cross section of the (a) Schottky gate GaN/AlGaN/GaN HEMT and (b) GaN/AlGaN/GaN MOSHEMT structures used in the present study.

The GaN-capped AlGaN/GaN HEMT was grown on a 150 mm diameter Si(111) substrate by MOCVD. The composition, crystalline quality and structural uniformity of the nitride epilayers across the wafer, as well as the thickness of the HEMT structure, were investigated by HRXRD (Table 7.1). The growth of the HEMT structure started with a thin AlN nucleation layer followed by four step-graded intermediate layers (AlGaN I-IV) with Al composition ranging from approximately 55 to 3%. Subsequently, an unintentionally carbon-doped GaN channel and an ultrathin AlN spacer were grown prior to the ~ 19-20 nm $Al_{0.23}Ga_{0.77}N$ HEMT barrier layer. Finally, the structure was capped with a ~ 2.0 nm thick undoped GaN cap. From Table 7.1 it can be observed that the nitride epilayers show good uniformity over the entire wafer. In addition, the average values of 517 and 1540 arcsec obtained for the GaN (002) and (102) rocking curve FWHM, respectively, are indicative of a high crystal quality device grade of the GaN layer.[1] The arithmetic average root mean square roughness measured using AFM in a 5 x 5 μm^2 scan area was 0.15 nm (Figure 7.2). Finally, from Hall-effect measurements at room temperature the sheet density of the

resultant 2DEG was in the order of ~ 7.1-7.7·10^{12} cm^{-2} and the electron mobility was about ~ 1300-1400 cm^2/Vs (Table 7.2).

TABLE 7.1. HRXRD parameters obtained from the centre, middle and edge of the GaN/AlGaN/GaN HEMT structure grown on a 150 mm diameter Si(111) substrate used in the present study.

GaN/AlGaN/GaN HEMT 367	Centre	Middle	Edge
Al content in AlGaN I buffer (%)	55.1	54.6	54.5
Al content in AlGaN II buffer (%)	37.0	35.9	35.7
Al content in AlGaN III buffer (%)	19.6	19.1	18.7
Al content in AlGaN IV buffer (%)	2.9	2.8	2.9
Al content in AlGaN barrier (%)	23.0	22.7	22.7
AlN space thickness (nm)	~ 0.7	~ 0.7	~ 0.7
AlGaN barrier thickness (nm)	19.9	20.3	18.2
GaN cap thickness (nm)	1.0	1.1	2.3
AlN 002 FWHM (arcsec)	1598	1514	1594
GaN 002 FWHM (arcsec)	525	503	522
GaN 102 FWHM (arcsec)	1509	1490	1621

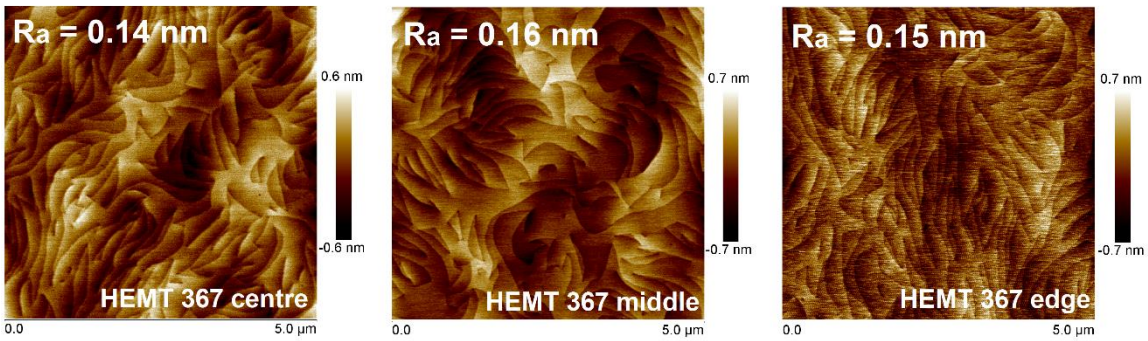

FIG. 7.2: 5.0 µm × 5.0 µm AFM surface images from the (a) centre, (b) middle and (c) edge of the GaN/AlGaN/GaN HEMT on Si(111) sample.

TABLE 7.2. 2DEG sheet density and electron mobility obtained from Hall measurements for the centre, middle and edge of the GaN/AlGaN/GaN HEMT structure grown on a 150 mm diameter Si(111) substrate used in the present study.

GaN/AlGaN/GaN HEMT 367	Centre	Middle	Edge
2DEG sheet density $_x10^{12}$ (cm^{-2})	7.1	7.1	7.7
Electron mobility (cm^2/Vs)	1390	1360	1380

7.3. Input characteristics

In order to investigate the effect of the dielectric layers on the devices input characteristics, CV measurements were carried out using a Schottky gate fatFET (Fig. 7.3a) and Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-fatFET (Fig. 7.3b) capacitor structures with a gate area of 100 µm by 160 µm.

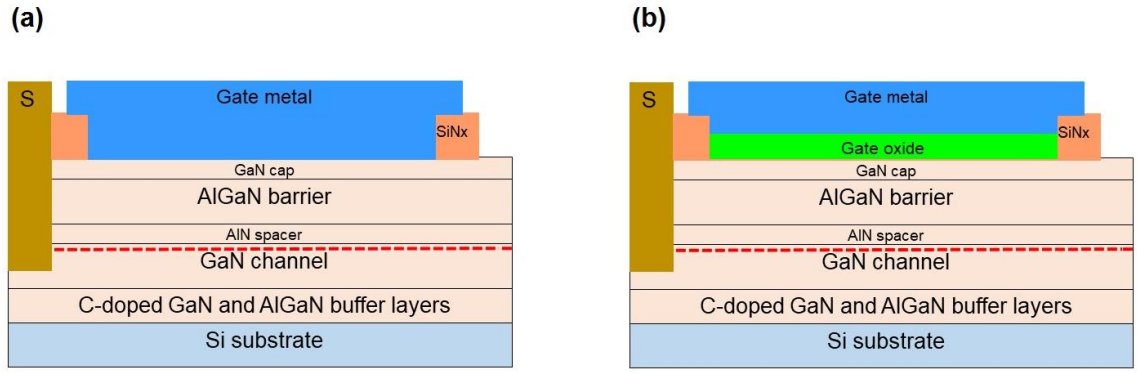

FIG. 7.3: Schematic of the cross section of the (a) Schottky gate fatFET and (b) MOS-fatFET structures.

7.3.1. Gate-source capacitance and threshold voltage

The gate-source capacitance (C_{GS}) is one of the key figures to describe the input behaviour of a HEMT. The Schottky HEMT gate-source capacitance (C_{GS}^{HEMT}) is the capacitance of a structure consisting of the gate electrode, the semiconducting layers between the gate and the source, and the source electrode (Fig.7.3a). It can be modelled as

a series of the capacitance of the AlN spacer (C_{AlN}), the AlGaN barrier (C_{AlGaN}) and the GaN cap (C_{GaN}):

$$\frac{1}{C_{GS}^{HEMT}} = \frac{1}{C_{AlN}} + \frac{1}{C_{AlGaN}} + \frac{1}{C_{GaN}} \tag{7.1}$$

where $C_{AlN}=\kappa_{AlN}\cdot\varepsilon_0\cdot A/t_{AlN}$, $C_{AlGaN}=\kappa_{AlGaN}\cdot\varepsilon_0\cdot A/t_{AlGaN}$ and $C_{GaN}=\kappa_{GaN}\cdot\varepsilon_0\cdot A/t_{GaN}$.

For the MOSHEMT structures with an additional dielectric layer between the gate electrode and the semiconductor (Fig.7.3b), the gate-source capacitance ($C_{GS}^{MOSHEMT}$) is assumed to form a series capacitance with the HEMT capacitance described above:

$$\frac{1}{C_{GS}^{MOSHEMT}} = \frac{1}{C_{GS}^{HEMT}} + \frac{1}{C_{ox}} \tag{7.2}$$

where $C_{ox}=\kappa_{ox}\cdot\varepsilon_0\cdot A/t_{ox}$.

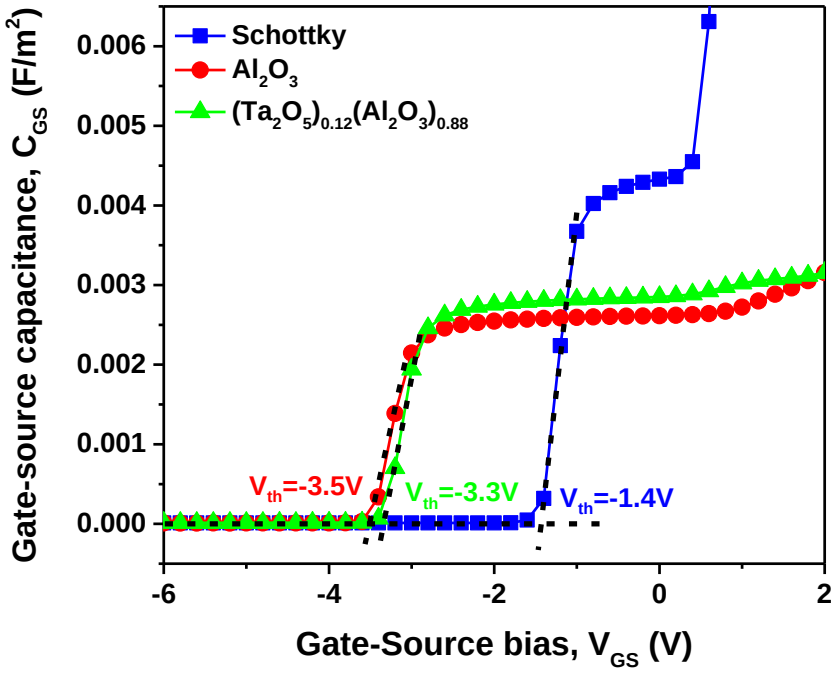

FIG. 7.4: CV measurements at 10 kHz for the ~ 100x160 μm^2 area Schottky gate fatFET and MOS-fatFET structures fabricated with ~ 10 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate oxides.

Figure 7.4 shows the C_{GS} of the Schottky gate fatFET and the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-fatFETs obtained as a function of the gate-source voltage (V_{GS}). The CV measurements were carried out at 10 kHz with the V_{GS} swept from – 6 V to + 2 V. It should be noted that for the Schottky HEMT the gate capacitance dramatically increased when the devices were swept beyond 0 V. This is attributed to a high forward bias current caused by a decrease of the barrier layer effective thickness due to a charge overflow from the 2DEG channel.[2] The measurements show that the maximum capacitance is significantly reduced for the MOSHEMTs. The C_{GS} obtained for the Schottky gate structure is $4.3 \cdot 10^{-3}$ F/m^2. For the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs, the C_{GS} values are $2.6 \cdot 10^{-3}$ F/m^2 and $2.8 \cdot 10^{-3}$ F/m^2, respectively. This reduction in the C_{GS} after the deposition of the gate oxides is attributed to the larger gate-to-channel separation and different effective potential barrier height that makes the MOSHEMTs channel depletion smaller than that for the HEMT for the same gate voltage.[3] Using the C_{GS} values measured in this section and equation 7.2, the κ values calculated for the ~ 10 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers are 7.2 and 9.8, respectively. These values are in good agreement with the κ values of 8.5 ± 1.5 and 12.6 ± 2.3 determined for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films at 10 kHz in section 5.3, which means that the model used is a suitable method to numerically evaluate the effect of the use of gate oxides on the MOSHEMTs capacitance. Furthermore, the results show that the C_{GS} obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT is higher than the C_{GS} of the Al_2O_3 MOSHEMT, which demonstrates that the use of a gate dielectric with a higher κ can increase the gate capacitance while maintaining the dielectric thickness to prevent gate leakage.

The threshold voltage (V_{th}) values can be linearly extracted from the CV characteristics. From figure 7.4, a negative shift in the V_{th} can be observed for the MOSHEMT structures. The V_{th} decreases from – 1.4 V for the Schottky HEMT to – 3.5 V and – 3.3 V for the Al_2O_3

and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs, respectively. This shift in the MOSHEMTs V_{th} is attributed to the increased gate-to-channel separation that causes the reduction of the C_{GS}.[4] Since C_{GS} describes the ability to change the 2DEG sheet carrier concentration by changing the V_{GS}, the reduction of C_{GS} is equivalent to a reduction in the ability to deplete the 2DEG channel of confined electrons and to suppress the flow of current in the channel from source to drain for an applied bias. Thus, a higher V_{GS} is required to deplete the 2DEG of the MOSHEMTs, which is reflected by a bigger V_{th} absolute value. For normally ON devices like the ones characterised in this study, this implies that the lower the C_{GS} the more negative the V_{th} is, which is in agreement with the results obtained. Assuming the same sheet charge density in the channel for the HEMT and MOSHEMT devices at zero gate bias and not taking into account the surface charge at the oxide/GaN interface, the V_{th} absolute value of the MOSHEMTs ($V_{th}^{MOSHEMT}$) increases with respect to that of the HEMT (V_{th}^{HEMT}) as follows:[4]

$$Q_S = q\,N_S = C_{GS}^{MOSHEMT} \cdot V_{th}^{MOSHEMT} = C_{GS}^{HEMT} \cdot V_{th}^{HEMT} \tag{7.3}$$

$$V_{th}^{MOSHEMT} = V_{th}^{HEMT}\left(\frac{C_{GS}^{HEMT}}{C_{GS}^{MOSHEMT}}\right) \tag{7.4}$$

where Q_S is the charge at the metal/oxide and metal/semiconductor interfaces and N_S is the 2DEG sheet carrier density.

According to equation 7.4, the V_{th} values calculated for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs are – 2.3 V and – 2.1 V, respectively, which are 1.2 eV bigger than the experimental values of – 3.5 V and – 3.3 V obtained experimentally. The difference between the experimental values and the values obtained using equation 7.4 is attributed to the charge ($\Delta Q = C\Delta V$) induced at the oxide/GaN interfaces due to interface and/or bulk oxide traps created after the deposition of the gate oxides.[3, 4, 5] Therefore, the

negative shift observed in the MOSHEMTs V_{th} compared to the Schottky HEMT V_{th} is caused by the charge density created at the oxide/GaN interface in addition to the larger gate-to-channel separation. Furthermore, since the V_{th} shift caused by the interface charge is the same for both the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs, the results indicate that the smaller negative V_{th} obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT in comparison to the Al_2O_3 MOSHEMT is related to the bigger C_{GS} achieved using a higher κ gate dielectric. This means that a smaller negative voltage bias is required to deplete the 2DEG channel and to suppress the current flow, which is relevant for the use of gate dielectrics in MOSHEMTs because the smaller V_{th} absolute value implies a lower amount of power consumed during the ON/OFF state transition.

7.3.2. 2DEG sheet carrier concentration

The C_{GS} can be used to define the 2DEG sheet carrier concentration (n_s) of a HEMT. The approximation of the n_s for a constant gate bias and low electric fields is given by a simple HEMT analytical model by Thayne et al.:[6]

$$n_s = \frac{C_{GS}}{q \cdot L_G \cdot W_G}[V_{GS} - V_{th}] \tag{7.5}$$

where L_G is the gate length and W_G is the gate width.

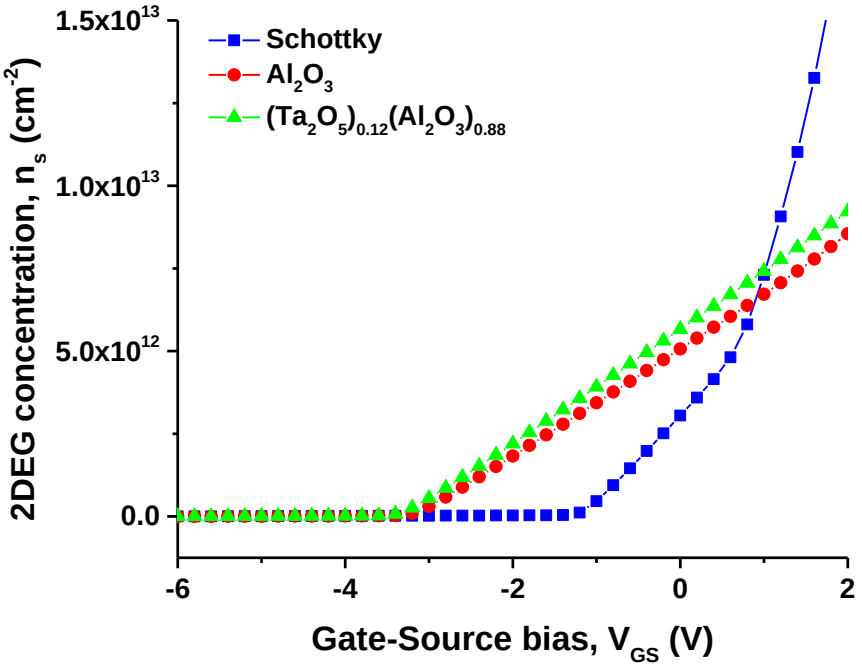

FIG. 7.5: n_s as a function of the V_{GS} obtained for the Schottky gate fatFET and MOS-fatFET structures fabricated with ~ 10 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate oxides.

Figure 7.5 shows the n_s of the three devices as a function of the V_{GS}. The results show that n_s is a linear function of V_{GS} for voltages beyond the V_{th}, which is in agreement with equation 7.5. For the Schottky HEMT, a higher rate of n_s increase is observed for V_{GS} values above 0 V. This corresponds to the increase of the C_{GS} previously observed for the HEMT, attributed to a charge overflow from the 2DEG channel.[2] It can be observed that the n_s of the MOSHEMTs is higher than the n_s of the Schottky HEMT for voltages $V_{th} < V < 0$. At $V_{GS} = 0$ V, the n_s obtained for the Schottky HEMT is $3.1 \cdot 10^{12}$ cm^{-2}, whereas the n_s of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs are $5.1 \cdot 10^{12}$ cm^{-2} and $5.7 \cdot 10^{12}$ cm^{-2}, respectively. From equation 7.5, the higher n_s measured in the active region of the MOSHEMTs can be explained by the fact that the reduction of C_{GS} does not exactly correspond to the increase of the V_{th}. For the Al_2O_3 MOSHEMT, the C_{GS} decreases by ~ 40 % whereas the V_{th} absolute value increases by 150 % with respect the Schottky HEMT, and for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT, the C_{GS} decreases by ~ 35 %

whereas the V_{th} absolute value increases by 136 %. Therefore, the experimental increase observed for the MOSHEMTs n_s is in accordance with the simple HEMT analytical model described in equation 7.5.[6] Furthermore, the n_s obtained for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs when V_{GS} = 0 V are ~ 65 % and ~ 84 % higher than the Schottky HEMT n_s, respectively. Since the increase in n_s after the gate oxides deposition is believed to be a result of the oxides passivation effect which reduces the density of surface states and leads to less electron depletion in the 2DEG channel,[7, 8] the results indicate that the use of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as gate dielectric can achieve a more positive effect in the device n_s compared to Al_2O_3.

Finally, from equation 7.5 the slope of the n_s can be approximated as:[5]

$$\frac{\partial n_s}{\partial V_{GS}} = \frac{C_{GS}}{q \cdot L_G \cdot W_G} \tag{7.6}$$

Thus, the decrease in the n_s slope observed for the MOSHEMTs (Fig. 7.5) is also in agreement with the simple HEMT analytical model, corresponding to the smaller C_{GS} obtained after the use of the gate dielectrics.

7.4. Output characteristics

The output DC IV characteristics of the Schottky HEMT and the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs were determined in order to model the influence of the dielectric layers on the electrical behaviour of the transistors.

7.4.1. Drain current

The drain current (I_D) is the key figure to describe the DC output characteristic of a HEMT. It can be described as:[9]

$$I_D = q \cdot L_G \cdot n_s \cdot v \tag{7.7}$$

where v is the 2DEG charge carrier velocity.

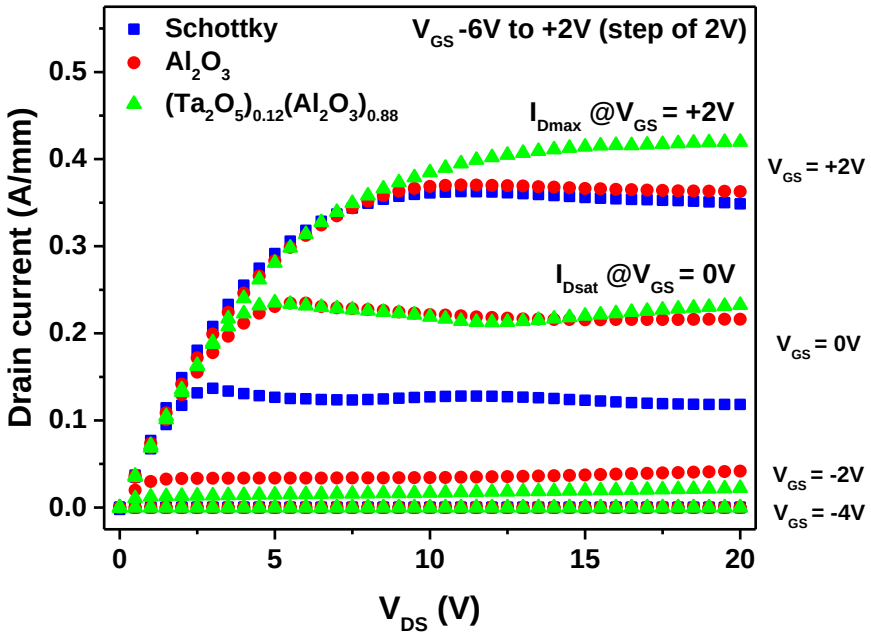

FIG. 7.6: Output characteristics of the Schottky HEMT and the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs showing I_D-V_{DS} for varying V_{GS} between – 6 V and + 2 V in steps of + 2 V.

Figure 7.6 shows a comparison of the I_D plotted over the drain-source voltage (V_{DS}) for various V_{GS} values between – 4 V and + 2 V, in steps of 2 V. The pinch-off voltage is – 2 V for the Schottky HEMT and – 4 V for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs. It can be observed that in some cases, after reaching the maximum value the drain current of the devices decreases as V_{DS} increases. This is due to self-heating as a result of the poor thermal conductivity of the Si substrate.[10] The MOSHEMTs show an improvement in the maximum drain current at positive gate bias. When a V_{GS} = + 2 V is applied, the I_D measured for the Schottky HEMT is 0.36 A/mm, and the I_D of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs are 0.37 A/mm and 0.42 A/mm, respectively. Considering equation 7.7, the experimental increase in the I_D obtained for the MOSHEMTs is probably caused by the increase in the n_s after the introduction of the gate oxides. This

is in agreement with the CV analysed in the previous section, which has showed that the use of the gate dielectrics causes the sheet carrier concentration of the active region of the device to rise significantly for a given gate bias (Fig. 7.5). Therefore, it can be concluded that the higher n_s obtained after the use of gate oxides is likely to be the main reason for the increase of I_D. Furthermore, the I_D increase observed for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs with respect to the Schottky HEMT are 3 % and 17 % when V_{GS} = 2 V, respectively. Thus, the use of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ to increase the dielectric constant of Al_2O_3 as gate dielectric further improves the DC output characteristics of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT by significantly increasing the maximum drain current at positive gate bias.

7.4.2. Drain saturation current

Using a more advanced model to describe the basic DC characteristics of an ideal HEMT proposed by Das,[11] the drain current, the drain saturation current ($I_{D,sat}$) and the drain source saturation voltage ($V_{DS,sat}$) can be expressed as follows:

$$I_D = \frac{C_{GS}}{L_G}\left([V_{GS} - V_{th}] \cdot \mu_o \cdot \frac{V_{DS}}{L_G} - \mu_o \cdot \frac{V_{DS}^2}{2\,L_G}\right) \cdot \left(1 + \frac{V_{DS}}{V_C}\right)^{-1} \tag{7.8}$$

$$I_{D,sat} = \frac{C_{GS}}{L_G}\left(V_{GS} - V_{th} - V_{DS,sat}\right) \cdot v_{sat} \tag{7.9}$$

where:

$$V_{DS,sat} = \sqrt{V_c^2 + 2V_c \cdot [V_{GS} - V_{th}]} - V_c \tag{7.10}$$

where μ_o is the field mobility of the 2DEG carriers, v_{sat} is the 2DEG charge carrier saturation velocity defining the critical field (E_{cr}) as the electrical field at which the carrier

velocity attains half of its saturation velocity (given by $v_{sat} = \mu_o \cdot E_{cr}$) and V_{cr} is the critical voltage given by $V_c = L_G \cdot E_c$.

From figure 7.6, an increase in the $I_{D,sat}$ at V_{GS} = 0 V is observed for the MOSHEMTs. This increase of the MOSHEMTs $I_{D,sat}$ is accompanied with a shift in the $V_{DS,sat}$. The $I_{D,sat}$ of the Schottky HEMT is found to be 0.14 A/mm at $V_{DS,sat}$ = 3 V, whereas the $I_{D,sat}$ obtained for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs are 0.23 A/mm and 0.24 A/mm at $V_{DS,sat}$ = 5.5 V and $V_{DS,sat}$ = 5 V, respectively. These results are in agreement with the HEMT DC model, according to which the decrease in C_{GS} with accompanying increase in V_{th} after the introduction of the gate oxides results in a higher $I_{D,sat}$ (Eq. 7.9) and a significant shift in the $V_{DS,sat}$ (Eq. 7.10). It has been reported that the saturation current value depends on the gate oxide and that the MOSHEMT $I_{D,sat}$ increases by a factor of approximately $C_{GS}^{MOSHEMT}/C_{GS}^{HEMT}$ for zero or small positive gate voltage bias.[12] This is in agreement with the results obtained in this study. The $C_{GS}^{MOSHEMT}/C_{GS}^{HEMT}$ values obtained for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs in the previous section were 0.60 and 0.65, respectively, which are very close to the increase of 64 % and 71 % observed for the $I_{D,sat}$ when V_{GS} = 0 V. Furthermore, it has also been reported that the increase in the MOSHEMT $V_{DS,sat}$ is close to the absolute value of the V_{th} shift,[12] which is also in agreement with the results. In the previous section, the V_{th} shift for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs were – 2.1 V and – 1.9 V, which are similar to the $V_{DS,sat}$ increase of 2.5 V and 2.0 V observed in this section. Since the DC saturation current is a key parameter in establishing the maximum RF power output for HEMT devices, the results confirm that the use of the gate oxides improves the DC saturation characteristics of the MOSHEMTs by increasing the saturation current and enabling the use of a higher positive gate voltage. The $I_{D,sat}$ achieved for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT is

bigger than the $I_{D,sat}$ of the Al_2O_3 MOSHEMT. However, the $V_{DS,sat}$ obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT is smaller than the Al_2O_3 MOSHEMT $V_{DS,sat}$. Although the increase in the $V_{DS,sat}$ is desirable to enable the use of a higher positive gate voltage, the smaller increase in the $V_{DS,sat}$ is related to a smaller V_{th} shift towards negative values, which is also beneficial to reduce the power consumption during switching.

7.4.3. ON resistance

The ON-resistance (R_{ON}) is another key figure for HEMT switching devices. The specific ON-resistance ($R_{ON,sp}$) is defined as the R_{ON} multiplied by the device active area defined as:

$$A = (L_{GS} \cdot L_G \cdot L_{GD}) \cdot W_G \tag{7.11}$$

where L_{GS} is the gate-source separation and L_{GD} is the gate-drain separation.

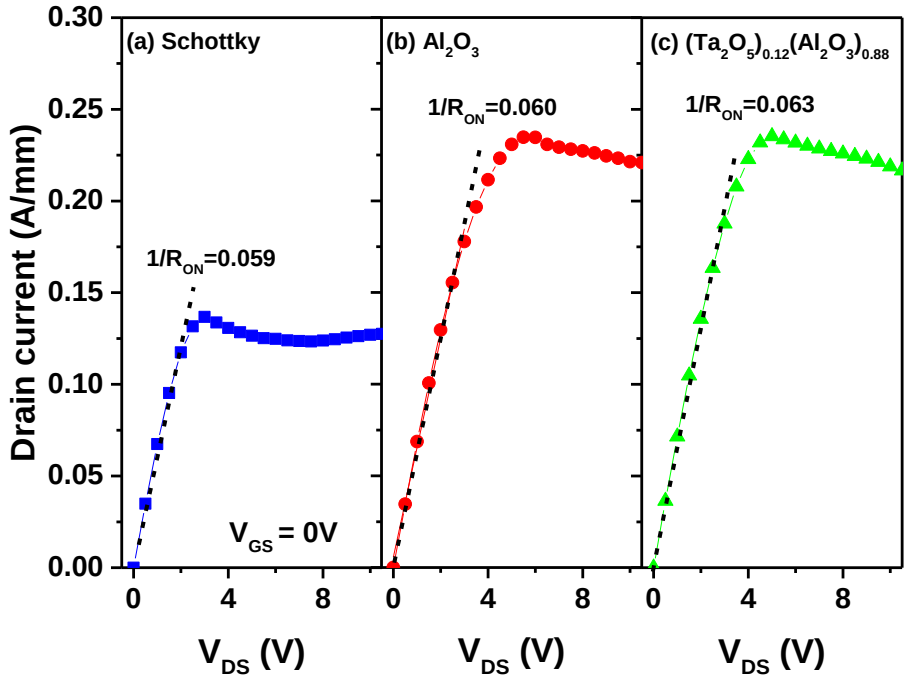

FIG. 7.7: Linear region of the output I_D-V_{DS} characteristics when V_{GS} = 0 V for (a) the Schottky HEMT, (b) the Al_2O_3 MOSHEMT and (c) the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT.

Figure 7.7 shows a comparison of the devices $1/R_{ON}$ value extrapolated from the linear region of the I_D-V_{DS} curves when V_{GS} = 0 V. According to equation 7.9, the $R_{ON,sp}$ decreases from 2.7 mΩ·cm^2 for the Schottky HEMT to 2.67 mΩ·cm^2 and 2.54 mΩ·cm^2 for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs, respectively. The $1/R_{ON}$ ratio is directly related to the efficiency of power devices.[13] Therefore, the results suggest that the introduction of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics has a slightly positive effect on the device R_{ON} value when V_{GS} = 0 V, with a better $1/R_{ON}$ ratio obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT compared to the Al_2O_3 MOSHEMT.

7.5. Gate transfer characteristics

In order to further investigate the effect of the gate dielectrics on the devices output characteristics, gate-transfer measurements were performed to analyse the transconductance and the output currents of the three devices as a function of the V_{GS}.

7.5.1. Transconductance

The gate transconductance is one of the most widely used figures of merit for HEMTs to quantify the ability to control the 2DEG channel. Differentiating the saturated drain current (Eq. 7.9) with respect to the gate-source voltage gives the HEMT intrinsic transconductance (g_m):[11]

$$g_m = \frac{C_{GS}}{L_G}\left(1 - \left(1 + 2\cdot\frac{V_{GS} - V_{th}}{V_{cr}}\right)^{-\frac{1}{2}}\right)\cdot v_{sat} \qquad (7.12)$$

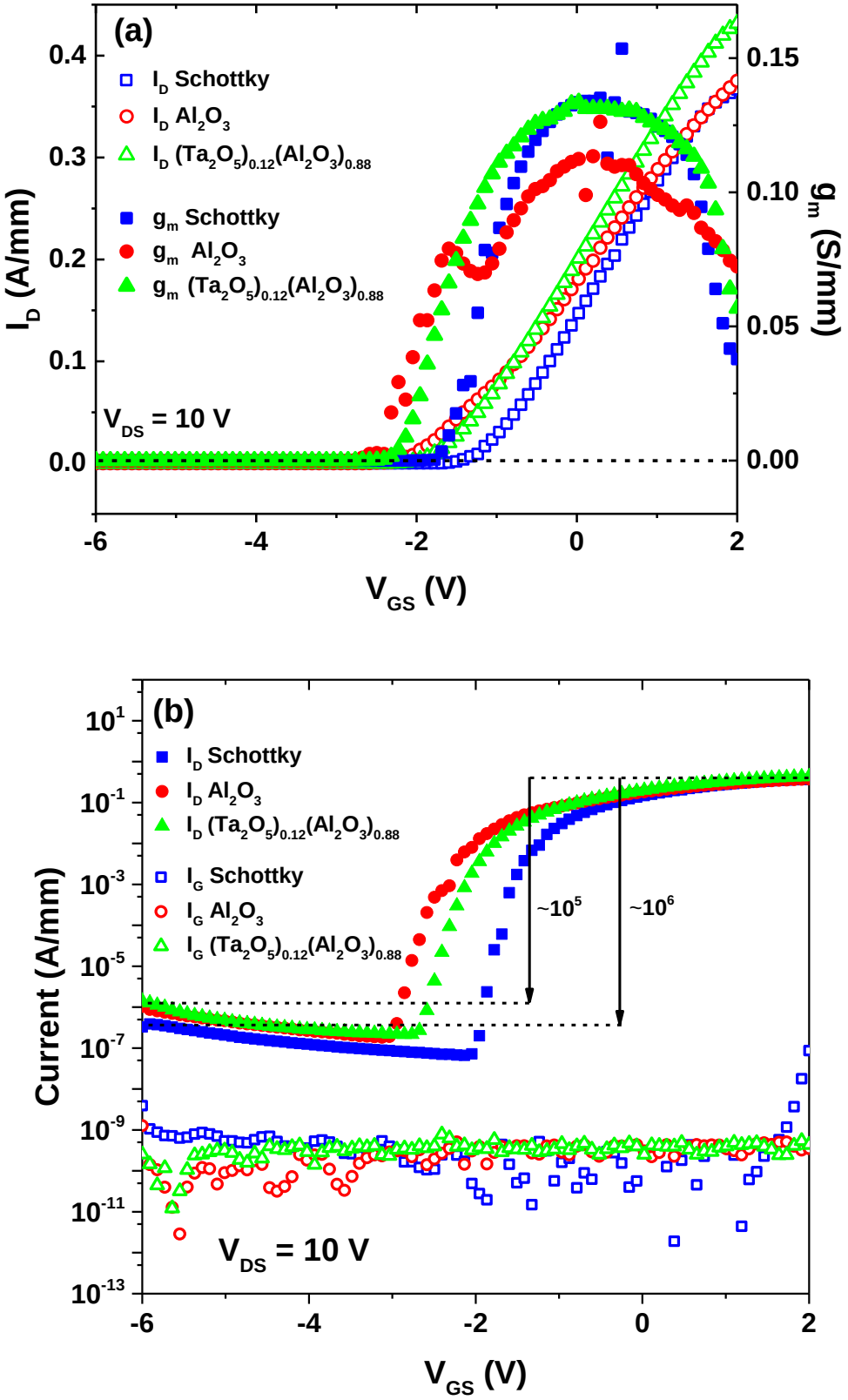

FIG. 7.8: (a) Output I_D and g_m and (b) I_D and I_G of the Schottky HEMT and the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs with V_{DS} = + 10 V and V_{GS} sweeps from – 6 V to + 2 V.

Figure 7.8a shows a comparison of I_D and g_m as a function of V_{GS}, obtained sweeping V_{GS} from – 6 V to + 2 V with V_{DS} kept at 10 V. g_m was extracted by differentiating I_D with respect V_{GS}. It can be observed that the maximum transconductance ($g_{m,max}$) is smaller for the Al_2O_3 MOSHEMT. The $g_{m,max}$ obtained for the Schottky HEMT and the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT is 0.13 S/mm, whereas for the Al_2O_3 MOSHEMT the $g_{m,max}$ decreases to 0.11 S/mm. It can also be noted that the g_m of the Al_2O_3 MOSHEMT exhibits a second peak. This indicates the presence of a parasitic current path beyond the 2DEG channel which could be avoided with further optimisation of the device fabrication process.[14] Taking into account equation 7.12, a decrease in the gate-source capacitance due to the introduction of a dielectric layer results in a smaller decrease of the transconductance ($g_m < C_{GS}/L_G \cdot v_{sat}$). In the case of the Al_2O_3 MOSHEMT, the measured g_m value shows a reduction with respect the Schottky HEMT g_m, which is in agreement with the HEMT DC model. However, the results show identical g_m values for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT and the HEMT. This could be due to the fact that the decrease in the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT g_m due to the C_{GS} decreasing effect may be compensated by the V_{th} absolute value increase. The gate transconductance critically affects the cut-OFF frequency (f_T) and the maximum frequency (f_{max}) of the device,[13] which are proportional to g_m and inversely proportional to C_{GS} ($f_T, f_{max} \propto g_m/C_{GS}$).[6] Therefore, the bigger g_m obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT in comparison to the Al_2O_3 MOSHEMT is a very important indicator of the superior device quality for microwave applications.

Figure 7.8b illustrates the output I_D and gate current (I_G) (in log scale) as a function of the V_{GS} when V_{DS} = + 10 V. The I_D ON-OFF ratio obtained for the Schottky HEMT is ~ 10^6 A/mm. For both the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs, the ON-OFF current ratio decreases by one order of magnitude to ~ 10^5 A/mm due to their higher

OFF-state drain leakage currents. The Schottky HEMT I_D is below $4 \cdot 10^{-7}$ A/mm when V_{GS} is – 6 V, whereas the I_D of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs is below $2 \cdot 10^{-6}$ A/mm when V_{GS} is – 6 V. The ON-OFF current ratio is another figure of merit used for transistors and thus the results indicate that the introduction of gate dielectrics adversely affects the MOSHEMTs ON-OFF I_D ratio. On the other hand, a reduction of two to three orders of magnitude is observed for the MOSHEMTs ON-state I_G. The I_G of the Schottky HEMT is ~ $8.7 \cdot 10^{-8}$ A/mm when V_{GS} is + 2 V, whereas the I_G at V_{GS} = + 2 V of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs is below ~ $3.5 \cdot 10^{-10}$ A/mm and ~ $4.4 \cdot 10^{-10}$ A/mm, respectively. This MOSHEMTs ON-state I_G reduction can be attributed to the substitution of the gate Schottky barrier by a more effective MOS structure to reduce gate leakage.[2]

7.6. OFF-state breakdown properties

OFF-state breakdown measurements were carried out to investigate the effect of the gate dielectrics on the devices OFF-state leakage currents.

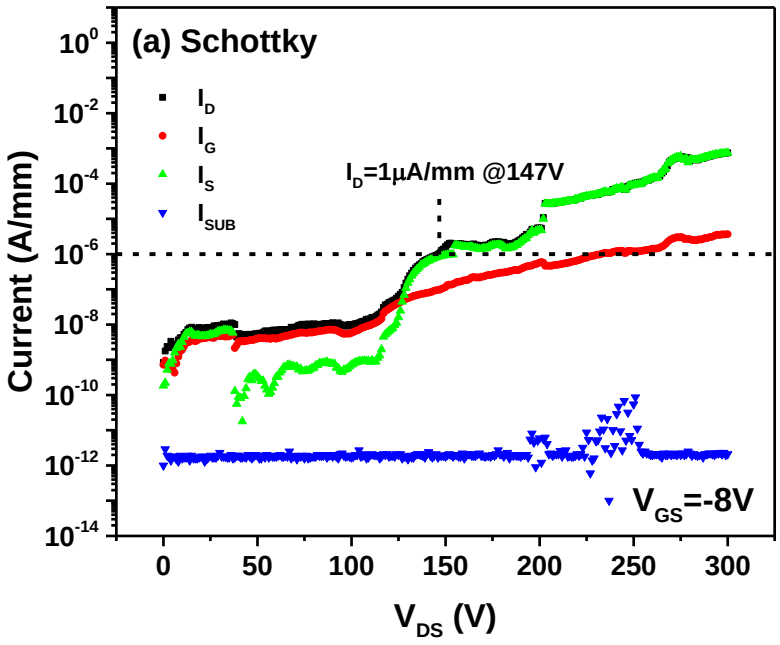

FIG. 7.9: (a) Three-terminal OFF-state measurements of the Schottky HEMT with V_{GS} = – 8 V and V_{DS} sweeping from – 0 V to + 300 V.

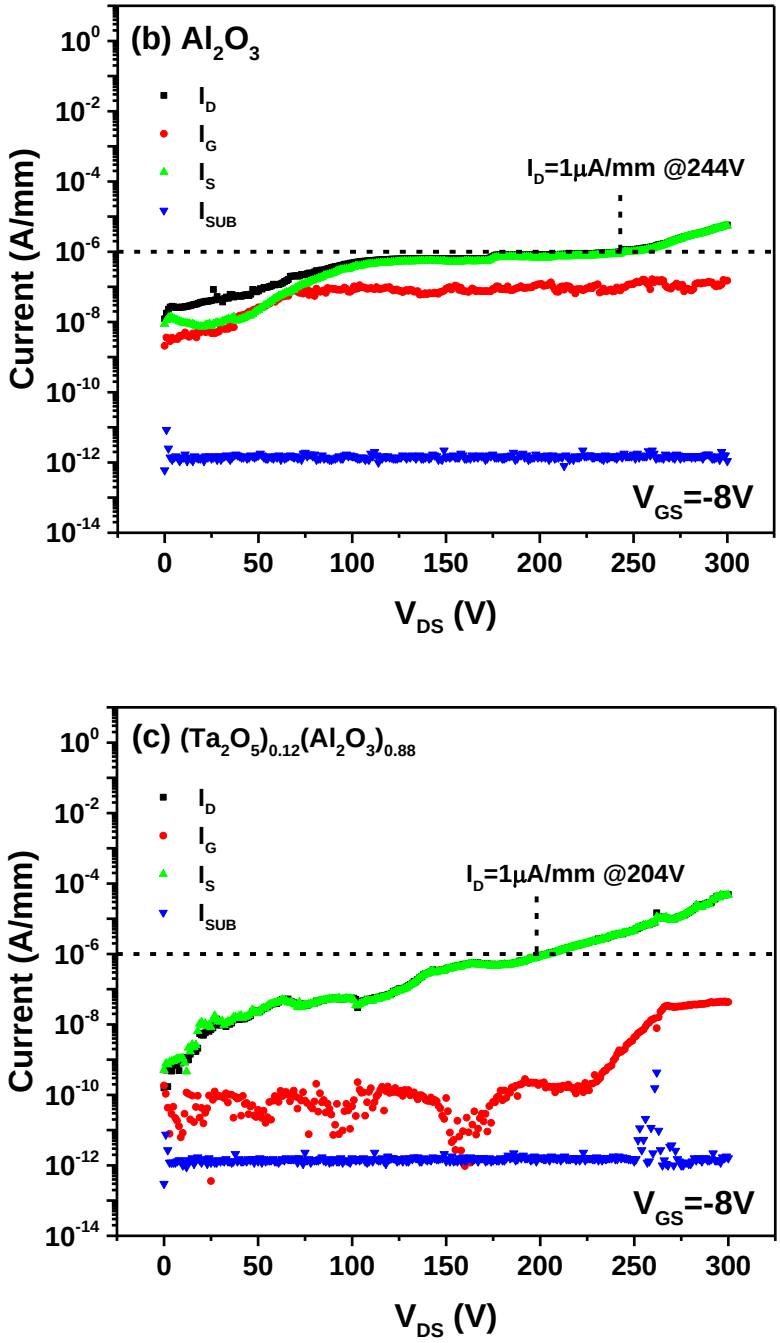

FIG. 7.9 (cont.): Three-terminal OFF-state measurements of the (b) Al_2O_3 MOSHEMT and (c) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT with V_{GS} = – 8 V and V_{DS} sweeping from – 0 V to + 300 V.

Figures 7.9a-c show the OFF-state IV characteristics (in log-linear scale) of the three devices obtained sweeping V_{DS} from 0 V to 300 V with V_{GS} kept at – 8 V. The OFF-state breakdown properties were evaluated by three-terminal breakdown tests with the samples substrates un-grounded during the measurements. A significant improvement of the voltage

blocking capability is observed for the MOSHEMTs structures compared to the Schottky HEMT. To avoid permanent degradation of the devices, the breakdown voltage (V_B) is defined as the voltage at which the OFF-state current exceeds 1 µA/mm. The V_B of the Schottky HEMT is found to be 147 V at I_D = 1 µA/mm (Fig. 7.9a), whereas the V_B values obtained for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs are 244 V and 204 V at I_D = 1 µA/mm, respectively (Figs. 7.9b and 7.9c). The V_B value is a fundamental parameter as the V_B^2/R_{ON} ratio is considered to be a figure of merit of a power device.[13] Thus, the use of the ~ 10 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics can achieve improvements of 66 % and 39 % with respect the V_B value obtained for the Schottky HEMT, respectively. The smaller V_B value obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT is expected considering the smaller breakdown electric field of Ta_2O_5 with respect Al_2O_3.[15, 16]

From Figure 7.9a, it can be observed that the gate leakage current of the Schottky gate HEMT structure dominates when V_{DS} is below 130 V, and the leakage between the source and the drain terminals (I_S) overtakes I_G for voltages above 130 V. Furthermore, the gate leakage current surpasses 1 µA/mm for voltages above 233 V. For the MOSHEMTs (Figs. 7.9b and 7.9c), I_G is smaller than I_S up to 300 V. This means that the gate leakage current is not the main source of leakage in the MOSHEMTs for the range of V_{DS} measured. In addition to this, I_G remains below 1 µA/mm up to 300 V.

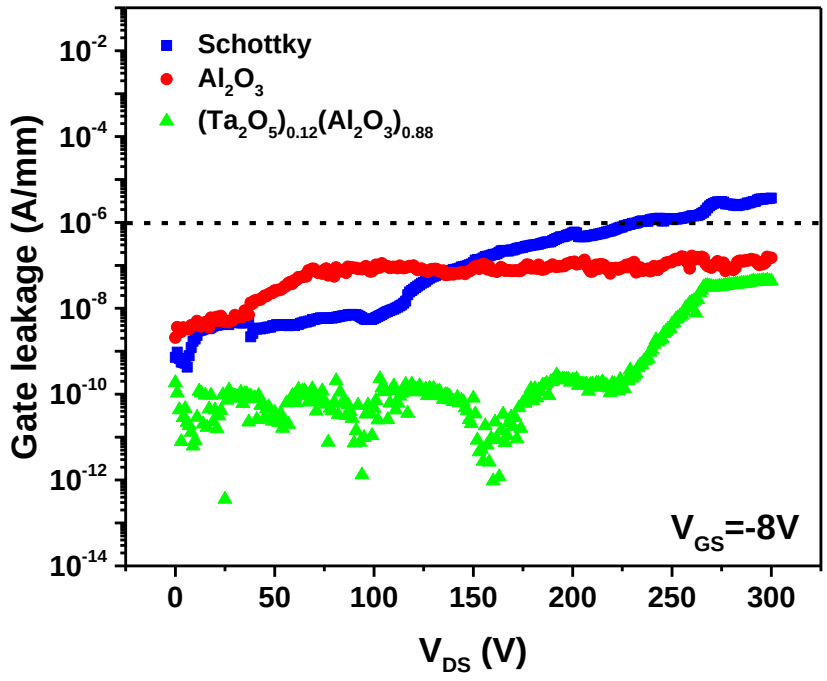

FIG. 7.10: OFF-state gate leakage of the Schottky HEMT and the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs with V_{GS} = – 8 V and V_{DS} sweeping from – 0 V to + 300 V.

Figure 7.10 shows a comparison of the OFF-state gate leakage currents (in log scale) of the three devices. The I_G measurements show that, compared to the Schottky HEMT, the gate leakage current of the MOSHEMTs significantly decreases at V_{DS} = 300 V. For the Schottky gate device, the I_G at V_{DS} = 300 V is found to be below $4 \cdot 10^{-6}$ A/mm, whereas the I_G of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs are under $1.5 \cdot 10^{-7}$ A/mm and $4.3 \cdot 10^{-8}$ A/mm at V_{DS} = 300 V, respectively. Thus, both Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics significantly reduce the gate leakage current of the MOSHEMTs with respect to the Schottky HEMT, with a reduction of over one order of magnitude achieved with the use of ~ 10 nm Al_2O_3 gate dielectric and a higher reduction of over two orders of magnitude achieved with ~ 10 nm $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectric.

TABLE 7.3. Summary of the Schottky gate HEMT and the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs electrical characteristics.

Device parameter	Schottky HEMT	Al_2O_3 MOSHEMT	$(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT
C_{GS} (F/m^2)	$4.3\cdot10^{-3}$	$2.6\cdot10^{-3}$	$2.8\cdot10^{-3}$
V_{th} (V)	– 1.4	– 3.5	– 3.3
n_s @ V_{GS} = 0 V (cm^{-2})	$3.1\cdot10^{12}$	$5.1\cdot10^{12}$	$5.7\cdot10^{12}$
I_D @ V_{GS} = + 2 V (A/mm)	0.36	0.37	0.42
$I_{D,sat}$ @ V_{GS} = 0 V (A/mm)	0.14	0.23	0.24
$V_{DS,sat}$ @ V_{GS} = 0 V (V)	3	5.5	5
R_{ON} @ V_{GS} = 0 V (Ω·mm)	16.9	16.7	15.9
$g_{m,max}$ (S/mm)	0.13	0.11	0.13
ON-OFF I_D ratio (A/mm)	~ 10^6	~ 10^5	~ 10^5
I_G @ V_{GS} = + 2 V (A/mm)	~ $8.7\cdot10^{-8}$	~ $3.5\cdot10^{-10}$	~ $4.4\cdot10^{-10}$
OFF V_B at I_D = 1 µA/mm (V)	147	244	204
OFF I_G @V_{DS} = 300 V (A/mm)	~ $4\cdot10^{-6}$	~ $1.5\cdot10^{-7}$	~ $4.3\cdot10^{-8}$

Table 7.3 shows the device characteristics obtained for the Schottky HEMT and the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs. In summary, it has been demonstrated that the introduction of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as gate dielectrics causes a reduction of the MOSHEMTs C_{GS} due to the addition of a series capacitance. Since the reduction of C_{GS} is equivalent to a reduced ability to deplete the 2DEG channel with a given bias, a much higher V_{GS} is needed to pinch-off the MOSHEMTs, which is reflected by a significant increase in the V_{th} absolute value. For normally ON devices like the ones studied in this chapter, this implies that the lower the C_{GS} the more negative the V_{th} is. In addition, the charge induced at the oxide/GaN interfaces due to interface and/or bulk oxide traps created after the deposition of the gate oxides results in a negative shift of the MOSHEMTs V_{th}

towards more negative values. The fact that the decrease of C_{GS} does not exactly correspond to the V_{th} absolute value increase causes a higher n_s in the active region of the devices and leads to an increase of the I_D, $I_{D,sat}$, $V_{DS,sat}$ and $1/R_{ON}$ values. Furthermore, the substitution of the gate Schottky barrier by a MOS structure reduces the MOSHEMTs output ON-OFF I_D ratio and decreases significantly the ON-state I_G. Finally, an increase of the V_B and a reduction of the OFF-state gate leakage current are achieved after the use of the gate oxides.

Considering the performance of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT with respect to the Al_2O_3 MOSHEMT, the use of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ to increase the κ of Al_2O_3 as gate dielectric can achieve a $C_{GS}^{MOSHEMT}$ value closer to the C_{GS}^{HEMT} together with a smaller negative V_{th}, which is advantageous to reduce the power consumption during switching. In addition to this, higher n_s, I_D, $I_{D,sat}$, and $1/R_{ON}$ values are obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT, which are associated with improved device DC performance. On the other hand, the $V_{DS,sat}$ of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT is marginally smaller than the $V_{DS,sat}$ of the Al_2O_3 MOSHEMT. Although a bigger $V_{DS,sat}$ is desirable to enable the use of a higher positive gate voltage, the smaller $V_{DS,sat}$ is related to a smaller V_{th} shift towards negative values, which is beneficial to reduce the power consumption during switching. Furthermore, the bigger $g_{m,max}$ value directly related to the device cut-OFF and maximum switching frequency indicates a superior performance of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT for microwave applications, whereas the ON-OFF I_D ratio and the ON-state I_G are of the same order of magnitude for both the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs. Finally, from OFF-state measurements the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT shows a smaller V_B and a reduced OFF-state gate leakage current in comparison to the Al_2O_3 MOSHEMT, which is expected considering the smaller V_B and higher κ of Ta_2O_5 with respect to Al_2O_3.

7.7. Conclusions

The use of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as a higher-κ gate dielectric compared to Al_2O_3 can achieve a bigger reduction of the MOSHEMT gate leakage current together with an improvement of the device electrical performance. The electrical characteristics of GaN/AlGaN/GaN HEMTs have been analysed before and after the introduction of Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics. CV measurements demonstrate that, compared to the Schottky HEMT, the C_{GS} of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs decreases from $4.3 \cdot 10^{-3}$ F/m^2 to $2.6 \cdot 10^{-3}$ F/m^2 and $2.8 \cdot 10^{-3}$ F/m^2, respectively, whereas the V_{th} increases towards negative values from – 1.4 V to – 3.5 V and – 3.3 V, respectively. This means that a higher V_{GS} is needed to pinch-OFF the MOSHEMTs, which is equivalent to a loss of channel control due to the reduced ability to deplete the 2DEG channel and an increase in the power consumed during switching. These variations in the C_{GS} and the V_{th} result in an increase in the n_s of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs from $3.1 \cdot 10^{12}$ cm^{-2} to $5.1 \cdot 10^{12}$ cm^{-2} and $5.7 \cdot 10^{12}$ cm^{-2}, respectively, when V_{GS} = 0 V. The increase in the n_s leads to an improvement of the MOSHEMTs I_D, $I_{D,sat}$, $V_{DS,sat}$ and R_{ON} values associated with a superior DC performance. From DC I_D-V_{DS} measurements, the maximum I_D of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMTs increases from 0.36 A/mm to 0.37 A/mm and 0.42 A/mm, respectively, at V_{GS} = 2 V. The $I_{D,sat}$ and $V_{DS,sat}$ also increase from 0.14 A/mm at + 3 V to 0.23 A/mm at + 5.5 V and 0.24 A/mm at + 5 V, respectively, when V_{GS} = 0 V. Finally, the ON-resistance decreases from 16.9 Ω·mm to 16.7 Ω·mm and 15.9 Ω·mm, respectively. Gate transfer measurements show that, compared to the Schottky HEMT, the $g_{m,max}$ of the Al_2O_3 MOSHEMT decreases from 0.13 S/mm to 0.11 S/mm, whereas the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT $g_{m,max}$ stays constant at 0.13 S/mm. The g_m quantifies the ability of the devices to control the 2DEG and is a very important indicator of the device RF performance quality. Furthermore,

although the substitution of the gate Schottky barrier by a MOS structure decreases the output ON-OFF I_D ratio, the ON-state I_G is reduced. The MOSHEMTs ON-OFF drain current ratio decreases by one order of magnitude to ~ 10^5 A/mm, while the ON-state gate current decreases by two orders of magnitude to ~ 10^{-9} A/mm. From OFF-state measurements, the V_B at I_D = 1 μA/mm obtained for the Schottky HEMT increases from 147 V to 244 V and 204 V after the introduction of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics, respectively, whereas the I_G leakage at V_{DS} = 300 V decreases from ~ $4 \cdot 10^{-6}$ A/mm to $1.5 \cdot 10^{-7}$ A/mm and $4.3 \cdot 10^{-8}$ A/mm, respectively. Therefore, this study demonstrates the superior DC performance of the MOSHEMTs compared to the Schottky HEMT despite the reduction of channel control, together with a significant increase of the V_B and decrease of the I_G leakage. Furthermore, the use of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectric compared to Al_2O_3 can achieve a bigger C_{GS} and smaller negative V_{th}, improving the gate modulation efficiency and reducing power consumption during switching. Higher I_D, $I_{D,sat}$, $1/R_{ON}$ and $g_{m,max}$ values are also obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOSHEMT, which are directly related to a better DC and RF performance. The results demonstrate that in addition to a reduction of the gate leakage current, the use of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ to increase the κ of Al_2O_3 as gate dielectric can achieve a further improvement of the MOSHEMT electrical performance while improving the OFF-state breakdown voltage with respect to the Schottky HEMT.

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8. Future work

This thesis has investigated a method to use ALD of Al_2O_3 with Ta modulation doping to grow $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers as a novel wide bandgap/high dielectric constant gate dielectric material for GaN-based MOSHEMT power transistors. Although GaN-capped AlGaN/GaN MOSHEMT devices were successfully fabricated using Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ films as gate dielectrics, the devices characteristics could be improved. InAlN/GaN MOSHEMTs were also fabricated but they failed to show transition to the OFF-state possibly due to short channel effect, which can have negative effects on device performance such as poor pinch-off. Many factors influence the overall performance of the devices. These include: substrate quality, electron mobility, source and drain ohmic contacts resistance, oxide/HEMT interface, gate to channel distance and gate length. Further optimisation work on the growth of the HEMT structures and the fabrication process could further improve device performance.

Research on the effects of HEMT surface preparation on the subsequent MOSHEMT devices electrical characteristics would be of interest to incorporate these devices into commercial applications. The investigation of ex situ HEMT surface cleaning treatments (such as HF, HCl-, and NH_3-based chemical procedures) prior to ALD of the gate oxide could help to minimise the defects density at the oxide/HEMT interface. XPS would be used to examine the ability of the cleaning chemistry to remove native GaO_x, excess oxygen and carbon from the nitride surface or any unintentional deposition of species from the cleaning environment. The use of in situ pre-deposition treatments such as fluorine treatments by plasma-enhanced ALD could achieve the fabrication of normally-OFF operation MOSHEMTs by forming negative charges near the oxide/nitride interface in the gate region of the device causing a positive shift in the threshold voltage. CV-IV electrical

measurements would be used to characterise the fabricated MOSHEMT devices electrical performance and to analyse their interface trap charge density. Additionally, deep-level transient spectroscopy (DLTS) could be used to study the origin of the defects on the MOSHEMTs. Further research could also be carried out on the impact of the gate oxide thickness on the MOSHEMTs performance and on the specific effects of the different post-deposition annealing processing parameters on the oxides interface with the HEMT structure and the MOSHEMTs electrical characteristics.

Work could also be carried out on the engineering of multi-layer gate oxide stacks such as $Al_2O_3/(Ta_2O_5)_x(Al_2O_3)_{1-x}$ bi-layer or Al_2O_3-to-$(Ta_2O_5)_x(Al_2O_3)_{1-x}$ graded layer with increasing Ta_2O_5 molar fraction with increasing distance from the GaN interface. The introduction of an Al_2O_3 interlayer could improve the oxide/GaN interface as well as the electrical properties of the MOSHEMT devices compared to the singe-layer gate dielectrics.

Finally, further research could also investigate the use of the Ta ALD precursor and NH_3 co-reactant for the growth of TaN as the Schottky gate metal contact. This would allow the use of integrated ALD of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ and TaN layers for the deposition of the gate oxide and the gate metal contact in a continuous process with no atmospheric exposure.