Recycled IC Detection through Aging Sensor

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***Abstract*—In this paper, we propose a novel technique to detect recycled ICs via an on-chip, coarse-grained aging sensor, which can be applied to low-power circuits featuring power gating. The sensor detects the increase in the power-rail discharge time of power-gated circuits, when the circuit enters the sleep condition. Through HSPICE simulations, we prove that power network discharge time (τ_{dV}) is extremely sensitive to the age of the circuit. Indeed, after only 1 month of operation, τ_{dV} increases by more than 3X and, after 1 year, its increase exceeds 7X. Our technique enables the detection of recycled ICs with a very high confidence and is a considerably more sensitive indicator of an aged device that alternative solutions relying on fine-grained performance degradation sensors.**

I. Introduction

There is global consensus that counterfeit ICs pose a major risk not only for reliability of embedded systems, but more importantly it can create life threatening scenarios when incorporated in real-time safety critical systems [1]. Counterfeit ICs include recycled, remarked, over-produced, cloned etc. However, a recent study reported that about 80% of total counterfeits are due to recycled and remarked ICs [1].

Currently, recycled ICs are detected by several methods, including physical inspection, electrical inspection, and aging-based fingerprinting [1]. However, physical and electrical inspections usually require specialized equipment and, as they are time consuming processes, have a limited scalability and are suitable for checking limited number of ICs [2], [3]. Aging-based fingerprinting is a promising solution to detect recycled ICs. It exploits the fact that aged ICs are going to operate at a slower speed due to their higher transistor threshold voltage, in comparison with newer counterparts [1], [4]. The performance is compared to that of a known golden model. Aging-based fingerprinting usually relies on path delay monitoring or ring oscillators [1], [5], [6]. This solution is a fine-grained approach targeting local effects, thus possibly missing out the general trend across the whole IC.

This paper presents a novel technique to detect recycled ICs. It exploits power gating infrastructure of circuits adopting power gating to reduce static power and meet their tight energy and power constraints in applications like autonomous systems, Internet of Things, etc. The proposed technique measures the discharge time τ_{dv} of the virtual power (VV_{dd}) network, which occurs through the leakage current of the power-gated circuit. Since bias temperature instability (BTI) aging causes an increase in transistor V_{th}, and leakage current decreases exponentially with V_{th}, τ_{dv} augments noticeably over time [7], allowing us to differentiate between recycled and new ICs. A small delay sensor, which may already be part of the power gating DFT infrastructure [8], is used to measure τ_{dv} that is then compared with the discharge time of a new IC. When compared with the traditional path delay monitoring method, it is found to provide a confidence in recycled IC detection which is more than 4 order of magnitude greater and it also provides coarse granularity at minimum area overhead.

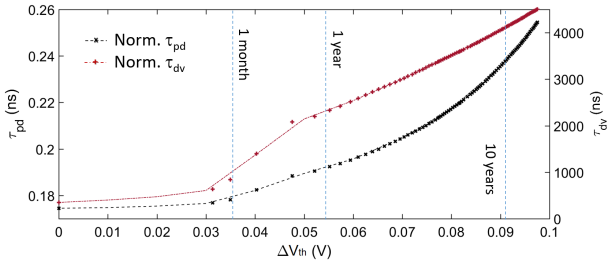

Fig. 1. Propagation delay and discharge time as a function of V_{th} degradation.

The remainder of the paper is organized as follows. In Section II, we describe the operation of the adopted aging sensor and validate the proposed approach considering a simple benchmark circuit. In Section III, we draw some conclusions.

II. Proposed Recycled IC Detection Technique

Many techniques proposed to detect recycled ICs rely on monitoring performance degradation, including path delay and ring oscillator frequency, whose degradations are both due to the linear decrease in active current induced by BTI. Therefore, we can expect that the discharge time of VV_{dd} network through leakage current is much more sensitive to aging than path delay or ring oscillator frequency, since the leakage current decreases exponentially with ΔV_{th}. This is confirmed by the obtained with HSPICE simulation results depicted in Figure 1. As an example, we have simulated a power-gated circuit of 21 cascaded inverters and its power distribution network synthesized with a 32nm CMOS technology. The power distribution network has been sized to have an IR-drop $\leq 0.1V_{dd}$. The figure shows that τ_{pd} increases less than 6% after a month of operation, 22% after a year, and up to 1.43X after 10 years of operation. Conversely, the discharge time τ_{dV} exhibits an increase exceeding 2X after a month of operation, 5.4X after a year, and escalating up to 15.7X in 10 years. Therefore, the discharge time of the VV_{dd} network through the leakage current of the power-gated circuit is a considerably more sensitive indicator of an aged device than path delay, and can be measured in order to detect recycled ICs.

When an IC operates, different devices may undergo different amount of stress and degradation, depending on their

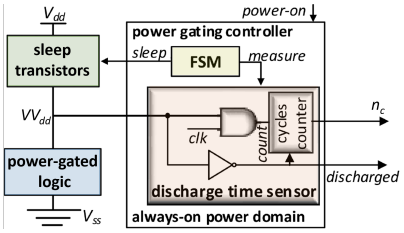

Fig. 2. VV_{dd} network discharge time sensor architecture.

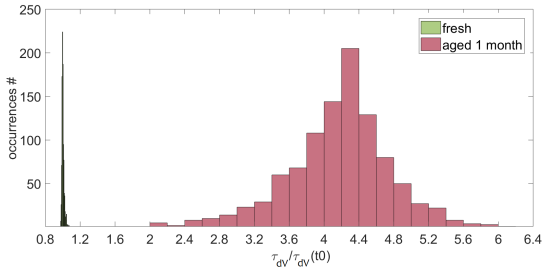

Fig. 3. Normalized distribution of τ_{dV} for fresh and 1-month aged circuits.

operating condition and switching activity. Therefore, it is problematic to address the detection of recycled ICs by using fine-grained aging sensors for path delay degradation, and many sensors may need to be deployed to guarantee that aging effects are captured. This limitation is overcome by the the proposed technique, which is based on a coarse-grained aging sensor targeting the discharge time of a power-gated core as an aging metric. This occurs through the whole power-gated circuit, with no need to pinpoint sub-blocks, or even paths undergoing the larger degradation. The discharge time sensor, shown in Figure 2 resides in the power-gating controller. It counts the clock rising edges n_c until the virtual voltage VV_{dd} drops to logic 0. The finite state machine FSM controls the sensor by asserting the measure signal together with the sleep signal in order to collect the τ_{dV}^{meas} value when the sleep signal is asserted and the circuit is power-gated. The measured discharge time is $\tau_{dV}^{meas} = n_c \times T_{clk}$, where n_c is number of clock cycles, and T_{clk} is the circuit clock period.

The very high confidence in proper detection of a recycled IC and its robustness to process variations have been evaluated by means of Monte Carlo simulations. We have assumed a 15% threshold voltage variation with a normal distribution and 1000 instances for both the fresh and 1-month aged circuit. The worst case temperature $T = 100^oC$ has been considered.

Figure 3 depicts the obtained results for our proposed technique. The histograms report normalized results against the nominal value exhibited at t_0 (fresh circuit), $\tau_{dV0}^{nom} \simeq 207.4ns$. As we can see, the distribution for a fresh circuit is very narrow, with a worst case discharge time (highest value) $\tau_{dV0} \simeq 225.2ns$, which is approximately 10% higher than τ_{dV0}^{nom}. The worst case value is determined in order to minimize the τ_{dV} difference between a fresh and an aged circuit. The aged distribution is much wider, since the threshold voltage shift due to BTI aging depends also on the initial threshold voltage. Nevertheless, in the worst case scenario for our technique (lowest discharge time), it is $\tau_{dV}^{1month} \simeq 455.6ns \gtrapprox 2 \times \tau_{dV0}^{nom}$, which represents a margin of more than 230ns

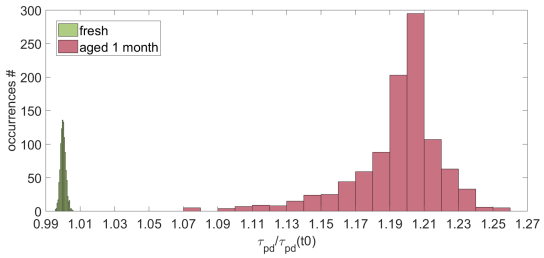

Fig. 4. Normalized distribution of τ_{pd} for fresh and 1-month aged circuits.

for our technique to distinguish between a fresh and an aged circuit that has been already operating for a month only.

The results obtained for the path delay are shown in Figure 4. In this case, the normalization factor is $\tau_{pd0}^{nom} \simeq 177ps$. As expected, the distribution for a fresh circuit is even narrower that for the discharge time, with a worst case path delay $\tau_{pd0} \simeq 179ns$, which is less than 1% higher than the nominal value. Similar to the discharge time case, the aged distribution after 1 month of operation is considerably wider, with a worst case $\tau_{pd}^{1month} \simeq 188ps$, which is only 6.2% greater than τ_{pd0}^{nom}. Indeed, with path delay, the margin for the identification of an aged circuit reduces to 9ps, which is very small and more than four orders of magnitude lower than the proposed technique. Therefore, a much more accurate sensor is needed to detect recycled ICs, with a consequent increase in design cost.

III. Conclusions

We have proposed a novel technique to detect recycled ICs based on coarse-grained aging sensor measuring the discharge time of the VV_{dd} network. Our technique provides a very high confidence in detecting recycled ICs, with an increase in the discharge time reaching 7X after 1 year of operation. This is more than four orders of magnitude greater that the margin allowed by techniques based on path delay sensors, and is obtained at a very low test time and negligible area overhead.

Acknowledgments

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