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Decoupled Vector Space Decomposition Based Space Vector Modulation for Dual Three-Phase Three-Level Motor Drives

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***Abstract*—In this paper, a novel space vector modulation (SVM) strategy is proposed and designed for dual three-phase three-level motor drives based on vector space decomposition (VSD), which could be applied for high-power high-reliability applications. The key of the proposed method is to design two decoupled groups of voltage vector candidates for synthesis on *α-β* subspace and *x-y* subspace, respectively. The two decoupled groups of voltage vectors will synthesize respective voltage references on *α-β* subspace and *x-y* subspace, while having no impact on each other. The redundant small voltage vectors and zero-sequence voltage vectors are utilized to mitigate voltage oscillation in mid-point of DC link and suppress zero-sequence current component for dual three-phase windings with a common neutral. For comparison, another VSD-SVM strategy is designed based on traditional solution, which can not offer closed-loop control on *x-y* subspace. Both simulation and experiments have been given to verify that the proposed decoupled VSD-SVM can suppress harmonic components on *x-y* subspace besides tracking torque components on *α-β* subspace. Furthermore, the harmonic performance of the proposed decoupled VSD-SVM has been compared with the traditional VSD-SVM strategy and the carrier disposition based pulse width modulation (CBD-PWM).**

***Index Terms*—multiphase motor drives, multilevel inverter, space vector modulation, vector space decomposition, harmonic performance.**

I. Introduction

Recently, the requirements of capacity and reliability are increasing for variable-speed drive systems in various industrial applications [1-2]. Meanwhile, the power electronics technology is experiencing fast development, and the phase number of drives has not been limited by AC grid. Thus, the multiphase variable-speed drives become a promising solution for high-power high-reliability electric drives [3-5]. With multiphase configuration, the power ratings and fault tolerant ability of drive systems can be enhanced. The applications include electric ship propulsion [6], turbo-compressor drives [7], electric traction [8], EV on-board charging system [9], etc. Various control schemes have been proposed and studied for multiphase motor drives previously. For motor drives with multiple stator windings, the multiple *d-q* frames based field oriented control (FOC) scheme could be applied. Thus, the phase currents in multiple three-phase windings can be controlled separately, and the currents in multiple windings are kept balanced [10].

The vector space decomposition (VSD) method is another well-known control scheme for multiphase motor drives, where fundamental components, harmonic components and zero-sequence components are decomposed onto three kinds of subspaces, namely the torque-component subspace, the harmonic-component subspace and the zero-sequence subspace. These three kinds of subspaces are orthogonal to each other [11]. The electro-mechanical torque can be regulated effectively by controllers on the torque-component subspace, while the harmonic components are limited by optimizing the switching vectors on the harmonic-component subspace. For further suppressing the low-order harmonics and the unbalanced currents between the dual three-phase windings, additional harmonic current controllers are required on the harmonic subspace [12]. The proportional-integral (PI) or proportional-resonant (PR) controllers could be used to regulate current components on torque-component subspace and harmonic-component subspace [13].

The model-based predictive control (MBPC) is a kind of control schemes studied intensively for multiphase drives. The MBPC scheme is proposed for the dual three-phase induction motor drives by choosing the optimum switching states for the best predicted performance of drives [14]. The parts of control and modulation can be integrated together in MBPC. To further reduce the current ripples while limiting the switching frequencies, some improved predictive control schemes are studied, such as one-step modulation predictive control, restrained search predictive control, and SVM based predictive control [15-17]. The direct torque control (DTC) including both the table-based DTC (ST-DTC) and the SVM based DTC schemes have also been discussed for multiphase motor drives [18]. To suppress the current harmonics for DTC, an additional switching table and a flux estimator on *x-y* plane are added, and a two-step ST-DTC scheme is proposed for the dual three-phase permanent-magnet synchronous motor (PMSM) drives [19]. However, all the aforementioned control schemes are discussed for multiphase motor drives which are fed by two-level voltage source inverters (VSIs).

On the other hand, the multilevel inverters have

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gained rapid developments recently. By combing techniques of multilevel inverters and multiphase drives, the multiphase multilevel drives provide an effective solution to mitigate both the voltage stress and current stress for high-power drives [2-3]. However, the research on multiphase multilevel drives is still less compared to the two-level inverters fed multiphase drives. In particular, it is very difficult to design and implement SVM strategy for multiphase multilevel motor drives due to the huge number of voltage vectors. Although the carrier based modulation is a convenient solution for controlling multiphase multilevel motor drives, the SVM strategies have the unique advantages such as digital implementation, high utilization of DC link voltage and well-defined switching vectors for fault tolerant operation [13, 20]. Based on a two-level multiphase modulator using displacement, a kind of SVM strategy is proposed for the five-phase five-level cascaded full-bridge inverter [21]. But the harmonic current suppression has not been considered with this strategy. For suppressing harmonic current components, a new SVM strategy is proposed for the five-phase neutral-point-clamping three-level (NPC-3L) induction motor drives based on VSD principle, where the optimum switching vectors are selected not only to regulate the fundamental current but also to eliminate the harmonics on the *x-y* plane [22]. In [23], this SVM strategy is improved for the NPC-3L five-phase induction motor drives by reducing variations of the common mode voltage. The number of sub-sectors is expanded from 10 to 14 in each sector, and different switching sequences are used in the newly added sub-sectors. The improved SVM strategy is also extended to the NPC-3L seven-phase induction motor drives in [24].

However, all the aforementioned multiphase multilevel SVM strategies can only limit the harmonics induced by the converter itself. It may still suffer from harmonic components induced by harmonics in back EMF of electrical machine. Besides, the asymmetric currents would be produced by unbalanced parameters of different phase windings, and the periodic components will be generated on *x-y* subspace. Different from them, the contribution of this paper includes the following two aspects: Firstly, a novel decoupled VSD-SVM strategy is proposed for NPC-3L inverters fed dual three-phase PMSM motor drives, and the closed-loop control of components on *x-y* subspace is achieved with this decoupled VSD-SVM strategy. Secondly, both isolated neutrals and common neutral connection are considered in design of modulation strategy for multiphase motor drives. The circulating current can be suppressed effectively in the drive. With volt-second balancing principle, the selected voltage vectors for voltage synthesis can be rearranged with proper switching sequences, in such a way that limited switching frequencies and low harmonics are provided. It should be noted that the proposed decoupled VSD-SVM could be valid for various multiphase drives. For exemplification, the NPC-3L inverters fed dual three-phase PMSM drives are used in this paper.

The organization of the rest of this paper is listed as following: In Section II, the principle and design procedure of the proposed decoupled VSD-SVM strategy and control are presented. In Section III, another VSD-SVM is designed for dual three-phase multilevel inverters based on traditional method for comparison. In Section IV, both simulation and experiments are taken to compare operating performance between the proposed decoupled VSD-SVM and the traditional VSD-SVM. Finally, the conclusions are drawn in section V.

II. Proposed Decoupled VSD-SVM

Fig. 1 shows the configuration of the NPC-3L dual three-phase motor drives. The phase angle between the two three-phase windings could be 0, 30 degrees, and 60 degrees. The dual three-phase PMSM drive with a 30-degree shifted angle is used in this paper. Two neutral points O_1 and O_2 of dual three-phase windings can be isolated or non-isolated. For isolated neutrals, the flowing route of zero-sequence currents will be blocked. On the other hand, there will exist zero-sequence current component when the common neutral is used. But fault tolerant ability of the system could be enhanced by this way. *M* is the mid-point of DC link. The details of dynamical modelling of the NPC-3L inverters fed dual three-phase motor drives have been presented in [13]. Due to limits in page length, the mathematical modeling is ignored in this paper.

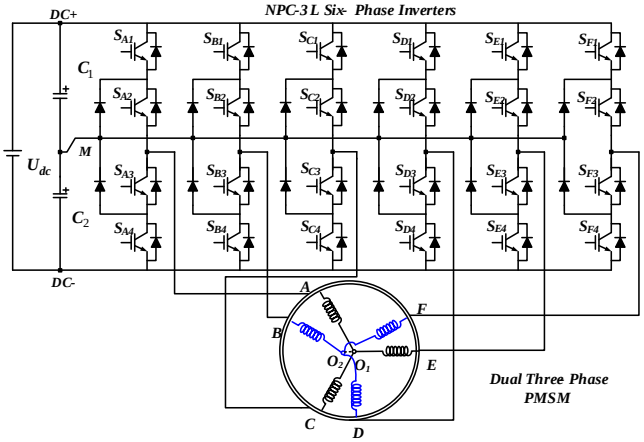

Fig. 1. Configuration of NPC-3L inverters fed dual three-phase PMSM drives.

The VSD transformation has been used widely for controlling multiphase motor drive. Based on VSD matrix in Eq. (1), the six-dimensional variables of dual three-phase motor drives on natural frame are converted into variables on three orthogonal subspaces, namely *α-β*, *x-y* and z_1-z_2 subspaces.

$$C_{VSD}=\frac{1}{3}\begin{bmatrix}1 & \sqrt{3}/2 & -1/2 & -\sqrt{3}/2 & -1/2 & 0\\ 0 & 1/2 & \sqrt{3}/2 & 1/2 & -\sqrt{3}/2 & -1\\ 1 & -\sqrt{3}/2 & -1/2 & \sqrt{3}/2 & -1/2 & 0\\ 0 & 1/2 & -\sqrt{3}/2 & 1/2 & \sqrt{3}/2 & -1\\ 1 & 0 & 1 & 0 & 1 & 0\\ 0 & 1 & 0 & 1 & 0 & 1\end{bmatrix} \tag{1}$$

It is recalled that the *α-β* subspace comprises the fundament and harmonic components with orders of $6m\pm5$ $(m=1,3,5,\cdots)$, and they participate in the electro-mechanical energy conversion. The *x-y* subspace comprises harmonic components with orders of $6m\pm1$ $(m=1,3,5,\cdots)$ and the z_1-z_2 subspace comprises the harmonic components with orders of $3m$ $(m=1,3,5,\cdots)$. When the neutrals of the dual three-phase windings are isolated, the harmonic components on the z_1-z_2 plane are

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zero. On the other hand, there will be components on z_1-z_2 subspace when the common neutral is used. Thus, the voltage components on α-β subspace and x-y subspace are expressed to be:

$$U_{\alpha\beta}=\frac{1}{3}[U_{AM}+e^{j\frac{\pi}{6}}U_{BM}+e^{j\frac{2\pi}{3}}U_{CM}+e^{j\frac{5\pi}{6}}U_{DM}+e^{j\frac{4\pi}{3}}U_{EM}+e^{j\frac{3\pi}{2}}U_{FM}] \quad (2)$$

$$U_{xy}=\frac{1}{3}[U_{AM}+e^{j\frac{5\pi}{6}}U_{BM}+e^{j\frac{4\pi}{3}}U_{CM}+e^{j\frac{\pi}{6}}U_{DM}+e^{j\frac{2\pi}{3}}U_{EM}+e^{j\frac{3\pi}{2}}U_{FM}] \quad (3)$$

where $U_{xM}(x=A\sim F)$ are relative voltages of inverter outputs to mid-point of DC link, and the values are $-U_{dc}/2$, 0, and $U_{dc}/2$. They are represented by 0, 1, and 2, respectively. So, there will be 729 voltage vectors for NPC-3L inverters fed dual three-phase motor drives. The huge number of voltage vectors will bring heavy burden on design of modulation strategy. Thus, the voltage vector candidates should be selected for simplicity. In this paper, a novel decoupled VSD based SVM strategy is proposed by designing decoupled voltage vector candidates for voltage synthesis on α-β subspace and x-y subspace, respectively.

A. Selection of Voltage Vector Candidates on α-β Subspace

First, the voltage vectors are selected on α-β subspace. The requirements include:

(1) The magnitudes of the voltage vectors on α-β subspace should be large enough to achieve high utilization of DC link voltage.

(2) The selected voltage vectors must include redundant vectors to control mid-point voltage of DC link.

(3) The voltage synthesis of selected vectors is zero on x-y subspace to limit harmonics induced from the inverter.

Complying the three rules mentioned above, the distribution of selected voltage vector candidates is plotted as shown in Fig. 2. There are 12 sectors on α-β subspace. For example, in sector I, the selected voltage vector candidates for synthesis are 220000, 221001, 111001/222112, 220002, 220011, and 110010/221121. Their magnitudes and phase angles are listed in Table I. The voltage vectors 220000, 221001 and 111001/222112 are with the same direction on α-β subspace, but they are distributed in opposite directions on x-y subspace. By properly designing dwelling time of these three voltage vectors, a new harmonic-free voltage vector is synthesized with a certain magnitude on α-β subspace while it is with zero value on x-y subspace. For example, the new harmonic-free voltage vector $\boldsymbol{V}_1$ can be synthesized by the three voltage vectors, namely $\boldsymbol{V}_a=220000$, $\boldsymbol{V}_b=221001$ and $\boldsymbol{V}_c=111001/222112$. The vectors $\boldsymbol{V}_a$ and $\boldsymbol{V}_b$ are used to synthesize one new voltage vector $\boldsymbol{V}_\alpha$, and the vectors $\boldsymbol{V}_b$ and $\boldsymbol{V}_c$ are used to synthesize the second new voltage vector $\boldsymbol{V}_\beta$. Due to the opposite directions of $\boldsymbol{V}_a$, $\boldsymbol{V}_b$ and $\boldsymbol{V}_c$ on x-y subspace, the newly synthesized voltage vectors $\boldsymbol{V}_\alpha$ and $\boldsymbol{V}_\beta$ will have zero harmonic component on x-y subspace after choosing dwelling time inversely proportional to magnitudes of $\boldsymbol{V}_a$, $\boldsymbol{V}_b$ and $\boldsymbol{V}_c$. The synthesis process is shown in Eqs. (4-5). Then, a factor λ is designed to distribute dwelling time between the two new voltage vectors of $\boldsymbol{V}_\alpha$ and $\boldsymbol{V}_\beta$, as shown in Eq. (6).

$$\boldsymbol{V}_\alpha=\frac{0.1494}{0.1725+0.1494}\boldsymbol{V}_a+\frac{0.1725}{0.1725+0.1494}\boldsymbol{V}_b \quad (4)$$

$$\boldsymbol{V}_\beta=\frac{0.2357}{0.1725+0.2357}\boldsymbol{V}_a+\frac{0.1725}{0.1725+0.2357}\boldsymbol{V}_c \quad (5)$$

$$\boldsymbol{V}_1=(1-\lambda)\boldsymbol{V}_\alpha+\lambda\boldsymbol{V}_\beta \quad (6)$$

The distribution factor λ is limited within (0, 1). The magnitude of the synthesized harmonic-free vector becomes smaller with increase of λ, since $\boldsymbol{V}_c$ is the small redundant voltage vector with small amplitude. But the controllability of the synthesized harmonic-free vector for the mid-point voltage of DC link will be enhanced accordingly with increase of λ. In this paper, λ is set as 0.5 to illustrate the principle. Thus, the new harmonic-free vector is derived as:

$$\boldsymbol{V}_1=0.52077\boldsymbol{V}_a+0.26794\boldsymbol{V}_b+0.21129\boldsymbol{V}_c \quad (7)$$

The magnitude of $\boldsymbol{V}_1$ is $0.5346U_{dc}$.

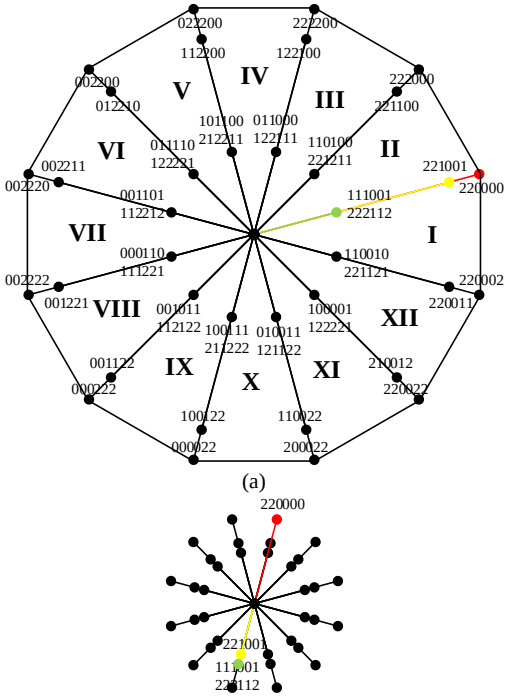

Fig. 2. Voltage vector candidate selection for α-β subspace: (a) α-β subspace; (b) x-y subspace.

Table I. Magnitudes and phase angles of selected voltage vector candidates of sector I on α-β subspace.

Voltage vector	α-β subspace		x-y subspace	
	Magnitude /U_{dc}	Angle	Magnitude /U_{dc}	Angle
220000	0.6440	π/12	0.1725	5π/12
221001	0.5577	π/12	0.1494	-7π/12
111001/222112	0.2357	π/12	0.2357	-7π/12
220002	0.6440	-π/12	0.1725	-5π/12
220011	0.5577	-π/12	0.1494	7π/12
110010/221121	0.2357	-π/12	0.2357	7π/12

The distribution of the twelve newly synthesized harmonic-free voltage vectors are plotted in Fig. 3(a). As shown in Fig. 3(b), the voltage reference V_{ref} can be synthesized by the harmonic-free V_1 and V_{12} when it is located in sector I. By defining the modulating index as $M_{\alpha\beta}=U_{ref}/0.5346U_{dc}$, the dwelling time is calculated as

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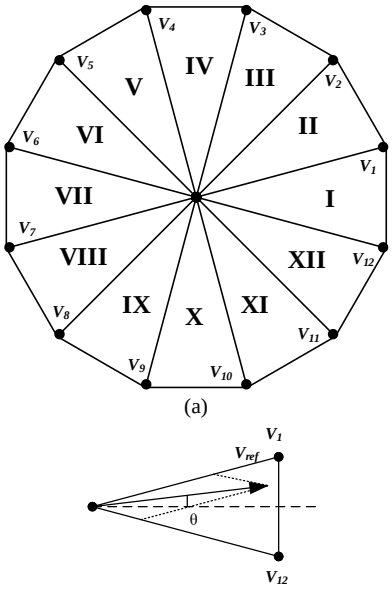
$T_\alpha = 2M_{\alpha\beta}\sin(\frac{\pi}{12}+\theta)T_s$ for V_1 and $T_\beta = 2M_{\alpha\beta}\sin(\frac{\pi}{12}-\theta)T_s$ for V_{12}, where T_s is the switching period. The maximum voltage amplitude by linear modulation will be (0.5346 U_{dc})·cos(π/12)=0.5164U_{dc}. The maximum modulation index for linear modulation is derived to be $M_{\alpha\beta}$=0.9659. With coefficients in Eqs. (4-6) and dwelling time of harmonic-free vectors, the dwelling time of original voltage vectors for sector I are calculated as shown in Table II.



(a)

(b)

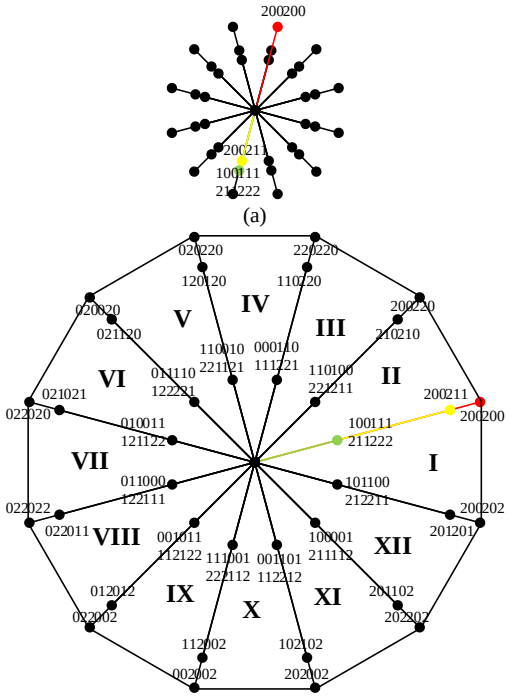
Fig. 3. Newly synthesized voltage vector distribution on *α-β* subspace: (a) voltage vector distribution; (b) voltage synthesis.

Table II. Dwelling time of voltage vector original voltage vectors of sector I.

Voltage vector	Dwelling time
220000	$0.52077T_\alpha$
221001	$0.26794T_\alpha$
111001/222112	$0.21129T_\alpha$
220002	$0.52077T_\beta$
220011	$0.26794T_\beta$
110010/221121	$0.21129T_\beta$

B. Selection of Voltage Vector Candidates on x-y Subspace

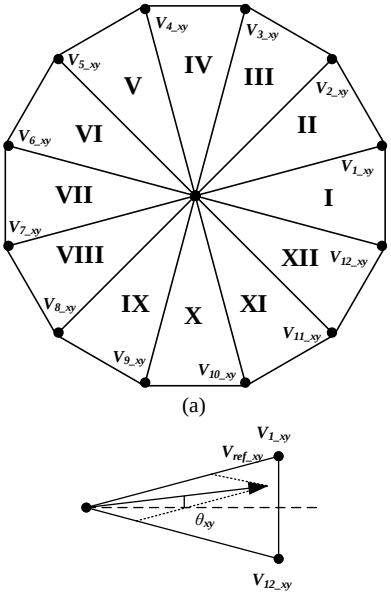
Another set of voltage vectors are selected for synthesizing voltage reference on *x-y* subspace, which will be generated to suppress harmonic components from back EMF and oscillating components from unbalanced parameters in electrical machine. Similar to voltage vector synthesis on *α-β* subspace, the magnitudes of the voltage vector candidates on *x-y* subspace should be large enough to suppress harmonic components. These voltage vector candidates should be synthesized as zero on *α-β* subspace, and redundant voltage vectors should also be included for mitigating fluctuation in mid-point voltage of DC link. For example. The voltage vector candidates 200200($\boldsymbol{V}_a$), 200211($\boldsymbol{V}_b$) and 100111/211222 ($\boldsymbol{V}_c$) are used to synthesize a new voltage vector, which has zero component on *α-β* subspace. The magnitude of the newly synthesized voltage vector is also 0.5346U_{dc}. Fig. 4 shows the selected voltage vector candidates, and Fig. 5 shows the twelve newly synthesized voltage vectors on *x-y* subspace, which have zero component on *α-β* subspace.



(a)

(b)

Fig. 4. Voltage vector candidate selection for *x-y* subspace: (a) *α-β* subspace; (b) *x-y* subspace.



(a)

(b)

Fig. 5. Newly synthesized voltage vector distribution on *x-y* subspace: (a) voltage vector distribution; (b) voltage synthesis.

Table III. Dwelling time of voltage vectors of sector I on *x-y* subspace.

Voltage vector	Dwelling time
220200	$0.52077T_x$
200211	$0.26794T_x$
111001/222112	$0.21129T_x$
220002	$0.52077T_y$
220011	$0.26794T_y$
110010/221121	$0.21129T_y$

By defining the modulation index on *x-y* subspace as $M_{xy} = U_{ref\_xy}/0.5346U_{dc}$, the dwelling time of newly synthesized voltage vectors on *x-y* subspace are $T_x = 2M_{xy}\sin(\frac{\pi}{12}+\theta_{xy})T_s$ for V_{1_xy} and $T_y = 2M_{xy}\sin(\frac{\pi}{12}-\theta_{xy})T_s$ for V_{12_xy}, respectively. θ_{xy} is the phase angle of reference voltage on *x-y* subspace. Similar to the process in last section, the selected original

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voltage vectors and their dwelling time are listed in Table III when the reference voltage vector is in sector I on *x-y* subspace.

C. Zero-sequence Component Suppression & Mid-point Voltage Control in DC Link

When neutrals of dual three-phase stator windings are connected, there will exist zero-sequence current component in the drive. This condition is similar when the electric drive is with the odd number of freedom such as six-phase, eight-phase, ten-phase, twelve-phase drives, etc. In addition to several orthogonal two-dimension subspaces obtained by VSD transformation, one dimension will be remained for the zero-sequence component. So, some special voltage vector candidates are in demand for suppressing the zero-sequence current component. For the dual three-phase motor drive in Fig. 1, the voltage vectors 202020 and 020202 can be used to regulate the zero-sequence current component. The mapping of these two voltage vectors on *α-β* subspace and *x-y* subspace are both zero. Thus, they have no impact on control of components on *α-β* subspace and *x-y* subspace. If the zero-sequence current component i_O flowing out of the first three-phase winding is larger than zero, the voltage vector 020202 could be used to suppress it. On the other hand, the vector 202020 is used when i_O is below zero. The dwelling time of the zero-sequence voltage vectors 020202/202020 is designed to be $T_0=M_0T_s$, where M_0 is the corresponding modulation index for zero-sequence subspace. It is noted that these two zero-sequence voltage vectors can be ignored when two neutrals of the dual three-phase windings are isolated.

Similar to three-phase NPC-3L inverters, the small voltage vectors of dual three-phase NPC-3L inverter also have impacts on mid-point voltage in DC link. For example, the voltage vector 222112 on *α-β* subspace in Fig. 2 and the voltage vector 211222 on *x-y* subspace in Fig. 4 connects the phase loads to the upper capacitor and makes the upper capacitor voltage have a upward trend. So they are called as the P-type voltage vector. On the other hand, the voltage vector 111001 in Fig. 2 and the voltage vector 100111 in Fig. 4 connect the phase loads to the lower capacitor and makes the lower capacitor voltage have a downward trend. They are called as N-type voltage vector. The mid-point voltage deviation in DC link is defined to be $\Delta U_c = U_{c1} - U_{c2}$. When $\Delta U_c > 0$, the P-type small voltage vectors, namely 222112 on *α-β* subspace and 211222 on *x-y* subspace can be used. On the other hand, the N-type small voltage vectors, namely 111001 and 100111 can be used.

Table IV lists summarization of voltage vector candidates and the dwelling time with different values of i_0 and ΔU_c. The selected voltage vectors in Fig. 2 are used to synthesize the voltage reference on *α-β* subspace while the selected voltage vectors in Fig. 4 are used to synthesize the voltage reference on *x-y* subspace. The blue vectors and the red vectors are redundant small voltage vectors on *α-β* subspace and *x-y* subspace for mitigation of mid-point voltage deviation in DC link, respectively. The green voltage vectors are used to suppress zero-sequence current component under common neutral point condition. The zero voltage vector 111111 is used to compensate the remaining time within one switching period T_s.

Table IV. Selected voltage vectors and dwelling time in sector I.

$\Delta U\leq 0$, $i_o\geq 0$	$\Delta U\geq 0$, $i_o\geq 0$	$\Delta U<0$, $i_o<0$	$\Delta U>0$, $i_o<0$	Dwelling time
220000	220000	220000	220000	$0.52077T_\alpha$
221001	221001	221001	221001	$0.26794T_\alpha$
111001	222112	111001	222112	$0.21129T_\alpha$
220002	220002	220002	220002	$0.52077T_\beta$
220011	220011	220011	220011	$0.26794T_\beta$
110010	221121	110010	221121	$0.21129T_\beta$
200200	200200	200200	200200	$0.52077T_x$
200211	200211	200211	200211	$0.26794T_x$
100111	211222	100111	211222	$0.21129T_x$
200202	200202	200202	200202	$0.52077T_y$
201201	201201	201201	201201	$0.26794T_y$
101100	212211	101100	212211	$0.21129T_y$
020202	020202	202020	202020	T_0
111111	111111	111111	111111	T_s-T_α-T_β-T_x-T_y-T_0

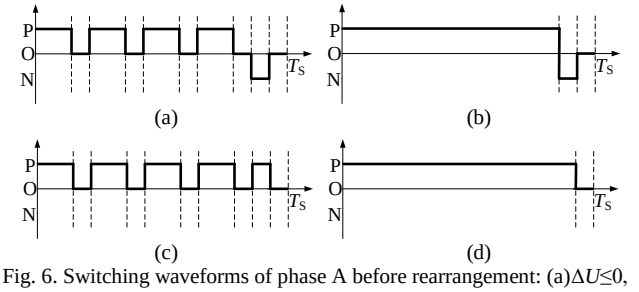

Fig. 6. Switching waveforms of phase A before rearrangement: (a)$\Delta U\leq 0$, $i_o\geq 0$; (b)$\Delta U\geq 0$, $i_o\geq 0$; (c)$\Delta U<0$, $i_o<0$; (d)$\Delta U>0$, $i_o<0$.

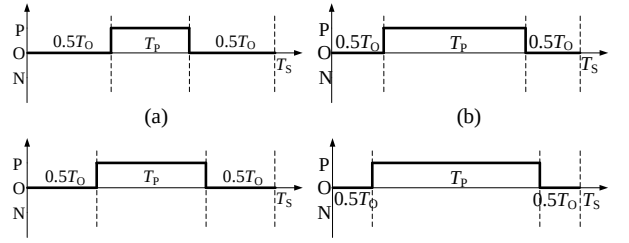

Fig. 7. Switching waveforms of phase A after rearrangement: (a)$\Delta U\leq 0$, $i_o\geq 0$; (b)$\Delta U\geq 0$, $i_o\geq 0$; (c)$\Delta U<0$, $i_o<0$; (d)$\Delta U>0$, $i_o<0$.

D. Rearrangement of Voltage Vectors

Due to many voltage vectors used within one switching period as shown in Table IV, the drive will suffer from high switching frequency without proper design of switching sequence. Fig. 6 shows the switching waveforms of phase A before rearrangement, the output may switch for more than one voltage level and it is not symmetrical. To solve this problem, the switching sequence of voltage vectors has to be rearranged. The voltage vectors will produce both positive and negative voltage levels with one switching period. Those different voltage levels can cancel with each other partly. Define T_P and T_N as the total dwelling time of P voltage level and N voltage level produced by all voltage vectors in one switching period, which could be calculated by adding the dwelling time of related voltage vectors from Table IV. If $T_P > T_N$, the final dwelling time of non-zero voltage level will be $T_P = T_P - T_N$ and $T_N = 0$. On the other hand, when $T_P < T_N$, the final dwelling time of non-zero voltage level will be $T_N = T_N - T_P$ and $T_P = 0$. The combined P voltage level or N voltage level will be distributed in middle of switching interval. The zero voltage level, namely O voltage level will be distributed on two sides of each switching interval, and the dwelling time is T_O. Fig. 7 shows the switching waveforms of phase A after rearrangement of switching sequence for different voltage vectors. In Fig. 7(a), $T_N = 0$,

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$T_O = T_s - 0.78865(T_\alpha + T_\beta + T_x + T_y) + T_0$, and $T_P = 0.78865(T_\alpha + T_\beta + T_x + T_y)$.

E. Control Scheme

Fig. 8 shows control block diagram of the proposed control scheme based on the decoupled VSD-SVM strategy. The closed-loop speed controllers generates the *q*-axis current reference, while the *d*-axis current reference is set to be zero. The feedforward terms $Q_{\mathrm{d}} = \omega\psi_f + \omega(L_{ls} + L_d)i_d$ and $Q_{\mathrm{q}} = -\omega(L_{ls} + L_q)i_q$ are used for decoupling between *d*-axis and *q*-axis. Since the components on *α-β* subspace have been converted under synchronous frame, the PI controllers are used to regulate the current components on *α-β* subspace. On *x-y* subspace and zero-sequence dimension, the periodic current components exist. So, the closed-loop PR controllers are used to track the reference signals.

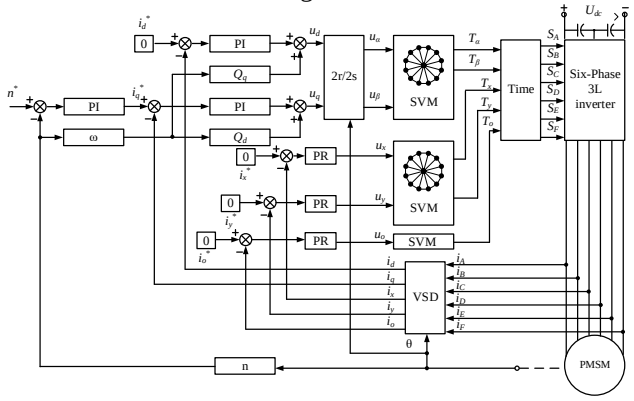

Fig. 8. Control block diagram of drive based on the proposed decoupled VSD-SVM strategy.

III. Traditional VSD-SVM

For comparison with the proposed decoupled VSD-SVM, another VSD-SVM strategy is designed for dual three-phase PMSM drives based on the traditional method in [22-25]. For simplicity, the design is taken for the condition where two neutral points are isolated. Different from traditional VSD-SVM methods for five-phase and seven-phase drives in [22-24], the authors implement the method for six-phase multilevel inverter system and apply it for closed-loop controlled motor drives [25]. For the traditional VSD-SVM method, only the voltage components on *α-β* subspace are used to synthesize the voltage reference while the voltage components on *x-y* subspace are forced zero. So, it is lack of controllability on *x-y* subspace.

Since there are numerous voltage vectors for the NPC-3L six-phase inverter, the first step is also to simplify the voltage vector candidates for the traditional VSD-SVM. To do that, the relationships among phase voltages within various large sectors are used. For instance, when the angle of reference voltage θ is within $(-\pi/12, 0]$, the phase voltage references of dual three-phases drives should comply with the following relationship: $u^*_{AO1} \geq u^*_{EO1} \geq u^*_{CO1}$ for the first three-phase winding and $u^*_{BO2} \geq u^*_{FO2} \geq u^*_{DO2}$ for the second three-phase winding. Thus, the inverter output voltages are required to satisfy the following condition: $u_{AM} \geq u_{EM} \geq u_{CM}$ and $u_{BM} \geq u_{DM} \geq u_{FM}$. Based on that requirement, some voltage vectors are omitted within $\theta \in (-\pi/12, 0]$. For example, the inverter voltages corresponding to the vector 200201 can not satisfy the requirement above. On the other hand, the voltage vector 220001 could satisfy the condition. So, the voltage vector 220001 is kept while the voltage vector 200201 is omitted from the candidates. Thus, the total number of voltage vectors reduces from 729 to 169. Fig. 9 shows the simplified voltage vectors on *α-β* subspace. Since the number of voltage vectors is huge, the ternary code is used to mark the simplified voltage vectors in Fig. 9. For example, the voltage vector 200201 is marked as 505 and the vector 220001 is marked as 649 in Fig. 9.

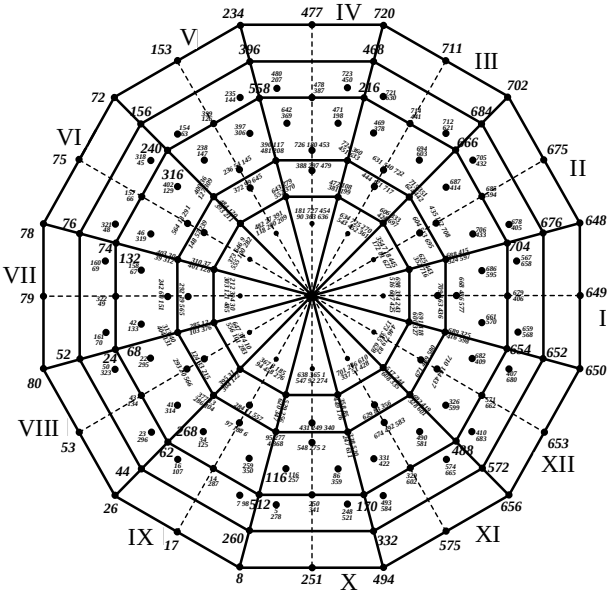

Fig. 9. Simplified voltage vectors on *α-β* subspace.

The synthesis of voltage references for the NPC-3L dual three-phase inverter is based on the voltage-second balancing principle. Thus, five voltage vectors are needed to synthesize the voltage references within each switching period to guarantee the solutions for the equations based on voltage-second balancing principle. For optimizing the performance of the drive system, the five voltage vectors should be chosen to synthesize the desired voltage reference on *α-β* subspace, minimize the harmonics on *x-y* subspace, and contain redundant voltage vectors for controlling voltage in mid-point of DC link at the same time. Table V lists the five optimum voltage vectors within sector I in Fig. 9, which satisfy the aforementioned requirements.

Table V. Selected optimum voltage vector combinations within sector I.

Combination	Optimum voltage vector combinations
I-1	110001-111001-111111-120111-221111
I-2	110001-111001-120001-120111-221111
I-3	110001-120001-120111-220011-221102
I-4	110000-120001-111001-221001-220111
I-5	110001-120001-221001-220011-221111
I-6	110001-220001-221001-220011-221111
I-7	110001-220002-220001-220011-221011
I-8	110000-220000-220001-221001-221011

According to the voltage-second balancing principle, the dwelling time of voltage vectors in optimum combinations are given as:

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$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \end{bmatrix} = \begin{bmatrix} V_1^{\alpha} & V_2^{\alpha} & V_3^{\alpha} & V_4^{\alpha} & V_5^{\alpha} \\ V_1^{\beta} & V_2^{\beta} & V_3^{\beta} & V_4^{\beta} & V_5^{\beta} \\ V_1^{x} & V_2^{x} & V_3^{x} & V_4^{x} & V_5^{x} \\ V_1^{y} & V_2^{y} & V_3^{y} & V_4^{y} & V_5^{y} \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_{ref} T_s \cos(\theta) \\ V_{ref} T_s \sin(\theta) \\ V_x \\ V_y \\ T_s \end{bmatrix} \quad (8)$$

where V_1^{α}, V_2^{α}, V_3^{α}, V_4^{α}, V_5^{α}, V_1^{β}, V_2^{β}, V_3^{β}, V_4^{β} and V_5^{β} are voltage vectors in optimum voltage vector combinations mapped to the α-axis and the β-axis, respectively. V_1^{x}, V_2^{x}, V_3^{x}, V_4^{x}, V_5^{x}, V_1^{y}, V_2^{y}, V_3^{y}, V_4^{y} and V_5^{y} are voltage vectors in optimum voltage vector combinations mapped to the *x*-axis and the *y*-axis, respectively. By setting the voltage references V_x and V_y to be zero, Eq. (8) becomes:

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \end{bmatrix} = \begin{bmatrix} 2\sqrt{6}H \cdot T_s \sin(\theta + 11\pi/12) \\ \sqrt{12/(2+\sqrt{3})}H \cdot T_s \sin(\theta + \pi/12) \\ T_s - 2\sqrt{3}H \cdot T_s \cos(\theta) \\ \sqrt{12/(2+\sqrt{3})}H \cdot T_s \sin(\theta + 11\pi/12) \\ 2\sqrt{6}H \cdot T_s \sin(\theta + \pi/12) \end{bmatrix} \quad (9)$$

where $H = V_{ref}/U_{dc}$, and the reference angle range is $-\pi/12 \le \theta \le \pi/12$. Since the dwell time of voltage vectors T_1, T_2, T_3, T_4 and T_5 should be above zero, it deduces the requirements that $T_s - 2\sqrt{3}HT_s\cos(\theta) \ge 0$ and $H \le 1/(2\sqrt{3}\cos\theta)$. On the boundary of sector I, $H \le 0.2887$ when $\theta = 0$. When $\theta = \pm\pi/12$, $H \le 0.2989$. Thus, the effective regions of optimum voltage vector combinations in sector I are determined as shown in Fig. 10. It is observed that there are 8 sub-sectors in sector I, corresponding to 8 optimum voltage vector combinations in Table V.

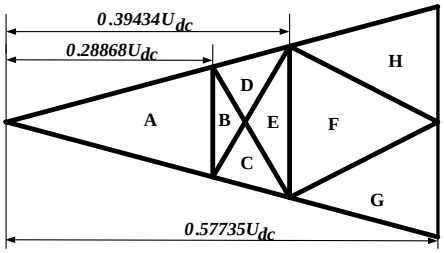

Fig. 10. Effective regions of optimum voltage vectors.

The determination of sub-sector containing reference voltage vector is taken by comparing the amplitudes of reference voltage vector and the amplitudes of boundaries of sub-sectors. Fig. 11 shows the criteria for determination of sub-sectors. For example, the boundaries of I-6 (sub-sector F1) are lines of *d-m3*, *m3-e* and *e-d*. The extending line of *d-m3* crosses the central line of sector 3 vertically at point *p6*, the extending line of *m3-e* crosses the central line of sector 11 vertically at point *p1*, and the extending line of *e-d* crosses the central line of sector 1 vertically at point *p4*. Thus, whether the voltage reference is located in sub-sector F1 is judged by comparing the amplitudes of voltage reference mapped to central lines (*o-d1*, *o-d3*, *o-d5*) and the amplitudes of boundaries of sub-sector mapped to central lines (*o-p1*, *o-p4*, *o-p6*). Table VI presents the criteria to determine the location of voltage vector in sector I. The maximum amplitudes of voltage reference vector under linear modulation would be $0.57735U_{dc}$.

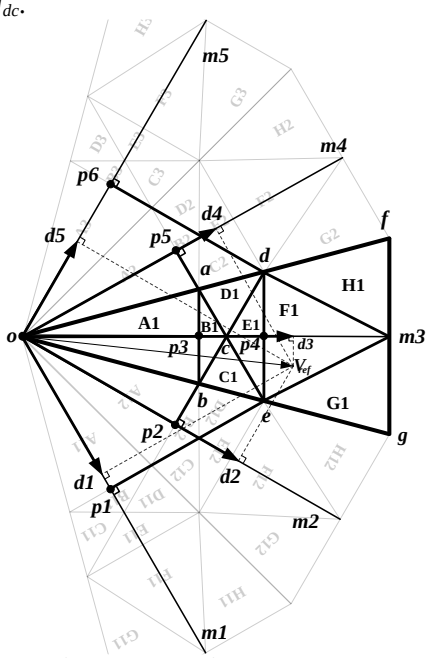

Fig. 11. Principle of determination of sub-sectors.

Table VI. The judgement criteria of vector reference in sector I.

Sub-sector	Criteria
A	*o–d3* ≤ *o–p3*
B	(*o–d2* ≤ *o–p2*)&&(*o–d3* > *o–p3*)&&(*o–d4* ≤ *o–p5*)
C	(*o–d2* > *o–p2*)&&(*o–d4* ≤ *o–p5*)
D	(*o–d2* ≤ *o–p2*)&&(*o–d4* > *o–p5*)
E	(*o–d2* > *o–p2*)&&(*o–d4* > *o–p5*)&&(*o–d3* ≤ *o–p4*)
F	(*o–d1* ≤ *o–p1*)&&(*o–d5* ≤ *o–p6*)&&(*o–d3* > *o–p4*)
G	*o–d1* > *o–p1*
H	*o–d5* > *o–p6*

The voltage fluctuation in mid-point of DC link of NPC-3L dual three-phase inverters can be controlled by using redundant voltage vectors. For instance, the voltage vectors 110001 and 221112 are two redundant small voltage vectors, which can generate the same phase voltages for NPC-3L dual three-phase inverters. However, they have different impacts on mid-point voltage of DC link. The voltage vector 110001 connects the phase loads to the lower capacitor and makes the lower capacitor voltage have a downward trend. So, it is the N-type voltage vector. The voltage vector 221112 connects the phase loads to the upper capacitor and makes the upper capacitor voltage have a upward trend. So, it is the P-type voltage vector.

The switching pattern of VSD-SVM should be designed not only to keep good harmonic performance but also to suppress the mid-point voltage fluctuation in DC link. With the optimum voltage vector combinations in Table V and the calculated dwelling time, the 11-section switching pattern is constructed as shown Fig. 12. The symmetric switching sequence in sector I-1 is formed as: 110001-111001-111111-120111-221111-221112-221111-120111-111111-111001-110001. The middle vector 221112 is the P-type voltage vector, and the N-type voltage vector, namely 110001 is distributed at two sides of the switching sequence. The balance factor λ is used to adjust the dwelling time between the P-type and N-type voltage

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vectors. The dwelling time of N-type voltage vector is defined as $T_{1n}=(1+\lambda)T_1/2$, while the dwelling time of P-type voltage vector is defined as $T_{1p}=(1-\lambda)T_1/2$. With feedback of voltage difference ΔU_c between the upper capacitor and the lower capacitor in DC link, the balance factor λ is tuned dynamically by bang-bang control. When ΔU_c is positive, λ is set as 0.8, otherwise λ=−0.8. The control diagram of traditional VSD-SVM is similar to that in last section. The only difference lies in that there is no closed-loop controller on *x-y* subspace of the traditional VSD-SVM. When there are low-order harmonics in back EMF and asymmetry in phase windings of electrical machine, there will be oscillating components on *x-y* subspace.

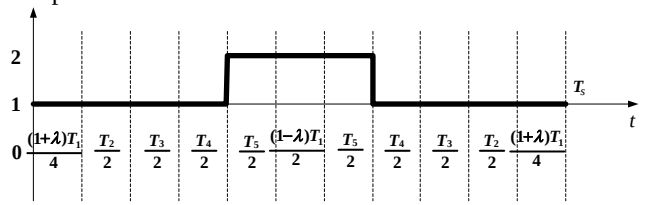

Fig. 12. Switching sequence of combination I-1 in sector I.

IV. Simulation and Experiments

The simulation is used to compare the performance of the proposed decoupled VSD-SVM with the traditional VSD-SVM by Matlab/Simulink. Table VII shows the parameters of a high-power medium-voltage dual three-phase PMSM drive system in simulation. Firstly, Fig. 13 and Fig. 14 are presented to compare the phase current waveforms between the traditional VSD-SVM and the propose decoupled VSD-SVM when the 100V (peak) 5th order harmonic exists in back EMF of electrical machine. Fig. 13(a) shows that the phase currents of electrical machine suffer from the distinct 5th order harmonics with traditional VSD-SVM because the traditional VSD-SVM method has no ability in suppressing current components on *x-y* subspace, as shown in Fig. 13(b). On the other hand, with the decoupled VSD-SVM, the closed-loop control of current components on *x-y* subspace can be achieved with control scheme in Fig. 14. Fig. 15 and Fig. 16 compare the drive performance when the inductance of phase B is 0.5mH larger than other phases. The unbalance in system parameters results in asymmetric phase current waveforms and distinct *x-y* subspace current components with traditional VSD-SVM, as shown in Fig. 15. On the other hand, Fig. 16 shows the phase currents are controlled balanced by suppressing current components on *x-y* subspace with the proposed decoupled VSD-SVM method.

Table VII. System parameters.

Name	Simulation (High-power drive)	Experiments (Low-power prototype)
Pole pair number n_p	8	3
PM flux ψ_f (peak)	4.971 Wb	0.2 Wb
Rate phase voltage (rms)	1236.6 V	110 V
Rated phase current (rms)	118.56 A	5.5 A
Rated frequency f	53.33 Hz	75 Hz
Stator resistor R_s	0.02421 Ω	0.21 Ω
Q-axis inductance L_d	9.816 mH	6.21 mH
D-axis inductance L_q	9.816 mH	6.21 mH
Stator leakage inductance L_{ls}	2 mH	5 mH
Load torque	20000 Nm	15 Nm
DC link voltage	4160 V	200 V
DC link capacitors	1000 μF	4000 μF
Sampling frequency f_s	5 kHz	5 kHz

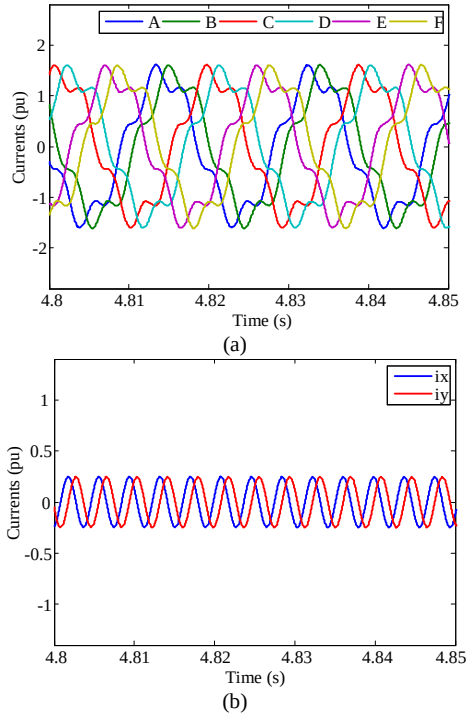

Fig. 13. Simulated performance of drive system with 5th order harmonics in back EMF of electrical machine using traditional VSD-SVM: (a) phase currents; (b) *x-y* current components.

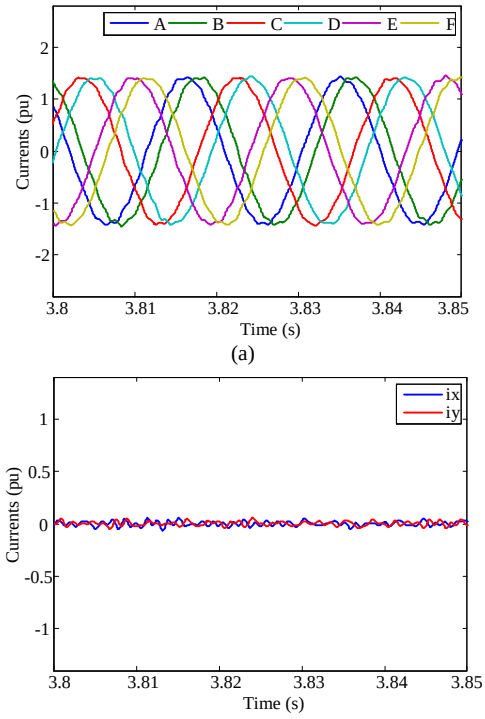

Fig. 14. Simulated performance of drive system with 5th order harmonics in back EMF of electrical machine using decoupled VSD-SVM: (a) phase currents; (b) *x-y* current components.

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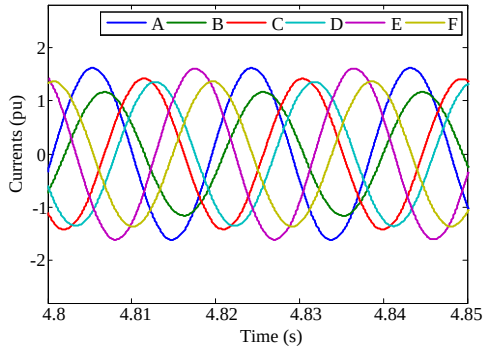
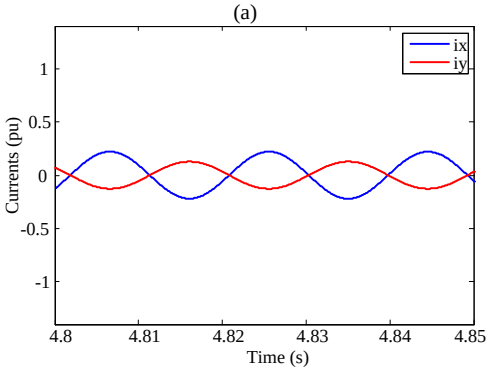
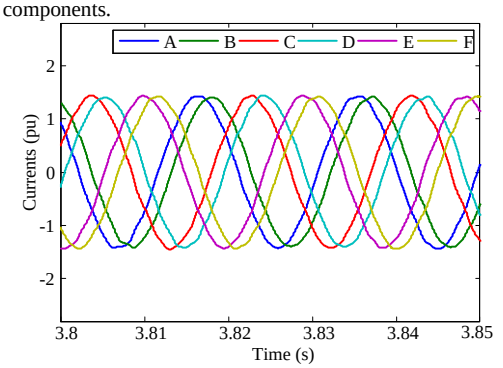


(a)

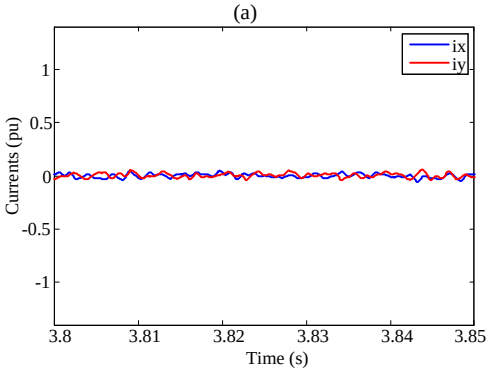


(b)

Fig. 15. Simulated performance of drive system with unbalanced phase inductances using traditional VSD-SVM: (a) phase currents; (b) *x-y* current components.



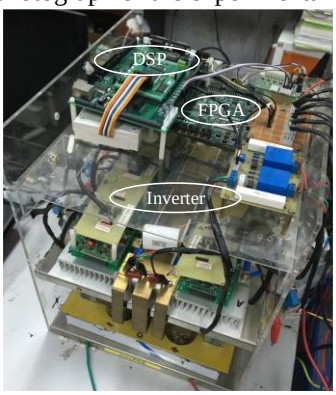
(a)



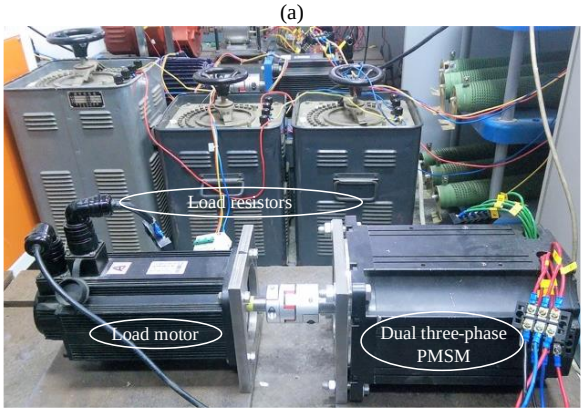
(b)

Fig. 16. Simulated performance of drive system with unbalanced phase inductances using proposed decoupled VSD-SVM: (a) phase currents; (b) *x-y* current components.

Secondly, a laboratory prototype of the dual-three NPC-3L inverter fed PMSM drive is built to verify the performance of the proposed decoupled VSD-SVM based control experimentally. The dual three-phase NPC-3L inverter is developed by using Infineon NPC-3L leg F3L100R07W2E3. The control chip consisting of DSP (TMS-F28335) and FPGA (Xinlix-Spartan6） are used to implement the control algorithms and switching strategies. Due to limit of experimental conditions in lab, a low-power dual three-phase PMSM system is used in experiments. The parameters of the laboratory prototype are also listed in Table VII. A permanent-magnetic synchronous generator (PMSG) acts as the electric load, which is coupled mechanically to the dual three-phase PMSM machine. Fig. 17 shows the photograph of the experimental setup.



(a)



(b)

Fig. 17. Photograph of experimental setup: (a) NPC-3L dual three-phase inverter; (b) dual three-phase PMSM drive.

Fig. 18 shows the measured steady-state performance of the NPC-3L inverters dual three-phase PMSM drive using the proposed decoupled VSD-SVM. The load torque is 9 Nm and the operating speed is 600 rpm. Fig. 18(a) shows the inverter produces the three-level output voltages in phase A and phase B. By using redundant voltage vectors of the proposed decoupled VSD-SVM in section II, the upper capacitor voltage and the lower capacitor voltage are balanced well in Fig. 18(b). Fig. 18(c) shows the current components on *x-y* subspace. When the closed-loop current controller on *x-y* subspace is not applied, the fundamental-frequency oscillation is observed in current components on *x-y* subspace clearly. The reason lies in that the parameters of the dual three-phase windings are not identical in practice. On the other hand, after using the closed-loop current controller on *x-y* subspace, the oscillation is suppressed effectively in Fig. 18(c). Thus, the symmetrical currents are presented in Fig. 18(d). The results agree with theoretical analysis and simulation results, which verifies that the proposed decoupled VSD-SVM based control can provide good control performance on both torque subspace and harmonic subspace.

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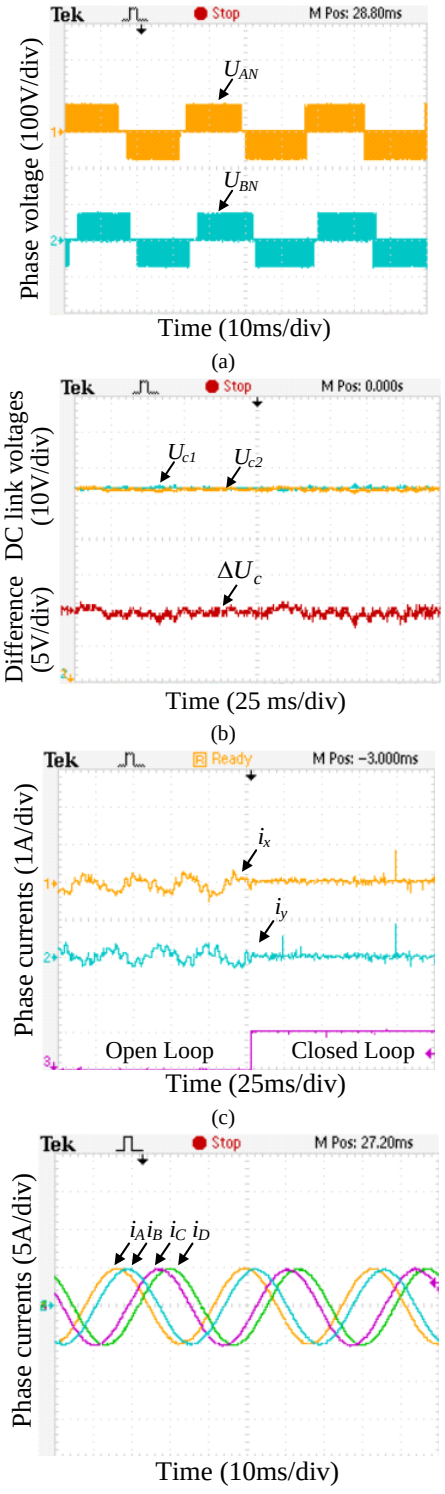
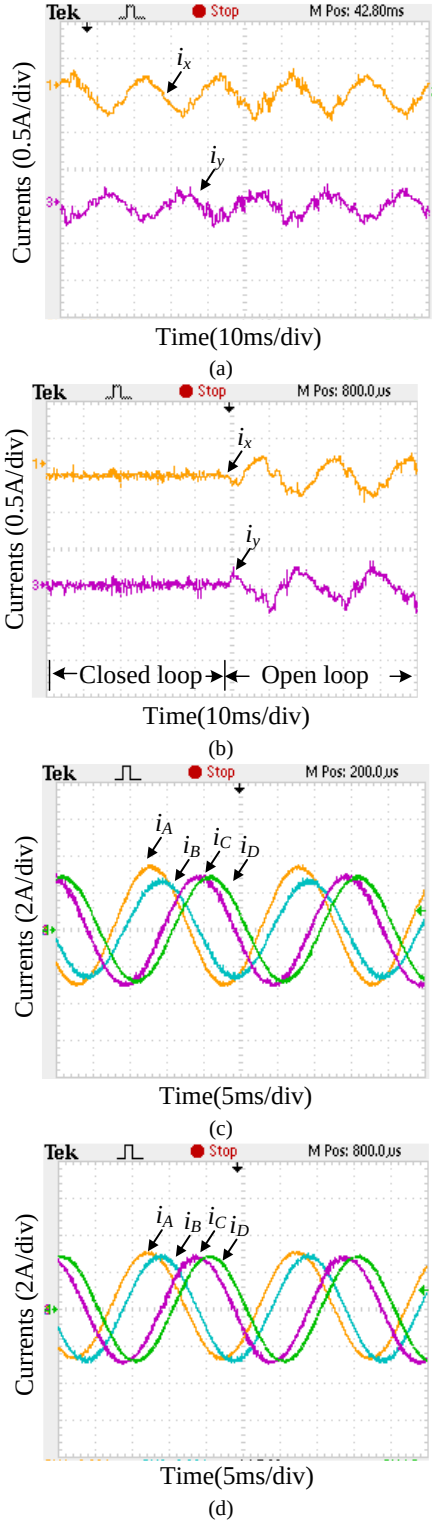


Fig. 18. Experimental results of steady-state performance of proposed control scheme based on decoupled VSD-SVM: (a) phase voltages versus mid-point of DC link; (b) DC link capacitor voltages; (c) *x-y* current components; (d) phase currents.

Fig. 19 compares the steady-state drive performance of the proposed decoupled VSD-SVM based control and the traditional VSD-SVM based control. To show the performance clearly, a resistor of 0.5 Ω is purposely added to phase B. Thus, distinct current component appears on *x-y* subspace with traditional VSD-SVM in Fig. 19(a). Hence, the dual three-phase windings suffer from asymmetric current waveforms in Fig. 19(c). On the other hand, the oscillating current components on *x-y* subspace are suppressed effectively by using the proposed decoupled VSD-SVM based control in Fig. 19(b), and the current waveforms of the dual three-phase windings are controlled symmetrical in Fig. 19(d). For both the traditional VSD-SVM and the proposed decoupled VSD-SVM, the upper capacitor voltage U_{c1} and the lower capacitor voltage U_{c2} are controlled effectively by tuning dwelling time of their redundant small voltage vectors. The results are shown in Fig. 19(e) and (f), respectively.



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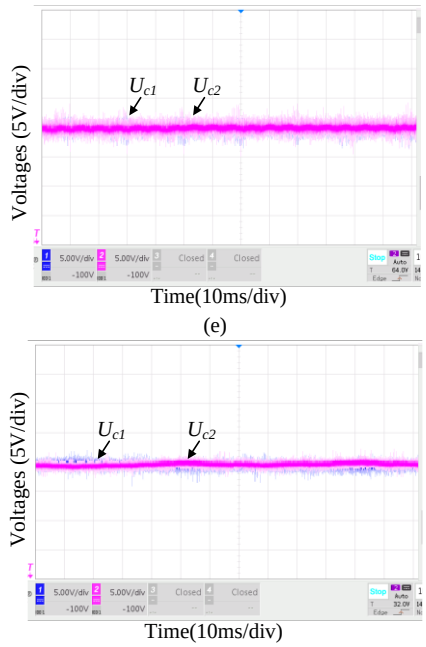

Fig. 19. Experimental comparison between the proposed decoupled VSD-SVM and the traditional VSD-SVM: (a) *x*-*y* current components using traditional VSD-SVM; (b) *x*-*y* current components using decoupled VSD-SVM; (c) phase currents using traditional VSD-SVM; (d) phase currents using decoupled VSD-SVM; (e) DC link voltages using traditional VSD-SVM; (f) DC link voltages using decoupled VSD-SVM.

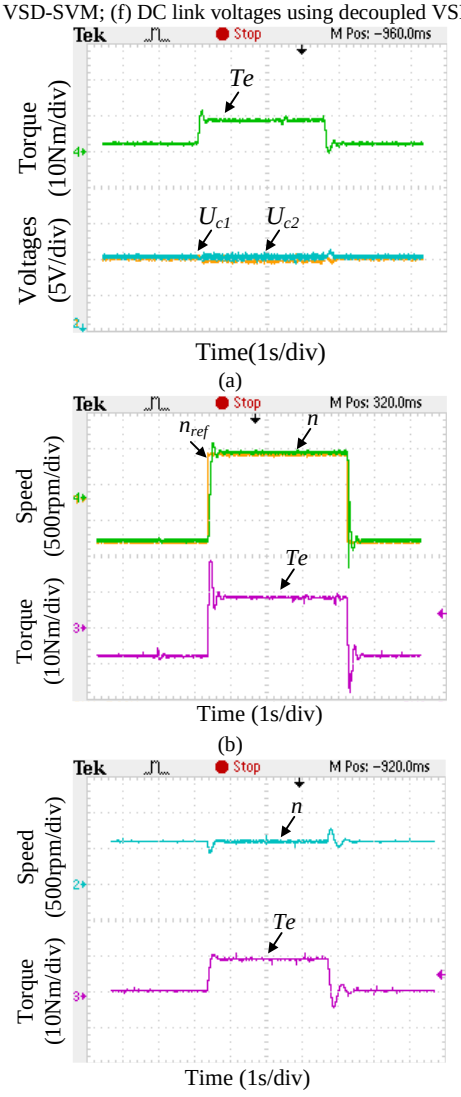

Fig. 20. Experimental results of dynamic response using decoupled VSD-SVM: (a) DC link voltages; (b) speed response; (c) torque response.

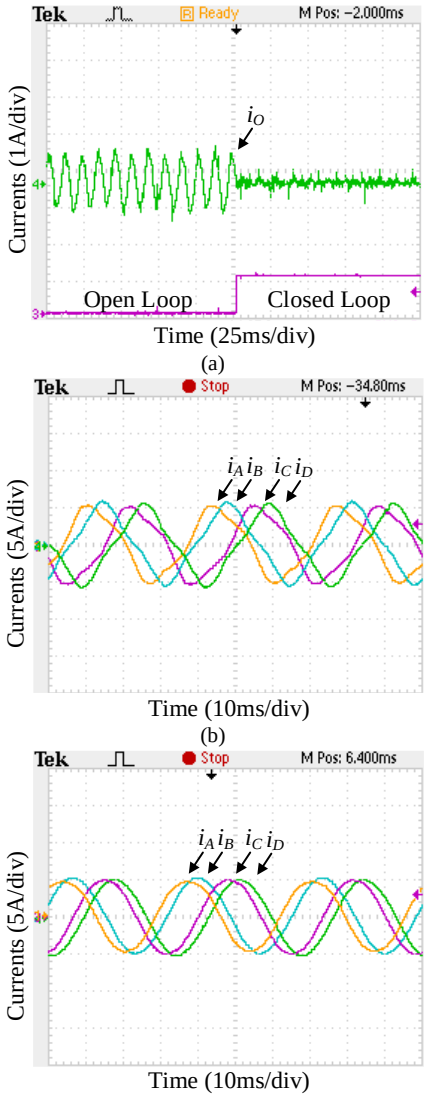

Fig. 21. Experimental results of dual three-phase PMSM drive with a common neutral using the proposed decoupled VSD-SVM: (a) zero-sequence current component; (b) phase currents without zero-sequence current suppression; (c) phase currents with zero-sequence current suppression.

Fig. 20 shows dynamic response of dual three-phase PMSM drives with the proposed decoupled VSD-SVM based control. Fig. 20(a) shows the DC link voltages dynamic when the load torque is switched between no load condition and 9 Nm. The upper capacitor voltage U_{c1} and the lower capacitor voltage U_{c2} are controlled effectively by redundant voltage vectors. Fig. 20(b) shows the speed response when the reference value is switched between –600 rpm and 600 rpm. The load torque value is 9 Nm. The speed tracks the reference value accurately. Fig. 20(c) shows the load torque response when the speed is maintained as 600 rpm. The load torque is switched between no load condition and 9 Nm. The drive also provides good performance during the dynamic process.

Thirdly, Fig. 21 shows operating performance of the dual three-phase PMSM drives when the two neutrals are connected together. As mentioned before, the zero-sequence current component will be generated due to different parameters of the two three-phase windings and different action instants of switches. As shown in Fig. 21(a), distinct current component i_O appears in zero-sequence dimension. Thus, the phase currents suffer from distorted waveforms in Fig. 21(b). By using zero-sequence voltage

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vectors mentioned in section II-C, the zero-sequence current component i_O is suppressed effectively in Fig. 21(a). The currents in dual three-phase windings become symmetrical and sinusoidal, as shown in Fig. 21(c). The speed is 600 rpm and the load is 9 Nm during the test.

Finally, the calculation time, harmonic performance and efficiency evaluation of the proposed decoupled VSD-SVM are compared with that of the traditional VSD-SVM. The carrier disposition based pulse width modulation (CDB-PWM) is also incorporated for comparison. Since only the harmonic performance of inverter voltage is investigated, the simple RL load is used. The resistive part in load R_s is 10Ω, and the inductive part in load L_s is 7mH. The output frequency is 50 Hz and the sampling frequency is 5 kHz. The total harmonic distortion (THD) values are calculated by considering frequencies below 21 kHz. The calculation time the traditional VSD-SVM, the proposed decoupled VSD-SVM and the CDB-PWM are 3.42×10^{-5}s, 2.08×10^{-5}s and 0.57×10^{-5}s respectively. The proposed decoupled VSD-SVM reduced the calculation time compared to the traditional VSD-SVM. The CDB-PWM is the fastest because it is the easiest to achieve, but it doesn't have the unique advantages such as digital implementation, high utilization of DC link voltage and well-defined switching vectors for fault tolerant operation which the SVM strategies have. Fig. 22 and Fig. 23 compare the THD performance of phase-to-phase voltage and phase voltage using the traditional VSD-SVM, the proposed decoupled VSD-SVM and the CDB-PWM, respectively. It can be observed that experimental results agree well with simulation results. The decoupled VSD-SVM offers the lower THD values compared to the other schemes when the modulation index is below 0.7. On the other hand, the THD values of the decoupled VSD-SVM are slightly higher when the modulation index is above 0.8. Table VIII compares the efficiency of the drive using the traditional VSD-SVM, the proposed decoupled VSD-SVM and the CDB-PWM. The losses in the drives are mainly conduction losses and switching losses. Conduction losses of devices are determined by the device saturation voltage and the instantaneous current passing through it. Switching losses are determined by the total commutation time when the device is turned on or off, and by the voltage and current across the device during the process [26]. In simulations, the device saturation voltage and the average current are used to calculate the conduction losses. The voltage and the current across the device during the commutation are used to calculate the switching losses. In experiments, the input power and output power are measured to calculate the efficiency. The switching losses are smaller than conduction losses. The conduction losses of three strategies are nearly the same thus the efficiency are nearly the same.

Table VIII. Efficiency of the drive using different modulation strategies.

Input power (W)	Power loss (W)			Efficiency (%)		
	Traditional VSD-SVM	Decoupled VSD-SVM	CDB-PWM	Traditional VSD-SVM	Decoupled VSD-SVM	CDB-PWM
235.9	19.1	18.8	18.2	91.9	92.0	92.3
323.1	23.6	22.6	21.6	92.7	93.0	93.3
429.9	27.1	25.8	24.9	93.7	94.0	94.2
542.7	29.8	27.7	28.2	94.5	94.9	94.8
670.2	32.8	32.1	31.5	95.1	95.2	95.3

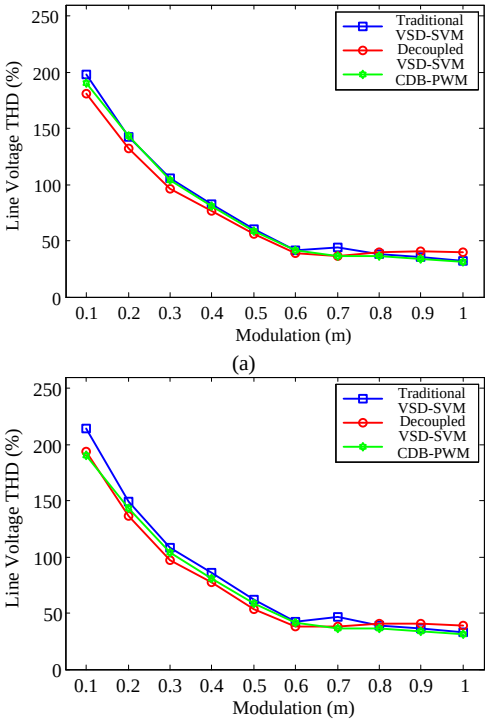

Fig. 22. Comparison of THD performance of phase-to-phase voltage using different modulation strategies: (a) simulation; (b) experiments.

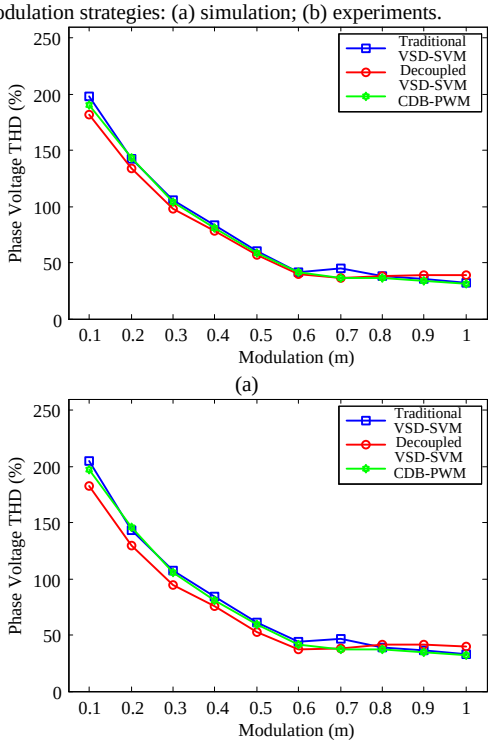

Fig. 23. Comparison of THD performance of phase voltage using different modulation strategies: (a) simulation; (b) experiments.

V. CONCLUSIONS

In this paper, the VSD based modulation and control schemes are studied for dual three-phase three-level PMSM drives. At first, a decoupled VSD-SVM strategy is proposed, where two groups of voltage vectors are selected to synthesize the voltage reference. The first group of voltage vectors participate in voltage synthesis on torque-component subspace (α-β subspace) while having no output on harmonic-component subspace (x-y subspace). The other group of voltage vectors are constructed to synthesize voltage reference on x-y subspace while having

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no impact on *α-β* subspace. Based on the two groups of decoupled voltage vectors, separate current controllers are designed on *α-β* subspace and *x-y* subspace, in such a way that the current components on *x-y* subspace induced by back EMF and unbalanced parameters can be suppressed effectively. Besides, the zero-sequence voltage vectors are incorporated in the modulation design to mitigate zero-sequence circulating currents caused by unbalanced parameters and asynchronous switching instants when different phase windings share one common neutral. The dwelling time of redundant small voltage vectors is adjusted to control voltage deviation in mid-point of DC link. For comparison, another VSD-SVM strategy is designed in this paper for NPC-3L inverters fed dual three-phase PMSM drives based traditional solution, where voltage vector synthesis is only considered on *α-β* subspace while limiting voltage components on *x-y* subspace to be zero. Both simulation and experiments have been given to compare the drive performance. It is verified that the proposed decoupled VSD-SVM can suppress the current components on *x-y* subspace, while the traditional VSD-SVM is lack of controllability on *x-y* subspace. Furthermore, good operation performance is offered by the proposed decoupled VSD-SVM in controlling zero-sequence current component and mid-point voltage of DC link. Finally, the harmonic performance of output voltages is compared among two VSD-SVM strategies and the carrier based PWM strategy. The proposed decoupled VSD-SVM offers lower THD values than the two other strategies under low modulation index, while suffering from slightly higher THD values under high modulation index.

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