

## Investigation of Tm<sub>2</sub>O<sub>3</sub> as a Gate Dielectric for Ge MOS Devices

L. Žurauskaitė<sup>a</sup>, L. Jones<sup>b</sup>, V. R. Dhanak<sup>c</sup>, I. Z. Mitrovic<sup>b</sup>, P. E. Hellström<sup>a</sup>, and M. Östling<sup>a</sup>

<sup>a</sup> Department of Electronics, KTH Royal Institute of Technology, Kista 164 40, Sweden

<sup>b</sup> Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool L69 3GJ, United Kingdom

<sup>c</sup> Department of Physics and Stephenson Institute for Renewable Energy, University of Liverpool, Liverpool L69 7ZF, United Kingdom

In this work atomic layer deposited Tm<sub>2</sub>O<sub>3</sub> has been investigated as a high-k dielectric for Ge-based gate stacks. It is shown that when Tm<sub>2</sub>O<sub>3</sub> is deposited on high-quality Ge/GeO<sub>2</sub> gates, the interface state density of the gate stack is degraded. A series of post-deposition anneals are studied in order to improve the interface state density of Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gates, and it is demonstrated that a rapid thermal anneal in O<sub>2</sub> ambient can effectively reduce the interface state density to below  $5 \cdot 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  without increasing the equivalent oxide thickness. Fixed charge density in Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gates has also been investigated, and it is shown that while O<sub>2</sub> post-deposition anneal improves the interface state density, the fixed charge density is degraded.

### Introduction

Germanium (Ge) has been intensively investigated as a high-mobility channel material alternative to silicon (Si). Formation of a high quality interfacial layer between the dielectric and Ge substrate is one of the crucial challenges regarding the fabrication of Ge metal-oxide-semiconductor (MOS) devices (1). Therefore, achieving a Ge gate stack with interface state density  $D_{it}$  compared to Si is essential for the competitive device performance. GeO<sub>2</sub> has been identified as a potential candidate for an interfacial layer (IL) due to effective Ge surface passivation with  $D_{it}$  in the range of  $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  (1). In order to achieve scaled effective oxide thickness (EOT) a combination of GeO<sub>2</sub> IL and a high-k dielectric is needed. However, it was shown that employing a conventional high-k dielectric such as HfO<sub>2</sub> degrades the electrical properties of Ge gate stacks due to intermixing of GeO<sub>2</sub> and HfO<sub>2</sub> (2). On the other hand, low interface state density in the range of  $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  has been achieved while employing Al<sub>2</sub>O<sub>3</sub> barrier (3) as well as rare earth oxides such as Y<sub>2</sub>O<sub>3</sub> (4). Therefore, a high-k rare-earth oxide with sufficient band offsets could be a good candidate for a high-k dielectric in Ge/GeO<sub>2</sub> gate stacks.

Rare-earth thulium oxide (Tm<sub>2</sub>O<sub>3</sub>) provides a high dielectric constant  $k \sim 16$  (5) and sufficient valence (3.05 eV) and conduction (2.05 eV) band offsets (6) for a high-k dielectric layer on Ge. In this work we investigate the effect of Tm<sub>2</sub>O<sub>3</sub> deposition on high-quality Ge/GeO<sub>2</sub> interfaces. The impact of the post-deposition anneal (PDA)

ambient, temperature and time on the interface state density, capacitance equivalent thickness (CET) and fixed charge in the gate stack is examined.

## Experiments

MOS capacitors were fabricated to evaluate the electrical properties of Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gate stacks. The process flow is depicted in Figure 1.

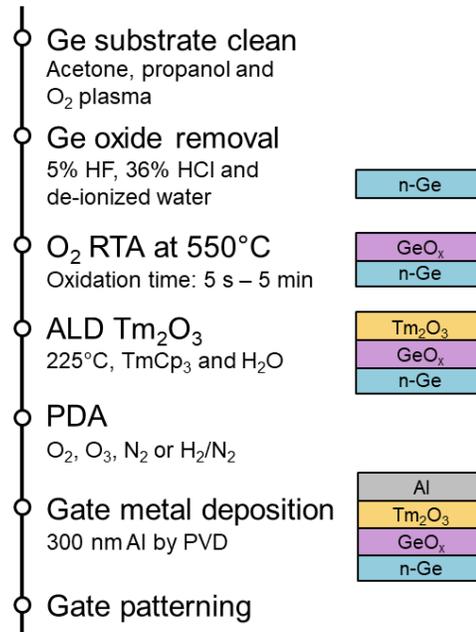


Figure 1. Process flow of Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> MOS capacitors. Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gate stacks are formed by thermal oxidation and subsequent Tm<sub>2</sub>O<sub>3</sub> deposition. The gates are then subjected to PDA at different ambients (O<sub>2</sub>, O<sub>3</sub>, N<sub>2</sub> or H<sub>2</sub>/N<sub>2</sub>) and temperatures (350 - 550 °C depending on the ambient).

In order to fabricate MOS capacitors, n-type Ge (100) substrates with doping concentration of  $\sim 10^{15} \text{ cm}^{-3}$  were cleaned with acetone, propanol and O<sub>2</sub> plasma. After native germanium oxide was removed with aqueous HF and HCl solutions and de-ionized water, the samples were immediately loaded into the rapid thermal anneal (RTA) chamber where oxidation was carried out at 550 °C for 5 s to 5 min. The temperature in the chamber is controlled by a pyrometer which is calibrated to a Si wafer, and oxidation is performed by placing a Ge substrate piece on a Si carrier wafer. The temperature of the Ge sample is thus lower than that of the Si wafer. After oxidation, the samples were loaded to atomic layer deposition (ALD) chamber where 40 cycles ( $\sim 7 \text{ nm}$ ) of Tm<sub>2</sub>O<sub>3</sub> were deposited using TmCp<sub>3</sub> and H<sub>2</sub>O as precursors. Then some of Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gate stacks were annealed in different ambients (O<sub>2</sub>, O<sub>3</sub>, N<sub>2</sub> and H<sub>2</sub>/N<sub>2</sub>) and temperatures (350 – 550 °C). Reference samples without Tm<sub>2</sub>O<sub>3</sub> deposition or without PDA were also fabricated. Al gate metal was deposited by physical vapor deposition and patterned.

MOS capacitors were electrically characterized with capacitance-voltage (CV) measurements. Interface state density in the midgap was evaluated from CV curves using a method described in (7). Some of the samples were investigated by X-ray photoelectron

spectroscopy (XPS) measurement in a chamber with a base pressure of  $5 \cdot 10^{-10}$  mbar and using Al K $\alpha$  X-ray (1486.6 eV) source. The Ge 3p spectra were calibrated using a measured GeO<sub>2</sub>/Ge substrate, and the position of its elemental germanium peak was used as a reference for all samples.

## Results and Discussion

### The impact of Tm<sub>2</sub>O<sub>3</sub> deposition on Ge/GeO<sub>2</sub> gates

Germanium MOS capacitors with Ge/GeO<sub>2</sub> gates and interface state density in the midgap below  $5 \cdot 10^{11}$  cm<sup>-2</sup>eV<sup>-1</sup> have already been realized by thermal oxidation in RTA chamber (7). The influence of Tm<sub>2</sub>O<sub>3</sub> deposition by ALD on these high-quality Ge/GeO<sub>2</sub> interfaces was determined by depositing a Tm<sub>2</sub>O<sub>3</sub> layer on Ge/GeO<sub>2</sub> stacks with varying GeO<sub>2</sub> thicknesses. Interface state density values in the midgap were extracted from the MOS capacitor CV measurements and are displayed in Figure 2. Tm<sub>2</sub>O<sub>3</sub> deposition degrades  $D_{it}$  in the midgap up to 5 times for low GeO<sub>2</sub> thickness (total CET < 5 nm). However, even for thick GeO<sub>2</sub> (total CET  $\geq$  9 nm)  $D_{it}$  is  $\sim 9 \cdot 10^{11}$  cm<sup>-2</sup>eV<sup>-1</sup> which is around two times higher than in reference MOS capacitors with Ge/GeO<sub>2</sub> gate stack. It is clear that the ALD Tm<sub>2</sub>O<sub>3</sub> layer deposition has a detrimental effect on the Ge/GeO<sub>2</sub> interface quality.

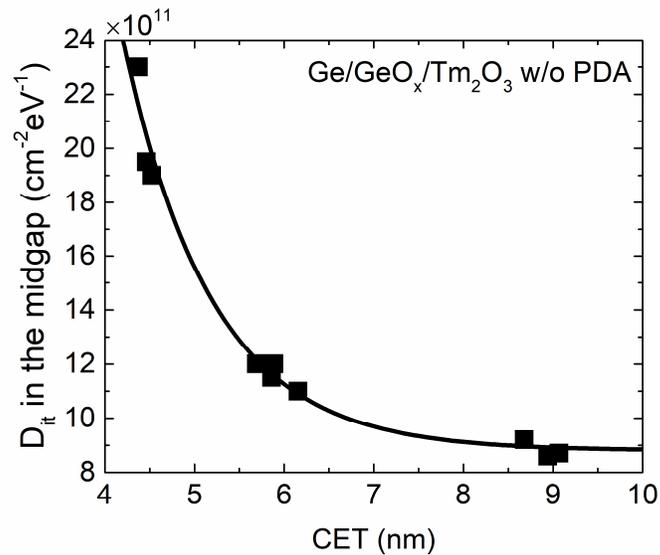


Figure 2.  $D_{it}$  in the midgap values for Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gate stacks with varying GeO<sub>x</sub> thickness.  $D_{it}$  decreases with increasing GeO<sub>x</sub> thickness and reaches  $\sim 9 \cdot 10^{11}$  cm<sup>-2</sup>eV<sup>-1</sup>. The line is an indicative guide for the eye.

### PDA influence on Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gates

Series of post-deposition anneals were performed on Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gates in order to investigate their impact on interface state density and capacitance equivalent thickness. PDAs in various ambients (O<sub>2</sub>, O<sub>3</sub>, N<sub>2</sub> or H<sub>2</sub>/N<sub>2</sub>) and temperatures (350 – 550 °C) were

carried out on the gate stacks with thin  $\text{GeO}_x$  ( $\text{GeO}_x$  thickness < 3 nm, total CET  $\sim 4.5$  nm in Figure 2). The impact of the anneals on  $D_{it}$  and CET is summarized in Figure 3.

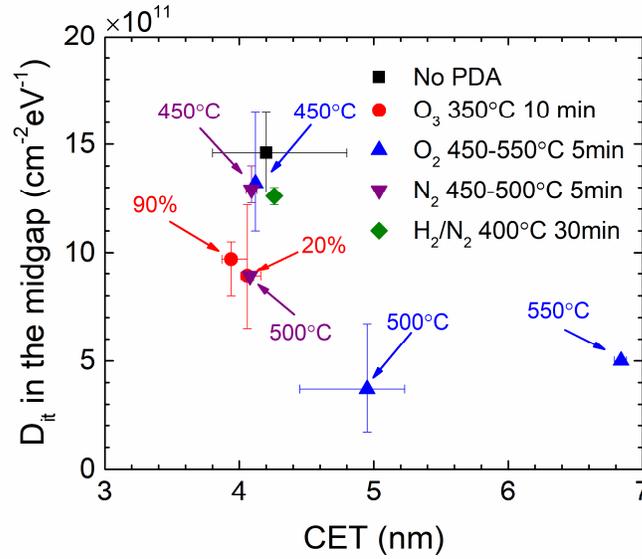


Figure 3.  $D_{it}$  in the midgap and CET values for Ge/ $\text{GeO}_x$ / $\text{Tm}_2\text{O}_3$  gate stacks after various post-deposition anneals. The anneals were performed in  $\text{O}_2$ ,  $\text{O}_3$ ,  $\text{N}_2$  or  $\text{H}_2/\text{N}_2$  ambient and at 350 – 550 °C.  $\text{O}_2$  anneal at 500 °C gives lowest  $D_{it}$  but with an increase in CET.

It was found that PDA in  $\text{N}_2$ ,  $\text{H}_2/\text{N}_2$  or  $\text{O}_2$  at temperatures below 500 °C does not significantly influence neither  $D_{it}$ , nor CET. PDA in ozone at 350 °C or  $\text{N}_2$  at 500 °C slightly reduces  $D_{it}$  to  $\sim 1 \cdot 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  without an increase in CET. On the other hand,  $\text{O}_2$  anneal at 500-550 °C significantly reduces the interface state density to similar values as in Ge/ $\text{GeO}_2$  gates.  $\text{O}_2$  PDA, however, increases the CET of the samples, and to a higher extent for higher PDA temperatures suggesting that  $\text{GeO}_x$  growth occurs during oxidation. This is further confirmed by XPS measurement of Ge/ $\text{GeO}_x$ / $\text{Tm}_2\text{O}_3$  stacks before and after  $\text{O}_2$  PDA at 500 °C. The obtained Ge 3p spectra are displayed in Figure 4. The ratio between  $\text{GeO}_x$  peak and Ge elemental peak in Ge 3p spectra grows after PDA in  $\text{O}_2$  confirming the growth of  $\text{GeO}_x$ . Moreover, in both spectra, before and after PDA, the difference between  $\text{GeO}_x$  peak and Ge elemental peak did not change suggesting that germinate was not formed after anneal. The binding energy difference is 2.6 eV which corresponds to  $\text{Ge}^{3+}$  oxidation state.

Even though  $\text{O}_2$  PDA at 500 °C offers the lowest  $D_{it}$  values, a 5 min anneal also increases the CET of the gate stack, which is unwanted for scaled MOS devices. Therefore, the impact of the anneal time was investigated. The results are shown in Figure 5 where  $D_{it}$  and CET values versus PDA time are displayed. It is shown that 1 min anneal is sufficient to decrease  $D_{it}$  to  $< 5 \cdot 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , and further oxidation does not improve the interface quality. CET also remains approximately the same after 1 min anneal but eventually starts increasing when oxidation continues. Therefore,  $\text{O}_2$  PDA at 500 °C for 1 min is concluded to be appropriate for Ge/ $\text{GeO}_x$ / $\text{Tm}_2\text{O}_3$  gates since low  $D_{it}$  values can be achieved without increasing CET.

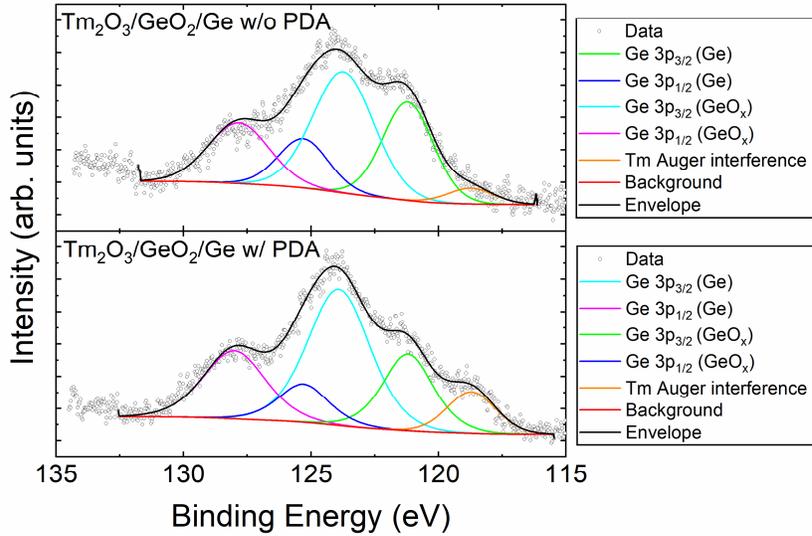


Figure 4. Ge 3p and spectra obtained by XPS measurements for Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gate stacks without (top) and with (bottom) O<sub>2</sub> PDA at 500 °C. The shift between Ge elemental and GeO<sub>x</sub> peaks corresponds to Ge<sup>3+</sup> oxidation state. The ratio between Ge elemental and GeO<sub>x</sub> peaks suggests GeO<sub>x</sub> growth during O<sub>2</sub> PDA.

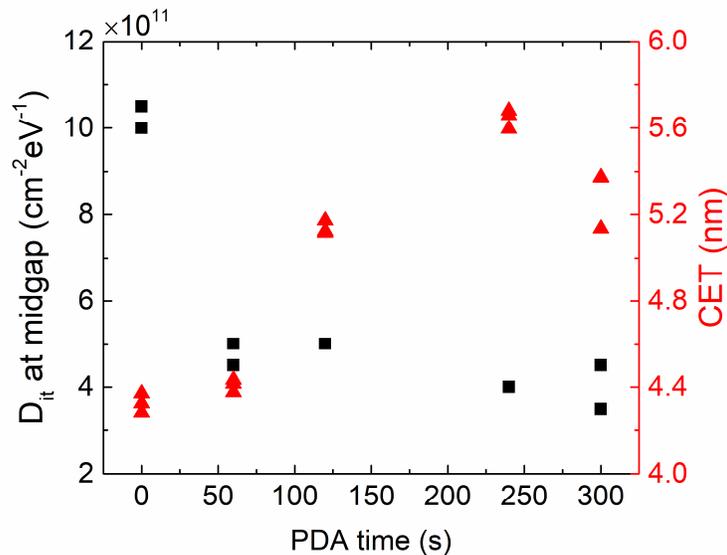


Figure 5. D<sub>it</sub> in the midgap and CET values for Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gate stacks after O<sub>2</sub> PDA at 500 °C for 0 – 5 min. D<sub>it</sub> decreases already after 1 min while CET only starts increasing after 2 min.

#### Fixed charges in Ge/GeO<sub>2</sub> and Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gates

Work function of Al electrode as well as fixed charge density N<sub>f</sub> of Ge/GeO<sub>2</sub> gates were calculated from flatband voltage V<sub>FB</sub> versus EOT plot which is displayed in Figure 6. The intercept is 0.11 V implying that Al work function is 4.34 eV which is in line with values calculated from Si/SiO<sub>2</sub>/Al MOS capacitors using the same method (8). Fixed charge extracted from the slope of the fitted line is ~5·10<sup>11</sup> cm<sup>-2</sup>, and the linear

shape of  $V_{FB}$  vs. EOT dependence suggests that the fixed charge is located at Ge/GeO<sub>2</sub> interface.

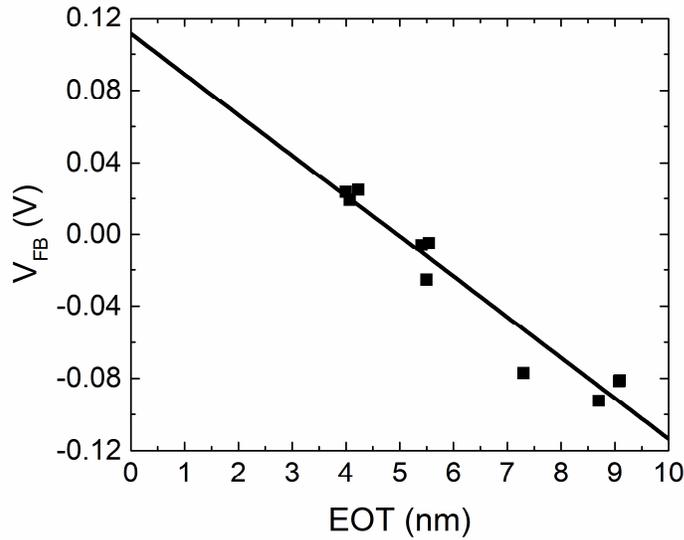


Figure 6. Flatband voltage  $V_{FB}$  vs. equivalent oxide thickness EOT of Ge/GeO<sub>2</sub> gate stacks with varying GeO<sub>2</sub> thickness. The amount of fixed charge density extracted from the slope of the linear fit is  $\sim 5 \cdot 10^{11} \text{ cm}^{-2}$ .

Fixed charge density in Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gate stacks with and without O<sub>2</sub> PDA at 500 °C was calculated assuming the previously estimated Al work function. Positive fixed charge of Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> stack before PDA is  $\sim 1 \cdot 10^{12} \text{ cm}^{-2}$ , and increases to  $\sim 2.5 \cdot 10^{12} \text{ cm}^{-2}$  after O<sub>2</sub> anneal. Positive fixed charge could be associated with Ge<sup>3+</sup> oxidation state since an oxygen vacancy in GeO<sub>2</sub> has been shown to be responsible for positive fixed charge near Ge/GeO<sub>x</sub> interface (9). The shift of the CV curve due to increased fixed charge is displayed in Figure 7a.

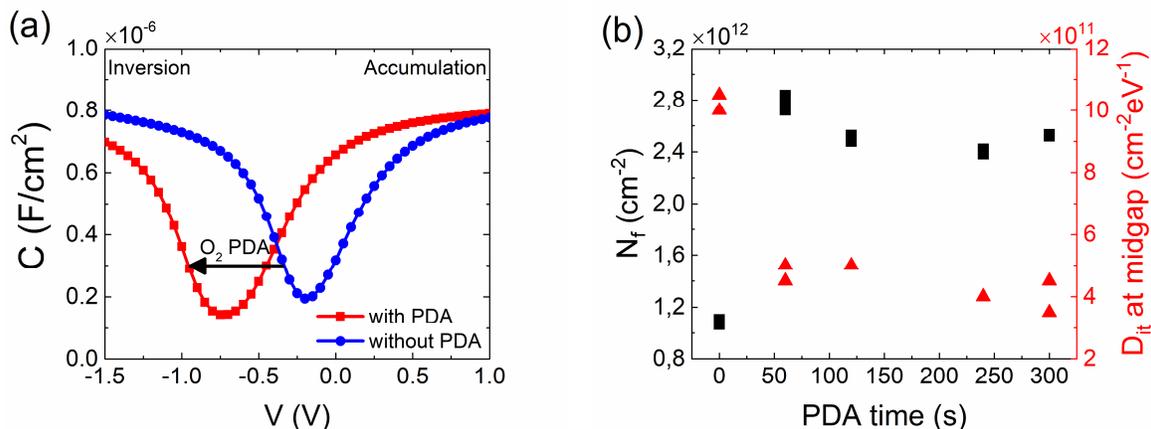


Figure 7. The influence of O<sub>2</sub> PDA at 500 °C on the fixed charge in Ge/GeO<sub>x</sub>/Tm<sub>2</sub>O<sub>3</sub> gate stacks: (a) CV characteristics before and after O<sub>2</sub> PDA for 1 min showing a shift to the left as the positive  $Q_f$  increases after PDA, (b)  $D_{it}$  decreases to  $< 5 \cdot 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  whereas  $Q_f$  increases to  $\sim 2.5 \cdot 10^{12} \text{ cm}^{-2}$  and does not significantly change for longer PDA.

Fixed charge reaches  $\sim 2.5 \cdot 10^{12} \text{ cm}^{-2}$  already after 1 min anneal (see Figure 7b) during which time  $D_{it}$  drops to  $< 5 \cdot 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ . Longer PDA does not significantly influence the fixed charge density. The correlation between decreasing interface state density and increasing fixed charge density suggests that the defects that were caused by ALD might be responsible for both, and PDA changes the energy level of the defects which turns interface states into fixed oxide charge.

## Conclusion

It has been shown that  $\text{Ti}_2\text{O}_3$  layer deposition by ALD increases  $D_{it}$  in high quality Ge/GeO<sub>2</sub> interfaces ( $D_{it} < 5 \cdot 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ). While interface state density is increased at least two times in all Ge/GeO<sub>x</sub>/Ti<sub>2</sub>O<sub>3</sub> MOS capacitors with varying GeO<sub>x</sub> thickness, this effect is much greater for the ones with thinnest GeO<sub>x</sub> (< 3 nm) when  $D_{it}$  increases up to 5 times. Nevertheless, optimized annealing conditions (O<sub>2</sub> RTA at 500 °C for 1 min) can reverse this effect and provide Ge/GeO<sub>x</sub>/Ti<sub>2</sub>O<sub>3</sub> gate stacks with low interface state density in the midgap ( $D_{it} < 5 \cdot 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ) without increasing CET. While this PDA decreases  $D_{it}$ , it has an opposite effect on the amount of fixed oxide charge which is increased to  $\sim 2.5 \cdot 10^{12} \text{ cm}^{-2}$ . This result suggests that the defects introduced during ALD are responsible for both interface states and fixed oxide charge.

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