Characterization of Transient Threshold Voltage Shifts in Enhancement- and Depletion-mode AlGaN/GaN Metal-Insulator-Semiconductor (MIS)-HEMTs

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Abstract

Both enhancement- and depletion-mode AlGaN/GaN metal-insulator-semiconductor HEMTs were fabricated with Al_2O_3 as the gate dielectric formed by atomic layer deposition (ALD). With the common problems of threshold voltage hysteresis in AlGaN/GaN MIS-HEMTs, DC I-V and fast transient I-V as well as frequency-dependent C-V measurements were performed to characterize the threshold voltage shifts ΔV_{th} and hence to systematically study the underlying mechanism. The experimental results reveal that ΔV_{th} can be as high as 1.0 V at $V_{G,max}$ = 5 V in transient I-V measurements despite the much lower values of 0.42 V in static and CV measurements. This has significant implications in using AlGaN/GaN MIS-HEMTs for high voltage switching applications. Besides, multi-frequency C-V measurements show that the primary ΔV_{th} is frequency independent but the second onset of voltage shifts (ΔV_2) shows obvious frequency dependence. These results imply the likely mechanism of slow (deep) Al_2O_3 interface traps accounting for ΔV_1 hysteresis, and fast (shallow) interface traps accounting for ΔV_2.

Key words: AlGaN/GaN MIS-HEMT, Al_2O_3/III-N interface traps (fast and slow) and threshold voltage hysteresis.

Introduction

AlGaN/GaN heterostructure-based high electron mobility transistors (HEMTs) are promising electronic devices for high frequency, high voltage and high temperature applications. Most of the reported AlGaN/GaN HEMTs are depletion-mode (D-mode) devices due to the nature of two-dimensional electron gas (2DEG) at the AlGaN/GaN hetero-interface. Various techniques have been developed to realize the normally-off enhancement-mode (E-mode) operation, such as gate recess [1], fluorine plasma treatment [2] and p-type cap layer engineering [3]. In the realization of D- and E-mode devices, gate insulator can be used to suppress the gate leakage current in AlGaN/GaN metal insulator semiconductor (MIS)-HEMTs. However, V_{th} hysteresis (ΔV_{th}) at large forward gate bias have been commonly reported in AlGaN/GaN MIS-HEMTs. The cause of V_{th} hysteresis is attributed to dielectric induced defect states at the dielectric/III-N interface. Different experimental efforts [4]-[7] have been attempted to the reduce V_{th} hysteresis. So far, very few research has been reported on the systematic studies of Al_2O_3/III-N interface states that induce ΔV_{th} hysteresis.

In this work, we use a combination of standard I-V, fast-ramp I-V and frequency-dependent C-V measurements to characterize the shifts in V_{th} of both E-mode and D-mode MIS-HEMTs for better understanding of the dielectric induced V_{th} hysteresis.

Experiments

The AlGaN/GaN epitaxy used in this work consists of a 4-µm GaN buffer on a Si substrate, a 0.4-µm AlN spacer, a 23-nm $Al_{0.25}Ga_{0.75}N$ barrier and a 3-nm GaN cap layer. The fabrication process started with mesa etching and the Au-free source and drain ohmic contacts were formed by e-beam evaporation of Ti/Al/Ni/TiN (25/125/45/55 nm) metal stacks. Annealing at 800 °C for 45 s in N_2 ambient was then performed by rapid thermal annealing (RTA). The contact resistance R_C is 1.3 Ω • mm.

Both D-mode and E-mode MIS-HEMTs were fabricated on the same wafer substrate in the first sample (referred to as sample A), with the structures and process steps shown in Fig. 1(a) and (b) respectively. 300 nm plasma enhanced vapor deposition (PECVD) SiN_x was deposited as an etching hard mask for the E-mode gate recess. Digital etching using O_2 plasma treatment at the GaN surface for 3 min at 60 °C with an RF power of 100 W was performed. Afterwards, the oxidation layer was removed by wet etching in 1:10 hydrochloric acid for 1 min, after 40 cycles of digital etching. A partial recess depth of around 22 nm was verified by atomic force microscopy (AFM) for a slow etch rate of about 0.6 nm per cycle. 15 nm ALD Al_2O_3 gate dielectric for E/D-mode was deposited and Ni/TiN were finally evaporated as the gate metal.

For comparison purposes, sample B of HEMTs was also fabricated but without the Al_2O_3 dielectric to study the III-N body induced ΔV_{th} hysteresis.

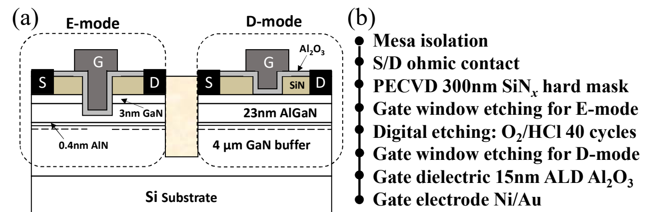

Fig. 1. (a) Schematic diagram and (b) fabrication steps of E- and D-mode MIS-HEMTs fabricated on the same substrate in sample A.

Results and Discussion

Figs. 2(a) and 2(b) respectively show the typical I_D-V_G (linear and semi-log scale) of the D-mode and E-mode MIS-HEMTs of sample A. The threshold voltage V_{th} is about -10.4 V for the D-mode device and +0.6 V for the E-mode device as determined by extrapolation in the linear region. Both devices show similarly high on/off current ratio of 10^8.

Bi-directional DC current-voltage (I-V) tests were performed to study the ΔV_{th} hysteresis (the shift in V_{th} between the up and down sweeps) at different maximum gate voltage $V_{G,max}$. During the up sweep, gate injection electrons are trapped by the dielectric/III-N interface states, and only fast electrons can emit during the down sweep. Deep acceptor-like traps (slow traps) cannot emit electrons and are usually

negatively charged. They can partially deplete 2DEG electrons and therefore induce a positive shift of V_{th} during down sweep [8]. Solid lines in Fig.3 (c) show the static V_{th} hysteresis of the D-mode (black line) and E-mode (red line) MIS-HEMTs with ALD-formed Al_2O_3 in sample A, and D-mode (blue line) HEMT without Al_2O_3 in sample B. The V_{th} hysteresis at different $V_{G,max}$ is similar for both D-mode and E-mode devices of sample A. This indicates that the V_{th} hysteresis induced by gate injection electrons is not related to the AlGaN barrier, but the ALD-formed Al_2O_3 gate dielectric. This can also be confirmed by measurement results (blue line) of sample B because V_{th} hysteresis without Al_2O_3 is negligible at $V_{G,max} < 5$ V compared with sample A. The small ΔV_{th} at $V_{G,max} = 5$ V might be caused by large gate leakage current (which is not shown here).

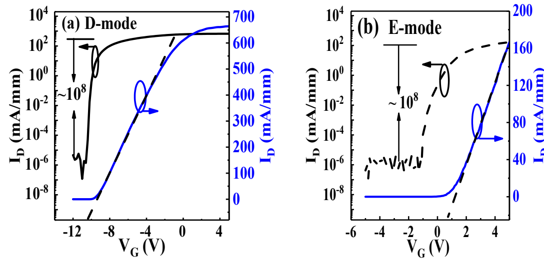

Fig. 2. Transfer characteristics of D-mode (a) and E-mode (b) MIS-HEMTs of sample A. (device dimension: $L_{GS}/W_G/L_G/L_{GD}$ = 5 /50 /3 /10 µm).

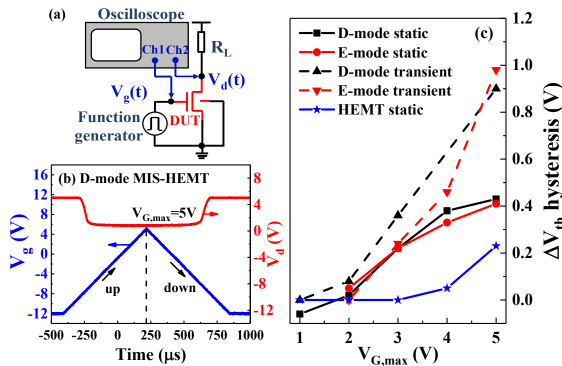

Fig. 3. Experimental setup for transient measurements with R_L = 1 kΩ. (b) Triangular waveform V_g (t) and response V_d (t). (c) $V_{G,max}$ dependent ΔV_{th} comparison between fast transient and static I-V measurements for E- and D-mode MIS-HEMTs with Al_2O_3 in sample A, and static I-V for D-mode HEMTs without Al_2O_3 in sample B.

Fig. 3(a) shows the fast transient measurement setup as described in [9] to study the dynamic V_{th} hysteresis. The device under test (DUT) is connected in series with a load resistor R_L =1 kΩ. The waveform of the fast ramp gate voltage V_g (t) and the corresponding drain voltage response V_d (t) are simultaneously recorded by a digital oscilloscope in Fig. 3(b). The calculated I_d-V_g curves are used to extract ΔV_{th} between ramp-up and ramp-down. Fig. 3(c) gives ΔV_{th} comparison between the fast transient and static measurements for both D-mode and E-mode MIS-HEMTs in sample A. It can be seen that ΔV_{th} of transient measurements is always larger than that of static measurements. The discrepancies become increasingly large with high $V_{G,max}$. ΔV_{th} is less than 0.45 V for both E- and D-mode devices in static tests while ΔV_{th} can be up to 1 V in transient tests at $V_{G,max}$=5 V. As a result, ΔV_{th} hysteresis can be much underestimated in conventional "slow" quasi-static measurements, due to recovery effects during relatively long measurement delay. Besides, higher $V_{G,max}$ leads to excessive filling of shallower (or fast) traps that can be detected by only fast transient I-V, but not the static tests [9].

To study fast traps of Al_2O_3/III-N interface states and their impact on V_{th} hysteresis, frequency-dependent C-V measurements were performed. Figs. 4(a) and 4(b) respectively show frequency-dependent C-V curves of D-mode and E-mode MIS capacitors in sample A. The normal Al_2O_3/AlGaN/GaN capacitor exhibits two rising slopes, with the first slope around -8 V related to 2DEG formation and the second slope around 5 V related to the Al_2O_3/AlGaN interface. The second slope reflects the electron transfer from the AlGaN/GaN interface to the Al_2O_3/AlGaN interfaces [7]. Fig. 4(c) shows the dependence of ΔV_{th} on the interface emission time constant $\tau_{emission}$, with ΔV_1 at 100 nF/cm^2 and ΔV_2 at 220 nF /cm^2. ΔV_2 increases with $\tau_{emission}$, indicating that fast traps ($\tau_{emission}$ from ms to several µs) contribute to the onset of voltage hysteresis ΔV_2 of the MIS capacitors but have little impact on ΔV_1.

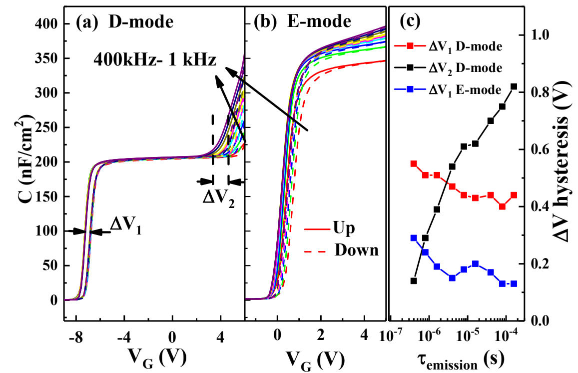

Fig. 4. Frequency-dependent C-V curves. (a) D-mode and (b) E-mode MIS capacitors of sample A. (c) Frequency-dependent voltage hysteresis (ΔV_1 for the first slope and ΔV_2 for second slope).

Conclusion

V_{th} hysteresis has been systematically studied in E-mode and D-mode AlGaN/GaN MIS-HEMTs by DC I-V, fast ramp I-V and frequency-dependent C-V measurements. Larger ΔV_{th} are obtained from transient I-V measurements and the worse V_{th} hysteresis is related to fast (shallow) traps at the Al_2O_3/III-N interface. The V_{th} hysteresis is underestimated in common static measurements of AlGaN/GaN MIS-HEMTs.

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