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Highly Reliable Back-To-Back Power Converter without Redundant Bridge Arm for Doubly-Fed Induction Generator-Based Wind Turbine

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***Abstract* -- In this paper, a highly reliable back-to-back (BTB) power converter is proposed for doubly-fed induction generator-based wind turbines (DFIG-WTs). When a power switch open-circuit fault is encountered in either the grid-side converter (GSC) or rotor-side converter (RSC), a four-switch three-phase (FSTP) topology is formed to avoid using redundant bridge arms, which reduces the power circuit complexity and minimizes the conduction and switching losses. A simplified space vector pulse width modulation (SVPWM) technique is used to eliminate sector identification and complex trigonometric calculations. In addition, the influence of DC-bus capacitor voltage unbalance on the electromagnetic torque is analyzed in detail. The offset current components are calculated, and they are deducted from the reference values in the modified control strategies to suppress the DC-bus voltage deviation. Moreover, the power loss model of BTB converter is analyzed in detail, and the efficiency study is performed in various post-fault situations. Simulations in Matlab/Simulink are carried out to verify the performance of a DFIG-WT based on FSTP BTB converter. Furthermore, the control hardware-in-the-loop (CHIL) setup with RSC and GSC separately simulated in a digital real-time simulator (DRTS) is applied for experimental verification of the proposed control strategy.**

***Index Terms*-- back-to-back converter, doubly-fed induction generator-based wind turbine, four-switch three-phase, DC-bus voltage unbalance, efficiency study, control hardware-in-the-loop.**

NOMENCLATURE

V_{dc}, V_{C1}, V_{C2}	DC-link voltage, upper and lower capacitor voltages
ΔV	DC-bus voltage difference (V_{C1} - V_{C2})
V_m, I_m; ϕ	Amplitudes of the three-phase voltages and currents; Phase angle difference between voltage and current
i_{C1}, i_{C2}	Upper and lower capacitor currents
p	Derivative calculator d/dt
e_{ga}, e_{gb}, e_{gc}	Three-phase grid AC voltages
v_{ga}, v_{gb}, v_{gc}	Three-phase GSC AC voltages
v_{sa}, v_{sb}, v_{sc}	Three-phase stator AC voltages
v_{ra}, v_{rb}, v_{rc}	Three-phase rotor AC voltages
φ_s, φ_r	Stator and rotor fluxes
i_g, i_r	Upper bridge GSC and RSC total currents
i_{ga}, i_{gb}, i_{gc}	Three-phase GSC AC currents
i_{ra}, i_{rb}, i_{rc}	Three-phase RSC AC currents
i_{ms}	Equivalent field current
R_g, R_s, R_r	Resistances on the grid, stator and rotor
L_m, L_{ls}, L_{lr}	Mutual inductance, stator leakage inductance and rotor leakage inductance
L_g, L_s, L_r	Inductances on the grid, stator and rotor ($L_s = L_m + L_{ls}$; $L_r = L_m + L_{lr}$)
C_{DC}	DC-link capacitance
S_a, S_b, S_c	Switching functions of three bridge arms
n_s	Number of power switches
σ	Leakage flux factor: $\sigma = 1-[L_m^2 / (L_r L_s)]$
P_s, Q_s	Stator output active and reactive power
P_r, Q_r	Rotor output active and reactive power
P_g, Q_g	Grid-side output active and reactive power
P_t, Q_t	Total output active and reactive power
d	Duty ratio
f_{NOM}	Nominal grid frequency
θ_s, θ_r, θ_{slip}	Grid voltage angle, rotor angle, and slip angle ($\theta_{slip} = \theta_s - \theta_r$)
ω_s, ω_{slip}, ω_r, ω_m	Nominal grid angular frequency, slip angular frequency, electrical rotor angular speed and mechanical rotor angular speed
T_s, T_{sw}	Sampling time and switching time
T_e, T_m	Electromagnetic torque, mechanical torque
n_p	Number of pole pairs
J	Inertia of wind turbine
η	Power efficiency
k_{vp}, k_{vi}	Voltage controller proportional and integral gains
k_s	Stator coupling factor: $k_s = L_m/L_s$
K_p	DC-bus voltage deviation suppresion controller proportional gain
P_{cl}, P_{DC}	Copper losses and DC-bus power losses
$P_{cond,T}$, $P_{cond,D}$	Power losses on the transistor and diode
$P_{sw,T}$, $P_{sw,rr}$	Power losses during the switching and reverse recovery periods
V_{CE0}, V_{F0}	Collector-emitter threshold voltage and diode forward threshold voltage
i_{CE}, i_F	Collector-emitter and diode forward currents
r_{CE}, r_F	On-state slope resistances for the transistor and diode
E_{sw}, E_{rr}	Energy dissipation during the switching and reverse recovery periods
$T_{sw,T}$, $T_{rr,d}$	Temperature coefficients of the transistor and diode switching losses
T_j	Junction temperature
$K_{v,T}$	Exponent for the voltage dependence of the transistor switching losses
$K_{v,d}$, $K_{i,d}$	Exponents for the voltage and current dependence of the diode switching losses

Subscripts & Superscripts

α, β	Direct and quadrature components referred to the stationary reference frame
d, q	Direct and quadrature components referred to the synchrnous reference frame
*ref; ref*1	AC and DC reference values

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*	Ideal value
-	Offset value

I. Introduction

TO reduce the volume of back-to-back (BTB) converter and realize flexible active and reactive power control, doubly-fed induction generator based wind turbines (DFIG-WTs) are commonly applied in wind energy conversion systems (WECSs), taking up around 50% of the wind turbines in the global wind energy market [1, 2]. As many DFIG-WTs are approaching the late stage of service time, aging issues occur, and the deteriorated performance for some components is encountered. Therefore, high reliability is required, especially for offshore wind turbines, where maintenance is difficult and expensive to be undertaken [3]. According to [4], the power module in a DFIG-WT is most likely to fail, where the failure rate of converter is the highest. In this paper, the main target is increasing the reliability of BTB converter in DFIG-WT.

The control of the grid-side and rotor-side converters (GSC and RSC) is of paramount significance to the normal operation of DFIG-WTs. GSC is responsible for maintaining a stable DC-bus voltage, achieving sinusoidal grid current waveforms and adjusting the power factor, while RSC is used to regulate the stator active and reactive power outputs [5-7]. Apart from the common six-switch three-phase (SSTP) converter topology, various other categories of BTB converters were also investigated. Owing to the advantage of eliminating the bulky DC-link capacitor, indirect matrix converters were applied in [8, 9] to control DFIG-WTs. In addition, three single-phase BTB converters were involved in a power sharing unit by using delta-connection in [10], so as to realize power exchange even if one of the DC-links fails. Besides, in [11], a self-tuning resonant control strategy was proposed for a seven-leg BTB voltage source inverter (VSI) interfaced with a permanent magnet synchronous generator (PMSG). Moreover, a BTB neutral-point clamped (NPC) converter-based PMSG wind power system was investigated in [12], and the system operating requirements were met by applying the model predictive control (MPC) strategy. Furthermore, an adaptive control scheme was proposed for parallel BTB wind power converters in [13], with improved efficiency and reliability achieved by power allocation optimization.

However, as the semiconductor devices in a converter are fragile, breakdown of these devices contributes to a large proportion of faults in converters, accounting for up to 21% of the total failure scenarios [14]. According to [15], in terms of the solutions to switch-level faults, the methods of utilizing inherently redundant switching states [16], DC-bus midpoint connection [17] and installing redundant parallel or series switches [18] have been investigated by many researchers. Taking the factors of minimum space occupation, switching and conduction losses into consideration, the second scheme is chosen in this paper. This kind of fault-tolerant topology is called four-switch three-phase (FSTP) [19].

In [20], a general pulse width modulation (PWM) strategy was proposed for FSTP inverters of induction motors. For the purpose of designing the controllers of FSTP voltage source rectifiers (VSRs), a *dq* model was first proposed for FSTP VSR in [21]. In this topology, two DC-link capacitors are applied to sustain a stable DC-bus voltage, and in each switching state, only the voltage on one capacitor is utilized, which obviously reduces the DC-bus voltage utilization rate. In addition, DC-link capacitor voltage deviation and more current harmonics are induced by applying this topology [22-24]. In [25], the double Fourier integral analysis approach was first applied to analyse the spectrum of DC-link currents by considering its effect on balancing the DC-link capacitor voltages. Furthermore, there is no intrinsic zero vector in FSTP topology, and it has to be synthesized in the modulation process. The effects of zero vector distribution on the performance of FSTP rectifiers and hybrid PWM techniques were researched in [26, 27].

Regarding the application of FSTP topology in a BTB three-phase converter, the authors in [28] proposed an eight-switch based current-controlled power converter. However, the issue of DC-bus voltage unbalance was not analysed in depth. As another competitive candidate in the wind energy market, PMSGs attract the attention of many researchers in converter fault tolerance [29-31], and the operation of a converter with two bridge arms at each side was investigated by applying hysteresis current control (HCC) in [30]. In [32], both the FSTP topology based GSC and RSC were used in DFIG-WT, but the modulation technique is based on all the four switching states, which increases the switching losses. Furthermore, a simplified space vector PWM (SVPWM) was utilized in [33] for post-fault DFIG-WTs. However, only the fault in RSC was considered.

In this paper, based on the work in [33], FSTP topology is employed in both the GSC and RSC in DFIG-WT to further increase the system reliability. The unified expressions for the duty cycles in the healthy bridge arms are derived for modulation simplification. In addition, the influence of DC-bus voltage unbalance on the electromagnetic torque is analysed in detail by applying different proportional gains in the DC-bus voltage deviation suppression process. Moreover, the efficiency study of BTB converter under different post-fault scenarios is carried out to further investigate the feasibility of DC-bus voltage deviation suppression control. Furthermore, the post-fault DFIG-WT with FSTP converter is verified in Matlab/Simulink 2017a, and the experimental results are obtained in the control hardware-in-the-loop (CHIL) setup. The power circuits of RSC and GSC are simulated in a digital real-time simulator (DRTS), and the control algorithm is implemented in a hardware controller.

The paper is arranged in the following structure: In Section II, the *dq* dynamic model of DFIG is established in the

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synchronous reference frame. The configuration and modelling of FSTP topology-based DFIG-WT are illustrated in Section III. Then, the proposed modulation technique is depicted in Section IV, and the control strategies are explained in Section V. Afterwards, the efficiency study is conducted in Section VI for BTB converter in various post-fault situations. To validate the proposed method for post-fault operation of DFIG-WT, the simulation and CHIL implementation are separately carried out in Section VII and Section VIII. In Section IX, the comparison between simulation and experimental results is discussed. Finally, the conclusion is given in Section X.

II. Modelling of DFIG in Synchronous Reference Frame

In this paper, grid voltage orientation (GVO) is applied for vector angle determination. The angular speed of *dq* axis is selected as the grid synchronous angular frequency ω_s, and then the voltage and flux equations of DFIG can be written as

$$\begin{cases} \vec{v}_s = R_s\vec{i}_s + p\vec{\varphi}_s + j\omega_s\vec{\varphi}_s \\ \vec{v}_r = R_r\vec{i}_r + p\vec{\varphi}_r + j\omega_{slip}\vec{\varphi}_r \end{cases} \tag{1}$$

$$\begin{cases} \vec{\varphi}_s = L_s\vec{i}_s + L_m\vec{i}_r \\ \vec{\varphi}_r = L_m\vec{i}_s + L_r\vec{i}_r \end{cases} \tag{2}$$

To reveal the field current effect more clearly, the stator flux can also be illustrated as

$$\vec{\varphi}_s = L_s\vec{i}_s + L_m\vec{i}_r = L_m\vec{i}_{ms} \tag{3}$$

In equation (3), $\boldsymbol{i_{ms}}$ indicates the equivalent field current vector, and the rotor flux can be expressed by

$$\vec{\varphi}_r = \frac{L_m^{\,2}}{L_s}\vec{i}_{ms} + \sigma L_r\vec{i}_r \tag{4}$$

where $\sigma = 1-[L_m^{\,2}/(L_rL_s)]$ is the leakage flux factor.

Substitute equations (3) and (4) into (1), the following equations are derived.

$$\begin{cases} \vec{v}_s = R_s\vec{i}_s + L_m p\vec{i}_{ms} + j\omega_s\vec{\varphi}_s \\ \vec{v}_r = R_r\vec{i}_r + \sigma L_r p\vec{i}_r + \dfrac{L_m^{\,2}}{L_s}p\vec{i}_{ms} + j\omega_{slip}\vec{\varphi}_r \end{cases} \tag{5}$$

By omitting the dynamic process of stator field currents, (5) can be updated as

$$\begin{cases} \vec{v}_s = R_s\vec{i}_s + j\omega_s\vec{\varphi}_s \\ \vec{v}_r = R_r\vec{i}_r + \sigma L_r p\vec{i}_r + j\omega_{slip}\vec{\varphi}_r \end{cases} \tag{6}$$

The mechanical performance of DFIG-WT is highly related to the electromagnetic torque T_e,

$$T_e = n_p(\varphi_{sd}i_{sq} - \varphi_{sq}i_{sd}) \tag{7}$$

Substitute (2) into (7), T_e can be calculated by using the stator and rotor *dq* currents.

$$T_e = n_pL_m(i_{rd}i_{sq} - i_{rq}i_{sd}) \tag{8}$$

The kinetic equation of DFIG is

$$T_m - T_e = Jp\omega_m \tag{9}$$

III. FSTP Topology-Based DFIG-WT

A. Configuration

As shown in Fig. 1, the stator of DFIG is connected to the grid directly, while the rotor is connected to the grid through a BTB power converter. The three phases on both the grid and rotor sides are assumed to be balanced. In this fault-tolerant topology, two DC-link capacitors C_1 and C_2 are employed in the DC-bus ($C_1 = C_2 = C_{DC}$). Between each phase of the grid (or rotor) and the midpoint, a triac (TR_a, TR_b, TR_c and TR_a', TR_b', TR_c') is placed to link the circuit when an open-circuit fault occurs in the corresponding bridge arm. In normal operation, six switches (IGBTs) are used at each side (S_1 to S_6 and S_1' to S_6'). When one of the switches breaks down, for example, S_5/S_6 in RSC or S_5'/S_6' in GSC, TR_A or TR_A' is triggered to isolate the faulty phase, leading to an FSTP RSC or GSC based DFIG-WT.

Considering the fault case above, only the four switches in bridge arms B and C (B' and C' for GSC) are controllable, and the switching states of them are defined as S_b and S_c (S_b' and S_c'), which can either be 0 or 1 to indicate the off or on state of the upper switch in the respective arm. The details of switching states in an FSTP converter are shown in TABLE I.

B. FSTP Converter Modeling

The rotor-side three-phase AC voltages can be expressed by the switching states S_b, S_c and the DC-link capacitor voltages V_{C1} and V_{C2} in an FSTP converter, which are

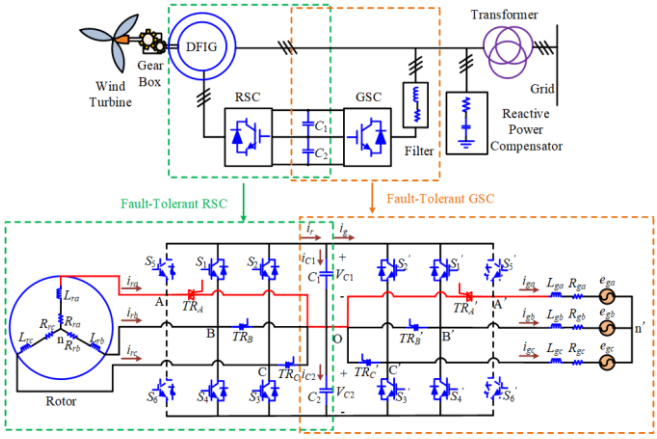

Fig. 1. Fault-tolerant RSC and GSC used in DFIG-WT by employing FSTP topology

TABLE I
Details of Switching States

S_b	S_c	Description	Vector
0	0	S_1 off & S_4 on; S_2 off & S_3 on	V_{00}
1	0	S_1 on & S_4 off; S_2 off & S_3 on	V_{10}
1	1	S_1 on & S_4 off; S_2 on & S_3 off	V_{11}
0	1	S_1 off & S_4 on; S_2 on & S_3 off	V_{01}

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TABLE II
THREE-PHASE AC VOLTAGES OF FSTP CONVERTER

Vector	v_A ($v_{A'}$)	v_B ($v_{B'}$)	v_C ($v_{C'}$)	v_α	v_β
V_{00}	$\frac{2V_{C2}}{3}$	$-\frac{V_{C2}}{3}$	$-\frac{V_{C2}}{3}$	$\frac{2V_{C2}}{3}$	0
V_{10}	$\frac{V_{C2}-V_{C1}}{3}$	$\frac{2V_{C1}+V_{C2}}{3}$	$-\frac{V_{C1}+2V_{C2}}{3}$	$\frac{V_{C2}-V_{C1}}{3}$	$\frac{\sqrt{3}(V_{C1}+V_{C2})}{3}$
V_{11}	$-\frac{2V_{C1}}{3}$	$\frac{V_{C1}}{3}$	$\frac{V_{C1}}{3}$	$-\frac{2V_{C1}}{3}$	0
V_{01}	$\frac{V_{C2}-V_{C1}}{3}$	$-\frac{V_{C1}+2V_{C2}}{3}$	$\frac{2V_{C1}+V_{C2}}{3}$	$\frac{V_{C2}-V_{C1}}{3}$	$\frac{\sqrt{3}(V_{C1}+V_{C2})}{3}$

expressed as shown below. The values of v_A', v_B' and v_C' are derived in a similar way.

$$\begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \frac{1}{3}\left(\begin{bmatrix} -1 \\ 2 \\ -1 \end{bmatrix} S_b V_{dc} + \begin{bmatrix} -1 \\ -1 \\ 2 \end{bmatrix} S_c V_{dc} + \begin{bmatrix} 2 \\ -1 \\ -1 \end{bmatrix} V_{C2} \right) \tag{10}$$

The instantaneous voltage values for the phase-to-ground voltages in the three phases are displayed in TABLE II for all the switching states, along with the values in the stationary $\alpha\beta$ coordinate system.

Considering the supersynchronous operation mode of DFIG-WT, the DC-link currents can be calculated from the following equations [34].

$$\begin{cases} i_{C1} = S_b i_{rb} + S_c i_{rc} - (S_a' i_{ga} + S_b' i_{gb} + S_c' i_{gc}) \\ i_{C2} = (S_b - 1) i_{rb} + (S_c - 1) i_{rc} - [(S_a' - 1) i_{ga} + (S_b' - 1) i_{gb} + (S_c' - 1) i_{gc}] \end{cases}$$
(RSC open circuit) (11)

$$\begin{cases} i_{C1} = S_a i_{ra} + S_b i_{rb} + S_c i_{rc} - (S_b' i_{gb} + S_c' i_{gc}) \\ i_{C2} = (S_a - 1) i_{ra} + (S_b - 1) i_{rb} + (S_c - 1) i_{rc} - [(S_b' - 1) i_{gb} + (S_c' - 1) i_{gc}] \end{cases}$$
(GSC open circuit) (12)

C. Open-Circuit Fault Detection

If one of the switches in a three-phase converter is with open-circuit fault, the current waveform for the respective phase will become highly distorted since the current cannot flow through this switch under certain switching states. For example, if switch S_6 is open circuited, i_{ra} can only flow through the freewheeling diode of S_5 during the positive half cycle, while the current flow of i_{ra} during the negative half cycle is not affected. The same principle is applicable for the other switches in either the RSC or GSC. The details for the influence on three-phase currents are illustrated in TABLE III.

The fault diagnosis schemes for three-phase power converters proposed in [35-38] can be used to detect the faulty switch, and the readers can refer to these papers for more details.

TABLE III
INFLUENCE OF SWITCH OPEN CIRCUIT ON THREE-PHASE AC CURRENTS (RSC IN FIG. 1 AS AN EXAMPLE)

Open-Circuit Switch	Affected Phase	Distorted Cycle
S_1	B	Negative
S_2	C	Negative
S_3	C	Positive
S_4	B	Positive
S_5	A	Negative
S_6	A	Positive

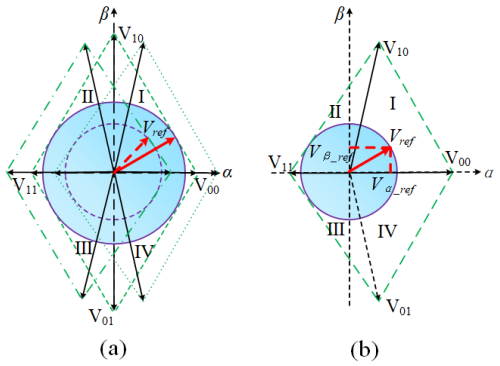

Fig. 2. Basic voltage vector distribution in an FSTP converter

IV. PROPOSED SIMPLIFIED SVPWM FOR FSTP CONVERTER

Only two bridge arms are controllable in an FSTP converter, and the number of switching states declines from 8 to 4. There are three situations for a three-phase converter to be reconfigured to a four-switch one, which includes the FSTP topologies with the bridge arm A, B or C isolated. In [39], the performances of FSTP converters under these three situations were proved to be identical. According to the calculation in an isosceles triangle, the magnitudes of V_{10} and V_{01} are $\sqrt{3}$ times that for V_{00} or V_{11}.

In this paper, the isolation of bridge arm A/A' is exemplified to illustrate the post-fault operation of DFIG-WT with FSTP RSC/GSC. The distribution of basic voltage vectors for an FSTP converter is presented in Fig. 2(a), with three different cases in the DC-link capacitor voltages considered. In this figure, it can be seen that when V_{C1} and V_{C2} have different values, the DC-bus voltage utilization rate becomes even lower, which is indicated by the dashed cycle inside. Therefore, the deviation between V_{C1} and V_{C2} needs to be suppressed for better performance of FSTP GSC/RSC.

An equivalent zero vector is created by distributing action time for the vector components with the opposite directions. For example, when the reference voltage vector V_{ref} is located in Sector I, which is shown in Fig. 2(b), the equivalent voltage vector is synthesized by allocating some action time in a switching period for the vector $\mathbf{V_{11}}$ (or $\mathbf{V_{01}}$) to compensate part of the action time in $\mathbf{V_{00}}$ (or $\mathbf{V_{10}}$). According to [40], when employing the two vectors with smaller amplitudes for obtaining equivalent zero voltage vectors, minimized current ripples can be achieved. In this case, $\mathbf{V_{00}}$, $\mathbf{V_{10}}$ and $\mathbf{V_{11}}$ are utilized. The following relationships can be derived [17].

$$\begin{cases} V_{C2} d_{00} - V_{C1} d_{11} + (V_{C2} - V_{C1}) d_{10} = 3 V_{\alpha ref} \\ (V_{C1} + V_{C2}) d_{10} = \sqrt{3} V_{\beta ref} \end{cases} \tag{13}$$

$$d_{00} + d_{10} + d_{11} = 1 \tag{14}$$

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where d_{00}, d_{10} and d_{11} are the duty ratios used in a switching period for the switching states $\mathbf{V_{00}}$, $\mathbf{V_{10}}$ and $\mathbf{V_{11}}$, respectively. By solving the equations (13) and (14), the values of d_{00}, d_{10} and d_{11} can be derived as

$$\begin{cases} d_{00} = \dfrac{V_{C1} + v_{Aref} - v_{Bref}}{V_{dc}} \\ d_{10} = \dfrac{v_{Bref} - v_{Cref}}{V_{dc}} \\ d_{11} = \dfrac{V_{C2} + v_{Cref} - v_{Aref}}{V_{dc}} \end{cases} \tag{15}$$

Then the duty ratios for the two healthy bridge arms d_b and d_c are calculated separately as

$$\begin{cases} d_b = d_{10} + d_{11} = \dfrac{V_{C2} + v_{Bref} - v_{Aref}}{V_{dc}} \\ d_c = d_{11} = \dfrac{V_{C2} + v_{Cref} - v_{Aref}}{V_{dc}} \end{cases} \tag{16}$$

This procedure can be replicated for the other three sectors, and the duty cycles for the four switches occupy the unified expression, no matter where the reference voltage vector is located. Therefore, sector identification and complex trigonometric calculations are omitted, which simplifies the SVPWM technique for FSTP power converter.

V. Control of FSTP BTB Converter

In a DFIG-WT, the control of GSC aims to maintain a constant DC-bus voltage, which provides power supply to the rotor side, and high current quality and unity power factor are to be obtained. While the stator active and reactive power, rotor speed and torque are controlled by RSC.

For the control of an FSTP converter, the upper and lower DC-bus capacitor voltages should be measured separately according to the SVPWM technique mentioned in the previous section. The balance between upper and lower DC-bus capacitor voltages is important for obtaining a high utilization rate, which must be considered in the control strategy. The control block diagram for the post-fault DFIG-WT is illustrated in Fig. 3.

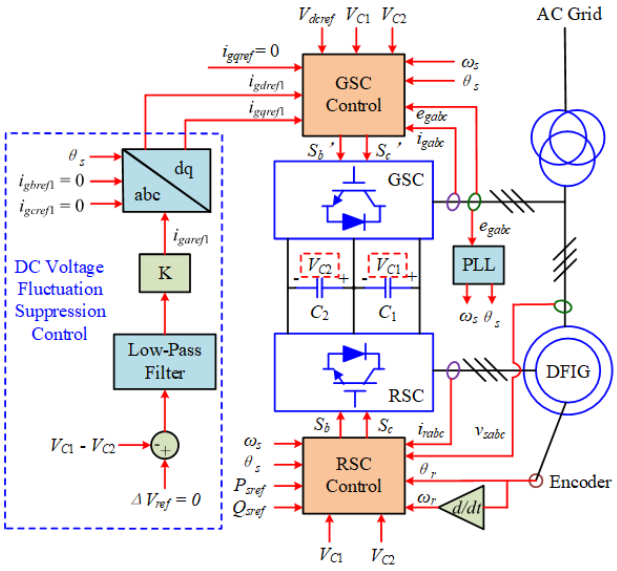

Fig. 3. Overall control strategy for FSTP BTB power converter based DFIG-WT

A. Influence of DC-Bus Capacitor Voltage Unbalance

Take the current flow direction in supersynchronous operation mode as the positive one. Then, according to Kirchhoff's current laws, the current in phase A is the difference between those in C_1 and C_2 when only the GSC or RSC is modified as an FSTP topology-based one, which can be expressed by the following equations.

$$i_{ga} = i_{C1} - i_{C2} \qquad \text{(GSC open circuit)} \tag{17}$$

$$i_{ra} = i_{C2} - i_{C1} \qquad \text{(RSC open circuit)} \tag{18}$$

The capacitor currents can be expressed by the derivatives of the capacitor voltages, which are

$$\begin{cases} i_{C1} = C_{DC} p V_{C1} \\ i_{C2} = C_{DC} p V_{C2} \end{cases} \tag{19}$$

Since V_{C1} and V_{C2} have low dynamics, the overall effect of capacitor voltage unbalance is revealed as a DC current offset, which is expressed as

$$\begin{cases} \bar{i}_{ga} = \dfrac{1}{C_{DC}} \int (i_{C1} - i_{C2}) dt \\ \bar{i}_{ra} = \dfrac{1}{C_{DC}} \int (i_{C2} - i_{C1}) dt \end{cases} \tag{20}$$

For the GSC open circuit case, the effects on the dq current components caused by current offset can be illustrated as

$$\begin{bmatrix} \bar{i}_{gd} \\ \bar{i}_{gq} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta_s & \cos(\theta_s - \frac{2}{3}\pi) & \cos(\theta_s + \frac{2}{3}\pi) \\ -\sin\theta_s & -\sin(\theta_s - \frac{2}{3}\pi) & -\sin(\theta_s + \frac{2}{3}\pi) \end{bmatrix} \begin{bmatrix} \bar{i}_{ga} \\ 0 \\ 0 \end{bmatrix} \tag{21}$$

$$= \begin{bmatrix} \dfrac{2\cos\theta_s}{3C_{DC}} \int (i_{C1} - i_{C2}) dt \\ \dfrac{2\sin\theta_s}{3C_{DC}} \int (i_{C1} - i_{C2}) dt \end{bmatrix}$$

Similarly, the rotor dq current offsets for the RSC open circuit case are derived as

$$\begin{bmatrix} \bar{i}_{rd} \\ \bar{i}_{rq} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta_{slip} & \cos(\theta_{slip} - \frac{2}{3}\pi) & \cos(\theta_{slip} + \frac{2}{3}\pi) \\ -\sin\theta_{slip} & -\sin(\theta_{slip} - \frac{2}{3}\pi) & -\sin(\theta_{slip} + \frac{2}{3}\pi) \end{bmatrix} \begin{bmatrix} \bar{i}_{ra} \\ 0 \\ 0 \end{bmatrix} \tag{22}$$

$$= \begin{bmatrix} \dfrac{2\cos\theta_{slip}}{3C_{DC}} \int (i_{C2} - i_{C1}) dt \\ \dfrac{2\sin\theta_{slip}}{3C_{DC}} \int (i_{C2} - i_{C1}) dt \end{bmatrix}$$

By substituting (22) into (8), the electromagnetic torque ripple component can be calculated as

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$$\bar{T}_e = \frac{2n_p L_m \int (i_{C2} - i_{C1})dt}{3C_{DC}} (i_{sq}\cos\theta_{slip} - i_{sd}\sin\theta_{slip}) \quad (23)$$

It can be seen that the torque ripple value is determined by the slip angle θ_{slip}, which is endowed with nonlinearity. For the capacitor voltage unbalance situation in the case of FSTP GSC, the offset component in phase A grid current leads to more distortions in the output currents, deteriorating the quality of power generation.

B. DC-Bus Voltage Unbalance Suppression Control

In order to achieve high output current quality and good torque performance, the DC-bus voltage unbalance has to be eliminated. According to the calculations in Section *A*, the corresponding *dq* offset current components need to be deducted. The transfer function of the voltage difference to the faulty phase offset current is expressed as

$$G(s) = \frac{\Delta V(s)}{\bar{i}_a(s)} = K_p G_{LPF}(s) G_{dc}(s) \quad (24)$$

Where K_p is the proportional gain of DC-bus voltage unbalance suppression control, G_{LPF}(s) is the transfer function of low-pass filter, and G_{dc}(s) is the transfer function of the DC-bus voltage to the phase A offset current.

The offset current components are derived as the integral term of the faulty phase current. In the proposed control strategy, the offset current component produced in phase A is fed back to the inner current control loop to be deducted.

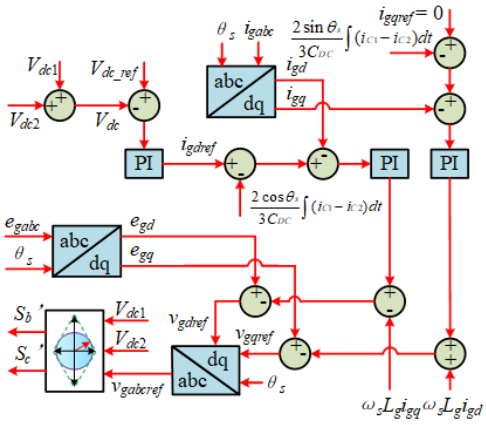

Fig. 4. FSTP GSC control block diagram

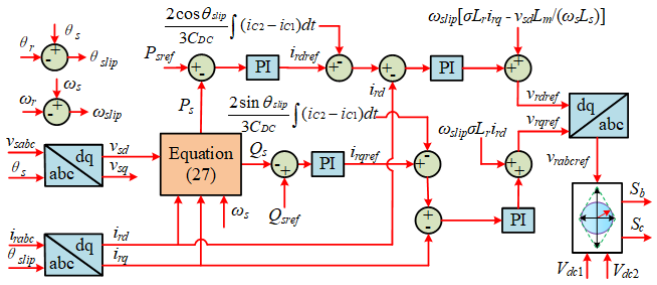

Fig. 5. FSTP RSC control block diagram

C. GSC Controller Design

A DC-bus voltage controller is designed to keep the DC-bus voltage at approximately the reference value, and it is the precondition of effective regulation of active power *P*. In the design of voltage controller, the steady-state error in the DC-bus voltage caused by parasitic elements and circuit inaccuracies is to be compensated by feeding back the real value V_{dc} [21]. Since GVO is applied, the *d*-axis grid current reference value i_{gdref} is derived by regulating the DC-bus voltage.

$$i_{gdref} = k_{vp}(V_{dcref} - V_{dc}) + k_{vi}\int(V_{dcref} - V_{dc})dt \quad (25)$$

Based on GVO, the three-phase AC voltages on GSC can be expressed as

$$\vec{v}_g = \vec{e}_g - R_g\vec{i}_g - L_g p\vec{i}_g - j\omega_s L_g \vec{i}_g \quad (26)$$

According to (26), the coupling terms $\omega_s L_g i_{gq}$ and $-\omega_s L_g i_{gq}$ are to be subtracted from the *d* and *q* axis components in the current control process, respectively.

When designing the grid-side current controllers, the *dq* current offset components should be deducted from the reference values. The FSTP GSC control block diagram is displayed in Fig. 4.

D. RSC Controller Design

The purposes of RSC current controllers are regulating the stator active and reactive power (P_s and Q_s), so it is necessary to derive the relationships among P_s, Q_s, i_{rd} and i_{rq}. By neglecting R_s, the expressions of P_s and Q_s can be derived as

$$\begin{cases} P_s = \dfrac{3}{2} k_s v_{sd} i_{rd} \\ Q_s = -\dfrac{3v_{sd}}{2}\left(\dfrac{v_{sd}}{\omega_s L_s} + k_s i_{rq}\right) \end{cases} \quad (27)$$

where $k_s = (L_m/L_s)$ is the stator coupling factor.

From (27), it can be seen that the control of P_s and Q_s is realized by the control of i_{rd} and i_{rq}, respectively.

As GVO is applied, and the stator resistance is small enough to be neglected, the stator *dq* flux components can be approximated as

$$\begin{cases} \varphi_{sd} \approx 0 \\ \varphi_{sq} \approx -\dfrac{|\vec{v}_s|}{\omega_s} \end{cases} \quad (28)$$

The rotor fluxes can be expressed by

$$\begin{cases} \varphi_{rd} = \sigma L_r i_{rd} \\ \varphi_{rq} = -k_s\dfrac{|\vec{v}_s|}{\omega_s} + \sigma L_r i_{rq} \end{cases} \quad (29)$$

Substitute (28) and (29) into (6), the rotor voltages can be expressed by

$$\vec{v}_r = (R_r + \sigma p L_r)\vec{i}_r + j\omega_{slip}(k_s\vec{\varphi}_s + \sigma L_r \vec{i}_r) \quad (30)$$

Similarly, with the *dq* rotor current offset deducted, the block diagram for FSTP RSC control is displayed in Fig. 5.

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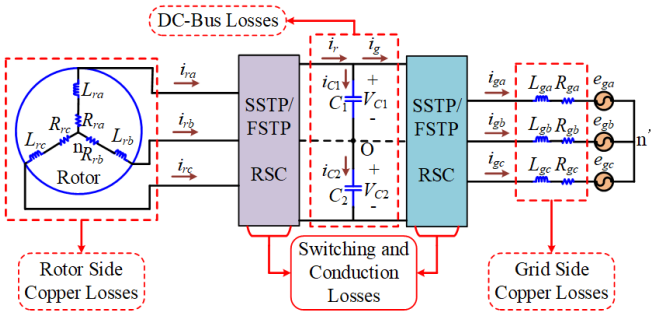

Fig. 6. Power loss model of BTB converter

VI. BTB Converter Efficiency Study

In order to further investigate the performance of DFIG-WT when FSTP BTB converter topologies are applied, the efficiency study of BTB converter is carried out. The efficiency of BTB converter is calculated as P_{gc}/P_r in the supersynchronous case or P_r/P_{gc} in the subsynchronous case. The power losses during the operation process can be divided into the copper losses, switching losses, conduction losses, and DC-bus losses. Take the case of supersynchronous operation as an example, the power loss model of BTB power converter is illustrated in Fig. 6.

TABLE IV
PARAMETERS OF DFIG-WT

Parameter	Value	Unit
Rated Power S_g	1.5	MVA
Rated Frequency F_{nom}	50	Hz
Rated Stator Voltage	575	V
Stator Resistance R_s	0.023	pu
Rotor Resistance R_r	0.016	pu
Stator Leakage Inductance L_{ls}	0.18	pu
Rotor Leakage Inductance L_{lr}	0.16	pu
Magnetizing Inductance L_m	2.9	pu
Friction Factor F	0.01	pu
Inertia Constant H	0.685	s
Pairs of Poles p	3	\
DC-Bus Capacitance C_{DC}	10000	μF
Rated Wind Speed v_w	11	m/s

The copper losses are calculated as

$$P_{cl} = \frac{3}{2}(R_r I_r^2 + R_g I_g^2) \tag{31}$$

TABLE V
CONTROLLER GAINS

	Proportional Gain	Integral Gain
DC-Bus Voltage Controller	0.5	15
GSC Current Controller	130	1500
RSC Current Controller	19.23	1

According to [41], assuming the duty cycles are related to time in a sinusoidal way, the conduction losses in an active power device and its freewheeling diode during a switching period are expressed as

$$\begin{cases} P_{cond,T} = V_{CE0} i_{CE}\left(\frac{1}{2} + \frac{m\cos\phi}{8}\right) + r_{CE} i_{CE}^2\left(\frac{1}{8} + \frac{m\cos\phi}{3\pi}\right) \\ P_{cond,D} = V_{F0} i_F\left(\frac{1}{2} + \frac{m\cos\phi}{8}\right) + r_F i_F^2\left(\frac{1}{8} - \frac{m\cos\phi}{3\pi}\right) \end{cases} \tag{32}$$

The switching losses during the switching and reverse recovery periods of a power switch are described by the following equations [41].

$$\begin{cases} P_{sw,T} = \dfrac{\sqrt{2} I_m E_{sw}}{\pi T_{sw} I_{mref}} \left(\dfrac{V_{dc}}{V_{dcref}}\right)^{K_{v,T}} \times [1 + T_{sw,I}(T_j - T_{ref})] \\ P_{sw,rr} = \dfrac{\sqrt{2} E_{rr}}{\pi T_{sw}} \left(\dfrac{I_m}{\sqrt{2} I_{mref}}\right)^{K_{i,d}} \left(\dfrac{V_{dc}}{V_{dcref}}\right)^{K_{v,d}} \times [1 + T_{rr,d}(T_j - T_{ref})] \end{cases} \tag{33}$$

The reference values are selected from the IGBT datasheet.

The DC-bus losses are modelled by the power losses in the two DC-link capacitors, which are mainly caused by the existence of equivalent series resistance (ESR) R_{esr} and leakage resistance R_l. When there is no current offset caused by DC-bus midpoint connection, $i_{C1} = i_{C2}$. However, after FSTP topology is applied, DC current components are induced in the capacitors. The DC-bus losses can be

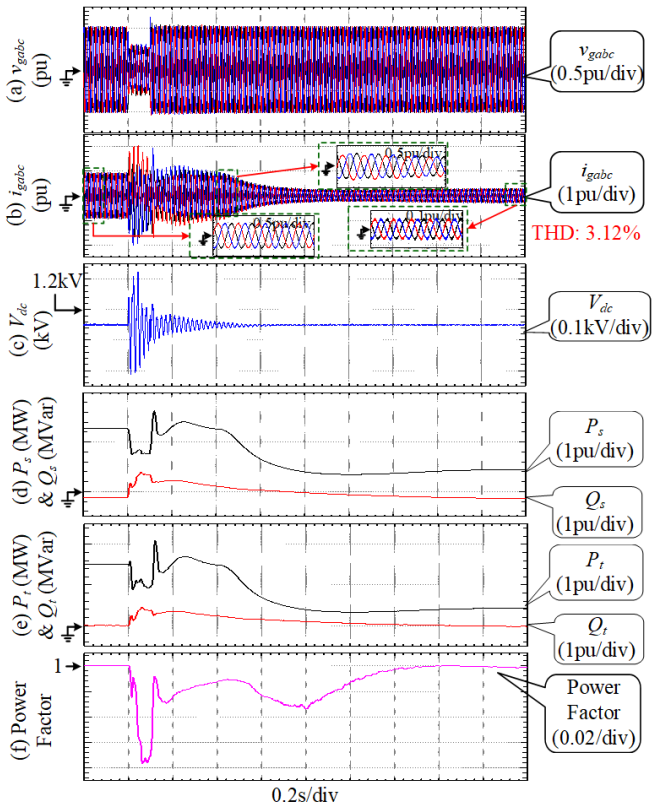

Fig. 7. Simulation results for the performance of SSTP GSC in DFIG-WT (a) three-phase grid voltages v_{gabc}; (b) three-phase grid currents i_{gabc}; (c) DC-bus voltage V_{dc}; (d) stator active and reactive power P_s & Q_s; (e) total output active and reactive power P_t & Q_t; (f) output power factor

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calculated by

$$P_{DC} = (R_{esr} + R_l)(\bar{i}_{C1}^{\,2} + \bar{i}_{C2}^{\,2}) \quad (34)$$

Taking the copper losses, DC-bus losses, switching and conduction losses into consideration, the whole power loss model of BTB converter can be expressed as

$$P_{loss} = P_{cl} + P_{DC} + \frac{n_s T_s}{T_{sw}}(P_{sw,T} + P_{sw,rr} + P_{cond,T} + P_{cond,D}) \quad (35)$$

When applying FSTP converter topology to ride through bridge arm open circuit fault, the number of switches n_s decreases, while the power consumption on the DC link increases. A case study is carried out in the following section.

VII. Simulation Results

To verify the reliability of the proposed control strategies of FSTP GSC and RSC in DFIG-WT, simulation studies are conducted in Matlab/Simulink2017a. A 1.5MW DFIG-WT is chosen, and the system parameters are illustrated in TABLE IV. The voltage and current controller gains are listed in TABLE V, along with the DC-bus voltage deviation suppression gains for the cases with FSTP GSC and RSC.

In the simulation process, an instantaneous grid voltage drop from 100% to 50% of the rated value at 0.1s that remains for 0.1s is adopted. In addition, the wind speed drops from 15m/s to 8m/s at 0.6s. The supersynchronous operational mode of DFIG-WT is chosen and the rated slip value is (-0.2). The sampling time is 5μs. The simulation results for the SSTP BTB, FSTP GSC and FSTP RSC based DFIG-WTs are displayed in Figs. 7 – 9, respectively.

After FSTP GSC is applied, the voltage controller's performance is still good enough to provide almost constant voltage supply for the RSC, as shown in Fig. 8. Besides, the DC-bus voltage fluctuation can be mitigated by either decreasing the power rating or increasing the maginitude of DC-bus voltage. Apart from the fluctuations caused by the grid voltage sag, the DC-bus voltage remains at a constant value for all cases. It can be seen that the total harmonic

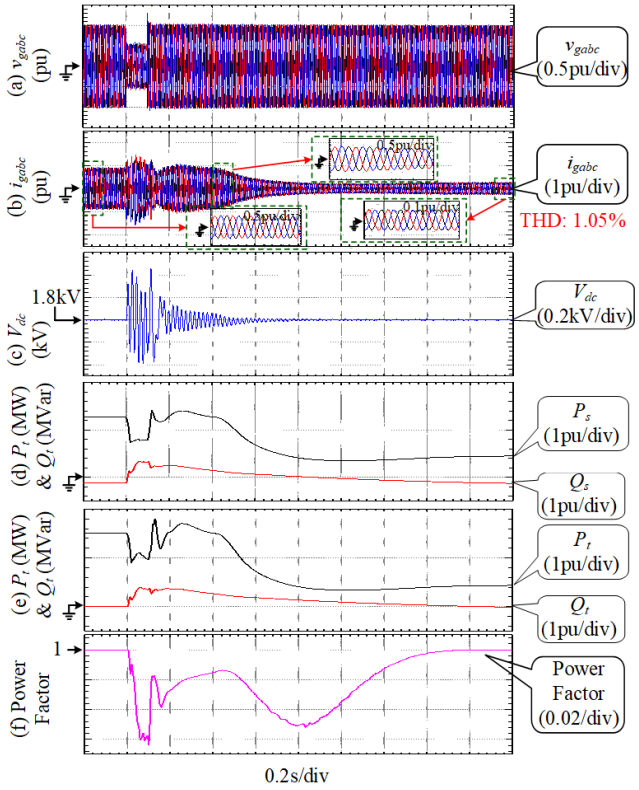

Fig. 8. Simulation results for the performance of FSTP GSC in DFIG-WT (a) three-phase grid voltages v_{gabc}; (b) three-phase grid currents i_{gabc}; (c) DC-bus voltage V_{dc}; (d) stator active and reactive power P_s & Q_s; (e) total output active and reactive power P_t & Q_t; (f) output power factor

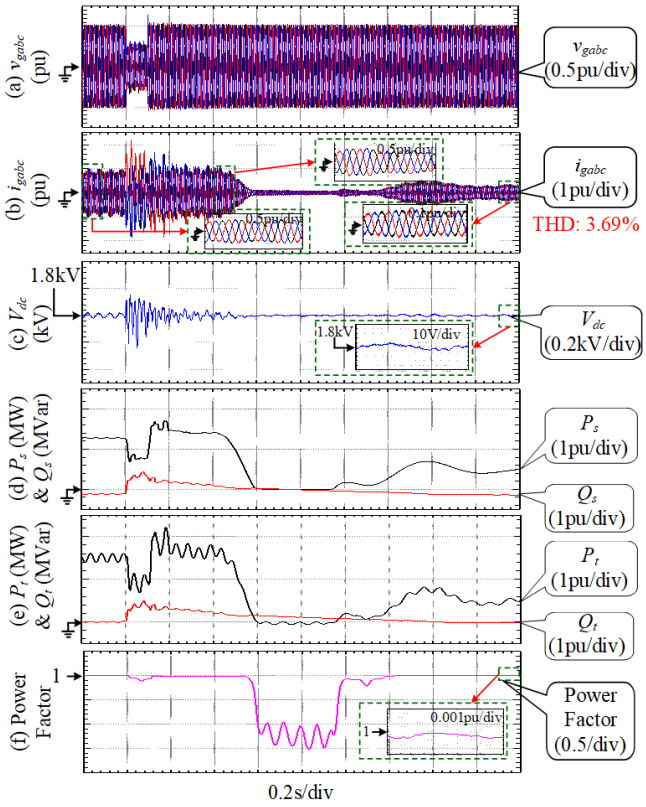

Fig. 9. Simulation results for the performance of FSTP RSC in DFIG-WT (a) three-phase grid voltages v_{gabc}; (b) three-phase grid currents i_{gabc}; (c) DC-bus voltage V_{dc}; (d) stator active and reactive power P_s & Q_s; (e) total output active and reactive power P_t & Q_t; (f) output power factor

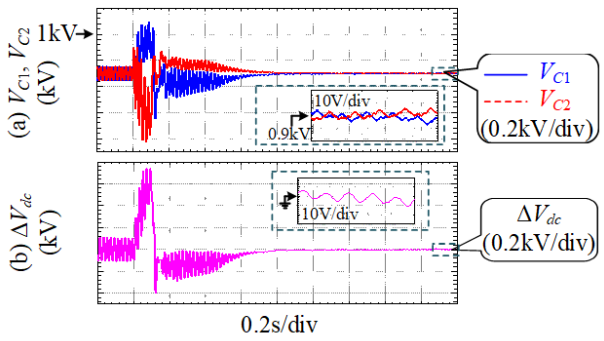

Fig. 10. DC-link capacitor voltage difference suppression

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distortion (THD) for SSTP GSC and that for FSTP GSC are 3.12% and 1.05%, respectively. For the FSTP RSC based DFIG-WT, some oscillations occur in the stator and total output power, resulting in some fluctuations in the DC-bus voltage (within ±10V) and three-phase grid currents. Although a higher THD of 3.69% is presented in the three-phase grid currents, the steady system operation is still obtained after the low voltage period and wind speed drop. On top of that, almost sinusoidal grid current waveforms are derived for all the three cases. In terms of the power factor, the performance of FSTP GSC is almost identical to that of the SSTP one. Moreover, a unity power factor can be ultimately achieved as time goes by in all the three scenarios. The DC-link capacitor voltage balancing is obtained by the proposed voltage suppression control strategy, as shown in Fig. 10(a). Furthermore, the difference between the upper and lower capacitor voltages is limited within a relatively small range (within ±10V around 0V after the grid voltage sag and wind speed step change), which is displayed in Fig. 10(b).

From the analysis above, the validity of FSTP GSC in DFIG-WT by employing the proposed control strategy is demonstrated, where a nearly constant DC-bus voltage, sinusoidal grid current waveforms and unity power factor can be derived after the converter reconfiguration is made. For RSC, its main function is regulating the stator active and reactive power, but its ability in balancing the DC-bus voltage deviation is limited. The FSTP RSC based DFIG-WT can still operate normally after the fault, and its performance can be improved by increasing the DC-bus capacitance.

In order to investigate the mechanical characteristics of the three types of DFIG-WTs, the plots of mechanical torque and rotor speed are displayed in Fig. 11. For the SSTP BTB and FSTP GSC cases, T_m and ω_m reach new steady values at around 0.6s after the wind speed step change. However, the fluctuations in the mechanical torque for the FSTP RSC case are apparent during the transition period. Ultimately, the steady operating state can be achieved.

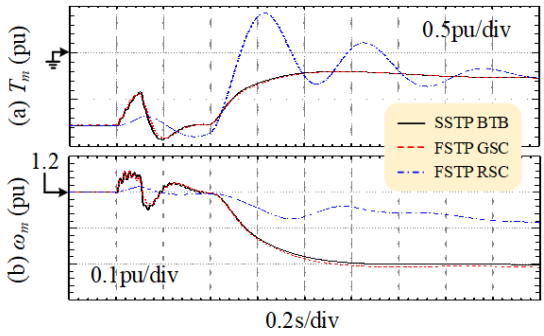

Fig. 11. Mechanical characteristics of DFIG-WT in different operation scenarios (a) mechanical torque T_m; (b) rotor speed ω_m

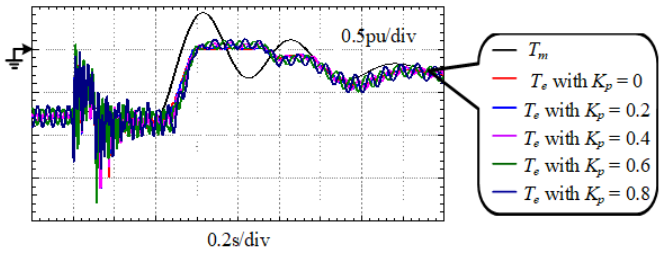

Fig. 12. Torque performances of FSTP RSC based DFIG-WT with different DC-bus voltage deviation suppression control proportional gains

The torque performance of FSTP RSC based DFIG-WT is also investigated from the aspect of changing the value of DC-bus voltage deviation suppression control proportional gain K_p. When applying different proportional gains for the DC-bus voltage difference suppression control, the respective torque performances are displayed in Fig. 12. It can be seen that the oscillation in T_e decreases with the decrease in K_p, while the tracking performance is deteriorated. Therefore, there is a tradeoff between the tracking accuracy and precision for different values of K_p.

Additionally, the power efficiencies of BTB converter by using SSTP topology, FSTP GSC, and FSTP RSC are investigated separately for the supersynchronous operation situation with the slip value of (-0.2), and the wind speed is maintained at 15m/s. The switching frequencies for both the GSC and RSC are equal to 2kHz. The average values of power efficiency η are displayed in TABLE VI for the three aforementioned cases, in which the effects of different proportional gains for the DC-bus deviation suppression control on η are investigated for FSTP GSC and RSC.

It can be seen from TABLE VI that when the commonly used SSTP BTB is applied for DFIG-WT, the power converter efficiency is 88.99%. In the fault scenario with FSTP GSC, η is maintained at around 91.8%. On the other hand, when applying FSTP RSC, the efficiency varies from 84.73% to 85.38% for the K_p values of 0, 0.2, 0.4, 0.6 and 0.8. Generally, the efficiency of FSTP GSC based topology is higher than that of the normal SSTP BTB, while the FSTP RSC based topology has a lower efficiency than that of SSTP BTB. Therefore, the proposed DC-bus voltage deviation suppression control method works better for FSTP GSC than FSTP RSC.

VIII. CHIL Setup and Results

To validate the proposed control algorithm in almost actual circumstances, the state-of-the-art real-time simulation

TABLE VI
EFFICIENCY TEST RESULTS

Normal Case: SSTP BTB			η = 88.99%		
Fault Scenario	K_p	η (%)	Fault Scenario	K_p	η (%)
FSTP GSC	0	91.79	FSTP RSC	0	85.38
	0.08	91.79		0.2	85.23
	0.16	91.79		0.4	85.18
	0.24	91.79		0.6	85.29
	0.32	91.80		0.8	84.73

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with CHIL setup is employed at NTUA laboratory. A network that allows connections to a real hardware controller is built up, and DRTS is applied for simulating the power converter circuit in real time with a time step of around 2μs [42]. In the CHIL setup, the proposed control algorithm is validated under real conditions, where time delays and noises are presented [42]. The experimental platform setup is illustrated in Fig. 13, and the power circuits of FSTP GSC and RSC are implemented independently in CHIL test. The FSTP GSC circuit is set up by using two DC-link capacitors at the DC side. On the other hand, the FSTP RSC circuit is established with two DC voltage sources, and the rotor voltages are simulated as a three-phase voltage source. The proposed control strategies are implemented in Matlab/Simulink and uploaded to a hardware controller that is interfaced with DRTS.

The values to be used as the inputs of the controller are the three-phase grid voltages v_{gabc}, three-phase grid currents i_{gabc}, three-phase rotor currents i_{rabc}, synchronous angular frequency ω_s, rotor electrical angular speed ω_r, and the DC-link capacitor voltages V_{C1} and V_{C2}. After the implementation of control strategies in the controller, the control signals are generated and fed back into DRTS. For the simulated power converter circuits in DRTS software, similar parameters are used as those in the previous section.

The experimental results for the operation of FSTP GSC are illustrated in Fig. 14. Since the GSC is directly connected to the grid and no distortions are injected, the three-phase grid voltages are in perfect sinusoidal waveforms as displayed in Fig. 14(a). The three-phase grid current waveforms are shown in Fig. 14(b), and current unbalance and phase shifts can be observed, which are caused by the modelling of a phase connected to the common point in DRTS. In Fig. 14(c), a step change of DC-bus voltage from 1.4kV to 1.6kV is presented, demonstrating the performance of the control loop in GSC for the actual DC-bus voltage value to track the change in the reference value within 2 seconds. Besides, the controller performance in balancing the upper and lower DC-link capacitor voltages is validated in Fig. 14(d), and the maximum difference between these two voltages is around 20V, which is about 1.25% of the DC-bus voltage value. Therefore, the influence of DC-link capacitor voltage unbalance on DC-bus voltage utilization rate can nearly be neglected, which fully demonstrates the validity of the proposed control algorithm in FSTP GSC.

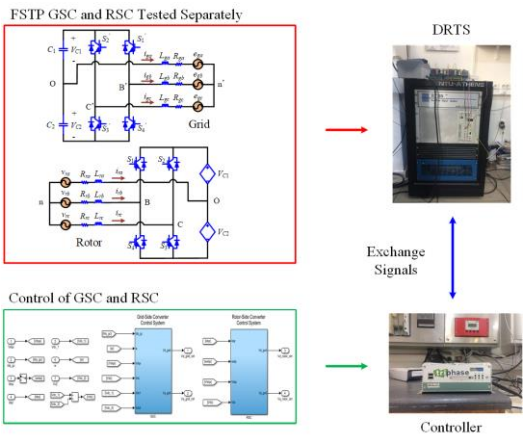

Fig. 13. Experimental platform setup

When an open-circuit fault occurs in one of the bridge arms in RSC, the performance of the PI current controllers in the rotor-side control system is investigated.

In CHIL setup for FSTP RSC, the DC-link capacitor voltages are supplied by two DC voltage sources to omit the use of GSC. A step change in the *d*-axis rotor current reference value i_{rdref} from 0.8A to 0.3A is presented in Fig. 15. It is observed from Fig. 15(a) that the actual d-axis rotor current i_{rd} tracks the reference value within a short time period and the rotor active power P_r also changes instantly as illustrated in Fig. 15(c), and it drops from 0.6kW to 0.2kW at the time of change in i_{rd}.

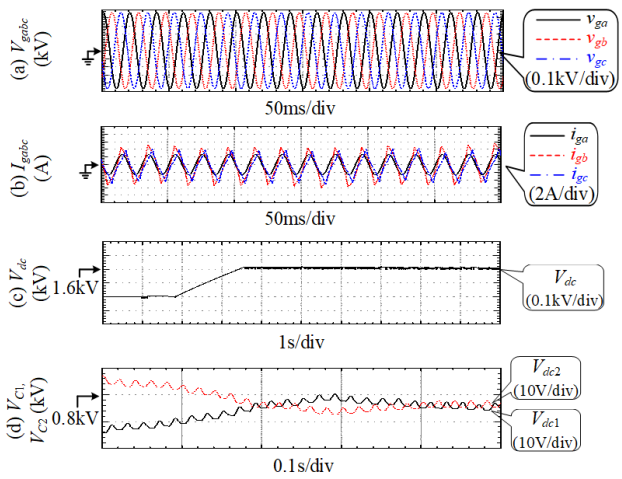

Fig. 14. Experimental results for FSTP GSC (a) three-phase grid voltages V_{gabc} (kV); (b) three-phase grid currents I_{gabc} (kA); (c) DC-bus voltage V_{dc} (kV) from 1.4kV to 1.6kV; (d) DC-link capacitor voltages V_{C1}, V_{C2} (V)

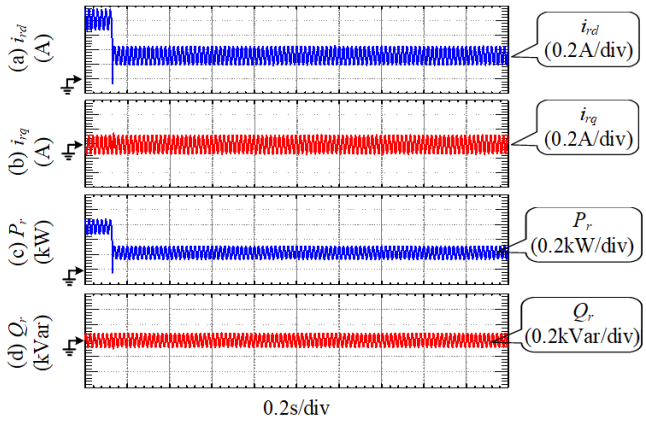

Fig. 15. Experimental results for (a) i_{rd} (A), (b) i_{rq} (A), (c) P_r (kW) and (d) Q_r (kVar) with the step change of i_{rd_ref} from 0.8A to 0.3A

IX. Comparison Between Experimental and Simulation Results

Compared with the results derived in Matlab simulations, there are unbalance and phase shifts in the three-phase grid currents in the experiment because of the modelling of phase connection to the common point in DRTS. In addition, the DC-bus voltage value is slightly reduced to mitigate the voltage stress on DC-link capacitors. Meanwhile, the voltage balance is achieved, with a difference of about 20V between the upper and lower capacitor voltages, while the corresponding value is 10V in the simulation results. Moreover, the tracking performance of rotor active power is verified in CHIL results, instead of stator active power in the simulation study, as the performances of FSTP GSC and RSC are individually verified. Furthermore, good tracking performances of V_{dc}, i_{rd} and P_r are validated in CHIL setup. However, fluctuations in the rotor currents are more significant than those in the simulation study.

X. Conclusion

In this paper, a highly reliable BTB power converter for DFIG-WT is proposed without employing redundant power switches for post-fault operation with an open-circuited bridge arm. A simplified SVPWM technique is utilized in this work by calculating the unified duty ratios for the remaining four switches, where the elimination of sector identification and complex trigonometric calculations is achieved. Besides, a DC-bus voltage deviation suppression control method is proposed, and the effects of changing the proportional gain on the torque performance are studied. Moreover, the BTB converter power loss model is analysed in detail, with the efficiency study carried out in different operating scenarios. According to the theoretical deduction, simulation study and experimental verifications, the key features of the proposed FSTP BTB converter in DFIG-WT can be summarized as

(1) Nearly sinusoidal three-phase grid current waveforms, constant DC-bus voltage, and unity output power factor are kept. (2) The difference between V_{C1} and V_{C2} is maintained within a small range. (3) A suitable proportional gain of DC-bus voltage deviation suppression control should be chosen for FSTP RSC to reach the trade-off between the torque tracking accuracy and precision. (4) A high power conversion efficiency is achieved for FSTP GSC based DFIG-WT with the proposed voltage deviation suppression control strategy. (5) Effective control of output power is demonstrated in Matlab/Simulink for all the three cases. (6) Excellent tracking performance for the DC-bus voltage, rotor active and reactive power are derived in CHIL setup.

With the proposed fault-tolerant BTB converter topology, a substantial number of unexpected WT strikes can be avoided, which is significant for improving the overall reliability of DFIG-WTs. Additionally, it is a promising strategy for minimizing the times of maintenance for offshore WTs to save cost and reduce risks during the maintenance process.

Acknowledgement

This work has been achieved using the ERIGrid Research Infrastructure and is part of a project that has received funding from the European Union's Horizon 2020 Research and Innovation Programme under the Grant Agreement No. 654113. The support of the European Research Infrastructure ERIGrid and its partner SmartRUE, ICCS-NTUA is very much appreciated.

This work is also supported by the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources under Grant LAPS17022.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIA.2019.2892925, IEEE Transactions on Industry Applications

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