High Voltage Step-up Multi-output DC/DC Converters for Power Conversion Systems

By

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Ph.D.

A thesis submitted in accordance with the requirements for the award of the degree of *Doctor of Philosophy* of the University of Liverpool

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I would like to dedicate this thesis to my loving girlfriend and my parents

Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text.

Song, Sen

2019

Acknowledgements

Abstract

With the increasing development of semiconductor components, solid-state DC/DC converters become popular in power conversion systems. Applications powered by sources with relatively low voltage level such as PV panels, and batteries require high voltage conversation ratios to meet the voltage level of load systems. Additionally, high voltage gain converters are also critical in grid-tied applications such as high voltage direct current (HVDC) transmission systems. Thus, the relatively low voltage level generated from offshore wind turbines or PV panels could be boosted up to the ultra-high line voltage level of HVDC transmission. Although conventional boost converters could achieve high voltage gain theoretically, their switches operate with an excessive duty cycle that degrades the reliability of converters. This thesis proposes the derivation, analysis, and verification of advanced high voltage step-up DC/DC converters that could obtain an improved performance compared with current state-of-the-art topologies.

Four novel DC/DC converters that have high step-up voltage ratios are proposed for applications as HVDC transmission systems, light emitting diode (LED) lightings, and electric vehicles respectively as following.

- The matrix configuration is proposed so that converters only suitable for low power applications could be scaled up to meet the requirements of HVDC transmission. Thanks to the matrix configuration, simultaneous ultra-high voltage step-up ratio as well as low voltage/current rating of components, and high reliability are obtained. Additionally, two topologies of submodules (SMs) are designed and installed in the matrix configuration to meet the specific requirements of HVDC transmission of offshore wind farms and large scale solar power plants. Moreover, owing to the design of SMs, the voltage step-up ratios of designed multi-module converters, G_{boost}, is increased to the number of SMs in series, N, times the voltage conversion ratio of SMs, G_{SM}, as $G_{boost}=N{\times}G_{SM}$. Compared with modular multilevel converters (MMCs), the proposed multi-module converters can achieve a higher voltage gain ratio since the output voltage of SMs implemented in MMCs equals to the input voltage.

- A stacked multi-output isolated DC/DC converter is proposed for the LED driver. The installation of transformers and switched capacitors enlarge the voltage gain.

Additionally, compared with two conventional isolated converters, the proposed one could use one less active switch to achieve similar performance, so that the cost is reduced. Moreover, all switches could achieve soft-switching operation. According to the experiment results, the proposed converter can maintain the high power efficiency 92%~94.6% with the output power range from 12 W to 200 W, which exceeds the similar topologies whose active switches are hard-switching.

- Furthermore, a three-switch-based single-input dual-output (SIDO) converter is presented in this thesis. Due to the integration of two switches, the proposed SIDO converter can use one less switch, and the operation performance is similar to that of applying two conventional two single-input single-output converters. Hence, the cost is reduced. Moreover, thanks to the independent power flow and two control variables, the cross regulation performance is improved, and simultaneous buck as well as boost output voltages are realised. According to the experiment results, the voltage error ratio caused by cross regulation problems is reduced to 1.55%, and the maximum power efficiency reaches 96.6%, which shows a better performance than current state-of-the-art SIDO converters.

This thesis has successfully demonstrated several novel topologies for DC/DC power conversion systems. The most challenging issues such as increasing voltage conversion ratios, scale up power converters applied in low power applications for high power applications, and improving power efficiency while keep the low cost at the same time have been overcome by applying the proposed techniques.

Key words: DC/DC converters, high voltage step-up ratio, soft-switching, low cost.

Contents

LIST OF FIGURES

LIST OF TABLES

Abbreviation

BMS: battery management system

CBC: current balancing circuit

CFPP: current-fed push-pull

DAB: dual-active-bridge

ES: energy storage

FB: full-bridge

HB: half-bridge

HVAC: high voltage alternating current

HVDC: high voltage direct current

IGBT: insulated-gate bipolar transistor

LED: light-emitting-diode

MMC: modular multilevel converter

MOSFET: metal-oxide-semiconductor field-effect transistor

PCB: printed circuit board

PI: proportional integral

PV: photovoltaic

RMS: root-mean-square

SCC: switched capacitor converter

SIDO: single-input dual-output

SIMO: single-input multi-output

SISO: single-input single-output

SM: submodule

ZCS: zero-current-switching

ZVS: zero-voltage-switching

Chapter 1.   BACKGROUND

During the last decades, power DC/DC converters have been attracted considerable interest in academia and industry due to the extensive improvement of power electronics. Currently, DC/DC converters play an essential part in the power conversion systems over the full range from low power applications like light-emitting-diode (LED) drivers to high power applications as high voltage direct current (HVDC) transmission systems. Although power DC/DC converters have been established and studied over a long time, there are still a lot of difficulties existing, and related work is yet developing in depth and width. This thesis concentrates on the DC/DC converter topology design to improve the performance, including voltage conversion ratio, power efficiency, reliability, and cost.

1.1   High Step-up DC/DC Converter Applications

1.1.1   HVDC Transmission

With the dramatical increment of the world's population and economy, the energy demand also experiences a remarkable growth. According to the British Petroleum Energy Outlook, the global energy consumption in 2035 is forecast to increase by 44% with comparison to that in 2016 [1]. According to the statistics, the commonly used non-renewable energy sources such as oil, natural gas and coal will be depleted in the next few decades to around a century based on the proven fossil energy reserves and the mining speed, where coal could last about 110 years as the final choice for people [2]. Therefore, it is imperative to utilise the renewable energies, and the offshore wind farms, as well as large-scale solar plants, are dominant solutions due to the advantages as environmentally friendly, free, and relatively constant [3, 4]. To utilise these renewable energy sources (RESs), generators such as wind turbines and PV panels first convert renewable energy to electric energy, and then, transmission systems are required to delivery generated electric power to urban areas. Compared with traditional high voltage alternating current (HVAC) transmission, the HVDC transmission is preferred for power transmission systems with large-scale, long-distance such as offshore wind farms and solar plants since both of them are located in the remote area from cities, i.e. the electric energy consumption centres.

As the quality of semiconductor components has been improved in recent years, HVDC transmission becomes popular and viable for bulk power transmission over a long distance due to economical and effective advantages [5, 6]. Fig 1.1 depicts the station cost trend of each transmission method with the increase of the transmission distances, and HVDC is an economical choice for the project when the transmission distance is over 40~60 km submarine cable and 500~800 km overhead line [7-9]. Additionally, the prices of HVAC and HVDC transmission systems for a 300 MW offshore wind farm are listed in Table 1.1 [10]. Due to the high cost of semiconductor components, the implementation cost of an HVDC substation is more expensive than that of an HVAC substation in the case of short transmission distance.
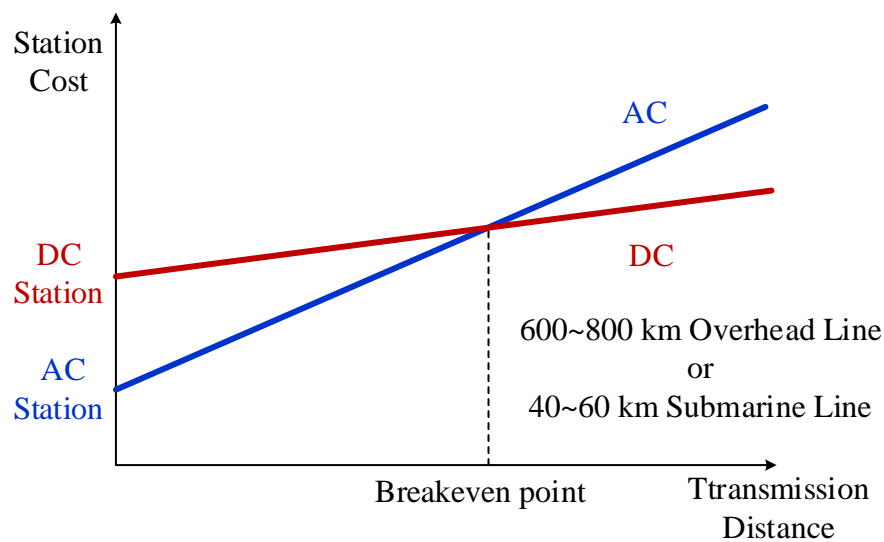
Figure 1.1 Distance versus cost for HVAC and HVDC cables [8-10].

Table 1.1 Prices of HVAC and HVDC systems for 300 MW offshore wind farm [7].

Item	HVAC	HVDC
Substation (M€)	10	45
Cable (k€/km)	1500	600
Cable installation (k€/km)	340	215
Offshore substation (M€)	13	24
Onshore land use (k€)	50	125

Besides the economical aspect, HVDC transmission also have the other advantages as following [11-15]:

- AC transmission line has series inductance and capacitance. Line power capability of a specific operation voltage is limited by steady-sated stability. Hence, the power capability is reduced with the increasing of line length. On

the contrary, DC transmission has no reactance and no stability problem so that no transmission distance limitation.

- AC tends to flow through the skin of line, which increases resistance and hence the power loss.

- Corona loss, noise, and radio interference are less in HVDC transmission systems.

- A DC circuit only requires two DC cables, which are fewer than that of conventional AC transmission systems, where at least three cables are contained. Therefore, the towers for DC transmission cables are narrower, simpler, and cheaper than those of AC cables.

To realise HVDC transmission systems, high voltage gain DC/DC converters play a vital role to convert a low voltage level from generators to the high line voltage level of HVDC transmission as illustrated in Fig. 1.2. For example, a DC/DC converter with high voltage step-up ratio as 400× is installed to convert the relatively low voltage level as 800 V generated from offshore wind turbines to the ultra-high voltage ±320 kV in DolWin offshore wind HVDC link [16].
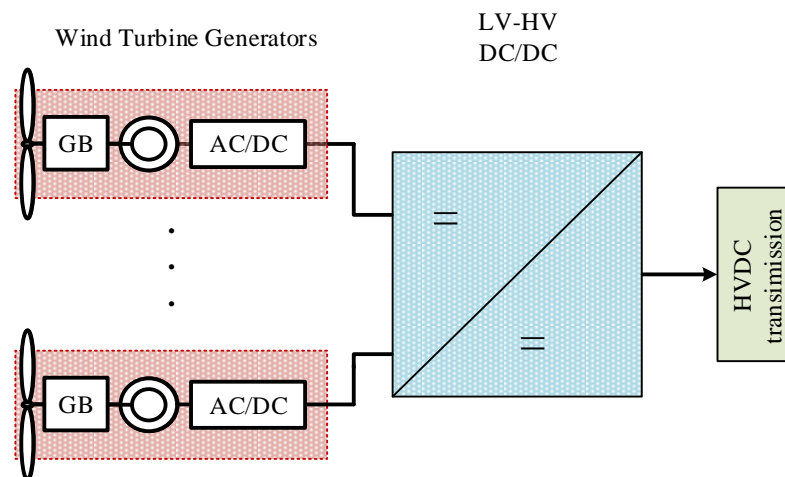
Figure 1.2 DC-based HVDC configurations for wind power transmission.

1.1.2 LED Driver

LED has enormous potential in replacing conventional lamps in residential, automotive, decorative and medical applications due to its advantages such as high power density, high luminous efficiency, long lifespan, mercury-free and quick response [17, 18]. For the high illuminance application scenarios, numerous LEDs are

placed. When LEDs are in series connection, the high output voltage level is required. For parallel-connected ones, regulating the current through different LED strings requires the current balancing technology because of the LEDs' current-voltage characteristic and the negative temperature coefficient [19]. For LED applications powered by 24 V batteries or PV panels, a boost voltage level around 300 V is required for 100 W LED strings. Therefore, converters with high voltage conversion ratio are critical for LED drivers.

1.1.3   EV

According to the group of MPs in the UK, Britain will ban all sales of new petrol and diesel cars by 2030 to tackle air pollution, posing a significant risk to public health [20]. Additionally, automotive companies such as BWM, Mercedes-Benz, Ford, and BYD have focused on electric vehicles (EV), hybrid electric vehicles (HEV), and fuel cells vehicles to meet vehicle market demand. However, the design of power DC/DC converters with high efficiency, low cost, and small volume is still a technical challenge. Fig 1.3 presents a typical fuel cell vehicle drive system. High step-up DC/DC converters are the necessary part to boost the low fuel cell voltage to power the electric motors. Normally, the low voltage level from the fuel cell is boosted up to 200~400 V, which is also compatible with the battery pack [21]. Then, the inverter is installed to drive the electric motor.
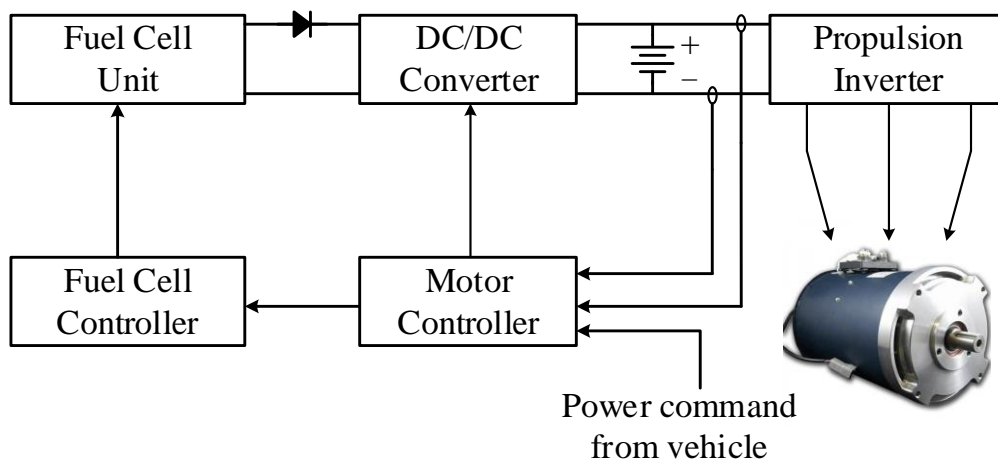
Figure 1.3 HEV drive train.

1.2   Operating Characteristics of High Voltage Step-up Converters

In this section, some desired advantages of high voltage step-up DC/DC converters are briefly introduced.

1.2.1   High Voltage Boost Ratio

High voltage step-up converters are installed in applications like HVDC transmission systems and power conversion systems powered by sources as single PV panel, fuel cells, super capacitors, and batteries. Compared with the output voltage level, the relatively low input voltage is required to be boosted up to 5~400 times.

1.2.2   High Power Efficiency

A high input current would be caused due to the low input voltage and high voltage step-up conversion ratios, which leads to a high conduction loss. For a specific topology, the components choice, transformer design, and printed circuit board (PCB) layout design could improve power efficiency by reducing conduction loss. Additionally, reducing the switching loss and conduction loss of active switches is also necessary to further increase the power efficiency. The soft-switching technology can minimize switching loss. Switches with low rated voltage have a low on-state resistance, which does the favour of reducing conduction loss.

1.2.3   Low Current/Voltage Ripple

The commutation within power converters will cause a fluctuation of output current and voltage, and a large current/voltage ripple is the detriment of power consumption devices. For example, the on/off state change of active switches would induce a triangular waveform of the filter inductor current. Then, the DC component flows through the load, and the AC part flows through the output capacitor, which produces an output voltage ripple.

1.2.4   Fast Response

For open loop controlled DC/DC converters, load variation or other external disturbances would cause output voltage errors. In closed loop controlled DC/DC converters, the duty cycle of switches is controlled according to the transient output voltages to maintain the normal operation and avoid output voltage error. A

compensation scheme such as PI compensation is required for closed loop control, and ensure the output voltage could be recovered to rated value quickly after interference has occurred to prevent devices from hazards.

1.3   Aims and Objectives

Theoretically, conventional boost converters can achieve high voltage step-up ratio when the power switch operates with extreme duty cycles, which will penalize the power efficiency, and the conversion ratio is limited due to the existing turn on/off time. Additionally, the switch in the conventional boost converter has high voltage stress. Then, high voltage rated components have a large on-state resistance, which results in a high conduction loss. One of the main converter design challenges is to obtain high boost ratios while avoiding extreme duty cycles operation condition. Besides that, improving performance, including high power efficiency, reliability, and low cost are also the motivations of this thesis.

The main objectives are as following:

- To propose matrix-configuration-based multi-module DC/DC converters applied in high power applications as HVDC transmission systems, which can achieve high voltage conversion ratios and low voltage and current ratings of components. The proposed converters should meet the requirements as high voltage conversion ratio, soft-switching, and high fault tolerance capability.

- To propose a novel LED driver that can delivery low voltage power from the battery or single PV panel to high illuminance LED applications with high efficiency. The cost of the energy conversion system should be low.

- To develop a single-input dual-output (SIDO) converter for EVs which can alleviate the cross regulation problems existing in all multi-output converters. The output voltage should be maintained even with the load variation of the other output ports. Additionally, the desired advantages as high voltage conversion ratio, high power efficiency and low cost are still required.

1.4   Thesis Outline

Based on the analysis of the current high voltage gain DC/DC converters, this thesis presents four novel high voltage gain DC/DC converters and the detailed analysis of their operation principles and the applications. The thesis is organized as follows.

In Chapter 2, the typical topologies of boost converters are discussed and analysed with the corresponding advantages and disadvantages. Additionally, relevant design considerations are presented.

Chapter 3 introduces an innovative multi-module converter applied in HVDC transmission for offshore wind farms. The design of the submodule (SM) and multi-module converter are shown. The current-fed push-pull (CFPP) SM could achieve soft-switching operation of all switches. With multiple modules connected in a scalable matrix configuration, the multi-module converter can achieve ultra-high voltage step-up ratio, high power level, and low voltage/current rating of components simultaneously.

Chapter 4 presents another multi-module converter with the three-port converter (TPC) as SMs. The TPC can integrate energy storage (ES) systems and HVDC systems to compensate for the generation fluctuations of RESs. The TPC SM and the multi-module converter are analysed in detail, and the design of the TPC and multi-module converter is verified by simulation results.

In Chapter 5, a stacked switched capacitor converter is designed as the LED driver for high illuminance (100 W) applications. Compared with using two switched capacitor converters, the proposed one uses one less switch to obtain similar performance. Additionally, the soft-switching operation of switches and the passive current balancing circuit (CBC) improve the power efficiency of the driver. Besides that, the passive CBC could auto-balance currents through different LED strings. Furthermore, a prototype is built to verify the operation and efficiency of the design.

Chapter 6 presents a novel SIDO converter consisting of three active switches that can alleviate the cross regulation problems of multi-output converters. Thanks to the independent power flow and two control variables, the cross-regulation performance is improved. Additionally, all switches can achieve soft-switching operation, which contributes to a significant switching loss reduction. Owing to the voltage multiplier

circuit, a high voltage boost conversion ratio is realised with relatively low voltage stress of switches. A prototype is built to verify the theoretical analysis and measure the power efficiency.

Chapter 7 draws the conclusion and future work.

Chapter 2.   HIGH VOLTAGE GAIN DC/DC CONVERTERS TECHNIQUES-A LITERATURE REVIEW

2.1   Introduction

In recent years, high voltage gain DC/DC converters have been extensively researched since the breakthrough of semiconductor in the 1950s [22]. The high voltage gain DC/DC converters are widely used in the power conversion systems for HVDC transmission and applications with relatively low input voltages. Although conventional boost converters can step up voltage level, there are some disadvantages such as extreme duty ratio and high voltage stress of switches. With the duty cycle approaching unity or zero, the power converter cannot maintain a constant output voltage with load variations and external disturbances.

This section introduces various techniques for extending voltage step-up conversion ratios. The transformer-based DC/DC converters can obtain high voltage conversion ratios by increasing the turns ratios of secondary over primary windings. However, a large turns ratio leads to significant leakage inductance, which will cause a high voltage spike on electronic components. Additionally, high rated switches with considerable on-state resistance are required due to large voltage spikes, resulting in high conduction loss. The other methods to boost output voltage are realised by using passive components such as capacitors and inductors. Energy is first transferred from input sources to the passive components, and the voltage of these passive components are increased. In the next operation stage, the passive components are series-connected to input sources and release their stored energy. Then, a boost output voltage is obtained, which equals to the sum of the voltage of passive components and the input voltage. Additionally, there are several methods to enlarge voltage gains by installing multiple converters. For example, the output port of the previous boost converter could be connected to the input port of the next following boost converter to enhance the voltage gain. Moreover, the parallel-input series-output structure could also further increase the voltage step-up conversion ratio.

In this chapter, several classification plans of converters are discussed based on their topologies, operation principles, and applications. Then, some typical DC/DC converters with high voltage conversion ratios are discussed. Additionally, a brief review of corresponding knowledge like control method, switching strategy, and failure mechanism of semiconductor components are presented.

2.2 Categories of Voltage Boost DC/DC Converters

As shown in Fig 2.1, converters could be catalogued according to the topologies, operation principles, performance, and applications. All converters could be classified into two types, including non-isolated converters and isolated converters based on whether they use transformers. Besides, according to their operation principles and performance, converters also could be catalogued as voltage-fed/current-fed converters and hard-switching/soft-switching converters. Furthermore, unidirectional and bidirectional converters are classified depending on whether there is bi-directional power flow through converters.
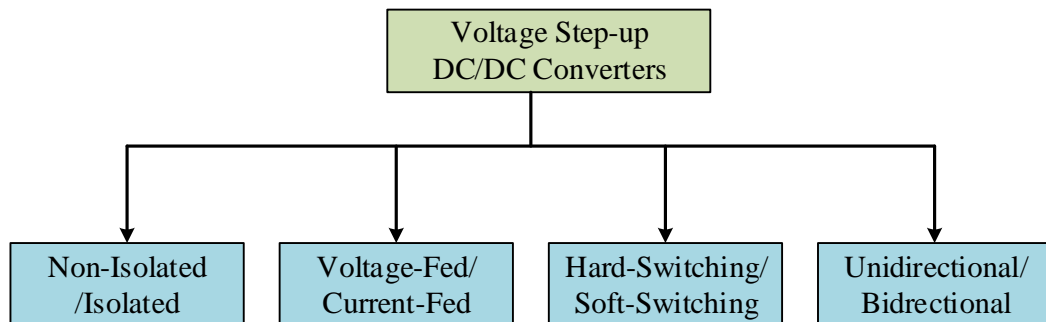
Figure 2.1 Categories of voltage boost DC/DC converters.

2.2.1 Isolated/Non-isolated Converters

Based on whether there is galvanic isolation provided by transformers, DC/DC converters can be catalogued into isolated and non-isolated converters whose schematics are shown in Fig 2.2. From the figures, the input power could be voltage-fed or current-fed. Additionally, output side loads could be devices or inverters in grid-tied systems. Active switches like metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) are installed in the switching converter modules with other passive components such as inductor, capacitors, and diodes.

Switching Converter

(a)

Switching Converter   Transformer   Rectifier

(b)
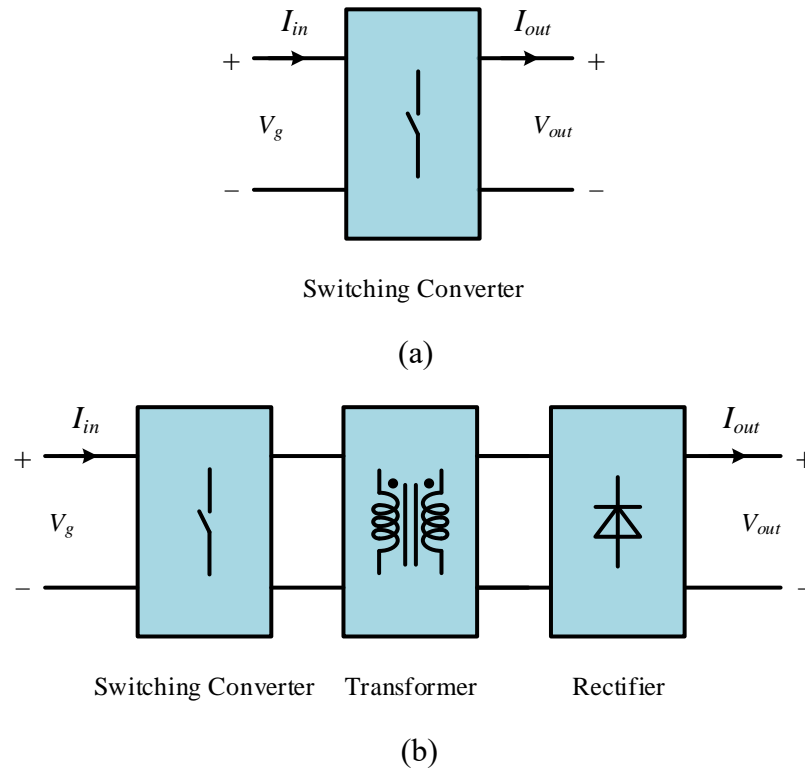
Figure 2.2 Schematic of non-isolated and isolated converters: (a) non-isolated; (b) isolated.

Isolated DC/DC converters with high efficiency transformers are a dominant technique for galvanic isolation and impedance matching between the input source and output load. Additionally, galvanic isolation is critical to avoid fatal safety hazards [23-25]. For isolated converters, the switching converter module firstly converts the DC input power into AC, and then the AC power is transferred from the primary side of the transformer to the secondary side by electromagnetic fields to realise isolation. Generally, the rectifier is required to convert AC to DC to supply power to load. Besides the voltage conversion ratio based on duty-cycles of active switches, the turns ratio of transformers can further boost the output voltage to a higher level [26, 27]. However, a significant turns ratio leads to large leakage inductance, which will cause a high voltage spike on electronic components. Moreover, the installation of transformers would lead to a large volume, weight, and increased power loss.

The non-isolated converters have advantages such as low cost, high efficiency, and high power density due to the simple design, straightforward control, and free of transformers [28-30]. The typical switching converter module adopts topologies as switched capacitors or switched inductors to achieve high output voltages [31-37].

Moreover, the volume and weight of passive components as inductors and capacitors are inversely proportional to the operation frequency. Hence, the size of non-isolated converters could be further decreased by increasing the operation frequency, where the typical operating frequency is from tens of kilohertz (kHz) to hundreds of kHz. However, non-isolated converters have a significant heat loss and low reliability in high power applications because of the magnetic saturation of inductors [38].

In summary, the isolated DC/DC converters are preferred for applications demanding galvanic isolation between the input source and output load due to safety reasons; the non-isolated converters are dominant in applications whose volume and weight are primary concerns.

2.2.2 Unidirectional/Bidirectional Converters

For unidirectional converters, the power is transferred from the input to the output. Bidirectional converters can transfer power in both directions, which are widely used in systems with batteries such as EVs, smartphones, and so on. Generally, bidirectional DC/DC converters are derived from typical unidirectional converters by installing extra active switches as shown in Fig 2.3. For example, in Fig 2.3(a), the bidirectional power converter is derived by using an external switch Q_2 to replace the diode D_o in the conventional boost converter. Similarly, the bidirectional Ćuk converter is realised as illustrated in Fig 2.3(b).

(a)

(b)
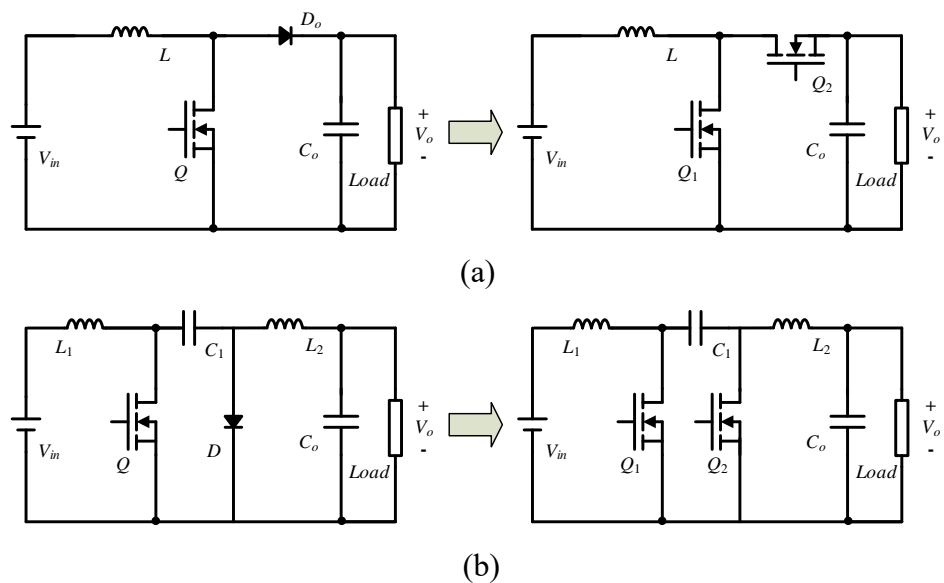
Figure 2.3 Derivation of bidirectional converters: (a) boost converter; (b) Ćuk converter.

2.3   Topology Review of Typical High Voltage Step-Up Converters

In this part, a brief review about the typical topologies of boost converters is presented. For non-isolated converters, switched capacitors, switched inductors and coupled inductors could enlarge the voltage boost ratios. Majority of isolated converters are achieved by combining transformers and non-isolated converters. Then, the turns ratios of transformers could provide high voltage conversion ratios.

2.3.1   Conventional Boost Converter

The conventional non-isolated boost converter is illustrated in Fig 2.4. The inductor is marked in red; capacitor is marked in blue; semiconductor components such as MOSEFTs and diodes are in purple. The voltage gain is calculated as the following equation:

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{2.1}$$
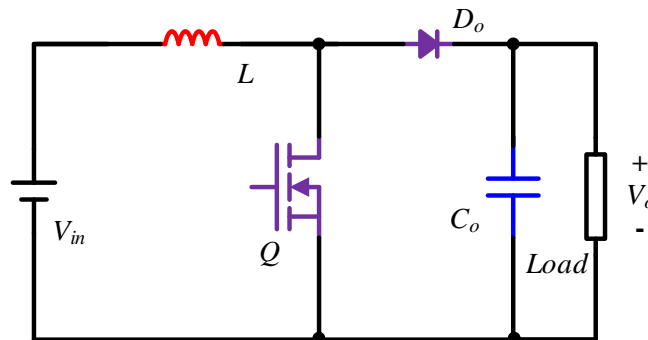
Figure 2.4 Topology of the conventional non-isolated converter.

The on/off state of switches is changed periodically, which is controlled by PWM signals. The switching frequency is defined as f_s, and the duty cycle D represents the ratio of the on-time t_{on} over the switching period t_{sw}. Based on the equation, the higher output voltage could be obtained by increasing the duty cycle D of the active switch Q. When the switch Q is on, the diode D_o is revers biased, and the input source charges the inductor L. When the switch is off, power is transferred from input source and the inductor to the output load. The output voltage is boosted since the inductor is represented as an equivalent voltage source due to the instantaneous voltage.

Conventional non-isolated boost converters are the simplest topology for voltage step-up conversion. Since the converter is controlled by PWM signals, a high voltage step-up conversion ratio can be obtained by an extreme duty cycle of the switch Q. Unfortunately, the turn-on and turn-off of semiconductor components take a certain time so that a large duty cycle degrades the reliability and dynamic operation [39]. For example, with the duty cycle approaching unity or zero, the power converter cannot maintain a constant output voltage with load variations and external disturbances. Moreover, output diodes would suffer a large current ripple due to the short off-time of the switch leading to the increased reverse recovery loss and electromagnetic interface (EMI) [40, 41]. Furthermore, the conduction loss and switching loss of the switch are large because of the high current ripples on the inductor and switch when the switch are turned off.

2.3.2 Cascaded Converters

As shown in Fig 2.5, due to the voltage gain limitation of traditional boost converters, multiple converters are in series connection as the cascade configuration to reach a higher output voltage [42-44].
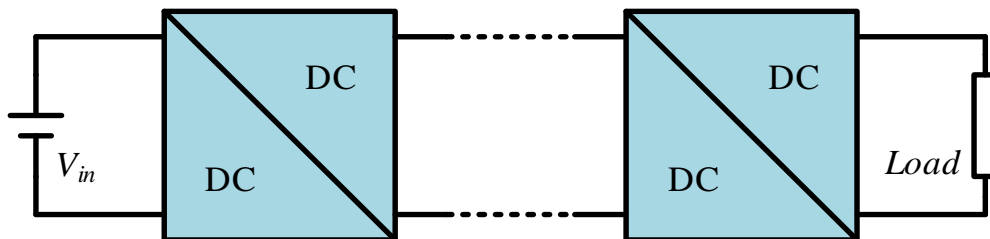
Figure 2.5 Configuration of cascaded DC/DC converter.

The output port of the previous boost converter is connected to the input port of the next following boost converter. Hence, the voltage step-up conversion ratio of the cascaded converter is increased to the product of the voltage gain of each boost converters. For example, the voltage gain of the cascaded connection of two boost stages shown in Fig 2.6 can be calculated according to the following equation.

$$G = \frac{V_{out}}{V_{in}} = \frac{V_{Cf1}}{V_{in}} \cdot \frac{V_{out}}{V_{Cf1}} = G_1 \cdot G_2$$
$$= \frac{1}{(1-D_1)} \cdot \frac{1}{(1-D_2)}$$

(2.2)

Therefore, a high voltage conversion ratio could be achieved without the unity duty cycle. Compared with a single conventional non-isolated boost converter, the voltage stress of the switch Q_1 and diode D_{o1} in the first stage converter is reduced, which leads to a low switching loss and conduction loss of switch Q_1 as well as better reverse recovery performance of diode D_{o1}. For the second conversion stage, the input current is reduced due to the intermediated voltage of capacitor C_{f1}, while the voltage stress of semiconductor components in the second conversion stage equals to the output voltage, which is the same as that in the single conventional non-isolated boost converter. The main disadvantage of the cascaded structure is that the complex control of two switches. Additionally, two closed-loop control circuits are required for the cascade converter to ensure stable operation, which increases the cost.
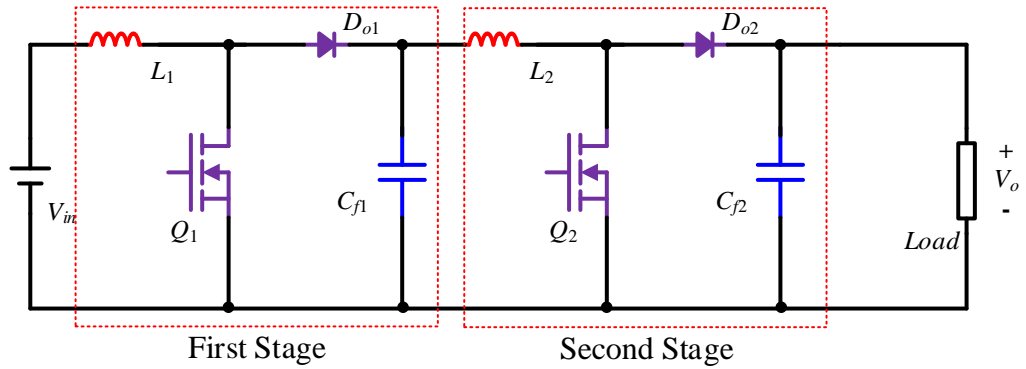
Figure 2.6 Cascade converter with two stages boost converters.

2.3.3   Quadratic Boost Converter

The quadratic boost converter as illustrated in Fig 2.7 using only one switch to achieve a high voltage conversion ratio is proposed to reduce the control complexity and increase the stability of the cascaded connection of two boost converters [45-48]. The switch Q_1 is replaced by the diode D_1 so that the switch count and the number of closed feedback control loop are reduced. The quadratic boost converter operates as the cascaded converter shown in Fig 2.6, and the following equation shows the voltage gain.

$$G = \frac{1}{(1-D)^2} \tag{2.3}$$

Similar to the cascaded converters, the quadratic boost converter can obtain high voltage gain without extreme duty cycle of switches. The main drawback is that energy

is converted twice, which affects the overall efficiency. Additionally, the switch Q and diode D_{o2} have high voltage stress and current stress so that the high rated components are required which causes increased conduction loss.
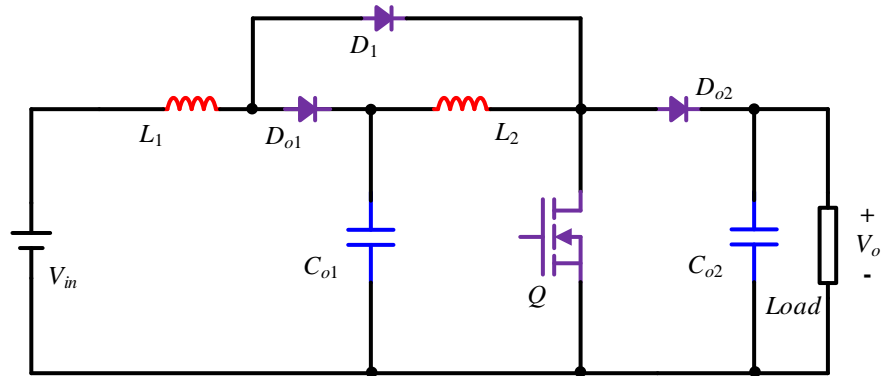
Figure 2.7 Quadratic boost converter.

2.3.4 Three Level Boost Converter

Fig 2.8 presents the three level boost converter, where the voltage stress of active switches equals to half of the output voltage [49-51]. Therefore, components with low on-state resistance could be installed so that the conduction loss is reduced. Additionally, there are also other advantages, such as the reduced switching loss of active switches and suppressed electromagnetic interference (EMI) noise. However, the three level boost converter has the same low voltage gain as that of conventional non-isolated boost converter shown in the below equation.

$$G = \frac{1}{1-D}$$

(2.4)

Where switches Q_1 and Q_2 have an identical control signal but are shifted by 180 degrees.

Therefore, the main drawback of the three level boost converter is that it can only obtain high voltage gain under extreme duty cycle, and the voltage gain is limited. Furthermore, the inductor current ripple is significant in high power applications.
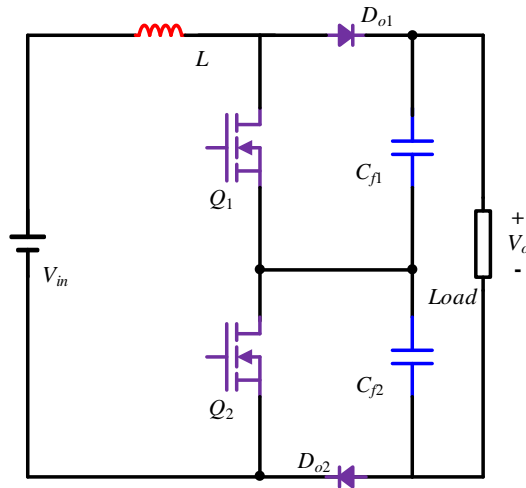
Figure 2.8 Three level boost converter.

2.3.5 Switched Capacitor Converters

The basic topology of switched capacitor converters is depicted in Fig 2.9, whose operation principle only involves electric energy transfer [52]. When switches Q_1 and Q_2 are on, and Q_3 is off, the voltage of the switched capacitor is increased to V_{in}. When Q_3 is on, and Q_1 as well as Q_2 are off, the capacitor C is series connected with the voltage source V_{in} to deliver power to the load. Hence, the high output voltage as the double value of the input voltage is achieved. With m switched capacitors charged in parallel and discharged in series as depicted in Fig 2.10, the voltage gain could reach $m+1$ times the input voltage.
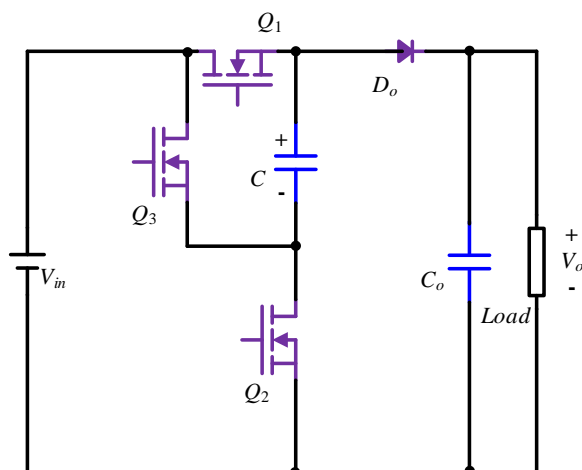
Figure 2.9 Topology of switched capacitor converter.
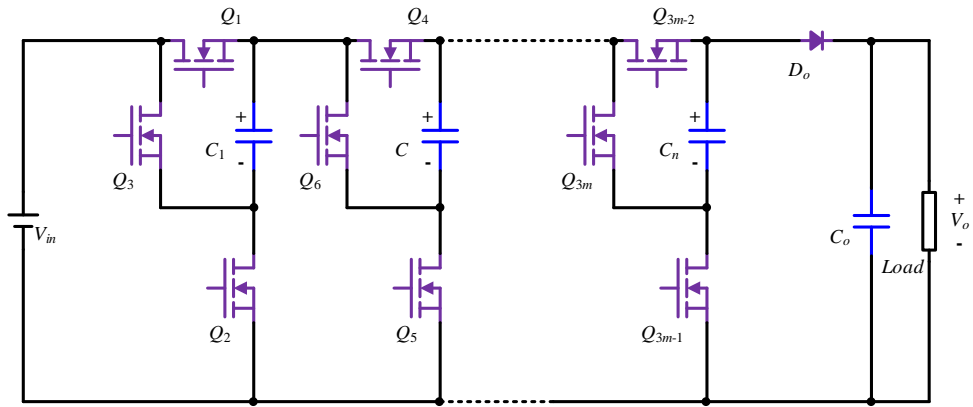
Figure 2.10 Cascaded *m* stages switched capacitor converter.

Without magnetic components, switched capacitor converters are famous for integrated circuit design due to their high power density [53-55]. However, a high voltage conversion ratio requires a large number of switched capacitor cells, and the voltage gain is always integer times of the input voltage. The cost and design complexity are high when a large amount of switched capacitor cells are applied. Additionally, there is a large current ripple of components because of the elimination of magnetic components. Hence, power quality and efficiency are low.

In [31-33], the switched capacitor cell is integrated into the boost converter, which is also called as the voltage lift circuit. The output voltage can be regulated by the duty cycles of switches to obtain a wide range of voltage conversion ratios. As depicted in Fig 2.11, the voltage lift cell is integrated with the conventional boost converter to increase the voltage gain. The capacitor C_1 is charged by the power source V_{in} and the inductor L_b when the switch Q is on. Then, when the switch is off, C_1 is in series connection with V_{in} and L_b to provide a high output voltage. Additionally, thanks to the inductor L_b, components would have a reduced current ripple. The main disadvantage is that the static voltage gain is still related to the number of voltage lift cells so that the high voltage step-up ratio is obtained with a large number of components. Additionally, the voltage stress of the switch is the difference value between the output voltage and the input voltage.
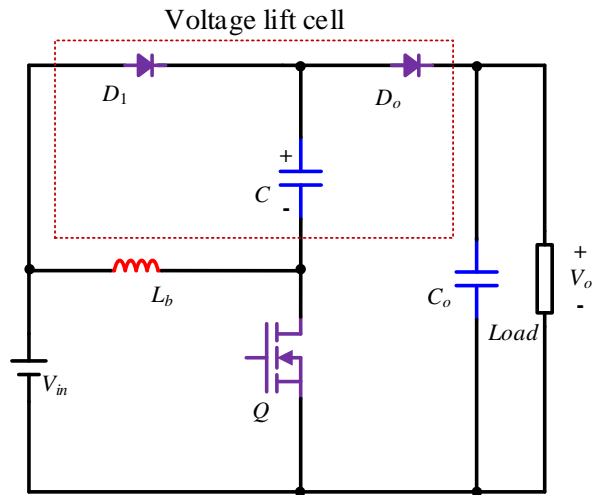
Figure 2.11 Topology of the voltage lift circuit.

2.3.6 Voltage Multiplier Circuits

Voltage multiplier circuits only contain capacitors and diodes as shown in Fig 2.12 that can convert AC power to DC power with a relatively high voltage level [56, 57]. The voltage multiplier circuits have the advantages as low design complexity and cost because of the simple structure and all passive components.

(a)

(b)

(c)
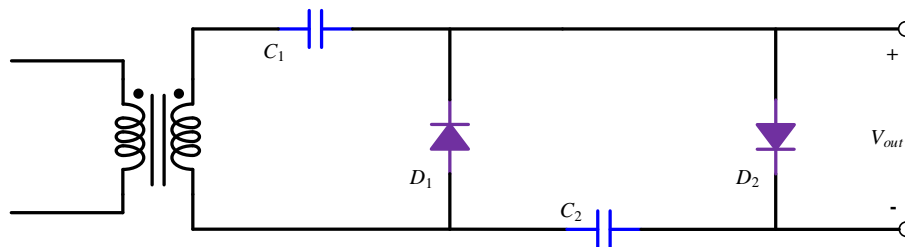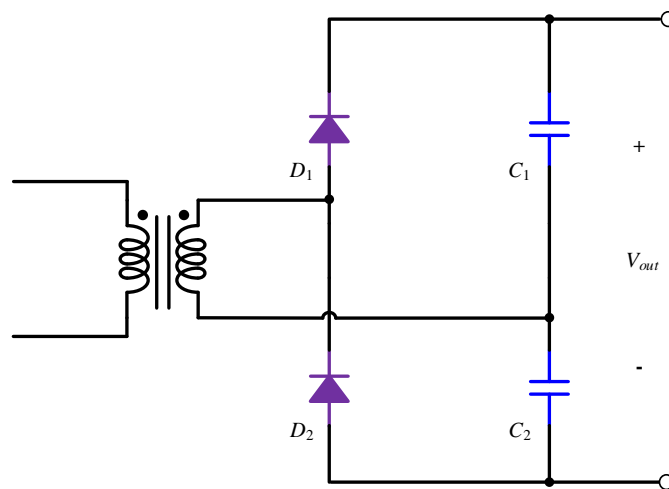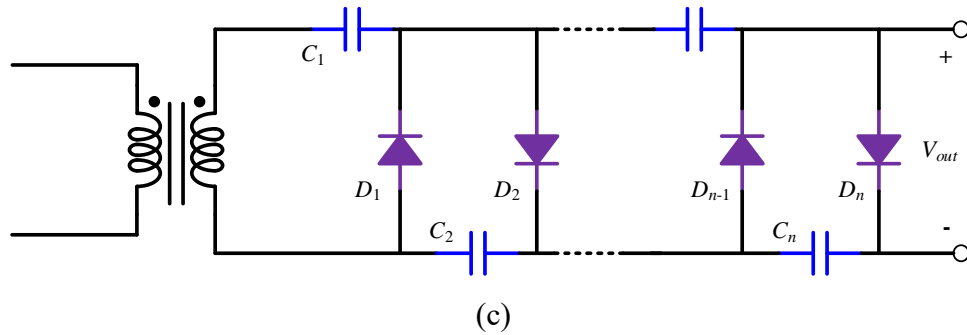
Figure 2.12 Topologies of voltage multiplier: (a) half-wave voltage doubler; (b) full-wave voltage doubler; (c) half-wave voltage multiplier extendable topology.

In the half-wave voltage doubler as shown in Fig 2.12 (a), the capacitor C_1 is charged through diode D_1 in the negative period, and the voltage of C_1 equals to the input voltage; then, the power from input source and C_1 is transferred to C_2 through diode D_2 when the voltage of transformer is positive. Hence, the voltage of C_2 and the output voltage are twice the input voltage. For the full-wave voltage doubler as depicted in Fig 2.12 (b), the voltages of capacitors C_1 and C_2 are charged to the input voltage during the positive and negative periods respectively. Hence, the output voltage is twice the input voltage since C_1 and C_2 are series connected. Fig 2.12 (c) shows the extension topology of the half-wave voltage multiplier circuit.

2.3.7   Switched Inductor Converters

With the similar operation principles of switched capacitor converters, switched inductor converters utilise the series connection of charged inductors and the voltage source to obtain a high output voltage [32, 36, 37, 58, 59]. As depicted in Fig 2.13, when switch Q is conducted, inductors L_1 and L_2 are charged through diodes D_1, D_2. After the switch is turned off, power is transferred from the input source together with both inductors L_1 and L_2 to the load through diode D_3. Hence, the value of the output voltage equals the sum of the input voltage and the voltage of either L_1 or L_2, where voltages of inductors L_1 and L_2 have the same value. However, the power efficiency is deteriorated because the voltage stress of switch Q is high, which equals the output voltage [32].
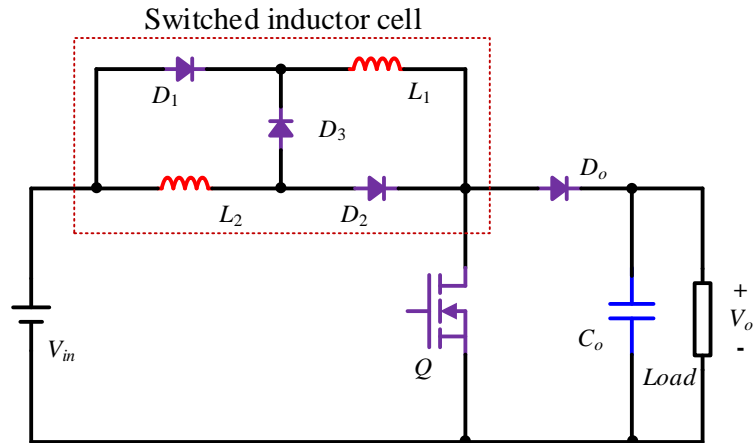
Figure 2.13 Topology of the switched inductor converter.

Fig 2.14 shows a two-switched-inductor-based boost DC/DC converter, which is also called as the active network converter. The active network converter is derived from switched inductor cell shown in Fig 2.13 by eliminating the diode D_3, and replacing the diodes $D_1 \sim D_2$ by active switches $Q_1 \sim Q_2$. When the two switches are conducted, the power is transferred into the inductors L_1 and L_2. When the switches are off, the power is transferred from the input and switched inductors to the output through diode D_o. Both switches have the same duty cycle.
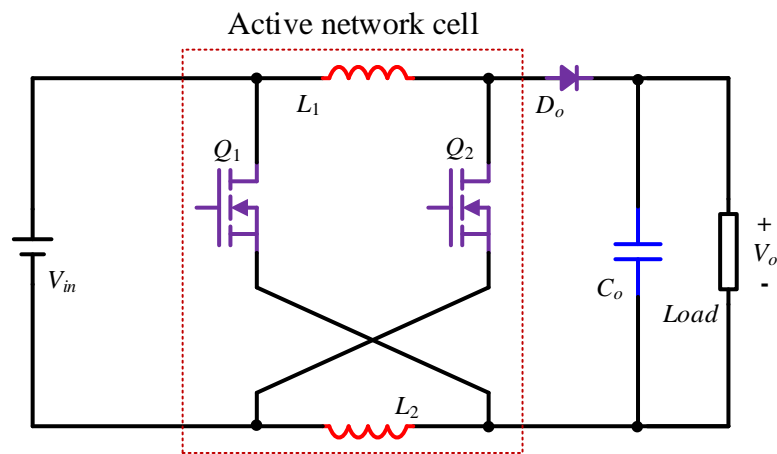
Figure 2.14 Topology of the active network converter.

Similar to the switched capacitor converter, the energy stored in inductors has an approximate magnitude of the input voltage. Therefore, the voltage gain of switched inductor converters is limited and cannot satisfy many applications. Although the voltage gain can be increased by replacing inductors $L_1 \sim L_2$ in the active network cell by switched inductor cells, the volume, weight, and cost of the converter will be

increased significantly [60]. Additionally, when there is a characteristic difference between the two inductors, currents of the two inductors are different. Furthermore, the voltage spike of switches is high when the switched inductors are discharged in series connection. Moreover, the voltage stress of diode D_o equals the sum of input and output voltages so that the reverse recovery loss is high.

2.3.8   Isolated Boost Converters

Fig 2.15 presents typical isolated converters consisting of the fly-back converter, the push-pull converter, the full-bridge (FB) and half-bridge (HB) converters that could achieve boost output voltage owing to the turns ratios N_s:N_p of transformers [61-67]. However, a high turns ratio would cause weak coupling between the primary and secondary windings resulting in low power efficiency. Additionally, high turns ratios also cause large leakage inductance, which leads to high voltage spikes when the switch is turned off [67]. Moreover, these converters have a significant input current ripple that degrades the performance of the solar panel and battery. To reduce the current ripple, input capacitors or input inductors are required, which would increase the volume and weight of converters.

(a)

(b)
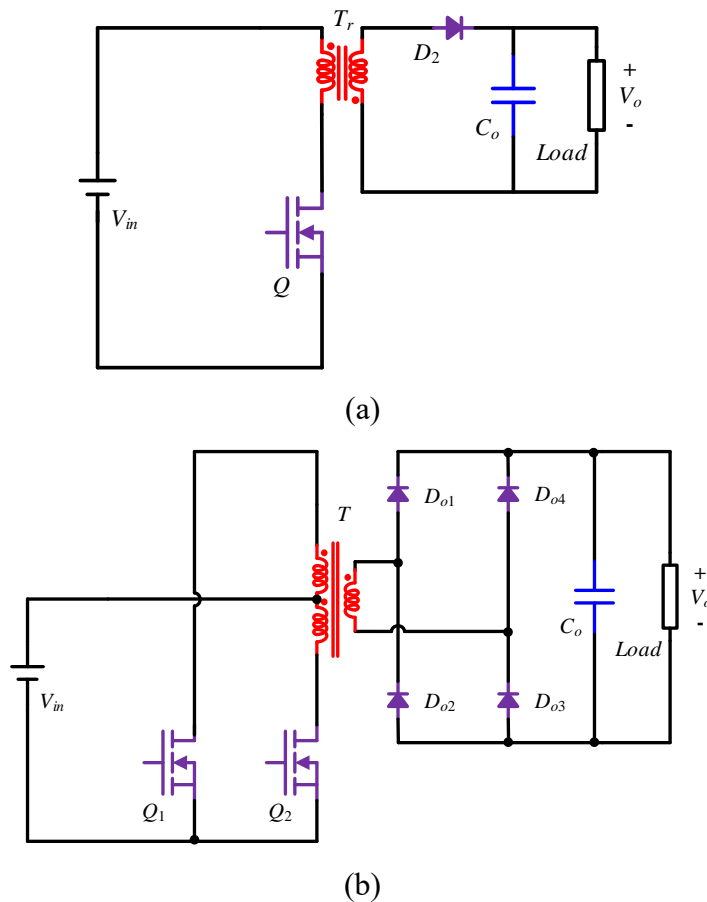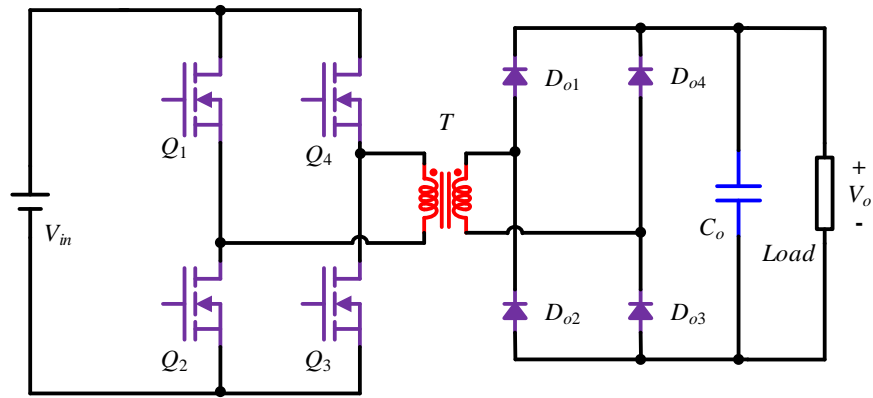
(c)
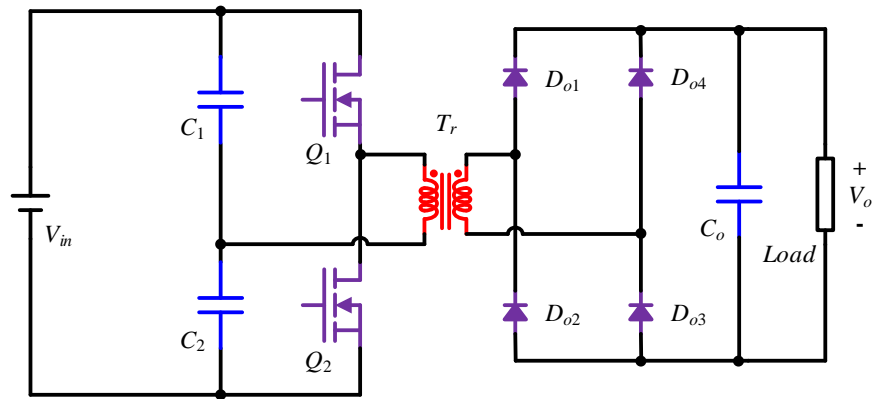
(d)

Figure 2.15 Typical isolated boost converters: (a) fly-back converter; (b) push-pull converter; (c) FB converter; (d) HB converter.

Fig 2.15 (a) presents the fly-back converter whose components count is low so does the cost. When switch Q is on, the transformer is charged, and the output power is transferred from the output capacitor. Then, the power stored in the transformer is delivered to the load when the switch Q is off. However, fly-back converters suffer from large current ripples, which requires a large EMI filter. Additionally, the fly-back converters have a higher power loss.

Fig 2.15 (b) depicts a push-pull converter. The drive signals for two main switches are 180° phase-shifted, and their duty cycles are larger than 0.5. When both switches Q_1 and Q_2 are closed simultaneously, the transformer is short-circuited. When there is only one closed switch, the power is delivered from the input source to the load. The voltage stress of switches is two times that of the output voltage.

The FB converter is shown in Fig 2.15 (c). Switches Q_1 and Q_3 have the same drive signal. Q_2 and Q_4 are also switched on and off at the same time. Additionally, the drive

signals for Q_1 and Q_2 have a 180° phase shift, and the duty cycles of two switches are larger than 0.5. When only switches Q_1 and Q_3 or Q_2 and Q_4 are closed, the power is delivered from the input source to the load. Compared with the push-pull converter in Fig 2.15 (b), the voltage stress of switches in FB converters is lower, which equals to the output voltage.

For HB converter illustrated in Fig 2.15 (d), the drive signals for the two switches are 180° phase-shifted, and their duty cycles are larger than 0.5. When only Q_1 is conducted, power from the input source is transferred to the capacitor C_2 and the load. Alternatively, the power from the input source is transferred to and capacitor C_1 and the load when switch Q_2 is conducted. The cost is reduced since the HB converter uses fewer active switches, while the turns ratio of the transformer is required to be twice that of the FB converter to obtain the same voltage gain.

In isolated converters, the leakage inductance of the transformer causes a high voltage spike when active switches are turned off. To reduce the voltage spike, auxiliary circuits are employed, which could recycle the energy stored in the leakage inductance. Therefore, power efficiency could be improved [68-71]. The auxiliary circuits such as the RCD snubber and the active clamp circuit are illustrated in Fig 2.16 (a) and (b) respectively.

(a)

(b)
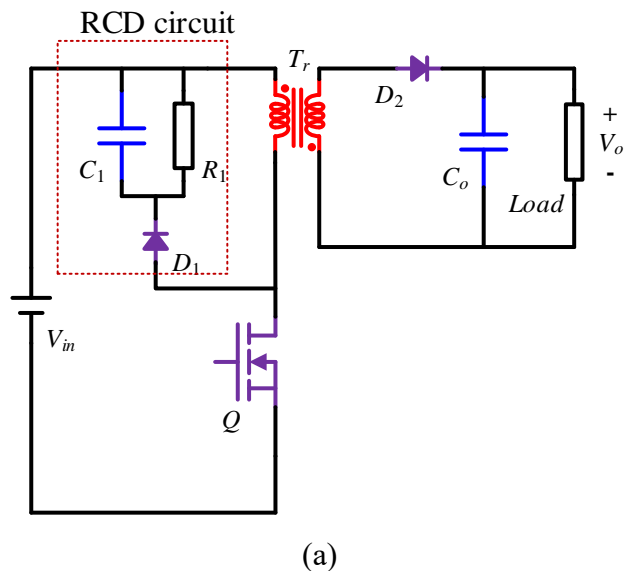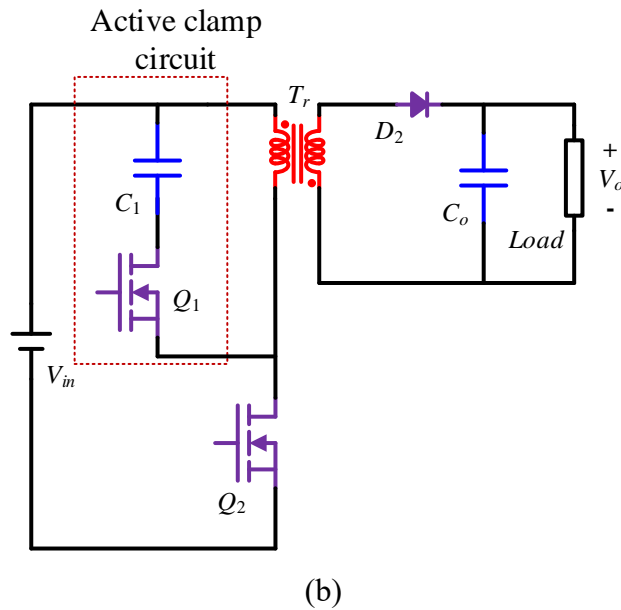
Figure 2.16 Auxiliary circuits for isolated boost converter: (a) RCD circuit; (b) active clamp circuit.

2.3.9 Coupled Inductor Converters

The voltage gain of boost converters could be increased by adding coupled inductors. As illustrated in Fig 2.17, a coupled inductor is employed to realise high voltage gain, whose primary winding connects to its secondary winding. The primary winding works as the input filter inductor. The secondary winding is the voltage source in series-connection to the output load. Compared with the conventional non-isolated boost converter, a higher voltage gain can be obtained by adjusting the turns ratio of the coupled inductor. Additionally, the clamp capacitor C_1 can recycle the energy stored in the leakage inductance, which increases the conversion efficiency.
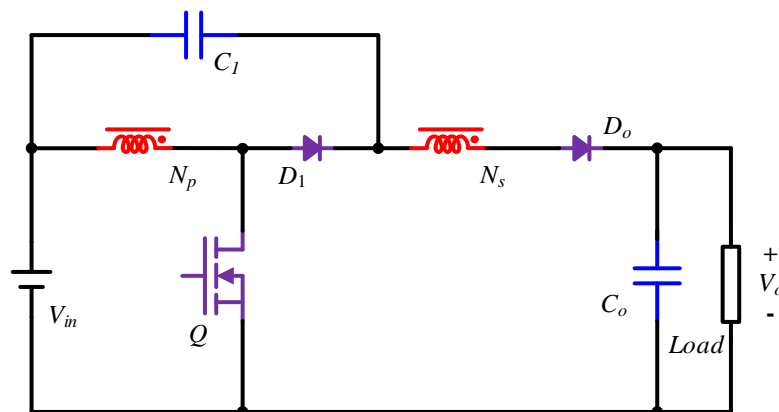
Figure 2.17 Topology of coupled inductor converter.

The topology shown in Fig 2.18 is derived by integrating the conventional non-isolated boost converter and the flyback converter, which could achieve a high voltage step-up ratio with the coupled inductor [72-74]. The coupled inductor is charged when the switch is on. After the switch is turned off, the output capacitors C_{o1} and C_{o2} are charged. The output ports of the conventional non-isolated boost converter and the flyback converter are in series-connection to enlarge the output voltage. However, in case of the voltage spikes caused by leakage inductance, installing energy regenerating techniques is necessary to clamp the voltage and improve the power efficiency, which will result in high cost and design complexity [75-77].
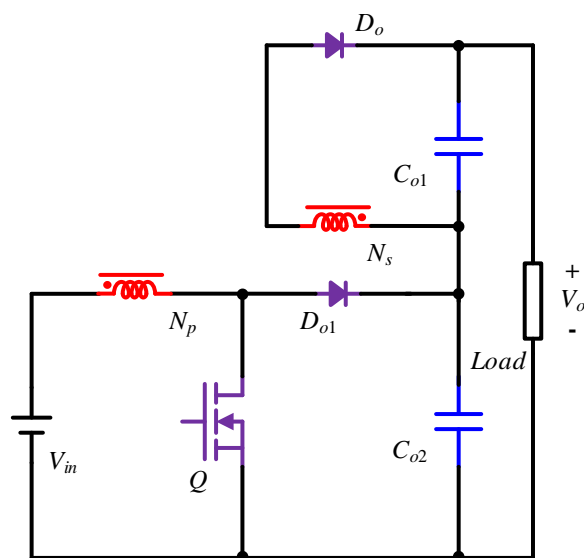
Figure 2.18 Topology of coupled inductor converter with two output capacitors.

2.3.10 Modular Multilevel Converters

Modular multilevel converters (MMCs) are prevalent in high power, high voltage applications [78, 79]. The typical topology is shown in Fig 2.19 with a stack of SMs, an input inductor, and one output LC filter. Unlike the cascade structure, the topologies of SMs in MMCs are based on the FB or HB converters, which are composed of switches and capacitors as depicted in Fig 2.20 [80, 81]. The output voltage is distributed into each SMs so that semiconductor components have a low voltage stress. With the series connection of SM, a high voltage gain is achieved.
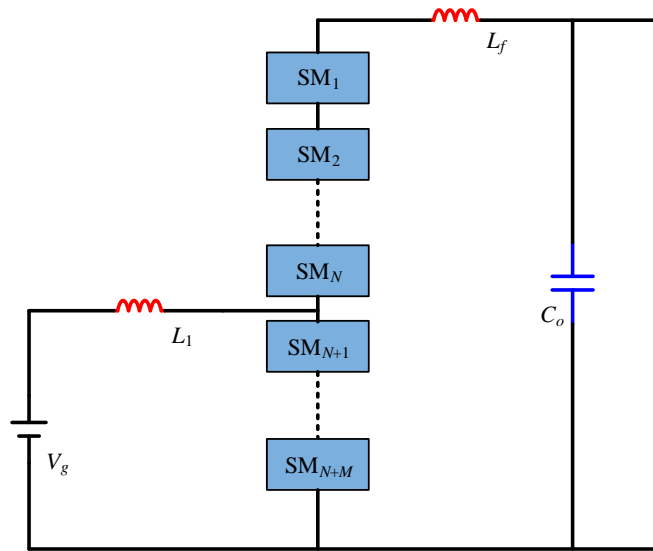
Figure 2.19 Configuration of MMCs.
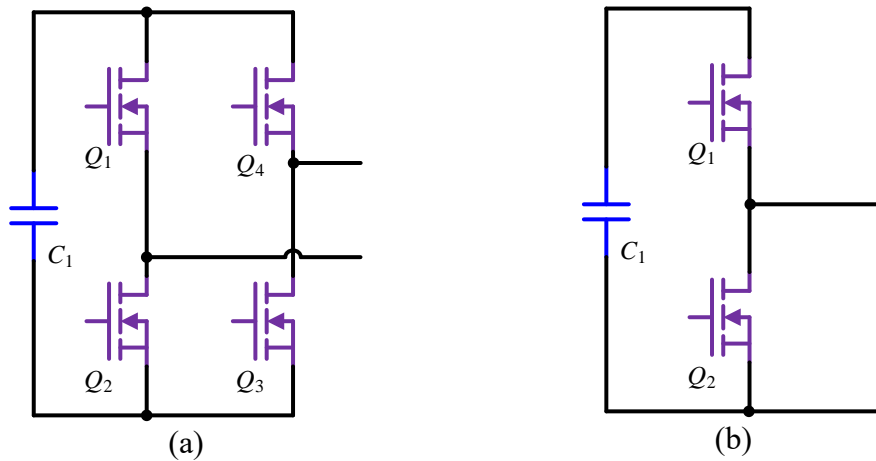
Figure 2.20 Topologies of SMs in MMCs: (a) FB circuit; (b) HB circuit.

2.3.11 Integrated Converters

According to the above discussion, no method could achieve high voltage step-up ratios without any drawbacks. The voltage gain of the conventional non-isolated boost converter and the three level boost converter are limited by the duty cycle of switches. Then, cascaded converters and quadratic boost converters could increase voltage gain by applying multiple cells in series connection, which uses a large number of components and leads to a complex control. The energy stored capacitors are successfully applied in switched capacitor converters and multiplier circuits to increase the output voltage; the charged inductors are installed in switched inductor converters to obtain a high voltage gain. However, the voltage gain of all these cases is increased with a significant increment of the components count. For the transformer-

based converters including isolated converters and coupled inductor converters, the high voltage gain is obtained by the high turns ratios of transformers, which leads to a large volume, high weight and high power loss. The core loss and winding loss of the transformer will reduce the power efficiency. Therefore, extensive researchers focus on the topologies integrating the capacitive method and magnetic method to design DC/DC converters with high efficiency and high voltage step-up ratios. For example, the voltage gain of converters could be extended by integrating coupled inductors and voltage multiplier circuits [82-86], coupled inductors and switched capacitors [87-90], three-state switching cells and auto transformers [91], three-state switching cells and voltage multiplier circuits [92]. With the integration, the following advantages can be obtained.

- With the integration, the voltage stress of active switches is reduced so that switches with low on-state resistance could be installed to reduce the conduction loss.

- The leakage inductance of transformers could be used to charge and discharge the parasitic capacitance of switches so that switches could achieve soft-swtiching operation without auxiliary circuits. Moreover, the leakage inductance can also reduce the current falling rate of diodes to reduce the reverse recovery loss and EMI noise.

- With a proper turns ratio, converters can achieve the desired voltage gain by an appropriate duty cycle of switches. On the other side, owing to voltage gain supplied by the switched capacitors or switched inductors, the turns ratios of transformers could be reduced so that the leakage inductance and the incurring current and voltage spikes.

2.4   Classification of DC/DC converters by Voltage Gain

Typical high voltage gain DC/DC converters are proposed in the last part to study their respective advantages and disadvantages. These converters can be catalogued as shown in Fig 2.21 according to whether they have an extensive voltage gain or not.
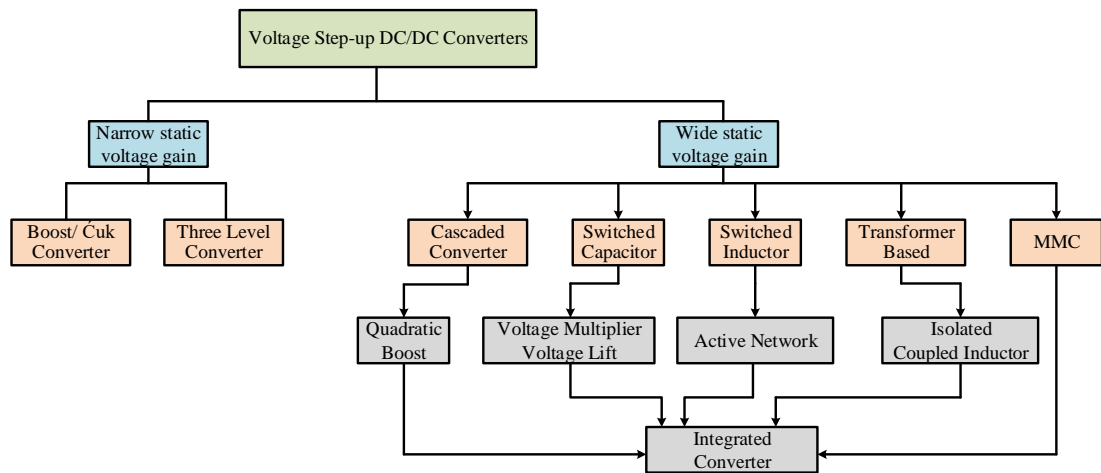
Figure 2.21 Classification of boost converters by voltage conversion ratio.

Conventional boost and Ćuk converters have a limited voltage conversion ratio. Besides that, the voltage gain ratio of three level converters is also limited. They can only achieve high voltage gain with an extreme duty cycle of switches. Wide static voltage gain converters extend their voltage step-up conversion ratio by installing multiple converter cells, switched capacitor, switched inductor, and transformers. For cascaded converters, switched capacitor/inductor converters, and MMCs, high voltage gain is achieved with a significant increment of components.

2.5   Converter Control Method

2.5.1   Voltage Control

Voltage control is one of the conventional control methods for converters [93]. As shown in Fig 2.22 (a), an error signal D_1 is generated by the error amplifier (proportional integral (PI) compensation) based on the difference between the output voltage and the reference voltage. The comparator compares the error signal D_1 and the sawtooth waveform V_t to obtain the control signal v_{gs1} for the switch Q_1 to realise the closed-loop control.

Some main waveforms of the closed-loop control circuit are depicted in Fig 2.22 (b). In the figure, there is only one control variable. Hence, design and analysis are relatively simple. This method has a strong anti-noise capability since the sawtooth has a significant amplitude compared with the error signal. However, the transient response is slow because the PI composition has a limited control bandwidth, and the change in the error signal takes a long time [94, 95]. Additionally, the voltage control

strategy cannot detect the output current so that auxiliary circuits are required to achieve overload protection.
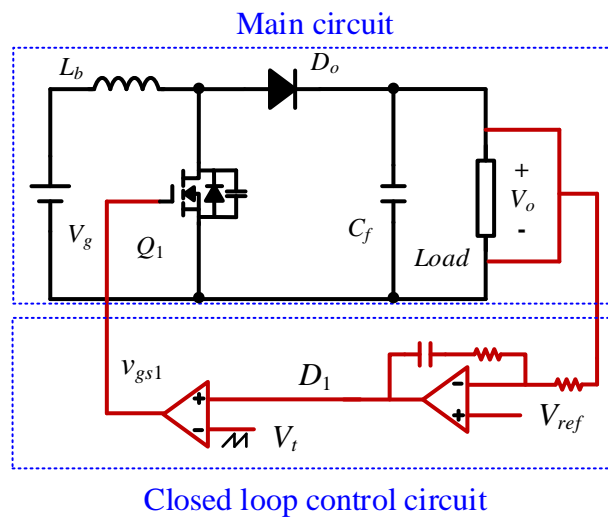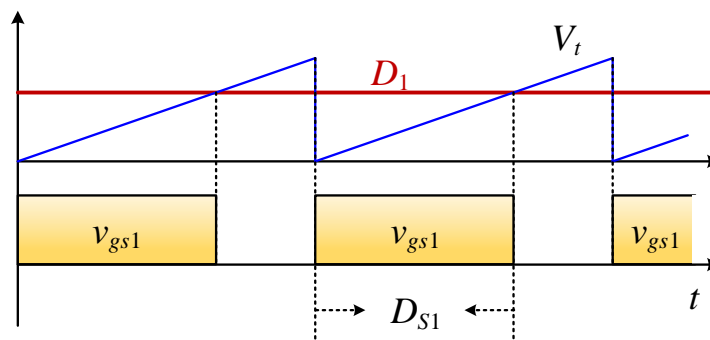
Figure 2.22 Voltage control system: (a) voltage control circuit; (b) key waveforms.

2.5.2 Current Control

Current control employs an additional current feedback loop as shown in Fig 2.23 (a) [96, 97]. The current control can be catalogued into three types as peak current control, valley current control, and average current control according to the detected inductor current i_L. Some main waveforms of peak current control are depicted in Fig 2.23 (b). Instead of the sawtooth waveform, the inductor current i_L is used to compare with the error signal D_1. The switch is turned off when i_L equals to the error signal. Then, the inductor current starts to decrease until the next clock pulse to set the trigger. After that, the switch is turned on, and the inductor current starts to increase.
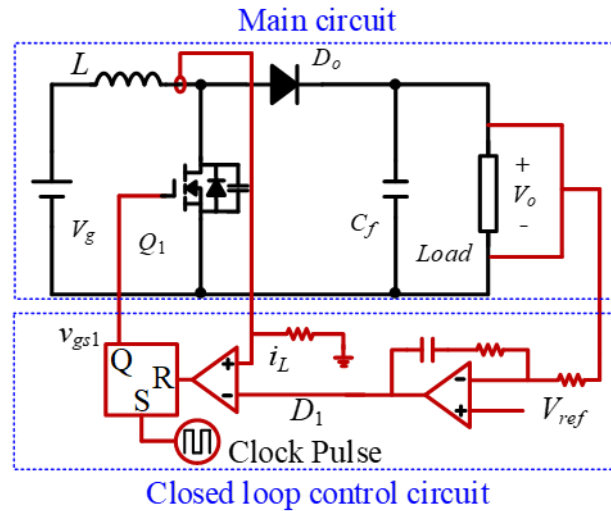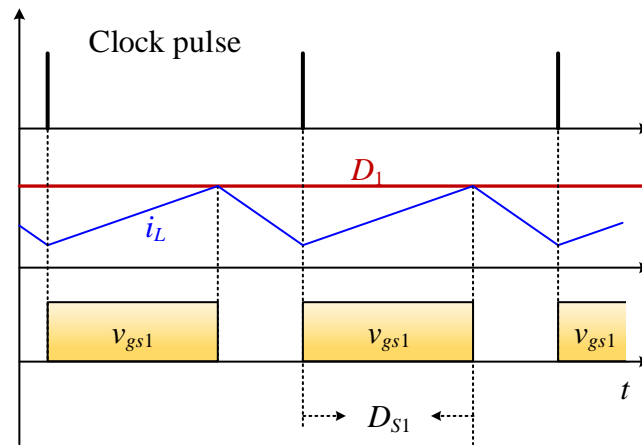
Figure 2.23 Current control system: (a) current control circuit; (b) key waveforms.

Current control has a better transient response performance compared with voltage control because there are two closed loops as the voltage loop and the current loop. Additionally, the current control systems have overload protection, and it can realise parallel current sharing among multiple converters [98]. However, when the duty cycle is larger than 0.5, harmonic oscillation happens in peak current control strategy leading to low system stability [99, 100].

2.6   Switching Strategy

In operation, semiconductor components have three kinds of power consumption, which are the conduction loss, the switching loss, and the driving loss. The driving loss is the power cost for turning power switches on/off, which is usually neglected.

Additionally, the conduction loss is presented as long as the corresponding devices are conducted, and it is only related to the on-state resistance of the device and the on-time t_{on} of the device in one cycle. Hence, the installation of components with low on-state resistance could reduce the conduction loss. The switching loss occurs when the switches are turned on or off, which could be reduced by decreasing switching frequency. However, the volume of passive components will be increased with the decreasing of switching frequency. Hence, techniques that reduce switching loss, such as soft-switching, are critical for the converter design to achieve objectives as high power efficiency and high power density.

2.6.1 Hard-switching

For hard-switching operation shown in Fig 2.24 [101], there are current-voltage overlaps during their switching periods, leading to the switching loss. When the switch is turned on, there is a specific time t_{ri} for the current rise to on-state value followed by the voltage fall time t_{fv}. The overlap area is the energy loss when the switch is turned on as $E_{on}=0.5\times(V_{DD}\times I_{D(on)})\times t_{turn\_on}$. When the switch is turned off, there is also an overlap area caused by the voltage rise time and current fall time as $E_{off}=0.5\times(V_{DD}\times I_{D(on)})\times t_{turn\_off}$. Then, the switching loss could be calculated as:

$$
\begin{aligned}
P_{switching} &= (E_{on}+E_{off})\cdot f_{sw}\\
&= (\frac{I_{D(on)}\cdot V_{DD}\cdot t_{turn\_on}}{2}+\frac{I_{D(on)}\cdot V_{DD}\cdot t_{turn\_off}}{2})\cdot f_{sw}
\end{aligned}
\tag{2.5}
$$

Where V_{DD} is the voltage stress; $I_{D(on)}$ is the on-state current stress, t_{turn_on} and $_{oturn\_off}$ are the time required to turn switches on/off; f_{sw} is the switching frequency. Hence, reducing the voltage/current stress of switches can reduce the switching loss. For a specific topology, reducing switching frequency can benefit the power efficiency of the converter.
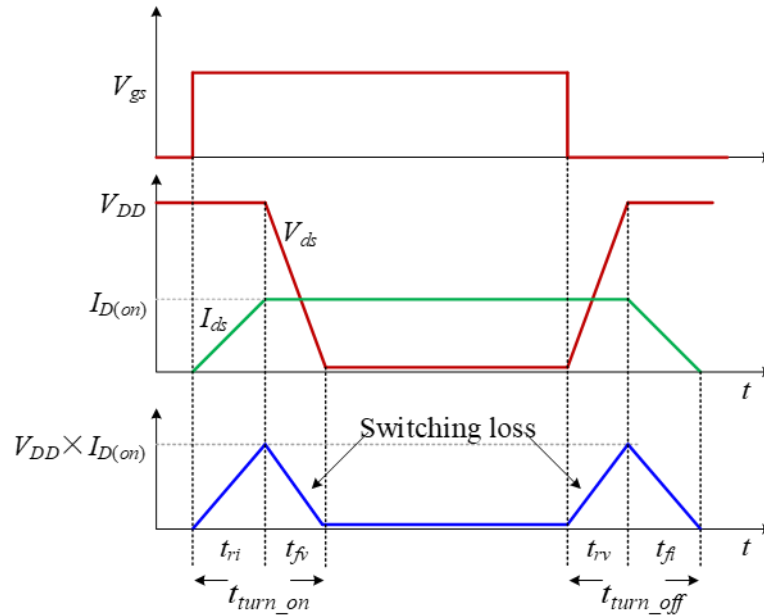
Figure 2.24 Typical hard-switching voltage-current waveform of power switches.

According to Eq.(2.5), power converters can reduce the switching loss by a low switching frequency. However, the low switching frequency will harm the power density and cost of converters. To meet the demanding of high compactness, the high operation switching frequency is essential to reduce the volume and weight of passive components such as capacitors, inductors, and transformers.

2.6.2 Soft-switching

Another way to reduce switching loss is applying an auxiliary resonant tank to ensure the voltage or current drops to zero before the turn on or off action of switches so that the overlap areas can be eliminated as shown in Fig 2.25. For example, turn on switching loss of MOSFETs could be eliminated when the parasitic capacitances of MOSFETs are discharged to zero before MOSFETs are turned on. Compared with IGBTs, the same power level MOSFETs have a much larger parasitic capacitance so that their main switching loss happens during the turn-on operation. Therefore, the zero-voltage-switching (ZVS) turn-on operation is essential for MOSFETs. Compared with MOSFETs, IGBTs have an additional substantial power loss during the turn-off transition caused by current trailing. Hence, zero-current-switching (ZCS) operation is mainly applied in the converters composed with IGBTs.
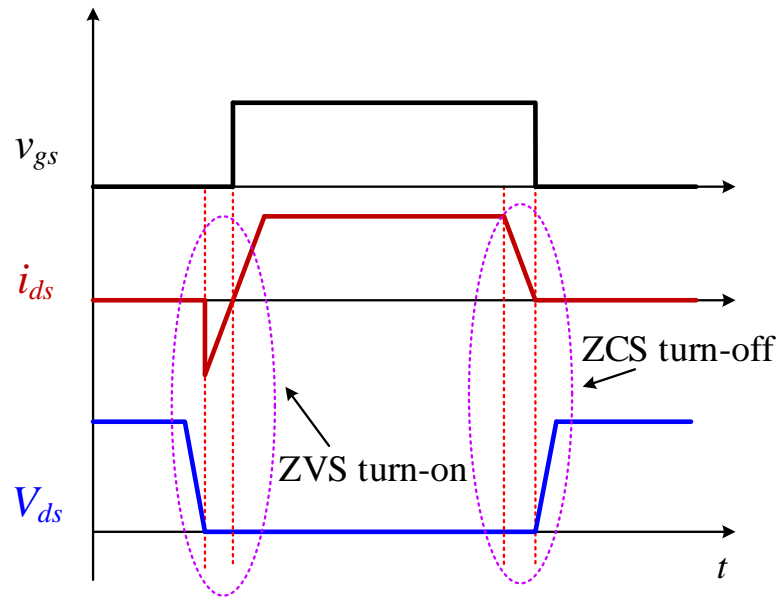
Figure 2.25 Typical soft-switching voltage-current waveform of power switches.

To achieve ZVS operation, resonant tanks are installed in converters as the configuration shown in Fig 2.26 (a). Fig 2.26 (b)~(e) present the passive circuits using only inductors and capacitors to form LC, LLC, LCC, and CLLC resonant tanks, respectively [102]. With specific parameters of these passive components, the value of output power and switching frequency are limited to a small range that can realise ZVS operation. Moreover, ZCS resonant tank for converters using IGBTs is presented in Fig 2.27. Alternatively, the active resonant tank illustrated in Fig 2.28 contains an additional switch to control its working states so that they can be successfully applied in converters that demand soft-switching operation within a wide voltage and current range.

(a)
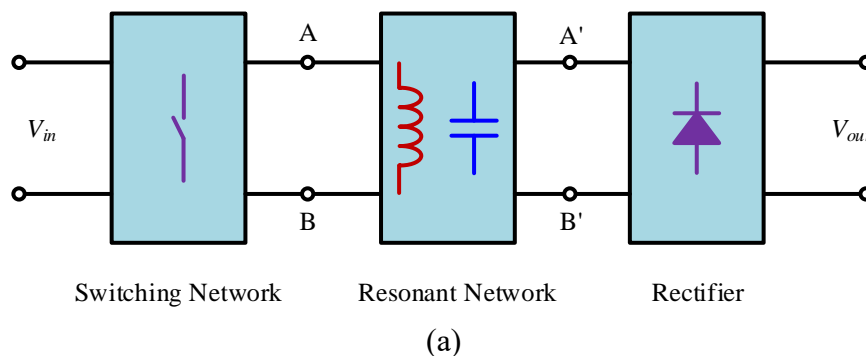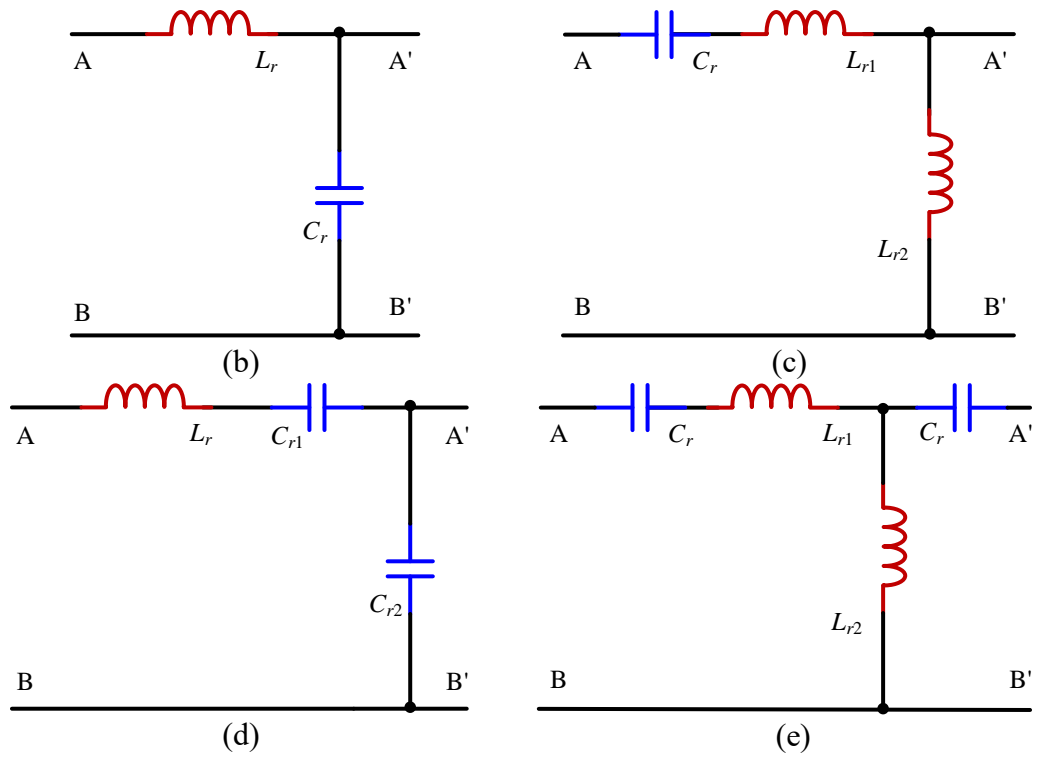
Figure 2.26 ZVS structure: (a) resonant circuit configuration; (b) LC resonant tank; (c) LLC resonant tank; (D) LCC resonant tank; (E) CLLC resonant tank.

(b)
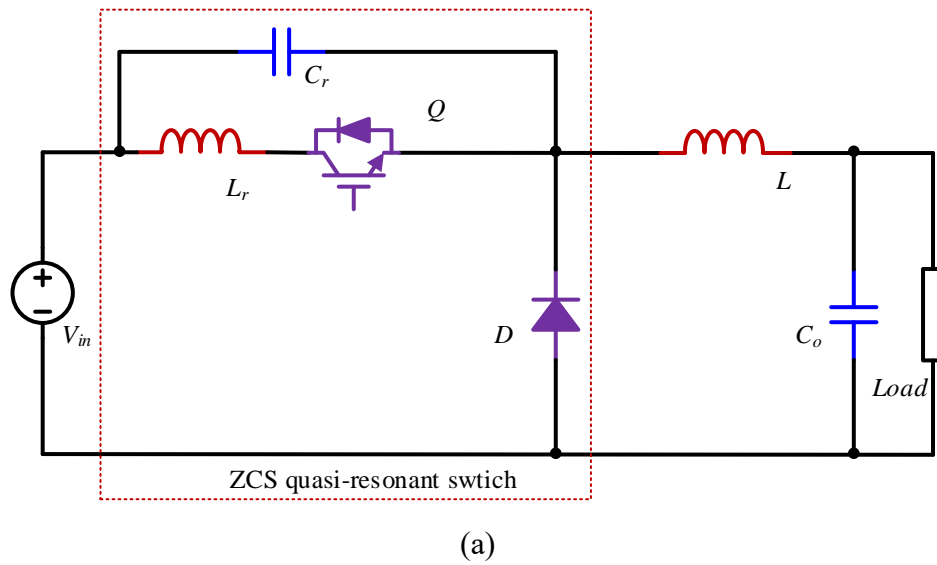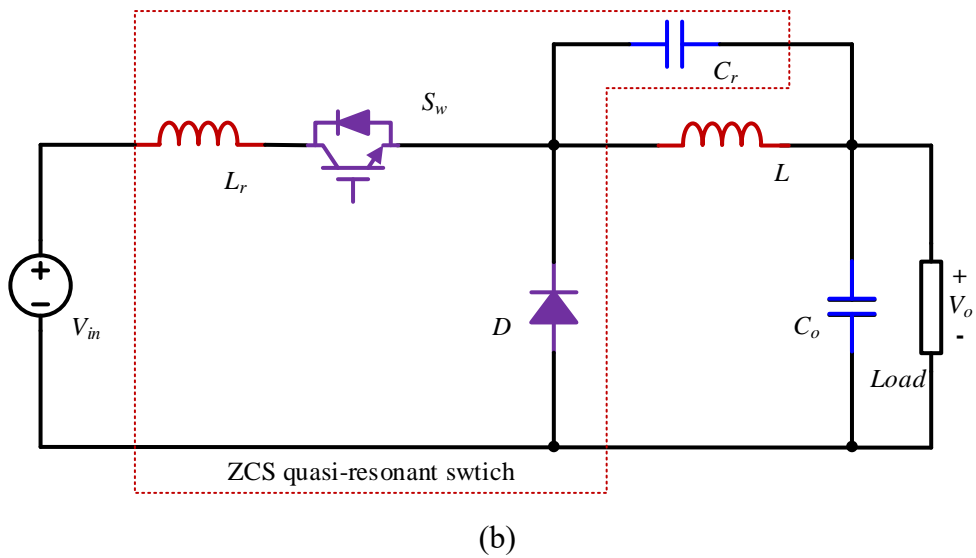
Figure 2.27 Installation of the ZCS quasi-resonant cell: (a) connection to the DC output; (b) connection to the DC input.
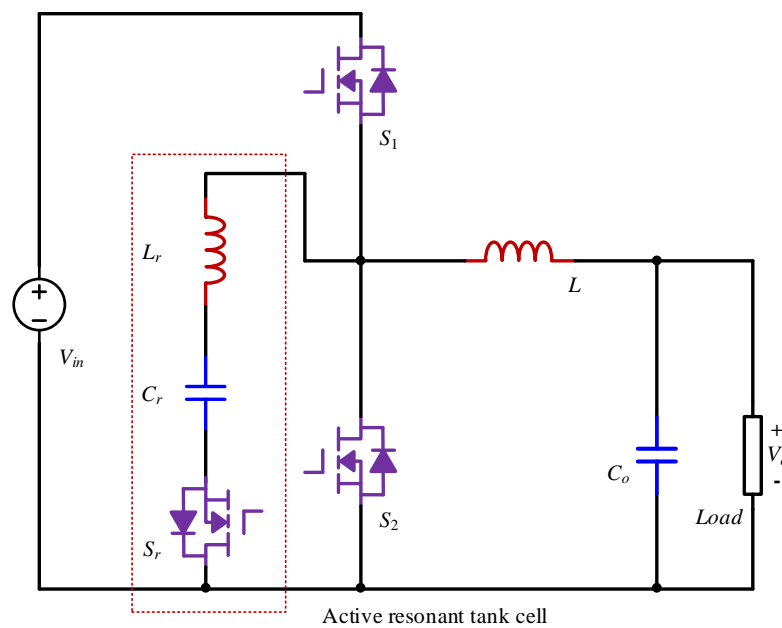
Figure 2.28 Active resonant tank circuit.

2.7 Failure Mechanism

According to field experience, the semiconductor components such as diodes, IGBTs, and MOSFETs are the most vulnerable components [103, 104], whose fault may cause series consequences related to personal safety. Therefore, the fault tolerance of power converters attracts much attention from academia and industry.

2.7.1 Failure Type

Faults can be catalogued into two types as short-circuit fault (SCF) and open-circuit fault (OCF). In DC/DC power converter, the SCF of components will cause an over-rated current flowing through the other elements such as output capacitor and load, which induces overheat resulting in break-down of the whole system and even explosion. Compared with the destructive consequences caused by SCF, OCF will shut down the power system and will not damage the other components. However, unexpected system shut-down will still put passengers into potential risks for some critical applications such as military, and aeroplanes.

2.7.2 Diode Failure Indications

Diodes are vulnerable components, especially when diodes operate under high voltage or high power applications. When diodes are short-circuited, the resistance drops to zero or a very low value in both forward and reverse directions. Occasionally, open circuit failure may occur, and the resistance of diodes becomes very high or infinite in both directions [105].

2.7.3 Transistor Failure Indications

Transistors such as IGBTs and MOSFETs are used under high voltages and currents scenarios while minimizing their internal power dissipation. It is possible to apply voltage, current and power exceeding the rated capability under fault conditions. Hence, the transistors are easily short-circuited. Additionally, the transistors would be open-circuited when the silicon chip is overheated and unsolder the transistor itself.

2.8 Summary

Based on the above analysis, extensive studies consisting of topologies, control methods, switching strategies and failure mechanism on high voltage step-up DC/DC converters have been done.

There are several typical topologies that could achieve a high voltage step-up ratio, such as cascaded converters, switched capacitor converters, switched inductor converters, transformer-based converters, and MMCs. However, each topology has specific limitations like high switch count number, large volume, low power efficiency, and leakage inductance problems. Therefore, extensive researchers focus on the

topologies integrating the capacitive method and magnetic method to solve the mentioned issues.

Additionally, the primary control and switching strategy of DC/DC converters are introduced in this section which is essential in the design of the following proposed converters. Furthermore, the fault tolerant capability is discussed in the high power application as HVDC transmission systems.

Chapter 3. MULTI-PORT HIGH VOLTAGE GAIN MODULAR POWER CONVERTER FOR OFFSHORE WIND FARMS

Due to the limitations of active switches, the use of a single high voltage step-up DC/DC converter cannot meet the ultra-high voltage level (320 kV in the DolWin project [16]) for HVDC transmission systems. Therefore, multi-module converters using multiple converters are developed to meet the bulk power and ultra-high voltage level [106]. Each converter is a SM of multi-module converters. The multiple SMs are connected in series to increase the voltage step-up conversion ratios, and adding the number of SMs in parallel connection could increase the power level. For the design of SMs, a high switching frequency is required to ensure a small volume of passive components such as capacitors, inductors and transformers to increase the power density. Then, all switches in SMs should realise soft-switching operation to reduce the switching loss. Additionally, voltage or current auto-balance of SMs should be obtained to reduce the control complexity since there will be a large number of SMs, and the connected components would have non-ideal factors.

This chapter presents a multi-module converter that can achieve a high voltage step-up ratio as 10× with only four SMs. Additionally, all components have a relatively low voltage/current rating. Compared with MMCs, the proposed converter can use fewer SMs to reach the same voltage conversion ratio. To achieve the above objectives, the integration of matrix configuration and current-fed push-pull SMs is designed. Thanks to the matrix configuration, output power and voltage level of the multi-module converter could be increased easily by adding SMs. Additionally, the voltage gain of SMs provides another degree of freedom to enhance the voltage step-up conversion ratio. Furthermore, high switching frequency as 5 kHz can reduce components size. Moreover, the leakage inductance of transformers in SMs could charge and discharge the parasitic capacitance of active switches (MOSFETs) to realise the soft-switching (ZVS) operation of all switches. The operation principles of the CFPP SM and the multi-module converter are analysed in detail. Simulation results verify the feasibility of the proposed multi-module converter.

3.1 Introduction

The global number of offshore wind farms is increasing in recent years [107, 108]. In Europe, 560 new offshore wind turbines were built in 17 wind farms in 2017 with a total generation capacity of 3148 MW, which is about 20% of the total offshore generation capacity [109]. The power generated offshore is typically transmitted over an average distance of 41 km (in 2017) through submarine cables before reaching a connection point with the onshore existing grid [109]. For example, Hornsea wind farm is located around 40 km away from the onshore station. Compared with HVAC transmission, HVDC transmission is the preferred method to transfer power over a long distance (>40 km) in terms of the economy and power efficiency [5, 6]. When delivering the same amount of power, the price of bipolar HVDC cable is lower than that of two parallel 3-core HVAC ones [10]. Additionally, HVDC has a higher transmission efficiency than HVAC since no inductance-reactive power exists within DC transmission cables.

Fig 3.1 presents three HVDC configurations. The hybrid HVDC system illustrated in Fig 3.1 (a) uses a medium voltage (MV) - high voltage (HV) AC/DC converter to obtain high voltage DC power. However, line-frequency (50/60 Hz) AC/AC transformers for low-voltage (LV) - MV conversion still occupy a significant portion of the substation space. In this topology, the transformer is replaced by a converter as shown in Fig 3.1 (b), which significantly reduces the system size and weight [110]. These two configurations use two-stage conversion to meet the voltage level of HVDC transmission. However, the configuration of two DC/DC conversion stages has the highest power loss, which is around four times of one conversion stage configuration presented in Fig 3.1 (c) considering the winding and core losses of transformers and the given datasheets of the semiconductors [111]. The converter applied in Fig 3.1 (c) not only provides a high voltage gain but also transfers power directly from multiple generators to HVDC terminals without bus cable. The converter design is a technical challenge for boosting LV directly to HV due to the conflict between the required high voltage level, e.g. ±320 kV [16], ±800 kV [112] and the restricted voltage ratings of semiconductor components, e.g. 22 kV for SiC thyristors, and 15 kV for SiC transistors [113].
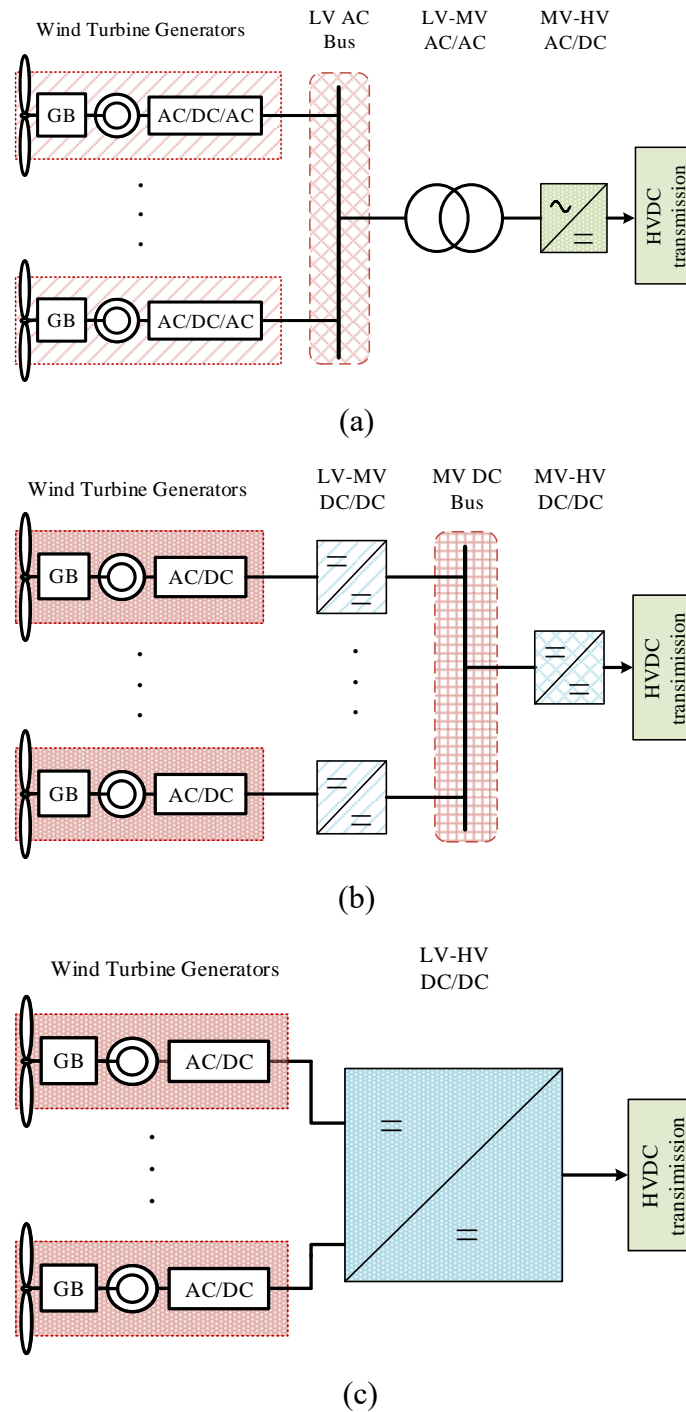
Figure 3.1 HVDC configurations for wind power transmission: (a) DC-based connection with two-stage hybrid conversion; (b) DC-based connection with two-stage DC/DC conversion; (c) DC-based connection with the proposed modular converter.

To address the challenges, DC converters with high voltage gains [114-117], MMCs [118-122] and multi-module converters [106, 123, 124] are studied. Although dual-active-bridge (DAB) converters [114, 115] and resonant converters [116, 117] can obtain high voltage step-up ratios, the voltage stress on their semiconductor

components is high, which can be reduced by applying MMCs. By adding SMs, a high output voltage is achieved without increasing the voltage stress. However, the MMC topologies based on HB or FB circuits [118, 119] and resonant MMC [120] cannot provide electrical isolation. The isolated MMCs in [121, 122] are presented with DC/AC/DC configuration, where medium-frequency high turns-ratio transformers are employed, resulting in a vast volume. Although resonant MMCs [125] achieve galvanic isolation and small volume of transformers at the same time, its conversion ratio only satisfies MV applications. Alternatively, transformers can be decentralized into multi-module converters, enabling the installation of high-frequency transformers, which reduces the sizes of transformers and passive components. However, by adopting active-clamping flyback-forward converters as SMs, the currents of different SMs are unbalanced because of the non-ideal factors such as unequable leakage inductances of transformers, and only half of the power switches can achieve ZVS, resulting in high switching loss [106].

In this chapter, active-clamping CFPP converters are adopted to replace the flyback-forward SMs in the multi-modular converter [106]. The currents of modules in series-connection are auto-balanced, and all power switches can achieve soft-switching. Therefore, the control complexity and switching loss are reduced. Furthermore, the matrix configuration brings about high control flexibility, which improves the fault tolerance capability. Additionally, thanks to the independent operation of each port, the converter can collect power from multiple sources without bus cable.

This chapter is organized as follows. The basic cell and two interleaved working modes are analysed in Section 3.2. Then the scalable topology design is discussed in Section 3.3. Section 3.4 depicts the fault tolerance strategies of the topology. Simulation results are presented in Section 3.5 to demonstrate the effectiveness and efficiency of the converter. Finally, the summary of this chapter is drawn in Section 3.6.

3.2   Design of the Proposed Multi-module Converter

3.2.1   Design and Operation of the SM

The basic cell topology based on CFPP converter shown in Fig 3.2 has the similar operation principles and characteristics with the converter presented in [62]. S_1~S_2 are

the two main switches. S_{c1}~S_{c2} are the two active clamping switches. C_c is the clamp capacitor. L_1 is the input transistor. The tri-winding transformer has a turns ratio of N_{p1}:N_{p2}:N_s=1:1:n and leakage inductance L_k at the secondary side. Furthermore, the secondary circuit consists of four rectifier diodes D_1~D_4, one output capacitor C_{out} and a load resistor R.
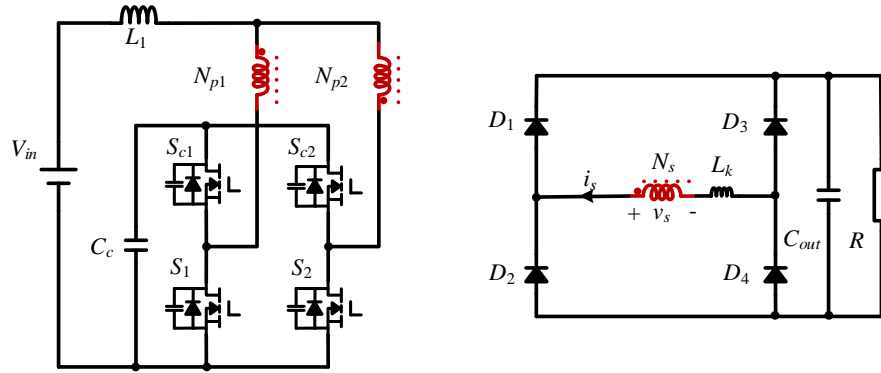
Figure 3.2 Topology of the basic cell on CFPP converter.

The key operating waveforms of CFPP cell are depicted in Fig 3.3. V_{gs1}~V_{gs2} are the control signals for the two main switches S_1~S_2, which have the phase shift angle of 180°. V_{gsc1}~V_{gsc2} are the control signals for the two clamp switches S_{c1}~S_{c2}. The control signals of the main switches and clamping switches are complementary. v_{ds1}~v_{ds2} and v_{dsc1}~v_{dsc2} are the drain-to-source voltages of the main switches and clamping switches respectively. i_{L1} is the current of input inductor L_1. v_s and i_s are the secondary voltage and current of the transformer respectively. The following assumptions are made to simplify the analysis.

- All switches and diodes are identical.

- The capacitance of clamp capacitor is large enough so that its voltage ripple can be ignored.

Due to the symmetrical operation, a brief introduction of the operation during t_0~t_5 when D≤0.5 is presented in this part.
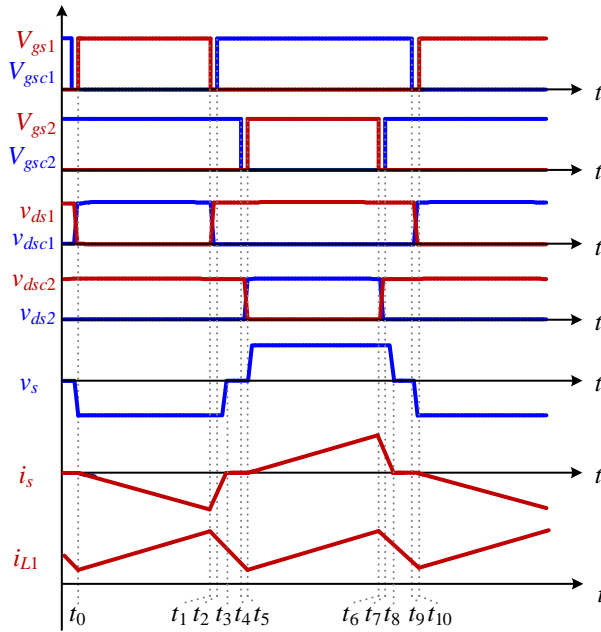
Figure 3.3 Operating waveforms of the basic cell.

Mode 1 (t_0-t_1): In this mode, the main switch S_1 and the clamping switch S_{C2} are on. The power is transferred to the output. The diodes D_2 and D_3 are forward biased, and the secondary current i_s decreases.

Mode 2 (t_1-t_2): At t_1, the main switch S_1 is turned off. The leakage inductances L_k resonate with the parasitic capacitances of S_1 and S_{C1}. Then, the voltage of S_{C1} drops to zero at t_2 to achieve zero voltage turn-on. At the same time, capacitance C_{S1} is charged.

Mode 3 (t_2-t_3): At t_2, the clamping switch S_{C1} is turned on with zero voltage. Because both the clamping switches S_{C1} and S_{C2} are on, the primary sides of the transformer are short-circuited. Then the power is transferred to the input inductor L_1, and the secondary current i_s rises rapidly.

Mode 4 (t_3-t_4): At t_3, the secondary current reaches zero. All four diodes are reverse biased. Additionally, the secondary voltage recovers to zero within a short time.

Mode 5 (t_4-t_5): At t_4, the clamping switch S_{C2} is turned off. The leakage inductances L_k resonate with parasitic capacitances of S_2 and S_{C2}. The voltage across S_2 drops to zero at t_5 so that ZVS operation of S_2 is obtained.

The operation in intervals [t_0-t_5] and [t_5-t_{10}] is symmetrical. The power is transferred to the output load R when one main switch and one clamping switch are on, and then the power flows from the input to inductor L_1 when both clamping switches are on. All

switches can obtain zero voltage turn-on and the energy stored in L_k is recycled by the parasitic capacitances of clamping switches, which contributes to a higher conversion efficiency.

The voltage of clamp capacitor V_{Cc} can be obtained according to the flux balance of L_1:

$$V_{Cc} = \frac{V_{in}}{1-D} \tag{3.1}$$

Additionally, with the turns ratio as 1:1:n, the output voltage of basic cell $V_{o,BC}$ can be determined:

$$V_{o,Bc} = \frac{n}{2}V_{Cc} = \frac{n}{2}\frac{V_{in}}{1-D} \tag{3.2}$$

The voltage stress of all four power switches V_{ds} can be obtained by:

$$V_{ds} = V_{Cc} = \frac{V_{in}}{1-D} \tag{3.3}$$

3.2.2   Design and Operation of the Matrix Configuration

A fundamental 2×2 modular topology is presented in Fig 3.4. The primary circuits of power cells are parallel connected so that they have an equal secondary voltage value with the same duty cycle of main switches. The secondary side of each cell is connected with four rectifier diodes for power regulation.
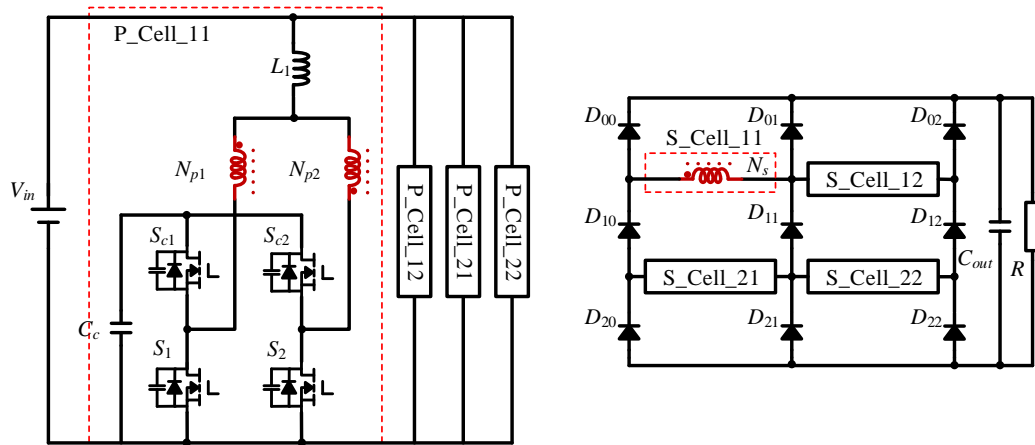
Figure 3.4 2×2 topology of the isolated high voltage gain DC/DC converter with basic cells.

As illustrated in Fig 3.5 (a) and (b), adjacent cells have opposite polarities in column interleaved modes. For example, the polarity of cell 11 is opposite to those of cell 21 and 12. In this case, cells in the same column are connected in series, and the adjacent columns are in parallel connection. The voltage ratings of diodes in the first and last rows, $D_{00} \sim D_{02}$ and $D_{20} \sim D_{22}$, are equal to the voltage of power cells v_s. While the voltage ratings of other diodes $D_{10} \sim D_{12}$ have twice the value of v_s since they are connected with two cells. The current rating of diodes in the first and last columns, $D_{00} \sim D_{20}$ and $D_{02} \sim D_{22}$ have the same value as the secondary current of one column. Diodes $D_{01} \sim D_{21}$ connect with two columns so that they have double the rated current of the others. Additionally, the sum of the average diode currents in all columns is equal to the output current. Therefore, in column interleaved modes, the voltage and current ratings of diodes in an expanded topology as shown in Fig 3.6 composed of s rows and p columns can be obtained:

$$V(D_{ij}) = \begin{cases} \dfrac{1}{s}V_{o,s\times p} = V_{o,BC} = \dfrac{n}{2(1-D)}V_{in} & i = 0, s \\[2ex] \dfrac{2}{s}V_{o,s\times p} = 2\times V_{o,BC} = \dfrac{n}{(1-D)}V_{in} & i = 1,2,\cdots,(s-1) \end{cases} \tag{3.4}$$

$$I(D_{ij}) = \begin{cases} \dfrac{1}{2}I_{o,BC} = \dfrac{1}{2p}I_{o,s\times p} & j = 0, p \\[2ex] I_{o,BC} = \dfrac{1}{p}I_{o,s\times p} & j = 1,2,\cdots,(p-1) \end{cases} \tag{3.5}$$

$$\sum_{j=0}^{p} I(D_{ij}) = I_{o,sp} \tag{3.6}$$

Where $I_{o,BC}$ is the average output current of single basic cell; $V_{o,s\times p}$ and $I_{o,s\times p}$ are the output voltage and current of $s\times p$ topology. In this case, all semiconductor components have low voltage and current ratings.

From Fig 3.5 (c) and (d), in series interleaved modes, all cells are series-connected. The cells in adjacent rows have the opposite polarities while the cells in the same row have the same polarity. Diodes D_{10} and D_{12} have twice the voltage rating higher than that of diodes in the first and last rows because they connect with two rows. The currents of all operating diodes have the same value since they are in series-connection.

Hence, the voltage and current ratings of diodes in series interleaved modes can be calculated as:

$$V(D_{ij}) = \begin{cases} \dfrac{1}{s}V_{o,s\times p} = p \times V_{o,BC} = \dfrac{p \times n}{2(1-D)}V_{in} & i = 0, s \\[3mm] \dfrac{2}{s}V_{o,s\times p} = 2p \times V_{o,BC} = \dfrac{p \times n}{(1-D)}V_{in} & i = 1, 2, \cdots, (s-1) \end{cases} \quad (3.7)$$

$$I(D_{ij}) = \dfrac{1}{2}I_{o,BC} = \dfrac{1}{2}I_{o,s\times p} \qquad\qquad j = 0, p \qquad (3.8)$$
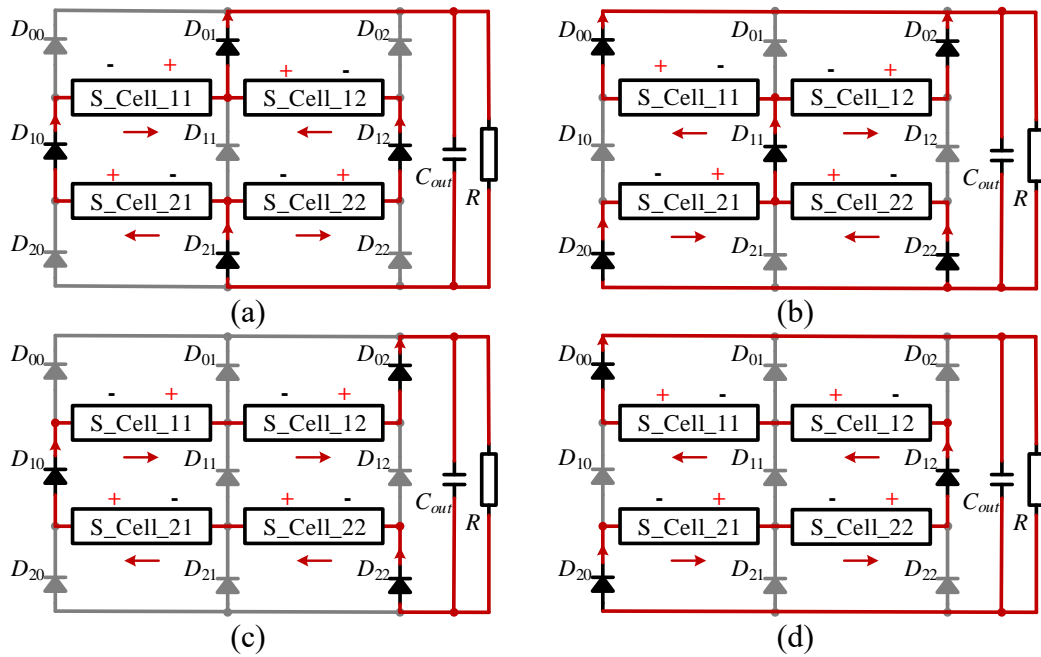
Figure 3.5 2×2 topology with different interleaved strategies: (a) column interleaved mode 1; (b) column interleaved mode 2; (c) series interleaved mode 1; (d) series interleaved mode 2.

According to Eq.(3.8), for series interleaved modes, the current rating of diodes is increased with the increment of output power. Besides, the diodes D_{01}~D_{21} are blocked, which benefits the fault tolerance operation to be described in Section IV.

3.3   Analysis of the Proposed Multi-module Converter

3.3.1   Scalable Topology

Thanks to modularity, multi-module converters can be easily expanded by increasing its row number and column number to attain a high voltage gain and the

desired high power level. In the normal scenario, the proposed converter operates with column interleaved modes to keep a low voltage/current rating of components. Three wind-turbine-generators, WTGs 1~3, are connected to the proposed converter as illustrated in Fig 3.6 (a). Fig 3.6 (b) shows the secondary circuits that are divided into three independent Groups 1~3 by diodes $D_{1\text{-}0p}$~$D_{1\text{-}sp}$, $D_{2\text{-}00}$~$D_{1\text{-}s0}$ and $D_{2\text{-}0p}$~$D_{2\text{-}sp}$, $D_{3\text{-}00}$~$D_{3\text{-}s0}$ based on input ports. The output power of each group consisting of the $s \times p$ expanded topology can be controlled individually and the bus cable is eliminated. With the same input voltage and power of each port, the voltages and currents of all basic cells are identical.

(a)

(b)
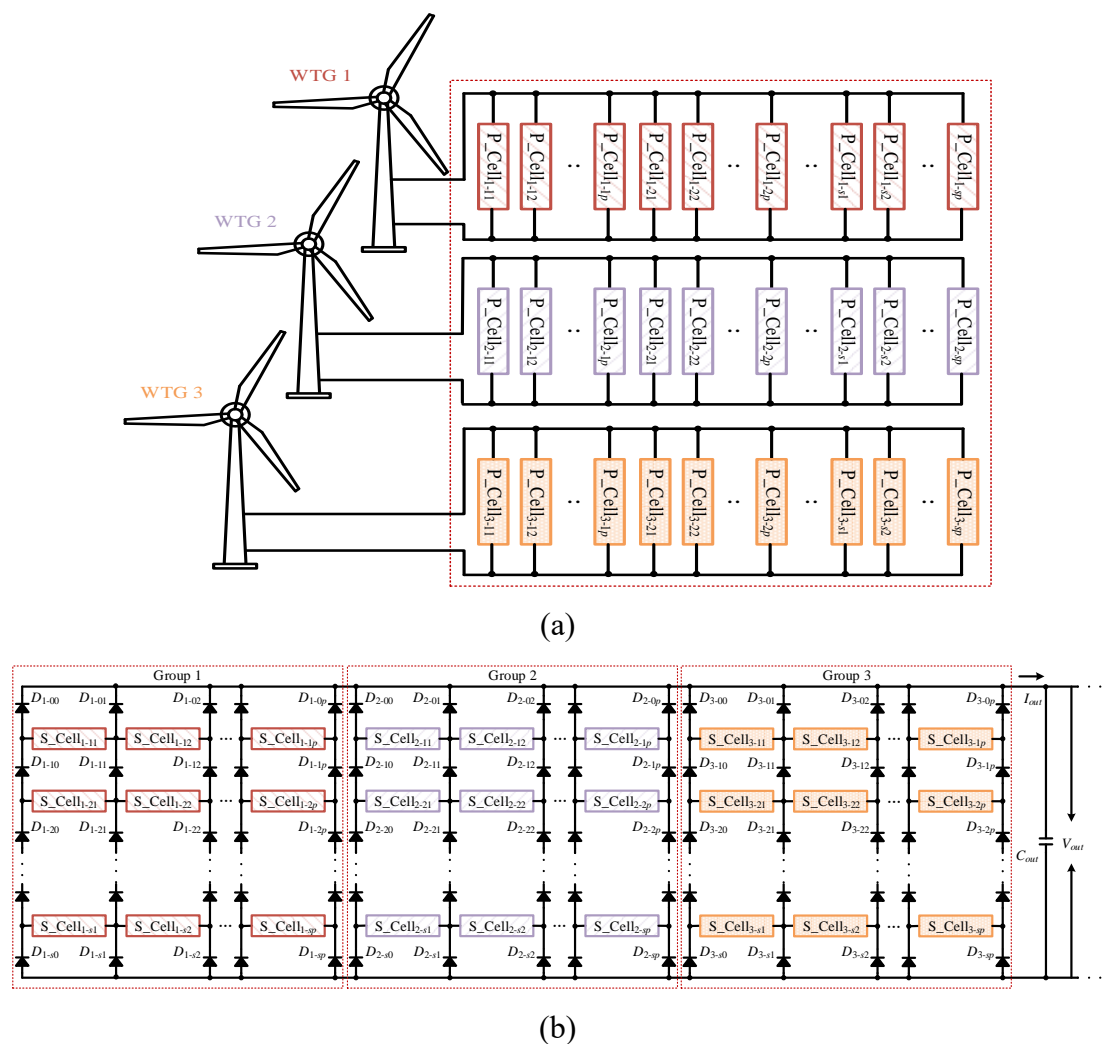
Figure 3.6 Topology of the proposed converter with three input-ports: (a) primary circuits with three power sources; (b) secondary circuits collecting power and delivering it to load.

3.3.2 High Voltage Step-up Ratio

The cells in the same column are in series-connection. Hence, every column has the same terminal voltage which is the sum of the voltages of cells in the same column. For converter with multi-ports, output voltage V_{out} equals to the identical terminal voltage of columns and the output current I_{out} is the sum of secondary currents of all columns. Therefore, the row number s determines the output voltage and the group number x with column number p determines the output power.

$$\begin{cases} V_{out} = V_{o,s \times p} = s \times V_{o,BC} = \dfrac{s \times n}{2(1-D)} V_{in} \\ I_{out} = x \times I_{o,s \times p} = x \times p \times I_{o,BC} \end{cases} \tag{3.9}$$

3.3.3 Current Balance with Column Interleaved Mode

The control complexity is reduced by the auto-balanced currents of cells in the same column. According to the currents through diodes $D_{10} \sim D_{13}$ and $D_{20} \sim D_{23}$ as shown in Fig 3.7, the relationships among all cells can be obtained as:

$$\begin{cases} I_{o,BC11+} + I_{o,BC12+} = I_{o,BC21+} + I_{o,BC22+} \\ I_{o,BC31+} = I_{o,BC21+} \\ I_{o,BC23+} = I_{o,BC13+} \\ I_{o,BC32+} + I_{o,BC33+} = I_{o,BC22+} + I_{o,BC23+} \end{cases} \tag{3.10}$$

$$\begin{cases} I_{o,BC11-} = I_{o,BC21-} \\ I_{o,BC31-} + I_{o,BC32-} = I_{o,BC21-} + I_{o,BC22-} \\ I_{o,BC12-} + I_{o,BC13-} = I_{o,BC22-} + I_{o,BC23-} \\ I_{o,BC33-} = I_{o,BC23-} \end{cases} \tag{3.11}$$

Where $I_{o,BC+}$ is the average current of secondary circuit in the interval $[t_0 \sim t_5]$ and $I_{o,BC-}$ is that in the interval $[t_5 \sim t_{10}]$. According to the symmetrical operation of the basic cell between the two intervals, it can be derived that $I_{o,BC+} = I_{o,BC-}$. Therefore, Eq.(3.12) is obtained with $I_{o,BC} = I_{o,BC+} + I_{o,BC-}$.

$$\begin{cases} I_{o,BC11} = I_{o,BC21} = I_{o,BC31} \\ I_{o,BC12} = I_{o,BC22} = I_{o,BC32} \\ I_{o,BC13} = I_{o,BC23} = I_{o,BC33} \end{cases} \tag{3.12}$$
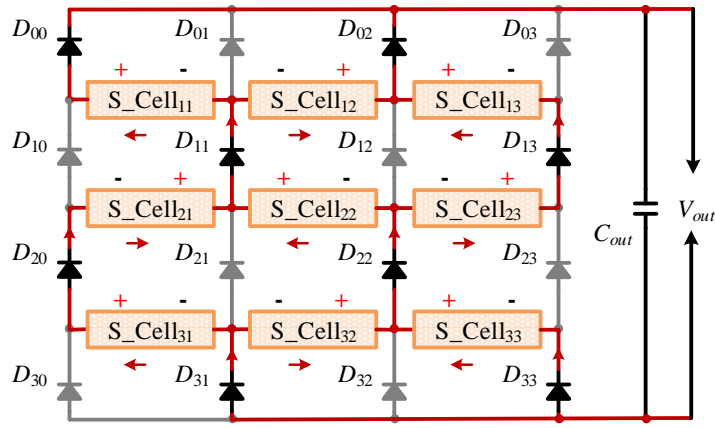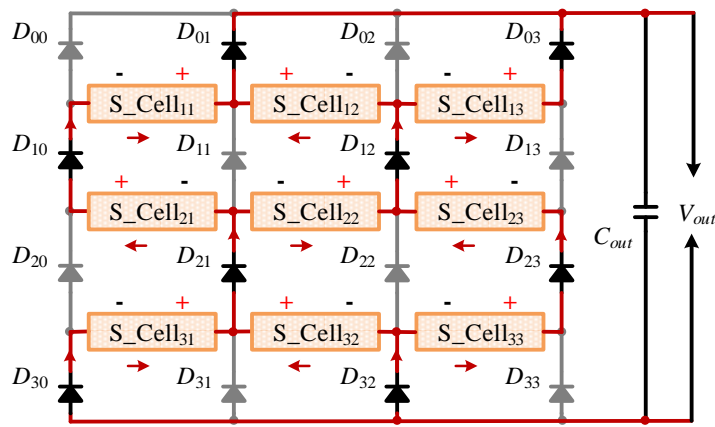
Figure 3.7 Auto-balanced currents of cells in the same column with column interleaved working strategy: (a) column interleaved working mode 1; (b) column interleaved working mode 2.

3.3.4 Closed Loop Control

According to Eq.(3.12), the average currents for cells in the same column are auto-balanced. Therefore, as shown in Fig 3.8, only the control of output voltage and current sharing in different columns is employed to achieve the required output voltage and power in the $s{\times}p$ topology, where $v_{o,ref}$ is the desired output voltage and $i_{L,i1}{\sim}i_{L,ip}$ are the currents collected from columns $1{\sim}p$.
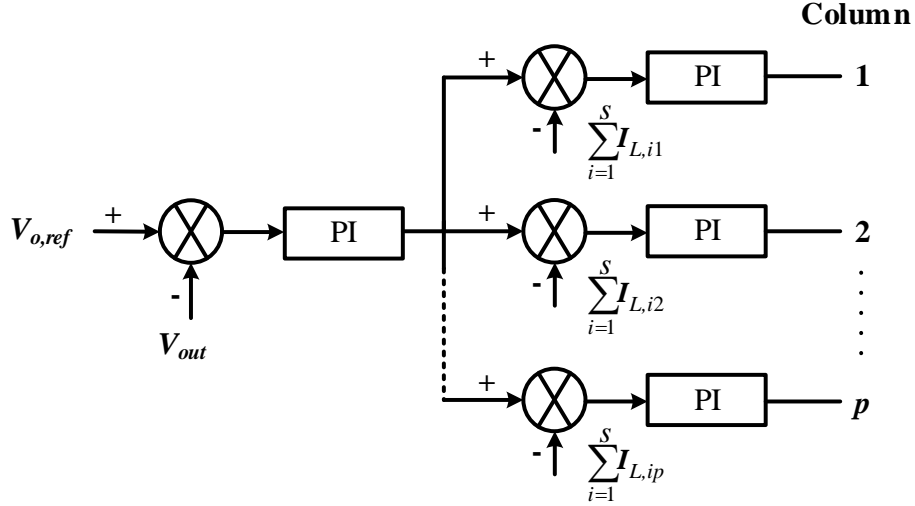
Figure 3.8 Control scheme of the $s{\times}p$ topology.

3.4 Fault Tolerance

3.4.1 Fault Tolerance for WTGs with Different Output Power

When disturbances occur, proper control strategies of WTGs and converters should be applied to ensure system protection and high power efficiency [126, 127]. For the proposed converter, not only the column number of the secondary circuits but also the duty-cycles of main switches determines the output power of one group. The output power of one group is obtained as:

$$P_{group} = (p-m) \times V_{out} \times I_{o,BC} \tag{3.13}$$

Where m is the number of idle column in the corresponding group.

The variation of duty-cycle will cause the change of currents through the cells in one column as:

$$I_{sub} = I_{o,BC} = \frac{2}{T_s} \cdot \int_0^{t_{on}} i_{out} \approx i_{max} \cdot D \tag{3.14}$$

Hence the output power is:

$$P_{group} = p \cdot V_{out} \cdot I_{sub} = p \cdot D \cdot V_{out} \cdot i_{max} \tag{3.15}$$

Where i_{max} is the maximum output current of power cells.

3.4.2   Redundancy Fault Tolerance

Semiconductor components are vulnerable components in a converter [128]. For offshore HVDC stations, fault components take long time for maintenance, resulting in high cost and loss [104].

Fig 3.9 shows the fault tolerance operation derived by installing redundant power cells. To maintain the normal operation, the column in a red dotted rectangle containing the damaged Cell 11 is replaced by one redundant column that is in the other red dotted rectangle. For the faulty diodes $D_{00}{\sim}D_{s0}$, they require only one redundant column since they connect with one column. However, for other diodes, two redundant columns are demanded. For example, when diode D_{11} fails, the columns $1{\sim}2$ in the blue dotted rectangle are idle, and the redundant columns $p1{\sim}p2$ are applied.
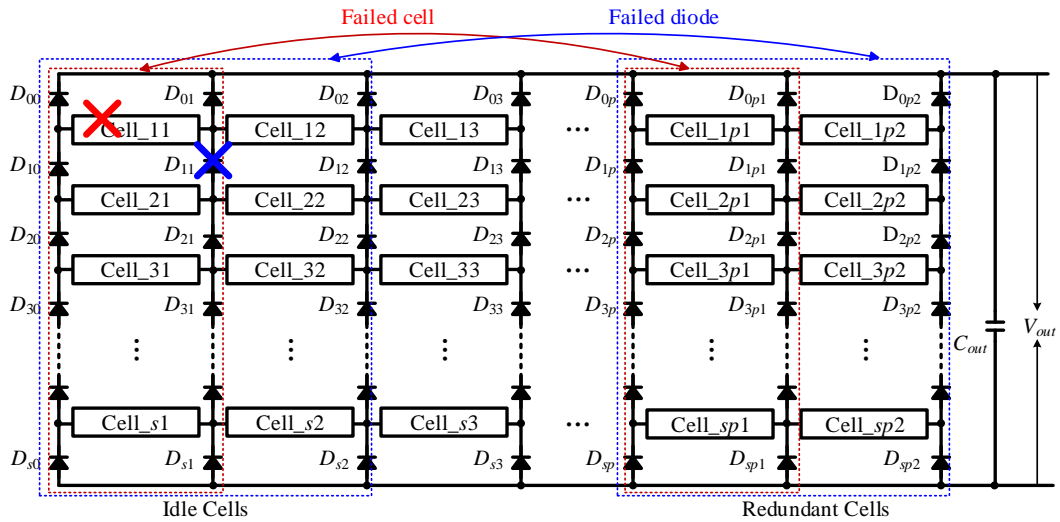
Figure 3.9 Fault tolerance with redundancy.

3.4.3   Fault Tolerance of Short-circuited Diodes and Failed SMs

The proposed topology can also obtain fault tolerant operation of diodes and power switches without redundancy. In Fig 3.10, when diode D_{11} is short-circuited, the cells in rows $1{\sim}2$ are inactive to block the faulty components, while the fault tolerance group still operates with the column interleaved strategy. Additionally, to maintain normal operation, the output voltages of the faulty group are controlled according to Eq.(3.2) and (3.9) to ensure the output voltage is the same as that in the normal case. Moreover, the fault tolerant operation of damaged cells without redundancy is similar to that when

diodes are short-circuited. For instance, when cell 11 fails, cells 11~1*p* and 21~2*p* are idle so that the faulty one is blocked.
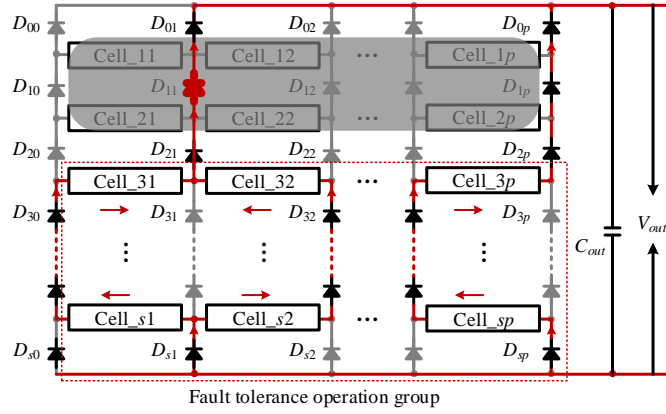
(a)
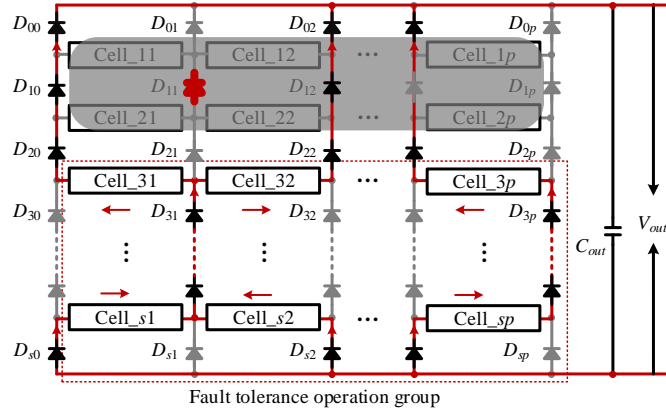
(b)

Figure 3.10 Fault tolerance when diode D_{11} is short-circuited: (a) working mode 1; (b) working mode 2.

3.4.4　Fault Tolerance of Open-circuited Diodes

When diode D_{11} is open-circuited, the fault tolerant operation group consisting of two columns works under the series interleaved modes to block D_{11} as illustrated in Fig 3.11 (a)~(b). Compared with the normal operation group, the number of cells in series connection in the faulty group is doubled. The voltages of cells in the fault group are adjusted as illustrated in Eq.(3.16) to keep same terminal voltage.

$$V_{o,FBC} = \frac{V_{o,s\times p}}{2\times s} = \frac{1}{2}V_{o,BC} \tag{3.16}$$
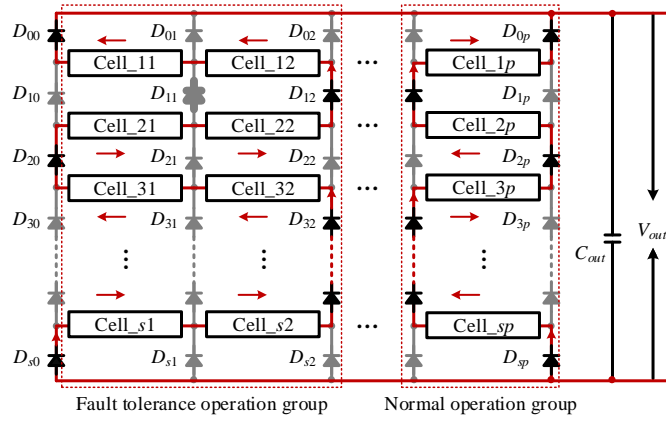
(a)
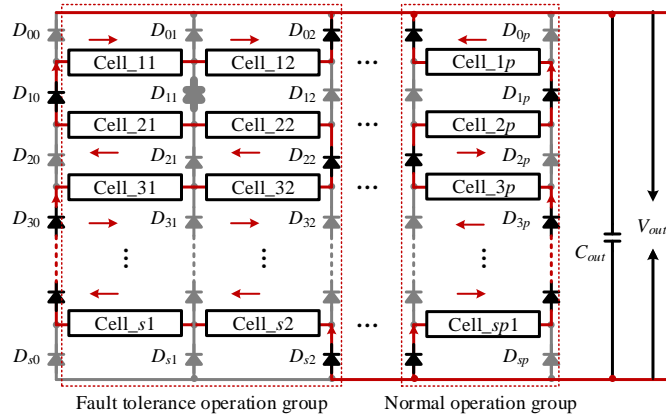
(b)

Figure 3.11 Fault tolerance when diode D_{11} is open-circuited: (a) working mode 1; (b) working mode 2.

3.5   Simulation Verification and Comparison Results

3.5.1   Simulation Results

To illustrate the functionality of the proposed power converter, a PSIM simulation model consisting of 3 groups×4 rows×5 columns with 2 redundant columns is built, which is similar to the model shown in Fig 3.6. The cells in columns 1~3 are active, while those in columns 4~5 are inactive. Table 3.1 presents the initial values for the simulation. It is noted that to verify the auto-balanced current characteristic, the leakage inductances of cells in column 1 are set as 70, 75, 80, 85 μH.

The steady-state waveforms of the converter with the same input power from WTGs are shown in Fig 3.12. All groups work under the column interleaved strategy and the voltages of the adjacent cells in the same column have opposite polarities. Meanwhile,

the currents of cells with diverse leakage inductances in column 1 are almost equal. The voltage stress of power switches is ¼ of the output voltage, and all diodes have the voltage and current rating as low as ¼ or ½ of the output voltage and current, respectively.

Table 3.1 Initial values of simulation.

System Parameters	Values	Components	Values
Input Voltage	650 V	Turns ratio 1:1:n	1:1:2
Output Voltage	6400 V	Leakage inductance	80 µH
Switching Frequency	5 kHz	Input inductance	5 mH
Output Power	40 kW	Clamp capacitor	20 µF
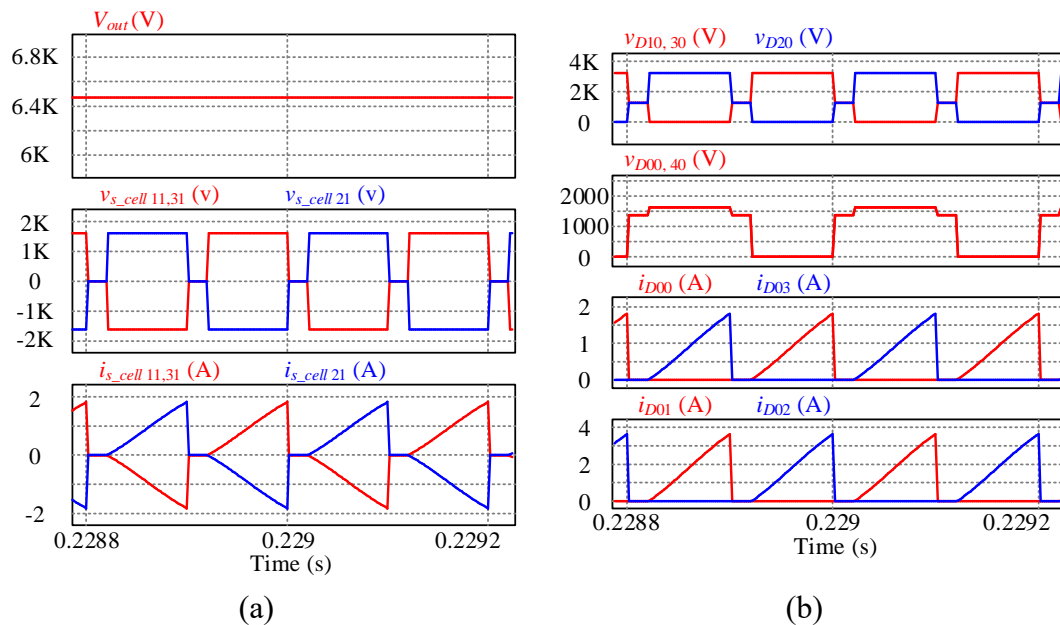
Figure 3.12 Steady state waveforms for cells and diode: (a) voltage/current of basic cells; (b) voltage/current of diodes.

For Fig 3.13, every group has different numbers of rows. Only one row operates in Group 1; in Group 2, there are two rows; Group 3 has four rows. The duty-cycle D of cells in each group is regulated to obtain the same terminal voltage, and the voltages of cells are shown in Fig 3.13 as: $V_{s\_cell\ 1-11}=2\times V_{s\_cell\ 2-11}=4\times V_{s\_cell\ 3-11}=V_{out}$. The peak current values of different columns are almost equal so that the duty-cycle control presented in Eq.(3.16) is verified.
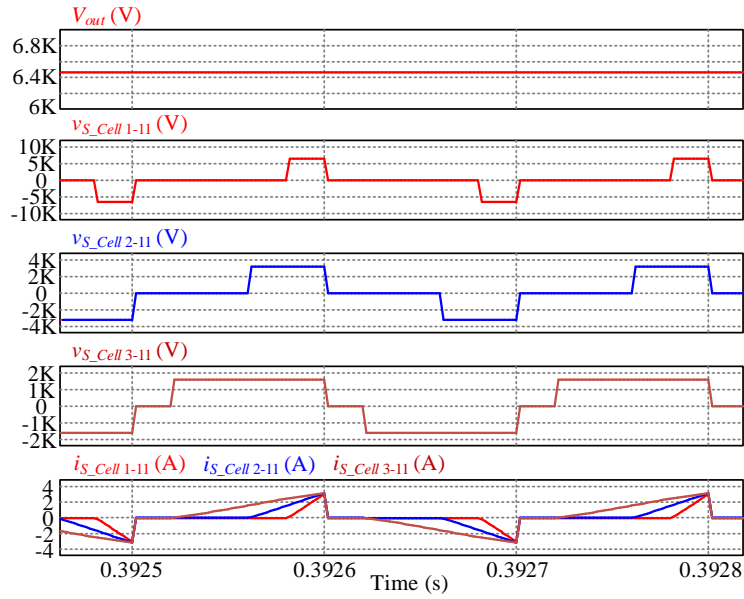
Figure 3.13 Waveforms of cells when Groups 1~3 have different output power.

Fig 3.14 shows the voltages of diodes in Group 1~2. The voltage of diodes in Group 3 has the same waveforms as those presented in Fig 3.12. It can be found that the voltage value is increased as the number of idle rows increases.
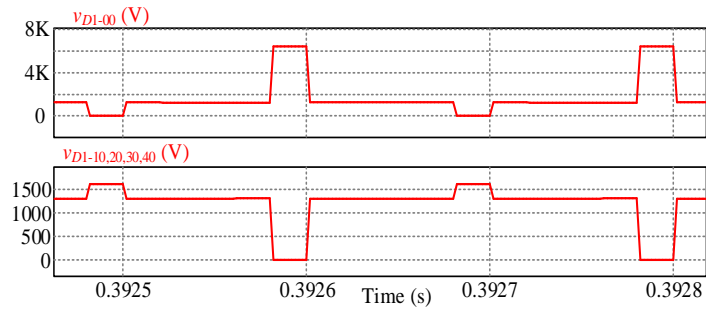
(a)
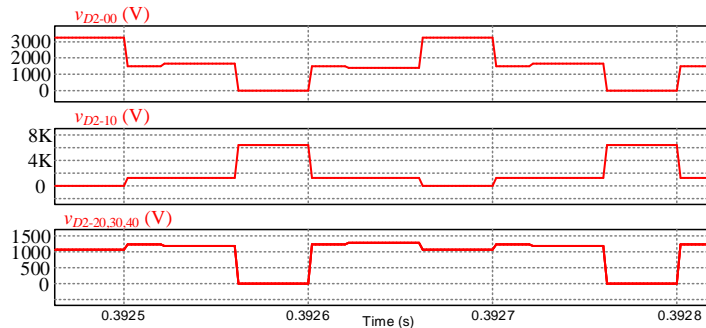
(b)

Figure 3.14 Voltages of diodes in each Group when Groups 1~3 have different output power: (a) voltages of diodes in Group 1; (b) voltages of diodes in Group 2.

As illustrated in Fig 3.15, before turning on switches S_1 or S_{C1}, the drain-to-source current flows through the parasitic diode of the switch to achieve ZVS operation. Similarly, the switches S_2 and S_{C2} can also obtain soft-switching. Therefore, the switching loss is significantly reduced.
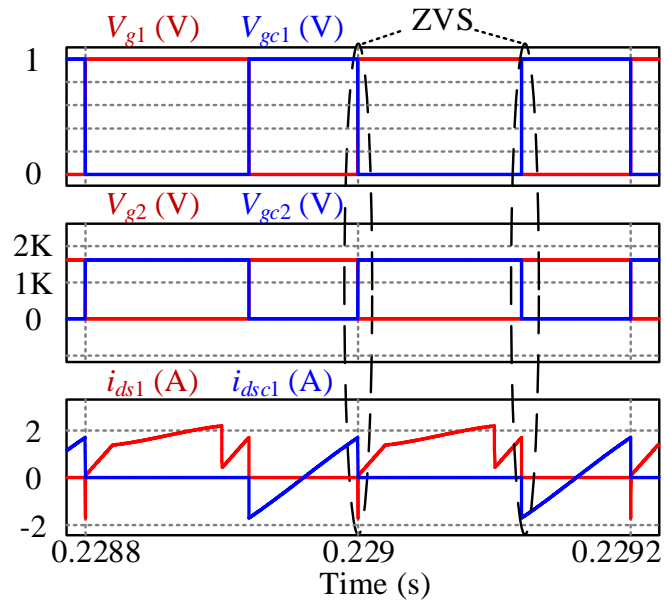
Figure 3.15 ZVS of main switches and clamping switches.

Fig 3.16 (a) shows the fault tolerance operation with redundancy. At 0.07s, fault cells 1~2 are idle, and the redundant columns 4~5 start to work to guarantee the normal operation. Fig 3.16 (b) and (c) present the fault tolerance without redundancy, where only columns 1~3 are active. In Fig 3.16 (b), when the diode D_{11} is short-circuited, the cells in rows 1~2 are blocked. The voltages of cells in row 3~4 are doubled to achieve the same terminal voltage. The diode D_{11} is open in Fig 3.16 (c). The faulty group consisting of columns 1~2 works in the series interleaved mode by changing the polarities of cells. Moreover, the voltages of cells in the faulty group are reduced to half of that in the normal operation group to obtain the same output voltage.
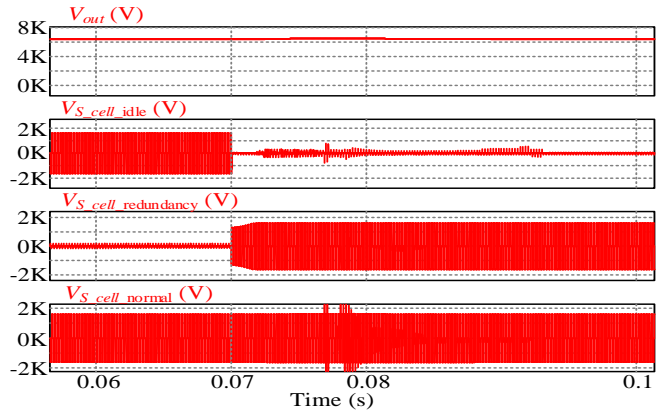
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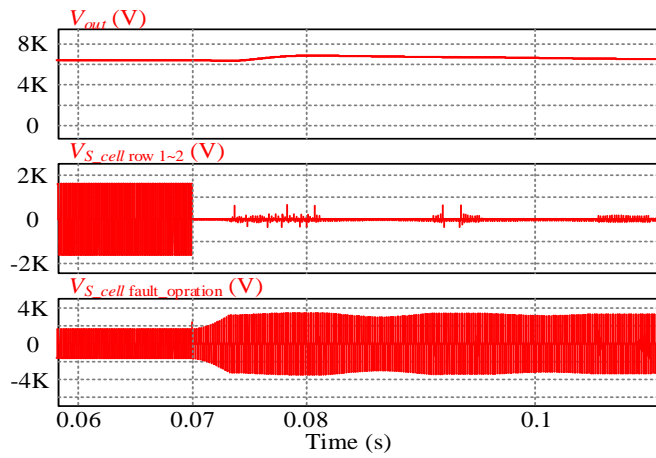
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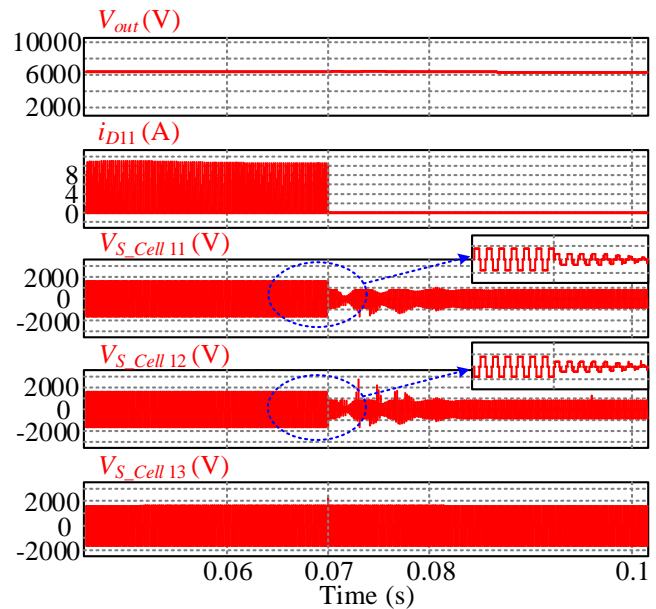
(c)

Figure 3.16 Fault tolerance operation: (a) with redundancy; (b) SCF of D_{11}; (c) OCF of D_{11}.

3.5.2 Comparison Results

Table 3.2 shows a performance comparison among several works of literature, where N is the number of SMs or power cells; n is the turns ratio of transformers. MMCs use several HB or FB SMs to increase their voltage conversion ratios, which have higher switching loss due to hard-switching [121]. The selection of operation frequency as 1 kHz aims to reduce the switching loss and the passive components volume. However, the component size is still large compared with the 5 kHz used in multi-module converters. To reduce switching loss, the LLC resonant tank is installed to achieve ZVS of switches [120]. Hence, the switching frequency is increased to 4 kHz to reduce the components size [120]. Due to the installation of HB/FB SMs, the voltage step-up ratio of MMCs only related to the number of SMs, while multi-module converters can achieve a higher voltage step-up ratio since they have two degree of freedom to enlarge the voltage gain. Both the cells number and the voltage gain of SMs could control the voltage step-up conversion ratios of multi-module converters. Therefore, to achieve the same voltage conversion ratio, multi-module converters require fewer components. As for multi-module converters, hard-switching of switches induces a high switching loss due to the installation of flyback-forward converters as SMs [106]. Furthermore, the implantation of CFPP converters can achieve currents auto-balancing of different SMs, which reduces the control complexity.

Table 3.2 Comparison of the proposed and other converters applied in HVDC transmission.

	MMCs		Multi-module Converters	
	[121]	[120]	[106]	Proposed
Soft-switching	✘	✓	✘	✓
Conversion Ratio	$\propto N, n$	$\propto N$	$\propto N, \dfrac{1}{1-D}, n$	$\propto N, \dfrac{1}{1-D}, \dfrac{n}{2}$
Switching Frequency	1 kHz	4 kHz	5 kHz	5 kHz
Control Among SMs	Complex	Complex	Complex	Current Auto-balance

3.6   Summary

A multi-port high voltage gain modular DC/DC power converter applied in offshore wind farms is proposed in this chapter. Thanks to the modularity, the high output voltage and power is achieved by adding power cells. With the independent operation of each port and high control flexibility, the converter can collect power from multi-sources without bus cable. Additionally, the CFPP cells reduce the switching loss and control complexity.

The performances of MMCs with galvanic isolation, resonant MMCs, multi-module converter with flyback-forwarding cells and CFPP cells are compared. The proposed one appears to be more efficient and reliable, including soft- switching, high conversion ratio, small volume and low control complexity.

The simulation results verify the advantages of the proposed converter as soft-switching of all power switches, flexible control, and improved fault tolerance operation.

Chapter 4. MODULAR MULTI-PORT ULTRA-HIGH POWER LEVEL POWER CONVERTER INTEGRATED WITH ENERGY STORAGE FOR HVDC TRANSMISSION

ES as batteries and fuel cells are widely used in RESs systems to compensate for the generation fluctuations of RESs. Current multi-port bidirectional converters (MPBCs) that integrate RES and ES are mainly applied for EV, and PV-battery systems, whose maximum output power and voltage can only reach up to 4 kW and 600 V [129-133].

This chapter presents another multi-module converter, which uses MPBCs as SMs in the matrix configuration to meet the high power and ultra-high voltage level of HVDC transmission of RESs. The proposed TPC is designed as the SMs of the multi-module converter. Hence, the output power and voltage level can be increased easily by adding the number of SMs. Compared with the CFPP converter in the last chapter, the proposed TPC uses the four-winding-transformer to transfer power among PV panels, batteries, and load to realise the bidirectional power flow of batteries. The leakage inductance of the transformer charges and discharges the parasitic capacitance of active switches before they are turned on/off to obtain the soft-switching operation of switches. Thanks to the soft-switching of switches, the switching loss is reduced, and a high operation frequency 10 kHz is used to minimise components size. Simulations results of the converter verify the feasibility of the proposed SM and multi-module converter.

4.1 Introduction

Solar and wind power are the dominant RESs nowadays, whose average levelised cost of electricity (LCOE) falls within the fossil fuel-fired cost range of USD 0.05~0.17/kWh [134]. For example, the global weighted average LCOE of utility-scale solar power has decreased by 73% since 2010, to USD 0.10/kWh for new projects commissioned in 2017 [1]. However, the variability of RESs caused by the weather fluctuation is a challenge to connecting RESs with grid-tied systems. For example, passing clouds can affect up to 70% of daytime solar capacity, and 100% of wind capacity is reduced in calm days for individual generation assets, which have a

negative impact on the stability and power quality of electric power systems [135]. To address this issue, ES systems with the ability to store and dispatch electricity are integrated to compensate the generation fluctuations of RESs. The battery has become a candidate of grid-tied large-scale RESs power plants with its increasing deployable capability and reducing cost [136]. Additionally, the HVDC transmission method is preferred for large-scale renewable power plants that have a large output power scale and long-distance transmission because HVDC transmission has the advantages of low cost and high transfer efficiency [5, 6, 137]. Therefore, RESs such as solar and wind power are delivered to the unity grid through HVDC transmission in conjunction with ES systems to improve the reliability and efficiency of the overall system.

Three dominant configurations illustrated in Fig 4.1 show the integration of ES system with DC transmission system, where the red arrow indicates the power flow direction. As illustrated in Fig 4.1 (a) and (b), the ES system, which is a battery, is either connected to DC link through an additional DC/DC converter [138, 139] or integrated into the grid side using a separate inverter [140, 141]. Both configurations use a large number of components. Additionally, for the configuration illustrated in Fig 4.1 (b), due to the direct connection with the unity grid, extra circuit protection for battery port is demanded and the power rate of the inverter linked with the ES system is as high as that of the inverter connected with the grid, which leads to high cost. Additionally, compared with the topology shown in Fig 4.1 (a), the voltage and size of batteries in the configurations illustrated in Fig 4.1 (b) are determined by the voltage of DC bus, which is at a high level. Thanks to the application of multi-port converters (MPCs), the configuration in Fig 4.1 (c) solves the problems caused by the configurations illustrated in Fig 4.1 (a)-(b). Additionally, it has a fewer component count, fewer conversion stages, higher compactness and improved reliability due to power stage integration [142, 143].
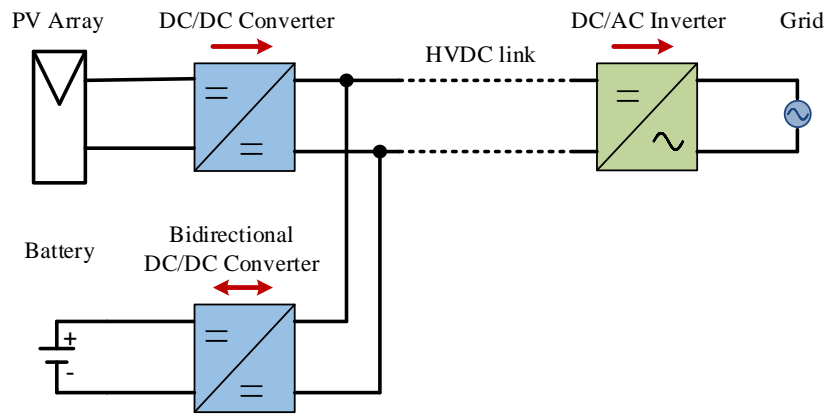
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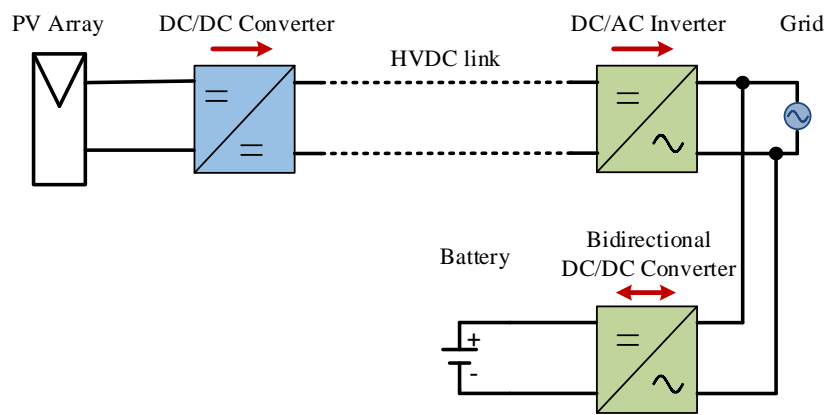
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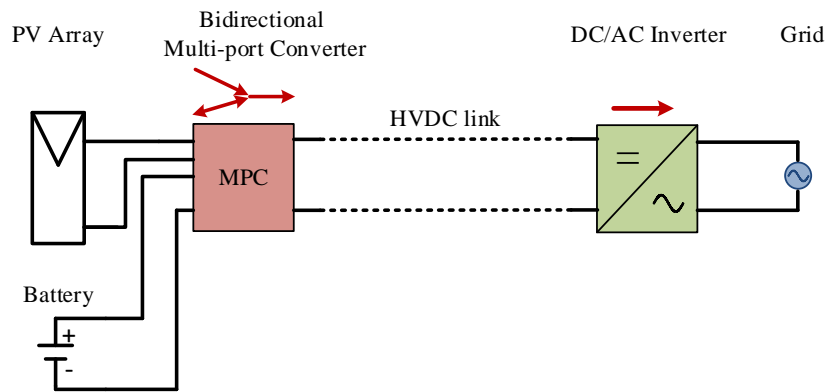
(c)

Figure 4.1 Main configurations for integrating ES system and HVDC system: (a) dual-converter architecture; (b) dual-inverter architecture; (c) multi-port converter architecture.

The MPC design is a technical challenge to meet the HVDC requirement due to the required high DC voltage, e.g. ±800 kV [144] and the large power scale, which requires numerous battery cells to be connected in series. Battery management systems

(BMS) are necessary to monitor and balance the state of charge of each battery cell for safe operation. To design an MPC suitable for the grid-tied system, isolated, partially-isolated and non-isolated MPCs are extensively studied.

The representative isolated MPCs install two transformers or one tri-winding transformer to extend the conventional DAB converter to a TPC, which can achieve high DC/DC voltage conversion ratios [145-147]. However, the voltage stress on their semiconductor components is high. The active switches connected with the output port could be eliminated by series-connecting the secondary sides of two transformers, while the converters are only suitable for unidirectional power flow [132]. Non-isolated MPCs use modules in parallel-connection to obtain the multi-port configurations that are mainly applied for the stand-alone systems such as EVs [148-150], which reduce the switch count and volume due to the elimination of bulky transformers. However, for safety consideration, galvanic isolation is preferred for the grid-tied system. For partially-isolated MPCs, the switch count is reduced by sharing the switches of DAB converters, FB converters, HB converters or phase-shift converters [151-153]. An interleaved HB three-port converter uses only two switches to achieve free power flows among the RES-ES-output loop [154]. Nevertheless, its output voltage has been determined at the design stage according to the characteristics of the components such as capacitors, inductors and transformers, which causes low control flexibility.

Furthermore, for MMC [155, 156], high voltage and large size battery can be distributed into several relatively smaller ones by connecting them with SMs. However, the battery cells are series connected to achieve a high voltage level, which requires BMS for them, resulting in high complexity [157]. With the modular structure of a multi-module converter [158, 159], high voltage and output power are obtained by increasing the number of SMs. By decentralizing the batteries cells into each SMs, the distributed control of battery cells is achieved, and the BMS among isolated battery modules can be eliminated.

In this chapter, a novel bi-directional MPC is developed and adopted as the SM based on the multi-module converter [158]. The desired advantages such as power stage integration, low voltage stress of semiconductor components, expandable output voltage and power remain. Additionally, the power flow control of PV-battery-output

is more flexible because battery cells are controlled individually by each power cells with phase-shift (PS) as well as pulse width modulation (PWM) control. Moreover, the fault tolerant capability is improved to increase the reliability.

The chapter is organized as follows: the basic cell is analysed in Section 4.2; the scalable topology design, and operation are discussed in Section 4.3; then, Section 4.4 gives the fault tolerance strategy; Section 4.5 presents the simulation results to verify the operation of the converter; finally, Section 4.6 draws the summary of the main contributions of this chapter.

4.2   Analysis of the Basic Cell

4.2.1   Design of the Basic Cell

The topology of the basic power cell with PV panel is shown in Fig 4.2, consisting of one CFPP circuit, one battery side circuit and a single-phase bridge rectifier linked through a transformer with four windings. The primary component in the CFPP circuit contains two main switches S_{M1}~S_{M2}, three clamp switches S_{C0}~S_{C1}, one clamp capacitor C_c, one input inductor L_1 and one input diode D_{in}. The primary circuit has the similar operating principles with the CFPP converter [158]. The battery side circuit is formed by two phase legs composing of switches S_1, S_4 and S_2, S_3 that charge and discharge the battery and the inductor L_2. The output is in series connection with the single-phase bridge rectifier consisting of four diodes D_1~D_4. The turns ratio of the transformer is N_{p1}:N_{p2}:N_{s1}:N_{s2}=1:1:1:n, and the leakage inductance for the output side is L_k.
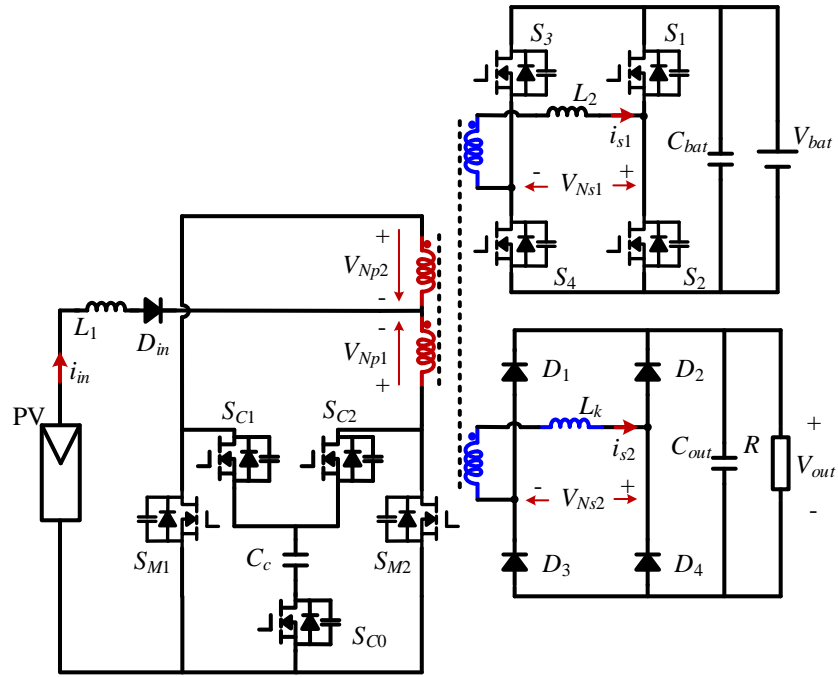
Figure 4.2 Topology of the basic cell.

4.2.2   Operation of the Basic cell with PV Source

The equivalent circuits of different operation modes and the steady-state waveforms for the basic cell with PV source are illustrated in Fig 4.3 and Fig 4.4. V_{gsM1}~V_{gsM2} are the control signals with the duty cycle D_p for the two main switches S_{M1}~S_{M2}, which have a 180° phase shift angle. V_{gsc1}~V_{gsc2} are the control signals for the two clamp switches S_{C1}~S_{C2}, which are complementary to V_{gsM1}~V_{gsM2}, respectively. V_{gs1}~V_{gs4} are the control signals for switches S_1~S_4, which are set as $V_{gs1}=V_{gs4}$, and $V_{gs2}=V_{gs3}$. V_{gs1} and V_{gs3} have the same duty cycle D_b. V_{dsM1}~V_{dsM2}, V_{dsc1}~V_{dsc2}, and V_{ds1}~V_{ds4} are the drain-source voltages of switches S_{M1}~S_{M2}, S_{C1}~S_{C2}, and S_1~S_4. When there are PV sources, the switch S_{C0} is on permanently and D_b=0.5. The PWM control for CFPP and the phase shift angle θ_1 between the V_{CFPP} and V_{FB} regulates the voltage level and power of the battery and output. To simplify the analysis, all switches and diodes are assumed to be identical, and the clamp capacitor is large enough so that the voltage ripple can be ignored.
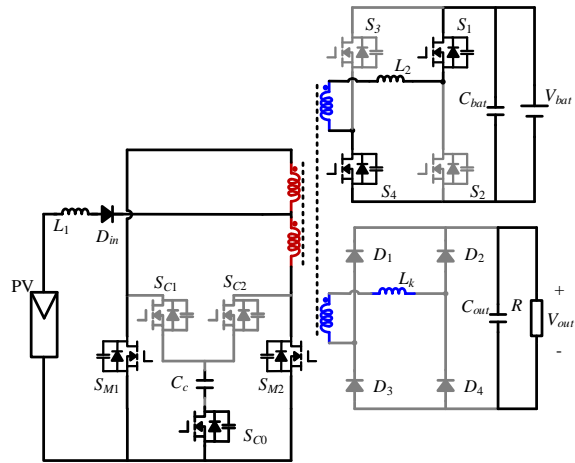
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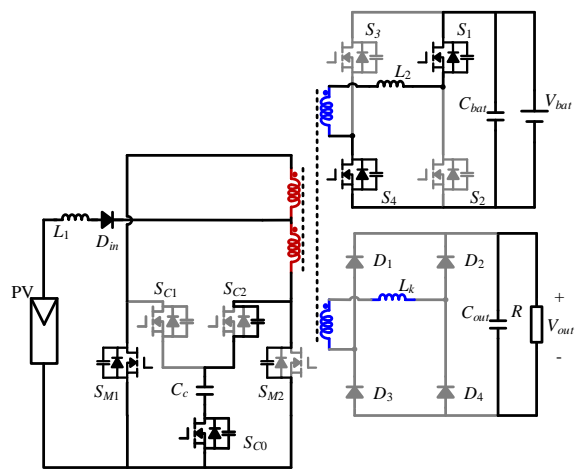
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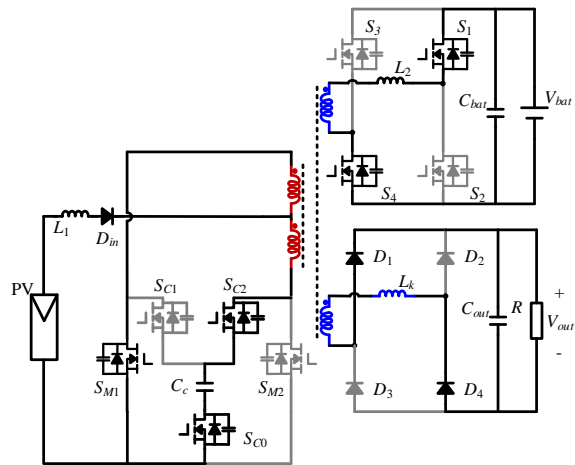
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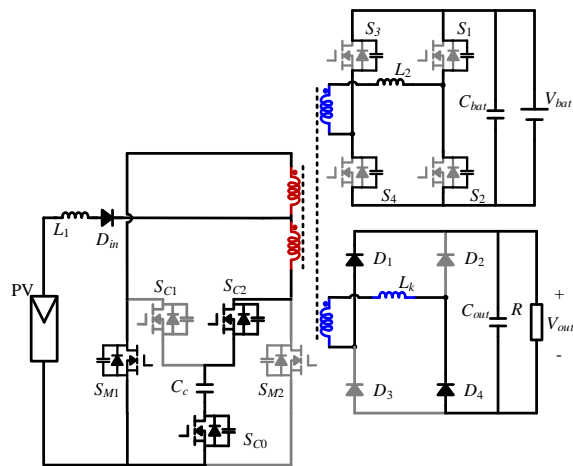
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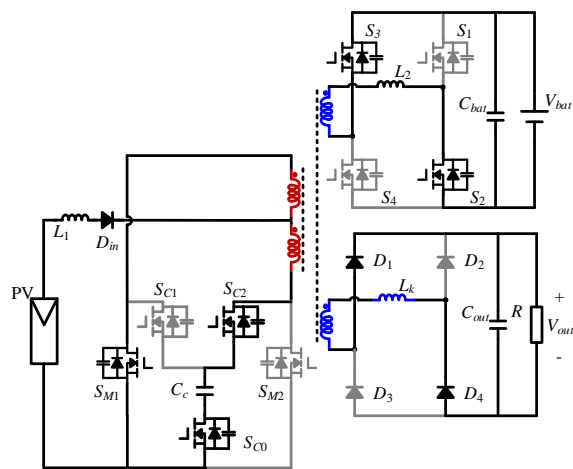
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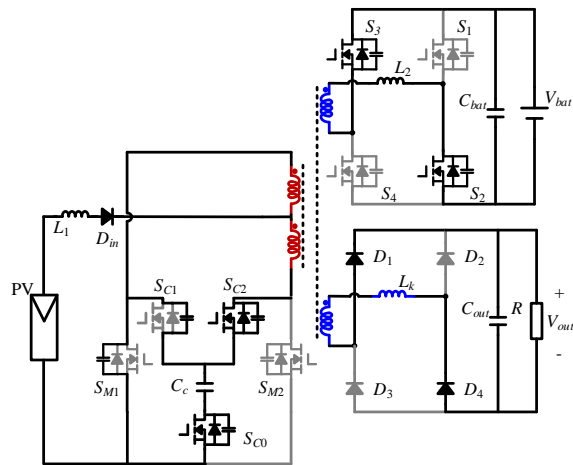
(f)

Figure 4.3 Equivalent circuits of operation modes with PV source: (a) Mode 1 (t_0-t_1); (b) Mode 2 (t_1-t_2); (c) Mode 3 (t_2-t_3); (d) Mode 4 (t_3-t_4); (e) Mode 5 (t_4-t_5); (f) Mode 6 (t_5-t_6).
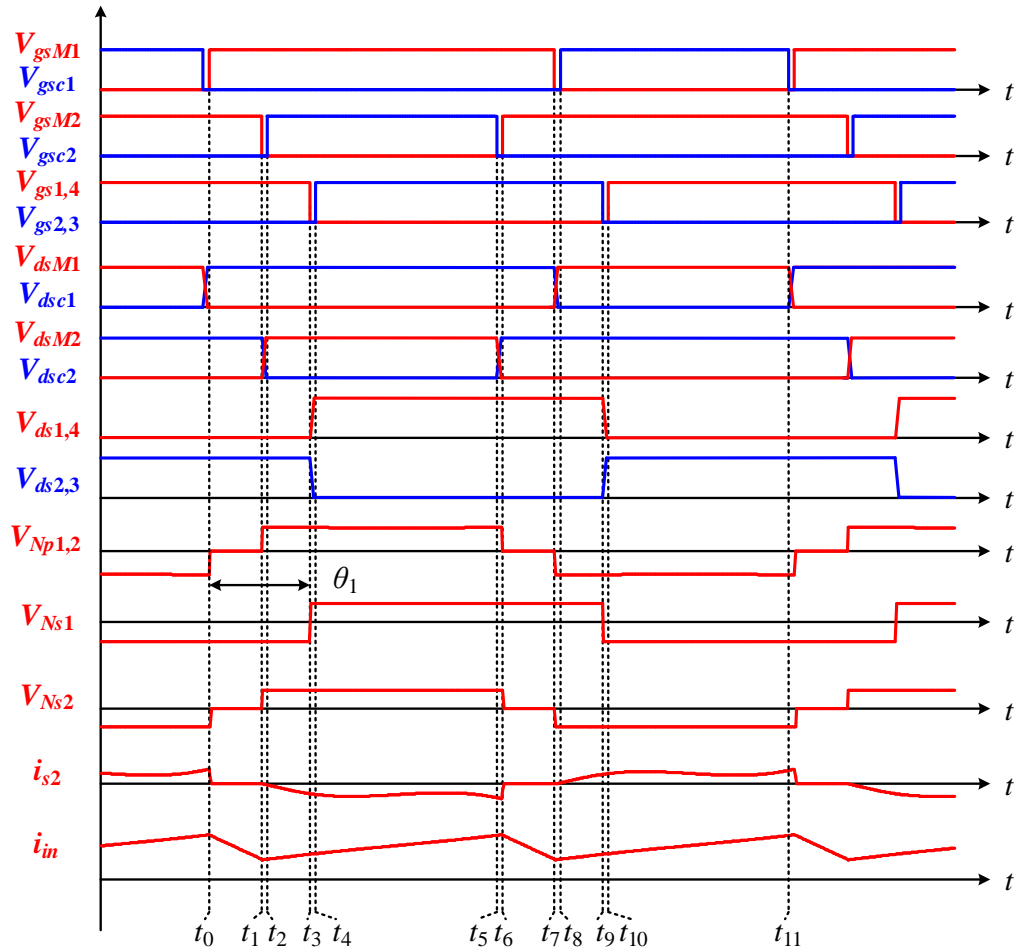
Figure 4.4 Operating waveforms of the basic cell with PV source.

In this example, the battery is charged. Only the operation of the basic cell during t_0-t_6 is introduced in this part because of the symmetrical operation.

Mode *1* (t_0-t_1): In this mode, the main switches S_{M1} and S_{M2} are on. The primary sides N_{p1}, N_{p2} are short-circuited. All the four diodes are reverse biased. At the same time, S_1 and S_4 are on. The voltage of the battery side N_{s1} is negative.

Mode *2* (t_1-t_2): At t_1, the main switch S_{M2} is turned off. The primary-preferred leakage inductance resonates with the parasitic capacitances of S_{M2} and S_{C2}. The voltage across S_{C2} drops to zero at t_3 so that ZVS of S_{C2} is obtained.

Mode *3* (t_2-t_3): At t_2, the clamping switch S_{C2} is turned on with zero voltage. The energy is transferred from the PV and input inductor L_1 to the output. The diodes D_1 and D_3 are forward biased, and the current i_s increases.

Mode *4* (t_3-t_4): At t_3, switches S_1 and S_4 are turned off. The voltage V_{FB} becomes positive. The inductor L_2 resonates with the parasitic capacitances of S_1-S_4. The voltage across S_2 and S_3 drops to zero at t_5 so that ZVS operation of S_2 and S_3 is obtained.

Mode *5* (t_4-t_5): At t_4, switches S_2 and S_3 are turned on with zero voltage. The power starts to be delivered into the FB circuit.

Mode *6* (t_5-t_6): At t_5, the clamp switch S_{C2} is turned off. The primary-preferred leakage inductance resonates with the parasitic capacitances of S_{M2} and S_{C2}. The voltage across S_{M2} drops to zero at t_6 so that zero voltage turn-on of S_{M2} is obtained.

Altering the duty cycle D_p, the three-level voltage waveforms $V_{Np1,2}$ and V_{Ns2} are generated in the primary side and the rectifier bridge. According to the flux balance of the input inductor L_1, the clamp voltage can be derived as:

$$V_{in}(D_p - 0.5) + (V_{in} - 0.5V_{Cc})(1 - D_p) = 0 \qquad (4.1)$$

$$V_{Cc} = \frac{V_{in}}{(1 - D_p)} \qquad (4.2)$$

The output voltage can be determined as:

$$\frac{V_{out}}{n} - \frac{V_{out}D_p}{n} - V_{in} + V_{in}D_p - V_{in}D_p + \frac{V_{in}}{2} = 0 \qquad (4.3)$$

$$V_{out} = \frac{n}{2}\frac{V_{in}}{(1 - D_p)} \qquad (4.4)$$

Additionally, based on the average power flow calculation of bidirectional power converters [160, 161], the power transfer between P_{in} and P_{bat} with the switching frequency f_s is obtained in Eq.(4.5). A specific phase shift θ_1 controls the power delivered to the battery. When $0 < \theta_1 < \pi$, the power can be transferred from the PV to battery and vice versa. Additionally, the power transfer between P_{in} and P_{bat} with the switching frequency f_s is obtained as:

$$P_{in \leftrightarrow bat} = \frac{1}{T}\int_0^T v_p(t)i_L(t) = \frac{V_{in}V_{bat}}{\omega L_2}\left(2(1 - D_p)\theta_1 - \frac{\theta_1^2}{\pi} - 2(1 - D_p)^2\pi + (1 - D_p)\pi\right)$$
$$D_p \geq 0.5$$

$$(4.5)$$

Where $\omega=2\pi f_s$.

4.2.3 Operation of the Basic Cell without PV Source

When there is no PV source, the equivalent circuits of different modes and the steady-state waveforms for the basic cell are illustrated in Fig 4.5 and Fig 4.6. When no power is generated from the PV panel, the primary circuits are blocked to reduce the conduction loss. Additionally, V_{gs1} and V_{gs3} have a 180° phase shift angle with the duty cycle $D_b \leq 0.5$. V_{gs2}, V_{gs4} are complementary to V_{gs1}, V_{gs3} respectively. Because the operation is symmetrical, only the operation during t_0-t_5 is introduced in this part.

(a)

(b)
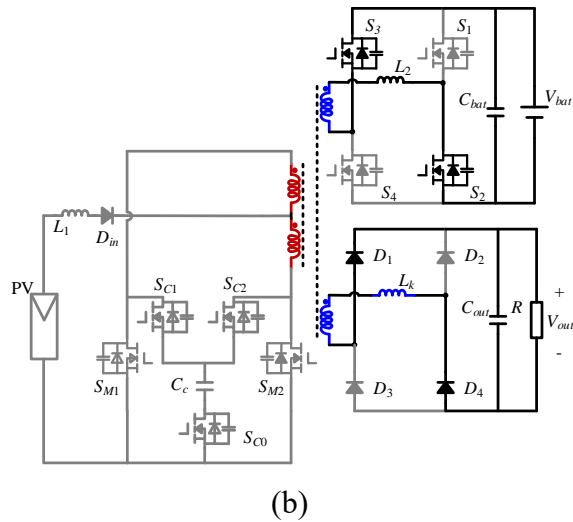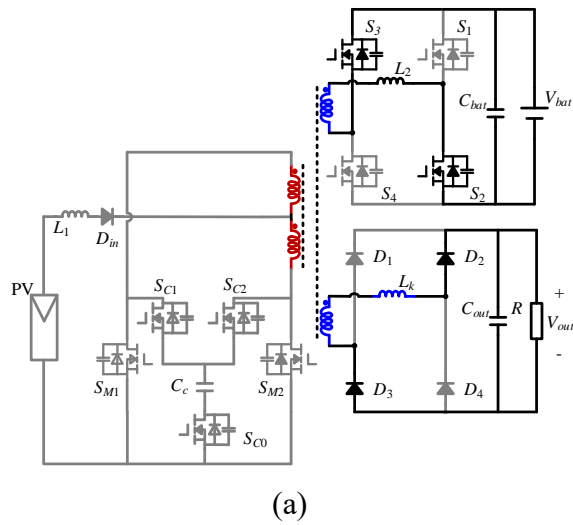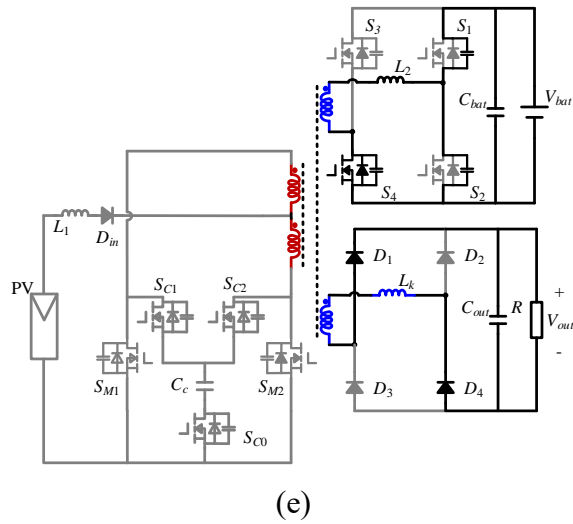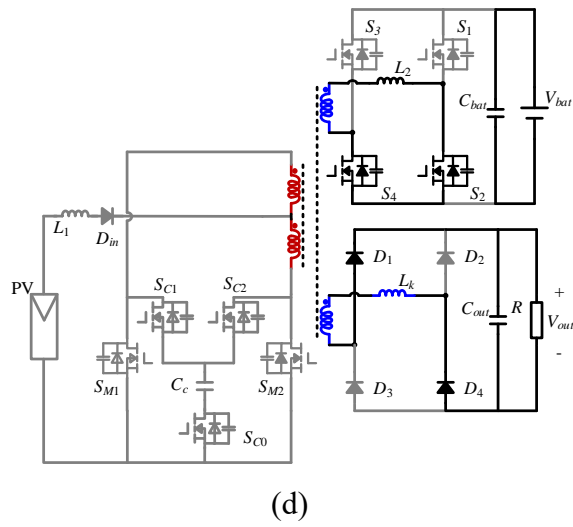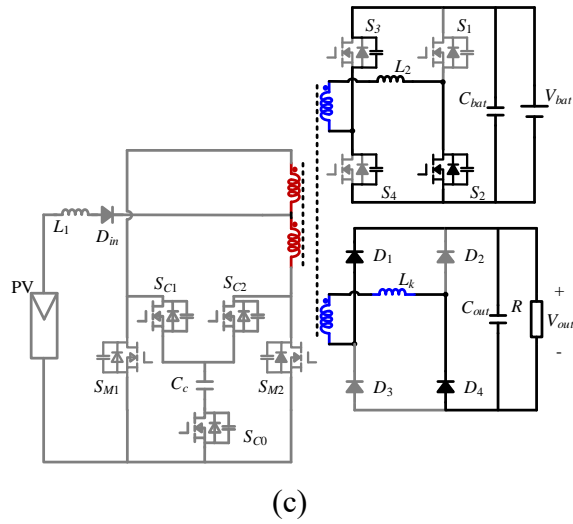
Figure 4.5 Equivalent circuits of operation modes without PV source: (a) Mode 1 (t_0-t_1); (b) Mode 2 (t_1-t_2); (c) Mode 3 (t_2-t_3); (d) Mode 4 (t_3-t_4); (e) Mode 5 (t_4-t_5).
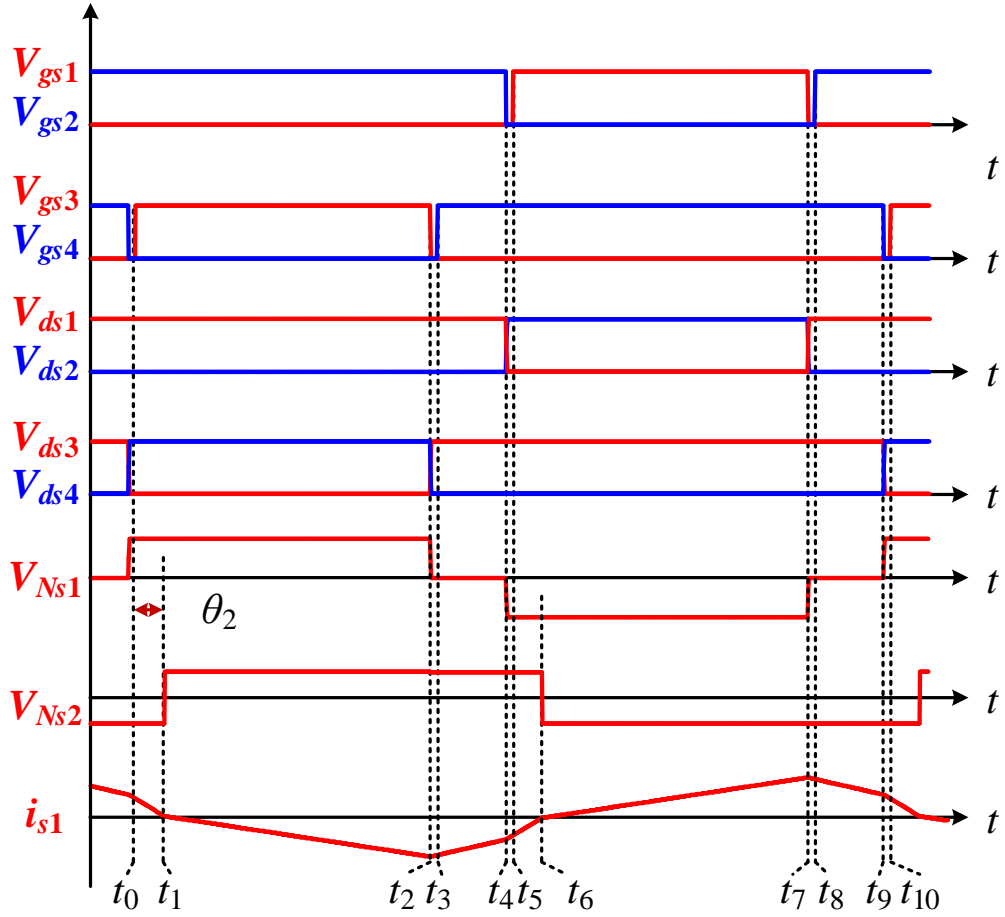
Figure 4.6 Operating waveform of the basic cell.

Mode *1* (t_0-t_1): At t_0, switch S_3 is turned on. There is a phase shift θ_2 between V_{Ns1} and V_{Ns2}, which is dependent on the inductance L_2, L_k and output load. The battery-side current i_{s1} recovers to zero at t_1. The current i_{s1} as a function of $\beta=\omega t$ is derived as:

$$i(\beta) = (\frac{V_{bat}+V_o^{'}}{\omega L_{bat}^{'}})\beta + i(0) \tag{4.6}$$

Where $V^{'}_o$ is the battery-side referred output voltage, which equals to V_{out}/n; L'_{bat} is the battery-side referred inductance and $L'_{bat}=L_2+L_{out}/n^2$.

Mode *2* (t_1-t_2): At t_2, i_{s1} starts to decrease. The voltage of V_{Ns2} becomes positive. In this mode, i_{s1} is determined as:

$$i(\beta) = (\frac{V_{bat}-V_o^{'}}{\omega L_{bat}^{'}})(\beta - \theta_2) + i(\theta_2) \tag{4.7}$$

Page | 73

Mode 3 (t_2-t_3): At t_2, switch S_3 is turned off. The voltage V_{Ns1} drops to zero. The battery-side referred inductance resonates with the parasitic capacitances of switches S_3 and S_4. The voltage across the parasitic capacitor of S_4 is discharged to zero. Therefore, ZVS of S_4 is obtained at t_3.

Mode *4* (t_3-t_4): At t_4, switch S_4 is turned on with zero voltage. The current i_{s1} starts to increase as shown in Eq.(4.8).

$$i(\beta) = (\frac{-V_o^{'}}{\omega L_{bat}^{'}})(\beta - (D_b + t_{ds}) \cdot 2\pi) + i((D_b + t_{ds}) \cdot 2\pi) \qquad (4.8)$$

Where t_{ds} is the dead zone between turn on and turn off operation of switches S_1~S_2 and S_3~S_4.

Mode *5* (t_4-t_5): At t_4, switch S_2 is turned off. The voltage V_{Ns1} drops to negative. The battery-side referred inductance resonates with the parasitic capacitances of switches S_1 and S_2. The voltage across the parasitic capacitor of S_1 is discharged to zero so that ZVS operation of S_1 can be achieved at t_5.

Because the dead time t_{ds} is relatively short, modes 3, 5 can be neglected in the calculation and the phase shift between voltage V_{Ns1} and V_{Ns2} defined as θ_2. Therefore, Eq.(4.9) is derived according to Eq.(4.8).

$$i(\beta) = (\frac{-V_o^{'}}{\omega L_{bat}^{'}})(\beta - D_b \cdot 2\pi) + i(D_b \cdot 2\pi) \qquad (4.9)$$

At t_5, $i(t_5) = -i(t_0)$ since it is the end of half cycle. Additionally, $i(\theta_2)=0$. Then, θ_2 can be derived as shown in Eq.(4.10).

$$\theta_2 = \frac{1}{2}(D_b \cdot \pi - d\pi) \qquad (4.10)$$

Where d is defined as $V_o^{'}/V_{bat}$. The power transfer is obtained as:

$$P_{bat \to out} = \frac{1}{T}\int_0^T v_{bat}(t)i_{s1}(t) = = \frac{V_{bat}V_{out}}{4\omega L_{bat}^{'} \cdot n}(2D_b \cdot \pi - \pi d^2 - D_b^2 \cdot \pi) \qquad (4.11)$$

4.3 Analysis of the Proposed Multi-module Converter

As shown in Fig 4.7, the proposed scalable multi-port bidirectional topology is composed of the basic cell illustrated in Fig 4.2. The primary sides are in parallel connection with the PV source V_{in}. Each battery cell is connected to a power cell for individual control. Additionally, the output side windings N_{s2} of transformers are connected in an $s \times p$ matrix configuration, where s is the row number, and p is the column number. The matrix configuration of the converter can be easily expanded to achieve high output voltage and power rating by increasing its row number and column number, respectively. Therefore, the converter can satisfy the applications demanding high voltage step-up ratios and high power scales.

(a)

(b)
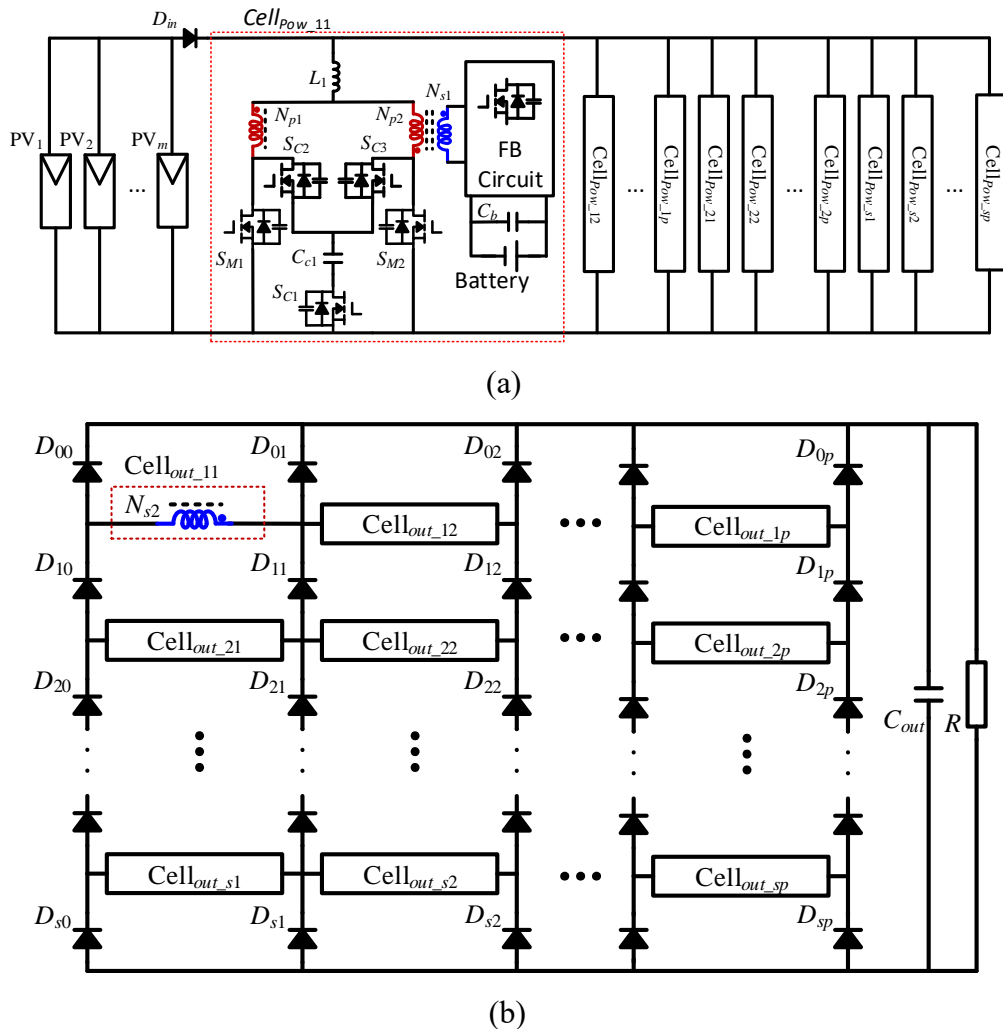
Figure 4.7 Topology of the proposed converter with s rows and p columns: (a) primary circuits with ES system; (b) secondary circuits connecting.

4.3.1 Voltage Gain of the Scalable Topology

The cells of scalable topology have the similar operations with those for one basic cell except that the drive signals of switches in adjacent cells have a 180° phase shift. For example, cells 12, 21, 23, and 32 have the same drive signals, whose phases are shifted by 180° from cell 22. Hence, the polarities of output voltages V_{s2} and currents i_{s2} for adjacent cells are opposite. Then, the column interleaved working strategy of matrix topology is shown in Fig 4.8.

(a)

(b)
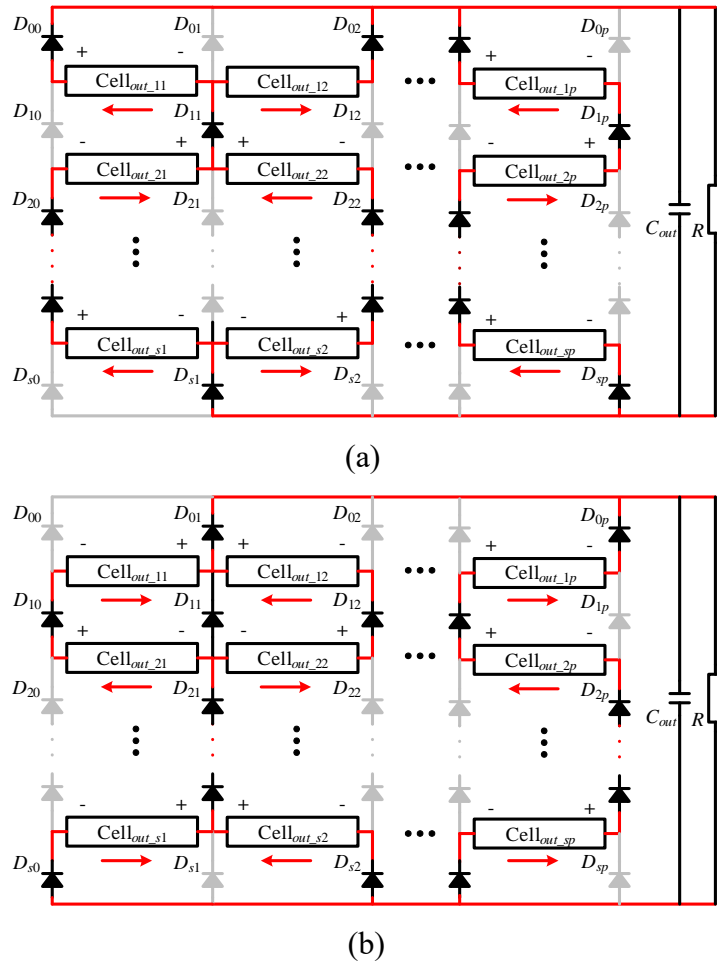
Figure 4.8 Equivalent secondary circuits of the $s \times p$ topology in the column interleaved strategy: (a) column interleaved mode 1; (b) column interleaved mode 2.

The output voltage is the sum of the voltages V_{s2} of cells in the same column, and the output current is the sum of the currents i_{s2} in every column, which are shown in Eq.(4.12) with the assumption that every cell has the identical output voltage and current. The higher output voltage and power rating can be easily obtained by increasing the row and column numbers of the matrix topology.

$$\begin{cases} V_{o,s \times p} = s \times V_{s2} = \dfrac{s \times n}{2(1-D_p)} V_{in} \\ I_{o,s \times p} = p \times I_{s2} \end{cases} \tag{4.12}$$

4.3.2 Voltage/Current Rating of Semiconductor Components

Due to the parallel connection of transformer windings N_{p1} and N_{p2}, all switches have the same low voltage and current ratings with those of the scalable topology. The voltage ratings of switches in power cells are derived as shown in Eq.(4.13).

$$\begin{cases} V_{ds\_Np} = V_{Cc} = \dfrac{V_{in}}{1-D_p} \\ V_{ds\_Ns1} = V_{bat} \end{cases} \tag{4.13}$$

The current rating of diodes in columns 0 and p has half the value of I_{s2}, which is the average output current of the output side N_{s2}. Nevertheless, the diodes in columns 1 to $p-1$ have twice the rated current higher than that of other diodes, since they are connected with two power cells. The sum of average currents of diodes in all columns equals the output current as shown in Eq.(4.14), and the current rating of diodes is derived in Eq.(4.15). Similarly, the voltage stress of diodes is obtained in Eq.(4.16). For diodes in rows 1 to $s-1$, the voltage stress has twice the value larger than that of the diodes in rows 0 and s.

$$\sum_{j=0}^{p} I(D_{ij}) = I_{o,sp} \tag{4.14}$$

$$I(D_{ij}) = \frac{1}{2} I_{s2} = \begin{cases} \dfrac{1}{2p} I_{o,s \times p} & j = 0, p \\ \dfrac{1}{p} I_{o,s \times p} & j = 1, 2, \cdots, (p-1) \end{cases} \tag{4.15}$$

$$V(D_{ij}) = \begin{cases} \dfrac{n}{2(1-D_p)} V_{in} & i = 0, s \\ \dfrac{n}{(1-D_p)} V_{in} & i = 1, 2, \cdots, (s-1) \end{cases} \tag{4.16}$$

The maximum current and voltage rating of diodes in the $s \times p$ topology are only twice larger than that of an individual cell, which is much lower than the average

output voltage $V_{o,s \times p}$ and current $I_{o,s \times p}$. Therefore, the low voltage/current rating semiconductor components such as switches and diodes can be used to achieve a high step-up ratio and output power.

4.3.3 Control Scheme

Since the number of working rows determines the value of output voltage and that of working columns determines the output current, the variable output power can be obtained. As shown in Fig 4.9, power control is achieved by controlling the working columns according to the input current and battery charged/discharged power value. The voltage control is mandatory to meet the system operation requirements by the PS-PWM control of switches in the circuits at the primary and battery sides.
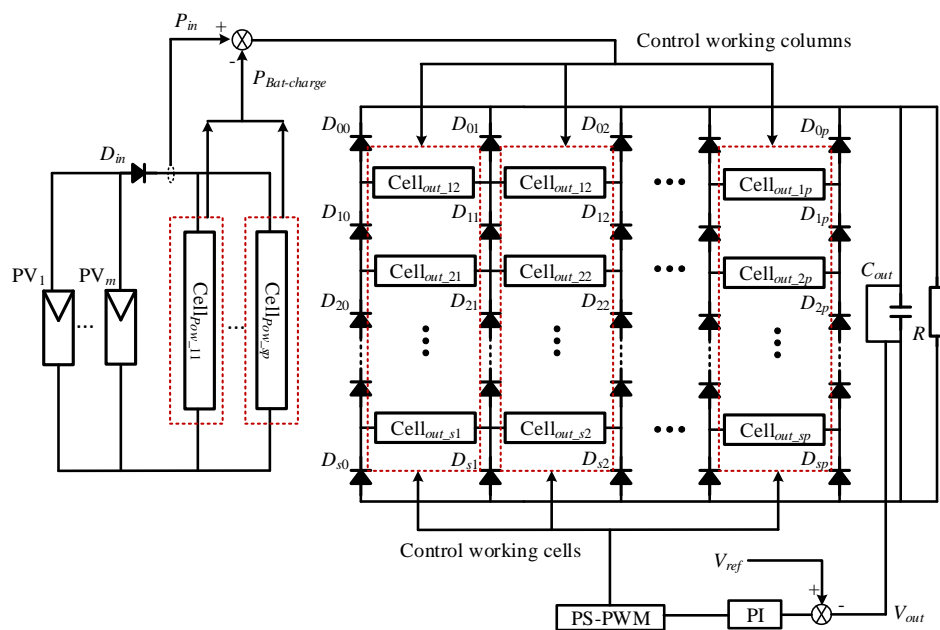
Figure 4.9 Control scheme of the *s×p* topology.

4.4 Fault Tolerance

4.4.1 Redundancy Fault Tolerance

For power electronics systems, semiconductor components are vulnerable devices [32]. With unexpectedly damaged devices, the whole system has to stop and wait for maintenance, resulting in high cost and loss. Fig 4.10 shows the fault tolerant operation with redundancy. In normal operation, the redundant cells in columns *p*1 and *p*2 are inactive, and the converter is working with the column interleaved strategy as shown

in Fig 4.8. When there are failed cells, the converter can maintain normal operation by replacing the faulty column with one redundant column. For the damaged diodes in columns 1 to $p-1$, two redundant columns are necessary. For example, when cell 11 fails, the column in the red dotted rectangle is replaced by the redundancy in another red dotted box. For the defective diode D_{11}, columns 1 and 2 in the blue dotted box are idle, and the redundant columns $p1$ and $p2$ are applied.
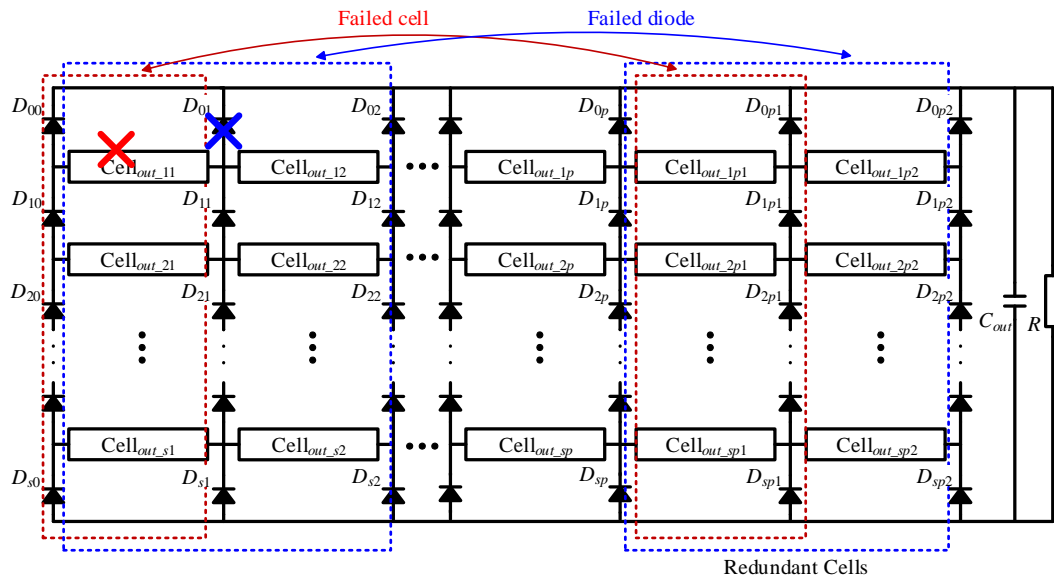
Figure 4.10 Fault tolerance with redundancy.

4.4.2 Fault Tolerance of Short-circuited Diodes and Failed SMs

Additionally, owing to the matrix configuration and flexible control, the converter can still obtain fault tolerance of cells and diodes without redundancy. When there are short-circuited cells or diodes, the converter can still work as represented in Fig 4.11 (a) and (b). When diode D_{11} is short-circuited, its connecting rows 1 and 2 are inactive to block the damaged devices. The other cells still operate with the column interleaved strategy and the duty cycle D_p of them is increased to obtain the normal output voltage with fewer working rows.
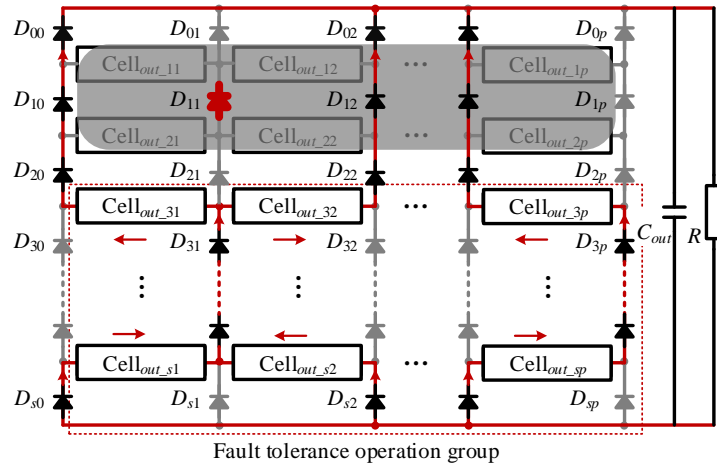
(a)
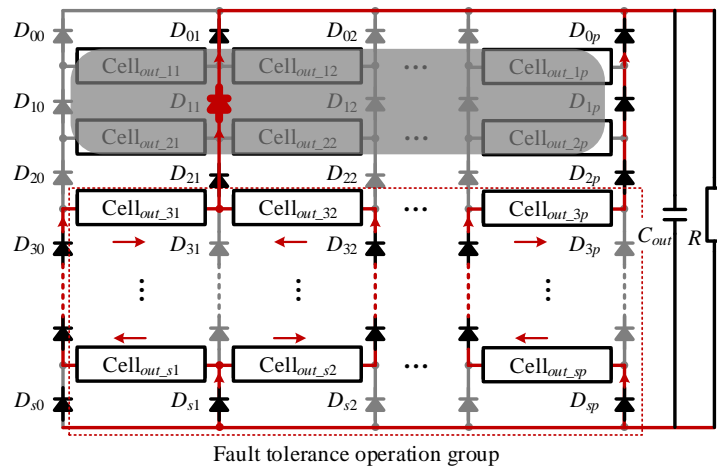
(b)

Figure 4.11 Fault tolerance when diode D_{11} is short-circuited: (a) working mode 1; (b) working mode 2.

4.4.3 Fault Tolerance of Open-circuited Diodes

Fault tolerance of open-circuited diode can be achieved as shown in Fig 4.12 (a) and (b). The fault tolerance operating group consists of the adjacent columns of the failed diode D_{11}, where the drive signals of cells in adjacent rows have a 180° phase shift and the cells in the same row have the same signals. Then, the adjacent rows have opposite polarities, and the cells in the same rows have the same polarity. Therefore, all the cells in the faulty group are connected in series to block the damaged devices. To achieve the same terminal voltage, the output voltages of cells in the faulty group is half of that in the normal operation groups since the number of cells in series connection in the faulty group is twice larger than that in the normal operation group.
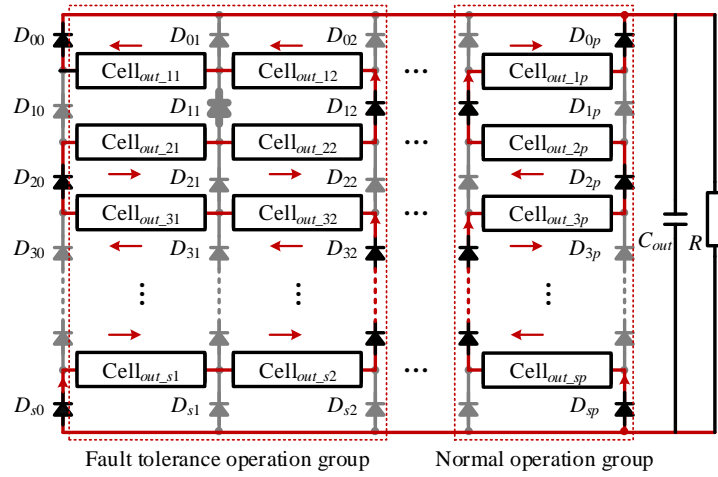
(a)
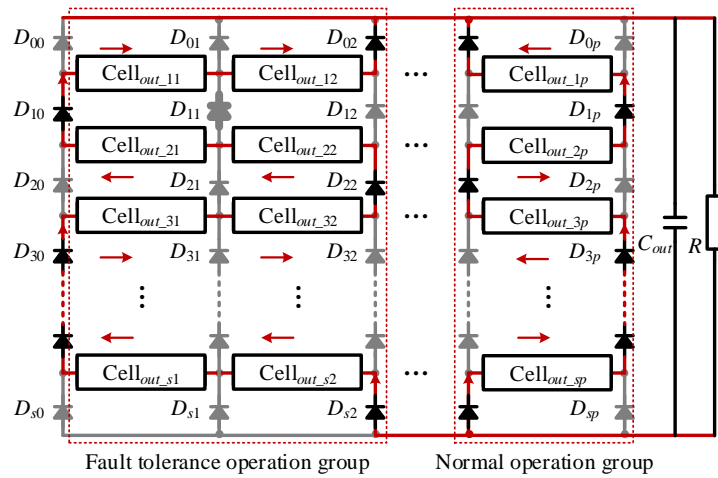
(b)

Figure 4.12 Fault tolerance when diode D_{11} is open-circuited: (a) working mode 1; (b) working mode 2.

4.4.4 DC Fault Tolerance

Furthermore, as illustrated in Fig 4.13, the diodes in the secondary circuits can be prevented from damage under DC fault condition, which is similar to the MMC converter by adding thyristors because they have a higher I^2t capacity compared with diodes.
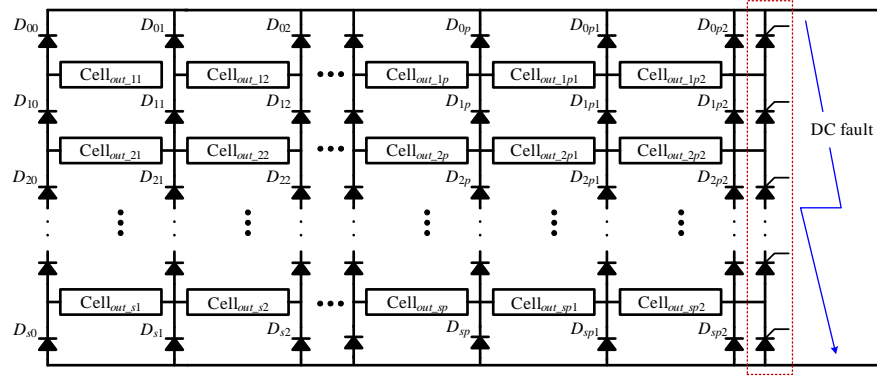
Figure 4.13 Addition of thyristors to protect secondary diodes under DC fault.

4.5   Simulation Verification and Discussion

To verify the functionality of the proposed converter, a simulation model consisting of 6 rows×6 columns that is similar to the one shown in Fig 4.7 is built in the software PSIM. For the 6 columns, columns 1~4 are active, while columns 5~6 are redundant. Table 4.1 presents the simulation parameters.

Table 4.1 Simulation parameters.

System Parameters	Values	Components	Values
Input Voltage	100 V	Turns ratio 1:1:1:n	1:1:1:2
Output Voltage	1500 V	Leakage inductance L_k	60 µH
Battery	125 V	Input inductor L_1	5 mH
Switching Frequency	10 kHz	Inductor L_2	2 mH
Output Power	5 kW	Clamp capacitor C_c	20 µF

The steady-state waveforms of the converter are shown in Fig 4.14 and Fig 4.15. All cells in columns 1~4 work with the column interleaved strategy. The adjacent cells have the opposite voltage and current polarities. With 6 rows in the matrix structure, the power switches have low voltage stress, which is 1/6 of the output voltage, and the voltage and current ratings of all diodes are as low as 1/6 or 1/3 of the output voltage and current respectively.
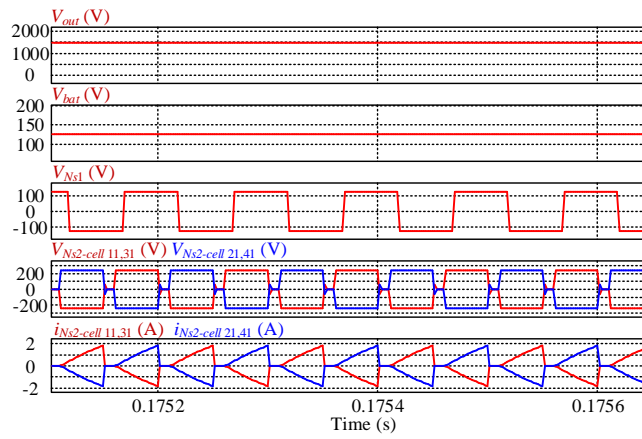
(a)
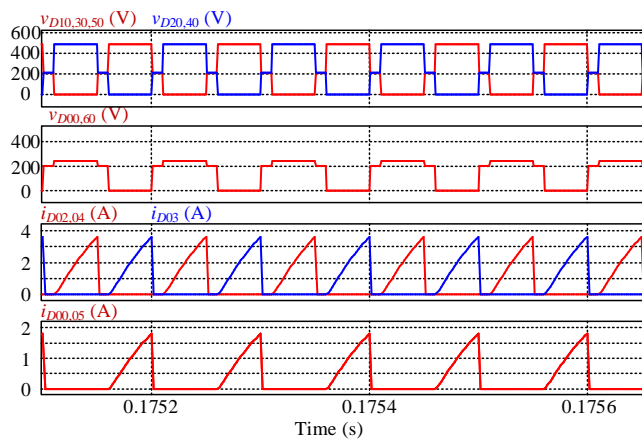
(b)

Figure 4.14 Steady-state waveforms with PV source: (a) voltage/current of basic cells; (b) voltage/current of diodes.
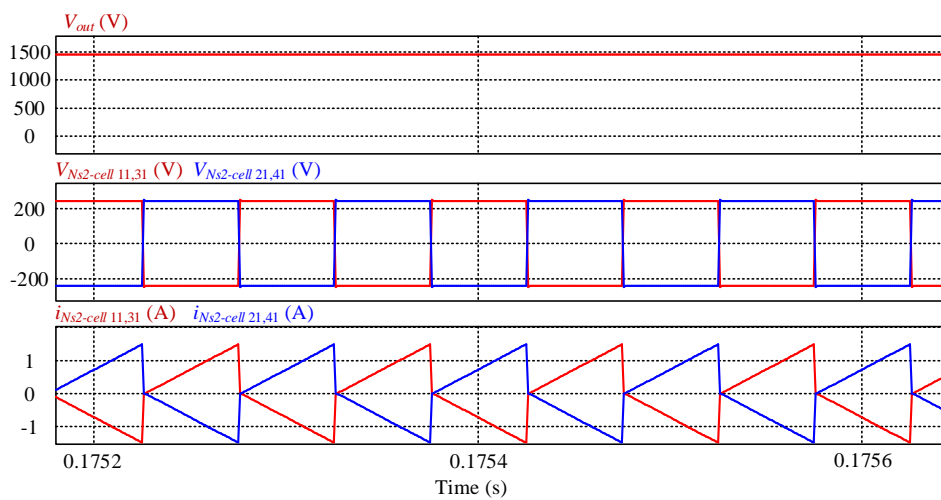
Figure 4.15 Steady-state waveforms of voltage/current of basic cells without PV source.

As illustrated in Fig 4.16, before turning on switch S_{M1} or S_{C1} in the primary circuits, the drain-source currents of both switches, i_{dsM1} and i_{dsC1} are negative which shows the currents flow through their parasitic diodes so that zero voltage turn-on is achieved for S_{M1} or S_{C1}. Similarly, the switches S_{M2} and S_{C2} can also obtain ZVS due to symmetrical operation.
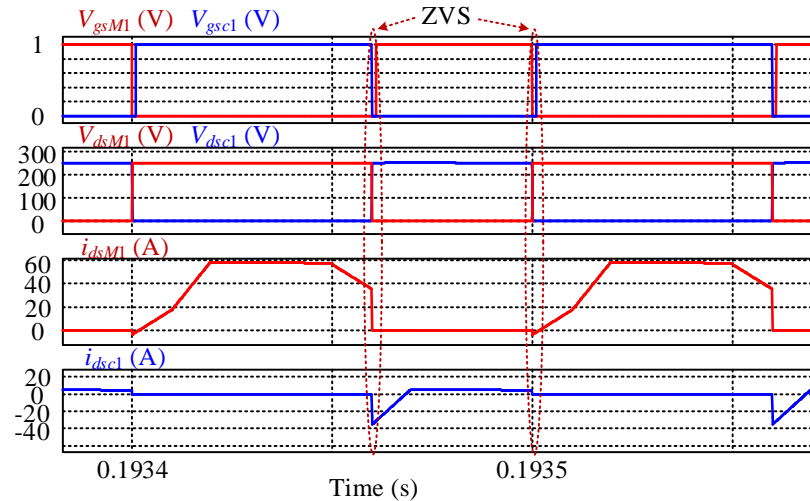
Figure 4.16 ZVS of switches in the primary circuit.

The voltage-current waveforms for switches $S_1 \sim S_4$ are depicted in Fig 4.17 where D_b is set as 0.5. As shown in Fig 4.17 (a), when the battery is charged, the currents flow through the parasitic diodes of the corresponding switch before the switch is turned on so that ZVS is achieved. When the battery is discharged in Fig 4.17 (b), four switches still can be turned on with zero voltage due to the resonance between the inductance L_2 and the parasitic capacitors of switches. Therefore, all switches can achieve zero voltage turn-on, which significantly reduces the switching loss.
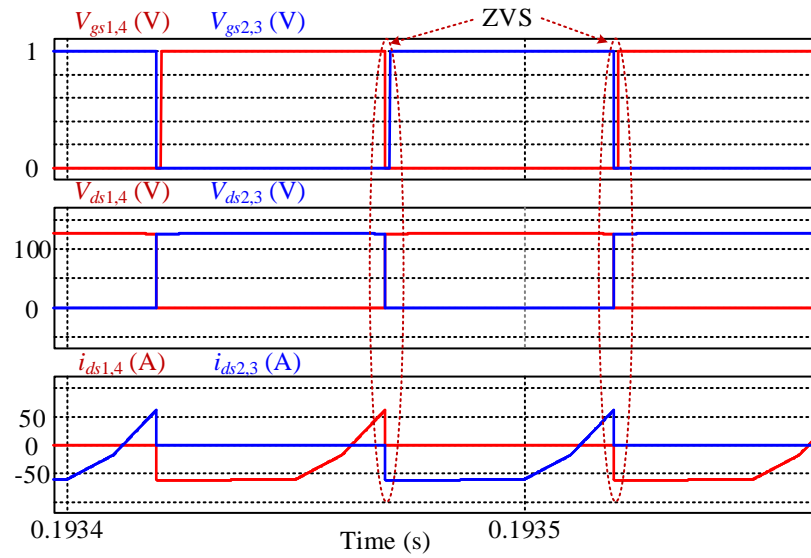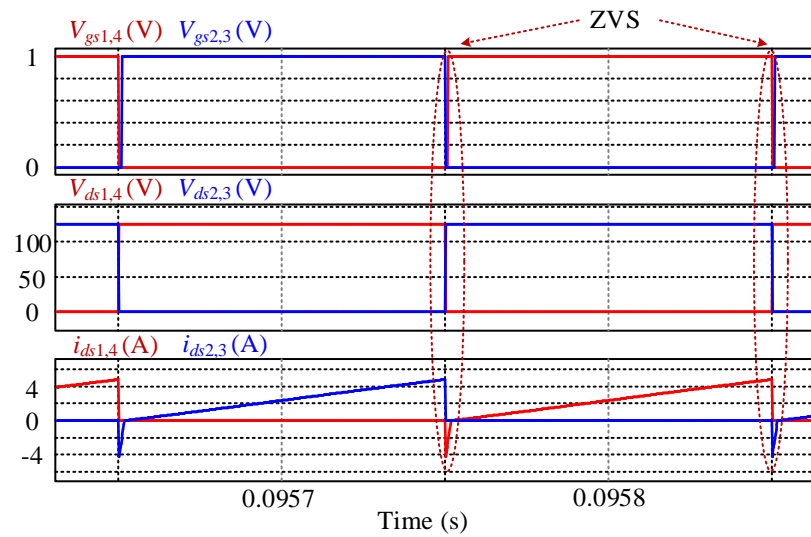
Figure 4.17 ZVS of switches in the battery side circuit: (a) battery is charged; (b) battery is discharged.

Fig 4.18 illustrates the fault tolerance capability with redundancy. At 0.1s, columns 1~2 are inactive in the case that there are fault cells in columns 1~2 or diodes in columns 0~1. Then the redundant columns 5~4 start to work to guarantee the normal operation.
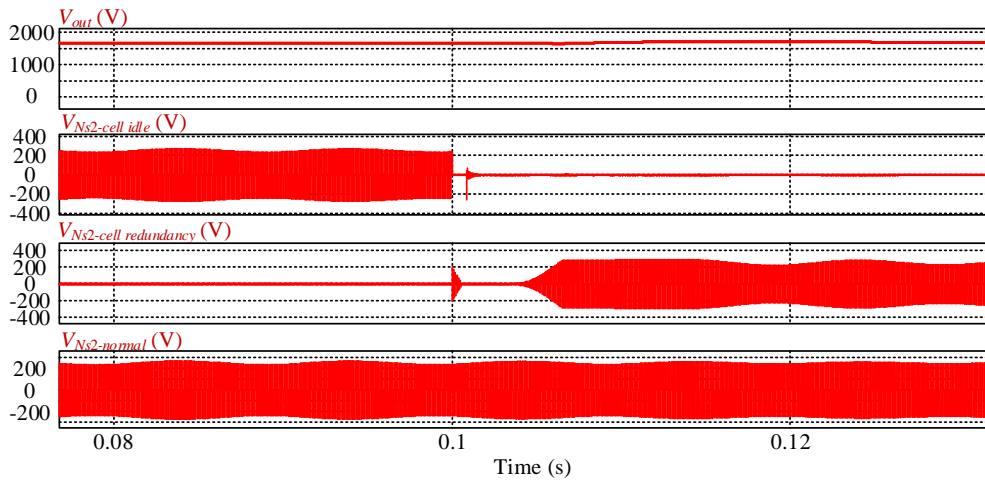
Figure 4.18 Fault tolerance operation with redundancy.

Fig 4.19 presents the fault tolerance operation without redundancy, where only columns 1~4 are active. In Fig 4.19 (a), when diode D_{11} is short-circuited, the cells in rows 1~2 are inactive at 0.1s to block the defective component. The duty cycle of switches in primary circuits is modified according to Eq.(4.12) to maintain the normal output voltage. In Fig 4.19 (b), diode D_{11} is open-circuited at 0.1s. To isolate the failed components, the cells in the columns that are adjacent to D_{11} work with the series interleaved strategy by changing the voltage polarities of the cells in column 1. Furthermore, the voltages of cells in the faulty group are reduced to half of that in the normal operation group to obtain the same terminal voltage.
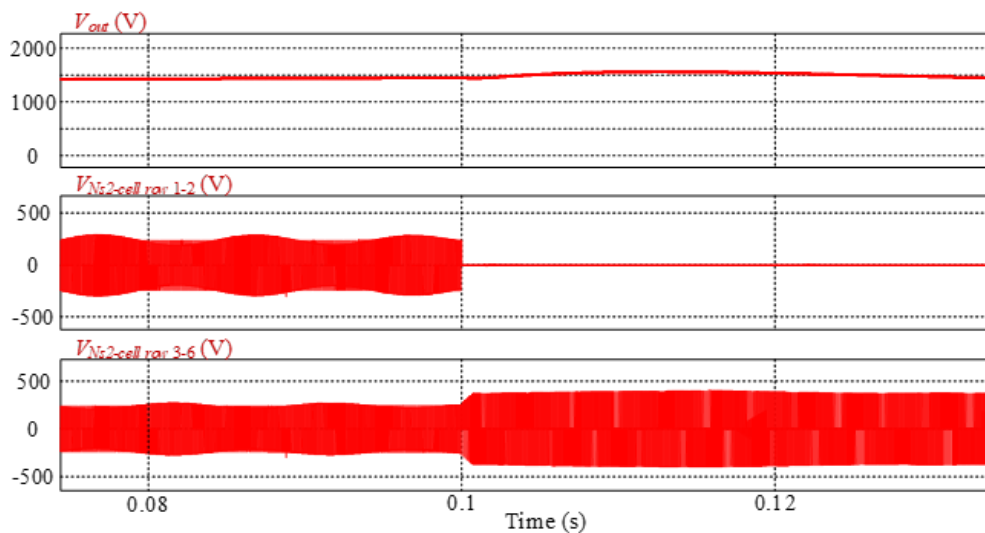
(a)
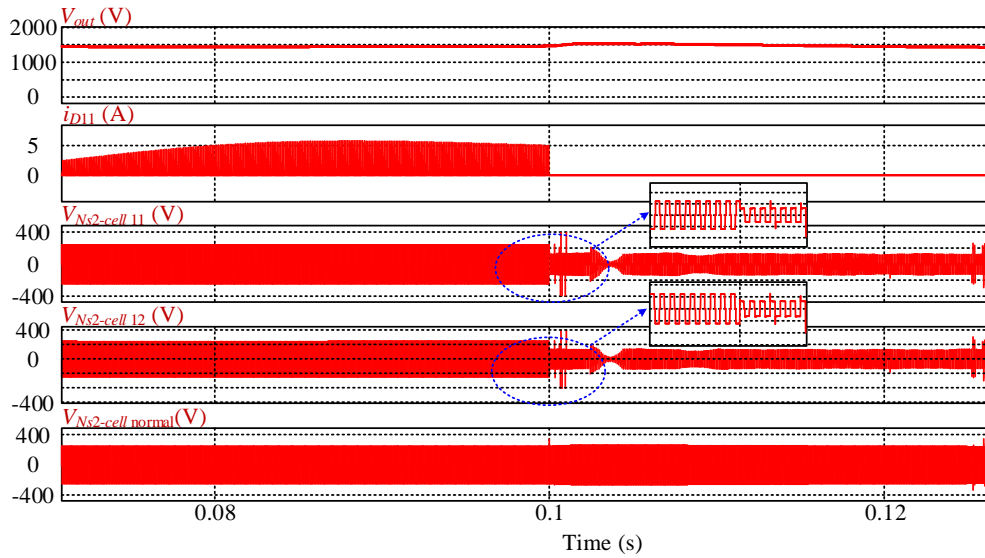
(b)

Figure 4.19 Fault tolerance operation without redundancy; (a) without redundancy for D_{11} short-circuit; (b) without redundancy for D_{11} open-circuit.

4.6   Summary

A modular multi-port high power level DC/DC power converter applied for HVDC transmission of RESs is proposed in this chapter. Thanks to the multi-port configuration, ES can be integrated with HVDC system with low component count as well as high compactness, and the power is transferred within one conversion stage. Additionally, due to the modularity, the proposed converter can achieve high output voltage and power by adding SMs.

The performances of isolated MPCs, partial-isolated MPCs, MMCs with ES system and the proposed converter are compared. The proposed model appears to be more efficient and reliable, presenting the features of low switching loss, high DC voltage conversion ratio, high control flexibility and high reliability.

The simulation results verify the feasibility of the SM and the proposed converter.

Chapter 5. MULTI-OUTPUT LED DRIVER INTEGRATED WITH 3-SWITCH CONVERTER & PASSIVE CURRENT BALANCE FOR PORTABLE APPLICATION

Instead of multi-module converters, the following two chapters present the design of two converters that can satisfy the applications with a relatively low power level (several hundred watts). This chapter introduces the stacked switched-capacitor-based multi-port DC/DC converter applied in portable high illuminance (100 W) LED applications such as camping lights. The converter should achieve the desired advantages of all power converters such as high compactness, high power efficiency, and low cost.

The switched capacitor structure is installed to obtain the high voltage step-up conversion ratio and the high compactness. Compared with employing two conventional converters, the proposed one uses one less active switch and hence the cost is reduced. Additionally, switching frequency of switches is 60 kHz, which reduces the weight and volume of passive components to ensure that the applications are portable. Furthermore, all switches could achieve low voltage stress and soft-switching, which are effective methods to improve power efficiency. The installed transformers can increase the voltage gain and reduce the voltage stress of switches. Besides that, the leakage inductance of transformers is utilised to realise soft-switching of switches. Hence, the conduction loss and switching loss of switches are significantly reduced, and high power efficiency as 94.6% is achieved. Moreover, for LED applications, the passive current balancing circuit is employed to guarantee the currents of the LED strings are same. A prototype with a 24 V input voltage is designed, fabricated, and measured to verify the theoretical analysis.

5.1   Introduction

LED has enormous potential in replacing conventional lamps in residential, automotive, decorative and medical applications due to its advantageous features such as high power density, high luminous efficiency, long lifespan, mercury free and quick response [17, 18]. For the high illuminance application scenarios, numerous LEDs are

connected in series or parallel. For series-connected LEDs, the high voltage stress is caused on the output capacitor and other insulation components. For parallel-connected ones, regulating the current through different LED strings requires the current balancing technology because of the LED's current-voltage characteristic and the negative temperature coefficient [19].

Achievement of high power efficiency while keeping high compactness of the whole system is still a challenge for LED drivers. To achieve high power density, the output capacitor of buck converter is removed, which decreases the power efficiency to under 90% [162]. Although the switched capacitor converter has a simple structure, the efficiency can only reach around 85% [163]. Fortunately, from the analysis of switched capacitor converters [164, 165], significant power loss can be avoided by employing inductors. Similarly, the flyback converter also has a simple structure and low power efficiency [166-168]. To increase its power efficiency, different types of snubber are utilised, but all of them have their deficiencies. For instance, active snubber [166] and TCR snubber [167] increase the circuit complexity and cost; RCD snubber [168] cannot recycle the leakage inductance power, which leads to hard-switching and causes massive switching loss. With at least two more inductors, LLC [169, 170] and CLCL topologies [171] can improve the power efficiency through achieving soft-switching operation of active switches. These projects improve the power efficiency with the sacrifice of compactness, which is not an ideal trade-off.

Current regulating for different LED strings can be achieved by applying active CBCs [172, 173] and passive CBCs [174-177]. The active way demands at least one active switch for each output channel resulting in the large switching loss. To avoid high cost and power loss, the majority of current products adopt passive methods, which can be realised by employing inductors [174, 175] or capacitors [176, 177]. The inductor-based method uses transformers to balance the currents through different branches. However, the deviation of transformers and the output voltages will reduce the balance accuracy. The capacitor-based method can provide precise current balancing with high power density and low cost.

This study designs an LED driver with several merits, for instance, multi-output, high power efficiency, controllable brightness, and reduced component count. With these advantages, the driver is suitable for high power portable applications such as

camping lights, vehicle headlights and emergency lights, etc. The proposed LED driver is presented in Fig 5.1.
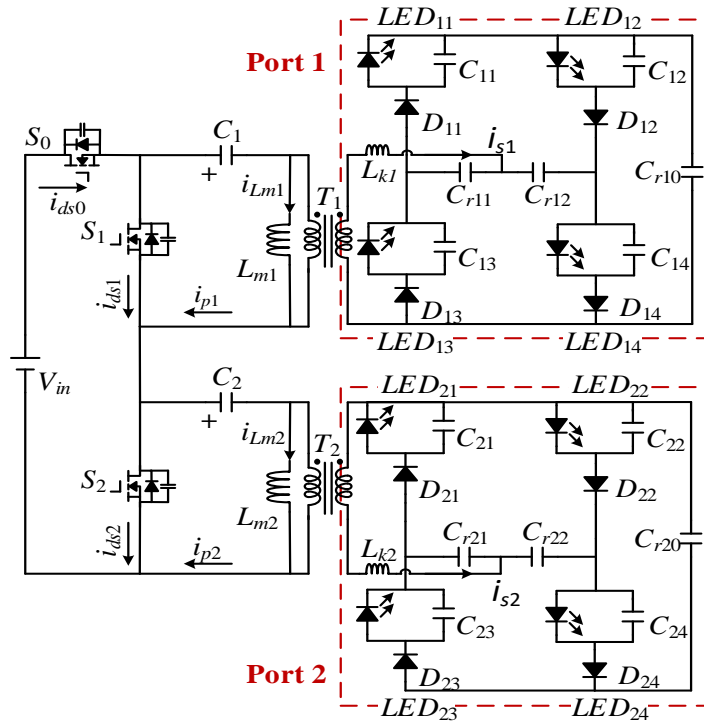
Figure 5.1 Equivalent topology of the proposed LED driver.

This chapter is organized as follows: Section 5.2 analyses the operation modes of the circuit; Section 5.3 discusses some main features of the topology; then Section 5.4 introduces the design guide; Section 5.5 presents the experiment results, and Section 5.6 gives the summary.

5.2   Operation Mode Discussion

The operation principles are discussed in this section. As depicted in Fig 5.1, the primary power stage consists of input DC voltage V_{in}, three active switches $S_0 \sim S_2$, two switched capacitors $C_1 \sim C_2$, and two transformers $T_1 \sim T_2$ with magnetic inductances $L_{m1} \sim L_{m2}$ as well as leakage inductances $L_{k1} \sim L_{k2}$. The three active switches, S_0, S_1, and S_2, control the two output ports: $S_0 \& S_1$ for Port 1, and $S_0 \& S_2$ for Port 2. The two ports are identical CBCs. More precisely, Port 1 has three resonant capacitors $C_{r10} \sim C_{r12}$, four diodes $D_{11} \sim D_{14}$, four output capacitors $C_{11} \sim C_{14}$, and four LED loads $LED_{11} \sim LED_{14}$.

Following assumptions are made to simplify the analysis.

1. All switches and diodes are ideal.

2. The transformers T_1 and T_2 are identical with the same voltage ratio of n:1 and the secondary side referred leakage inductance L_k.

3. The input voltage is an ideal DC voltage.

4. The capacitance of the resonant capacitors C_{r10}, C_{r11}, C_{r12}, C_{r20}, C_{r21}, and C_{r22} are equal.

   $C_{r10}=C_{r11}=C_{r12}=C_{r20}=C_{r21}=Cr_{22}=C_r$.

5. Voltages of capacitors C_1~C_2 are constant.

6. Switches S_1 and S_2 have the same duty cycle, $D_{S1}=D_{S2}=D$.
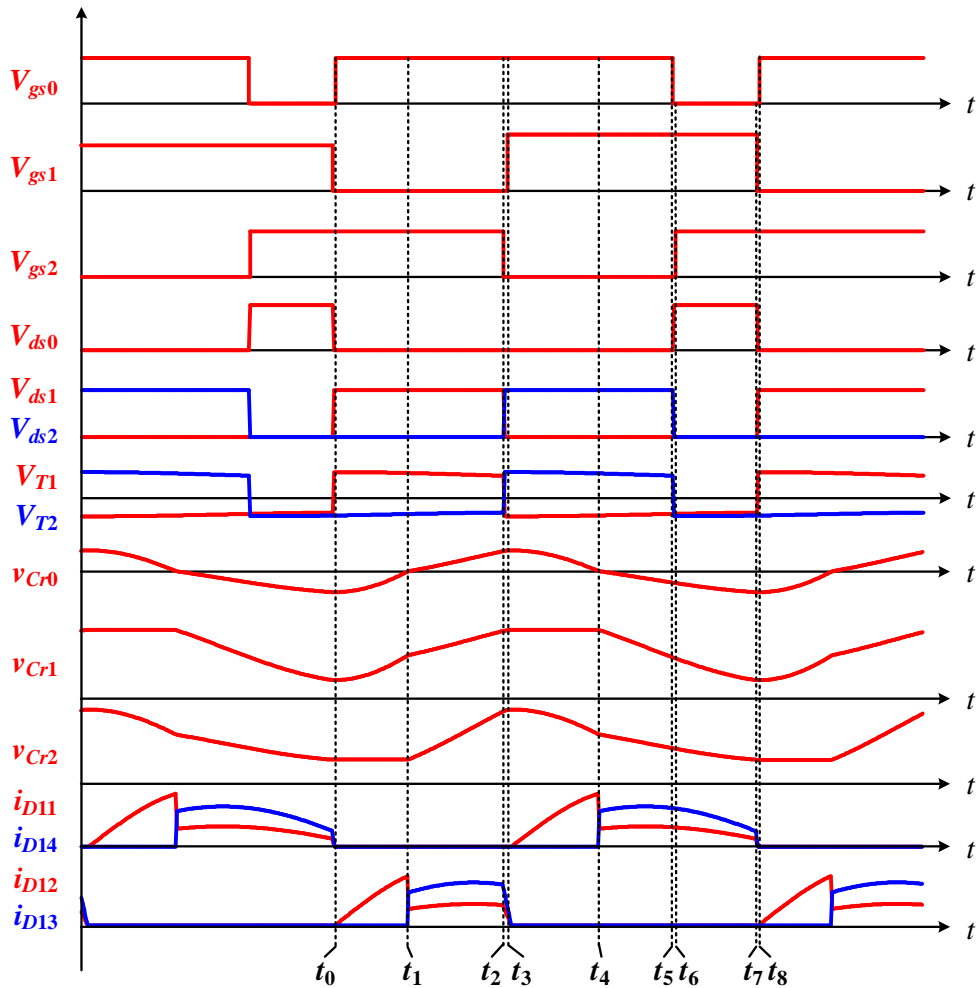
Figure 5.2 Key waveforms of the proposed LED driver.

Fig 5.2 shows the key waveforms corresponding to the eight operating modes depicted in Fig 5.3. V_{gs0}~V_{gs2} and V_{ds0}~V_{ds2} are control signals and drain-to-source

voltages of switches $S_0 \sim S_2$ respectively. $V_{T1} \sim V_{T2}$ are the primary voltages of transformers $T_1 \sim T_2$; $V_{Cr0} \sim V_{Cr2}$ are voltages of three resonant capacitors $C_{r10} \sim C_{r12}$; $i_{D11} \sim i_{D14}$ are currents through diodes $D_{11} \sim D_{14}$. The two passive CBCs have a similar operation so that the operation of Port2 is not discussed.

(a)

(b)

(c)

(d)

(e)

(f)

(g)   (h)
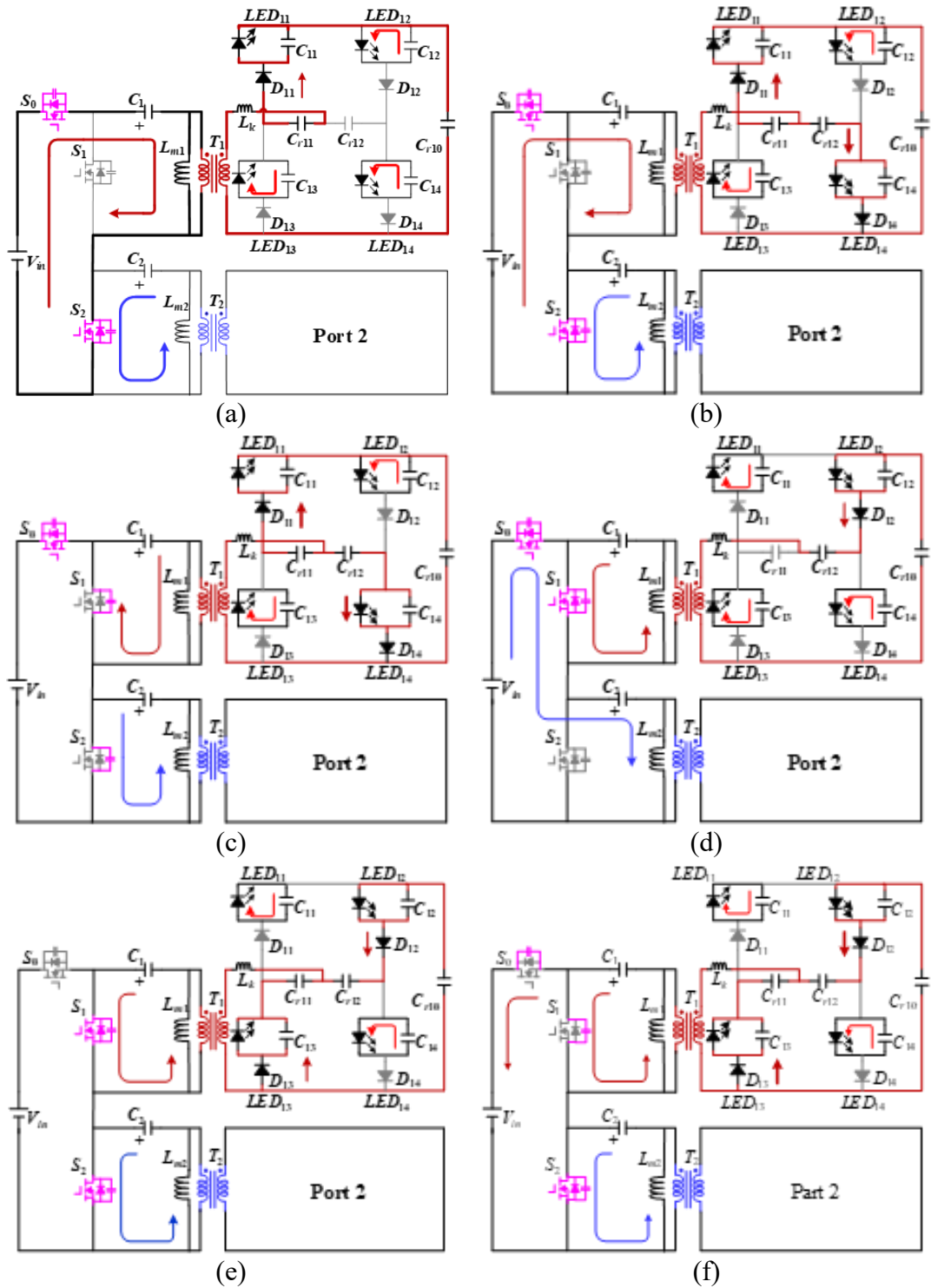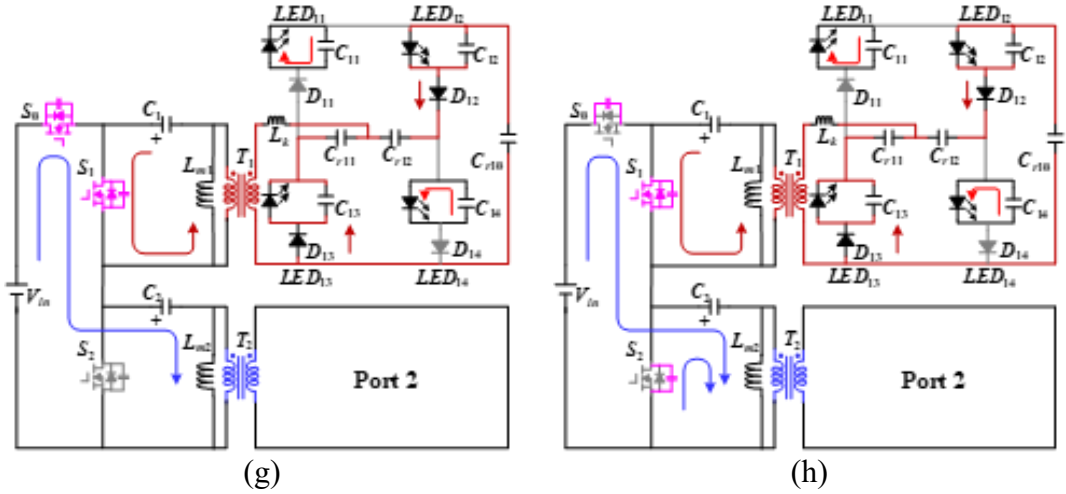
Figure 5.3 Operation Modes 1-8 of the proposed LED driver: (a) Mode 1 [t_0-t_1]; (b) Mode 2 [t_1-t_2]; (c) Mode 3 [t_2-t_3]; (d) Mode 4 [t_3-t_4]; (e) Mode 5 [t_4-t_5]; (f) Mode 6 [t_5-t_6]; (g) Mode 7 [t_6-t_7]; (h) Mode 8 [t_7-t_8].

According to the volt-second balance, the voltage across $C_1 \sim C_2$ can be obtained.

$$V_C \cdot D \cdot T_s = (V_{in} - V_C) \cdot (1-D) \cdot T_s \tag{5.1}$$

$$V_C = V_{in}(1-D) \tag{5.2}$$

Where $D = t_{on}/t_s$ and t_{on} is the on-time of switches $S_1 \sim S_2$ in each switching cycle.

Mode 1 [t_0-t_1]: At time t_0, the switch S_0 is turned on, and the switch S_1 is off. The voltage across the transformer T_1 is $V_{in} - V_c$. The current through L_{m1} keeps increasing linearly until t_2.

$$i_{Lm1}(t) = \frac{V_{in} - V_C}{L_{m1}}(t - t_0) \tag{5.3}$$

At time t_0, the total voltage across C_{r10}, C_{r11} and C_{11} is lower than that of C_{r12} and C_{14}.

$$v_{Cr10}(t_0) + v_{Cr11}(t_0) + V_{C11} < v_{Cr12}(t_0) + V_{C14} \tag{5.4}$$

Therefore, D_{11} is firstly forward biased to transfer power to LED_{11}, and C_{r10} and C_{r11} are charged. The state equations of this mode are obtained as:

$$\begin{cases} L_{k1}\dfrac{di_{S1}}{dt} = \dfrac{V_{in}-V_C}{n} - v_{Cr10} - v_{Cr11} - V_{C11} \\[2mm] i_{S1}(t) = i_{Cr10}(t) = i_{Cr11}(t) \\[2mm] i_{Cr10}(t) = C_{r10}\dfrac{dv_{Cr10}}{dt} \\[2mm] i_{Cr11}(t) = C_{r11}\dfrac{dv_{Cr11}}{dt} \\[2mm] i_{Cr12}(t) = 0 \end{cases} \qquad (5.5)$$

With Eq.(5.5), the secondary side current and the voltages across capacitors C_{r10}, C_{r11} and C_{r12} can be calculated as:

$$\begin{cases} v_{Cr10}(t) = -\dfrac{\Delta v_{Cr-ini}}{2}\cos\omega_a(t-t_0) + \dfrac{\Delta v_{Cr-ini}}{2} + v_{Cr10}(t_0) \\[3mm] v_{Cr11}(t) = -\dfrac{\Delta v_{Cr-ini}}{2}\cos\omega_a(t-t_0) + \dfrac{\Delta v_{Cr-ini}}{2} + v_{Cr11}(t_0) \\[3mm] i_{S1} = i_{Cr11}(t) = \dfrac{\Delta v_{Cr-ini}}{Z_n}\sin\omega_a(t-t_0) \end{cases} \qquad (5.6)$$

Where $\Delta v_{Cr-ini}=(V_{in}-V_C)/n-v_{Cr10}-v_{Cr11}-V_{C11}$ is the voltage across the leakage inductance L_{k1} at time t_0. Z_n is the characteristic impedance of the resonant tank formed by L_{k1}, C_{r10}, and C_{r11}; ω_a is the resonant angular frequency. $z_n = \sqrt{L_k/0.5C_r}$ and $\omega_a = 1/\sqrt{0.5L_kC_r}$. At time t_1, the total voltage across C_{r10}, C_{r11} and C_{11} is the same as that of C_{r12}.

$$v_{Cr10}(t_1) + v_{Cr11}(t_1) + V_{C11} = v_{Cr12}(t_1) + V_{C14} \qquad (5.7)$$

Then, D_{14} is conducted. The time duration of Mode 1 is determined as:

$$\tau_1 = \frac{1}{\omega_a}\arccos(\frac{(V_{in}-V_{C1})/n - v_{Cr12}(t_0) - V_{C14}}{\Delta v_{Cr-ini}}) \qquad (5.8)$$

Mode 2 [t_1-t_2]: From t_1, D_{14} begins to be forward biased, and the power is transferred to LED_{11} and LED_{14}. In the secondary circuit, the resonant tank is composed of C_{r10}, C_{r11}, C_{r12} and L_{k1} in this mode. The state equation of Mode 2 is:

$$\begin{cases} L_{k1}\dfrac{di_{s1}(t)}{dt} = \dfrac{V_{in}-V_{C1}}{n} - v_{Cr10} - v_{Cr11} - V_{C11} \\ \qquad\qquad = \dfrac{V_{in}-V_{C1}}{n} - v_{Cr12} - V_{C14} \\ i_{s1}(t) = i_{Cr10}(t) + i_{Cr12}(t) = i_{Cr11}(t) + i_{Cr12}(t) \\ \qquad i_{Cr12}(t) = C_{r12}\dfrac{dv_{Cr12}(t)}{dt} \\ i_{Cr10}(t) = C_{r10}\dfrac{dv_{Cr10}(t)}{dt} = i_{Cr11}(t) = C_{r11}\dfrac{dv_{Cr11}(t)}{dt} \end{cases} \qquad (5.9)$$

According to Eq.(5.9), the secondary current i_{s1} is derived as:

$$i_{s1}(t) = 1.5i_{Cr1} = 3i_{Cr2} = \frac{k\Delta v_{Cr-ini}}{Z_n}\sin[\omega_b(t-t_1)+\theta] \qquad (5.10)$$

The time duration of Mode 2 is:

$$\tau_2 = t_{off} - t_1 \qquad (5.11)$$

Where t_{off} is the off-time of switches S_1 and S_2; $k=sin\omega_a\tau_1/sin\omega b\tau_{com}$, $\theta=\pi-\omega b\tau_{com}$ is the initial phase of i_s at t_1, $\omega_b = 1/\sqrt{1.5L_kC_r}$ is the resonant angular frequency according to Fig 5.3 (b) and $\tau_{com}=t_{com}-t_1$. t_{com} is the time taken for the resonant tank to achieve completing resonance, and t_{com} can be derived as:

$$\begin{aligned} t_{com} &= \tau_{com} + \tau_1 \\ &= \frac{\pi-\theta}{\omega_b} + \frac{1}{\omega_a}\arccos(\frac{(V_{in}-V_{C1})/n - v_{Cr12}(t_0) - V_{C14}}{\Delta v_{Cr-ini}}) \end{aligned} \qquad (5.12)$$

Mode 3 [t_2-t_3]: S_2 is turned off at time t_2. During Mode 3, the parasitic capacitor of S_1 is discharged while the parasitic capacitor of S_2 is charged. The voltage across S_1 drops from V_{in} to zero to achieve ZVS operation. The resonant processes of the power stage are given below.

$$\begin{cases} L_{m1}\dfrac{di_{Lm1}(t)}{dt} = v_{ds1}(t) - V_{C1} \\ L_{m2}\dfrac{di_{Lm2}(t)}{dt} = V_{in} - v_{ds2}(t) - v_{ds1}(t) - V_{C2} \\ i_{p2} - i_{p1} = 2\cdot C_s \cdot \dfrac{dv_{ds1}(t)}{dt} \end{cases} \qquad (5.13)$$

Where C_s represents the parasitic capacitance of the active switches.

Mode*s 4~5* [t_3-t_5]: At time t_3, switch S_1 is turned on with ZVS. During Modes 4~5, transformer T_1 is powered by capacitor C_1, and the polarity of the voltage across T_1 is opposite to that of Modes 1~3. The current through L_{m1} keeps decreasing linearly.

$$i_{Lm1}(t) = i_{Lm1}(t_3) - \frac{V_{C1}}{L_{m1}}(t - t_3)$$ (5.14)

Modes 4~5 is similar to Modes 1~2 except that the three resonant capacitors given reference of the capacitors here are discharged due to the reversed power flow direction. During Mode 4, D_{12} is firstly forward biased to transfer power from input to LED_{12}. At t_4, $v_{Cr0}+v_{Cr2}+V_{C12}=v_{Cr1}+V_{C13}$, and D_{13} is conducted when the power is transferred to LED_{12} and $LED_{13.}$

Mode *6* [t_5-t_6]: S_0 is turned off at t_5. Energy stored in the parasitic capacitor of S_2 is released while the parasitic capacitor of S_0 is charged. The resonant process can be expressed as:

$$i_{s1}(t) = 1.5i_{Cr1} = 3i_{Cr2} = \frac{k\Delta v_{Cr-ini}}{Z_n}\sin[\omega_b(t - t_1) + \theta]$$ (5.15)

Mode *7* [t_6-t_7]: At t_6, switch S_2 is turned on with zero voltage. Mode 6 takes a relatively short time that can be neglected. Mode 7 is a continuation of Mode 5.

Mode *8* [t_7-t_8]: S_1 is turned off at t_7. The parasitic capacitor of S_0 is discharged while the parasitic capacitor of S_1 is charged. The voltage across S_0 is decreased with the rising of the voltage across S_1. Therefore, at the start of the next switching cycle, S_0 can achieve ZVS. The resonant process in Mode 8 can be expressed by the following equations:

$$\begin{cases} L_{m1}\dfrac{di_{Lm1}(t)}{dt} = V_{in} - v_{ds0}(t) - V_{C2} \\ i_{p1} = 2 \cdot C_s \cdot \dfrac{dv_{ds1}(t)}{dt} \end{cases}$$ (5.16)

5.3   Topology Characteristics Analysis

5.3.1   Passive Current Balancing

By the charge balance of resonant capacitors, energy charged to C_{r11} through D_{11} in Modes 1~3 equals to the energy discharged from C_{r11} through D_{13} in Modes 5~8.

Because Modes 3, 6 and 8 are very short, they are ignored in this discussion. The balance of C_{r11} is between Modes 1~2, 5 and 7. The average current of D_{11} and D_{13} in a switching cycle T_s is:

$$i_{D11-avg} = \frac{Q_{11-ch}}{T_s} = \frac{Q_{11-dis}}{T_s} = i_{D13-avg} \qquad (5.17)$$

Where Q_{11_ch} is the energy charged to C_{r11} in Modes 1~2 and Q_{11_dis} is the energy discharged from C_{r11} in Modes 5 and 7.

Similarly, the charge balance of C_{r10} is achieved through D_{11} and D_{12}. C_{r12} is charged through D_{14} and discharged through D_{12}. Then, Eq.(5.18) ~ (5.19) are obtained as:

$$i_{D11-avg} = \frac{Q_{10-ch}}{T_s} = \frac{Q_{10-dis}}{T_s} = i_{D12-avg} \qquad (5.18)$$

$$i_{D14-avg} = \frac{Q_{12-ch}}{T_s} = \frac{Q_{12-dis}}{T_s} = i_{D12-avg} \qquad (5.19)$$

Therefore, according to Eq.(5.17)~(5.19), the relationship among average currents of diodes D_{11}~D_{14} are shown as:

$$i_{D11-avg} = i_{D12-avg} = i_{D13-avg} = i_{D14-avg} \qquad (5.20)$$

Additionally, because the output capacitors C_{11}~C_{14} are large enough, the four output currents and the notations of the four currents equal to the diodes average currents, respectively. Hence:

$$i_{LED11} = i_{LED12} = i_{LED13} = i_{LED14} \qquad (5.21)$$

Owing to the CBC, the currents of the four LED loads are balanced. Moreover, in accordance with Eq.(5.17)~(5.20), non-ideal factors of C_{r10}, C_{r11} and C_{r12} are tolerable.

5.3.2   Operation of Resonant Capacitors

According to the operations in Modes 1~2 and 4~7, power is delivered to the four output channels through four paths, which are C_{r10}-C_{r11}-LED_{11}, C_{r12}-LED_{14}, C_{r10}-C_{r12}-LED_{12} and C_{r11}-LED_{13}. When S_1 is open, C_{r10}-C_{r11} and C_{r12} are charged. When S_1 is closed, C_{r10}-C_{r12} and C_{r11} are discharged. Based on the current balancing analysis, the average current through LED_{11} and LED_{14} are equal. Therefore, Eq.(5.22) is derived.

$$\frac{0.5C_r(\Delta v_{Cr10-charge} + \Delta v_{Cr11-charge})}{T_s} = \frac{C_r \Delta v_{Cr12-charge}}{T_s} \qquad (5.22)$$

$$\rightarrow \Delta v_{Cr10-charge} + \Delta v_{Cr11-charge} > \Delta v_{Cr12-charge}$$

Hence, at time t_0, Eq.(5.4) is verified. After t_0, the power is delivered to LED_{11} firstly and then to LED_{14}. Similarly, when S_1 is turned on, the power is transferred to LED_{12} firstly and then to LED_{13}.

5.3.3   Control System

As illustrated in Fig 5.4 (a), currents through all LED strings in Port 1 and Port 2 are controlled by the PWM control where two individual PI compensators are adopted. Due to the current balancing characteristic, the currents through four LED strings in port 1 LED_{11}~LED_{14} have the same value as i_{o1}, and the value of currents through four LED strings LED_{21}~LED_{24} is i_{o2}. To collect output current i_{o1} and i_{o2}, two sample resistors R_{s1} and R_{s2} are series connected to one LED string in each port respectively. Thus, i_{o1} and i_{o2} will be regulated as $V_{o1,ref}/R_{s1}$ and $V_{o2,ref}/R_{s2}$. The control variables a and b are received from the two individual PI compensators according to the error voltage between reference voltages $V_{o1,ref}$–$V_{o2,ref}$ and voltages V_{o1} and V_{o2} across sample resistors R_{s1} and R_{s2}.

As shown in Fig 5.4 (b), the control signals for switches S_0, S_1 and S_2 are obtained by comparison of $(a+b, V_{t1})$, (V_{t1}, a) and (V_{t2}, b) respectively. D_{S0}, D_{S1}, and D_{S2} are the duty cycles of three switches. Compared with the sawtooth V_{t1}, V_{t2} is $a \times T_s$ delayed. To achieve the same operation of two ports, $V_{o1,ref}=V_{o2,ref}$ and $R_{s1} = R_{s2}$ so that the control variables $a=b$ and $D_{S1}=D_{S2}$. The duty cycle of three switches can be calculated by (23).

$$\begin{cases} D_{S1} = 1 - a \\ D_{S2} = 1 - b \\ D_{S0} = a + b \end{cases} \qquad (5.23)$$
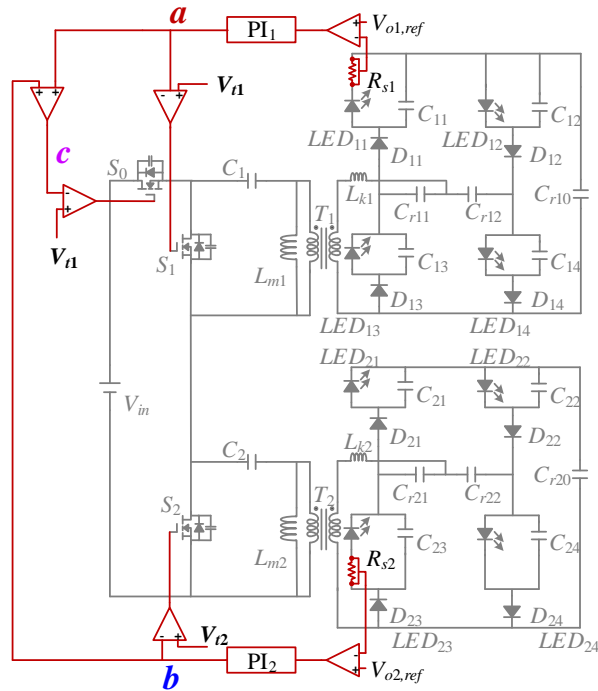
(a)
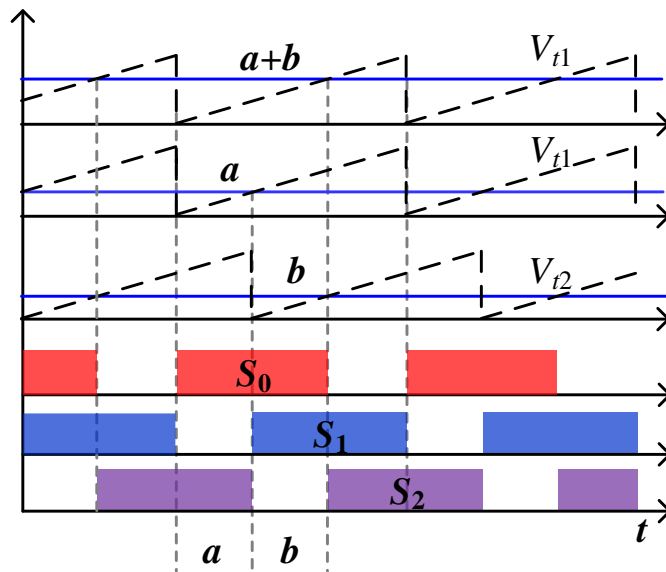
(b)

Figure 5.4 Control systems: (a) control system schematic; (b) control signals for three switches.

To adjust the brightness, the switch S_2 can be short-circuited by an external wire so that there is no power transferred to Port 2. The variable c becomes to zero. Therefore, the LED driver can provide two-stage brightness: 100% when both S_1 and S_2 are working and 50% when only S_1 or S_2 is operating. Furthermore, the driver also

increases reliability because of the two individual PI compensators and two isolated ports.

5.3.4 Soft-switching Analysis

As illustrated in Fig 5.5, all three power switches can achieve ZVS turn on. In Mode 3, before the switch S_1 is turned on, the energy stored in the parasitic capacitor of switch S_1 is released to zero. Then, the body diode of the switch is forward biased to conduct S_1 with zero voltage. Furthermore, because L_{m1} and L_{m2} are large enough, the parasitic capacitor of S_1 can be discharged completely. According to Eq.(5.13), if the dead time t_{ds1} is shorter than t_3–t_2, S_1 can achieve ZVS operation. Similarly, in Eq.(5.15)~(5.16), if the dead time t_{ds2} is shorter than t_6–t_5, S_2 can obtain ZVS; S_0 can achieve ZVS when $t_{ds0}<t_8$–t_7.
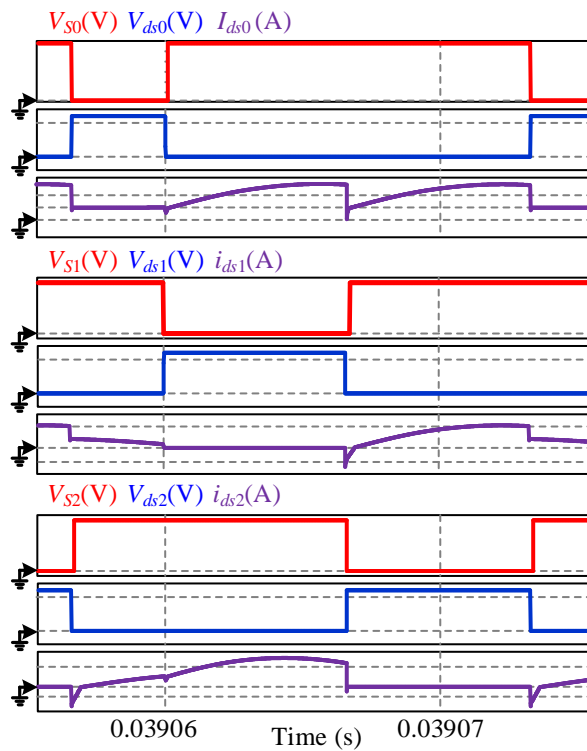
Figure 5.5 ZVS turn on of three switches in simulation.

$$\begin{cases} t_{ds1} > \tau_3 = \dfrac{2 \cdot C_s \cdot V_{in}}{i_{Lm1}(t_3) - i_{Lm2}(t_3)} \\[4mm] t_{ds2} > \tau_6 = \dfrac{2 \cdot C_s \cdot V_{in}}{i_{Lm2}(t_6)} \\[4mm] t_{ds0} > \tau_8 = \dfrac{2 \cdot C_s \cdot V_{in}}{-i_{Lm1}(t_8)} \end{cases} \qquad (5.24)$$

Where τ_3 is the time duration of mode 3; τ_6 is the time duration of mode 6; τ_8 is the time duration of Mode 8.

5.3.5 Expandable Topology

As illustrated in Fig 5.6, the converter can be extended in the output channels by adding resonant capacitors. According to the current balancing operation, one phase leg requires one resonant capacitor, e.g. $C_{r11} \sim C_{r12}$ for phase leg 1~2 respectively, and one more resonant capacitor, e.g. C_{r10} is connected between the two phase legs. Hence, by adding $2n-1$ resonant capacitors, $2n$ output channels can be achieved.
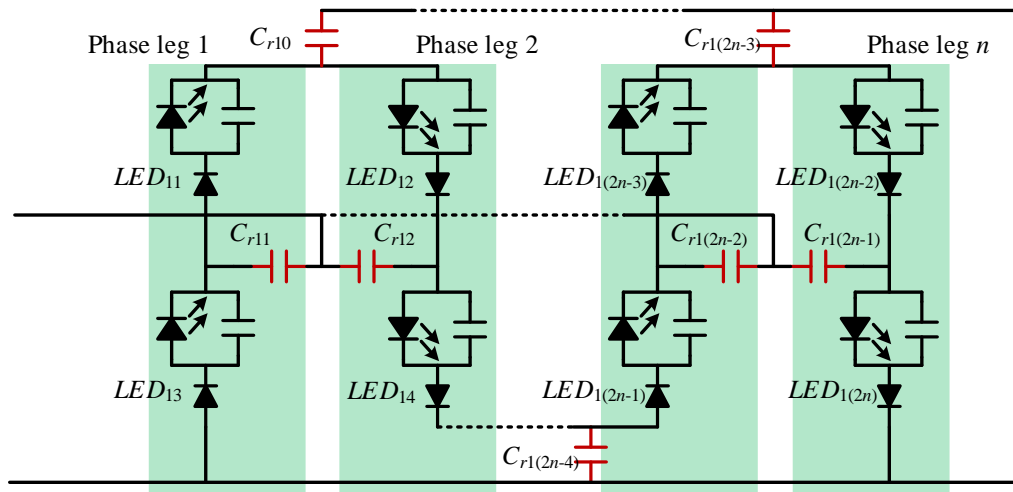
Figure 5.6 Expandable topology.

5.4   Design Guide

This section introduces the design considerations including the relationship among switching frequency, leakage inductor and the resonant capacitors, as well as the operating characteristics of components.

5.4.1 Passive Current Balancing

The average input current can be calculated as:

$$i_{in-avg} = \frac{t_{\text{off}} \cdot i_{p1}(t_2)}{2} \cdot \frac{2}{T_s}$$

(5.25)

The output power can be derived as:

$$i_{in-avg} = \frac{t_{\text{off}} \cdot i_{p1}(t_2)}{2} \cdot \frac{2}{T_s}$$

(5.26)

With the analysis and the trade-off between power dissipation in the active switches and transformers, the switching frequency is set at 60 kHz in the experiment. To achieve ZVS turn-on of switches, the on/off time of switches should be larger than the resonant time based on ω_a and ω_b so that there is always primary current i_p to discharge the parasitic capacitance of active switches. Moreover, the off-time of two switches S_1 and S_2 are shorter than their on-time. Hence, according to Eq.(5.12), the following equation can be obtained as:

$$t_{\text{off}} < t_{\text{com}} \rightarrow$$
$$L_k C_r > \frac{t_{\text{off}}^2}{0.5 \cdot A^2 + 1.5 \cdot (\pi - \theta)^2 + \sqrt{3} \cdot A \cdot (\pi - \theta)}$$

(5.27)

Where $A = arccos\{[(V_{in} - V_{C1})/n - v_{Cr12}(t_0) - V_{C14}]/\Delta v_{Cr\text{-}ini}$.

However, with a large leakage inductance, the secondary current i_s cannot recover to zero immediately after the turn-on/off of active switches. Hence, the leakage inductance is finally chosen as 9 µH, and the 3.3 µF resonant capacitance C_r is designed to satisfy Eq.(5.27).

Based on the primary side referred leakage inductance and switching frequency, the minimum value of switched capacitors is determined according to:

$$C_r > \frac{1}{4\pi^2 f_s^2 (L_k/n^2)}$$

(5.28)

For switched capacitor $C_1 \sim C_2$, a large capacitance can reduce their voltage ripple. However, to reduce the volume of the proposed converter, the switched capacitors are designed as 20 µF.

5.4.2 Maximum Voltage and Current of Switches

As shown in Fig 5.3, the maximum voltage of three switches equals the input voltage V_{in} when the corresponding switch is off. With the primary currents, the current of switch S_1 can be obtained as:

$$
\begin{aligned}
i_{s1}(t) &= i_{p2}(t) - i_{p1}(t) \\
&= \frac{1}{n}i_{s2}(t) + i_{Lm2}(t) - \frac{1}{n}i_{s1}(t) - i_{Lm1}(t) \\
&\approx \frac{1}{n}(i_{s2}(t) - i_{s1}(t))
\end{aligned}
\tag{5.29}
$$

Due to the large magnetic inductances and the voltage clamping transformers, the currents through magnetic inductances are ignored. According to the operation mode discussion, the current through S_1 reaches its maximum value in the interval $[t_3 \sim t_5]$. Additionally, the maximum current of switch S_2 is obtained at time t_7, which has the same value as that of S_1. Moreover, the current through S_0 is either i_{p1} or i_{p2}. Therefore, the maximum current value can be derived as:

$$
\begin{cases}
i_{ds0\_max} = \dfrac{k\Delta v_{Cr-\text{ini}}}{n \cdot Z_n} \\[4mm]
i_{ds1\_max} = i_{ds2\_max} = \dfrac{k\Delta v_{Cr-\text{ini}}}{n \cdot Z_n} - \dfrac{k\Delta v'_{Cr-\text{ini}}}{n \cdot Z_n}
\end{cases}
\tag{5.30}
$$

Where $\Delta v'_{Cr\text{-}ini} = -V_{C1}/n - v_{Cr10} + v_{Cr12} - V_{C12}$ indicates the voltage across leakage inductance L_{k1} at time t_4.

5.4.3 Voltage Variation of Resonant Capacitors

According to Eq.(5.17)~(5.19) and (5.22), Eq.(5.31) can be derived as:

$$
\begin{cases}
Q_{Cr10ch} = Q_{Cr10dis} = Q_{Cr11ch} = Q_{Cr11dis} = Q_{Cr12ch} = Q_{Cr12dis} \\
\Delta v_{Cr10-A} + \Delta v_{Cr10-B} = \Delta v_{Cr11-A} + \Delta v_{Cr11-B} = \Delta v_{Cr12-A} + \Delta v_{Cr12-B}
\end{cases}
\tag{5.31}
$$

Where $\Delta v_{cr\text{-}A}$ and $\Delta v_{cr\text{-}B}$ are the voltage change of corresponding switches in mode 1 and 2 respectively. Additionally, in mode 2, $i_{Cr12}(t) = 2i_{Cr10}(t) = 2i_{Cr11}(t)$, hence:

$$
Q_{Cr12ch} = 2Q_{B\_ch} = 2Cr\Delta v_{Cr10-B} = 2Cr\Delta v_{Cr11-B}
\tag{5.32}
$$

Where Q_{B_ch} indicates the energy stored in C_{r10} or C_{r11} in mode 2 and Q_{A_ch} is the energy stored in C_{r10} or C_{r11} in mode 1. Then the relationship among the voltage and energy variation of three resonant capacitors can be obtained:

$$\begin{cases} Q_{A\_ch} = Q_{B\_ch} = 0.5Q_{ch} \\ \Delta v_{Cr10-A} = \Delta v_{Cr10-B} = \Delta v_{Cr11-A} = \Delta v_{Cr11-B} = \Delta v_{Cr12-A} = \Delta v_{Cr12-B} = \Delta v_{Cr} \end{cases} \quad (5.33)$$

Depend on Eq.(5.8), (5.10), and (5.33), the following equation is obtained by:

$$C_r \Delta v_{Cr} = Q_{chA} = Q_{chB} \rightarrow$$
$$\int_{t_0}^{t_1} \frac{3\Delta v_{Cr-ini}}{Z_n} \sin \omega_a (t-t_0) dt = \int_{t_1}^{t_2} \frac{k \cdot \Delta v_{Cr-ini}}{Z_n} \sin[\omega_b (t-t_1) + \theta] dt \quad (5.34)$$

With the assumption $C_{r10}=C_{r11}=C_{r12}=C_r$, variables in Eq.(5.34) can be obtained as $\theta=1.37$ rad and $k=0.962$.

5.5 Experiment Verification and Comparison Results

5.5.1 Hardware
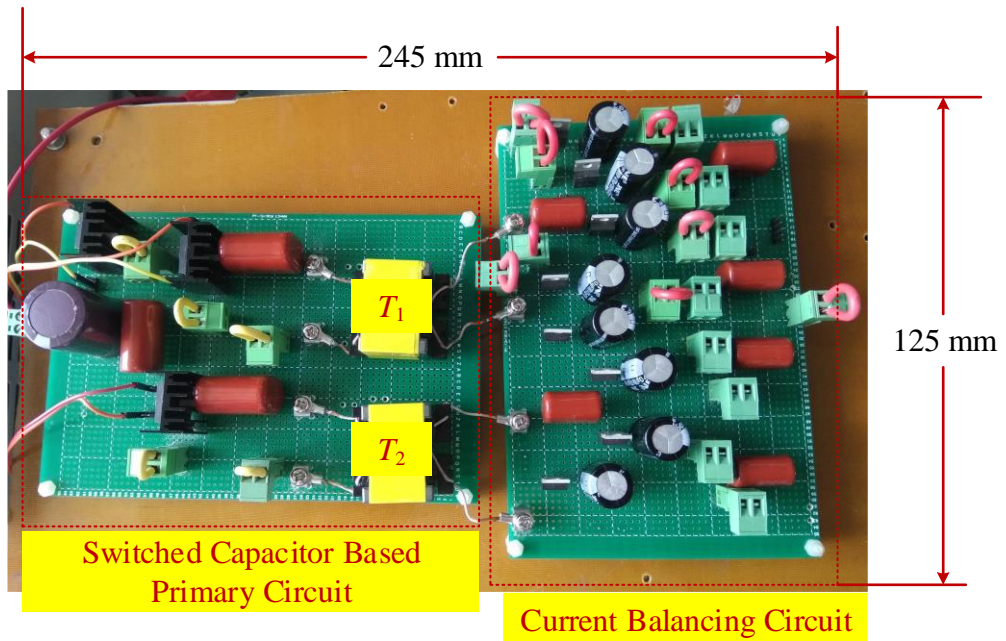
Figure 5.7 Prototype of the proposed LED driver.

To test and verify the performance of the designed LED driver, a prototype with 24 V DC input is built and displayed in Fig 5.7. Besides the proposed converter, main power supply as the input power source, auxiliary power supply to for control board

and MOSFET driver, oscilloscope, and the load LED strings are used to conduct the experiment.

Table 5.1 shows the elements employed in the prototype. The power efficiency of this prototype can reach 94.6% with 60 kHz switching frequency. Because of the similar operation of the two ports, only the experiment results of the primary power stage and Port 1 are illustrated.

Table 5.1 Experiment parameters.

Symbol	Definition	Value
V_{in}	Input voltage	24 V
P_{out}	Output power	100 W
C_r	Resonant capacitor	3.3 μF
C_{out} C_{1i}~C_{2i}	Output capacitor	440 μF
C_1~C_2	Converter capacitor	20 μF
V_{out}	Output voltage	30.8 V
i_{out}	Output current	0.4 A
Transformer:		
n	Voltage ratio	1:3
L_m	Magnetic inductance	203/201 μH
L_k	Leakage inductance	8.27/8.46 μH
$Core$	PQ3525	/
Semiconductor components:		
S_0~S_2	SFP65N06	/
D_{1i}~D_{2i}	MBR20100CT	/

5.5.2   Experiment Results

Fig 5.8 shows the voltages and primary currents of the two transformers. The experimental waveform is consistent with that in the theoretical analysis. When S_1 is closed, the voltages of transformer T_1 is negative as $-V_c$, and the current i_{p1} keeps decreasing. When S_1 is open, the voltage across transformer T_1 is positive as $V_{in}-V_c$, and the current i_{p1} keeps increasing. Due to the large magnetic inductance, the primary side current i_{p1} is mainly affected by the secondary side current i_{s1}. Moreover, due to the same reason, there is a delay for i_{p1} to recover to zero after the switch's states changed. Port 2 has a similar operation based on the on/off states of switch S_2. Additionally, when S_0 is off, the voltages of both transformers are negative.
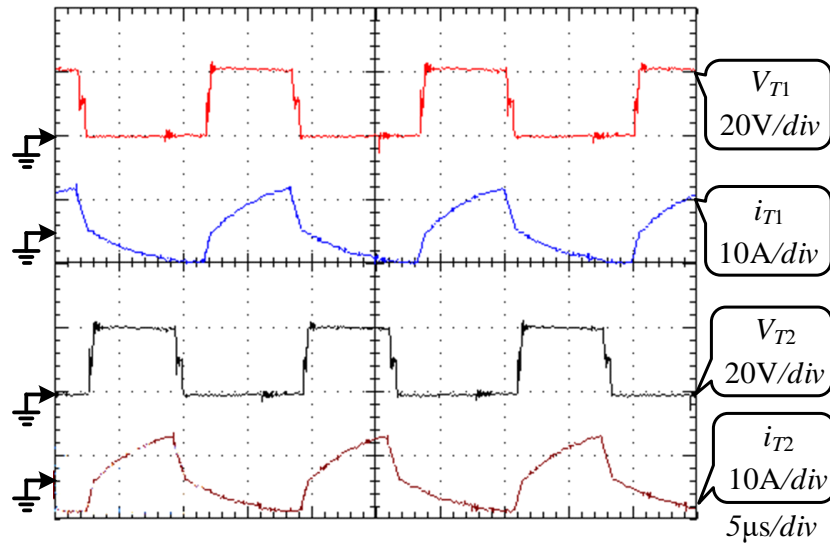
Figure 5.8 Currents and voltages of transformers T_1~T_2.

As illustrated in Fig 5.9, the ZVS operations of active switches are verified. For example, the drain-source i_{ds1} increases to $i_{p2}-i_{p1}$ after S_1 is closed; when S_0 is open, i_{ds1} drops to $-i_{p1}$. The drain-source current i_{ds} flows through the parasitic diode before the turn-on of the corresponding switch and ZVS turn-on of the switch is achieved so that the switching loss is significantly decreased.
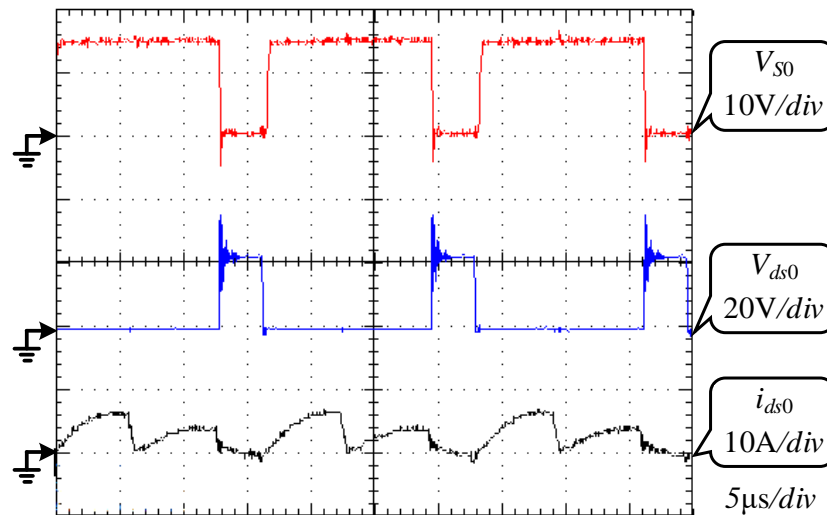
(a)
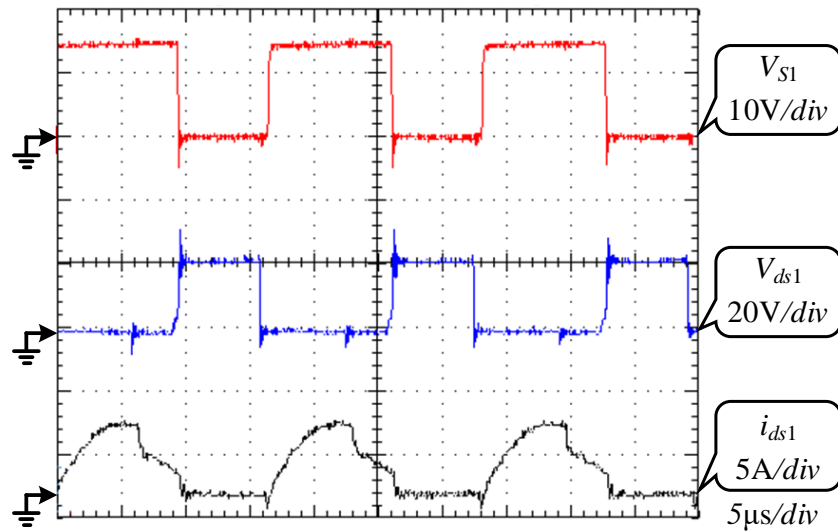
(b)
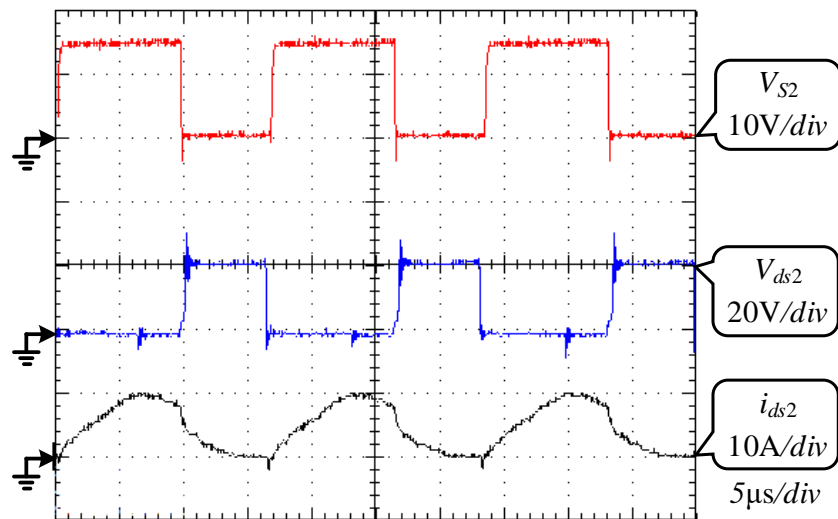
(c)

Figure 5.9 ZVS operation of the three MOSFET switches: (a) S_0; (b) S_1; (c) S_2.

In Fig 5.10, the charge and discharge processes of the resonant tank are tested and shown. The two pairs of diodes, D_{11}&D_{14} and D_{12}&D_{13} have the same operations. In Fig 5.10 (a), D_{14} is conducted after D_{11} with a time delay as τ_1, and then they are reverse biased at the same time. Additionally, according to Fig 5.10 (b), C_{r10} and C_{r11} are charged before C_{r12}. Then, C_{r10} and C_{r12} are discharged before C_{r11}. The voltages across C_{r11} and C_{r12} are always positive; however, for C_{r10}, the voltage crosses zero at t_1 and t_4 when the voltages of two branches are equal. The Fig 5.10 (c) displays the constant balanced output currents of the four output channels in Port 1.
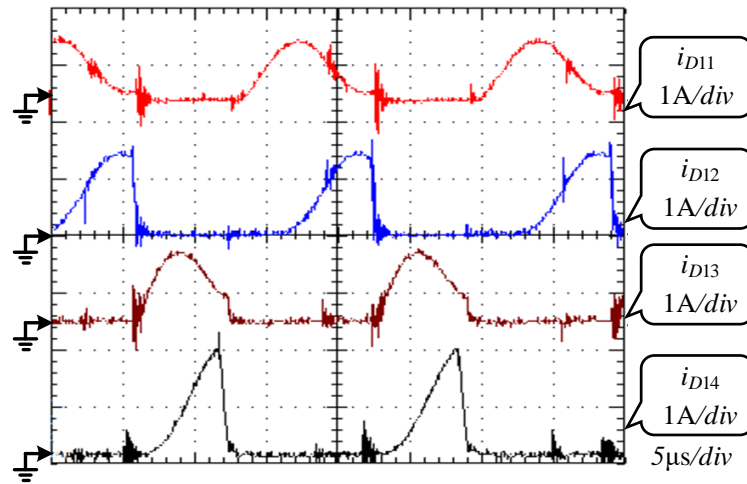
(a)
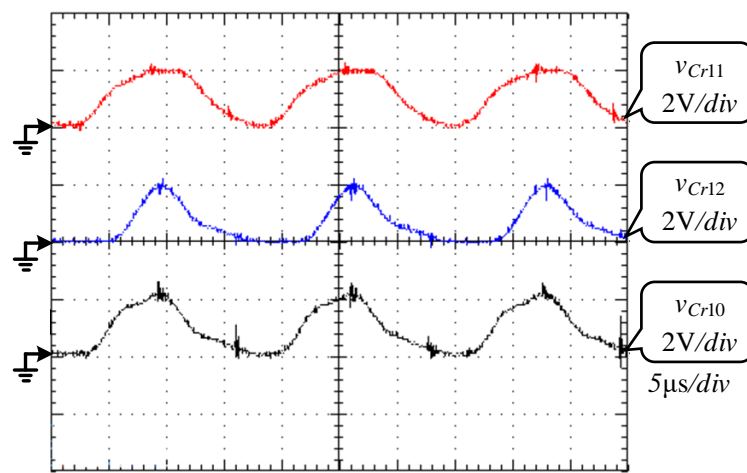
(b)
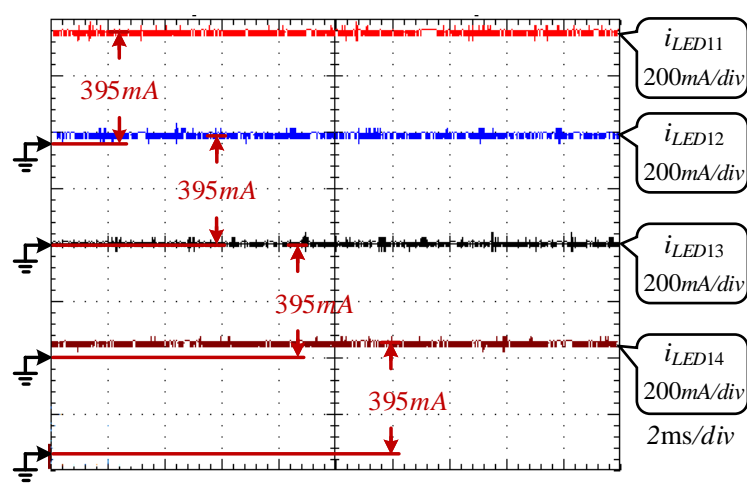
(c)

Figure 5.10 Current balance operation based on resonant capacitors: (a) currents through the diodes D11~D14; (b) voltages of resonant capacitors Cr10~Cr12; (c) output currents through four LED loads LED11~LED14.

The power efficiency of the LED driver is recorded under different input voltage values as shown in Fig 5.11. The red line with diamond markers is obtained when both switches S_1 and S_2 are working with 8 LED strings. The blue line with triangle markers is obtained when only switch S_1 is working with 4 LED strings in Port 1. The output power in the case presented by the blue line is half of that by the red line. With 8 LED strings, the efficiency can reach the highest point at 94.6%.
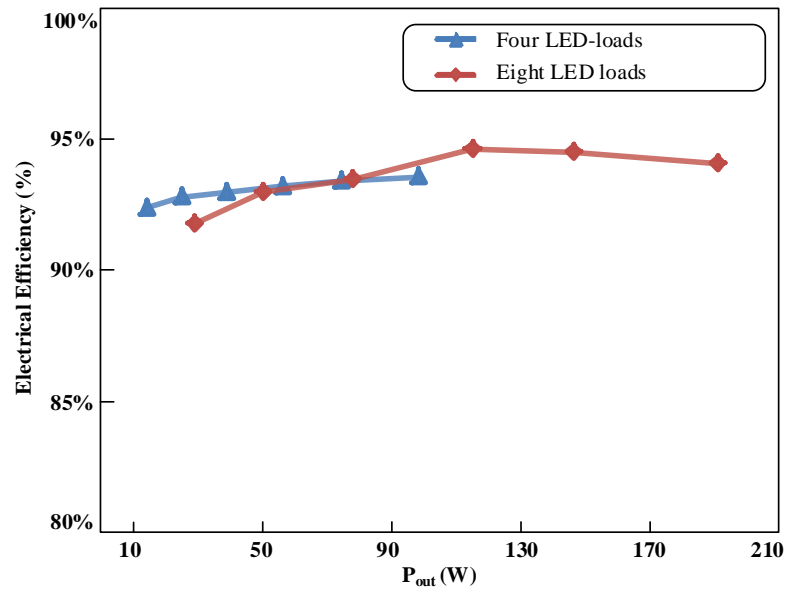
Figure 5.10 Power efficiency curve of the proposed LED driver.

5.5.3 Comparison Results

Comparison results in terms of design complexity, power efficiency, and output power scale are shown in Table 5.2. The non-isolated LED driver with switched capacitor [163] has the most straightforward design and fewest components. The LED driver with a flyback converter [167] uses only one active switch to achieve high compactness. However, their power efficiency is less than 90%, and they are preferred for low power application. For high illuminance applications, [171] and [174] can achieve the power efficiency of around 95%. However, two external inductors are applied in [171] to compose the CLCL resonant tank, which increases the design complexity and volume. Thanks to the transformers installed for current balancing among different LED strings, [174] is suitable for high power applications, while the non-ideal factors of those transformers result in high control complexity. From the aforementioned characteristic analysis, the proposed LED driver can achieve a high efficiency as 94.6% with the reduced component count. Additionally, the current

balancing of LED strings is obtained by resonant capacitors whose values are not necessary to be the same.

Table 5.2 Comparison of the proposed and other LED drivers.

LED drivers	Design complexity	Power efficiency	Output power
Switched capacitor [163]	Low	83%	4.85 W
Flyback converter [167]	Low	90%	8 W
CLCL resonant [171]	Medium	94.5%	100 W
Inductor-based CBC [174]	High	96.4%	80 W
Proposed	Low	94.6%	100 W

5.6   Summary

This study proposes a novel LED driver designed for portable applications. The primary power stage uses only 3 active switches which is one less than conventional separate 2 output isolated converters. The following advantages are achieved:

- High power efficiency: thanks to the ZVS turn-on and passive CBCs, high power efficiency as 94.6% is obtained.

- Low design complexity: the power stage uses only two magnetic components and two capacitors to achieve ZVS for all active switches. The current balancing operation is achieved due to the three resonant capacitors. Additionally, compared with a conventional two isolated output converter, the proposed one uses one less active switch.

- Multiple outputs: because of the two separate ports power stage and the two CBCs, the driver provides eight LED output-channels, which are divided into two parts with the same structure.

Experiment results are presented to verify the ZVS of active switches, the operation of two isolated ports and the balanced output currents of the proposed LED driver. This project is suitable for high power portable applications such as camping lights, vehicle lights and emergency lights.

Chapter 6. A THREE-SWITCH-BASED SINGLE-INPUT DUAL-OUTPUT CONVERTER WITH SIMULTANEOUS BOOST & BUCK VOLTAGE CONVERSION

Due to the integration of components, multi-port converters can use fewer elements to achieve a similar performance as applying multiple single-input single-output (SISO) converters. Hence, the cost is reduced. With the increasing demand of applications that have various output voltages such as EV, HEV, personal computers, and micro-grid systems, the single-input multi-output (SIMO) converter with fewer components is becoming the cost-effective option instead of employing multiple SISO converters. However, SIMO converters have cross regulation problems which cause the voltage error when there is external disturbances or load variation of the other output ports. This chapter proposes a SIDO converter with simultaneous buck and boost output stages, which has an improved cross regulation performance by reducing the voltage error caused by other output ports. At the meantime, the proposed SIDO converter should contain other desired advantages introduced before, such as low cost, high voltage gain, high operation frequency, and high power efficiency.

Thanks to the design as the independent power flow and two control variables, the cross regulation performance is improved, and the voltage error ratio is decreased from 11.5% to 1.55%. To save cost, the proposed SIDO converter uses one less switch to achieve almost the same performance as that of employing two SISO converters by integrating two switches into one. The coupled inductor and voltage multiplier circuit are installed to enlarge voltage gain of the boost output stage. 150 kHz switching frequency can achieve small converter size. Additionally, the soft-switching and low voltage stress of switches are obtained due to the installation of the coupled inductor, which reduces the switching loss and conduction loss of switches. The maximum power efficiency reaches 96.6%. To verify the theoretical analysis and measure the power efficiency, a prototype circuit with 48 V input and 24 V/2 A, 200 V/1 A outputs is built.

6.1 Introduction

The DC/DC power converters with multiple outputs are widely used in applications such as hybrid electric vehicles, DC micro-grid systems, renewable energy systems, and personal computers that require energy flow and voltage regulation of different outputs [140, 153, 178-183]. A simple way to realise these requirements is employing N SISO converters for N voltage levels, as illustrated in Fig 6.1(a), which results in high cost and low power efficiency due to a large number of components [184]. In order to reduce the number of components and overall cost, the SIMO converter as shown in Fig 6.1(b) becomes the dominant option since it can integrate multiple SISO converters into one.
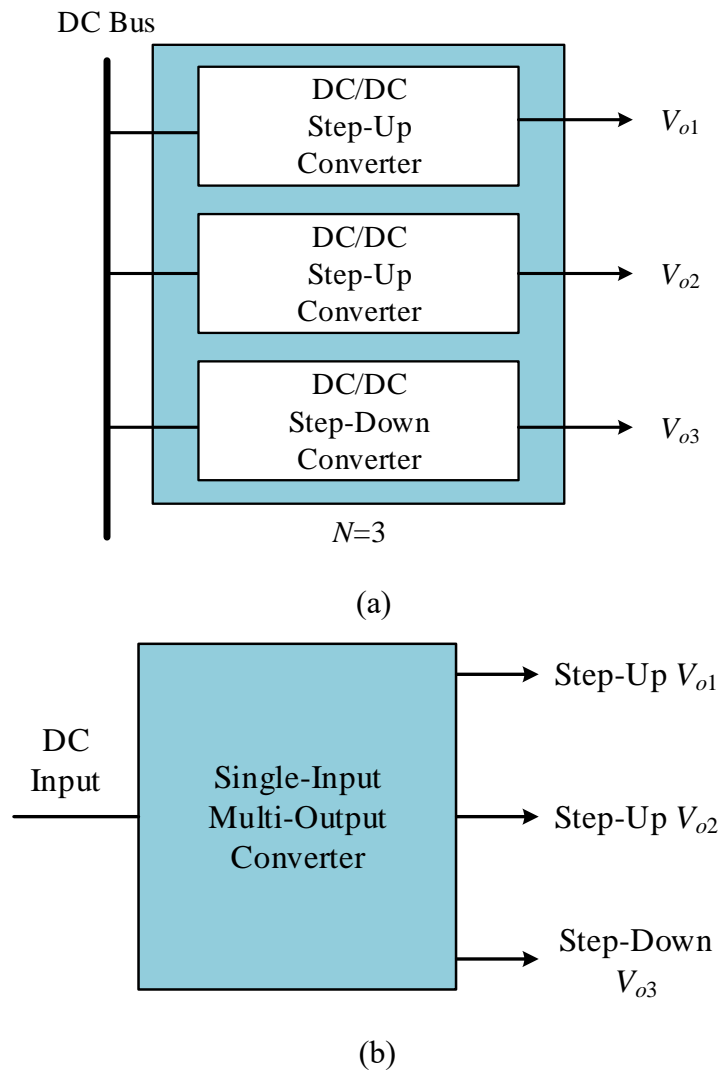
Figure 6.1 The schematic of converters with multiple outputs: (a) conventional method; (b) SIMO converter.

Additional secondary windings or transformers are utilised in conventional isolated SISO converters to obtain multiple outputs, whose cost is low owing to the simple configuration [185-189]. There is only one control variable, and the other output voltages are regulated depending on the turns ratios of their corresponding windings or transformers. However, the load variation of one output port will cause overshoot or undershoot voltages of other outputs due to parasitic characteristics of components, which is called cross regulation problem. Hence, voltage error of the unregulated output ports is significant. To achieve independent control of each output, secondary-side post-regulators (SSPRs) are installed to supply additional control variables for each output by adding external active switches in the secondary circuits [190, 191]. However, the cross regulation problem still exists during the dynamic response with load variation because the currents of all loads flow through the same magnetized inductor. For SSPRs solutions, single-inductor multi-output converters are the promising topologies because they use only one inductor and a small number of switches, thus the cost is low [17-19][192-194]. Unfortunately, it also suffers from the cross regulation problem in the continuous conduction mode (CCM) due to the interface among the loads. Various remedial methods are proposed to suppress the cross regulation of single-inductor multi-output converters [195-199]. The time multiplexing control technique based on discontinuous conduction mode is employed to improve the cross regulation performance [198]. Nevertheless, the inductor current ripple is large in the heavy load condition, resulting in a large output voltage ripple and switching noise. Furthermore, an additional switch is connected with the inductor in parallel to realise pseudo continues conduction mode (PCCM), which reduces the high current ripple of components when applying heavy loads [199]. However, the power loss is increased due to the appearance of nonzero inductor current during the freewheeling interval.

Then, the independent power flow of different outputs is required to improve dynamic performance. However, improved cross regulation performance is obtained at the expense of other desired advantages such as low cost, simultaneous boost as well as buck output voltages, and high efficiency. Topologies use dual-buck structure or two FB circuits with one joint leg to obtain independent two outputs [200-202], while, a large amount of active switches as six switches for two output ports increases the cost. To reduce cost, the converters using two HB circuits [203] or one FB converter

with parallel-series LLC resonant tanks [204] are proposed. However, except the voltage gain caused by transformers, their two output voltages are either at the buck or boost stages at the same time [200-204]. Besides the simple integration of two converters, several SIDO converters use only two switches to obtain concurrent step-up and –down outputs, which are developed from conventional buck-boost as well as Ćuk SISO converters [205-208]. However, the hard-switching of switches limits their power efficiency as 91.3% [208]. Moreover, three-level converters can achieve a high power efficiency as 95.9% while the cross regulation performance is weak due to significant voltage spikes [209]. From the above discussion, current SIDO converters do have part of the desired advantages, while their weakness is significant.

Therefore, a novel topology is proposed to not only improve cross regulation performance, but also maintain other advantages like low cost, both step-up and -down output voltages, and high power efficiency at the same time. To obtain improved cross regulation performance, two control variables and independent power flow are achieved from the proposed topology and two individual proportional integral (PI) compensators. Hence, the cross regulation problem is alleviated with a proper control strategy. Compared with two SISO converters, the proposed topology uses one less active switch so that cost is reduced. Furthermore, with the integration a buck converter and a coupled inductor connecting with a voltage multiplier circuit, simultaneous boost and buck output voltages are realised. Thanks to the voltage multiplier circuit, the proposed converter can obtain a high voltage step-up conversion ratio with low voltage stress of active switches. Additionally, all switches can achieve ZVS operation, which significantly reduces the switching loss. This chapter is organized as follows. The operation principles are introduced in Section 6.2. Then, a detailed theoretical analysis and design consideration are shown in Section 6.3. In Section 6.4, experimental results and discussion are illustrated to verify the theoretical analysis. Finally, the summary is given in Section 6.5.

6.2   Operation Principles

6.2.1   Operation Modes Analysis

As illustrated in Fig 6.2 (a), the proposed SIDO converter contains the single input V_{in}, boost output V_{o1}, and buck output V_{o2}. The converter is composed of three active

switches $S_1 \sim S_3$, one clamp capacitor C_5, one coupled inductor T_1, one filter inductor L_1, and the voltage multiplier circuit as well as two filter capacitors C_{o1} and C_{o2}. The voltage multiplier circuit consists of four clamp capacitors $C_1 \sim C_4$ and four diodes $D_1 \sim D_4$. For the coupled inductor, the dot end of the primary side connects with the positive side of sources, and the other end of the primary side is connected to the dot end of the secondary side. Additionally, as depicted in Fig 6.2 (b), the coupled inductor is equivalent to an ideal transformer with the magnetic inductance L_m, leakage inductance L_k, and the turns ratio of $N_s : N_p$. To simplify the analysis, all switches and diodes are assumed to be identical. Additionally, the capacitances of $C_1 \sim C_5$ are large enough and their voltages $V_{C1} \sim V_{C5}$ are assumed to be constant.

(a)

(b)
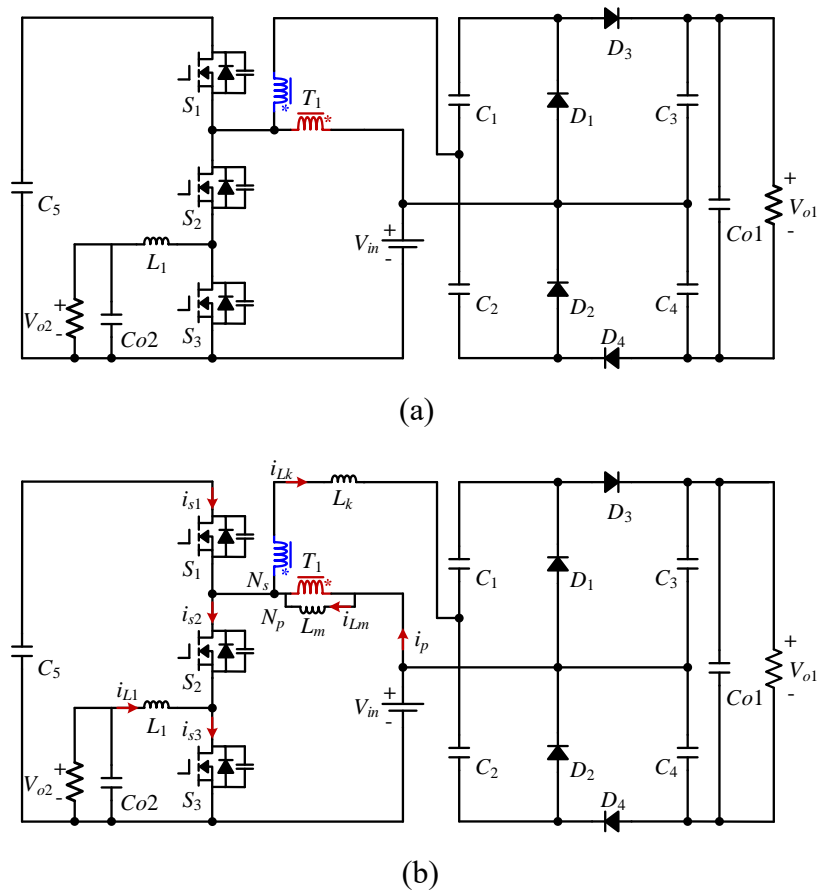
Figure 6.2 The proposed SIDO converter: (a) the topology; (b) the equivalent circuit.

Some key waveforms are depicted in Fig 6.3, and the equivalent circuits of the corresponding operation modes are shown in Fig 6.4. $v_{gs1} \sim v_{gs3}$ are the control signals for active switches $S_1 \sim S_3$ respectively. When S_1 is on, switches S_2 and S_3 are off alternatively. Additionally, v_{gs1} leads v_{gs3}, and v_{gs3} leads v_{gs2}. $V_{ds1} \sim V_{ds3}$ and $i_{ds1} \sim i_{ds3}$ are the drain-to-source voltages and currents of three switches respectively. i_{L1}, i_{Lm} are the

currents of the filter inductor L_1 and magnetic inductance L_m. i_p is the primary side current of the coupled inductor. I_{Lk} is the current of leakage inductance L_k. $i_{d1}\sim i_{d4}$ are the currents of four diodes $D_1\sim D_4$.
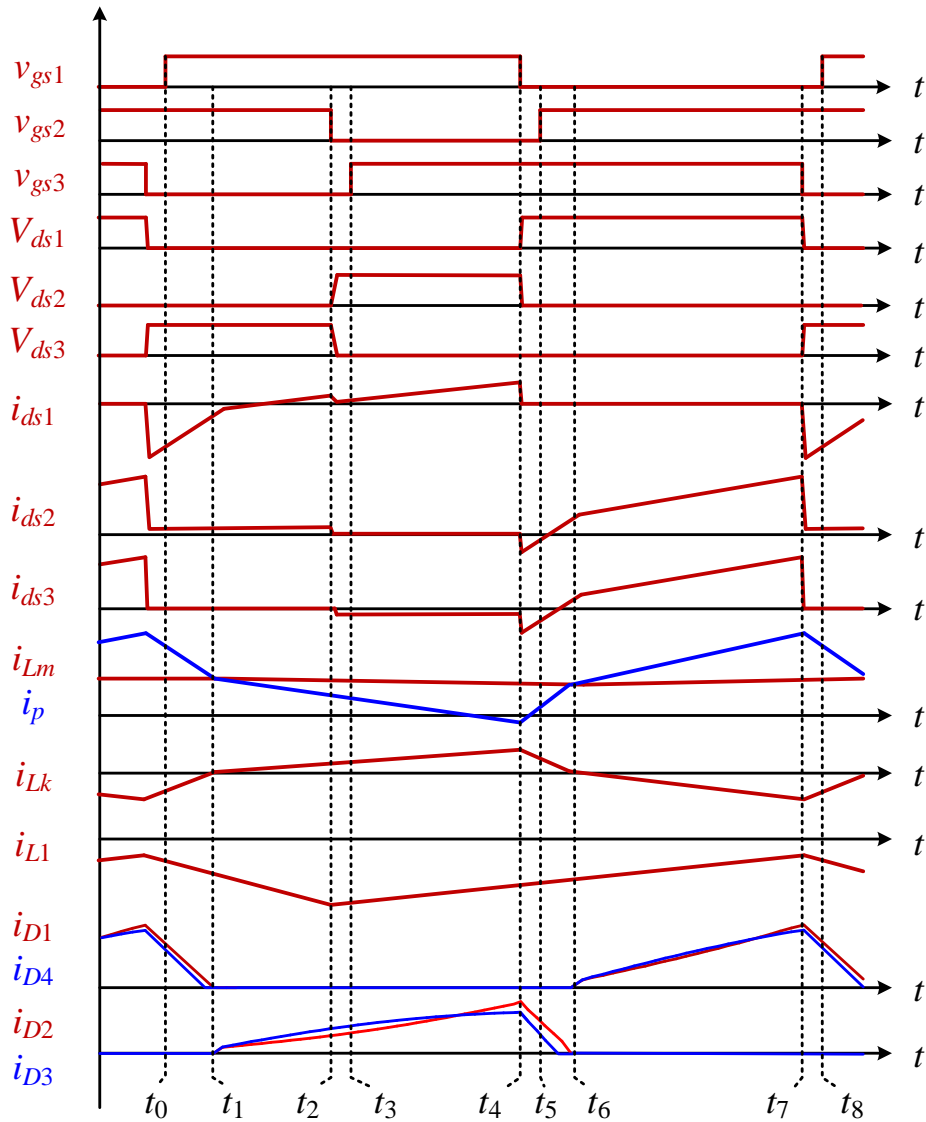
Figure 6.3 Some key waveforms of the proposed converter.
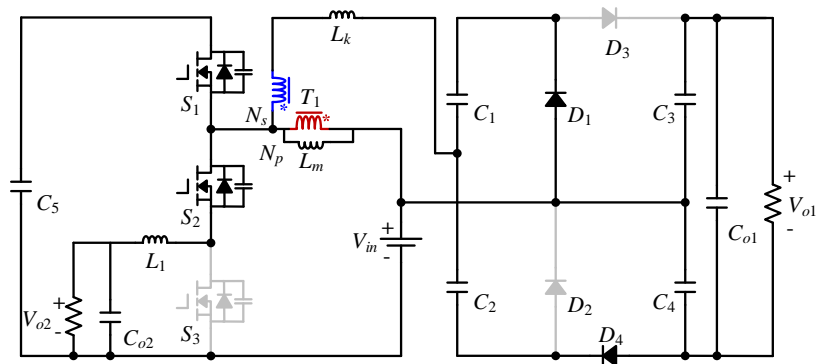
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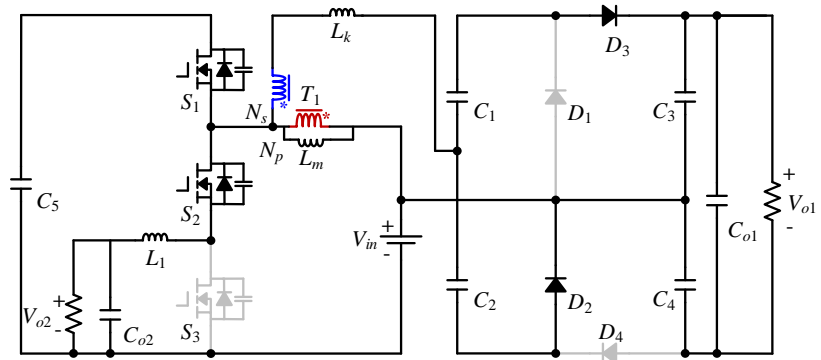
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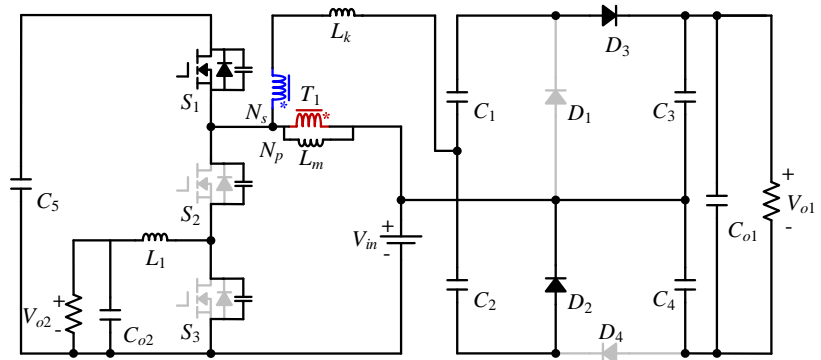
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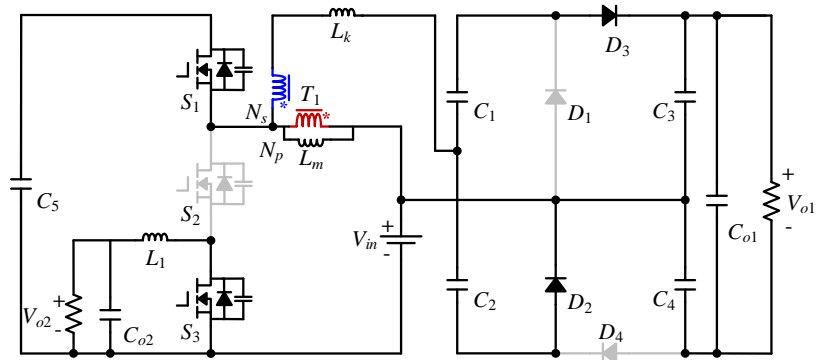
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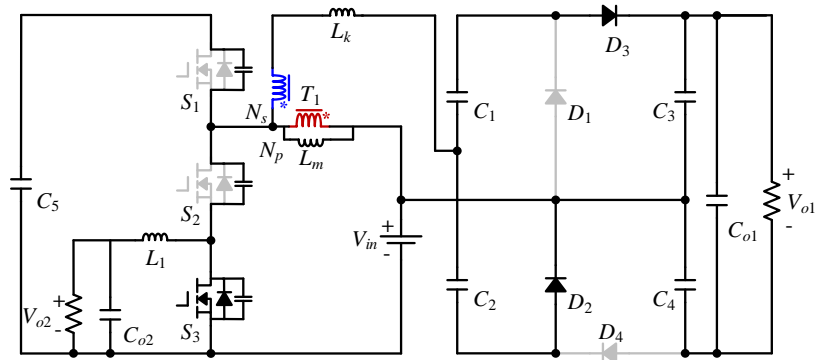
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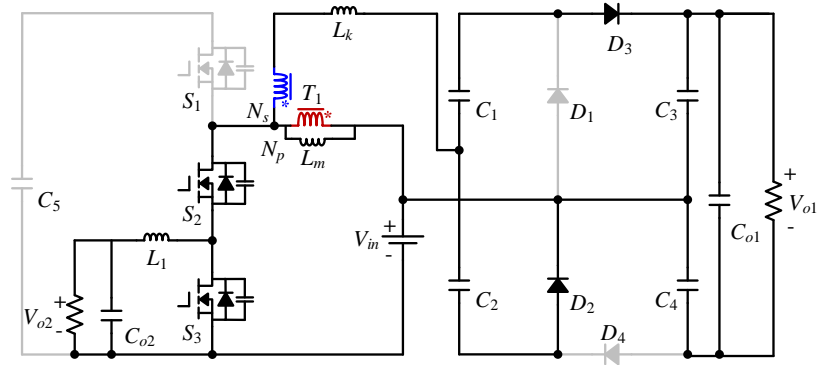
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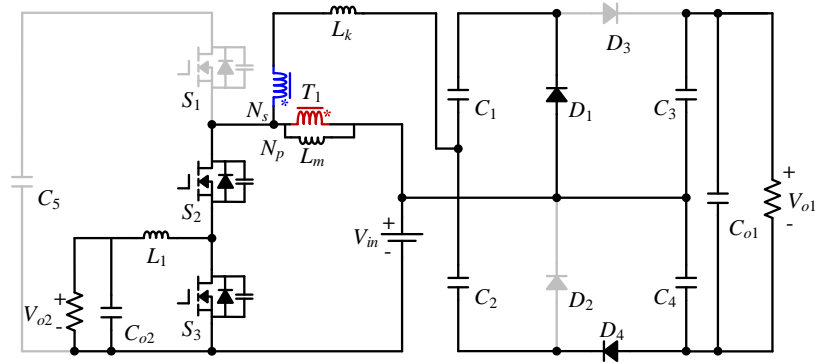
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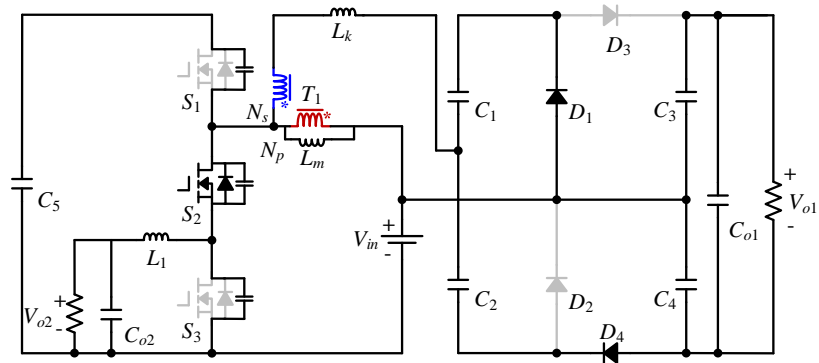
(h)

Figure 6.4 The equivalent circuits of the proposed converter in different operation modes: (a) Mode 1 [t_0-t_1]; (b) Mode 2 [t_1-t_2]; (c) Mode 3 [t_2-t_3]; (d) Mode 4 [t_3-t_4]; (e) Mode 5 [t_4-t_5]; (f) Mode 6 [t_5-t_6]; (g) Mode 7 [t_6-t_7]; (h) Mode 8 [t_7-t_8].

Mode 1 [t_0-t_1]: At time t_0, switch S_1 is turned on. Filter inductor L_1 is charged, and the power is transferred from input to output V_{o2}. Current i_{Lk} recovers to zero until time t_1 since the leakage inductance exists. The secondary side of coupled inductor and C_3 are in series connection to charge C_4 through diode D_4. Additionally, capacitor C_1 is charged through D_1.

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = V_{c5} - V_{o1} \\[2mm] L_m \dfrac{di_{Lm}}{dt} = (V_{c5} - V_{in}) \\[2mm] L_k \dfrac{di_{Lk}}{dt} = \dfrac{V_{c5} - V_{in}}{n} + V_{C2} - V_{C4} \\[2mm] L_k \dfrac{di_{Lk}}{dt} = \dfrac{V_{c5} - V_{in}}{n} - V_{C1} \end{cases} \tag{6.1}$$

Mode 2 [t_1-t_2]: After time t_1, current i_{Lk} keeps increasing and becomes positive. Therefore, diodes D_1, D_4 are reverse biased and diodes D_2, D_3 are forward biased. Capacitor C_1 and source V_{in} charge the capacitor C_2. Additionally, C_3 is charged by the current commuting from D_3.

$$L_k \frac{di_{Lk}}{dt} = \frac{V_{c5} - V_{in}}{n} + V_{C1} - V_{C3} = \frac{V_{c5} - V_{in}}{n} - V_{C2} \tag{6.2}$$

Mode 3 [t_2-t_3]: At time t_2, S_2 is turned off. Then, the parasitic capacitor of S_2 is charged, and that of S_3 is discharged.

Mode 4 [t_3-t_4]: At time t_3, S_3 is turned on. The power stored in L_1 is discharged to the output V_{o2} until switch S_3 is off.

$$L_1 \frac{di_{L1}}{dt} = -V_{o2} \tag{6.3}$$

Mode 5 [t_4-t_5]: Switch S_1 is turned off at t_4. The voltage of S_1 is reduced to zero, and that of S_2 is increased to a high level due to the primary side current i_p and leakage inductance current i_{Lk}.

Mode 6 [t_5-t_6]: Switch S_2 is turned on at time t_5. The current i_{Lk} starts to reduce. Owing to the leakage inductance of the coupled inductor, i_{Lk} reaches zero at t_6.

$$\begin{cases} L_m \dfrac{di_{Lm}}{dt} = -V_{in} \\[2mm] L_k \dfrac{di_{Lk}}{dt} = \dfrac{-V_{in}}{n} + V_{C1} - V_{C4} = \dfrac{-V_{in}}{n} - V_{C2} \end{cases} \tag{6.4}$$

Mode 7 [t_6-t_7]: After t_6, the current of leakage inductance becomes negative. Diodes D_1, D_4 are forward biased. The power is delivered from the input source and capacitor C_3 to capacitor C_4, and capacitor C_1 is charged.

$$L_k \frac{di_{Lk}}{dt} = \frac{-V_{in}}{n} + V_{C2} - V_{C4} = \frac{-V_{in}}{n} - V_{C1} \tag{6.5}$$

Mode 8 [t_7-t_8]: At t_7, switch S_3 is turned off so that the power stored in the parasitic capacitor of S_1 is transferred to that of S_3. Hence, switch S_1 can realise ZVS at t_8.

6.2.2 Voltage Gain

To simplify the calculation, the effect of leakage inductance L_k is ignored. According to the voltage-second balance of the primary side of coupled inductor, the voltage of capacitor C_5 can be derived as:

$$V_{c5} = \frac{V_{in}}{D_{s1}} \tag{6.6}$$

D_{S1}~D_{S3} are the duty cycles of switches S_1~S_3. Then, according to the voltage-second balance of inductor L_1, the buck stage output voltage is obtained as:

$$V_{o2} = (1 - D_{s3})V_{c5} \tag{6.7}$$

According to the operation characteristics of the voltage multiplier [210], the voltages of C_1 and C_2 are obtained as shown in Eq.(6.8) since C_1 is charged with the voltage V_{in}, and C_2 is charged with the voltage $V_{C5}-V_{in}$.

$$\begin{cases} V_{c1} = (1 + \frac{N_s}{N_p})V_{in} \\ V_{c2} = (1 + \frac{N_s}{N_p})(V_{c5} - V_{in}) \end{cases} \tag{6.8}$$

Hence, the voltages of capacitors C_3, C_4, and the boost stage output voltage are calculated by the following two equations.

$$V_{c3} = V_{c4} = V_{c1} + V_{c2} \tag{6.9}$$

$$V_{o1} = V_{c3} + V_{c4} \tag{6.10}$$

Therefore, the voltage gain of two outputs is presented.

$$\begin{cases} G_{boost} = \dfrac{V_{o1}}{V_{in}} = \dfrac{2}{D_{s1}}(1 + \dfrac{N_s}{N_p}) \\[4mm] G_{buck} = \dfrac{V_{o2}}{V_{in}} = \dfrac{1 - D_{s3}}{D_{s1}} \end{cases} \qquad (6.11)$$

6.3 Design Consideration and Analysis

6.3.1 Design Consideration

The inductor value is decreased with an increment of inductor ripple current. Then, the volume of the inductor will be smaller when the inductance is reduced since fewer turns of winding and a smaller core could be installed. However, with a broad inductor ripple, the corresponding output capacitor must have a sufficiently high ripple current rating, or the capacitor will overheat and dry out. Therefore, the capacitor size is increased with the increment of inductor ripple current. Additionally, the switch conduction loss is also increased because the RMS current of switch climbs with inductor current ripple. Moreover, too large inductor ripple current may cause saturation effects. On the contrary, a lower inductor ripple current will increase the inductor size.

In this design, the current ripple of filter inductor L_1 is set as 20%, a typical industry applied ripple current range, of its average current value I_{L1}, which is $\Delta i_{L1} \leq 0.2 I_{L1}$ [211]. Then, the value of filter inductor L_1 can be calculated based on Eq.(6.12).

$$L_1 = \frac{V_{o2}}{0.2 \cdot I_{L1}} \cdot t_s \cdot D_{S3} \qquad (6.12)$$

Where $I_{L1} = P_{o2}/V_{o2}$ and P_{o2} is the buck stage output power. Similarly, the current ripple of magnetic inductance L_m is also limited to 20% of the average current value I_{Lm}. Then, the value of magnetic inductance can be obtained as:

$$L_m = \frac{V_{C5} - V_{in}}{0.2 \cdot I_{Lm}} \cdot t_s \cdot D_{S1} \qquad (6.13)$$

$$I_{Lm} = \frac{P_{o1} + P_{o2}}{V_{in}} \qquad (6.14)$$

In the loop consisting of capacitor C_5 and three switches $S_1 \sim S_3$, there is only one switch in the off-state when the converter is not operating in modes 3, 5, and 8. Hence, the voltage stress of three switches can be calculated by Eq.(6.15) based on Eq.(6.6):

$$V_{S1\_MAX} = V_{S2\_MAX} = V_{S3\_MAX} = V_{c5} = \frac{V_{in}}{D_{s1}} \tag{6.15}$$

According to Eq. (6.11) and (6.15), the voltage stress of switches is lower than half of the voltage of boost output V_{o1} as $V_{si\_MAX} < 0.5 V_{o1}$. Therefore, the high voltage step-up ratio with low voltage stress of switches is achieved so that switches with low on-state resistance could be installed, and hence the conduction loss of switches is reduced [212].

6.3.2 Reduced Switch Count

Compared with conventional two SISO converters shown in Fig 6.5, the proposed converter illustrated in Fig 6.2 can use one less switch to achieve almost the same performance by integrating switches S_{11} and S_{21}. Hence, the cost is reduced.
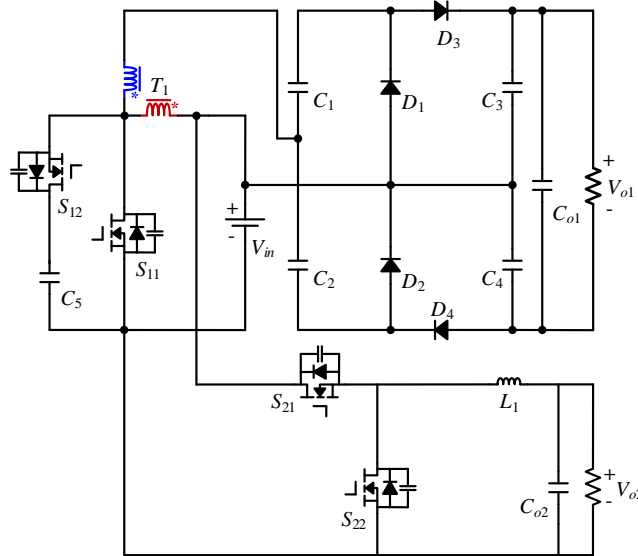
Figure 6.5 Topology of two SISO converters.

6.3.3 ZVS Operation

To achieve ZVS operation of switches, a proper dead zone t_{ds} is set between the turn-on and turn-off periods of two different switches as the intervals t_2-t_3, t_3-t_4, and t_7-t_8 so that the drain-to-source voltages of switches can drop to zero when the corresponding switch is turned on. Additionally, the drain-to-source currents of

switches should be negative when they are turned on, which indicates that their freewheeling diodes are forward biased. For example, the ZVS operation of switch S_3 is illustrated in Fig 6.6. The drain-to-source voltage V_{ds3} starts to decrease when switch S_2 is turned off at time t_2, and reaches zero at $t_{2'}$. Therefore, switch S_3 can be turned on with zero voltage at t_3, and $t_{ds} = t_3 - t_2$. Additionally, the drain-to-source current ids_3 becomes negative since t_2 because the parasitic capacitance of S_3 is discharged. Moreover, the value of ids_3 is required to be lower than zero before t_3 to ensure that S_3 is not charged.
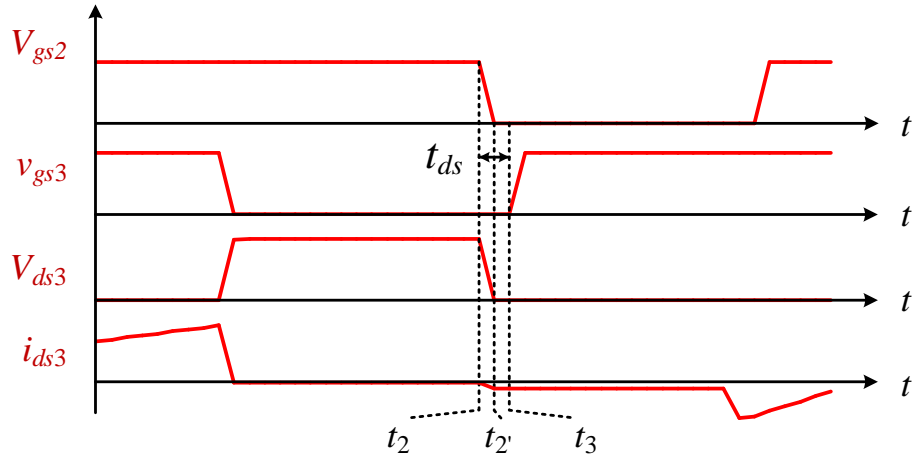
Figure 6.6 ZVS operation of switch S_3.

According to the operation modes 3, 5 and 8, the currents $i_{ds1} \sim i_{ds3}$ at the time when switch $S_1 \sim S_3$ are turned on are obtained.

$$\begin{cases} i_{ds1}(t_0) = -[i_{L1}(t_0) + i_{Lm}(t_0) - (N_s / N_p + 1)i_{Lk}(t_0)] \\ i_{ds2}(t_5) = -[(N_s / N_p + 1)i_{Lk}(t_5) - i_{Lm}(t_5)] \\ i_{ds3}(t_3) = i_{L1}(t_3) \end{cases} \qquad (6.16)$$

Eq.(6.17) is derived from Eq.(6.16) when $i_{ds1}(t_0) < 0$.

$$1.2I_{Lm} - i_{Lk}(t_0)(1 + \frac{N_p}{N_s}) > 0.8I_{L1} \qquad (6.17)$$

To ensure the ZVS operation of switch S_1, the current I_{Lm} should be large enough so that $i_{ds1}(t_0)$ is negative. In the experimental design, the boost stage output is 200 V/1 A, and the buck stage output is 24 V/2 A so that I_{Lm} is larger than I_{L1}. Additionally, the current of leakage inductance i_{Lk} is negative at time t_0, and i_{L1} is always negative during

the operation. Hence, the ZVS operation of switches S_1 and S_3 is realised. Furthermore, to achieve $i_{ds2}(t_5)<0$ in Eq.(6.16), Eq.(6.18) is obtained.

$$L_k > \frac{V_{in} \cdot (1+\frac{N_s}{N_p}) \cdot t_{ds}}{i_{Lk}(t_3) - \frac{0.8 \cdot I_{Lm}}{1+\frac{N_s}{N_p}}} \tag{6.18}$$

Therefore, all the three switches can achieve ZVS operation, and the switching loss is significantly reduced. In practical operation, the discharge time of switches S_1 and S_3 will be increased with the increase of switching frequency due to the smaller discharge current and larger drain-to-source voltage. Hence, it will be more challenging for the proposed converter to achieve ZVS operation of all switches with the increase of switching frequency. Additionally, with a set value of leakage inductance, a significant reduction of I_{Lm} caused by the variation of P_{o1} may affect the ZVS operation of S_1 and S_2.

6.3.4 Closed Loop Control

According to Eq.(6.11), the output voltages V_{o1} and V_{o2} are regulated by the duty cycles D_{S1} and D_{S3}. Therefore, two individual PI compensators PI$_1$ and PI$_2$ are installed to generate the two control variables D_1, D_3 to obtain control signals v_{gs1} and v_{gs3} as depicted in Fig 6.7 (a). Furthermore, the control signal v_{gs2} is generated based on v_{gs1} and v_{gs3} as $v_{gs2}=v_{gs1}$XORv_{gs3}. From Fig 6.7, the relationship between duty cycles D_{S1}~D_{S3} and control variables D_1, D_3 is shown as Eq.(6.19).

$$\begin{cases} D_{S1} = 1 - D_1 \\ D_{S2} = D_1 + D_3 \\ D_{S3} = 1 - D_3 \end{cases} \tag{6.19}$$

As illustrated in Fig 6.7 (b), the control singles of S_1 and S_3 are obtained from the comparison of control variables D_1, D_3, and the sawtooth wave V_t as (1−D_1, V_t) and (V_t, D_3) respectively. When 1−D_1 is smaller than V_t, S_1 is on. When D_3 is larger than V_t, S_3 is on. Furthermore, S_2 is in the on-state when 1−D_1 is larger than V_t, and D_3 is smaller than V_t.

(a)

(b)
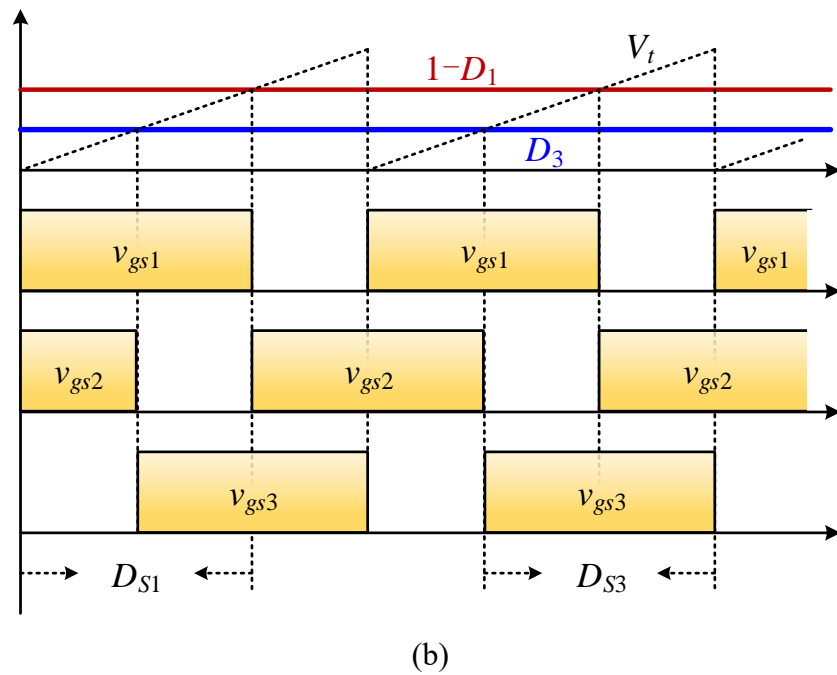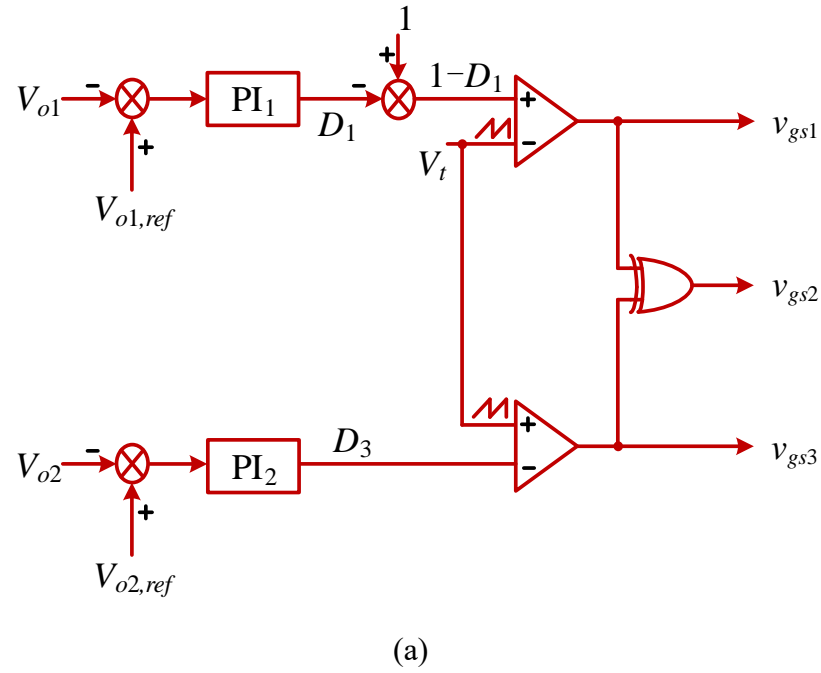
Figure 6.7 Control system: (a) scheme; (b) drive signals generation.

6.4   Experiment Verification and Comparison Results

6.4.1   Hardware

In order to verify the performance and theoretical analysis of the proposed converter, the prototype circuit with 48 V input and the boost output V_{o1} 200 V/1 A as well as the buck output V_{o2} 24 V/2 A is built as shown in Fig 6.8, which consists of the main

circuit and the digital signal processor control circuit. The parameters of the prototype are listed in Table 6.1. Three MOSFETs IPP530N15N3 and four Schottky diodes DST5200 are employed in the proposed circuit to achieve high power efficiency and better performance. Besides the prototype and control circuit, one main power source, two auxiliary power sources, two electronic power load, and the oscilloscope are applied to conduct the experiment. The parameters of PI compensators in Fig 6.7 are shown in Eq.(6.20).

$$\begin{cases} \mathrm{PI}_1 = 0.025 + \dfrac{0.001}{s} \\ \mathrm{PI}_2 = 0.02 + \dfrac{0.01}{s} \end{cases} \tag{20}$$
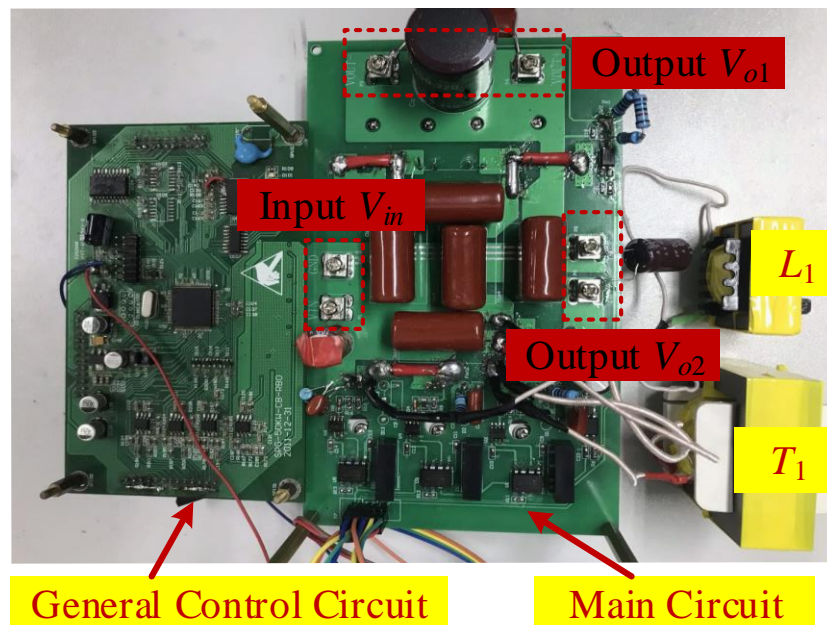
Figure 6.8 Photograph of SIDO circuit prototype.

Table 6.1 Parameter Specifications.

Symbol	Definition	Value
V_{in}	Input voltage	48 V
V_{o1}/V_{o2}	Output voltage for boost/buck stage	200 V/24 V
I_{o1}/I_{o2}	Output currents for boost/buck stage	1 A/2 A
$P_{o,\max}$	Output power	248 W
f_s	Switching frequency	150 kHz
$C_1{\sim}C_5$	Clamp capacitors	10 µF
Magnetic components:		
L_1	Filter inductor	196.48 µH
T_1	Coupled inductor	/
L_m	Magnetic inductance	129 µH
L_k	Leakage inductance	22.1 µH
$N_p{:}N_s$	Turns ratio	10:13
Semiconductor components:		
$D_1{\sim}D_4$	DST5200	/
$S_1{\sim}S_3$	IPP530N15N3	/

6.4.2   Experiment Results

In Fig 6.9, the steady-state output currents and voltages are shown. Compared with the 48 V input voltage, the output V_{o1} has a high voltage step-up conversion ratio with the 200 V output voltage, and the output V_{o2} has a buck voltage level of 24 V. Hence, simultaneous buck and boost output voltages are obtained.

The steady-state waveforms consisting of the primary side current i_p, leakage current i_{Lk}, and filter inductor current i_{L1} are shown in Fig 6.10 to illustrate the power flow of the proposed converter. The power delivered to V_{o1} and V_{o2} is controlled by switches S_1 and S_3 respectively according to the charge and discharge operation of currents i_{Lk} and i_{L1}. Due to the leakage inductance, the current i_{Lk} cannot reach zero immediately with the turn-on and turn-off of switch S_3. Additionally, the current i_p is negative, and i_{Lk} is positive when switch S_2 is turned on so that Eq.(6.16) is achieved.
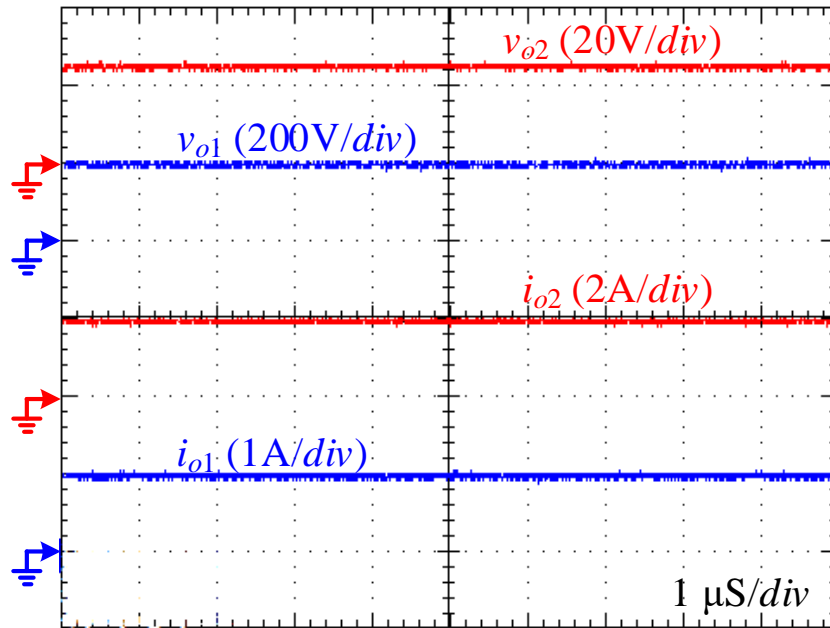
Figure 6.9 Voltages and currents of two outputs.
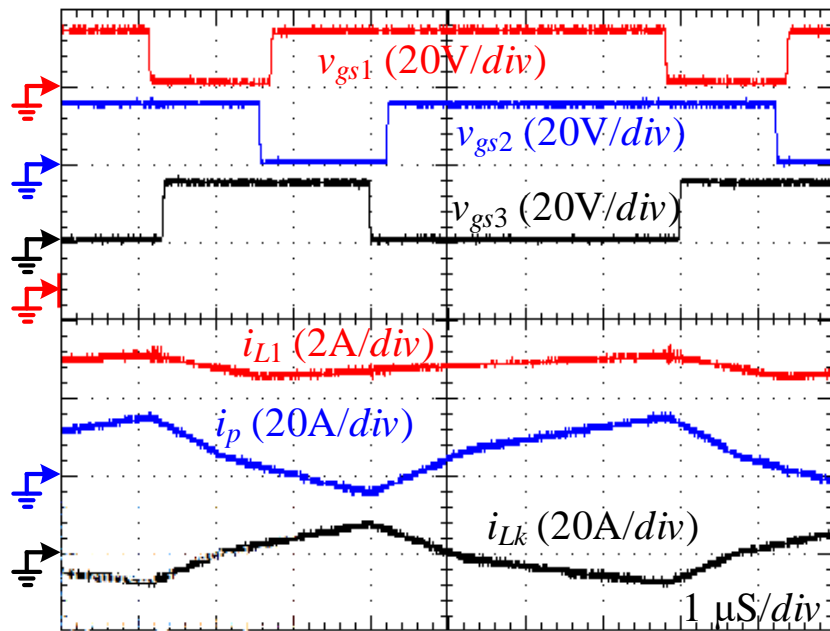
Figure 6.10 Experimental waveforms of drive signals $v_{gs1} \sim v_{gs3}$, the inductor current i_{L1}, the primary side current i_p, and the leakage inductance current i_{Lk}.

The drive signals, drain-to-source voltages, and drain-to-source currents of three switches $S_1 \sim S_3$ at the full load condition are depicted in Fig 6.11 to present the ZVS operation of all switches. It can be found that the drain-to-source voltages $v_{ds1} \sim v_{ds3}$ are reduced to zero before the turn-on of the corresponding switch. Moreover, the drain-to-source currents $i_{ds1} \sim i_{ds3}$ are negative when switches $S_1 \sim S_3$ are turned on respectively,

which indicates that the freewheeling diodes of switches are forward biased to conduct the switches. Therefore, the switching loss of switches is significantly reduced. Furthermore, the voltage stress of switches is lower than half of the boost stage output voltage shown in Fig 6.9. Hence, the conduction loss of switches is also reduced.
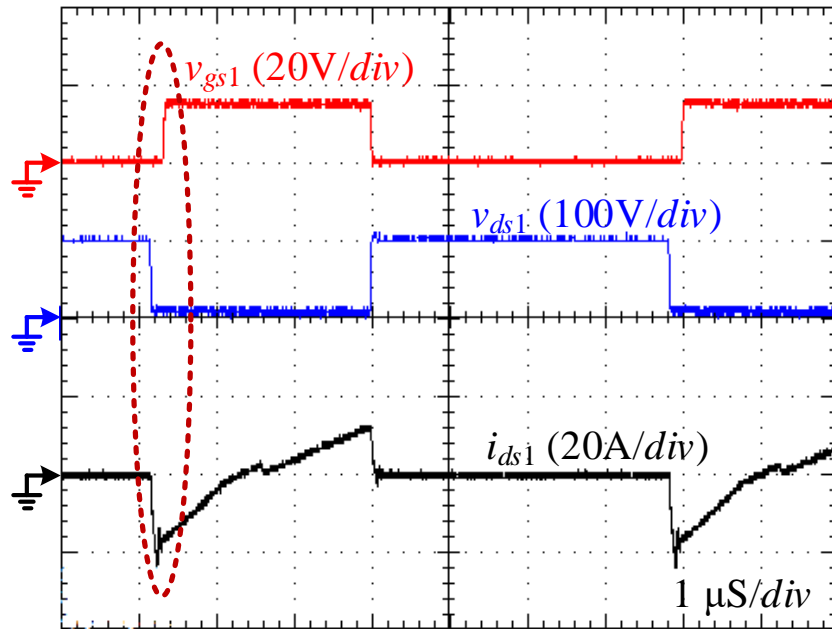
(a)
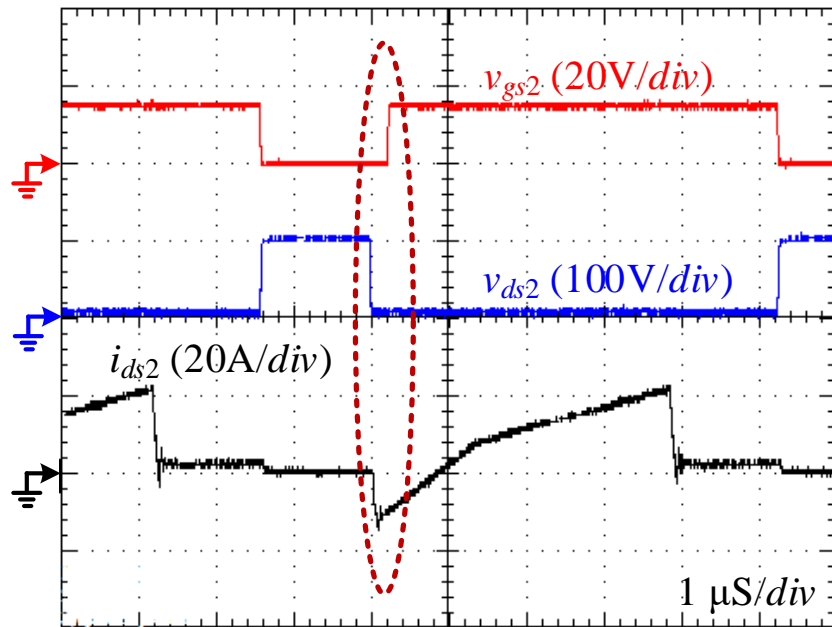
(b)
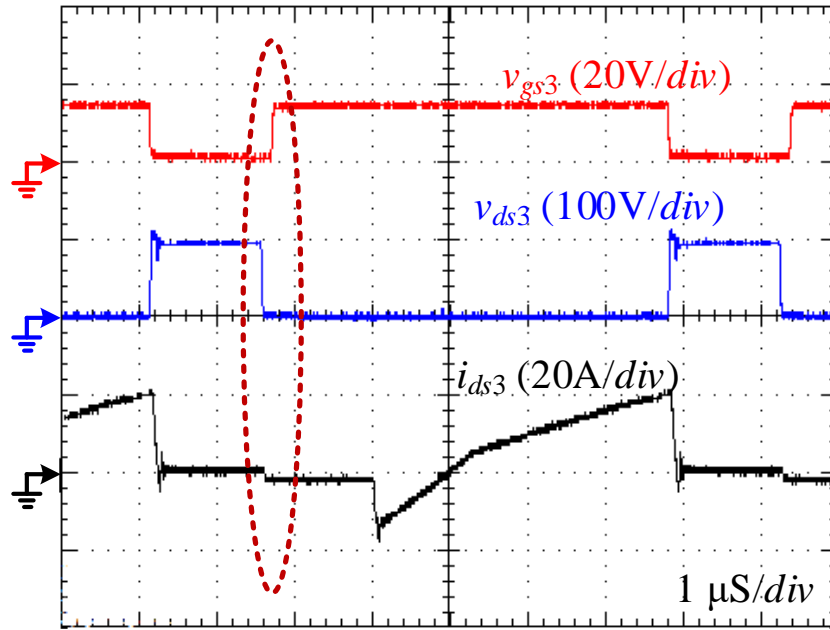
(c)

Figure 6.11 ZVS operation of switches: (a) S_1; (b) S_2; (c) S_3.

Then, the voltages and currents of four diodes $D_1 \sim D_4$ are given in Fig 6.12, which illustrates the operation of the voltage multiplier circuit. The diodes D_1, D_4 are conducted when the other two diodes D_2, D_3 are reverse biased. Then, all experimental results are coincidence with the operation analysis and design consideration.

The transient response of two outputs with the load variation shown as the output currents i_{o1} and i_{o2} that changes from 100% to 50% and from 50% to 100% are given in Fig 6.13. Then, the specific voltage variations caused by cross regulation, and the ratio of voltage error over the rated value are listed in Table 6.2. When i_{o2} is changed from 100% to 50%, the voltage undershoot of v_{o1} is 0.92 V; when i_{o2} is changed from 50% to 100%, the voltage overshoot of v_{o1} is 3.09 V. Compared with the rated value as 200 V, the corresponding voltage error ratios are 0.92% and 1.55%, which is low and shows a good cross regulation performance. Likewise, the voltage error ratios of v_{o2} are also low with the variation of i_{o1}. With the small voltage error ratio, the proposed converter has improved cross regulation performance.

The power efficiency during the interval from $(0.1I_{o1}, 0.1I_{o2})$ to (I_{o1}, I_{o2}) illustrated in Fig 6.14 are measured based on the prototype shown in Fig. 6.8, where the power efficiency=P_{out}/P_{in}=$(V_{o1} \cdot I_{o1} + V_{o2} \cdot I_{o2})/(V_{in} \cdot I_{in})$. In the figure, the efficiency is larger than

90% over the most of load range, and the maximum efficiency 96.6% is achieved at I_{o1}=0.1 A, I_{o2}=2 A.
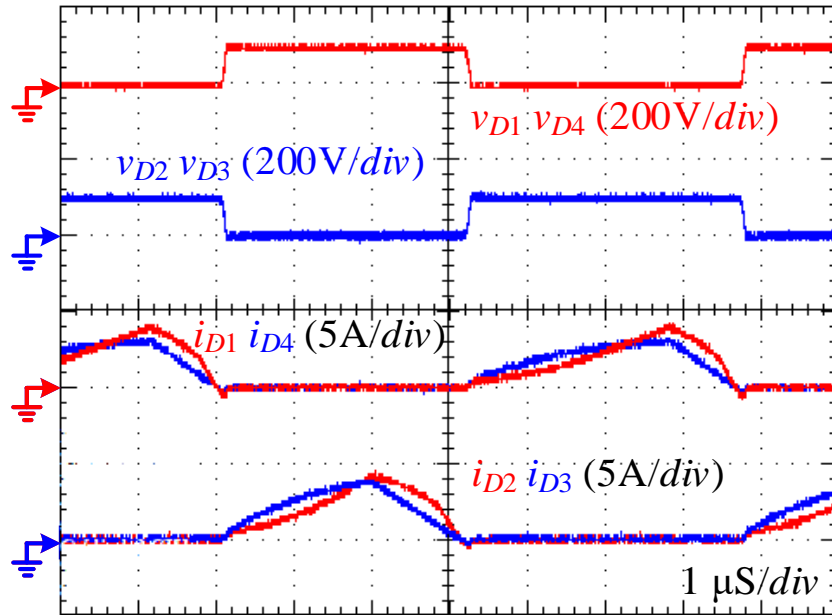
Figure 6.12 Voltages and currents of diodes $D_1 \sim D_4$.
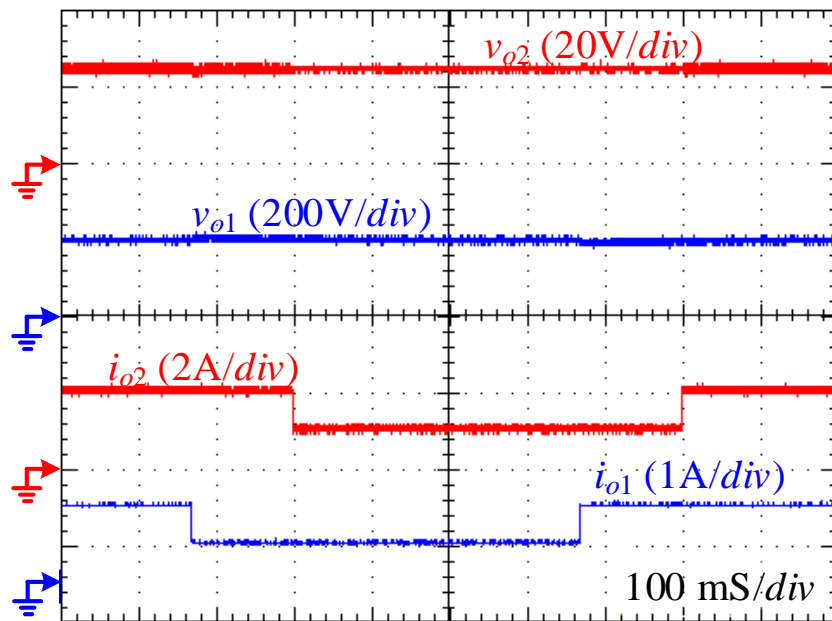
Figure 6.13 Dynamic response with load variation from 100% to 50%.
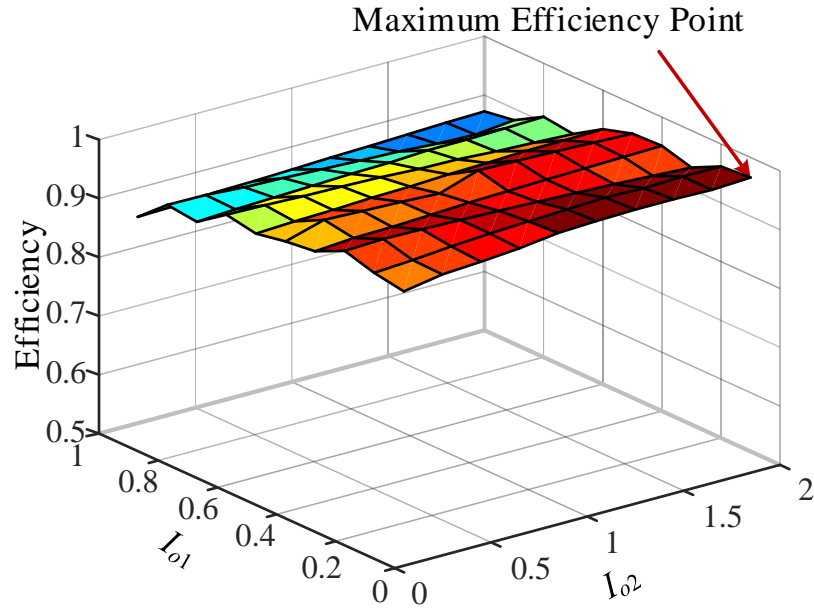
Figure 6.14 Measured efficiency as a function of output current I_{o1} and I_{o2}.

Table 6.2 Cross regulation performance.

Output	Voltage Undershoot	Voltage Error Ratio	Voltage Overshoot	Voltage Error Ratio
V_{o1}	1.83 V	0.92%	3.09 V	1.55%
V_{o2}	0.07 V	0.29%	0.05 V	0.21%

6.4.3   Comparison Results

Table 6.3 shows the comparison results in terms of operation parameters, active switch count, voltage stress of switches, ZVS operation, power efficiency, and cross regulation performance among the proposed converter and other typical SIDO converters, where the cross regulation performance is compared according to the voltage error ratio, and V_{MAX} equals to the maximum voltage value among the input voltage as well as two output voltages.

Because there is one control variable, only one output voltage is regulated, and the voltage error of the unregulated output port reaches 22.4% of its rated output voltage [185]. For single-inductor dual-output converters in [195, 198], the cross regulation is improved owing to the installation of SSPRs by applying external control variables and complex control circuits. The voltage error ratios are reduced to 10% and 2.5% separately [195, 198]. However, the cross regulation of single–inductor dual-output

converters is still deficient because the currents of both outputs flow through the same inductor, and both output voltages are step-down. Furthermore, high voltage stress and hard-switching result in low power efficiency.

The integrated converter uses six switches to obtain multiple control variables as well as independent power flow to improve the cross regulation [202]. The corresponding ratio is decreased to 0.47%, which is better than that of the proposed converter [202]. Furthermore, it also has a high power efficiency beyond 95% [202]. Nevertheless, it can only supply two step-down output voltages, and the installation of six switches results in high cost [202]. For the SIDO converter based on Ćuk converter [206], it can obtain both buck and boost output stages simultaneously with improved cross regulation performance owing to independent power flow and two control variables. The voltage error ratio is not given in the table due to the lack of detailed information. However, the power efficiency is low as 91.3% due to high voltage stress and hard-switching of switches [206]. Although the three-level DC/DC converter reaches a high power efficiency as 95.9%, the voltage error ratio is increased to 11.5% so that the cross regulation performance is reduced [209].

From the aforementioned operation principles and performance analysis, the proposed SIDO converter can achieve improved cross regulation performance, high power efficiency, and simultaneous boost as well as buck output voltages. According to Table 6.3, the low voltage error ratio as 1.55% indicates improved cross regulation performance owing to multiple control variables and independent power flow. Additionally, maximum power efficiency as 96.6% is realised due to low voltage stress and ZVS operation of all switches.

Table 6.3 Comparison of the proposed and other SIDO converters.

References	Input voltage	Output voltage V_{o1}	V_{o2}	Output power (full load)	Switch Count	Conversion ratios V_{o1}/V_{in}	V_{o2}/V_{in}	Voltage stress of switches	ZVS	Efficiency	Voltage error ratio
[185]	170 V	5 V	6.7 V	1 W	4	Step-down		>V_{max}	NO	/	22.4%
[195]	20 V	8 V	12 V	39 W	2	Step-down		V_{max}	NO	83.1%	2.5%
[198]	30 V	8 V	21 V	25 W	3	Step-down		V_{max}	NO	86%	10.0%
[202]	100 V	28 V	42 V	420 W	6	Step-down		V_{max}	YES	96.5%	0.47%
[206]	48 V	24 V	156 V	252 W	2	$\dfrac{D_{s1}+D_{s2}-1}{1-D_{s1}}$	$\dfrac{D_{s1}-1}{1-D_{s1}}$	V_{max}	NO	91.3%	Good
[209]	60 V	36 V	125 V	200 W	2	$\dfrac{1-D_{s1}}{2-D_{s1}-D_{s2}}$	$\dfrac{1}{2-D_{s1}-D_{s2}}$	$V_{max}/2$	YES	95.9%	11.5%
Proposed	48 V	24 V	200 V	248 W	3	$\dfrac{1-D_{s3}}{D_{s1}}$	$\dfrac{2}{D_{s1}}(1+\dfrac{N_s}{N_p})$	<$V_{max}/2$	YES	96.6%	1.55%

6.5   Summary

This paper presents a novel integrated SIDO converter consisting of a buck converter and a voltage multiplier circuit, which has advantages as simultaneous buck and boost output voltages, improved cross regulation performance, and high power efficiency. The operation analysis, design consideration, experiment verification, and comparison are discussed in detail.

Compared with two SISO converters, the proposed topology uses one less active switch to obtain the same capability, such as independent step-up and -down output voltages at the same time. The improved cross regulation performance is obtained owing to independent power flow and two control variables for two outputs. The independent power flow is realised by the inductor L_1 as well as the coupled inductor T_1, and two control variables are obtained from the two individual PI compensators. Thanks to the voltage multiplier circuit, a high voltage step-up ratio is achieved with low voltage stress of active switches, so that conduction loss of switches is reduced. Furthermore, all switches can achieve ZVS operation, which reduces the switching loss significantly. With low conduction loss and switching loss of switches, the proposed converter obtains a high power efficiency. Finally, the experiment results based on the prototype with 48 V input and 200 V/1 A, 24 V/2 A outputs are measured to verify both steady-state and transient theoretical analysis.

Chapter 7. CONCLUSION

7.1 Summary

In this thesis, DC/DC converters for power conversion systems consisting of RESs and ES (battery) have been introduced in detail. The techniques of increasing voltage step-up conversion ratio have been studied, analysed, and applied in four converters as the multi-module converters, the LED driver, and the SIDO converter. Besides the main objective as high voltage step-up ratio, the designed converters also achieve other advantages such as high switching frequency, high power efficiency, low cost, and so on. The following five characteristics are highlighted in the converter design to improve their performance:

- high voltage step-up conversion ratio without extreme duty cycle of switches;
- low voltage/current rating of semiconductor components;
- soft-switching operation of switches;
- small volume;
- low component count.

Two multi-module converters that are applied in HVDC transmission systems have been designed and introduced. The design could achieve the high voltage step-up conversion ratios with a low voltage/current rating of semiconductor components to meet the high power and voltage level of HVDC transmission systems. The matrix configuration could increase output voltage and power by adding the number of SMs. Furthermore, two novel topologies of SMs further increase voltage gain and meet the specific requirements of power transmission of offshore wind farms and large scale solar plants. A LED driver has been proposed and verified, which can provide power for high illuminance portable LED applications with desired high power efficiency and small volume. The design uses one less active switch to obtain a similar operation as that of employing two conventional converters. Additionally, the ZVS operation and passive CBC have improved the power efficiency of the designed converter. A SIDO converter is proposed for power conversion systems with two different output voltages, which can alleviate cross regulation problems occurred to the two outputs. The output voltage error caused by load variation and external disturbances of other outputs is

reduced to ensure the stable operation of the power conversion system. Additionally, the designed topology can also achieve simultaneous buck and boost output stages, high voltage step-up conversion ratio, low cost, and high power efficiency.

In chapter 2, a literature interview about the voltage step-up DC/DC converter has been presented. The merits and drawbacks of the conventional topologies have been introduced, analysed, and compared. The basic knowledge of previous work will help readers to understand the derivation and design consideration of the proposed converters.

Chapter 3 introduces the design and simulation results of the multi-module converter applied in HVDC transmission of offshore wind farms. Due to the matrix configuration, the multi-module converter can meet the requirements as high power and ultra-high voltage level. Owing to the modularity, the high DC transmission line voltage and the bulky power is achieved by merely adding SMs without increasing rated voltage/current of semiconductor components. Additionally, the multi-module converter can achieve a higher voltage step-up ratio than MMCs, since it has two degree of freedom to enlarge the voltage gain due to the installation of CFPP SMs. It presents another choice besides MMCs and should be valuable for the converter topology design of HVDC transmission systems. The performance of the proposed model is compared with current popular DC/DC converters applied in HVDC transmission systems, and the simulation results verify the advantages such as high voltage step-up conversion ratios, flexible control, and improved fault tolerance capability.

Chapter 4 introduces a TPC operating as the SM in the multi-module converter to integrate HVDC transmission systems and batteries to compensate the generation fluctuations of RESs. The proposed TPC serves as the interface among the PV panel, battery, and output port. With proper control, the battery is charged when the generated power is more than consumed, and the battery is discharged to enable a stable operation when the generated power is less than the required power. The design of the TPC and multi-module converter is verified by simulation.

In chapter 5, a multi-output LED driver is proposed for portable high illuminance LED applications. The recommended LED driver uses one less switch to achieve similar operation as applying two switched capacitor converters. The integration of

switched capacitor and transformer enlarges the voltage gain. Besides that, soft-switching of switches is realised by using transformers to form the resonant tank consisting of the switched capacitor and magnetic inductance of the transformer. Additionally, the low voltage stress of active switches is obtained due to the installation of transformers. Hence, high power efficiency is achieved. Moreover, the designed converter has a small volume due to the high switching frequency.

Chapter 6 presents the design method to alleviate the cross regulation problem of multi-output converters. The derivation, design, and experiment results of a SIDO converter consisting of three active switches have been discussed in this chapter. Compared with conventional two SISO converters, the proposed converter can use one less switch to achieve almost the same performance by integrating two switches. Thanks to the two control variables, each output voltages could be controlled individually. Additionally, the voltage error is further reduced due to the independent power flow that reduced the effect from other output ports. Furthermore, due to the independent power flow, simultaneous buck as well as boost output voltages are realised. Owing to the use of a voltage multiplier circuit, a high step-up voltage conversion ratio is achieved with relatively low voltage stress of switches, so that conduction loss of switches is reduced. Additionally, all switches can perform ZVS operation by the installation of magnetic components, which contributes to a significant switching loss reduction.

7.2   Key Contributions

The key contributions of each chapter are listed below:

1. Chapter 1&2: Background and literature review

The application background and motivation have been presented. Additionally, a comprehensive literature review of techniques to enlarge voltage conversion ratio has been introduced and discussed.

2. Chapter 3: Multi-module converter for HVDC transmission of offshore wind farms

Instead of MMCs, the idea of multi-module converters presents another choice for HVDC transmission systems. The proposed multi-module converter can achieve high

power and voltage level with low voltage stress as well as low current rating of semiconductor components so that it can meet the requirements of HVDC transmission. Compared with MMCs, the CFPP SMs provides another degree of freedom to enlarge the voltage gain by two times. Furthermore, the design of CFPP topology can realise the automatic current balancing of different SMs. Additionally, the high operation frequency as 5 kHz can keep small size of passive components. Simulation results have shown the feasibility of the proposed multi-module converter.

3. Chapter 4: Multi-module converter for HVDC transmission of large scale solar plants

A TPC is designed as SMs of the multi-module converter introduced in the last chapter to integrate HVDC transmission and ES. Then, RESs such as solar power are delivered to the unity grid through HVDC transmission in conjunction with ES systems that can compensate the generation fluctuations of RESs, and improve the reliability as well as the efficiency of the overall system. Besides that, fault tolerance capability is enhanced by adding thyristors to prevent diodes in the secondary circuits from damage under DC fault condition.

4. Chapter 5: LED driver for portable high illuminance LED applications

This chapter presents a LED driver that can use one less switch to achieve similar operation as that of using two switched capacitor converters. The derivation, design consideration, and experiment results of the prototype are presented. 50 kHz operation frequency do favour of reducing passive components size. With the capacitor-based CBC, the currents through different LED strings are auto-balanced. Instead of installing inductor-based CBCs, currents through different LED strings are balanced even with manufacturing faulty of components. All switches can achieve ZVS operation so that the switching loss is significantly reduced. For high illuminance LED applications as 100 W, the proposed LED driver can achieve a high power efficiency as 94.6%. Compared with previously announced works, the proposed LED driver can provide a better performance in terms of high power efficiency and current auto-balance. Experiment results have verified the merits and application prospect of the designed LED driver.

5. Chapter 6: SIDO converter for EV

A SIDO converter with improved cross regulation performance has been introduced in this chapter. With multiple control variables and independent power flow, the proposed SIDO converter has a maximum voltage error ratio as 1.66% that is much smaller than 22.4% without the proposed techniques. Additionally, other methods do improve cross regulation performance, while with the sacrifice of desired advantages such as low cost and high power efficiency. The proposed one can use one less switch to achieve almost the same performance as that of using two SISO converters. Moreover, all switches can obtain low voltage stress and ZVS operation, so that conduction loss and switching loss of switches are reduced. Then, the efficiency is larger than 90% over the most of load range, and the maximum efficiency 96.6% is achieved at I_{o1}=0.1 A, I_{o2}=2 A. The overall performance is better than any previously announced work, and the proposed method has shown a potential in applications such as EV, DC micro-grids, and some renewable power conversion systems.

7.3   Future Work

Based on the limitations of the proposed researches, future work could be carried out as follows.

Due to the limited experiment condition, the operating characteristics of two multi-module converters are only verified by simulation results. Therefore, their experiments with small amount of SMs could be conducted on in the future to improve the performance of this configuration in terms of fault-tolerant capability and output voltage ripple. Additionally, the control algorithms for the multi-module converters could be tested and enhanced by practical experiments.

The proposed topologies for low power applications only focus on the integration of switches to reduce cost, while the diodes and passive components count are still high. Low cost of power converters is one crucial consideration in applications. Therefore, further study could be focused on topology synthesis methods for developing multi-port converter with low price.

The literature provides the feasibility of increasing switching frequency to reduce components size. However, the high switching frequency will also bring some disadvantages, such as increasing power loss of transformers. Hence, the limitation of switching frequency should be further investigated. Additionally, further study of

DC/DC converters and the performance improvement in terms of compactness and power efficiency should be conducted via the design optimization and the comparison with current state-of-the-art topologies.

Switches have a significant current rating with the installation of coupled inductors and voltage multiplier circuits, which results in an increased conduction loss. Additionally, the power loss of coupled inductor is high due to the high current value. Therefore, further researches on gain extension cells could focus on the potential of improving power efficiency.

7.4 Publications Arising from this Research

Journal papers:

[1] **S. Song**, Y. Hu, K. Ni, J. Yan, G. Chen, H. Wen, and X. Ye, "Multi-Port High Voltage Gain Modular Power Converter for Offshore Wind Farms," *Sustainability*, vol. 10, no. 7, pp. 2176, 2018.

[2] **S. Song**, W. Li, K. Ni, H. Xu, Y. Hu, and J. Si, "Modular Multi-Port Ultra-High Power Level Power Converter Integrated with Energy Storage for High Voltage Direct Current (HVDC) Transmission," *Energies,* vol. 11, no. 10, pp. 2711, 2018.

[3] **S. Song**, K. Ni, G. Chen, Y. Hu, and D. Yu, "Multi-Output LED Driver Integrated with 3-Switch Converter and Passive Current Balance for Portable Applications," *Journal of Power Electronics*, vol. 19, no. 1, pp. 58-67, 2019.

[4] **S. Song**, G. Chen, Y. Liu, Y. Hu, K. Ni, and Y. Wang, "A Three-Switch-Based Single-Input Dual-Output Converter with Simultaneous Boost & Buck Voltage Conversion," *IEEE Trans. Ind. Inform.*, Accepted.

[5] T. Wu, W. Li, K. Ni, S. Song and M. Alkahtani, "Modular Tri-Port Converter for Switched Reluctance Motor based Hybrid Electrical Vehicles," *IEEE Access*, vol. 7, pp. 15989-15998, 2019.

Conference papers:

[6] **S. Song**, Y. Hu, G. Chen and K. Ni, "High reliability converter for LED torch," 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia), Kaohsiung, 2017, pp. 214-220.

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