DLFCR Reduction Based on Power Predictive Scheme for Full-bridge Photovoltaic Micro-inverter

Jiarong Kan, *Member, IEEE*, Yunya Wu, Yu Tang, *Senior Member, IEEE*, Lin Jiang, *Member, IEEE*

***Abstract*—This paper proposes a double-line-frequency current ripple (DLFCR) reduction strategy for PV micro-inverter. A power predictive scheme is established according to the output power mathematical model of prestage full-bridge DC/DC converter (PFDDC), which is the basis of the proposed DLFCR reduction strategy. The control effect is analyzed with considering parameters estimation error and the analysis results show that the proposed strategy has good dynamic performance and robust performance. The small signal model of the PFDDC has been established to design the voltage-loop parameters. The bandwidth of the system controlled by the power predictive scheme is large, which can effectively reduce the design complexity because no parameter is needed to design for power prediction. Experimental verifications are presented to verify the analysis.**

***Index Terms*—PV micro-inverter, DLFCR reduction, power prediction, current prediction, robust performance.**

I. INTRODUCTION

COMPARED with the centralized and the string photovoltaic (PV) generation system[1]-[2], PV AC module has been paid more and more attention due to the following advantages: mitigating the shading effect and mismatch problem, low installation cost, plug and play operation, high flexibility. The inverter used in AC module is called micro-inverter (MI) because of its low power, whose typical value is 100~300W [3]. A lot of researches have focused on improving the efficiency, reliability, topology and cost reduction, etc [4]–[25].

The most commonly used topology used in MI is based on flyback converter [9] or interleaved flyback converter [10]. With the increasing of photoelectric transformation efficiency, the output power of a single PV panel becomes large. The rated power of MI is 500W in [11]. Thus, MIs based on other topologies, which can easily achieve higher efficiency with higher power, are also studied, such as forward[12], half-bridge[13], current-fed and voltage-fed push-pull [14]-[15], current-fed isolated dual-boost[16], various kinds of resonant full-bridge converter [17]-[18].

The lifespan of MI should match lifespan of the PV cell. However, MI is usually operated in harsh environment, such as top of building or barren desert. The electrolytic capacitor is used to smooth the DC voltage but it decreases the lifespan of MI. The film capacitor has longer lifespan but its capacitance is too small with the same volume. Larger double-line-frequency current ripple (DLFCR) component will be included in output current of PV panel if the electrolytic capacitor is substituted by the film capacitor with smaller capacitance. The DLFCR will cause lower energy harvest of PV panel [19]. So, the DLFCR must be removed by proper control strategy or additional active power decoupling circuit (APDC) used to store the energy difference between PV panel and the grid.

According to [3], MI was classified into three categories: with pseudo DC-link[20], with DC-link[21] and without DC-link[22]. If MI has a pseudo DC-link or hasn't DC-link, the APDC must be inserted into the circuit to buffer the power different because there is no other element for energy storing in MI. There are two decoupling strategies to control the power flow between the PV panel, the APDC, and the AC grid. One is the whole PV power decoupling [23] and the other is sectional PV power decoupling [24]-[25]. The efficiency of MI with whole PV power decoupling is low due to its loss in APDC. The APDC in [24] is paralleled with the PV panel and it contains a boost converter with a synchronous switch. The power difference is controlled by the paralleled boost converter. Different from conventional power decoupling method, the scheme in [25] is discussed from the point of the current decoupling. The DLFCR can be well reduced by the APDC. However, the additional APDC increases the cost and complexity of MI and the efficiency is decreased due to the loss in APDC.

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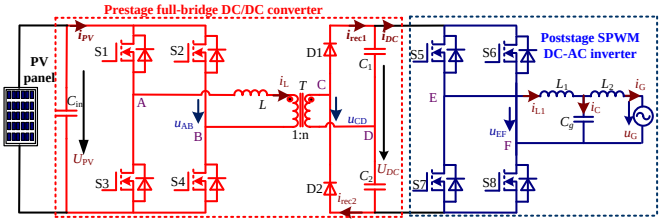


Fig. 1. The PV MI based on full-bridge converter.

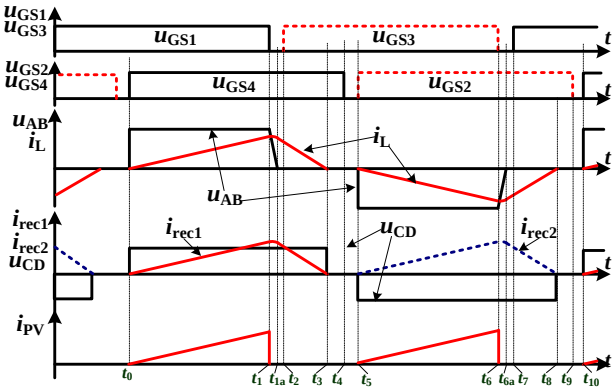


Fig. 2. Theoretical waveforms and switching time of the PFDDC. Note that u_{GS1} - u_{GS4} represent control signal of relative switches, u_{AB} is the output voltage across point A and point B, i_L is buffering inductor current, u_{CD} is the output voltage across point C and point D, i_{rec1} and i_{rec2} are the current through rectifier diodeD1 and D2 respectively, i_{PV} is input current of the PFDDC.

The MI with DC-link is equipped a large capacitor to filter the harmonic. This capacitor can be used to buffer the power difference between the PV panel and the AC grid. The DC bus capacitor is used to realize this function in some medium power converter [26]-[28]. There are two closed-loop to control the prestage DC/DC converter [26]. The design key is that the open-loop gain of the outer voltage-loop at double-line-frequency must be a very small value to suppress DLFCR, which results to a low bandwidth and slow dynamic performance of the converter. A notch filter, whose resonant frequency is at double-line frequency, can be inserted after the voltage-loop regulator to reduce the gain at double-line frequency [27]. The added notch filter only affects the phase of the system in a small frequency bands. Thus, the bandwidth can be enlarged greatly and the effect of DLFCR reduction is better than that in [26]. A current-fed full-bridge converter is used to reduce the DLFCR with the two freedom control strategy [28]. One variable is the duty cycle to control the energy flowing from the input-side. The other variable is the phase-shift between the two legs to control the energy flowing into the output-side. The DLFCR is reduced by a resonant controller of the inner current-loop with a high gain at double-line-frequency. The prestage circuit in [26]-[27] belongs to voltage-fed converter and their open gain from input-side current to the DC bus voltage is large. Thus, a large filter capacitor of the DC bus voltage must be equipped to reduce the voltage ripple [26]-[27]. So, the capacitor with large capacitance must be equipped for the DC bus filter, but it will shorten the lifespan if it is used in MI. The performance of the converter in [28] is excellent. However, the circuit topology is too complex and its cost is expensive for MI.

In this paper, simple DLFCR reduction scheme with good dynamic performance for PV MI should be found to solve the shortcomings mentioned above, such as additional circuit, complex control strategy and lifespan limited by a certain element, etc. The current predictive strategy is commonly used in dual active bridge (DAB) [29], which can effectively enlarge the bandwidth of the converter and increase the capacity of the current tracking. The effect of DLFCR reduction is bad if the current predictive strategy is directly used in MI because of non-linear relationship between the input current of MI and the predictive current. There are also other model predictive methods used in power electronic converters for realizing maximum power point tracking (MPPT), seamless transfer between different modes, power decoupling, etc [30] - [34]. However, these methods cannot be used in the MI for reducing DLFCR without APDC [34]. In this paper, the topology is properly designed according to the characteristic of MI and the mathematical model is derived for establishing the power predictive scheme, which can effectively reduce DLFCR component in the output current of the PV panel.

II. Characteristic And Operational Principle of the Selected Full-Bridge Topology

The input voltage of a single PV panel is low and it has to be stepped up significantly to match the utility voltage. A transformer is commonly used to boost the voltage. The proposed topology for PV MI is based on an isolated full-bridge converter, as shown in Fig. 1, which includes a prestage full-bridge DC/DC converter (PFDDC) and a poststage DC/AC inverter (PDAI). The PFDDC is used to interface the PV panel, where a buffering inductor and a high frequency transformer are used to couple a high-frequency inverter formed by S1-S4 and the double-voltage rectifier. The PFDDC is different from the conventional voltage-fed full-bridge with LC low-pass filter. The PDAI is a full-bridge topology modulated by double-frequency unipolar sinusoidal pulse width modulation (SPWM) strategy and it isn't the emphasis of this paper. We focus on the study of the PFDDC and its control strategy for DLFCR reduction.

Based on the symbols and signal polarities shown in Fig. 1, the theoretical waveforms of the PFDDC in discontinuous conduction mode (DCM) are shown in Fig. 2. The intervals in Fig. 2 describe the various operational steps during a switching cycle of the PFDDC. Setting the duty cycle is

$$D = \frac{t_1 - t_0}{0.5\left(t_{10} - t_0\right)} = \frac{t_1 - t_0}{0.5T_s} = \frac{t_6 - t_5}{0.5T_s} \qquad (1)$$

Where, T_s is the switching cycle of the converter.

The inverter formed by S1-S4 in the PFDDC is adopted phase-shift modulation strategy, as shown in Fig. 2. The current in DCM is convenient to achieve zero current switching (ZCS) for switches S2 and S4 in lagging leg. The switches S1 and S3 in leading leg can realize zero voltage switching (ZVS) if the parasitic capacitor (or external paralleled capacitor) of switches is large enough. The turn-on and turn-off time of the rectifier diodes D1 and D2 are always happens at zero current time. Thus, there is almost no reverse recovery loss to rectifier diodes.

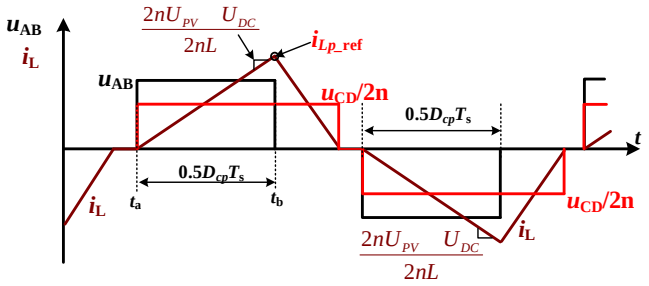


Fig. 3. Current and voltage waveforms showing the referencing instances of the buffering inductor current.

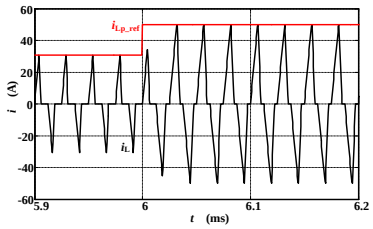


Fig. 4. The simulation waveform of current predictive control.

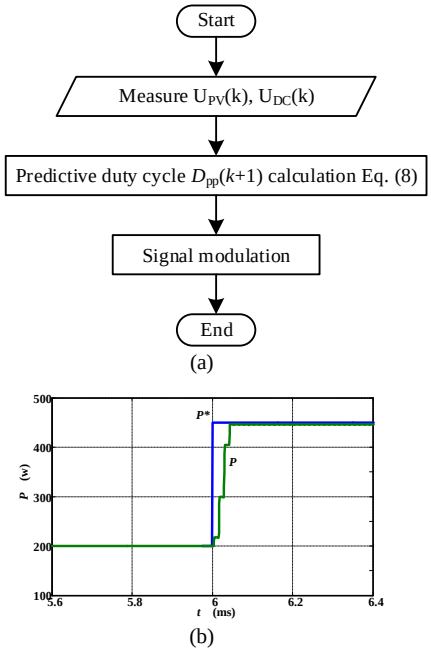


Fig. 5. Realization of power predictive scheme and its simulation results. (a) Flowchart, (b) The simulation waveform.

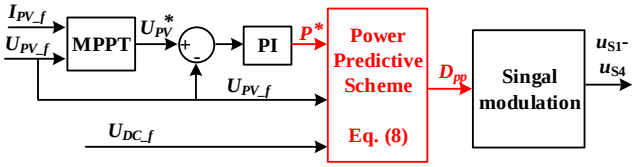


Fig. 6. The control strategy for the PFDDC of the MI.

III. Power Predictive Scheme and Corresponding DLFCR Reduction Strategy

A. Principle of the current predictive scheme

A current predictive control scheme is proposed for DAB in [29], which can effectively enlarge the bandwidth of current-loop and improve dynamic performance. In other words, a proper phase shift angle for DAB can be calculated for the converter using the current predictive scheme, which is established in terms of the mathematical model of the converter. This current predictive scheme can be introduced into the PFDDC in this paper. The current and voltage waveforms of the PFDDC for current predictive scheme establishment is shown in Fig. 3. With the known parameters, such as the input voltage U_{PV}, the DC bus voltage U_{DC} of the PFDDC, the duty cycle D_{cp} can be obtained according to the slope of the current i_L shown in Fig. 3.

$$D_{cp}=\frac{4nLi_{Lp\_ref}}{(2nU_{PV}-U_{DC})T_S} \tag{2}$$

The peak current i_L can reach its reference value i_{Lp_ref} in a half switching cycle after using the duty cycle in (2). The advantage of the current predictive scheme is that the current can track its reference value quickly. It is different from that of the conventional current-loop, where the current i_L is rectified and filtered before its feedback [29].

Fig. 4 shows the simulation result of current tracking. It can be seen that the current can track its reference in a switching cycle. It should be mentioned that the current sensor can be removed due to current in DCM in this paper and zero current from the beginning of every half switching cycle. However, the current sensor must be equipped in [29] because the inductor current is operated in continuous conduction mode (CCM) and the current at the beginning of every switching cycle must be measured for duty cycle calculation.

The essential content of DLFCR reduction strategy is to guarantee that the mean value of the input-side current i_{PV}, shown in Fig. 2, is constant. However, the mean value of i_{PV} isn't proportional to peak value of i_L and their relationship is

$$I_{PV}=0.5D_{cp}i_{Lp\_ref}=\frac{2nLi_{Lp\_ref}^2}{(2nU_{PV}-U_{DC})T_S} \tag{3}$$

Where, I_{PV} is the mean value of current i_{PV}. It can be seen that the value of I_{PV} is related to U_{DC}, which is fluctuant in every line cycle because of power difference between the PV panel and the AC grid. So, double-line-frequency harmonic is also included in I_{PV} if the current predictive scheme is adopted.

B. Principle of the power predictive scheme

The energy can be transmitted from PV-side to DC bus side only when $u_{AB}\neq 0$ from Fig. 3. In a switching cycle, the relationship between i_{PV} and i_L is as Eq. (4).

$$i_{PV}=\begin{cases} i_L & t\in(t_0,t_1) \\ -i_L & t\in(t_5,t_6) \\ 0 & t\in(t_1,t_4)\cup(t_6,t_{10}) \end{cases} \tag{4}$$

The mean value of i_{PV} can also be expressed as (5) according to the relationship in (4).

$$I_{PV}=\frac{(2nU_{PV}-U_{DC})D_{pp}^2T_S}{8nL} \tag{5}$$

Where, D_{pp} is duty cycle which can make the output power equal to expected value. Therefore, the power in the PV-side is

$$P=U_{PV}I_{PV}=\frac{(2nU_{PV}-U_{DC})D_{pp}^2T_SU_{PV}}{8nL} \tag{6}$$

So, the duty cycle can be achieved if the expected output power P is known in terms of (6).

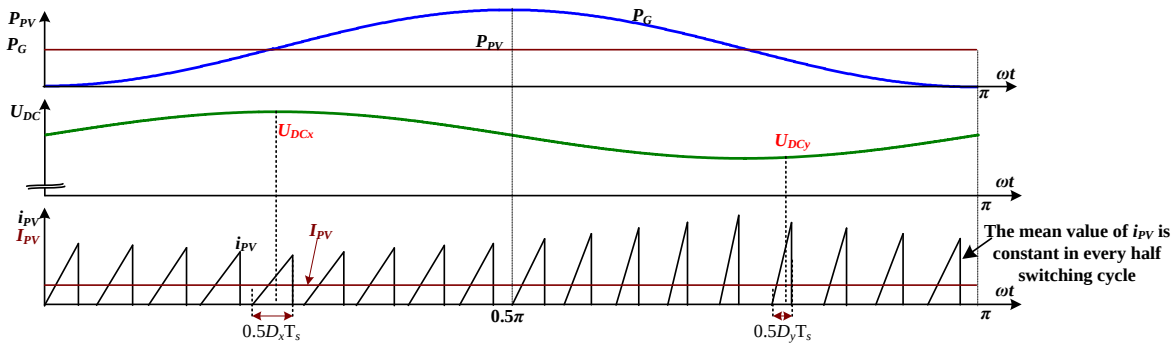


Fig. 7. The LFCR reduction sketch map.

$$D_{pp}=\sqrt{\frac{8nLP}{(2nU_{PV}-U_{DC})U_{PV}T_S}} \tag{7}$$

In the actual prototype, U_{PV} and U_{DC} are approximately equal in the two adjacent switching cycle. So, we can achieve the duty cycle in the (k+1)th switching cycle $D_{pp}(k+1)$ from the measurement parameters in the kth switching cycle, which is shown in (7).

$$D_{pp}(k+1)=\sqrt{\frac{8nLP^{*}}{(2nU_{PV}(k)-U_{DC}(k))U_{PV}(k)T_S}} \tag{8}$$

Where, P^* is the expected output power in the (k+1)th switching cycle. The duty cycle in (8) can make that the output power of PV MI equal to P* in the next switching cycle. The input current is constant if the power reference P* is constant, which can effectively solve DLFCR problem in PV-side. Fig.5(a) shows the flowchart of the power predictive scheme and Fig. 5(b) shows the simulation result of power tracking condition after using the power predictive scheme shown in Fig.5(a), where P* and P are the power reference and actual output power of the PFDDC, respectively. A step in Fig. 5b represents a half switching cycle.

C. DLFCR reduction strategy based on power prediction

The two stage converters in PV MI are controlled separately. The MPPT of PV panel and the DLFCR reduction are fulfilled by the PFDDC. The DC bus voltage control and the high quality grid current is performed by the PDAI. The control strategy for the PDAI with LCL filter is same as literature [35], which is our previous work. It doesn't be discussed here.

The emphasis of this paper is DLFCR reduction strategy under large fluctuation amplitude of U_{DC} after adopting small capacitance of film capacitor. The output voltage reference value of the PV panel U_{PV}* can be achieved from the MPPT algorithm and the PV panel voltage U_{PV} is controlled to track its reference U_{PV}*. Generally, the output signal of the outer voltage loop regulator acts as the reference value of the inner current-loop. If the current predictive scheme in [29] is adopted, there is a considerable DLFCR in the current I_{PV} because of the effect of DC bus voltage fluctuation shown in (3). An important task to PV MI is to reduce DLFCR. Thus, the output current of the PV panel includes the large low frequency component.

The proposed control strategy for the PFDDC, which is based on the scheme in (8), is shown in Fig. 6. The output of the outer voltage loop regulator acts as the power reference value P* and the duty cycle D_{pp} can be achieved from Eq. (8). The calculated duty cycle D_{pp} can guarantee that the output power can follow up its reference P* in a switching cycle. If P* is constant, the output power of the PFDDC is constant. On one hand, the output power of the PV panel is constant. On the other hand, there is no DLFCR component in the output current of the PV panel.

There may be some error between the actual output power P and its reference value P* after using the calculated duty cycle D_{pp} from power predictive scheme because of the effect of kinds of nonlinear factors, such as sensing precision, estimation errors and line impedance. The following content is to estimate the control precision with these errors.

Setting $\hat{L}$ is the estimated value of the buffering inductor L, the duty cycle D_{pp} can be achieved from Eq. (8).

$$D_{pp}(k+1)=\sqrt{\frac{8n\hat{L}P^{*}}{(2nU_{PV}(k)-U_{DC}(k))U_{PV}(k)T_S}} \tag{9}$$

According to Eq. (6), the actual power P is expressed as (10) if the duty cycle in (9) is applied to the PFDDC.

$$P=\frac{\hat{L}}{L}P^{*} \tag{10}$$

It can be seen that the actual power isn't equal to its reference P* and there is a linear relationship between them as long as the estimation error exists. However, the current i_L drops to zero in every half switching cycle and the power error doesn't accumulate cycle by cycle. So, the power error doesn't result in system instability. Moreover, there is no direct relationship between the power reference value P* and the maximum output power of the PV panel. The power reference value P* is determined by the PV panel power and the other parameters of the PFDDC. For example, in a certain environment, the maximum output power of the PV panel can reach P_{PV}=280W. If P*=300W, the actual output power P=250W when $\hat{L}/L=5/6$. The absorbing power P_{PV} of the input capacitor C_{in} is greater than that of its releasing power P, that is to say, 280W=P_{PV}>P=250W. This power difference will result in rising of the voltage U_{PV}. The rising voltage U_{PV} inevitably leads to further increasing of the power reference P* from Fig. 6 (parameters of voltage-loop is negative shown in (17)). When P*=336W ($\hat{L}/L=P^{*}/P_{PV}$), the output power of the PV panel P_{PV} is equal to the actual power P (280W) and the converter is in steady state. That is to say, the estimation error won't affect the operation of the converter.

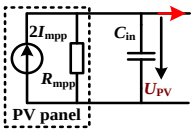


Fig. 8. Equivalent circuit of the photovoltaic cell.

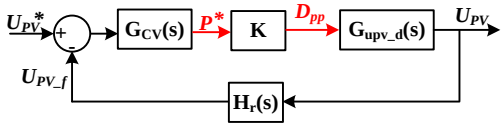


Fig. 9. The control diagram for the former stage of the MI.

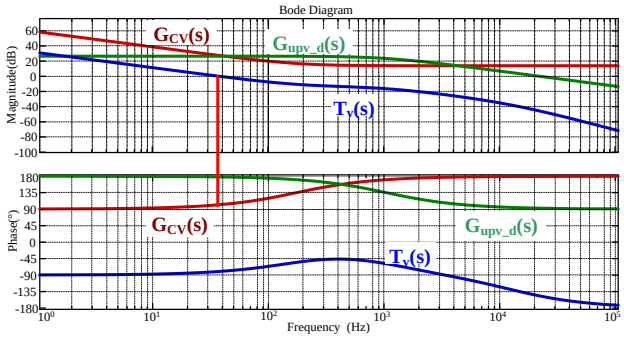


Fig. 10. The bode diagram of control system before and after compensating.

Only the estimation error of the buffering inductor L is considered in Eq. (10). The other parameters, such as the turns ratio of the transformer n, the estimation error of the PV voltage $U_{PV}(k)$ and the DC bus voltage $U_{DC}(k)$, will also result in error between P and P^*. Here, we can't express it any more. Generally, the estimation errors of these three parameters are small. The power difference doesn't accumulate even if the estimation error is large.

Fig.7 shows waveforms of the PFDDC after using the control strategy based on the power predictive scheme. The waveforms are given only in a half line-cycle because the ripple frequency in the DC bus voltage is two times of line-frequency. The DC bus voltage U_{DC} has double line frequency harmonic component because of difference between input power P_{PV} and AC grid power P_G. It should be noted that P_{PV} and P_G are all the mean power in switching cycle. The rising time of i_L is $0.5DT_s$. According to (7), the higher U_{DC} makes the larger duty cycle D_{pp} (D_x shown in Fig. 7) and small rising slope of i_L, and vice versa, the lower U_{DC} makes the smaller duty cycle D_{pp} (D_y shown in Fig. 7) and large rising slope of i_L. It makes a constant mean value I_{PV} in every half switching cycle. The last aim of the proposed strategy in Fig. 6 is to realize constant output power by the predictive duty cycle. Thus, the power P_{PV} is constant in steady state and there is no DLFCR in the input current.

IV. The Parameter Design of the Voltage-Loop Regulator

The control strategy with current inner-loop and the voltage outer-loop for the prestage DC/DC converter had been proposed in [26]. The DLFCR can be effectively reduced by proper control parameters design of current-loop, voltage-loop, and gain at specific frequency. However, the dynamic performance of the converter is bad due to the small bandwidth of the voltage-loop. The proposed power predictive scheme change the principle of DLFCR reduction and the bandwidth of the voltage-loop is greatly enlarged. The specific design process is as follows.

The equivalent circuit of the PV panel and its filter capacitor is shown in Fig. 8 [28]. Where, I_{mpp} and R_{mpp} are the current and the impedance of the PV panel in maximum power.

The mean value equation to the capacitor C_{in} in a switching cycle is expressed in (11).

$$C_{in}\frac{dU_{PV}}{dt}=2I_{mpp}-\frac{U_{PV}}{R_{mpp}}-I_{PV}=2I_{mpp}-\frac{U_{PV}}{R_{mpp}}-\frac{(2nU_{PV}-U_{DC})D_{PP}^2T_S}{8nL} \quad (11)$$

The small disturbance of each parameter is introduced into (11) to achieve the small-signal model. The disturbance model can be obtained after cancel the DC component and high-order component. So,

$$C_{in}\frac{d\tilde{U}_{PV}}{dt}=-X\tilde{U}_{PV}+Y\tilde{d}+Z\tilde{U}_{DC} \quad (12)$$

Where, $X=(\frac{1}{R_{mpp}}+\frac{D_{pp}^2T_S}{4L})$ $Y=\frac{(U_{DC}-2nU_{PV})D_{pp}T_S}{4nL}$ $Z=\frac{D_{pp}^2T_S}{8nL}$

The Laplace transform is performed to (12), we can obtain

$$\tilde{U}_{PV}(s)=\frac{Y}{sC_{in}+X}\tilde{d}(s)+\frac{Z}{sC_{in}+X}\tilde{U}_{DC}(s) \quad (13)$$

So,

$$G_{Upv\_d}(s)=\frac{\tilde{U}_{PV}(s)}{\tilde{d}(s)}=\frac{Y}{sC_{in}+X} \quad (14)$$

The simple control diagram of the proposed strategy is shown in Fig. 9 with the small-signal model. Where, $G_{CV}(s)$ is the transfer funcion of PV voltage regulator. The link of power predictive scheme in Fig. 6 can be viewed as a proportional component because the duty cycle D_{pp} can be obtained from (8) within a switching cycle. $H_r(s)$ is the transfer function of the feedback filter, which is a firstorder low-pass filter with corner frequency of 1/3 switching frequency in experiment and its expression is

$$H_r(s)=\frac{1}{1.2\times10^{-5}s+1} \quad (15)$$

The total open-loop transfer function is shown in Fig. 10 with the compensator.

$$T_v(s)=KG_{cv}(s)H_r(s)G_{Upv\_d}(s) \quad (16)$$

According to the parameters shown in the next section, the bode plot before and after the compensation of the control system with 350W can be achieved. The used regulator of the PV voltage-loop is

$$G_{cv}(s)=-5-\frac{5500}{s} \quad (17)$$

The bandwidth of the control system is 35Hz, which is far greater than that in [26]. The phase margin is 75°and it can enough guarantee the stability of the converter. The DLFCR reduction is mainly fulfilled by the power predictive scheme. Thus, there is almost no DLFCR component in U_{PV}. The total open-loop gain is -8dB at 100Hz, which can sufficient guarantee that there is almost no DLFCR component in the power reference value P*.

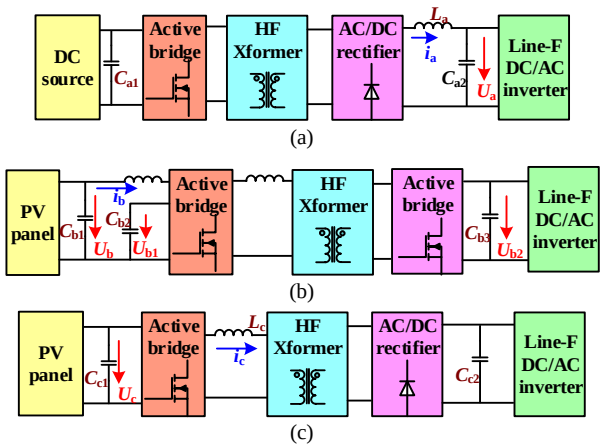


Fig. 11. Two-stage inverter configuration used in previous works for DLFCR reduction. (a) In [26-27]. (b) In [28]. (c) In this paper.

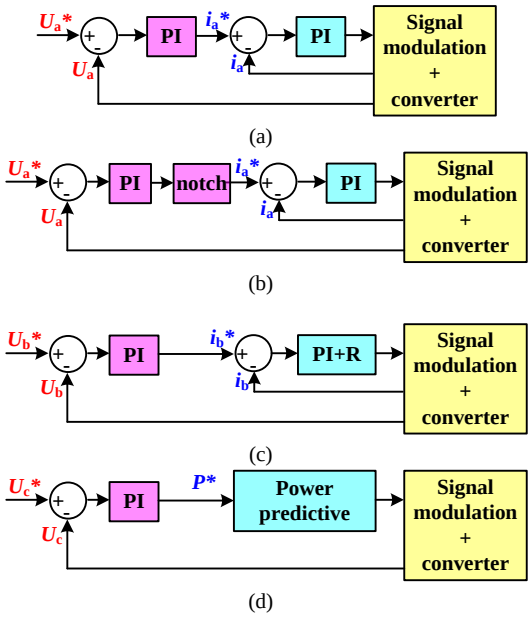


Fig. 12. Control schematic used in previous works for DLFCR reduction. (a) In [26]. (b) In [27]. (b) In [28]. (d) In this paper.

TABLE I

PERFORMANCE ANALYSIS AMONG DIFFERENT STRATEGIES USING DC BUS CAPACITOR AS BUFFERING ELEMENT

	Topology configuration	Closed loop	Complexity of realization	E-capacitor used	DLFCR component	Voltage-loop bandwidth
in[26]	**simple**	two	easy	yes	small	2Hz **(60Hz inverter)**
in[27]	**simple**	two	hard	yes	small	**300Hz(400Hz inverter)**
in[28]	complex	two	hard	**no**	**Almost no**	**23Hz (60Hz inverter)**
in this paper	**simple**	**one**	**easiest**	**no**	**Almost no**	**35Hz(50Hz inverter)**

V. PERFORMANCE COMPARISON BETWEEN DIFFERENT DLFCR REDUCTION STRATEGIES

There are many strategies for DLFCR reduction [19, 23-28]. The proposed strategy can be used in two-stage inverter and DC bus filter capacitor acts as the power buffering element to reduce DLFCR. This characteristic is same as that of [26-28]. However, there are many distinctive characteristics in the proposed strategy.

The two-stage inverter configurations in [26-28] and in this paper are shown in Fig. 11. The topology in [26] is same as the topology in [27], as shown in Fig.11 (a). The prestage converter has a LC filter, composed of L_a and C_{a2}, in the output terminal and it belongs to the voltage-fed converter. DC bus voltage U_a is selected as the outer voltage-loop feed-back variable and filter current i_a is selected as the inner current-loop feed-back variable. The control objective is to hold the current i_a constant. There is a voltage pulsation across DC bus filter capacitor because it acts as the energy buffering element. As a result, there is a power pulsation in the output terminal of the prestage converter, which results in a small DLFCR in the input current of the prestage converter. Thus, a large capacitance must be selected as DC bus filter to decrease DC bus voltage pulsation. The capacitors are 2200μF and 1000μF in [32] and [33] respectively and the output frequency and the rated power of the corresponding inverter is 60Hz/1.6kW and 400Hz/2kW respectively. Therefore, the electrolytic capacitor is inevitably used as DC bus filter.

In [28], a type of current-fed prestage converter is adopted, as shown in Fig. 11 (b). The configuration of the prestage converter is complex due to two active full-bridge and many reactive elements. Researchers select the PV panel voltage U_b as the outer voltage-loop feed-back variable and select input current i_b as the inner current-loop feed-back variable. One advantage of these two closed-loops control is that the output current of PV panel is directly controlled. There is no DLFCR in the output current of PV panel if the two closed-loops are well designed. The other advantage is that DC bus voltage is controlled by the poststage inverter and large voltage pulsation is allowed across DC bus capacitor. The selected DC bus capacitor is 120μF for 5kW rated power. Thus, so small capacitance make it possible to use the film capacitor.

The inductor is in series with the primary-winding of the transformer in this paper, as shown in Fig. 11 (c). Its corresponding current i_c is a high-frequency AC and it is hard to directly act as current feedback variable. So, we only use a single PV voltage-loop to control the prestage converter with the proposed power predictive link. This strategy not only has the same two advantages owned by the strategy in [28], but also has the advantage of simple circuit configuration and simple realization.

In previous works, control systems are all configuration of two closed-loops. The voltage-loop must have very low loop-gain at DLF to guarantee no DLF signal in current reference. The current-loop-gain must have high loop-gain at DLF to realize good performance of current tracking. In [26], the compensators of two closed-loops are all regular PI regulator with a pole at high frequency (20kHz or higher frequency), as shown in Fig. 12 (a). The result of the controller design is the outer loop has a very low bandwidth and the dynamic performance of the converter is very poor.

In order to improve the dynamic performance of the inverter, researchers in [27] added a notch filter after the PI regulator of voltage-loop, as shown in Fig. 12 (b). It can effectively decrease the gain at DLF and improve the bandwidth of the system. A small drawback of this strategy is realization of the controller is complex.

A resonant link is added into the current-loop regulator for high loop gain and good current tracking performance in [28], as shown in Fig. 12 (c). The compensator for voltage-loop is PI regulator. There is another low-voltage-side voltage feedback

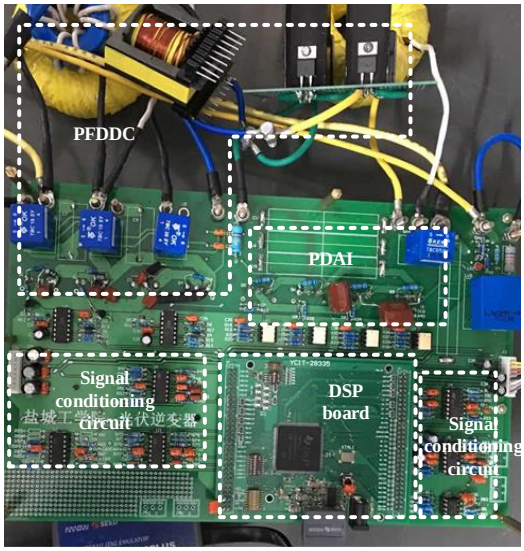
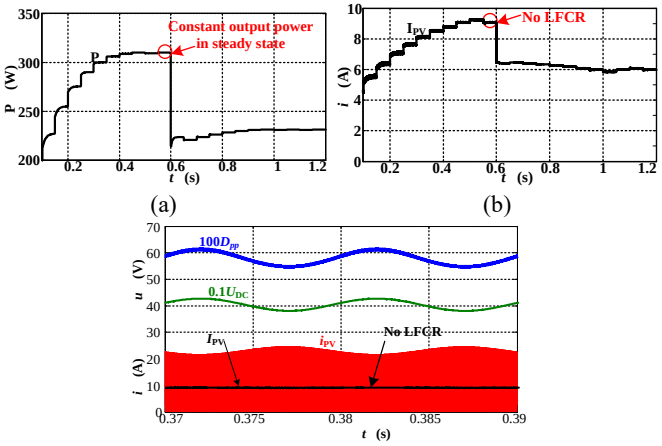


Fig. 13. Photo of the prototype.

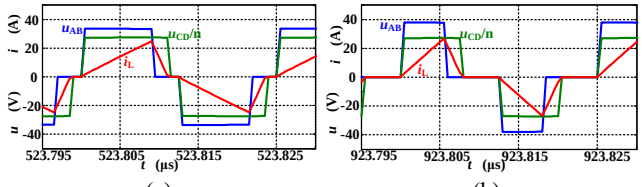
TABLE II
PARAMETERS AND ELEMENT TYPE OF THE PROTOTYPE

Switching frequency for prestage	40kHz
Grid voltage	$220\sqrt{2}\sin(100\pi t)$
PV cell	Maximum power：350W Maximum power point voltage：36V
switches	S1-S4: IRFB4110 D1-D2:C3D05060A S5-S8:C2M0080120D
Filter capacitors	C_{in}:50μF/50V C_1, C_2:100μF/250V C_f:10μF/250V
inductors	L:2.5μH L_1:1mH L_2:0.5mH
transformers	n=7.5
PV voltage regulator	Regulator:-5-5000/s, sample ime:12.5us



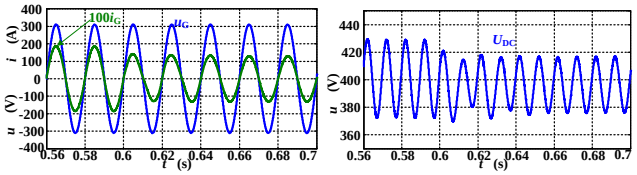
(a) (b) (c)

Fig. 14. The PV MPPT process and LFCR reduction condition. (a) PV power. (b) PV current. (c) LFCR reduction principle.



(a) (b)

Fig. 15. The voltage and current waveforms of buffering inductor in different power. (a) P=310W. (b) P=230W.



(a) (b)

Fig. 16. The waveforms of the second stage grid-connected inverter. (a) Grid voltage and current. (b) The DC voltage.

variable U_{b1}, which is independent of the control schematic in Fig. 12 (c) and is irrelevant to DLFCR reduction.

Fig. 12 (d) shows the control schematic in this paper. It is the simplest one among strategies in [26-28] and this paper because power predictive link has no parameters to design. Only parameters in voltage-regulator are needed to design, which is convenient to optimize system and improve the performance of MI.

Tab. I gives a conclusion of the performance analysis mentioned above. It can be seen that the bandwidth of MI in this paper is large. It is noted that the bandwidth of the voltage-loop is 300Hz in [27], which is far greater than that of in [28] and this paper. The causation is that the frequency of the inverter is 400Hz, while they are 60Hz and 50Hz in [34] and this paper, respectively.

VI. SIMULATION AND EXPERIMENT VERIFICATION

In order to verify the proposed strategy in this paper, a simulation model and a 350W prototype, as shown in Fig. 13, are built. The parameters adopted in simulation model and prototype are same, all as shown in Tab. II. The most important parameter is the inductance of L, which is designed according to the principle that the current i_L is in boundary conduction mode with its maximum output power. Moreover, the selected inductance of L should be less than the calculation value for operational margin.

A. Simulation results

The waveforms shown in Figs. 14-16 are all obtained from the simulation model with the proposed control strategy shown in Fig. 6. At 0.6s, the solar irradiance deceases from 950W/m^2 to 600W/m^2. Figs. 14 (a) and (b) show the PV MPPT process. The method of MPPT is perturbation and observation and its step size is 0.5V to U_{PV}* per 0.05s. The output power will eventually approach the MPP of the PV cell. In duration of every step size, there is no DLFCR in i_{PV} and its mean value is constant after using the power predictive scheme shown in (8). Fig. 14 (c) shows the waveforms of i_L, U_{DC} and duty cycle D_{pp} of the PFDDC. The DC bus voltage is fluctuating because of the instantaneous power difference between the PV panel and the AC grid. The power predictive controller regulates the duty cycle according to (8) and it almost varies with the voltage U_{DC}. The peak value of i_L is same as waveform shown in Fig. 8. The varying duty cycle D_{pp} guarantees that the DLFCR in PV side is well controlled.

Fig. 15 shows the voltage and current waveforms of buffering inductor in different power. The current i_L is designed in DCM from zero to rated power. The higher power corresponds to the lager duty cycle.

Fig. 16 shows the dynamic waveforms of grid side inverter. When the solar irradiance drops, the DC bus voltage will also

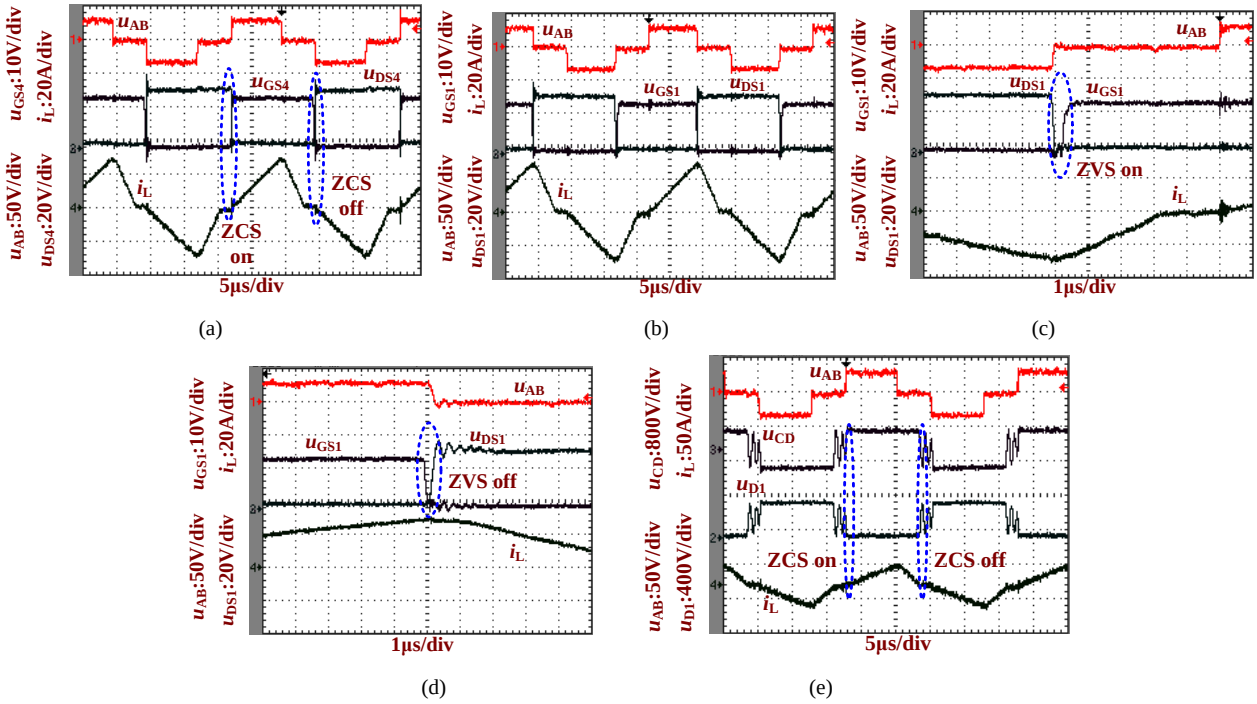


Fig 17. The waveforms of the PFDDC. (a) Waveforms of u_{GS4}, u_{S4}, i_L and u_{AB}. (b) Waveforms of u_{GS1}, u_{S1},i_L and u_{AB}. (c) Zoomed waveforms of turn-on process of S1. (d) Zoomed waveforms of turn-off process of S1. (e) Waveforms of u_{AB}, u_{CD}, i_L and reverse voltage of diode D1 u_{D1}.

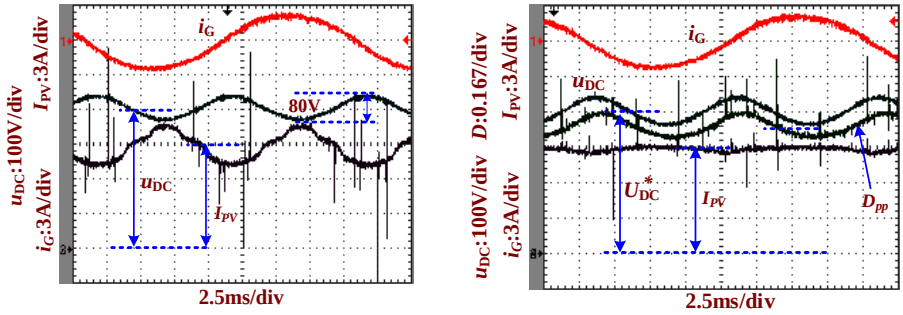


Fig 18. The input current ripple suppression comparison. (a) Without DLFCR reduction strategy. (b) With DLFCR reduction strategy based on the proposed power predictive scheme.

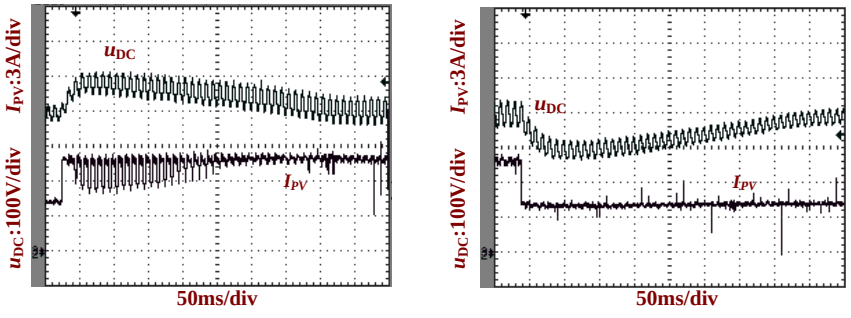


Fig. 19. Waveforms of MI with abrupt change of powe. (a) The PV power switching from 150W to 300W, (a) The PV power switching from 300W to 150W.

decrease and the DC bus voltage loop regulates the amplitude of grid current. Moreover, the low frequency component in DC voltage also becomes smaller because the energy buffering value carried out by DC bus capacitors C_1 and C_2 is deceased.

B. Experimental results

Fig. 17 shows experimental waveforms of the PFDDC in steady state when the output power is 300W. The waveforms of the voltage u_{AB}, the current i_L, and the drive voltage u_{GS4} and terminal voltage u_{S4} of switch S4 in lagging leg are shown in Fig. 17 (a). The turn-on time and turn-off time always happen at i_L=0. Thus, S4 realizes ZCS ON and OFF. Another switch S2 in lagging leg has the same characteristic with the switch S4.The waveforms of the voltage u_{AB}, the current i_L, and the drive voltage u_{GS1} and terminal voltage $u_{S1}$of switch S1 in leading leg are shown in Fig. 17 (b). Fig. 17 (c) and Fig. 17 (d) are the

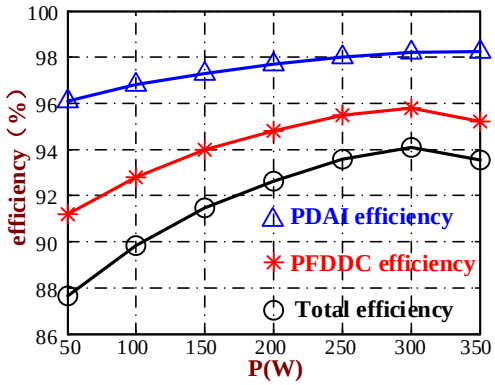


Fig. 20. Efficiency curves of the proposed MI controlled by power predictive scheme.

zoomed waveforms of turn-on process and turn-off process of S1. It can be seen that the voltage has dropped to zero before turn-on time. So, S1 realizes ZVS ON. The rising time of terminal voltage u_{S1} is 0.2μs after its driven voltage u_{GS1} becomes zero and this duration can enough guarantee its turn-off. So, S1 also realizes ZVS OFF. Another switch S3 in leading leg has the same characteristic with the switch S1.

Generally, an external capacitor is paralleled with the switch to decrease the voltage rising slope across the switch, which can guarantee ZVS. The switches S2 and S4 in lagging leg can realize ZCS. The energy stored in junction capacitor or external paralleled capacitor will be wasted at the turn-on time to switch S2 and S4, which decreases the efficiency. Thus, the switches S1 and S3 in leading leg are paralleled with an external capacitor (10nF) for ZVS and the switches S2 and S4 in lagging leg don't need to parallel with an external capacitor for decreasing loss. The efficiency doesn't affect much by the loss in junction capacitor because of its small capacitance (less than 1nF).

The waveforms of the voltage u_{AB}, u_{CD}, the current i_L, and the reverse voltage of diode D1 shown in Fig. 17 (e). It can be seen that the turn-on and turn-off time of the rectifier diode is always at zero current time, which can greatly decrease reverse recovery loss. There is a resonant process during the duration of zero current, as shown in Fig. 17 (e). There is almost no loss from this resonance due to the dinky resonant current.

Fig. 18 shows the waveforms comparison of the PFDDC without DLFCR reduction strategy and with the strategy based on power predictive scheme. The equivalent capacitance of the filter C_1 and C_2 is 50μF and the power difference between the PV panel and the AC grid is buffered by the filter C_1 and C_2. The pulsation amplitude of the voltage U_{DC} is ±40V when the output power is 300W as shown in Fig. 18. The capacitors C_1 and C_2 can be realized by the film capacitor due to its small capacitors, which can prolong the lifespan of the PV MI. Fig. 18 (a) shows the experimental waveforms of the MI without DLFCR reduction strategy and the waveforms include the grid current i_G, DC bus voltage U_{DC}, the mean value of the input current I_{PV}. The mean value I_{PV} includes large double-line-frequency harmonic component due to large fluctuation in the voltage U_{DC} according to (6). Fig. 18 (b) shows the experimental waveforms of the MI with DLFCR reduction strategy based on the proposed power predictive scheme and the waveforms include the grid current i_G, DC bus voltage U_{DC}, the mean value of the input current I_{PV} and the duty cycle D_{pp} calculated by the (8). The duty cycle D_{pp} is varying with the DC bus voltage U_{DC}. Thus, the mean value of the input current I_{PV} can hold constant with a proper duty cycle. It should be mentioned that the waveform of I_{PV} is measured by using a second-order low pass filter with a 5kHz cut-off frequency.

Fig. 19 shows the waveforms of U_{DC} and I_{PV} when the power of the PV has an abrupt change. Fig. 19(a) shows waveforms when the PV power is switching from 150W to 300W and Fig. 19(b) shows waveforms of the opposite process. The dynamic performance of the DC bus voltage is slow because the reference amplitude of the grid current i_G is obtained from the DC bus voltage-loop and the DC bus filter capacitors have a large inertia. However, the whole regulation process is gentle and there is no oscillation. It can be seen that there is some DLFCR component in the current I_{PV} only in the dynamic process and almost no DLFCR component is included in the current I_{PV} in steady state.

From the simulation and experimental results, it can be seen that the MI has a good effect of DLFCR reduction and fast dynamic performance. Fig. 20 shows the efficiency curves of the PFDDC, the PADI and the two-stage MI. The maximum efficiency of the MI is 94.1%, which is located in the medium level of the previous work. The previous reported values of maximum efficiency are 90% [9], 93.8% [11] and 96% [18], respectively. The efficiency is not the highest one because the swing DC bus voltage requires the switches with higher voltage stress, which results in higher loss.

The power predictive scheme in this paper is only verified in PV MI based on full-bridge. We find that it can be introduced to other topologies, such as flyback, which has been verified by simulation. Our next work is to establish general rules for the power predictive scheme in different topologies.

VII. Conclusion

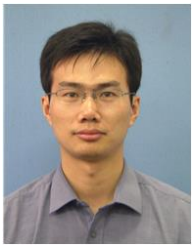
This paper proposes a DLFCR reduction strategy based on power predictive scheme, which is derived from the mathematical model of the corresponding converter. The power predictive scheme can effectively guarantee that the output power of the PFDDC tracks its reference value in a switching cycle. Only the voltage-loop parameters are needed to design and it is easier to realize large bandwidth of the control system. So, the dynamic performance of the PFDDC controlled by the proposed power predictive scheme is good and the robust performance of the control system is also good with the consideration of the estimation error of the different parameters. Experimental results verifies the good effectiveness of the proposed power predictive scheme to PV MI.

Moreover, the proposed power predictive scheme isn't limited in the full-bridge DC/DC converter studied in this paper and it can be extended to other commonly used topologies. This result is proved by our preliminary simulation results and we will further study the characteristic of the proposed power predictive scheme.

References

[1] C. A. Rojas, M. Aguirre, S. Kouro, T. Geyer and E. Gutierrez, "Leakage Current Mitigation in Photovoltaic String Inverter Using Predictive

Control With Fixed Average Switching Frequency," *IEEE Trans. Ind. Electron.*, vol. 64, no. 12, pp. 9344–9354, Dec. 2017.
[2] J. Krata, T. K. Saha, R. Yan, "Model-drive real-time control coordination for distribution grids with medium-scale photovoltaic generation," *IET Renewable Power Generation*, vol. 11, no. 12, pp. 1603–1612, Dec. 2017.
[3] Q. Li and P.Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.
[4] Y. Zhou, L. Liu, and Hui Li, "A High-Performance Photovoltaic Module-Integrated Converter (MIC) Based on Cascaded Quasi-Z-Source Inverters (qZSI) Using eGaN FETs," IEEE Trans. Power Electron., vol. 28, no. 6, pp. 2727–2738, Jun. 2013.
[5] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2015.
[6] F. C. Melo, L. S. Garcia, L. C. de Freitas, E. A. A. Coelho, V. J. Farias, and L. C. G. de Freitas, "Proposal of a Photovoltaic AC-Module With a Single-Stage Transformerless Grid-Connected Boost Microinverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2289–2301, Mar. 2018.
[7] F. Evran, "Plug-in repetitive control of single-phase grid-connected inverter for AC module applications," *IET Power Electron.*, vol. 10, no. 1, pp. 47–58, Jan. 2017.
[8] S. A. Arshadi, B. Poorali, E. Adib, and H. Farzanehfard, "High Step-Up DC–AC Inverter Suitable for AC Module Applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 832–839 Feb. 2016.
[9] S. Zengin, F. Deveci, M. Boztepe, "Volt-second-based control method for discontinuous conduction mode flyback micro-inverters to improve total harmonic distortion," *IET Power Electron.*, vol. 8, no. 4, pp. 1600–1607, Aug. 2013.
[10] F. F. Edwin, W. Xiao, and V. Khadkikar, "Dynamic Modeling and Control of Interleaved Flyback Module-Integrated Converter for PV Power Applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1377–1388, Mar. 2014.
[11] C. Felgemacher, . Jager, A. Kobeissi, J. Pfeiffer, D. Wiegand, W. Kruschel, B. Dombert, S. V. Araujo, and P. Zacharias, "Design of Photovoltaic Microinverter for Off-Grid and Grid-Parallel Applications," *in Proc. IEEE. Integrated Power Electronics Systems Conf.*, Feb. 2014, pp. 1–6.
[12] D. Meneses, O. Garcia, P. Alou, J. A. Oliver, and J. A. Cobos, "Grid-Connected Forward Microinverter With Primary-Parallel Secondary-Series Transformer," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4819–4830, Sep. 2015.
[13] S. Jiang, D. Cao, Y. Li, and F. Peng, "Grid-Connected Boost-Half-Bridge Photovoltaic Microinverter System Using Repetitive Current Control and Maximum Power Point Tracking," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 2711–2722, Nov. 2012.
[14] C. T. Rodríguez, D. V. Fuente, G. Garcera, E. Figueres, and J. A. G. Moreno, "Reconfigurable Control Scheme for a PV Microinverter Working in Both Grid-Connected and Island Modes," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1582–21595, Apr. 2013.
[15] Y. Kim, S. Shin, J. Lee, Y. Jung, and C. Won, "Soft-Switching Current-Fed Push–Pull Converter for 250-W AC Module Applications," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 863–872, Feb. 2014.
[16] H. Chiu, Y. Lo, C. Yang, S. Cheng, C. Huang, C. Chuang, M. Kuo, Y. Huang, Y. Jean, and Y. Huang, "A Module-Integrated Isolated Solar Microinverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 781–788, Feb. 2013.
[17] S. M. Tayebi, and I. Batarseh, "Mitigation of Current Distortion in a Three-Phase Microinverter With Phase Skipping Using a Synchronous Sampling DC-Link Voltage Control," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp.3910–3920, May. 2018.
[18] A. Trubitsyn, B. J. Pierquet, A. K. Hayman, G E. Gamache, C. R. Sullivan, D. J. Perreault "High-Efficiency Inverter for Photovoltaic Applications," *in Proc. IEEE Energy Conversion Congress and Exposition Conf.*, Jun. 2010, pp. 2803–2810.
[19] H. Hu，S. Harb，N. Kutkut，et al, "A Review of Power Decoupling Techniques for Microinverters With Three Different Decoupling Capacitor Locations in PV Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711-2726, Jun. 2013.
[20] S. Ozturk, and I. Cadirci,, "A Generalized and Flexible Control Scheme for Photovoltaic Grid-Tie Microinverters," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 505–516, Jan./Feb. 2018.
[21] D. Hamza, M. Qiu, and P. K. Jai, "Application and Stability Analysis of a Novel Digital Active EMI Filter Used in a Grid-Tied PV Microinverter Module," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2867–2874, Jun. 2013.
[22] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-Type Single-Phase Utility Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, May. 2006.
[23] G. C. Christidis, A. Ch. Nanakos, and E. C. Tatakis, "Hybrid Discontinuous/Boundary Conduction Mode of Flyback Microinverter for AC–PV Modules," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4195–4205, Jun. 2016.
[24] S. Harb, M. Mirjafari, and R. S. Balog, "Ripple-Port Module-Integrated Inverter for Grid-Connected PV Applications," *IEEE Trans. Ind. App.*, vol. 49, no. 6, pp.2692-2698, Nov./Dec. 2013.
[25] C. Liao, W. Lin, Y. Chen, C. Chou, "A PV Micro-inverter With PV Current Decoupling Strategy," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6544–6557, Aug. 2017.
[26] C. Liu，J. S. Lai, "Low frequency current ripple reduction technique with active control in a fuel cell power system with inverter load," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1429-1436, Apr. 2007.
[27] G. Zhu, X. Ruan, L. Zhang, and X. Wang, "On the Reduction of Second Harmonic Current and Improvement of Dynamic Response for Two-Stage Single-Phase Inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1028–1041, Feb. 2015.
[28] Y. Shi, R. Li, Y. Xue, H. Li, "High-Frequency-Link-Based Grid-Tied PV System With Small DC-Link Capacitor and Low-Frequency Ripple-Free Maximum Power Point Tracking," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 328-339, Apr. 2016.
[29] S. Dutta, S. Hazra, S. Bhattacharya, "A Digital Predictive Current-Mode Controller for a Single-Phase High-Frequency Transformer-Isolated Dual-Active Bridge DC-to-DC Converter," *IEEE Transactions on Ind. Electron.*， vol. 63, no. 9, pp. 5943-5952, Sep. 2016.
[30] J. Liu, S. Vazquez, L. Wu, A. Marquez, H. Gao, and L. G. Franquelo, "Extended State Observer-Based Sliding-Mode Control for Three-Phase Power Converters," IEEE Transactions on Ind. Electron.， vol. 64, no. 1, pp. 22-31, Jan. 2017.
[31] S. Vazquez, R. P. Aguilera, P. Acuna, J. Pou, J. I. Leon, L. G. Franquelo, and V. G. Agelidis "Model Predictive Control for Single-Phase NPC Converters Based on Optimal Switching Sequences," *IEEE Transactions on Ind. Electron.*， vol. 63, no. 12, pp. 7533-7541, Dec. 2016.
[32] X. Li, H. Zhang, and R. Balog, "Control strategy for seamless transfer between island and grid-connected operation for a dual-mode photovoltaic inverter," in Proc. IEEE Energy Convers. Congr. Expo. , 2015, pp. 5983–5990.
[33] A. Lashab, D. Sera, J. M. Guerrero, L. Mathe, and A. Bouzid, "Discrete Model-Predictive-Control-Based Maximum Power Point Tracking for PV Systems: Overview and Evaluation," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7273-7287, Aug. 2018.
[34] B. Ge, X. Li, H. Zhang, Y. Liu, R. S. Balog, H. Abu-Rub, and L. Alpuerto, "Direct Instantaneous Ripple Power Predictive Control for Active Ripple Decoupling of Single-Phase Inverter," *IEEE Transactions on Ind. Electron.*， vol. 65, no. 4, pp. 3165-3175, Apr. 2018.
[35] J. Xu, S. Xie, J. Kan, B. Zhang, "Research on Stability of Grid-Connected LCLFiltered Inverter with Capacitor Current Feedback Active Damping Control," *in Proc. International Conference on Power Electronics Conf.*, Jun. 2015, pp. 682–687.



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