NOVEL HIGH-K DIELECTRICS FOR MOS APPLICATIONS

Thesis submitted in accordance with the requirements of the University of Liverpool for the degree of Doctor in Philosophy

by

Pouvanart Taechakumput

31 May 2008

ABSTRACT

The ever increasing demand for improved performance of silicon based microelectronics, at a lower cost, has resulted in an aggressive reduction, or scaling, in the dimensions of the metal-oxide-semiconductor field effect transistors (MOSFET) in integrated circuits (IC). Silicon oxynitride-based gate dielectrics (SiON) have been used in MOSFETs, due to their stable high quality interface with the silicon channel and excellent electrical isolation properties. However, the transistor feature size the gate dielectric has recently been reduced to the point where direct electron tunnelling effects and the leakage currents presented serious problems to device performance in sub-90 nm node IC technology. The same problem also occurs in dynamic random access memory (DRAM), another key device component in the silicon microelectronics industry which faces the challenge of increasing the effective capacitor area without increasing its footprint in the cell. Alternatively, the use of materials with a higher dielectric permittivity (high-k or ε_k) than that of SiO_2 (ε_k = 3.9) allows an equivalent capacitance to be achieved in a physically thicker insulating layer which leads, in turn, to reduced leakage currents. Such materials includes: (i) the metal oxides (e.g., HfO_2, ZrO_2 and Y_2O_3); (ii) the lanthanide oxides (e.g., Pr_2O_3, Gd_2O_3 and Ln_2O_3); and (iii) the pseudobinary alloys (e.g., $ZrSi_xO_y$ and $NdAlO_x$).

In this thesis, physical and electrical characteristics of the deposited high-k materials (HfO_2 and $NdAlO_x$) were thoroughly investigated. Both the atomic layer deposition (ALD) and metalorganic chemical vapour deposition (MOCVD) methods were applied in fabricating high-k dielectrics using novel precursors. The chemical vapour deposition (CVD) method is introduced and discussed and the applications of the high-k dielectrics in microelectronics are reviewed. The effect of heat treatment,

both prior to and after gate metallization, on the film crystallinity and the associated electrical properties was examined in detail. Electrical measurements, of the materials studied, showed promising dielectric properties such as high permittivity values and low leakage current densities. Other properties, such as microstructures, interfacial layer thickness and morphology were also characterized. The origin of frequency dispersion effects, frequently observed in C-V measurements, was also systematically investigated. Finally, a novel reconstruction model has also been implemented for C-V measurements in order to minimize the measurement errors using the adapted dual frequency technique. It is believed that these results will be of significant interest to both academic and industrial researchers in this fast moving field.

ACKNOWLEDGMENTS

It would be difficult for me to adequately thank all those who have helped me with this project, but I would like to name at least a few. I am most grateful to Dr. Stephen Taylor and Dr. Ce Zhou Zhao for the guidance and advice for the initiative and possibility to carry out research on this interesting topic. Also, I wish to express my sincere appreciation to Prof. Steve Hall, Dr. Paul K. Hurley, Dr. Richard J. Potter, Prof. Paul R. Chalker, Dr. Helen C. Aspinall and Prof. Anthony C. Jones for their help and fruitful discussions.

My profound gratitude goes to Dr. Octavian Buiu for his assistance in the ellipsometric measurements, Dr. Jeffrey M. Gaskell for the MOCVD/ALD sample depositions, Dr. Matthew Werner for the MEIS measurements and analysis, Dr. Kate Black and Dr. Nam Pham for the XRD measurements, Dr. Robert T. Murray and Dr. Dinesh L. Ram for providing the TEM measurements, Mr. Kevin Molloy for providing the technical assistance and facilities for MOS capacitor preparation and Dr. Alex Koh, Dr. Evelyn Pang, Dr. Yi Lu and Dr. Pamela Dugdale for their invaluable advices.

Financial support from the Engineering and Physical Sciences Research Council (EPSRC) is gratefully acknowledged.

Finally, I would like to thank my family, the Taechakumputs, and Ms. Tippayarattana Sirichantaropass for their continuous support and encouragement at infinite patience.

31 May 2008

Pouvanart Taechakumput

LIST OF PUBLICATIONS

In addition to the present review, this thesis includes the following refereed journal papers publications and conference proceedings, which are referred to in the text by their corresponding Roman numerals.

Refereed Journal papers

I. J. M. Gaskell, A. C. Jones, H. C. Aspinall, P. R. Chalker, K. Black, H. O. Davies, P. Taechakumput, S. Taylor and G. W. Critchlow, Deposition of $LaAlO_3$ films by liquid injection ALD and MOCVD using a [La-Al] single source alkoxide precursor, *J. Materials Chemistry*, **16**, pp.3854-3860 (2006).

II. P. Taechakumput, O. Buiu, S. Taylor, R. J. Potter, P. R. Chalker and A. C. Jones, Optical and electrical characterization of hafnium oxide deposited by liquid injection atomic layer deposition, *Microelectronics Reliability*, **47**, pp.825-829, (Special Issue) (2007).

III. J. M. Gaskell, S. Przybylak, A. C. Jones, H. C. Aspinall, P. R. Chalker, K. Black, P. Taechakumput, S. Taylor, and H. O. Davies, Deposition of Pr- and Nd-aluminate by Liquid Injection MOCVD and ALD using Single Source Heterometallic Alkoxide precursors, *Chemistry of Materials*, **19**, pp.4796-4803 (2007).

IV. J. M. Gaskell, A. C. Jones, H. C. Aspinall, S. Taylor, P. Taechakumput, P. R. Chalker, P. N. Heys and R. Odedra, Deposition of lanthanum zirconium oxide high-k films by liquid injection MOCVD and ALD, *Appl. Phys. Lett.*, **91**,pp.112912-3 (2007).

V. J. M. Gaskell, A. C. Jones, P. R. Chalker, M. Werner, H. C. Aspinall, S. Taylor, P. Taechakumput and P. N. Heys, Deposition of Lanthanum Zirconium Oxide High-k Films by Liquid Injection ALD and MOCVD, accepted for publication in *Chem. Vap. Dep* (2008).

Conference proceedings

I. Y. F. Loo, S. Taylor, P. Taechakumput, A. C. Jones, P. R. Chalker and L. M. Smith, Low Temperature Post metallization Annealing of High-k Dielectrics' presented at *1st International conference on Memory Technology and Design ICMTD* (Giens, May 2005), (awarded best student presentation).

II. P. Taechakumput, O. Buiu, S. Taylor, R. J. Potter, D. L. Ram and P. R. Chalker and A. C. Jones, Optical and Electrical characterization of high-k hafnium oxide gate dielectric grown by liquid injection atomic layer deposition LI-ALD, presented at the *14th Workshop on Dielectrics in Microelectronics WODIM*, published in Conference Abstract Proceedings pp. 176-177 (Catania, June 2006).

III. A. C. Jones, H. C. Aspinall, J. M. Gaskell, T. D. Manning, P. R. Chalker, S. Taylor, P. Taechakumput and H.O. Davies, Deposition of $LaAlO_3$ films by liquid injection ALD using a [La-Al] single source precursor, presented at *AVS 6th International Conference on ALD* (Seoul, July 2006).

IV. A. C. Jones, J. M. Gaskell, H. C. Aspinall, P. R. Chalker, S. Taylor, P. Taechakumput, R. Odedra and P. N. Heys, Development of precursors for the ALD of high k dielectric oxides, invited

presentation at *AVS 7th International Conference on ALD* (San Diego, June 2007).

V. C. Z. Zhao, S. Taylor, P. Taechakumput, M. Werner, P. R. Chalker, X. L. Huang, T. J. Greenshaw, J. M. Gaskell and A. C. Jones, High-k materials and their response to X-ray radiation, accepted for presentation at the *7th International Semiconductor Technology Conference ISTC* (Shanghai, March 2008).

VI. P. Taechakumput, C. Z. Zhao, S. Taylor, M. Werner, P. R. Chalker, J. M. Gaskell, A. C. Jones and M. Drobnis, Origin of frequency dispersion in high-k dielectrics, accepted for presentation at the *7th International Semiconductor Technology Conference ISTC* (Shanghai, March 2008).

VII. P. Taechakumput, C. Z. Zhao, S. Taylor, M. Werner, N. Pham, P. R. Chalker, B. Murray, J. Gaskell and A. C. Jones, Annealing Effect on Neodymium Aluminates high-k dielectric deposited by Liquid Injection MOCVD using single source Heterometallic Alkoxide precursors, accepted for presentation at the *7th International Semiconductor Technology Conference ISTC* (Shanghai, March 2008).

CONTENTS

LIST OF FIGURES

Number *Page*

LIST OF TABLES

Number *Page*

LIST OF ABBREVIATIONS AND ACRONYMS

AES. Auger Electron Spectroscopy

Al_2O_3. Aluminium Oxides/Alumina

ALCVD/ALD. Atomic Layer (Chemical Vapour) Deposition

CET. Capacitance Equivalent Thickness

CMOS. Complementary Metal Oxide Semiconductor

Cp. Cyclopentadienyl, C_5H_5

C-V. Capacitance-Voltage

CVD. Chemical Vapour Deposition

D. Deuterium

DRAM. Dynamic Random Access Memory

EOT. Equivalent Oxide Thickness

F-N. Fowler-Nordheim conduction mechanism

FGA. Forming Gas Annealing

GaAs. Gallium Arsenide

Gd_2O_3. Gadolinium Oxides

H. Hydrogen

HF. Hydrofluoric acid

HfO_2. Hafnium Oxides

IC. Integrated Circuit

^{i}Pr. Isopropyl, $-CH(CH_3)_2$

I-V. Current-Voltage

JVD. Jet Vapour Deposition

La_2O_3. Lanthanum Oxides

$La_xZr_{1-x}O_y$. Lanthanum Zirconium Oxides

LI-CVD/LI-ALD. Liquid Injection CVD or ALD system

LSTP. Low Standby Power

MBE. Molecular Beam Epitaxy

Me. Methyl, (CH_3)

MEIS. Medium Energy Ion Scattering

MOCVD. Metalorganic Chemical Vapour Deposition

MOSFET. Metal Oxide Semiconductor Field Effect Transistor

N_2. Nitrogen

Nd_2O_3. Neodymium Oxides

$NdAlO_3$. Neodymium Aluminate

O_2. Oxygen

O_3. Ozone

PDA. Post Deposition Annealing

P-F. Poole-Frenkel conduction mechanism

PLD. Pulsed Laser Deposition

PMA. Post Metallization Annealing

PrO_2, Pr_2O_3, Pr_6O_{11}. Praseodymium Oxides

PVD. Physical Vapour Deposition

RTA. Rapid Thermal Annealing

SA. Spike Annealing

SCLC. Space Charge Limited Current

Sc_2O_3. Scandium Oxides

SE. Spectroscopic Ellipsometry

Si. Silicon

SILC. Stress Induced Leakage Current

Si_3N_4. Silicon Nitride

SiO_2. Silicon Dioxide

SOI. Silicon On Insulator

Ta_2O_5. Tantalum Pentoxide

TEM. Transmission Electron Microscopy

TFEL. Thin Film Electro-Luminescence

TiO_2. Titanium Dioxides

XRD. X-Ray Diffraction

Y_2O_3. Yttrium Oxides

ZrO_2. Zirconium Oxides

$ZrSi_xO_y$. Zirconium Silicates

(OH). Hydroxyl group

Chapter 1 – Literature review

1.1. THE MOTIVATION BEHIND HIGH-K GATE MATERIALS AND ALTERNATIVE HIGH-K GATE DIELECTRICS

Over the past three decades, astounding progress has been made in silicon technology, achieved through continual scaling of the planar silicon metal oxide semiconductor (MOS) field effect transistor (FET) to ever smaller dimensions. This equates to a steady increase in the number of devices per chip, at a lower cost.[1,2]

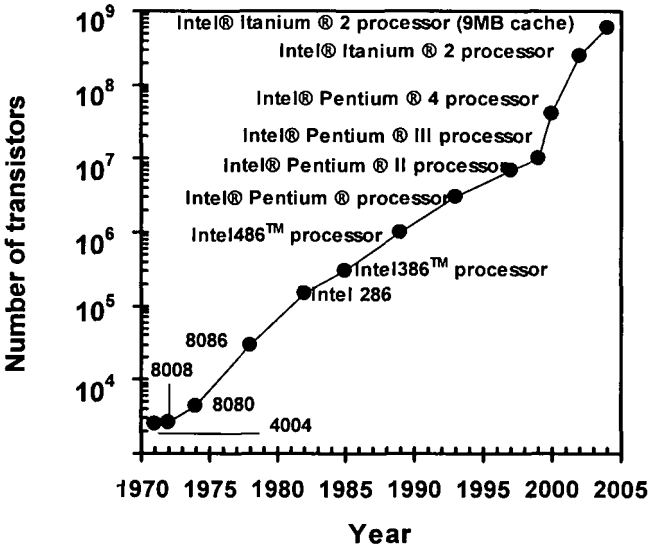

Figure 1.1.1. Schematic showing the continual increase in number of transistors used in Intel Microprocessors.[3]

The exponential increase of device density, as quantified by Moore's law,[4] and scaling of device dimensions into the nanotechnology regime (Fig. 1.1.1) has resulted in vast improvements in numerous electronic devices ranging from personal computers to control systems found in

automobiles and aircraft. Although considerable innovation and investment have been involved in order to realize this rate of dimensional scaling, there has been no major revolution in the fundamental device concept and the materials system for the basic MOSFET to date.

In 2007 MOSFET's are reported with effective channel lengths of approximately 30nm, silicon oxynitride gate dielectric thicknesses of approximately 1.2nm and supply voltages of approximately 1.1V.[5] Although it may be possible to manufacture traditional MOS devices with thinner layers of silicon oxynitride, the performance of the scaled device will eventually be affected by tunnelling leakage current larger than that currently associated with the 1.2nm gate dielectric (i.e., $\geq$ 10 Acm^{-2}), resulting in unacceptably high power dissipation levels ($\geq$ 10 W) for the total integrated circuit. Furthermore the scaled devices will suffer from channel length modulation effects, which are caused by the increase of the depletion layer width at the drain as the drain voltage is increased, thereby shortening the length of the inverted channel region. This leads to an increased drain current and a reduction of output resistance, which deteriorates the reliability of 'switching' states. The highly doped polysilicon gate will also no longer behave effectively at high electric fields, but instead will limit the MOSFET performance. This is caused by the formation of a depletion layer near the polysilicon/oxide interface when the device is biased in strong inversion, the so-called poly-depletion effect, which in turn results in the degradation of the total gate capacitance of MOS devices and the current drivability.[6,7] Thus as silicon MOSFET technology approaches its boundaries and owing to the fundamental limits associated with the traditional MOSFET,[8] entirely new materials and/or device structures will be required to replace and augment the traditional MOSFET. Many possible emerging technologies are currently under investigation, which can be categorized[5] into: (i) materials-limited MOS; (ii) non-classical MOS; and (iii) beyond MOS.

Materials-limited MOS refers to both alternative insulating gate dielectric materials and alternative channel materials. Until recently, the gate dielectric has been made from silicon dioxide (or its nitride derivatives) and the higher capacitance values are achieved only by decreasing the oxide thickness according to Eq. 1.1.1.

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_k A}{t_{ox}} \tag{1.1.1}$$

where ε_0 is the dielectric permittivity of free space (8.85×10^{-14} Fcm^{-1}), ε_k is the dielectric permittivity of the gate dielectric, A is the device area (cm^2) and the oxide thickness is denoted with t_{ox}. However, a practical limit for the gate thickness seems to be around 0.7-1.2nm for pure SiO_2 before the leakage current, due to direct tunnelling, becomes prohibitive.[9] Alternative materials with higher dielectric permittivity values, while maintaining sufficiently high energy barriers to carriers in the valence and conduction bands, have been developed to replace silicon oxynitride according to the guidelines for selecting the substitute materials.[10,11] New channel materials are also being widely investigated, in order to improve the MOSFET speed. These includes strained silicon and III-V materials (e.g., Indium gallium arsenide and indium antimonite)[2,12]

Non-classical MOSFET structures are also being considered for extension `beyond the performance improvements found with the dimensional scaling and new materials. This includes the re-engineering of the substrate into silicon-on-insulator (SOI), where the active silicon is buffered by a layer of thick SiO_2. This greatly decreases the parasitic junction capacitance from the source/drain to the substrate and enhances the speed of the devices.[13] A more radical approach is the design of the tri-gate (finFET) structure.[13,14] These devices exhibit good short channel behaviour, thereby allowing a greater scalability. However, they pose a host of technological problems and a number of challenges (i.e., degraded channel mobility, low current drivability, parasitic series resistance and

high production cost due to the difficulty of producing uniform size fins) that still remain to be overcome.

In the next decade, it is very likely that potential improvements in device performance are mainly achieved through further dimensional scaling with changes in both materials and device structures. However, at some point, the properties of these nanodevices will be susceptible to perturbations due to fundamental limitations once again. Entirely new approaches 'beyond MOS' will be mandatory. Currently, these include the engineering of carbon nanotubes,[15] nanowire transistors,[16] single-electron transistors[17] and quantum dots,[18] where very specific electronic properties can be synthesized in a possible manner and the promise of fabrication through self-assembly. In addition, ferromagnetic devices have attracted much attention, for their revolutionary computing power, due to their inherently low power dissipation (as compared with charge-based devices) and the use of electron spin as the computational state. This allows the possibility of spin-based devices such as spin MOSFETs,[19] spin-torque transistors[20] and spin-gate transistors.[21]

While the future of the MOS devices may lie with various alternative approaches that had been briefly discussed, the scope of this research remains within the near-term, implementation of traditional MOS devices using high-k dielectric materials (materials-limited MOS). The task of incorporating high-k gate dielectrics into a future Low Standby Power (LSTP) technology, however, can not be taken without due consideration. The sole motivation for the material change is to lower the gate tunnelling current. Nonetheless, high-k films though physically thicker do not always possess reduced leakage since the bandgap for most films is smaller than SiO_2 as depicted in Fig. 1.1.2.[10] Numerous issues relating to high-k materials include: (i) the associated intrinsic and extrinsic defects that may alter the desired electrical properties; (ii) their stability on silicon, in which a thin layer of SiO_2 or its nitride is often required to

enhance the interface match; (iii) integrating issues that arise through switching to metal gates; (iv) the resistivity to impurity penetration and the associated thermal budget upon high temperature annealing; and (v) the geometric MOSFET structural challenges with high-k gate dielectrics that cause the additional fringe capacitance effect.[2]

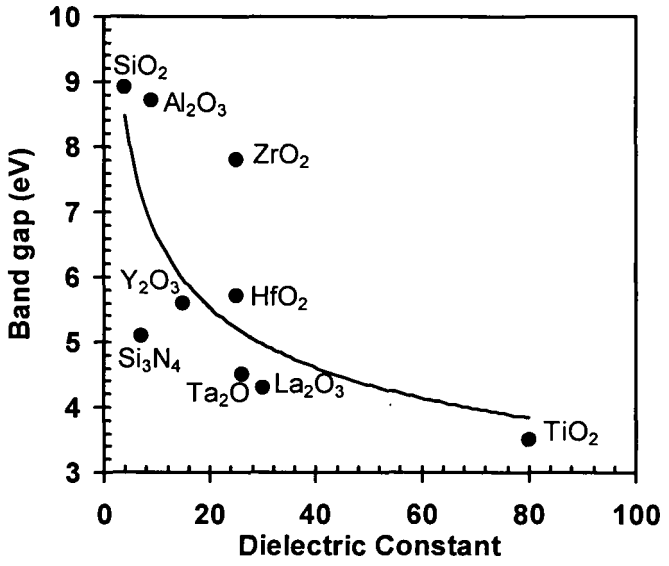

Figure 1.1.2. Schematic showing the bandgap versus dielectric constant for insulators.[10]

The use of materials with a higher dielectric permittivity than that of SiO_2 (ε_k = 3.9) does however allow an equivalent capacitance to be achieved in a physically thicker insulating layer which leads, in turn, to reduced leakage currents. However, the equivalent oxide thickness (EOT) of the high-k replacement should be less than ~ 1.2nm in order to provide an advantage over the mainstream nitrided SiO_2. The EOT is generally expressed using the relation:

$$EOT = t_{SiO_x} + \left(\frac{3.9}{\varepsilon_k}\right) t_k \qquad (1.1.2)$$

where t_{SiOx} and t_k are the thicknesses of SiO_x layer and high-k layer respectively. A key requirement for a FET is that the potential high-k dielectrics must be compatible with silicon, forming an extremely high-quality interface with silicon and capable to withstand CMOS processing conditions (i.e., withstanding an activation anneal at a temperature of 1100°C) while in contact with silicon. Several approaches have been used in fabricating potential high-k candidates which includes: (i) physical vapour deposition (PVD); (ii) solution deposition; and (iii) chemical vapour deposition (CVD). The most commonly studied high-k dielectrics have been materials systems such as tantalum pentoxide (Ta_2O_5) and alumina (Al_2O_3), which have been employed mainly due to their maturity of use in memory applications.[22,23] However, Ta_2O_5 is not thermodynamically stable in direct contact with silicon, thus creating unacceptable levels of bulk fixed charge, high density of interface trap states and hence low silicon interface carrier mobility. Much effort[24,25] has been expended to demonstrate the feasibility of using Ta_2O_5 within a standard complementary metal oxide semiconductor (CMOS) process, nevertheless, the inherent thermal instability when in direct contact with silicon severely limits the ultimate device performance.[22] In an attempt to minimize the reaction with the underlying silicon, interface engineering schemes have also been developed to form oxynitride and oxide/nitride barriers between high-k materials and silicon.[26-28] These barriers have been shown to reduce the extent of reaction between high-k dielectric and silicon, as well as to help maintain a high channel mobility. However, the presence of the capping 'barrier' layer limits the lowest achievable EOT and increases the process complexity for deposition. Much research has been exerted in investigating several other high-k candidates of both metal oxides and pseudobinary systems. They were categorized accordingly for their chemical similarities by group in the periodic table

as: (i) group IIIA and IIIB metal oxides; (ii) group IVB metal oxides; and (iii) pseudobinary alloys.[10]

Among the group IIIA candidates, Al_2O_3 has been extensively studied due to its high bandgap, thermodynamic stability on silicon up to high temperatures and is amorphous under the conditions of interest. The drawback is a slightly higher permittivity value ($\varepsilon_k \sim 8$) than that of SiO_2, thereby making it a relatively short-term solution for the needs of gate dielectric replacement. Al_2O_3 is thermodynamically stable on silicon, but different deposition techniques that operate under non-equilibrium conditions may trigger reactions at the alumina /silicon interface.[29,30] It was later shown to be possible to control the interface reactions (and hence the growth of Al_2O_3 on silicon) without forming an interfacial SiO_2 layer, by atomic layer CVD (ALCVD).[31] Encouraging reliability characteristics of Al_2O_3 were reported for both ALCVD and PVD, showing a reduction in leakage current of ~ 100 times compared to the equivalent thickness of SiO_2 and low stress-induced leakage current (SILC) effect.[32,33] Some drawbacks observed in the deposited Al_2O_3 film however included mobility degradation, low resistivity to boron and phosphorus diffusion upon annealing and the presence of negative fixed charges.[33-35]

For group IIIB, a substantial amount of investigation has been done with oxides of yttrium (Y_2O_3) and scandium (Sc_2O_3). Y_2O_3 has been successfully deposited with sputtering,[36] molecular beam epitaxy,[37] pulsed laser deposition (PLD)[38] and metalorganic chemical vapour deposition (MOCVD).[39] The dielectric permittivity of the Y_2O_3 was found to range from 9-20, together with interface state density of the order $\sim 10^{12}$ $cm^{-2}eV^{-1}$.[36,40] The measured leakage currents varied with the depositing techniques and thermal treatment conditions, however, the breakdown field strength was approximately 4 $MVcm^{-1}$.[36,37] It was also found that Y_2O_3 could readily form silicates depending on the kinetics of

the depositing process and exhibited very large threshold voltage shifts measured in a broad array of sample conditions.[41] Sc_2O_3 has been deposited by both chemical vapour deposition (CVD) and atomic layer deposition (ALD).[42-44] The dielectric permittivity obtained in as-deposited films were ~17 with average breakdown field strength of 3.5 $MVcm^{-1}$. Crystallinity and surface roughness were observed in as-deposited films, regardless of the growth temperatures, and increased with increasing annealing temperatures.[44] Sc_2O_3 may not be well suited for gate dielectric applications due to a stringent requirement of high-quality interface with silicon, however, it is feasible for protective coating, damage-resistant antireflection multilayer coatings in high-power UV lasers, etch-stop layers in multilayer dielectric gratings and resist layers in electron beam lithography.[44-46]

Among group IIIB elements, there has been much recent research in the rare-earth (lanthanide) oxides such as the oxides of lanthanum (La_2O_3), praseodymium (Pr_2O_3), gadolinium (Gd_2O_3) and neodymium (Nd_2O_3). They are good insulators due to their large bandgaps (e.g., 5.6 eV for Gd_2O_3), they have high dielectric constants (e.g., La_2O_3: ε_k = 30) and good thermodynamic stability on silicon, making them attractive materials for high-k dielectric applications.[47] Rare-earth oxides have mainly been deposited by various PVD methods, including electron beam evaporation[48-50] and molecular beam epitaxy (MBE).[51,52] However, CVD techniques (e.g., MOCVD and ALD) are more flexible methods that allow the controlled growth of highly conformal films on planar and high-aspect ratio substrates. In spite of these advantages, very few studies have been realized on the CVD of rare-earth oxides due to a lack of suitable precursors with appropriate stability, volatility and decomposition characteristics.[53] La_2O_3 is being considered as a potential candidate for the gate dielectrics of the next generation MOSFET due to its good dielectric integrity.[54,55] EOTs as low as 0.5nm were reported

together with a high effective breakdown field (13.5 $MVcm^{-1}$), low interface state density (order of $\sim 10^{10}$ $cm^{-2}eV^{-1}$) and an excellent reliability with more than 10 years lifetime even at 2V bias.[55] The main conduction mechanisms were determined to be the space-charge limited current (SCLC) at low oxide field and Fowler-Nordheim (F-N) conduction at high oxide field region regardless of any thermal treatments.[50] The downfall of La_2O_3 is the lack of ambient stability, its very hygroscopic nature and its tendency to react with the underlying silicon to form La-silicate interfacial layer that lowers the overall permittivity of the gate stack.[52] This has led to further research focussing on the permittivity and ambient stability of lanthanum oxide by adding zirconium atoms to create lanthanum zirconium oxide ($La_xZr_{1-x}O_y$).[56-58] It was anticipated that certain La concentrations the material would have a relatively high dielectric constant and that it would remain amorphous to high temperature. In addition, the addition of La may stabilise the cubic or tetragonal phases of ZrO_2 which are expected to have higher ε_k values than the more thermodynamically stable monoclinic phase. The ongoing research seems to deliver promising results using La or La-based materials and is considered to be a leading candidate for the 32nm logic technology node and beyond.[59]

Pr_2O_3 is also of great interest as an alternative gate dielectric candidate due to the close lattice match with silicon, moderate bandgap (3.9eV) and high permittivity ($\varepsilon_k \sim$ 23-30).[60-62] In particular, Pr_2O_3 was reported to exhibit leakage current densities 10^4 times lower than hafnia (HfO_2) and zirconia (ZrO_2) at the same EOT.[62] The presence of large electron effective mass, which occur in the lowest conduction band in the oxide, together with the suitable conduction band offset to silicon (1eV) led to the ultra-low measured leakage currents.[62] Another possible suggestion for the ultra-low leakage currents observation in Pr_2O_3, despite having a lower bandgap than HfO_2 and ZrO_2, can be associated with large electron

trapping sites in the oxide. The dominant conduction mechanism at high electric field is purely Fowler-Nordheim conduction with the average breakdown field reported to be as high as 43 $MVcm^{-1}$, the value which was based on EOT of 1.4 nm.[62] Moreover, Pr_2O_3 is found to be compatible with the standard CMOS lithography process (e.g., wet chemical cleaning and etching, resist removing and process integration of Pr_2O_3 in a polysilicon gate CMOS process), demonstrating that it is not necessary to re-engineer the manufacturing procedures.[63] Different crystallographic structures are known for the stoichiometric praseodymium oxides, depending on their oxidation states, and so a range of oxides (e.g., PrO_2, Pr_6O_{11} and Pr_2O_3) as well as intermediate compositions are available. Therefore much attention has been devoted on the growth process and parameter selection.[60,62,64,65] However, Pr_2O_3 is unstable in air/moistures and can undergo electrical degradation.[65] This currently inhibits Pr_2O_3 alone as a winning candidate for alternative gate dielectric.

The studies on other exotic rare-earth elements include the oxides of gadolinium (Gd_2O_3) and neodymium (Nd_2O_3). The main attracting features of Gd_2O_3 also lie with its relatively close lattice match with silicon (e.g., $a(Gd_2O_3)$ = 10.812Å), that offers the possibility for epitaxial growth,[66] and its moderate permittivity value (ε_k) of 14.[49] Gd_2O_3 has featured prominently as one of the first insulating materials used in the successful fabrication of gallium arsenide (GaAs) MOSFETs.[66-68] Much work on Nd_2O_3 was previously carried out mainly for luminescent materials and protective coatings on stainless steels,[69,70] only recently has Nd_2O_3 been considered for gate dielectric applications.[71,72] Nonetheless, electrical properties of the latter materials have not been thoroughly investigated and a finer control of the interfacial structures would be needed before integrating these materials into silicon processing. Despite their attractive features, both Gd_2O_3 and Nd_2O_3 appear to be chemically

unstable upon annealing and can undergo a partial transformation (e.g., to NdO(OH)) when exposed to atmospheric conditions.[49,71] This has led to further development in surface passivation and interface stability using oxynitrides and pseudobinary alloys (e.g., silicates and aluminates), where desirable properties can be achieved through various combinations of chosen materials. Further details of rare-earth elements and pseudobinary alloys, in particular with neodymium, are described in chapter 5, section 5.1.

Work on alternate dielectric materials systems of group IVB metal oxides, such as titanium dioxide (TiO_2), has been actively pursued for both memory capacitors and in transistors. The attraction of the TiO_2 system is mainly due to its very high permittivity (ε_k) of 30-100,[73-75] depending on the crystal structure and the method of deposition. However, titanium (Ti) possesses several stable oxidation states (e.g., Ti^{3+} and Ti^{4+}) that lead to problems associated with carrier traps, due to oxygen vacancies, and high leakage paths. Several deposition techniques have been used to deposit TiO_2, including CVD,[75] the jet vapour deposition (JVD)[76] and RF magnetron sputtering.[77] Later findings[75,78] concur that TiO_2 is not stable on silicon during deposition by CVD, therefore, both a reaction layer at channel interface and metal electrodes interface will be required to maintain interface stability. Although the post deposition treatment sequences for CVD process were successfully developed,[79] in which the interfacial reactions were minimized and the leakage currents were lowered by four orders of magnitude, the requisite presence of the reaction barrier layers limit the ultimate device scaling and performance.

Hafnium dioxide (HfO_2) is arguably the leading candidate of all high-k systems. Intense investigation has been previously carried out using HfO_2 as an optical coating and in dynamic random access memory (DRAM) applications. HfO_2 is attractive as an alternative gate dielectric owing to

its high dielectric permittivity (ε_k) of ~25 in its monoclinic, tetragonal or cubic form, moderate bandgap (~5.7 eV) and a good thermal stability on silicon. To date, Hf-based materials are incorporated in the 45-nm technology node.[80] A recent article[81] shows the world's first working 45-nm CPUs, which are currently under major production for the second half of 2007. The process claims 1 nm electrically thick Hf-based gate dielectrics, deposited via atomic layer deposition (ALD), with dual-band edge work function metal gates. A reduction in switching power (~30%), greater than 20% improvement in switching speed, greater than five times reduction in source/drain leakage and greater than 10 times reduction in gate leakage currents are expected from the Intel Penryn silicon.[82] Further details of HfO_2, which includes growth and characterization, are described in chapter 4.

Finally, much effort has also been exerted on zirconium dioxide (ZrO_2).[83-86] ZrO_2 also has high dielectric permittivity (ε_k) of ~25, high breakdown field strength (6-10 $MVcm^{-1}$),[87,88] and a moderate bandgap (7.8eV).[10] However, ZrO_2 is not completely chemically or thermally stable on silicon. It crystallizes at relatively low temperatures (~400-500°C),[83] which leads to current leakage along the polycrystalline grain boundaries and promotes the formation of a lower permittivity SiO_2 layer during the high temperatures (~ 900°C) involved in CMOS processing. Further drawbacks also include ionic conductivity in the bulk oxide (i.e., vacancies or traps that arise from oxygen ions diffusion) and carrier mobility degradation in the MOSFET channel that hinder its application.[89] As previously discussed, one solution to interface stability problem is to deposit a mixed oxide film, such as $ZrSi_xO_y$,[90,91] which remains amorphous up to high temperature (~ 800 - 900°C), leading to reduced leakage currents and inhibits the formation of the SiO_2 interlayer. Although the permittivity of $ZrSi_xO_y$ (ε_k = 12-25) is lower than the pure metal oxide, this is considered to be an acceptable trade-off for greatly

improved interface stability. Alternatively, a buffer layer of silicon nitride (Si_3N_4) can be used to improve the interface stability, at a cost of the restricted minimal EOT.[92] Work on effects of annealing on oxide fixed charge density have also been discussed, in which the correlation between depassivation of defect density and generation of fixed charges as a function of annealing temperatures were determined.[86] The conduction mechanisms in ZrO_2 thin films have also been thoroughly investigated, indicating that the dominant transport mechanism was Poole-Frenkel conduction.[93-95] Several studies have shown encouraging results on Zr-based dielectrics, in which the fabricated films exhibited excellent thermal stability and good dielectric properties.[88-91] For the above reasons, Zr-based dielectrics are also considered to be promising alternative candidates for future high-k dielectric applications.

The purpose of the work, reported in this thesis, was to develop new processes for the MOCVD/ALD of metal oxides, rare-earth oxides and their associated alloys. The scope of the work also remains close to the development of new precursors and their associated physical/electrical characteristics. Therefore the thicknesses of the deposited films reported in this work tend to lie in a thicker regime (>10nm) rather than the associated gate dielectric application (<5nm). However, building on the success of the novel precursors investigated here, future work would involve the optimization of films with thickness relevant to the industry.

This chapter has reviewed the current status of the high-k oxides and their compatibility with the current technology. Chapter 2 describes various experimental techniques used in this research, which includes the deposition process and characterization methods. In order to better understand the importance of heat treatments, involved in the semiconductor processing steps, a literature review on annealing studies is also included. Theoretical modelling of the MOS structure, which lays the groundwork for discussions in the later chapters, is presented in

chapter 3. Also, the causes of frequency dispersion in high-k dielectric stacks, together with the reconstructing formulae are presented to recover the actual capacitance from errors. Chapter 4 and 5 are concerned with growth and characterization of both HfO_2 and $NdAlO_3$. The effects of processing temperature on the degree of crystallization are presented, together with the associated electrical characteristics.

Chapter 2 – Experimental

2.1. DEPOSITION TECHNIQUES – LIQUID INJECTION (MOCVD AND ALD) SYSTEMS

Metal oxide thin films are finding increasing applications in microelectronics and telecommunications such as next-generation computer memories, gate dielectric layers in CMOS technology and infrared detectors.[23,96] A number of techniques have been used for the deposition of the metal oxide thin films, which can be divided into three general categories:

1. Physical vapour deposition (e.g., magnetron sputtering, ion beam sputtering and molecular beam epitaxy)[97-99]
2. Solution deposition (e.g., sol-gel, metalorganic decomposition)[100,101]
3. Chemical vapour deposition (e.g., metalorganic chemical vapour deposition, atomic layer deposition)[85,102-104]

A successful dielectric deposition method must deposit contamination-free films with precise and uniform thickness over large areas, while remaining cost effective. Of those techniques, chemical vapour deposition (CVD) is the most versatile and promising deposition technique that fulfils the latter requirements. Metalorganic chemical vapour deposition (MOCVD) commonly uses vapour-phase mixtures of metal-organic ligands that can chemically react with oxygen and settle on the surface site to form layers of metal oxides. Due to its durability and compatibility, MOCVD has proven to succeed in depositing thin films for several industrialised applications.[23,96] However, an essential requirement of the CVD process is the availability of suitable precursor that possesses

a number of demanding properties. More specific details of the properties of an ideal precursor are further described in chapter 4, section 4.1. In a conventional MOCVD reactor, of the type used for depositing metal oxides, the precursor is contained in a stainless steel container (bubbler). Due to the usually high evaporating temperature of the precursor, for an efficient oxide deposition, the bubbler and inlet pipes are heated and held at high temperature (e.g., 150-250°C) throughout the MOCVD process. The majority of metal precursors, however, are unable to withstand heating for long periods and often undergo thermal decomposition in the bubbler or in the inlet pipes leading to reactor blockages and poor oxide layer uniformity. This problem of premature thermal decomposition, associated with the low volatility of the precursor, can be overcome by the use of liquid injection MOCVD.[83,102,105,106] The technique utilizes a point of use vaporization, in which the precursor solution is usually held at room temperature. During the MOCVD process, the precursor is delivered at a precisely controlled rate and quantity into a heated evaporator and is later transported by a carrier gas into the reactor zone. Therefore liquid injection MOCVD system offers a wider choice of precursors and has been widely used to fabricate metal oxide thin films.[103,106,107] However, the method leads to additional requirements that the precursors must be soluble and stable for long periods in the chosen solvent. In addition, the presence of a single heated evaporator at a fixed temperature makes it important that co-precursors, used for the growth of multi-component oxides, also evaporate in a similar temperature regime. Otherwise, it would be difficult to control the composition of the deposited complex oxides. The schematic of the liquid injection CVD (LI-CVD) system is illustrated in Fig 2.1.1.

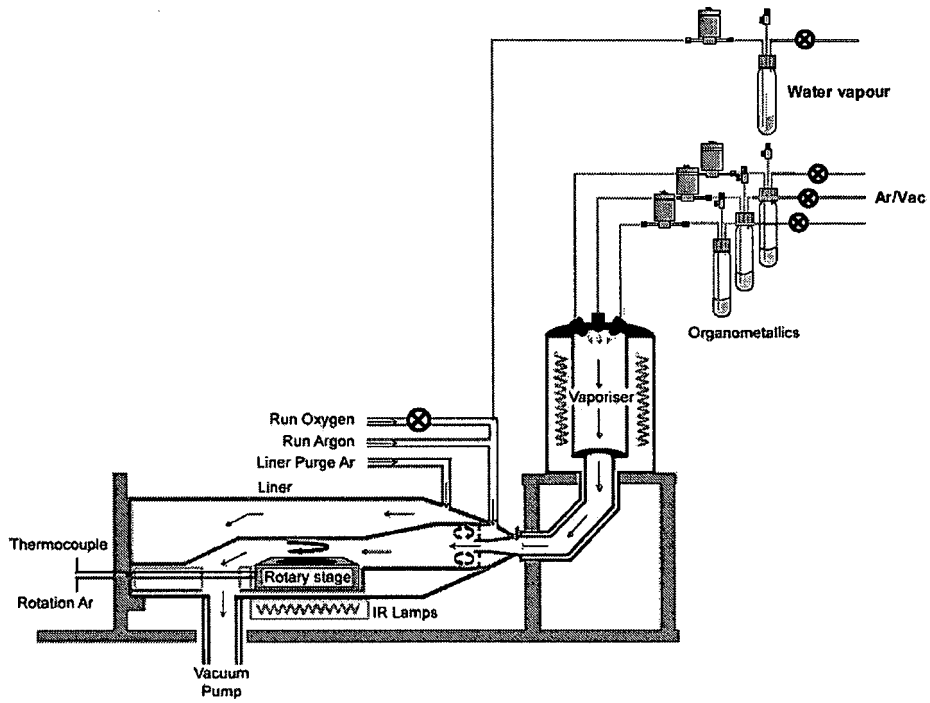

Figure 2.1.1. A schematic diagram of a liquid injection MOCVD reactor, after Potter et al.[102]

Despite the potential of the MOCVD process, atomic layer deposition (ALD) is swiftly becoming the technique of choice for the deposition of high-k dielectric oxides.[47,104,108] The technique was originally developed to meet the needs of producing high-quality and large area flat panel displays based on thin film electroluminescence (TFEL).[109] However, ALD has also been used in depositing alumina (Al_2O_3) in a current mass production of dynamic random access memory (DRAMs).[110] ALD is a type of chemical vapour deposition process based on sequential self-terminating surface reactions. ALD uses pulse and purge sequences, which constitute an ALD half-cycle, to produce one atomic monolayer layer at a time. The surface-controlled ALD mechanism is corroborated by the fact that the precursor dose has no effect on the growth rate, providing that the surface is saturated. This is the so called 'ALD-window', indicating the temperature range where film growth ensues by

the self-limiting process as shown in Fig. 2.1.2. ALD process are typically carried out in the 200°C to 400°C temperature range in order to avoid either condensation or thermal decomposition of precursors.[102-104] However, several studies have demonstrated that a distinct ALD window could not be easily obtained.[103,111] The deposition rate is still largely affected by the depositing temperature, nevertheless, it can still be used for self-limiting ALD processes. This phenomenon has been explained by the high reactivity towards reactive surface site, typically the hydroxyl (OH) group, the concentration of which is dependent of the deposition temperature.[112] In the work reported in this thesis, various high-k dielectric thin films were deposited using both liquid injection MOCVD and ALD. The growth rates are expressed, where relevant, in terms of (i) nanometer per hour (nm/hr); or (ii) nanometer per mole. Typically, the 'nm/hr' unit is often used to compare growth rates at different growth temperatures. The 'nm/mole' unit indicates the film growth with respect to the amount of remaining precursor solutions and is often used to compare growth rates from different processes. More detailed descriptions (including, where relevant, growth conditions and pulsing sequences) can be found separately in chapters 4 and 5.

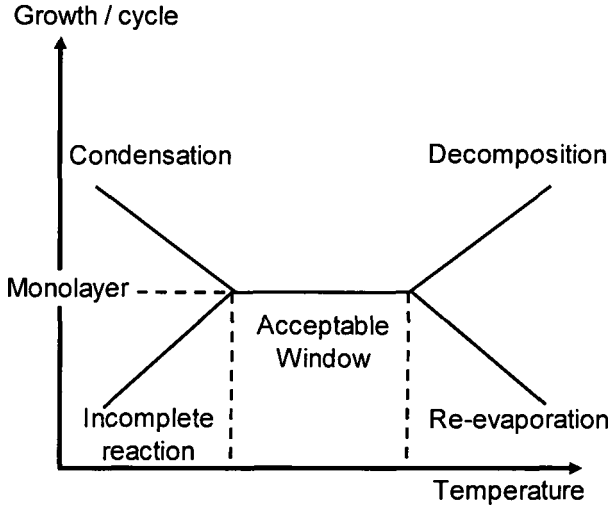

Figure 2.1.2. A schematic of an ALD processing window.

2.2. PROCESS TREATMENT – ANNEALING

Annealing is generally a heat treatment process, widely used in semiconductor device fabrication, wherein material properties are altered by heating, maintaining at a suitable temperature and then cooling. Annealing is used to relieve internal stresses, passivate electronic states and refine the structure of the deposited material in order to improve its electrical properties. Annealing treatment can be designed for different effects such as dopant activation, film densification and crystal phase transition. Annealing can be categorized into (i) rapid thermal annealing (RTA); and (ii) post deposition annealing (PDA) and post metallization annealing (PMA).

RTA is a heat treatment process, using an arc lamp or halogen lamp, at high temperatures (e.g., > 1000°C) on a timescale of several seconds or less on a single wafer. The objective of RTA is mainly to incorporate dopant atoms (e.g., boron or arsenic) into substitutional positions in the crystal lattice, resulting in drastic changes in the electrical properties of the semiconductor devices. For sub-65 nanometre production, it is becoming necessary to reduce thermal budget during heat treatment process in order to minimize the short channel effects. A variant of RTA is spike annealing (SA), in which the temperature is rapidly ramped up and down, and this has recently been employed during the dopant activation step.[30,113,114] However, different types of other RTA methods (e.g., flash annealing, solid phase epitaxial regrowth and laser thermal annealing)[115,116] are also being considered as the need for shallower junctions in MOSFET becomes greater.

PDA and PMA are heat treatment processes used in semiconductor device fabrication and are commonly exercised in a furnace on a timescale of several minutes. The objective of furnace annealing, prior to and after gate metal deposition, is mainly to refine the structure of the

deposited material, to study the crystal phase transition and passivate electronic states. Several types of defects can also be formed during deposition process steps, such as gate deposition and patterning of metal, as illustrated in Fig. 2.2.1.

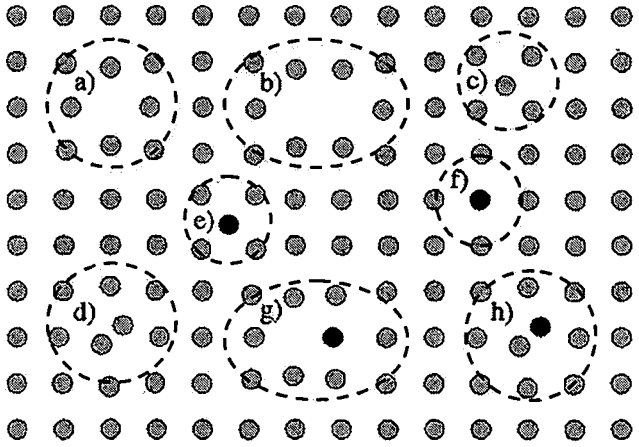

Figure 2.2.1. A schematic of different types of defects: a) vacancy, b) di-vacancy, c) self-interstitial, d) interstitialcy, e) impurity interstitial, f) substitutional impurity, g) impurity vacancy pair, h) impurity self interstitial pair.

Different types of gases are used in annealing semiconductor devices, which typically include oxygen (O_2),[117,118] nitrogen (N_2),[119,120] deuterium (D)[121] and forming gas,[122] depending on the designated purpose of the anneal. Since oxygen vacancies often act as shallow donors in high-k dielectric layer, annealing in O_2 ambient can partially remove oxygen vacancies in the layer and will improve electrical characteristics.[117,123] However, there is also a tendency for the growth of the interfacial layer as a trade off.[124] This therefore restricts the usefulness of O_2 annealing of gate oxides if the minimum equivalent oxide thickness (EOT) below 1.5nm was to be achieved. The effect of incorporating nitrogen into the deposited films has been studied extensively.[125-127] It was demonstrated that nitrogen anneal, not only resulted in a good barrier for interfacial reaction and dopant diffusion, but it also alleviated the issues of thermal

stability and enhanced the dielectric constant without increasing the EOT. Despite the latter advantages, however, nitrogen incorporation may induce extra charges in the gate dielectric and so cause a shift in the flatband voltage, which limits its useful applications. Forming gas, a mixture of up to 10% hydrogen in nitrogen, is used mainly to drive out moisture and oxygen for processes that need the properties of hydrogen gas without the explosion hazard. Effects of forming gas anneal (FGA), on charges in high-k stacks, have been widely studied. FGA has been shown to reduce the interface charge and improving carrier mobility effectively due to passivation by hydrogen (H^+) ions at both interfaces.[122,128,129] Nonetheless, both PDA and PMA processes can enhance the degree of crystallization if the excess thermal energy is given, thereby generating additional defects, that will result in a reduction of breakdown voltage and an increase of the gate leakage currents. The phase transition from an amorphous to a crystalline structure is thus a key issue for the replacement materials of SiO_2. The search for optimum time and temperature conditions remains a challenging task, as different materials possess different degree of crystallization. Recent work has also reported improvements in the reliability of deuterium annealed MOS capacitors, yielding less charge trapping and interface states. The improved reliability is attributed to the heavy mass effect of deuterium in Si-D bond, which results in a higher bond energy and make the devices less susceptible to hot electron induced defects. Therefore, it has a potential for future use in a fabrication process.[130] Thermal annealing effects are therefore other important issues that remain to be further investigated.

2.3. FILM CHARACTERIZATION

The oxide thin films were analyzed by various techniques for their composition, thickness, structure and electrical properties. Table 2.3.1 lists the techniques used in this thesis and also summarizes the information that may be obtained using each technique. Not all techniques were used for every sample.

The thickness and crystallinity of the deposited films was partly determined, using Spectroscopic Ellipsometry (SE), by measuring the optical reflectance spectra (JA Woollam multiple angle instruments) in the wavelength range of 185 to 1700 nm. The data acquisition and analysis was made using the WVASE32 software. A general oscillator model, which consisted of three Tauc Lorentz and a Cauchy component,[131] was employed for extracting the optical properties of the layers. This models the dielectric function of a film or substrate as a linear summation of real and complex terms, each of which is a function of wavelength (or photon energy).

Technique	Information obtained
SE	Film thickness, crystallinity, relative permittivity
MEIS	Thickness, ion movements, composition
XRD	Crystallinity extent, crystalline phase
TEM	Thickness of interfacial layer, microstructure
AES	Impurity contamination level, composition
C-V	Dielectric properties of the bulk stack and interface
I-V	Leakage current, electric breakdown strength, conduction mechanism

Table 2.3.1. Film characterization techniques used.

Thickness and the redistribution of ion species in the dielectric were examined using Medium energy ion scattering (MEIS). MEIS experiments were carried out using the Daresbury MEIS facility.[132] A 200 keV He^+ ion beam was employed with a current of up to 200 nA and a dose per data set of 10 μC. The angle and energy of the scattered ions were determined using a toroidal electrostatic energy analyzer with a position-sensitive detector. This allowed the simultaneous collection of ions from a 24° range of scattering angles and with a range of energies equal to 2% of the pass energy. The samples were aligned to the ion beam along the [100] channelling direction of the silicon substrate and the electrostatic analyzer was positioned to record data along the [111] blocking direction.

Crystallite orientations and crystallinity of the deposited films were assessed by x-ray diffraction (XRD) using nickel-filtered Cu Kα radiation (λ=1.5405Å) with a 2θ increment of 0.2° per second in a Rigaku miniflex x-ray diffractometer. Transmission electron microscopy (TEM) was also applied in order to examine the cross-section of an ultra thin sample as well as the interfacial layers between selected deposited films and the silicon substrate. TEM samples were prepared by hand-grinding to ≈ 40μm and final thinning by using a Gatan precision ion polishing system (PIPS). Cross section transmission electron images were obtained using JEOL 2000FX operated at 500kV.

Auger electron spectroscopy (AES) was used to obtain more information on residual carbon and hydrogen impurities. AES was carried out on a Varian scanning Auger spectrometer. The atomic compositions quoted are from the bulk of the film (typically > 20 nm depth), free from surface contamination, and were obtained by combining AES with sequential argon ion bombardment until comparable compositions were obtained for consecutive data points. Compositions were determined

using experimentally derived factors based on powder reference materials.

To assess the electronic properties of the deposited films, MOS capacitors (MOSCs) were fabricated by thermal evaporation of metal gates (aluminium or gold) through a shadow mask with an area of 4.9×10^{-4} cm^2. The backside contact of the Si wafer was cleaned with a buffer HF solution and subsequently was deposited a 2000Å thickness of Al film by thermal evaporation to minimize the effect of series resistance. High frequency capacitance-voltage (C-V) measurements were conducted using a HP4192 impedance analyzer with a 30mV RMS ac probe signal. Measurements were performed in parallel mode from a strong inversion towards a strong accumulation (vice versa), with a sweep rate of 0.05 V/s at various frequencies (1kHz-1MHz). Current-voltage measurements (I-V) were performed at room temperature using a Keithley K230 programmable voltage source and a 617 type electrometer. In addition, an automated hot chuck and standard thermocouple were incorporated into the I-V equipment for I-V measurements at elevated temperatures.

2.4. CURRENT CONDUCTION MECHANISMS THROUGH INSULATORS

High field conduction can be broadly divided into two categories:[133] (i) current that is limited by the events at the interfaces of the insulator (electrode limited); and (ii) current that is limited by the events in the bulk of the insulator (bulk-limited). In electrode limited currents such as Fowler-Nordheim (F-N) conduction, which have been frequently observed in good quality gate dielectrics,[134] electrons have a finite probability of passage from the semiconductor or metal contact through the energy gap of the insulator into the conduction band. The presence of an intense electric field reduces the energy gap of the insulator, thereby allowing the

tunnelling process to take place. Electrode limited currents show polarity dependence due to different barriers against injection, but they depend very little on temperature. In very thin gate oxides, direct tunnelling from channel to gate is also probable.[135] The latter tunnelling processes are depicted in Fig. 2.4.1.

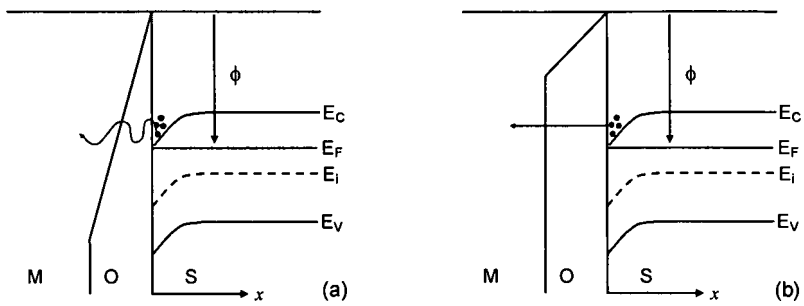

Figure 2.4.1. Diagrams of electrode limited current conduction processes: (a) Fowler-Nordheim conduction; (b) Direct tunnelling. The potential barrier height for electron emission is denoted with Φ.

The bulk limited current conduction is expected to be dominant in insulating thin films, where they have a large trap density and are thick enough to avoid direct tunnelling.[136] The high density of traps hinders the transport of electrons in the conduction band by drift and diffusion mechanisms, but allows trapping and detrapping (hopping) of electrons to become the dominant process that controls the current conduction in the insulating films. These bulk limited conduction mechanism are strongly dependent on temperature. Several types of bulk limited conduction mechanisms have been found which include trap-assisted (TAT) tunnelling,[137] Poole-Frenkel conduction (P-F),[138] and tunnelling-assisted Poole-Frenkel emission (TAPF).[139] In particular, the P-F conduction behaviour has been frequently observed in HfO_2 due to the high density of traps.[140,141]

In the Poole-Frenkel effect, electrons that are injected into the conduction band of the insulator can be trapped into shallow defects and transported through the insulator via a hopping process between these traps. This conduction mechanism is known as the electric field enhanced thermal hopping. However, the existence of an experimentally observable P-F effect demands the presence of donor-like states in the material, since only these states can have Coulombic potential which lead to the characteristic dependence.[142]

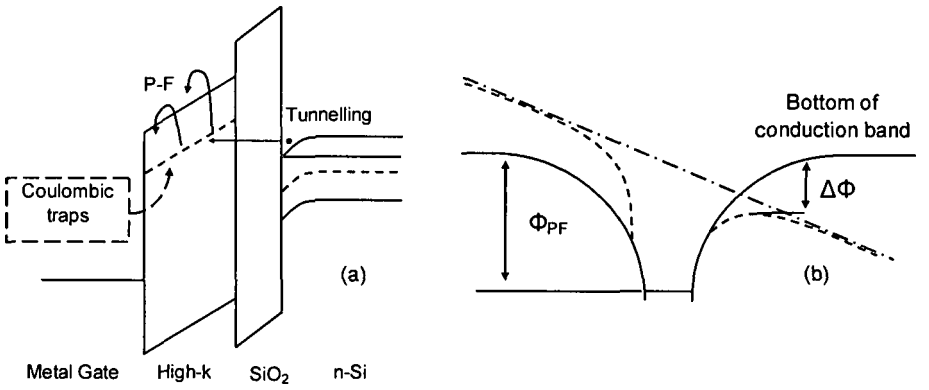

Figure 2.4.2. Schematic representation of Poole-Frenkel (P-F) conduction mechanism for substrate injection leakage current in high-k/SiO_2 stacks: (a) direct tunnelling plus P-F hopping effect via shallow traps that are located below the Si conduction band; (b) Mechanism of P-F effect. The solid line represents a Coulombic barrier without a field. The dashed line shows the effect of an electric field on the barrier. The slope of the dash-dot line is proportional to the applied field. The P-F trap level and the barrier attenuation are denoted with Φ_{PF} and $\Delta\Phi$ respectively.

The P-F mechanism predicts an increase in leakage current with increasing electric field due to the lowering of the Coulombic trap in the oxide (Fig. 2.4.2).[138] The current density due to P-F emission can be described as:[143,144]

$$J_{PF} \sim J_0 \exp\left(\beta_{PF} E^{1/2}\right) \exp\left(-q\phi_{PF}/rk_B T\right) \qquad (2.4.1)$$

where J_0 is the low-field current density (Acm^{-2}) that is related to the applied field E (Vcm^{-1}) through the low field conductivity, k_B is the

Boltzmann constant (JK^{-1}), T is the absolute temperature (K), and Φ_{PF} is the trap level (eV) of the P-F site. r denotes the coefficient that ranges from 1 to 2 depending on the position of the Fermi level. When the insulator contains a non-negligible number of traps that are lower in energy level than the bottom of conduction band of semiconductor and when the concentration of acceptor levels is small compared to the density of donor level and free electrons (e.g., $N_A << N_D$ and $N_A << n$), the coefficient equals to 2.[143] The adoption of this coefficient is based on two assumptions,[144] which are: (i) the carrier may be assumed to be trapped by the nearest centre down-stream (e.g., the distance travelled is independent of the applied field and the current is directly proportional to the probability of emission); and (ii) the liberated carriers travel for a constant period of time before being re-trapped. The conduction is now called the modified Poole-Frenkel conduction. Since in the samples considered this mechanism is more probable, the modified Poole-Frenkel formula is adopted here. The Poole-Frenkel field lowering coefficient, β_{PF}, can be expressed as:

$$\beta_{PF} = (q/2k_BT)\cdot(q/\pi\varepsilon_0\varepsilon_i)^{1/2} \qquad (2.4.2)$$

where ε_0 is the permittivity of free space (Fcm^{-1}) and ε_i is the dynamic permittivity of the high-k layer (i.e., $\varepsilon_i \sim n^2$ where n is the refractive index and assuming zero absorption coefficient). The field lowering coefficient (β_{PF}) of the Poole-Frenkel conduction mechanism can be found experimentally by finding the gradient of the Poole-Frenkel plot, which in turn leads to the extraction of ε_i.

2.5. EXTRACTION OF INTERFACE STATE DENSITY BY TERMAN'S METHOD

Terman[145] developed and used the high frequency capacitance method for determining density of interface state (D_{it}) profiles. In the high frequency capacitance method, capacitance is measured as a function of gate bias with frequency fixed at a high enough value so that interface traps do not respond. The ideal capacitance-voltage (C-V) curve is calculated for the same doping density (N_D) and oxide thickness, but without interface traps. The D_{it} profile of the MOS capacitor can then be extracted by comparing the experimental C-V curves with the theoretical ones using the following relation:

$$D_{it}(\psi_s)=\left\{C_{ox}\left[\left(\frac{d\psi_s}{dV_G}\right)^{-1}-1\right]-C_s(\psi_s)\right\}\Big/q \qquad (2.5.1)$$

where ψ_s is the surface band bending, V_G is the applied gate bias, q is the electronic charge, C_s is the substrate capacitance and C_{ox} is the capacitance of the dielectric layer measured in strong accumulation. The position of the Fermi level (E_C-E_t) from the conduction band edge, with respect to the mid-gap level at the silicon surface (Fig. 2.5.1), was also calculated using the relation:

$$\frac{E_c-E_t}{q}=\frac{E_g}{2q}+\psi_s-\phi_B \qquad (2.5.2)$$

where E_g is the silicon bandgap (~1.1eV) and Φ_B is the bulk potential (calculated using Eq. 3.1.33).

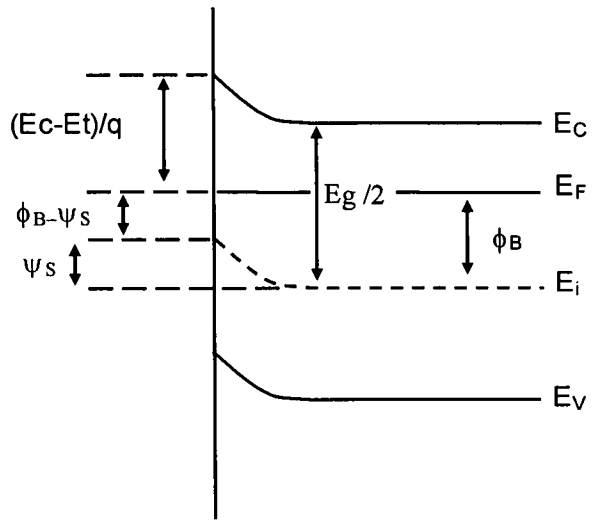

Figure 2.5.1. Band bending diagram of n-type silicon showing the position of the interface trap level density as a function of energy in the silicon bandgap.

Chapter 3 – C-V modelling and C-V reconstruction model

3.1. CLASSICAL C-V MODELING FOR AN N-TYPE MOS CAPACITOR

Integrated circuit characterization typically includes capacitance-voltage (C-V) assessment, which has been one of the major factors that have led to stable and high performance silicon integrated circuits. Although metal-oxide-semiconductor capacitors (MOSC) are simple to fabricate, the MOSC and the MOS field-effect-transistor (FET) also exhibit similar sensitivities to doping profiles, oxide charges and interface traps, whose control are so critical to proper MOSFET operation. For that reason, the MOS capacitor provides direct assessment and monitoring of the MOS system as identical processing steps to that of the integrated circuit may be used. The current semiconductor technology trend towards thinner dielectric layers is creating a demand for a tighter process control. Due to this fact, MOS C-V is an important tool for monitoring process variables, controlling contamination and studying device models.[145-147]

In this chapter, following Nicollian and Brews[148], the steady state characteristics of the n-type MOS capacitor are derived and discussed using a classical approach. In this context, the steady state is defined so that the macroscopic parameters of a system that are either time independent or vary sinusoidally in time with time-independent amplitudes. This approach lays the groundwork for the later chapters that discuss measurements using the MOS capacitor.

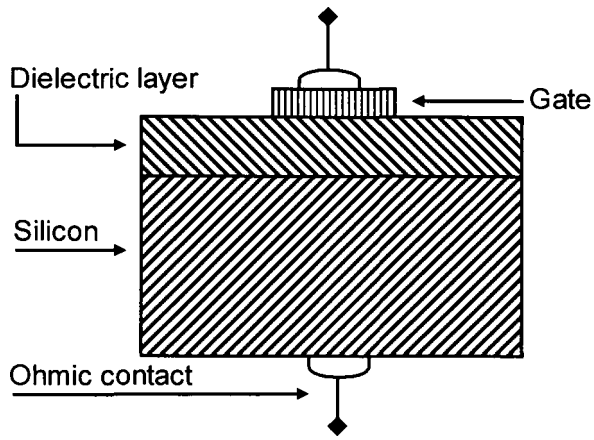

Figure 3.1.1. Cross section of a MOS capacitor

Figure 3.1.1 illustrates a typical MOS capacitor, which usually consists of the dielectric (oxide) layers sandwiched between a gate electrode and a silicon substrate. The differential capacitance can be measured by applying the gate bias that is superimposed upon a small alternating *ac* voltage. The amplitude of this *ac* signal, however, must be in the small signal range to produce a linear response of *ac* current to *ac* voltage. The mathematical expressions for the equivalent circuit representing the ideal MOS capacitor (Fig. 3.1.1) can be formulated as:

$$\frac{1}{C} = \frac{1}{C_s} + \frac{1}{C_{ox}} \tag{3.1.1}$$

where C and C_{ox} denote the total capacitance per unit area (Fcm^{-2}) of the MOS capacitor and the oxide capacitance per unit area (Fcm^{-2}) respectively. C_s is the silicon substrate capacitance per unit area (Fcm^{-2}) that is dependent on the surface band bending [$\psi(x)$] established by gate bias. The band bending [$\psi(x)$], being the total potential difference between the silicon surface and the bulk, is defined as:

$$\psi(x) = \phi(x) - \phi_B \qquad (3.1.2)$$

where $\Phi(x)$ denotes the potential at any point x in the depletion layer with respect to its value in the bulk (Φ_B) as depicted in Fig. 3.1.2.

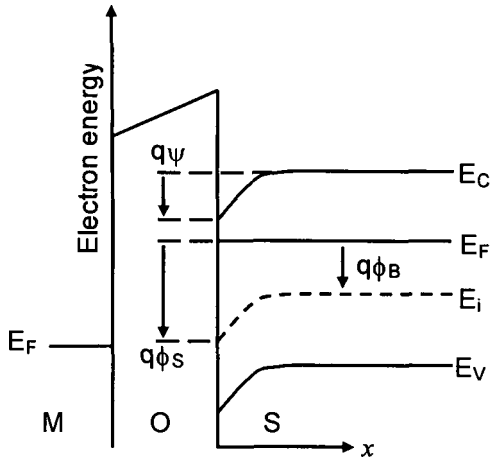

Figure 3.1.2. An energy diagram of the MOS system, for n-type silicon, in accumulation. The various potentials defined in the text are shown along with their sign conventions as indicated by the arrows. An arrow pointing down denotes positive potential and vice versa.

Silicon is treated as a semi-infinite homogeneous crystal in thermal equilibrium, with its surface represented by the plane at $x = 0$ and the bulk by positive value of x. This narrows the problem into one dimension, so that the Poisson equation can be applied and solved under the specified conditions where the band bending approximation is valid. The band bending approximation[148] assumes that the density of states in the conduction and valence bands are not changed by an electric field. The only effect of an electric field is to shift all the energy levels in the conduction and valence bands by a constant amount determined by the potential at each given point in silicon. However, two cases where the band bending approximation fails are: (i) surface quantization, where the density of states is changed by the electric field; and (ii) very heavy

doping, where the impurities can produce band tails. Neither of these cases is treated here. The surface potential (Φ_s) as a function of distance x is given by the Poisson equation in one dimension as:

$$\frac{d^2\phi_s(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_0\varepsilon_s} \tag{3.1.3}$$

and

$$\rho(x) = q\left[p(x) - n(x) + N_D - N_A\right] \tag{3.1.4}$$

where ε_0 is the dielectric permittivity of free space (8.85×10^{-14} Fcm^{-1}) and ε_s is the dielectric permittivity of silicon (11.9). $\rho(x)$ is the charge density (Ccm^{-3}) composed of immobile ionized donors (N_D) and acceptors (N_A), mobile hole density [$p(x)$] and electron density [$n(x)$]. Deep in the silicon bulk, for n-type, electron and hole densities follow the relation:

$$n(x) = n_i \exp\left(\frac{E_F - E_i}{kT}\right) = n_i \exp\left[\frac{q\phi(x)}{kT}\right] \tag{3.1.5}$$

and

$$p(x) = n_i \exp\left(\frac{E_i - E_F}{kT}\right) = n_i \exp\left[-\frac{q\phi(x)}{kT}\right] \tag{3.1.6}$$

where E_F is the extrinsic Fermi level (eV). The intrinsic energy level (E_i) is parallel to both bands throughout the silicon (eV). q is the electronic charge (C), n_i is the intrinsic concentration (cm^{-3}) in the uncharged semiconductor where the concentrations of electrons and holes are equal. The Boltzmann's constant (8.617×10^{-5} eVK^{-1}) and the absolute temperature of the system (K) are symbolized by k and T respectively. It is also convenient to define the surface potential and the band bending in silicon in dimensionless form, as shown in Eq. 3.1.7.

$$u(x) = \frac{q\phi(x)}{kT} \quad and \quad v(x) = \frac{q\psi(x)}{kT} \tag{3.1.7}$$

Using the definitions in Eqs. (3.1.2) and (3.1.7), Eqs. (3.1.5) and (3.1.6) can be written as:

$$n(x) = n_i \exp[u(x)] = N_D \exp[v(x)] \tag{3.1.8}$$

and

$$p(x) = n_i \exp[-u(x)] = N_A \exp[-v(x)] \tag{3.1.9}$$

The condition of charge neutrality must always exist in the bulk, that is, Φ_s will approach the bulk potential (Φ_B) as the distance (x) move towards semi-infinity [$\Phi_s(\infty) = \Phi_B$ and $\rho(x) = 0$]. Therefore, deep in the bulk ($x \rightarrow \infty$), Eq. (3.1.4) becomes:

$$n(\infty) - p(\infty) = N_D - N_A \tag{3.1.10}$$

when Eqs. (3.1.8) and (3.1.9) are used, Eq. (3.1.10) becomes:

$$N_D - N_A = n_i[\exp(u_B) - \exp(-u_B)]. \tag{3.1.11}$$

As $[\exp(u_B) - \exp(-u_B)] = 2\sinh(u_B)$, Eq. (3.1.11) becomes

$$N_D - N_A = 2n_i \sinh(u_B). \tag{3.1.12}$$

In general, for any value of x, Eq. (3.1.12) can be written as:

$$n(x) - p(x) = 2n_i \sinh u(x). \tag{3.1.13}$$

Substituting Eqs. (3.1.12) and (3.1.13) into (3.1.3), Poisson's equation can now be expressed in the dimensionless form as:

$$\frac{d^2u(x)}{dx^2} = \lambda_i^{-2}[\sinh u(x) - \sinh u_B] \tag{3.1.14}$$

and λ_i, the intrinsic Debye length (cm), is defined as:[149]

$$\lambda_i = \left(\frac{\varepsilon_0 \varepsilon_s kT}{2q^2 n_i} \right)^{1/2} . \qquad (3.1.15)$$

In order to find the electric field (F_s) at the semiconductor surface, Eq. (3.1.14) needs to be integrated with appropriate boundary conditions that ensure charge neutrality in the bulk. With the use of an integrating factor and boundary conditions and integrate from the surface to the bulk, one obtain the expression as:[148]

$$\int_{du_S/dx}^{0} d\left(\frac{du}{dx}\right)^2 = 2\lambda_i^{-2} \int_{u_S}^{u_B} [\sinh u(x) - \sinh u_B] du \qquad (3.1.16)$$

and

$$du_s/dx = (q/kT)F_s . \qquad (3.1.17)$$

Integrating each term in Eq. (3.1.16) yields the expression of F_s as:

$$F_s = Sgn(u_B - u_s)(2)^{1/2} \frac{kT}{q\lambda_i} [(u_B - u_s)\sinh u_B - (\cosh u_B - \cosh u_s)]^{1/2} . \qquad (3.1.18)$$

where $Sgn(u_B-u_s)$ is the sign of the difference between the dimensionless surface and bulk potentials (e.g., $Sgn(u_B-u_s)$ is positive for $u_s < u_B$ and vice versa). Eq. 3.1.18 can be further simplified by writing in terms of a dimensionless electric field [$F(u_s,u_B)$] as:

$$F_s = Sgn(u_B - u_s)(2)^{1/2} \frac{kT}{q\lambda_i} F(u_S, u_B) \qquad (3.1.19)$$

and

$$F(u_S, u_B) = (2)^{1/2} [(u_B - u_s)\sinh u_B - (\cosh u_B - \cosh u_s)]^{1/2} . \qquad (3.1.20)$$

Eq. (3.1.20) appears to be rather complicated. However, the meaning of the parameters in the expression of F_s can be further clarified, using Eqs. (3.1.13), in terms of electron (n_B) and hole (p_B) densities in the silicon bulk correspondingly so that:

$$\sinh u_B = \frac{n_B - p_B}{2n_i}, \cosh u_B = \frac{n_B + p_B}{2n_i}, \cosh u_S = \frac{n_S + p_S}{2n_i}. \qquad (3.1.21)$$

Substituting Eq. (3.1.21) into Eq. (3.1.20) yields:

$$F(u_S, u_B) = \left(\frac{n_B}{n_i}\right)^{1/2} \left[(u_B - u_S - 1) - \frac{p_B}{n_B}(u_B - u_S + 1) + \frac{n_S}{n_B} + \frac{p_S}{n_B} \right]^{1/2}. \qquad (3.1.22)$$

However, the bulk doping concentration in n-type is largely donor type. Therefore the electron density in bulk can be regarded as $n_B = N_D$ and the ratio p_B/N_D is approximate to zero, so that Eq. (3.1.22) becomes:

$$F(u_S, u_B) = \left(\frac{N_D}{n_i}\right)^{1/2} \left[(u_B - u_S - 1) + \frac{n_S}{N_D} + \frac{p_S}{N_D} \right]^{1/2} \qquad (3.1.23)$$

or writing in terms of the dimensionless band bending (v) as:

$$F(v) = \left(\frac{N_D}{n_i}\right)^{1/2} \left[(-v - 1) + \exp(v) + \exp(-v)\left(\frac{n_i}{N_D}\right)^2 \right]^{1/2} \qquad (3.1.24)$$

Eqs. (3.1.19) and (3.1.24) can then be used to calculate the silicon surface charge density per unit area (Q_s) according to Gauss's law as:

$$Q_S = \varepsilon_0 \varepsilon_s F_s \approx Sgn(-v)\left(\frac{kT}{q}\right)\frac{\varepsilon_0 \varepsilon_s}{\lambda_i} F(v) \qquad (3.1.25)$$

Surface differential capacitance per unit area is expressed as:

$$C_S = -\left(\frac{\delta Q_S}{\delta v}\right)\left(\frac{\delta v}{\delta \psi}\right) = -\left(\frac{q}{kT}\right)\left(\frac{\delta Q_S}{\delta v}\right). \tag{3.1.26}$$

From Eqs. (3.1.25) and (3.1.26), one obtains:

$$C_S = -Sgn(-v)\left(\frac{\varepsilon_0 \varepsilon_s}{\lambda_i}\right)\frac{\delta}{\delta v}[F(v)]. \tag{3.1.27}$$

At low frequencies, *ac* changes are so slow that equilibrium is maintained and both majority and minority carriers follow changes in *ac* band bending. The expression for low frequency silicon surface capacitance can be found by differentiating Eq. (3.1.27) as:

$$C_S = \frac{\varepsilon_0 \varepsilon_s}{\lambda_n \sqrt{2}} \frac{\exp(v) - (n_i/N_D)^2 \exp(-v) - 1}{\left[(-v-1) + \exp(v) + \exp(-v)(n_i/N_D)^2\right]^{1/2}}. \tag{3.1.28}$$

where λ_n, the extrinsic Debye length (cm), is defined as:

$$\lambda_n = \left(\frac{\varepsilon_0 \varepsilon_s kT}{q^2 N_D}\right)^{1/2}. \tag{3.1.29}$$

At high frequencies, minority carrier generation cannot follow the measuring signal but can follow the slow d.c. sweep. The low and high frequency C-V curves are practically identical in accumulation, depletion and most weak inversion. This is because the minority carrier concentration in the depletion layer, of the latter cases, is negligibly small compared to majority carrier concentration. The major difference only occurs in weak to strong inversion where minority carrier concentration in the inversion layer at the oxide/Si interface becomes comparable to and exceeds majority carrier concentration. Similarly to low frequencies, the approximate expression for high frequency silicon surface capacitance can be found as:

$$C_S = \frac{\varepsilon_0 \varepsilon_s}{\lambda_n \sqrt{2}} \frac{\exp(v) - 1}{[(-v-1) + \exp(v)]^{1/2}}. \qquad (3.1.30)$$

Finally the corresponding gate bias, in relation with the calculated MOS capacitance using Eqs. (3.1.1), (3.1.25) and (3.1.28) or (3.1.30), is expressed as the sum of the voltages across the oxide and the silicon substrate as:

$$V_G = -\frac{(Q_s + Q_f + Q_{it})}{C_{ox}} + \psi + \phi_{MS}. \qquad (3.1.31)$$

where Q_f and Q_{it} are the oxide fixed charge density per unit area and the interface trap charge per unit area (Ccm^{-2}), respectively. In addition, the voltages due to the surface band bending (ψ) and the effect of work function difference between the metal gate and the semiconductor (Φ_{MS}) must be taken into an account. The work function difference, also equivalent to the ideal flatband voltage (V_{FB}), is generally described as:

$$\phi_{MS} = \phi_M - \chi - \frac{E_g}{2q} + \phi_B \qquad (3.1.32)$$

where Φ_M is the metal work function (V), χ is the electron affinity (V) and E_g is the energy gap in silicon (eV). The bulk potential Φ_B (V) is positive, for n-type, and is generally defined as:

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) \qquad (3.1.33)$$

Figure 3.1.3 shows the fit of calculated differential capacitance as a function of gate bias for a thermal oxide sample (SiO_2), taking into account the effect of oxide charge and interface trapped charge, for an n-type sample. The band bending (ψ) is also chosen to be the independent variable in order to calculate the theoretical C-V curve, although in

measurements, the gate bias (V_G) is the actual independent variable parameter. SiO_2 was thermally grown using dry oxidation in O_2 with Dichloroethylene (DCE) at 1100 °C on n-type Si substrate (100) with doping concentration of $7.5\times10^{15}cm^{-3}$. Samples were also cleaned prior to oxidation using standard FSI B mercury spray cleaner. MOS capacitors ($Al/SiO_2/n\text{-}Si$) were fabricated with an area (A) of 4.9×10^{-4} cm^2. Certain independently measured parameters (e.g., Q_{it}, Q_f and ε_k) were taken as adjustable values, chosen to fit theory to experimental values.

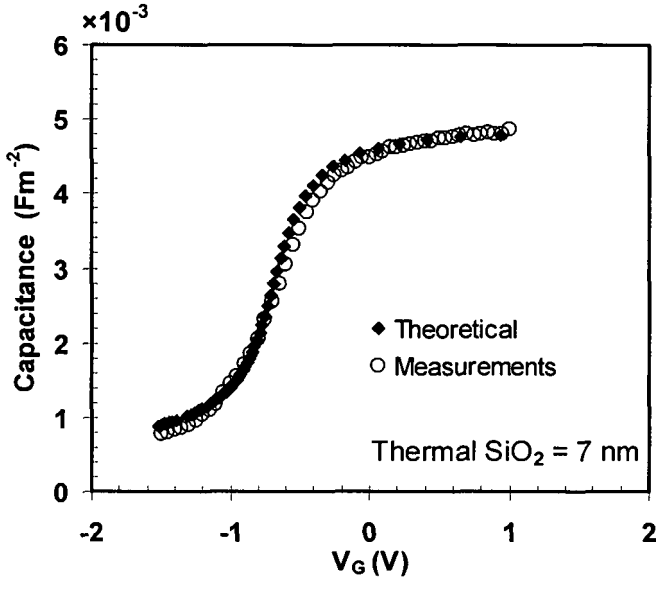

Figure 3.1.3. A comparison of a theoretical high frequency C-V curve, calculated using (3.1.1), (3.1.25), (3.1.30) and (3.1.31), with the experimental values. Capacitance was obtained at 1 kHz for [$Al/SiO_2/n\text{-}Si$] capacitors. The sample was thermally grown using dry oxidation in O_2 at 1100°C to achieve the oxide thickness (t_{ox}) of 7nm. The substrate area was 25 cm^2. The fitting values were as follow: (i) N_D of 7.5×10^{15} cm^{-3}; (ii) dielectric permittivity of 3.9; (iii) interface trap charge (Q_{it}) of 1×10^{-11} Ccm^{-2}; (iv) flatband voltage shift (ΔV_{FB}) of -0.17V.

Of those parameters, the doping concentration N_D is known least accurately. The inaccuracy results mainly from the impurity redistribution during the deposition process, however, the uniform doping assumption[148] is sufficient for doping concentrations in the range of

10^{15}-10^{16} cm^{-3}. In this case, the fitted value of N_D ($7.5\times10^{15}cm^{-3}$) was calculated iteratively from the measured C-V curve using the relation:

$$N_D = \frac{4}{A^2}\frac{kT}{q^2}\frac{1}{\varepsilon_o\varepsilon_s}\left[\frac{1}{C_{\min}} - \frac{1}{C_{\max}}\right]^{-2} \ell n\left(\frac{N_D}{n_i}\right) \qquad (3.1.34)$$

A flatband capacitance (C_{FB}), which refers to the associated capacitance of the MOS device measured at a specific flatband voltage (V_{FB}), is a universally accepted reference point on the C-V curve for comparison between the measured and the calculated C-V curves. The flatband capacitance per unit area (Fcm^{-2}), and its associated flatband voltage (V), can be found experimentally using the relation:

$$C_{FB} = \left(\frac{A}{C_{ox}} + \frac{\lambda_n}{\varepsilon_0\varepsilon_s}\right)^{-1}. \qquad (3.1.35)$$

According to Fig. 3.1.3 measurement data, the extracted V_{FB}, which takes into account the effects of work function difference, was found to be -0.6 V. The deviation from its ideal value (-0.45 V for the given doping concentration) suggests the presence of defects in the oxide, in this case being positive fixed charges. The density of oxide trapped charge (N_{OT}) that represents a figure of merit for the quality of a dielectric film, with larger values (e.g., $>10^{11}$ cm^{-2}) being an indication of a poorer dielectric,[85] was found to be 4.55×10^{11} cm^{-2} using Eq. 3.1.36.

$$N_{OT} = \frac{C_{ox}\Delta V_{FB}}{qA}. \qquad (3.1.36)$$

where ΔV_{FB} is the calculated flatband voltage shift from its ideal value (V).

3.2. RECONSTRUCTION MODEL FOR HIGH-K DIELECTRICS AND ORIGINS OF FREQUENCY DISPERSION

C-V measurements are a fundamental characterization technique for

MOS devices and are used widely for oxide thickness extraction,[150-152] mobility measurement[153] and interface trap characterization in the conventional thermal oxide.[145,154] However, the relentless scaling of SiO_2 in MOS devices has made it increasingly difficult to obtain accurate measurement due to a dramatic increase of direct tunnelling current through a thin gate dielectric layer. Solutions to this problem have been sought either by creating an accurate simulation model for the device that included quantum mechanical effects,[155-158] or by finding an equivalent circuit model that are sufficiently accurate for reliable gate dielectric parameter extraction.[159,160] The methods based on equivalent circuit models are extensions of the widely accepted C-V technique, where capacitance is first measured and the correction is then applied.

Unwanted frequency dispersion in SiO_2 has frequently been observed in C-V measurements.[159,161] Several models and analytical formulae have been thoroughly investigated for correcting the data from measurement errors. Attention has been given to eliminating the effects of series resistance,[148] oxide leakage,[159-161] undesired thin lossy dielectric layer between oxide and semiconductor,[162] polysilicon depletion[6,7] and surface roughness.[163] However, the recent introduction of high-k based dielectrics into production lines have renewed interest into frequency dispersion in particular at the accumulation region of the measured C-V curve.[106,164-166] To date, the causes of frequency dispersions still remain under discussion.

In this chapter, the causes of frequency dispersion in high-k dielectric stacks were investigated. The dependency of dielectric permittivity (ε_k) on measuring frequency, in particular, was proposed to be responsible for the dispersion in high-k based dielectrics. In order to validate the effect of ε_k dependency, the effects of the lossy interfacial layer between high-k dielectric and Si-substrate, together with the significance of silicon back metal contact, were also thoroughly investigated. Formulae are presented

to recover the actual capacitance from their measured values, together with the simulation using the proposed four-element equivalent circuit models.

Under normal circumstances, where an area of the substrate is large, reliable C-V measurements from a thick (> 8nm) SiO_2 gate dielectric can usually be obtained and are also reproducible. The measured capacitance (C_m) in this case shows no dispersion with varying frequencies, especially at the accumulation region. However, the measured capacitance becomes dependent on the measuring frequency when the sample size is drastically reduced as shown in Fig. 3.2.1. The SiO_2 samples, deposited by thermal oxidation as previously described, were cut into pieces with different areas, denoted by s1 (1 cm^2) and s2 (25 cm^2) respectively. The dispersion of the measured capacitance was evident only on the smaller s1 sample. It was also observed that the measured results were no longer reproducible for sample s1, regardless of the identical measuring conditions. This therefore affects the reliability of the measurement technique.

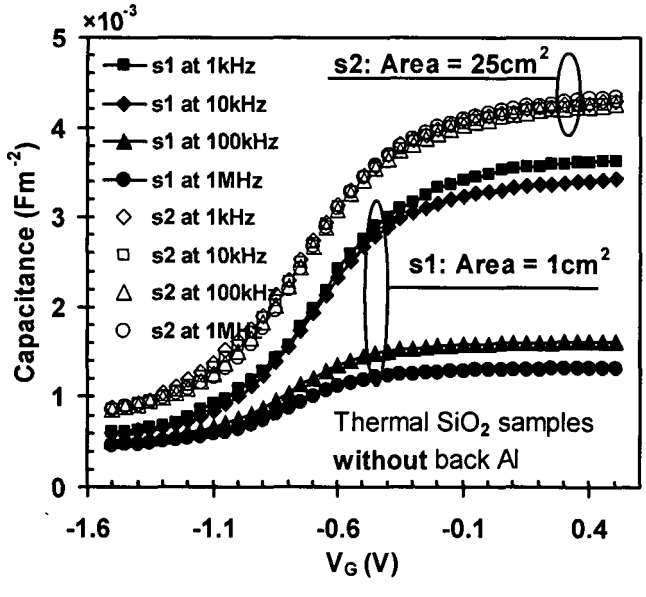

Figure 3.2.1. Frequency dispersion in C-V measurement observed in thermal oxide (SiO_2) samples. Dispersion was obtained only in the sample with a smaller substrate area, denoted by s1.

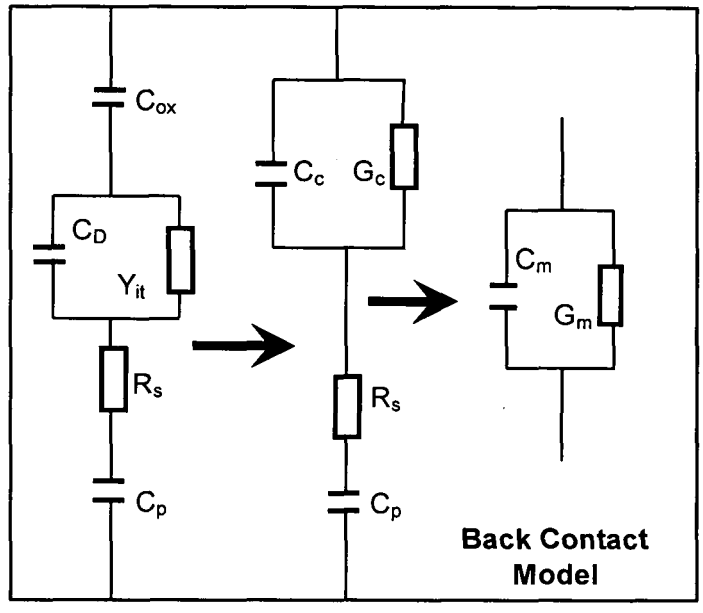

Figure 3.2.2. Equivalent circuit models, taking into account the presence of parasitic components from back contact imperfection with the addition of Cp and Rs.

In order to reconstruct the measured C-V curves for SiO_2, one must take into an account the "parasitic" components that may arise due to imperfections in the back contact. A correction may then be applied to the measured C-V curves in order to obtain their true values. Figure 3.2.2 shows an equivalent circuit of an ideal case in comparison with the actual measurement mode, where C_{ox} represents the actual frequency independent capacitance across the gate dielectric, C_D and Y_{it} are depletion capacitance and admittance due to interface states, and R_s is the resistance in silicon substrate. The presence of "parasitic" components, due to the back contact imperfection, is modelled by capacitance C_p. C_C, C_m, G_C, G_m refer to corrected or measured capacitance (Fcm^{-2}) and conductance (S) respectively. Following Kwa,[162] the corrected capacitance C_C is given by:

$$C_C = \frac{\left(\omega^2 C_m C_p - G_m^2 - \omega^2 C_m^2\right)\left(G_m^2 + \omega^2 C_m^2\right) C_p}{\omega^2 C_p^2 \left[G_m\left(1 - G_m R_S\right) - \omega^2 C_m^2 R_S\right]^2 + \left(\omega^2 C_m C_p - G_m^2 - \omega^2 C_m^2\right)^2} \qquad (3.1.37)$$

and

$$C_p = \frac{C_{ox}(G_{ma}^2 + \omega^2 C_{ma}^2)}{\omega^2(C_{ma}^2 C_{ox} - C_{ma}^2) - G_{ma}^2} \qquad (3.1.38)$$

where C_{ma} and G_{ma} are the capacitance and conductance measured in strong accumulation. The measured capacitance can be recovered, independent of measuring frequencies, by applying the correction according to the model as depicted in Fig. 3.2.3. Frequency dispersion, in this case, is simply removed by depositing aluminium (Al) at the back of the substrate. This demonstrates that once the parasitic components induced by series resistance effect are taken into account, it is possible to achieve the true capacitance values that are free from error. The measurements were also reproducible as shown in Fig. 3.2.4, indicating that the reliability of the C-V measurement can now be maintained. Therefore, back contact imperfection can be regarded as one of the causes of frequency dispersion as previously reported by Venkatesan.[167]

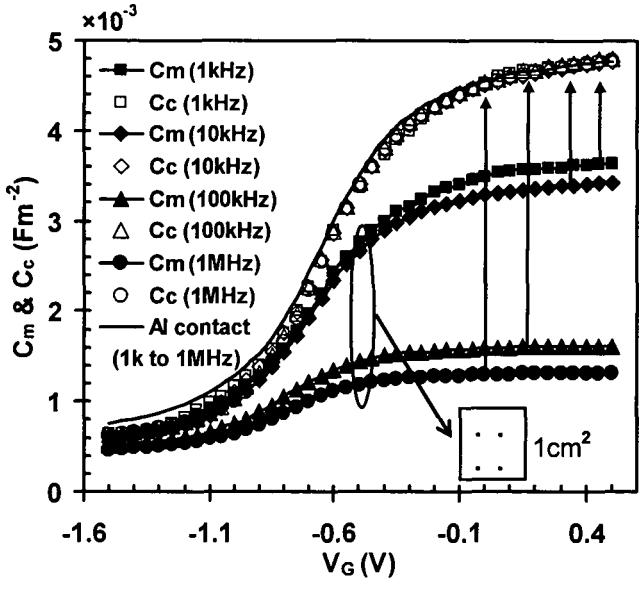

Figure 3.2.3. Extracted corrected capacitance curves based on data from Fig 3.2.1 and the model from Fig. 3.2.2. Dispersions were no longer observed after Cp and Rs were taken in consideration, or alternatively by depositing back aluminium (Al) contact (solid line).

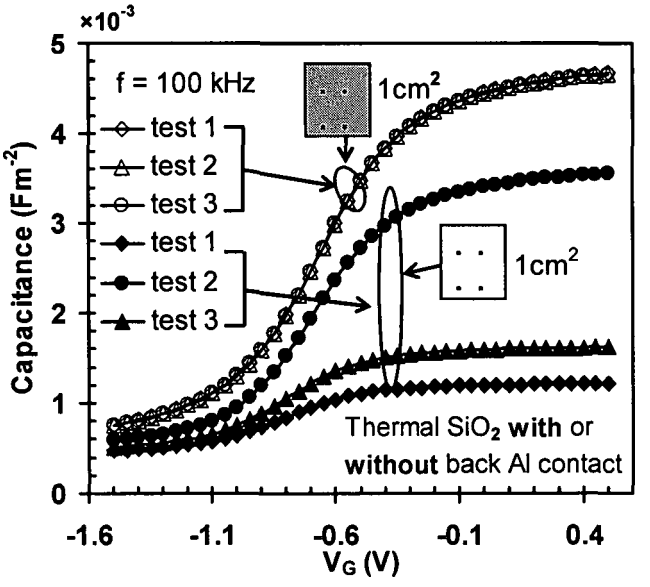

Figure 3.2.4. The reproducibility of the tested devices in either the presence or absence of back metal contact. Both of the sample sets were measured three times within 24 hours. Closed symbols (e.g., ▲) signify the C-V results from the sample without back aluminium contact (as also indicated by a blank square), while the opened symbols (e.g., ○) show the C-V results from the other sample with back aluminium contact (as also indicated by a shadow square).

Figure 3.2.5 shows the measured C-V curves of a $LaAlO_3/SiO_2$ capacitor with Al back contact. No frequency dispersion was observed when the high-k layer thickness is much greater than that of the interfacial layer thickness. That is, the role of interfacial layer capacitor (C_i) is negligible when compared with the high-k layer capacitor (C_{ox}). However, regardless of the Al back contact, a strong frequency dependence of accumulation capacitance was observed when the C_{ox} value is similar to that of C_i, as shown in Fig.3.2.6. Possible explanations for this occurrence can be resolved into three categories. Firstly, it may be due to the effect of direct tunnelling of carriers through the gate oxide. However, for gate oxides thicker than 3nm, it has already been shown that the direct tunnelling currents are small.[168,169] Since the devices tested have their physical oxide thicknesses greater than 7nm,[56,103] it can be safely assumed that tunnelling is not a significant issue here. Secondly,

the stability of LCR meter to accurately measure the capacitance can be disrupted in the presence of high leakage current. A common way to assess the accuracy of the measurement is by checking a dissipation factor (D) with the measured capacitance (C_m) and conductance (G_m). An approximation for the instrumentation error (%) in the presence of high oxide leakage is given by the formula:[170]

$$D = 0.1 \times \sqrt{1 + (G_m / \omega C_m)^2} \qquad (3.1.39)$$

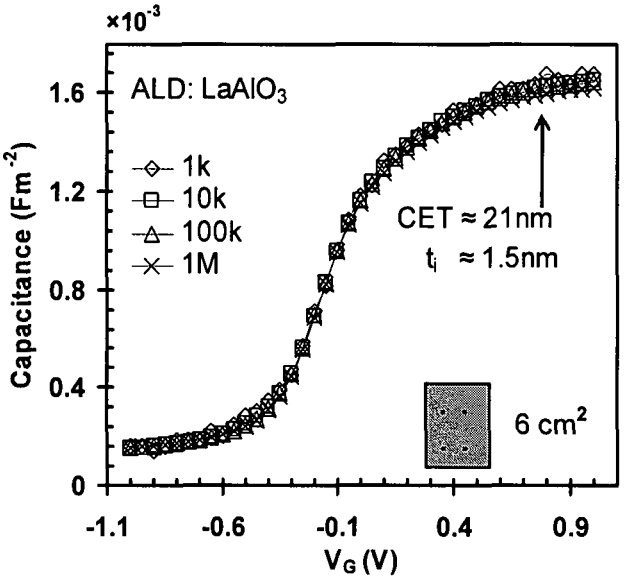

Figure 3.2.5. High frequency C-V curves for [Al/$LaAlO_3$/SiO_2/n-Si/Al] capacitors. $LaAlO_3$ was deposited by liquid injection MOCVD on Si (100) substrates at 350°C using 0.05M solution of $[LaAl(OPr^i)_6(Pr^iOH)]_2$ in toluene and H_2O. The sample received post metallization anneal with forming gas (FGA) at 400°C for 30 minutes. The $LaAlO_3$ film physical thickness was 45nm with 1.5nm SiO_x interfacial layer (t_i). The substrate area was 6 cm^2. Frequency dispersion in the C-V measurement was not observed in $LaAlO_3$ samples after back Al contact deposition.

It was found that the instrumentation errors for the tested devices were below 0.5% across the whole gate bias range and for all frequencies, indicating that the frequency dispersion of accumulation capacitance was not due to instrument error. Finally, the above considerations imply that frequency dispersion may be attributed to the presence of a thin lossy

interfacial layer (~1nm native SiO_2), in which the interfacial defects were caused by dislocation and intrinsic differences in bonding coordination across the chemically abrupt high-k/SiO_2 interface.

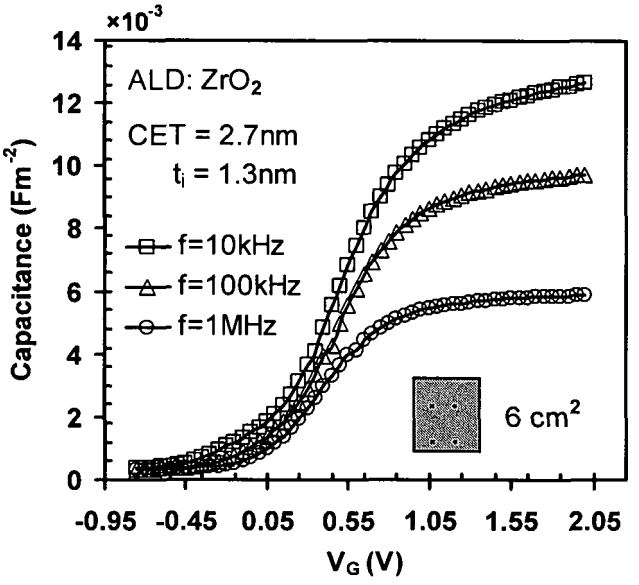

Figure 3.2.6. High frequency C-V curves for [Al/ZrO_2/SiO_2/n-Si/Al] capacitors. ZrO_2 was deposited by ALD on Si (100) substrates at 300°C using 0.05M solution of $Zr[(MeCp)_2Me(OMe)]$ in toluene and H_2O. The sample was post metallization annealed with forming gas (FGA) at 400°C for 30 minutes. The ZrO_2 film physical thickness was 8nm with 1.3nm SiO_x interfacial layer (t_i). The substrate area was 6 cm^2. Frequency dispersion in C-V measurement was observed in ZrO_2 samples after back Al contact deposition.

Based on this explanation, Fig. 3.2.7 shows a proposed four-element circuit model for high-k stacks, adapted from a dual frequency technique.[159,160] The dual frequency method imposes no theoretical limits on the choice of two measurement frequencies. However, it had been shown that the associated error in the calculated "corrected" value can be excessively large for different frequency pairs.[160,171] Nonetheless, a guideline for selecting measurement frequencies and an optimal device size, suitable for in-line quality control for manufacturing, was reported shortly afterwards.[172] In this case, the model (Fig. 3.2.7) neglects the effects of series resistance, owing to the deposition of Al back contact as

previously discussed. The model, however, includes the presence of a lossy interfacial layer capacitor, which is modelled by capacitance (C_i) connected in parallel with conductance (G_i). The leakage component, in the high-k dielectric layer itself, is also denoted with a conductance (G_{ox}) element. The corrected values (C_c and G_c) include the effects of both gate leakage current and all the internal resistance within the depletion layer.

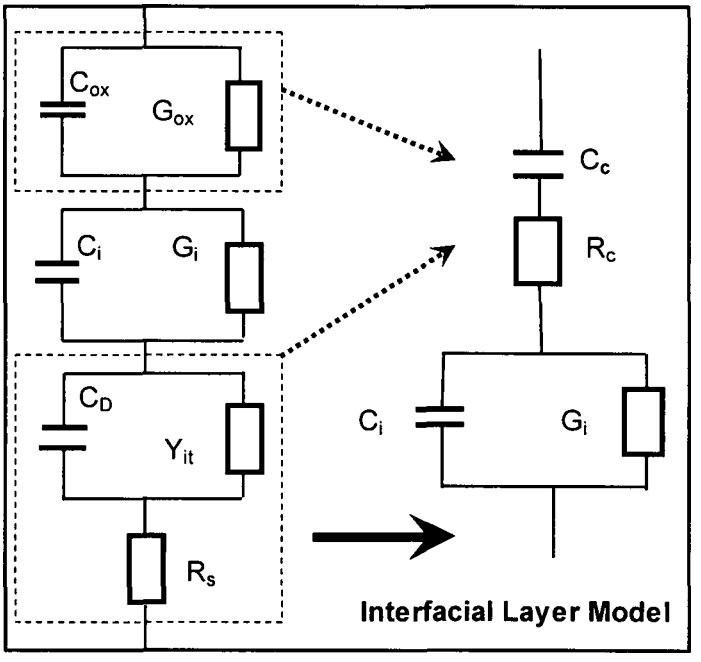

Figure 3.2.7. Equivalent circuit model for high-k stacks, taking into account the presence of a lossy interfacial layer with the additional Ci and Gi parallel circuit components.

In order to reconstruct the capacitance values from the loss, the impedance of the four-element circuit model (Fig. 3.2.8) is compared with the measured impedance of the tested device accordingly. The impedance of the four-element circuit model is given by:

$$Z_c = Z_m - Z_i \tag{3.1.40}$$

where Z_c, Z_m and Z_i are expressed as:

$$Z_c = R_c + \frac{1}{j\omega C_c},\quad Z_m = \left(G_m + j\omega C_m\right)^{-1} \text{ and } Z_i = \frac{\Delta - j\omega}{C_i\left(\Delta^2 + \omega^2\right)} \qquad (3.1.41)$$

where $\Delta = G_i/C_i$ and ω is the angular frequency ($Rad \cdot s^{-1}$). By equating the real (R_{mj}) and imaginary (I_{mj}) parts in Eq 3.1.40 at two different frequencies, and after algebraic manipulation, the corrected capacitance (C_c) is obtained as:

$$C_c = \frac{\Delta^2\left(\omega_1^2 - \omega_2^2\right)}{\left[I_{m2}\omega_2\omega_1^2\left(\Delta^2 + \omega_2^2\right) - I_{m1}\omega_1\omega_2^2\left(\Delta^2 + \omega_1^2\right)\right]} \qquad (3.1.42)$$

where

$$\Delta = \frac{\omega_1 I_{m1} - \omega_2 I_{m2}}{R_{m1} - R_{m2}},\quad I_{mj} = \frac{\omega_j C_{mj}}{\left(G_{mj}^2 + \omega_j^2 C_{mj}^2\right)},\quad R_{mj} = \frac{G_{mj}}{\left(G_{mj}^2 + \omega_j^2 C_{mj}^2\right)} \text{ and } j = 1,2. \qquad (3.1.43)$$

Proceeding in a similar manner with the real parts of the impedance, one obtains the relations for the lossy interfacial layer capacitance (C_i) and its conductance (G_i) as:

$$C_i = \frac{\Delta\left(\omega_2^2 - \omega_1^2\right)}{\left(\Delta^2 + \omega_1^2\right)\left(\Delta^2 + \omega_2^2\right)} \times \frac{1}{\left(R_{m1} - R_{m2}\right)} \quad \text{and} \quad G_i = \Delta C_i . \qquad (3.1.44)$$

Figure 3.2.9 shows the corrected C-V curves, extracted using Eqs (3.1.42 and 3.1.43). All of the extracted C-V curves closely align with one another over the three widely different frequencies pairs, demonstrating the success in retrieving the true capacitance values. Therefore by taking into account the presence of a lossy interfacial layer, the effect of frequency dispersion in high-k stacks can be eliminated.

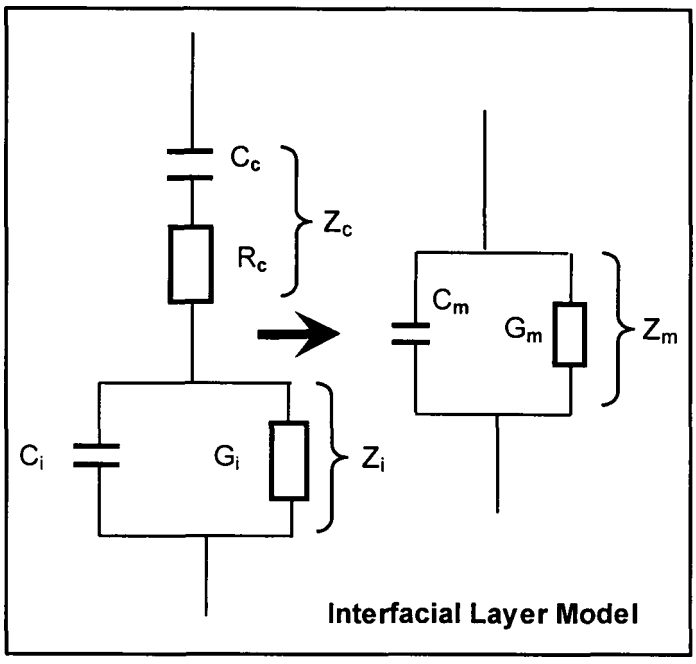

Figure 3.2.8. A direct comparison between the impedance of the four-element model with the measured impedance of the actual device that includes the effect of unwanted lossy interfacial layer.

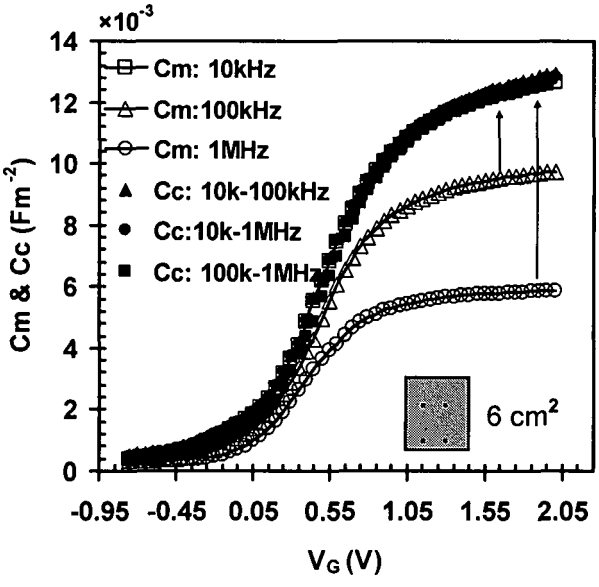

Figure 3.2.9. The extracted C_c-V_G curves based on data from Fig. 3.2.6 and the four-element equivalent circuit model in Fig. 3.2.8. Dispersion was no longer observed after the lossy dielectric layer was taken in consideration.

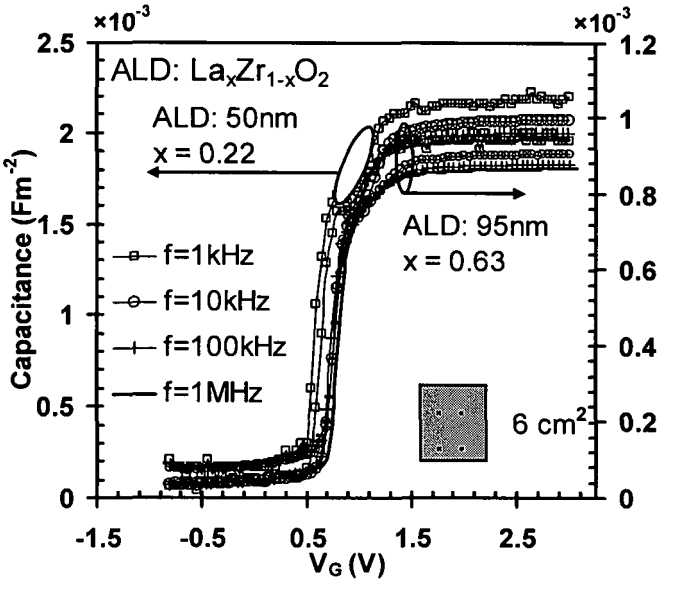

Figure 3.2.10. High frequency C-V curves for [Au/ $La_xZr_{1-x}O_2$ /SiO_2/n-Si/Al] capacitors with two different compositions of Lanthanum. $La_xZr_{1-x}O_2$ was deposited by ALD on Si (100) substrates at 300°C using 0.05M toluene solutions of Zr[$(MeCp)_2Me(OMe)$] and [$(Pr^iCp)_3La$] in H_2O. The La content in the films was varied by changing the injection rates of the individual precursors. The sample was post metallization annealed with forming gas (FGA) at 400°C for 30 minutes. Frequency dispersion in C-V measurements observed in $La_xZr_{1-x}O_2$ samples after back Al deposition. The substrate area was $6cm^2$.

Finally, by taking into an account both the effects of series resistance and lossy interfacial layer, the frequency dependence of ε_k value can now be assessed. Figures 3.2.10 and 3.2.11 show typical frequency dispersion in $La_xZr_{1-x}O_2/SiO_2$ stacks before and after the correction, of the lossy interfacial layer model, was applied. It was observed that the frequency dispersion still remained and the effect could now be associated with the frequency dependence of its permittivity value. It may be attributed to the dielectric relaxation nature in different high-k stacks such as lanthanum zirconium oxide ($La_xZr_{1-x}O_2$) thin films. Recent work[173] also shows that the relative dielectric permittivity values tend to exhibit significant variation and spread widely over different frequency regimes (e.g.., 1kHz

to 1MHz). This is particularly evident with non-thermally treated samples, which tend to provide higher relative permittivity values (i.e., the ε_k value of non-thermally treated TiO_2 varies in the range of 40-160), but appear to be highly unstable.

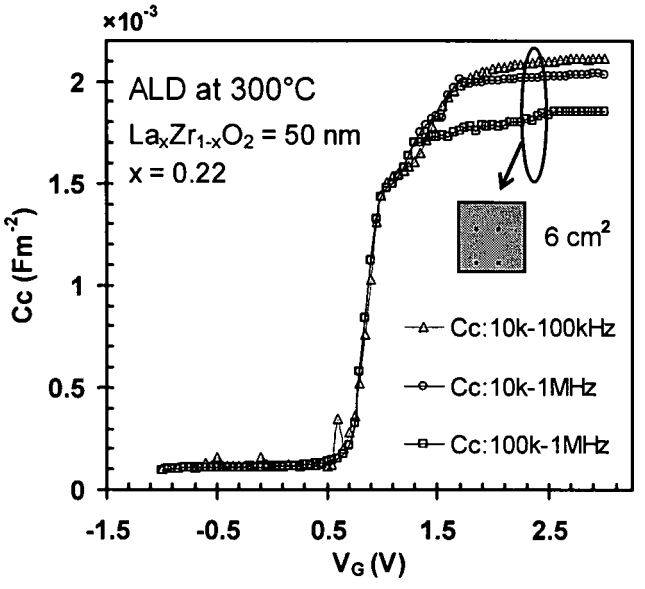

Figure 3.2.11. The extracted C_c-V_G curves based on data from Fig. 3.2.10 and the four-element equivalent circuit model in Fig. 3.2.8. The $La_xZr_{1-x}O_2$ film physical thickness was 50nm with 2nm SiO_x interfacial layer (t_i). Dispersion was still observed after the lossy dielectric layer was taken in consideration.

The dielectric relaxation effect refers to a momentary relaxation response of a dielectric medium to an external field that is caused by movement of dipoles and electric charge. This phenomenon can prevent the application of some dielectrics and deteriorates the performance of MOSFETs [for example, by shifting the threshold voltage (V_t)]. Time and amplitude dependence of the dielectric relaxation can be visualized as a series of parallel RC-shunt circuits. Picturing the positive charged gate of the n-channel MOSFET that couples with several RC-shunt circuits (e.g., the presence of the dielectric relaxation effect) for a long period of time,

all RC-shunts will be charged. When switching to zero, the RC-shunt circuits will still be charged for sometime before gradually returning to their off-state. This therefore has the same effect as a negative shift of threshold voltage due to positive trapped charges. However, unlike V_t shifts due to fixed charge, that due to dielectric relaxation charge is dependent on the amplitude of the applied voltage step.

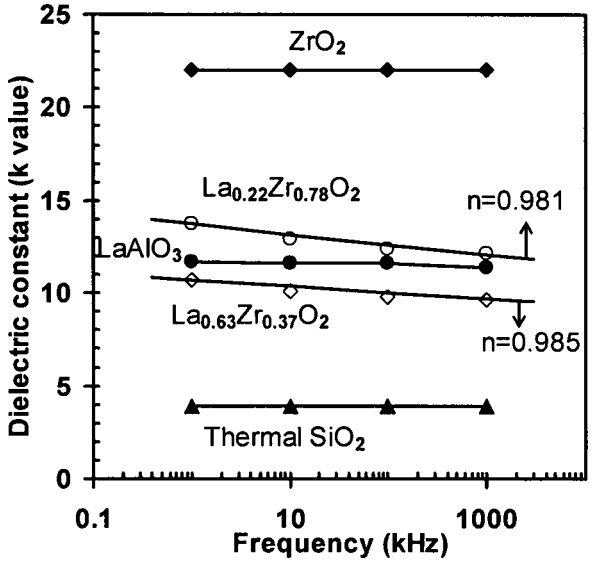

Figure 3.2.12. A summary of frequency dependence of κ-value. No frequency dependence of k value was observed for $LaAlO_3/SiO_2$ stacks and ZrO_2/SiO_2 stacks. The frequency dependence of k value, observed in $La_xZr_{1-x}O_2/SiO_2$ stacks, can be fitted by the Curie von Schweidler law and the exponent (n) changes from 0.981 to 0.985 when the composition of La changes from 0.22 to 0.6.

The frequency dependence of $La_xZr_{1-x}O_2$, ZrO_2, $LaAlO_3$ and thermal SiO_2 dielectrics are shown in Fig.3.2.12 for comparison. The permittivity value of $La_xZr_{1-x}O_2$ dielectric clearly shows a power-law dependence on frequency (f) known as the Curie von Schweidler law, $\varepsilon_k \propto f^{n-1}$, $(0 \leq n \leq 1)$, where the value of the exponent (n) indicates the degree of dielectric relaxation.[174,175] The n value is 0.981 and 0.985 when the composition of

La, x, is 0.22 and 0.6, respectively. Two possible causes for this observation were proposed as: (i) ion movement of unbounded La^+ or Zr^+ ions in the metal oxide resulting in dielectric relaxation;[173] (ii) the combination of unbound metal ions with electron traps, generating dipole moments and inducing dielectric relaxation.[176] A further study is needed to unveil the mechanism of dielectric relaxation of $La_xZr_{1-x}O_2$ oxides.

In summary, the steady state characteristics of the n-type MOS capacitor were derived and discussed, together with simulations using the derived formulae. In this chapter the origins of frequency dispersion, commonly observed in C-V measurements, in high-k dielectrics are explained and successfully modelled. C-V data showed frequency dependence which decreased significantly after reducing the back contact impedance, emphasizing the significance of back metal contact. This effect is frequently ignored in the literature. A reconstruction model has been implemented, for extracting the frequency independent capacitance of high-k dielectric materials from the lossy interfacial layer, using the adapted dual frequencies technique. This method can be integrated easily into a routine C-V measurement procedure. Finally, the effect of dielectric relaxation was suggested to be another reason for frequency dispersion in different high-k stacks. It was attributed to movements of unbound metal ions or combinations with defects that result in dielectric relaxation, hence the variation of accumulation capacitance leading to the frequency dependence of dielectric permittivity.

Chapter 4 – Hafnium oxides

4.1. CHOICES OF AVAILABLE PRECURSORS AND OXYGEN SOURCES

Due to the fast moving pace in the development of hafnium oxide deposition methods, it has became necessary to closely tailor the physical properties of the precursor in order to optimize the physical and electrical characteristics of the deposited hafnium oxide films. To achieve successful dielectric characteristics and to be suitable as a practical vapour deposition process, a careful selection of the precursor is of utmost importance. The precursor should be sufficiently volatile and vaporize rapidly at a reproducible rate. Also, it must not undergo a significant self-decomposition at the depositing temperature. The precursor must be chemically reactive towards both the surface sites and its oxygen source. Furthermore, the precursor and its reaction by-products should not be corrosive leading to film non-uniformities due to etching and corrosion of the tool. Selecting precursors with all of the desired properties remains a challenging task, as relatively little data is available and detailed the chemistry has not been well understood.

In this chapter, some recent developments in the molecular design of precursors used for the chemical vapour deposition process of HfO_2 are described, highlighting the very different requirements for MOCVD and ALD precursors. The influence of molecular structure on the physical properties of a precursor and on the growth dynamics is also discussed. Finally, the dielectric properties of HfO_2 film grown by liquid injection MOCVD and ALD, in the same reactor, using a new organometallic precursor [$(MeCp)_2HfMe(OPr^i)$] are reported.

Hafnium dioxide (HfO_2) has been extensively investigated as a replacement for SiO_2 as the gate dielectric oxide in sub-65 nm complementary-metal-oxide-semiconductor (CMOS) technology.[10,177-179] A wide variety of precursors have been used for both the MOCVD and ALD of HfO_2, many of which have discontinued due to a number of problems associated with them. For instance the metal halides, which consist of a metal atom directly bonded to halogen atoms (e.g., $HfCl_4$ and HfI_4), are usually low volatility solids that need substrate temperatures of at least 800°C for oxide deposition.[180] This drawback makes the metal halides unsuitable for many IC applications where a low thermal budget is required. However, despite a risk of chloride contamination in the films and an aggressive side product [hydrochloric acid (HCl)], the metal chloride (e.g.,$HfCl_4$) has attracted a considerable amount of attention in ALD systems where the importance of carbon-free deposition was emphasized.[181-185] Transition metal bromides and iodides do not offer significant advantages over the chloride.[182]

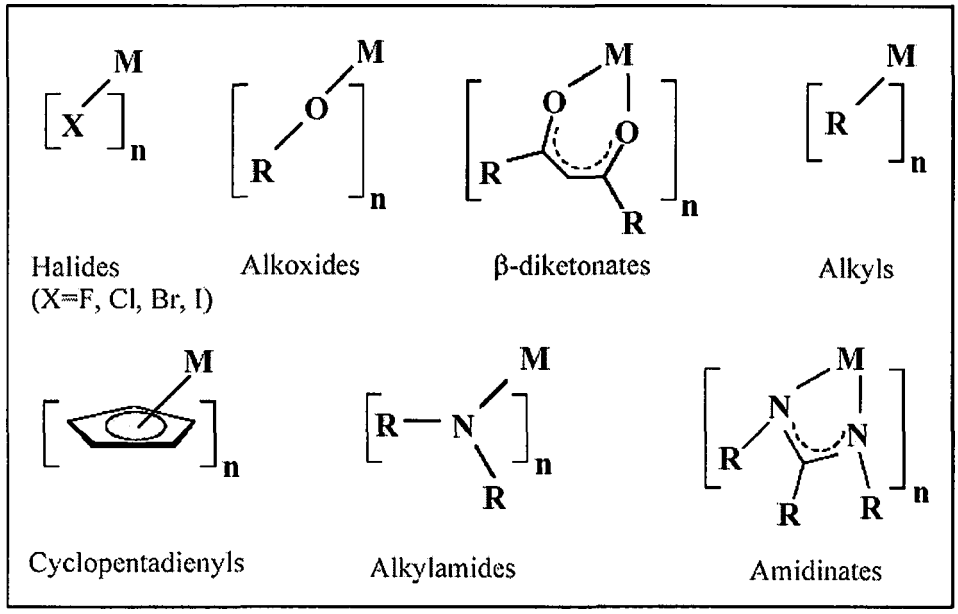

Figure 4.1.1. Precursor types. The R's represent alkyl groups consisting of carbon and hydrogen, such as methyl (CH_3). Metal and oxygen atoms are represented by (M) and (O) respectively.

Precursors with nitrogen bonded to the metal include metal alkylamides ($M(NR_2)_n$) and metal amidinates ($M(N_2CR_3)_n$). These metal nitrate complexes have considerable potential as both MOCVD and ALD precursors for the deposition of both metal nitrate and metal oxide thin films. They are generally more reactive towards hydroxylated surfaces, due to weaker metal-nitrogen bonding. This facilitates nitrogen incorporation into the oxide films, which helps to inhibit further oxidation of silicon, thereby suppressing the equivalent oxide thickness (EOT) to a minimum. Also, metal amides produce less corrosive by-products compared with metal chlorides and have a superior volatility than other reported solid precursors (e.g., $HfCl_4$).[186] Previous work has shown that high quality hafnium oxide thin films, deposited by ALD with self-limiting characteristics, can be obtained by using $[Hf(NO_3)_4]$ and $Hf(NMeEt)_4$ precursors.[186-190] However, their limited thermal stability restricts the ALD growth window to relatively low substrate temperatures (150-275°C), which can lead to the incorporation of impurities in the HfO_2 films.[186,188] Furthermore, there are safety concerns about the widespread use of anhydrous nitrate complexes that may obstruct its application in the chemical vapour deposition process.

Precursors with oxygen attached to the metal, are categorized as alkoxides or β-diketonates as shown in Fig. 4.1.1. In β-diketonate complexes, the metal centre is usually surrounded by two oxygen atoms per ligand, making them generally more stable towards hydrolysis. They are therefore common precursors for CVD and have been investigated for ALD of hafnium oxides such as $[Hf(thd)_4]$ (thd = 2,2,6,6,-tetramethyl-3,5-heptanedionate),[191] $[Hf(tod)_4]$ (tod = 2,7,7-trimethyl-3,5-octanedionate)[192] and $[Hf(tfac)_4]$ (tfac = 1,1,1,-trifluoropentane-2,4-dionate).[193] However, there are some major drawbacks that impede the applicability of those precursors such as high evaporation temperatures (~200°C) required for a sufficient vaporization of the precursor, high

growth temperatures (>600°C) for the oxide deposition and a substantial amount of carbon or fluorine contamination in the deposited films.[193] In addition, a strong oxidizer, such as ozone (O_3), is required as the source of oxygen in order to break the strong carbon to oxygen bonds. These features, as well as the use of ozone that causes extensive oxidation of silicon, make them unsuitable for gate dielectric applications.[194]

Much attention has also been given to metal alkoxides (e.g., $[Hf(OR)_4]$) in MOCVD as the precursors permit lower deposition temperatures, and under optimized growth conditions, allow the deposition of carbon free films.[195] However, the majority of these complexes tend to undergo polymerization, thereby reducing the precursor volatility. To inhibit polymerization in these metal alkoxides, the bulky groups namely *tert*-butoxide (O^tBu) were introduced and have been successfully used for the MOCVD of HfO_2.[196,197] Nevertheless, these precursors still contain unsaturated ligands that can easily undergo a catalytic "hydrolytic thermal decomposition",[198] making them highly air and moisture sensitive and vulnerable to pre-reaction in the MOCVD reactor. Consequently, this greatly reduces their shelf-life, especially in solution-based liquid injection MOCVD or ALD applications.[177] Another strategy used to limit oligomerization in hafnium alkoxides, and reducing their moisture sensitivity at the same time, was achieved by incorporating the sterically-hindered ligand 1-methoxy-2methyl-2-propanolate (mmp) that formed stable bidentate chelate rings with the metal centre (Fig. 4.1.2). A series of mmp-based complexes, including $[Hf(O^tBu)_2(mmp)_2]$ and $[Hf(mmp)_4]$, have been used successfully in MOCVD for the deposition of HfO_2 films with excellent materials and electrical properties.[85,106,199] Those latter precursors, however, were later found to be incompatible with ALD process. The film growth was not entirely self-limiting, with the oxide growth rate increased with the increasing precursor pulse length, due to the decomposition of the precursor.[111] It was however

possible to control the dependency on pulse length by lowering the growth temperature to be below 300°C, but this greatly reduced the precursor reactivity as evidenced by the very low growth rate (~0.02 nm $cycle^{-1}$). This was attributed to the steric shielding of the surface exchange reaction between (OH) species and $[Hf(mmp)_x]$ precursor moieties.[111,177] Alternatively, a more recent study has reported a use of another hafnium alkoxide complexes, containing the amino-functionalized ligand 2-4,4-dimethyloxazolinyl-propanolate (dmop), which were also very suitable for solution-based liquid injection MOCVD.[83] Reasonable electrical properties were obtained from the deposited hafnium films using $[Hf(O^tBu)_2(dmop)_2]$ precursor with low hysteresis and a slight shift in the flatband voltage, indicative of more trapped charges at the HfO_2/Si interface. The extracted permittivity value was found to be 18.6. The reduction from the expected value, ($\varepsilon_k \sim 25$),[10] was attributed to the presence of a low permittivity mixed interfacial layer of hafnium oxide and native SiO_2 and the series resistance effect.[83]

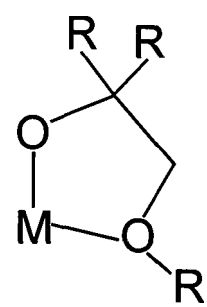

Figure 4.1.2. Chelate ring formed by an (mmp) ligand coordinated to a metal atom. The methyl groups (CH_3) are represented by (R), while metal and oxygen atoms are represented by (M) and (O) respectively.

Organometallic precursors have metal atoms bound directly to alkyl groups $[M(C_xH_y)_n]$. They are volatile, highly reactive and possess a significantly higher thermal stability than other hafnium-alkoxides and alkylamides precursors. Despite those advantages, metal

cyclopentadienyl precursors, such as [Cp_2HfMe_2] (Cp = cyclopentadienyl, C_5H_5), have not been extensively explored for gate dielectric applications. Recent work[200] shows encouraging results on the dielectric properties, using a potential [Cp_2HfMe_2] precursor, by ALD. The self-limiting mechanism, at an optimum growth temperature of 350°C, was obtained together with high purity HfO_2 films (0.2 atom% of carbon contamination).[104,200] Dielectric behaviour of the as-deposited films, where the HfO_2 film thickness and the native SiO_2 interfacial layer were 4.9nm and 1.8nm respectively, showed low hysteresis and a diminutive shift of flatband voltage, indicating a small amount of fixed oxide charge as well as relatively low interface state density. The extracted dielectric permittivity from C-V measurement was found to be ~13 and the leakage current density at 2MVcm^{-1} was below ~10^{-5} Acm^{-2} in all films.

Metal precursor	Oxygen source	T_{growth} (°C)	Impurities (atom %)	ε_k	Ref.
$HfCl_4$	H_2O	300	- and 1.0 (0.4 % Cl)	12-20	182,183,185, 194
HfI_4	H_2O / H_2O_2	300	- and 1.0 (0.4 % I)	14	182,201
$Hf(NMeEt)_4$	H_2O	250	0.3 and 2.0	11-14	186,188
$Hf(ONEt_2)_4$	H_2O	300	6.0 and 11.0	10	202
$Hf(O^tBu)_4$	O_2/O_3	250-480	-	23	203,204
$Hf(mmp)_4$	H_2O/O_2	360	2.6 and 2.2	13-26	85,111
$Hf(O^tBu)_2$ -$(mmp)_2$	H_2O	360	11.0 and 2.7	12-19	205
$Hf(O^tBu)_2$ -$(dmop)_2$	O_2	450	5.2 and -	19	83
$Cp_2Hf(CH_3)_2$	H_2O	350	0.4 and 0.2	12-14	200

Table 4.1.1. Published processes for the MOCVD and ALD of HfO_2 thin films on silicon. T_{growth} and ε_k represents the preferred or most frequently used growth temperature and the dielectric permittivity of the material respectively. Impurities refer to carbon (C) and hydrogen (H) contamination respectively.

Table 4.1.1 summarizes the reported MOCVD and ALD process of HfO_2 thin films, deposited from various combinations of precursors. In general, lower growth temperatures ($\leq 300°C$) are required to increase the growth rate while decreasing the degree of polycrystallization. Meanwhile, high growth temperatures can also be used when films free of residual halide contaminations need to be obtained.[200] The organometallic cyclopentadienyl compounds series can be considered as promising alternative precursors for producing high quality HfO_2 films to replace their predecessors (halides, alkoxides and alkylamides). Those promising results have motivated further studies on the cyclopentadienyl series, in both the liquid injection MOCVD and ALD. In this chapter, dielectric properties of HfO_2 films using the new organometallic cyclopentadienyl [$(MeCp)_2HfMe(OPr^i)$] precursor are reported.

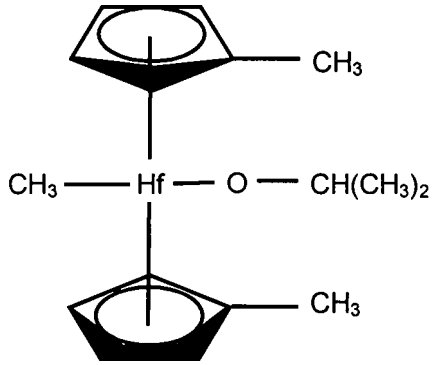

Figure 4.1.3. A schematic diagram of the organometallic cyclopentadienyl [$(MeCp)_2HfMe(OPr^i)$] precursor. The methyl groups (Me), denoted with CH_3, are attached directly to both metal hafnium (Hf) and the pentagonal cyclopentadienyl ligands (Cp). Oxygen and isopropyl group (Pr^i) are denoted with O and $CH(CH_3)_2$ respectively.

4.2. GROWTH AND CHARACTERIZATION OF HAFNIUM OXIDE THIN FILMS FABRICATED USING THE [(MECP)$_2$HFME(OPR^i)] PRECURSOR

Liquid injection MOCVD and ALD experiments were carried out on an Aixtron AIX 200FE AVD reactor fitted with the "Trijet"^{TM} liquid injector system.[102] Thin films of hafnium oxide were deposited by MOCVD in the temperature range 400-650°C and by ALD in the temperature range 300-450°C using a [(MeCp)$_2$HfMe(OPr^i)] precursor, with thicknesses varying from 9.6nm to 102nm. During the MOCVD experiments, oxygen was introduced at the inlet of the reactor as the oxygen source. For the ALD experiments, the oxidant was replaced by water vapour, which was controlled by a pneumatic valve. The substrate was rotated throughout all experiments. Films of HfO_2 were deposited on Si (100) substrates using a 0.05M solution of [(MeCp)$_2$HfMe(O^{i}Pr)] in toluene. Full MOCVD and ALD growth conditions can be found in Tables 4.2.1.

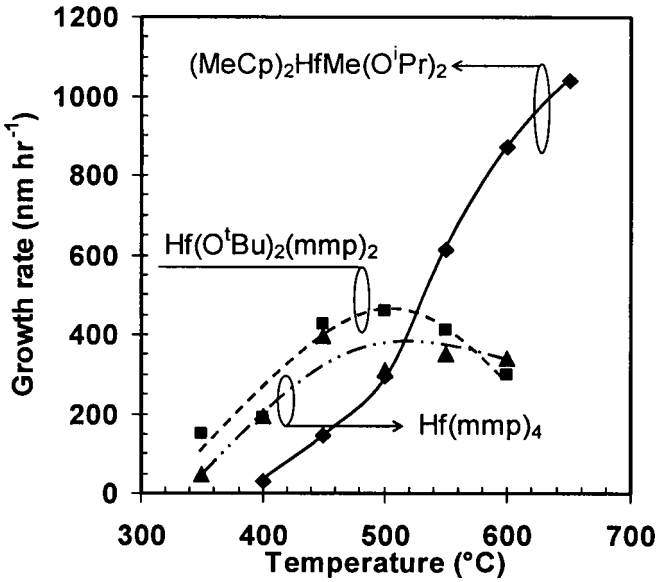

Figure 4.2.1. Variation of growth rate with substrate temperature for HfO_2 films grown by liquid injection MOCVD using [(MeCp)$_2$HfMe(OPr^i)] precursor. Growth data from[Hf(O^{t}Bu)$_2$(mmp)$_2$] and [Hf(mmp)$_4$], after Williams et al.,[199] were also presented for a comparison.

Figure 4.2.1 shows the effect of growth temperature on growth rate of HfO_2 by liquid injection MOCVD using $[(MeCp)_2HfMe(O^iPr)]$ precursor. For a direct comparison, growth data from both $[Hf(O^tBu)_2(mmp)_2]$ and $[Hf(mmp)_4]$ were also presented.[199] The growth rate of HfO_2 by $[(MeCp)_2HfMe(O^iPr)]$ precursor commenced at a higher substrate temperature (400°C) than other alkoxides, with the highest growth rates occurring at 650°C. This corresponds to the region of kinetic control where film growth is dominated by thermal decomposition of the precursor on the substrate. Further plotting of the curves was not possible due to the temperature limitations of the reactor. With hafnium alkoxide precursors such as $[Hf(O^tBu)_2(mmp)_2]$ and $[Hf(mmp)_4]$, thermal depletion of the precursor in the gas phase begins at approximately 500°C.[199] This strongly suggest that the $[(MeCp)_2HfMe(O^iPr)]$ precursor has a significantly higher thermal stability than those alkoxide predecessors and is likely to give a larger range of low-temperature MOCVD applications.

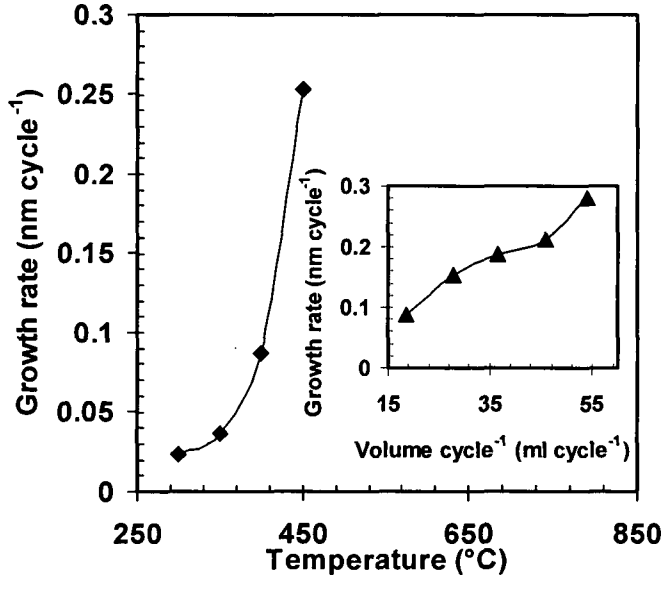

Figure 4.2.2. Variation of growth rate with substrate temperature for HfO_2 films grown by liquid injection ALD using $[(MeCp)_2HfMe(OPr^i)]$ precursor. The inset shows a variation of growth rate, at 400°C growth temperature, with precursor solution pulse length.

	MOCVD	ALD
Substrate temperature	400-650°C (Si 100)	300-450°C
Evaporator temperature	200°C	200°C
Pressure	5 mbar	5 mbar
Injection rate	30 $cm^3 h^{-1}$	2.5µl / pulse
Solvent	Toluene	Toluene
Concentration	0.05 M	0.05 M
Argon flow	200 $cm^3 min^{-1}$	200 $cm^3 min^{-1}$
Oxygen flow	100 $cm^3 min^{-1}$	—
Run time	10 min	—
Pulse sequence (Precursor/purge/water/purge)	—	2/2/0.5/3.5
Number of cycles	—	300

Table 4.2.1. Growth conditions used for the deposition of HfO_2 by liquid injection MOCVD and ALD using $[(MeCp)_2HfMe(OPr^i)]$.

Figure 4.2.2 shows the effect of growth temperature on growth rate of HfO_2 by ALD. No significant growth was observed below 300°C due to the high thermal and chemical stability of the precursors. The growth rate increased steadily up to 400°C and then increased dramatically at 450°C with the onset of thermal decomposition. No growth occurred in the absence of water at or below 400°C. The inset of Fig. 4.2.2 shows the variation of oxide growth rate with precursor volume injected per ALD cycle. For self-limiting growth in ALD, the oxide growth per cycle would be expected to increase with increasing injected precursor volume until surface-saturation is achieved,[200] at which point the growth rate should become constant. This should occur at 0.2-0.25 nm/cycle for hafnium oxide corresponding to the deposition of a single atomic layer per cycle. With $[(MeCp)_2HfMe(O^iPr)]$, the growth rate tends towards monolayer growth at 0.21nm/cycle (50µl/cycle), but continues to increase as the

volume per cycle is increased. As the growth per cycle exceeds that of a hafnium oxide monolayer, the precursor is not self-limiting. The lack of self-limiting growth may be due to the presence of residual adsorbed water inside the modified MOCVD reactor that had not been fully removed during the purge step.

Temperature	Technique	Sample	Hf	C	O	Hf/O
500	MOCVD	844	30.6	2.3	67.1	0.46
550	MOCVD	847	32.8	2.1	65.1	0.50
300	ALD	864	32.9	0	67.1	0.49
400	ALD	852	34	0	66	0.52

Table 4.2.2. Auger electron spectroscopy data showing the composition (at%) of HfO_2 films deposited by liquid injection MOCVD and ALD using $[(MeCp)_2HfMe(O^iPr)]$.

The atomic compositions of the HfO_2 films were determined by Auger Electron spectroscopy (AES) and the data are shown in Tables 4.2.2. The level of carbon impurity in MOCVD ranges from 2.1-2.3 at.%. The relatively low values observed indicate a clean decomposition of the precursor with little breakdown of the ligand carbon skeleton. These results are in marked contrast to those obtained with $[(MeCp)_2ZrMe_2]$, in which carbon levels as high as 30 at.% were detected by XPS in ZrO_2 films deposited in the presence of O_2 at 400-550°C.[188] The high carbon contamination was attributed to the presence of the Me group on the Cp ring which leads to the formation of $[Cp\text{-}CH_2\text{-}Zr\text{-}CH_2\text{-}Cp]$ intermediate species. These subsequently liberate H_2 and Cp to form stable [Zr-C] moieties resulting in heavy carbon contamination.[188] The relatively low levels of carbon in the HfO_2 films grown using $[(MeCp)_2HfMe(O^iPr)]$ indicate a different pyrolysis mechanism is taking place in which the (MeCp) ligand is eliminated without significant decomposition. On average, the films grown from $[(MeCp)_2HfMe(O^iPr)]$ are closely match

with the correct Hf:O stoichiometry. In ALD process, despite non-self limiting nature of the precursor, no carbon impurities were detected indicating that negligible thermal decomposition occurred at 400°C.

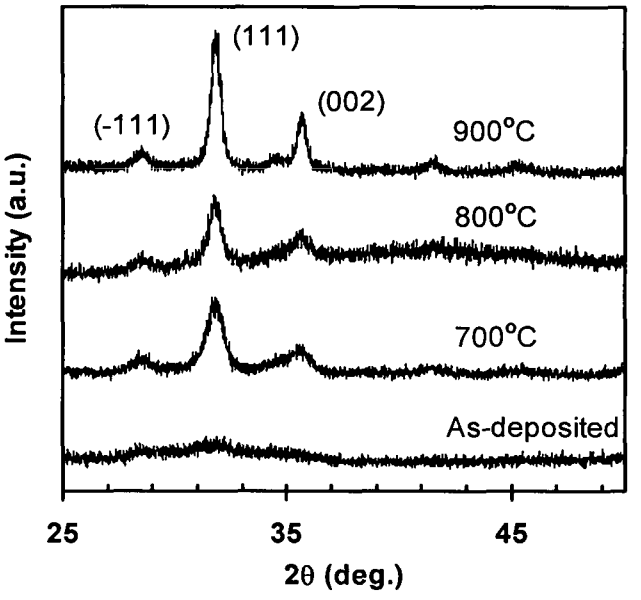

Figure 4.2.3. X-ray diffraction of a 102nm HfO_2 film deposited at 550°C by liquid injection MOCVD. The film was essentially amorphous, but developed a polycrystalline monoclinic structure after annealing above 700°C for 15 minutes in dry air.

The phase transitions of the gate dielectric from amorphous to crystalline were investigated by x-ray diffraction (XRD) analysis, which was performed on the studied films using nickel-filtered Cu Kα radiation (λ=1.5405Å) with a 2θ increment of 0.2° per second. To investigate this, selective studies were carried out only on near stoichiometric samples, to that of HfO_2, achieved by MOCVD. Samples of HfO_2 films, grown by MOCVD at 550°C, were subsequently annealed in air for 15 minutes over the temperature range 700°C to 900°C. Figure 4.2.3 shows the XRD diffraction patterns before and after annealing. The as-deposited HfO_2 layers showed no diffraction features suggesting that the films were essentially amorphous. After annealing at 700°C to 900°C for 15 minutes in dry air, the diffraction patterns showed the development of characteristic

(111) and (002) reflections of the monoclinic phase at 2θ values of 31.83° and 35.66° respectively.

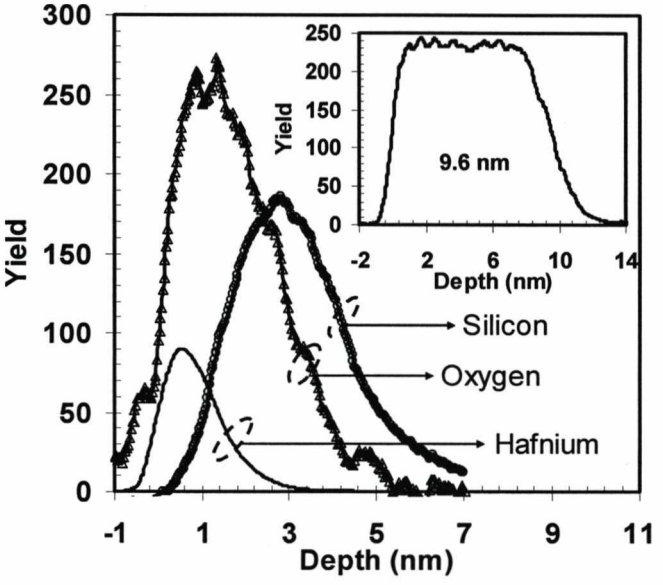

Figure 4.2.4. MEIS depth profile of the hafnium, silicon and oxygen distribution in an ALD deposited HfO_2 film, illustrating the small level of interfacial mixing between the oxide thin film and silicon substrate. The inset shows the extracted thickness from the depth profile of the deposited HfO_2 film.

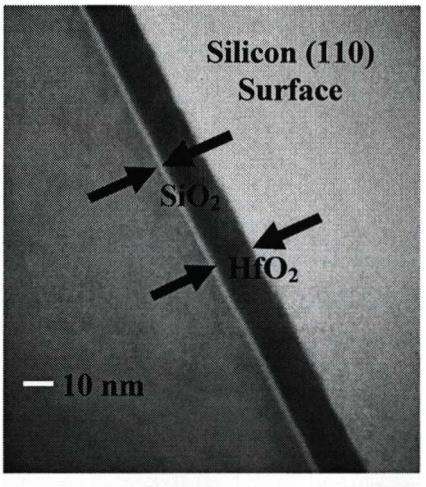

Figure 4.2.5. A cross sectional TEM image, of the as-deposited HfO_2 sample grown at 340°C by ALD, showing the HfO_2 thickness (13nm) and a thin (1.6nm) native oxide interlayer adjacent to the silicon substrate, respectively.

Film thicknesses and the presence of interfacial layer were determined by means of medium energy ion scattering (MEIS) experiments and cross sectional transmission electron microscopy (TEM) as described in chapter 2. MEIS experiments were carried out using a nominally 200 keV He^+ ion beam at 70.5° scattering angle. MEIS results show that the thickness of the near stoichiometric HfO_2 sample, deposited at 300°C by ALD, was 9.6nm. Figure 4.2.4 shows the combined Hf, Si and O depth profiles. The Si background has been subtracted from the O peak and the scattering yield from each element has been normalized to the Si yield, in order to indicate the relative abundance of the different elements. The results show the presence of a HfO_2 layer and a SiO_2 layer. When the system resolution and energy straggling are considered, it would tend to indicate that there is very little interfacial mixing. The presence of interfacial layer was also confirmed with TEM microscopy. The selected as-deposited HfO_2 samples, grown at 340°C by ALD, were prepared by hand-grinding to $\approx$ 65μm and final thinning by using a Gatan precision ion polishing system (PIPS). TEM observations were made using JEOL 2000FX operated at 500kV. TEM micrograph (Fig. 4.2.5) validates the presence of a thin native oxide interlayer, with the nominal thickness of 1.6nm.

To assess the electrical properties of the gate dielectric, metal-oxide-semiconductor capacitors ($Al/HfO_2/SiO_2/n\text{-}Si$) were fabricated with an area of 4.9×10^{-4} cm^2. High-frequency capacitance-voltage (C-V) measurements were conducted using a HP4192 impedance analyzer. Measurements were performed in parallel mode from a strong inversion towards a strong accumulation (and vice versa), with a sweep rate of 0.05 V/s at various frequencies (1kHz-1MHz). The measured capacitance was also corrected for the lossy interfacial layer effect following the methodology presented in chapter 3.

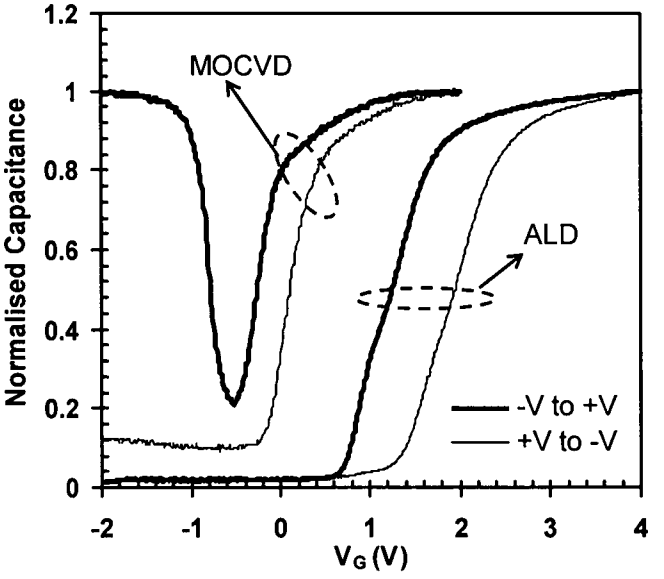

Figure 4.2.6. A comparison of the extracted high frequency capacitance-voltage (C_C-V_G) curves, based on the four-element equivalent circuit model in Fig. 3.2.8 using dual frequencies at 10kHz and 1MHz, for [Al/HfO_2/ SiO_2/n-Si/Al] capacitors by MOCVD and ALD. In MOCVD, HfO_2 was deposited on n-Si (100) substrates at 550°C using 0.05M solution of [$(MeCp)_2HfMe(O^iPr)$] in toluene and H_2O. In ALD, HfO_2 was deposited on n-Si (100) substrates at 300°C using 0.05M solution of [$(MeCp)_2HfMe(O^iPr)$] in toluene and H_2O. The pulse sequence used for ALD (2s precursor/2s purge/0.5s water/ 3.5s purge) was carried out for 300 cycles. All samples received post metallization annealed with forming gas (FGA) at 400°C for 30 minutes. The HfO_2 films thicknesses were 102nm (MOCVD) and 9.6 nm (ALD).

Figure 4.2.6 shows plots of the corrected C_C-V_G characteristics for the HfO_2 films, deposited by both MOCVD and ALD. Accumulation, depletion and inversion regions are clearly seen in both cases. The 'low frequency type behaviour' observed in high frequency C-V plots in MOCVD could be attributed to a very low carrier lifetime such that the true high frequency condition has not been met. Clockwise hysteresis was observed for both samples, irrespective of deposition processes, suggesting the existence of slow traps and electron traps at the HfO_2/ SiO_2 interface and/or in the bulk of the dielectric oxide film. A shift in the experimental flatband voltage, deviated from its ideal value (approximate to -0.15V for both cases) calculated using Eq. (3.1.32), was more prominent in ALD film as demonstrated in Table 4.2.3. The

permittivity values (ε_k) of the MOCVD and ALD films were ~21 and ~19 respectively.

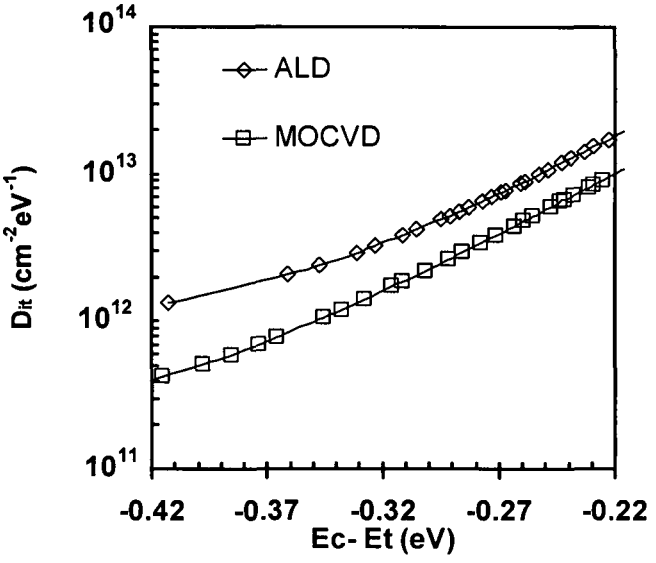

Figure 4.2.7. The extracted density of interface states (D_{it}), based on data from Fig. 4.2.6, with respect to the position of the Fermi level (Ec-Et) from conduction band edge for MOCVD and ALD films.

The D_{it} profiles of both MOCVD and ALD samples, from the conduction band, are shown in Fig. 4.2.7. The interface state densities were found to be an order of magnitude lower in the MOCVD film than the ALD film. The estimated interface state densities at flatband level are presented in Table 4.2.3 along with other electrical parameters.

Process	ε_k	V_{FB} (V)	V_{hys} (V)	D_{it} ($cm^{-2}eV^{-1}$)	J (Acm^{-2})
MOCVD	21.43	-0.12	0.41	6.94×10^{11}	8.4×10^{-5}
ALD	19.81	0.76	0.59	2.85×10^{12}	3.5×10^{-7}

Table 4.2.3. Electronic parameters, extracted from C-V and I-V measurements in Fig. 4.2.6, of the HfO_2 films deposited by liquid injection MOCVD and ALD. ε_k represents the permittivity value extracted from C-V in accumulation. The extracted flatband voltage, hysteresis voltage and interface state density are denoted with V_{FB}, V_{hys} and D_{it} respectively. The gate leakage current at $2MVcm^{-1}$ is indicated with J.

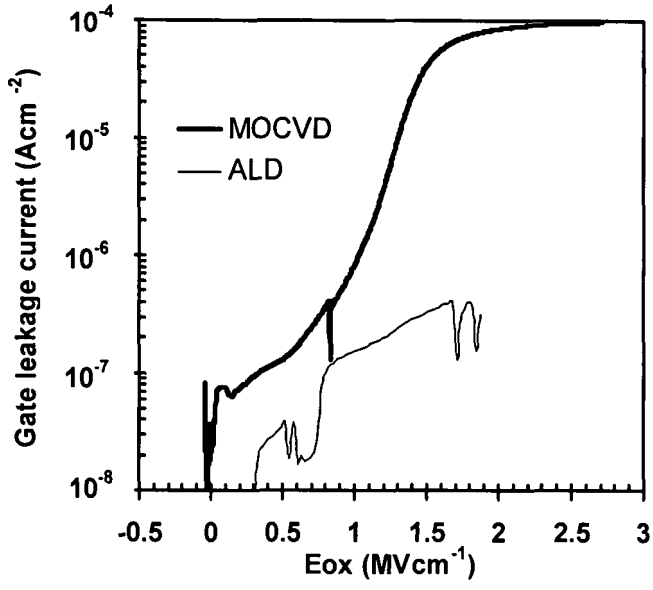

Figure 4.2.8. A comparison of the measured leakage current density vs. the applied electric field (Eox) in MOCVD and ALD films. The HfO_2 films thicknesses were 102nm (MOCVD) and 9.6 nm (ALD).

Figure 4.2.8 shows a plot of leakage current density (J) as a function of the electric field across the oxide (E_{ox}), which was taken using a Keithley K230 programmable voltage source and 617 type electrometer. It is evident that the leakage current in the ALD film, at 2 $MVcm^{-1}$, is two orders of magnitude lower than the MOCVD film and is comparable with other leading edge high-k dielectrics reported previously.[83,200 206-208]

The microstructural evolution and resulting changes in electrical properties of the HfO_2 films, as a function of annealing temperature in a nitrogen (N_2) ambient, have been widely studied.[120,178,183,209-211] It is well known that nitrogen-based post deposition annealing (PDA) plays a major role in removing trapped charges and strengthening immunity against oxygen diffusion. However, it was later discovered that there is also a trade off between PDA temperatures and the ratio of deep and shallow trapping centers.[120,212] The effect of crystallization on optical and electrical characteristics of the HfO_2, deposited by ALD using the organometallic cyclopentadienyl-link precursor, has not yet been reported

in detail. For this reason, further investigations were carried out on the low temperature crystallization effects on the grown HfO_2 films. Selective studies were performed on HfO_2 samples, deposited by ALD at 340°C. In order to investigate the phase transformation, samples were post-deposition annealed from 400°C to 600°C in N_2 ambient for 20 minutes prior to gate electrode deposition. Phase transition was determined using spectroscopic ellipsometry (SE) following the methodology presented elsewhere.[213] Aluminium was then deposited as metal electrode to form MOS capacitors for C-V and I-V assessment.

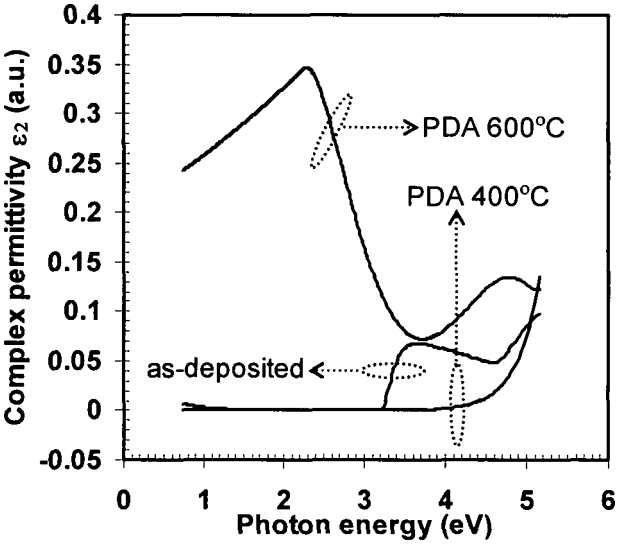

Figure 4.2.9. The dependency of the imaginary complex dielectric constant (ε_2) as a function of photon energy (E).

Figure 4.2.9 shows the dependence of the complex permittivity (ε_2) for the as-deposited and annealed samples. A near bandgap peak was recorded at 3.64 eV, for the as-deposited sample, which could be related either to a phase non-homogeneity and/or oxygen vacancy. The 400°C annealed sample showed a dramatic reduction of the near bandgap states. Increasing the anneal temperature up to 600°C brought important structural changes in the HfO_2 film, which were reflected by peaks at

2.30 and 4.76 eV. This concurs with previous observations on HfO_2 samples, deposited by DC magnetron sputtering, that are subjected to high temperature anneal.[214] The observed peaks were considered to be due to formation of defects and accompanied by an extension of the polycrystalline phase in the film, in particular with the range 4.5-5 eV which was attributed to oxygen vacancies.[215]

Figure 4.2.10 shows the normalized high frequency C-V characteristics at 1MHz, as a function of PDA temperatures, for the as-deposited and annealed samples. The C-V characteristics showed clear accumulation, depletion and inversion regions. Annealing at 500°C and above, however, instigated a stretch out of the curve and the upturns in capacitance in the inversion regime, although the capacitance did not return to its maximum value. The 'upturn' effect may be due to positive charge generation during N_2 anneal. The number of generated positive charges can be large enough to further support the inversion region initially, making the inversion capacitance (C_{inv}) much larger than the depletion capacitance (C_{dep}), so that the total capacitance can be expressed as a series combination of the oxide capacitance (C_{ox}) and the inversion capacitance. However, unlike a true low frequency characteristic, C_{inv} is comparable to C_{ox} in this situation and thus making the magnitude of the total capacitance in inversion regime lower than that of C_{ox}. Meanwhile, the 'stretch out' effect could be attributed to defect formations at the HfO_2/SiO_2 interface. This is because the additional change in charge density, due to the interface traps, will only be accommodated by changes in band bending. Consequently, to drive the MOS capacitor from accumulation to inversion requires a larger range of gate charge variation, for the case with interface traps, hence the stretch out along the gate bias axis of the C-V curve.[148] In the present case, the positive flatband shift of the as-deposited sample was moderate ($\Delta V_{FB} \sim 0.7V$), indicating negative fixed oxide charge in the dielectric. However, it was observed that

annealing in N_2 ambient also allowed the flatband voltage to shift negatively. This indicates that negative fixed oxide charges can be annealed out by the nitrogen anneal or they are compensated by nitrogen induced positive fixed oxide charges, generated during post deposition annealing. This is consistent with previous studies.[178,216,217] Significant hysteresis (0.5V-2V) of the C-V curves was observed in all samples, due to rechargeable traps inside the gate dielectric. The hysteresis effect became more severe with increasing anneal temperature as demonstrated in Table 4.2.4. This observation can also be related with crystallization in HfO_2 films mentioned previously.

The distribution of D_{it} from the conduction band, as a function of PDA temperatures, is shown in Fig. 4.2.11. The D_{it} of the annealed samples was higher than that of the as-deposited one. The increased of D_{it}, with increasing PDA temperatures, suggested that traps were formed at and/or near the interface between the HfO_2 and SiO_2 layer, evidently with the 'stretch out effect' of the obtained C-V curves. The estimated D_{it} at flatband level is presented in Table 4.2.4.

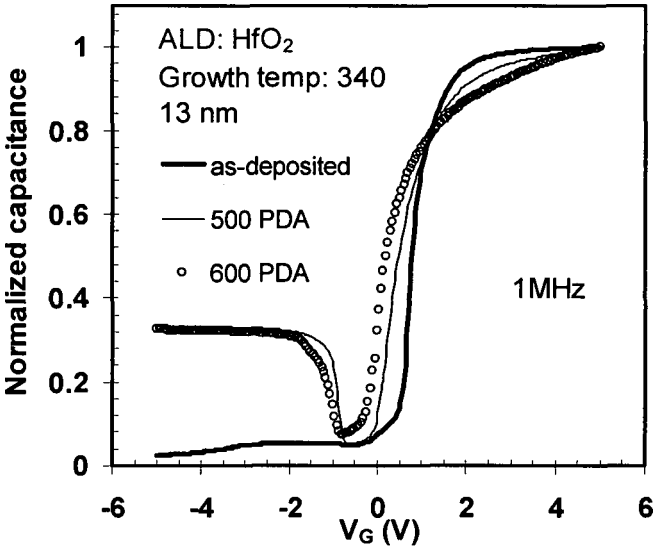

Figure 4.2.10. The effect of post deposition annealing, in N_2 ambient, on the C-V characteristics (positive sweep) of the HfO_2 stacks.

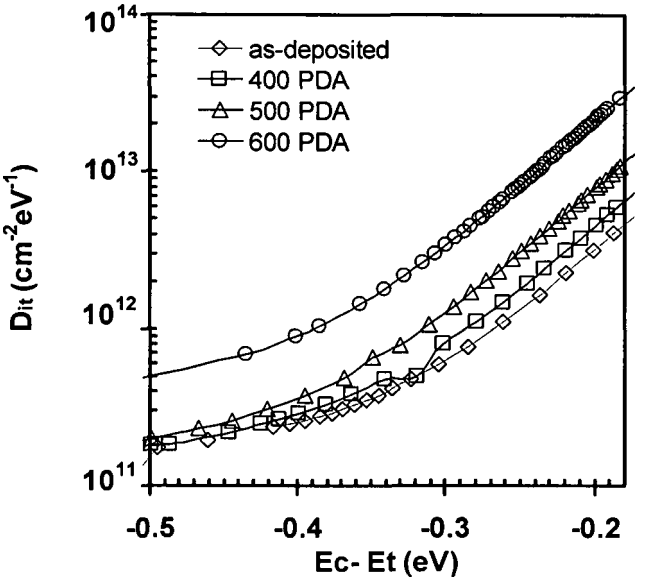

Figure 4.2.11. The extracted density of interface states (D_{it}), based on data from Fig. 4.2.10, with respect to the position of the Fermi level (Ec-Et) from conduction band edge as a function of PDA temperatures.

Room temperature leakage current behaviour was measured after post deposition annealing. Figure 4.2.12 depicts the gate leakage current versus the applied electric field across the oxide (E_{ox}) as a function of PDA temperatures. The electric field (E_{ox}) refers to the high-k layer as:[218]

$$E_{ox} = (V_G - \phi_{MS} - \phi_s)/[t_k(1 + \varepsilon_k t_{IL}/\varepsilon_{IL} t_k)] \qquad (4.2.1)$$

where V_G is the gate voltage, Φ_{MS} is the work function difference between metal electrode and substrate, Φ_s is the surface potential (calculated as $\Phi_{s(depletion)} \leq 2\Phi_B$, taking into account doping density N_d extracted from C-V plots), t_k and t_{IL} is the thickness of the high-k and interfacial layer respectively and ε_k, ε_{IL} is the permittivity of high-k and interfacial layer respectively. The leakage current density, at $2MVcm^{-1}$, was found to be below 3.91×10^{-6} Acm^{-2} in all films. At a higher electric field ($>3MVcm^{-1}$), however, higher leakage density was obtained in the 600°C PDA sample. Furthermore, the breakdown strength of the dielectric was reduced with increasing PDA temperatures, demonstrating

the effects of crystallinity on leakage current in the gate dielectric. The experimental I-V data obtained also showed strong temperature dependence as illustrated in Fig. 4.2.13. The measurements were performed using an automated hot chuck, at the temperature ranging from 17°C to 130°C.

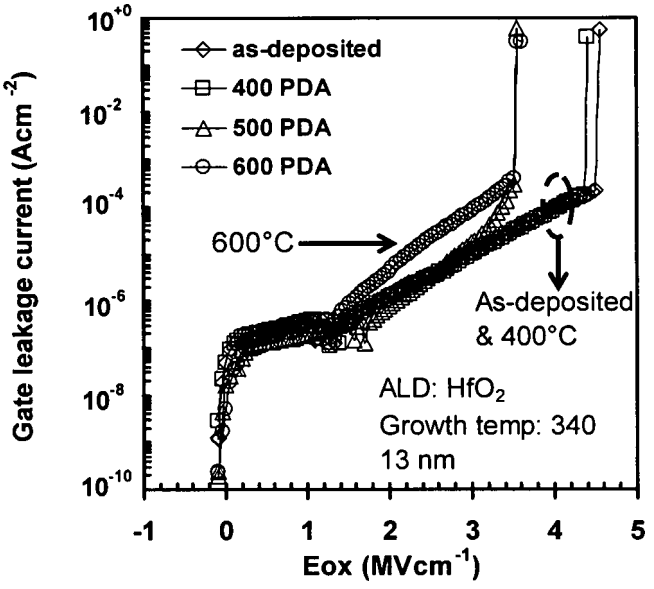

Figure 4.2.12. Gate leakage current vs. electric field (Eox) characteristics of the HfO_2/SiO_2 stacks, as a function of PDA temperatures.

The referring Poole-Frenkel plots, based on data from Fig. 4.2.12, are shown in Fig. 4.2.14. The dynamic permittivity values extracted from Fig. 4.2.14 ranges from 2.9 to 4.9 (Table 4.2.4). Taking into account the ε_i value for the as-deposited sample, the trap level (Φ_{PF}) can be evaluated from the slope of the Arrhenius plot (Fig. 4.2.15) and is found to be ~0.4 eV below the conduction band. This result is in agreement with the previous studies (Φ_{PF} ~ 0.5 to 0.8 eV below the conduction band).[135,218]

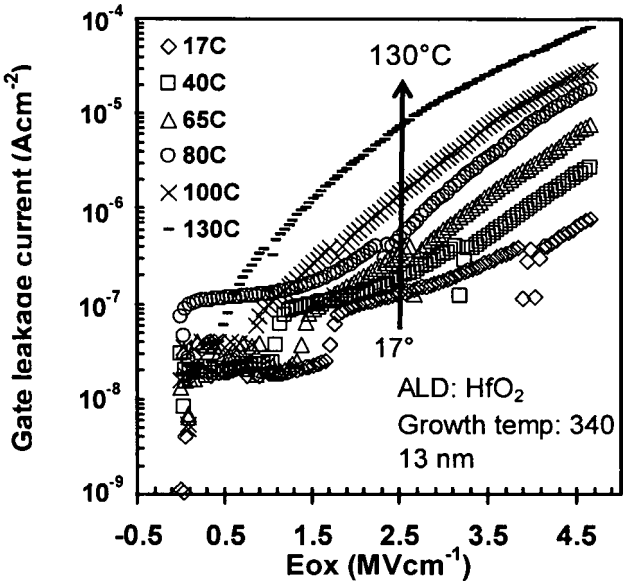

Figure 4.2.13. Gate leakage current vs. electric field (Eox) characteristics of the as-deposited HfO_2/SiO_2 stacks, measured at elevated temperatures (17°C-130°C), showing the temperature dependence.

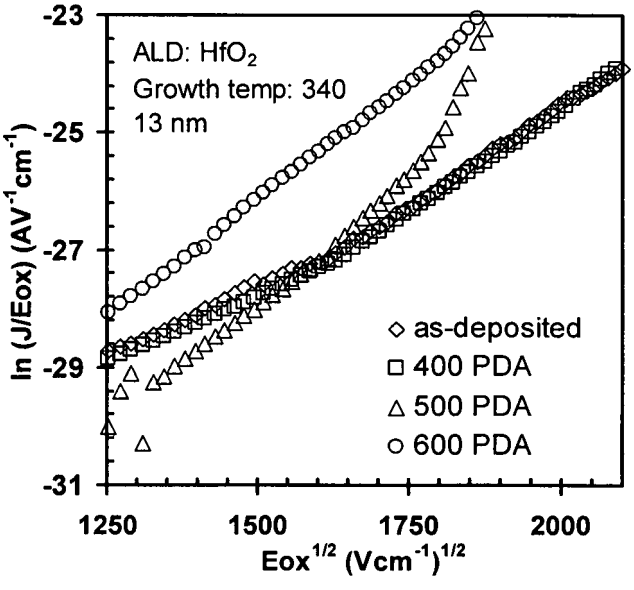

Figure 4.2.14. A plot of ln(J/E) vs. $E^{½}$, showing Poole-Frenkel conduction, data was extracted from Fig. 4.2.12.

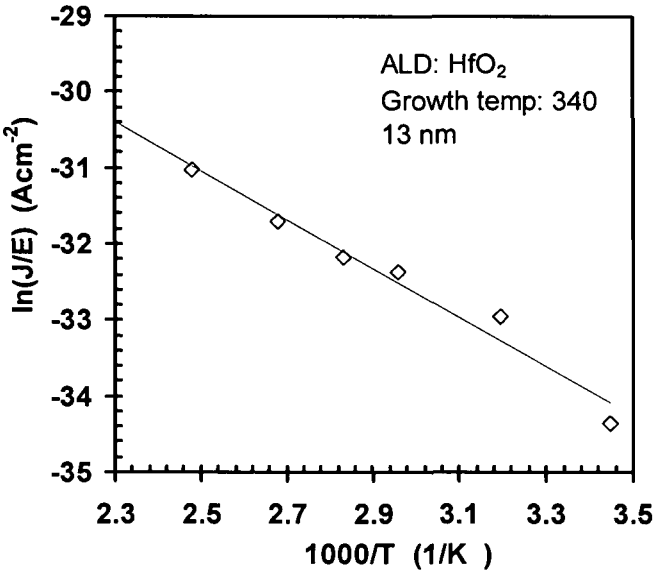

Figure 4.2.15. Arrhenius plot for the as-deposited Al/HfO_2/SiO_2/n-Si MOS capacitor at V_G of 3V.

Sample	V_{hys} (V)	V_{FB} (V)	D_{it} ($cm^{-2}eV^{-1}$)	ε_i	J (Acm^{-2})
as-deposited	0.40	0.58	7.69×10^{11}	4.93	1.37×10^{-6}
400°C	1.18	0.13	7.91×10^{11}	4.25	1.15×10^{-6}
500°C	3.22	0.12	7.90×10^{11}	2.93	7.55×10^{-7}
600°C	2.78	-0.12	1.78×10^{12}	3.62	3.91×10^{-6}

Table 4.2.4. Electronic parameters, extracted from C-V and I-V measurements in Figs. 4.2.10 and 4.2.12, of the HfO_2 films as a function of PDA temperatures. The extracted hysteresis voltage, flatband voltage, and interface state density are denoted with V_{FB}, V_{hys} and D_{it} respectively. ε_i is the dynamic permittivity of the high-k layer and the leakage current density at $2MVcm^{-1}$ is indicated with J.

In conclusion, the growth and characterization of HfO_2 thin films have been investigated using the new cyclopentadienyl [$(MeCp)_2HfMe(OPr^i)$] precursor. The precursor evaporates at moderate temperatures, making it very suitable for liquid injection MOCVD and ALD. X-ray diffraction analysis shows that the films are deposited with essentially amorphous microstructures. Auger electron spectroscopy indicated that thin films,

deposited by MOCVD, generally contained more carbon contaminations than the ALD ones. Nonetheless, the carbon residual was still at the very low level (2.1-2.3 at.-%) when compared with other precursors previously reported.

The dielectric characteristics of the as-deposited films have been evaluated from Al/HfO_2/SiO_2/n-Si capacitors with dielectric thicknesses ranging from 9.6nm to 102nm, showing the permittivity values (ε_k) ranging from 19-21 and the leakage current density as low as 3.91×10^{-6} Acm^{-2} at 2 $MVcm^{-1}$. The crystallization effects on electrical and optical properties of the deposited films were also reported. N_2-based PDA at above 500°C crystallized the film structures which resulted in increased leakage currents. Spectroscopic ellipsometry revealed large changes in the complex dielectric function (ε2) as PDA temperature was elevated, thereby suggesting the changes in the film crystallinity. It is suggested that the origin of the deep traps in HfO_2 were related to oxygen deficiencies in the film. I-V characteristics strongly suggest a P-F type mechanism of carrier transport through the films for the high-field region. The extracted dynamic permittivity values from the modified P-F concept give better agreement with the theory and literatures ($\varepsilon_i \sim n^2$ and the refractive index of $HfO_2 \sim 2$),[104,111,205] implying re-trapping at the nearest sites as the most likely mechanism.

Considering the properties of the deposited HfO_2 thin films, the new cyclopentadienyl [$(MeCp)_2HfMe(OPr^i)$] precursor is suitable for preparation by ALD. The feasibility of this novel precursor has been shown possible to achieve a high quality HfO_2 gate dielectric as a step towards future generation gate dielectrics.

Chapter 5 – Rare earth dielectrics Neodymium Aluminate thin films

5.1. CHOICES OF AVAILABLE RARE EARTH DIELECTRICS

Although ZrO_2, HfO_2 and their associated silicates and aluminates have been the most intensively investigated high-k materials,[10] there has been much recent interest in the lanthanide oxides.[47,53,219] The oxides M_2O_3 (M = La, Pr, Gd and Nd) are good insulators due to their large bandgaps (3.9 eV for Pr_2O_3, 5.6 eV for Gd_2O_3). They also have high dielectric constants (Nd_2O_3 ~ 12, La_2O_3 ~ 30 and Pr_2O_3 ~ 26-30), high symmetrical band offsets relative to Si (> 1eV for Pr_2O_3) and reasonable thermodynamic stability on silicon, making them attractive candidates for high-k CMOS and DRAM applications.

All of the earlier mentioned materials clearly have many advantages as high-k gate dielectrics, however, they also suffer from various drawbacks in their material properties which have hindered their application in microelectronics. For instance, La_2O_3 is chemically unstable, readily converting to $La_2(CO_3)_3$ during growth or upon storage or annealing,[220,221] and is easily converted to $La(OH)_3$ on reaction with ambient water due to its hygroscopic nature.[54,221] They also undergo an amorphous to polycrystalline transition at moderate temperatures (at 400-450°C for Gd_2O_3[222] and Nd_2O_3[223]). This can lead to a large increase in leakage current and the growth of a low-k SiO_2 interfacial layer during CMOS processing, which involves a high-temperature (>800°C) annealing step.

It is possible however to combine the desirable properties from two different oxides, while eliminating the undesirable properties of each individual material. A considerable amount of research has gone into the

development of innovative multi-functional advanced materials. Lanthanide aluminates-based ceramics, $MAlO_3$ (M = La, Pr, Gd and Nd), are promising materials for optical, magnetic, solid-state electronic and structural applications.[224-227] The aluminate doped with a lanthanide element offers a longer lifetime and is useful as a host for solid-state laser applications, luminescence systems and as window material for a variety of lamps.[228] In terms of a gate dielectric replacement, the effect of adding alumina (Al_2O_3), to such metal or rare earth oxides, is to produce an amorphous film that is thermodynamically stable on silicon with reduced leakage current. It is inevitable however that the overall permittivity of the perovskite aluminate will be lower than that of the pure metal oxides or rare earth oxides, but this trade-off can be worthwhile for the improved stability. Owing to such wide applications of perovskite aluminate-based ceramics, new routes for the synthesis of various aluminates are therefore highly desirable.

Lanthanum aluminate ($LaAlO_3$) has a wide range of potential material applications, apart from a gate dielectric replacement. The structural compatibility of $LaAlO_3$ with other multi-component oxides makes it a potential substrate or buffer layer for a variety of high temperature superconductor, ferroelectric and metal-conducting oxides.[229-231] Under optimized processing conditions,[232] it was reported that amorphous $LaAlO_3$ thin films without a SiO_2 layer could be obtained by laser molecular beam epitaxy (MBE). The sharp interface between the $LaAlO_3$ and Si substrate were achieved by forming a hydrogen-terminated surface by hydrofluoric acid (HF) dip prior to growth, which in turn prevented the oxidation of silicon at a lower growth temperature and pressure (500°C and 5.0×10^{-5} Pa). This phenomenon was also observed in other studies[233,234] on $LaAlO_3$ films on Si, and has been considered to give an advantage over HfO_2 films. More recent work[103,235] has also demonstrated that $LaAlO_3$ could remain amorphous up to high

temperatures (e.g., 850°C). The dielectric permittivity of $LaAlO_3$ is in the range of 13-15.[103,206,232,234,236] However, dielectric permittivity values as high as 25 were also achieved by molecular beam epitaxy.[237]

There has also been much recent interest in the rare earth oxides of praseodymium and gadolinium due to their attractive feature of having a relatively close lattice match with silicon (e.g., $a(Gd_2O_3)$ = 10.812Å; $2a(Si)$ = 10.862Å).[177] This offers the possibility for epitaxial growth, which thereby eliminates problems related to grain boundaries in polycrystalline films. A recent study[66] shows that an epitaxial layer of Gd_2O_3 on gallium arsenide (GaAs) surface can be grown to fulfil the MOSFET dielectric requirement, which may in turn start a new era for GaAs MOSFETs. A more recent study[207] shows that high purity and conformal praseodymium aluminate ($PrAlO_x$) dielectric thin films can be achieved by ALD. The permittivity of the thin film with the stoichiometry of $Pr_{1.15}Al_{0.85}O_3$ was 18. The film obtained, with the physical thickness of 19 nm, also displayed good electrical properties with a positively flatband voltage shifts of 0.51 V, low hysteresis (~ 4mV) and low leakage current density (1.7×10^{-7} Acm^{-2} at 2 $MVcm^{-1}$). Meanwhile, work on gadolinium aluminate ($GdAlO_x$) was mostly reported in the search for alternate materials for neutron absorption and control rods in nuclear applications.[228,238,239] In contrast to their oxides, $PrAlO_x$ and $GdAlO_x$ have not been fully investigated for gate dielectric applications.

Similarly, the incorporation of neodymium (Nd) ions in insulating hosts has important applications as solid-state laser materials, luminescent materials, protective coatings on stainless steels and optical amplifiers for fibre optic communication.[69,70,240,241] In addition, a substantial amount of effort has also been exerted in developing neodymium oxide thin films for a replacement of the conventional SiO_2 based gate dielectric.[71,72,177,223,242] The dielectric properties of Nd_2O_3 thin films were

first reported[243] in the early '80s, together with their leakage conduction mechanisms.[244,245] A clear consensus shows that at low field, the current is ohmic and the conduction is due to the hopping of the carriers between the localized sites. However, at high field (> 1 $MVcm^{-1}$), the current is governed by both space-charge limited and Schottky type conduction. The dielectric permittivity of Nd_2O_3 was in the range of 10-14 and the breakdown field strength was approximately $1.5MVcm^{-1}$.[71,242,243,246] However, despite those encouraging results from Nd_2O_3, it was later discovered[71] that Nd_2O_3 thin films were chemically unstable upon annealing treatment and partially transformed to NdO(OH) when exposed to atmospheric conditions. Work on $NdAlO_x$ was mostly reported for the finding of alternate ceramic materials for microwave applications,[247] a diffusion barrier in solid-oxide fuel cell structure[248] and other applications similar with those perovskite aluminates previously mentioned. Nevertheless, since little is still known about $NdAlO_3$, this has motivated us to further exploit these perovskite thin films for gate dielectric applications.

5.2. GROWTH AND CHARACTERIZATIONS OF NEODYMIUM ALUMINATE THIN FILMS

Growth of $NdAlO_x$ thin films have previously been achieved by various deposition methods including pulsed laser deposition,[249] e-beam evaporation[248] and sol-gel deposition.[250] Nevertheless, a homogeneous distribution of neodymium ions (Nd^{3+}), in a host matrix (e.g., SiO_2), is relatively difficult to achieve due to their clustering tendency. This is because in a fully connected network such as SiO_2, the absence of non-bridging oxygen atoms results in a poorer integration of rare earth ions, hence a clustering of the Nd^{3+} ions.[251] The addition of alumina as a co-dopant effectively eliminates the microscopic segregation by providing

Nd^{3+} ions a favourable coordination state, thereby keeping them homogenously dispersed.[252] The Nd-Al oxide ceramics are usually prepared by solid-state reaction, in which high temperatures (>1600°C) are demanded for the diffusion of one component into the other. The limitations of the latter approach are the differential vapour pressures of each individual source and the contamination from halide ions (e.g., Cl) that deteriorates the film quality. An alternative route is the use of molecular compound precursors for chemical vapour deposition[253,254] (CVD) or atomic layer deposition (ALD).[71] To date, however, very few studies have been realized on characteristics of $NdAlO_x$ due to a lack of suitable precursors with appropriate stability, volatility and decomposition characteristics. $NdAlO_x$ thin films have been deposited by ALD[71] using $Nd(thd)_3$ (thd = 2,2,6,6,-tetramethyl-3, 5-heptanedionato) precursor together with the hazardous pyrophoric precursor, [$Al(CH_3)_3$ / H_2O], required as the Al and O_2 sources respectively. A simpler approach is to utilize single-source heterometal alkoxides, $[Nd\{Al(OPr^i)_4\}_3(Pr^iOH)]$ or $[NdAl(O^iPr)_6(Pr^iOH)]_2$, precursors containing the preformed lanthanide and Al atoms in the required 1:1 stoichiometry.[253-255] This allows a better mixing of the components at atomic level, significantly lower decomposition temperature and free from halide ion contamination.[253]

Liquid injection MOCVD and ALD experiments were carried out on the Aixtron AIX 200FE AVD reactor fitted with the "Trijet"™ liquid injector system.[102] During the MOCVD experiments, oxygen was introduced at the inlet of the reactor. For the ALD experiments, the oxidant was replaced by water vapour, which was controlled by a pneumatic valve. The substrate was rotated throughout all experiments. Films of neodymium aluminate were deposited on Si (100) substrates using a 0.05M solution of $[NdAl(O^iPr)_6(Pr^iOH)]_2$ in toluene. Full MOCVD and ALD growth conditions can be found in Tables 5.2.1.

Growth rates were calculated from the weight gained by the substrate during the growth run. Film thicknesses were calculated by assuming the film has the same density as $LaAlO_3$ (6.57 g cm^{-3}).

	MOCVD	ALD
Substrate temperature	300-600°C (Si 100)	180-350°C
Evaporator temperature	200°C	175°C
Pressure	5 mbar	5 mbar
Injection rate	30 $cm^3 h^{-1}$	2.5µl / pulse
Solvent	Toluene	Toluene
Concentration	0.05 M	0.05 M
Argon flow	200 $cm^3 min^{-1}$	200 $cm^3 min^{-1}$
Oxygen flow	100 $cm^3 min^{-1}$	—
Run time	10 min	—
Pulse sequence (seconds) (Precursor/purge/water/purge)	—	2/2/0.5/3.5
Number of cycles	—	400

Table 5.2.1. Growth conditions used for the deposition of $NdAlO_x$ by liquid injection MOCVD and ALD using $[NdAl(OPr^i)_6(Pr^iOH)]_2$.

Figure 5.2.1 shows the effect of growth temperature on the growth rate for $NdAlO_x$ by liquid injection MOCVD. The growth rate increases in the temperature range of 300-450°C. This corresponds to the region of kinetic control in which the film growth is dominated by thermal decomposition of the precursor onto the substrate. The oxide growth rate reaches a maximum at 450°C before decreasing rapidly due to thermal depletion of the precursor in the gas phase and a poorer adhesion on the target substrate between 450°C and 600°C.[253] In turn, the maximum growth rate of this material is still greater than the $LaAlO_x$ previously reported by MOCVD at 450°C from the analogous precursor

$[LaAl(O^iPr)_6(Pr^iOH)]_2$.[177] The trend of increasing growth rate across the lanthanide series is most likely due to the extra volatility associated with the decreasing ionic radii of the lanthanide metal. The temperature for the onset of growth increases across the series, indicating an increase in thermal stability as the size of the ionic radii of the lanthanide decreases.

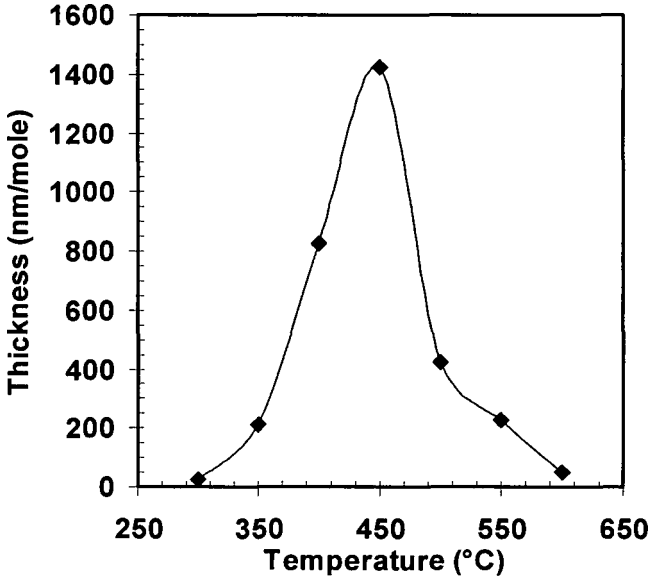

Figure 5.2.1. Variation of growth rate with substrate temperature for $NdAlO_x$ films grown by liquid injection MOCVD using $[NdAl(OPr^i)_6(Pr^iOH)]_2$ precursor.

The growth rate of $NdAlO_x$ by ALD is shown in Fig. 5.2.2 with a maximum of 0.52 nm $cycle^{-1}$ at 180°C. The growth rate steadily decreases over the temperature range 180-350°C, which can also be ascribed to desorption from the substrate surface. This shows that the precursor is thermally stable up to 350°C. The growth of $NdAlO_x$ by ALD was not self limiting, with the growth rate increasing with injected volume of precursor $cycle^{-1}$. This is consistent with the lack of self-limiting ALD previously observed for $[La(Al(OPr^i)_6(Pr^iOH)]_2$,[177] and can be attributed to precursor decomposition via beta-hydride elimination from the $[OPr^i]$ ligand,[177] or to the presence of trace residual water inside the modified MOCVD reactor which had not been fully removed during

the purge step. The inset of Fig. 5.2.2 shows a plot of ALD cycles against variation of film thickness for $NdAlO_x$ films. The growth rate of $NdAlO_x$ had a linear relationship with the number of ALD cycles showing that the deposition of this material was highly controllable, despite a lack of self limiting growth.

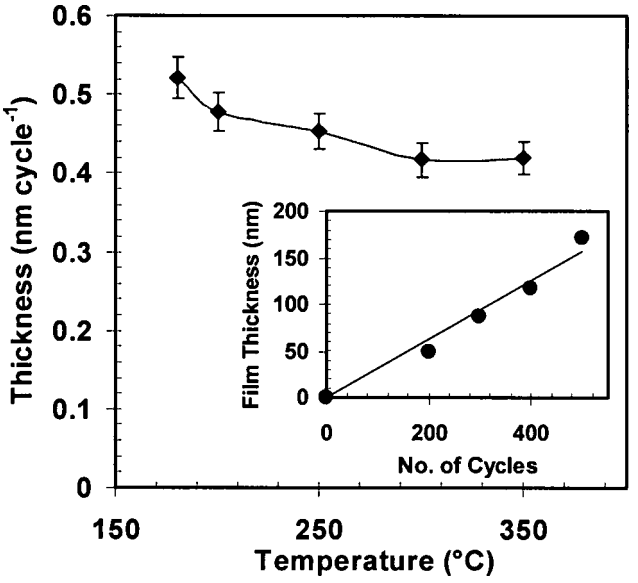

Figure 5.2.2. Variation of growth rate with substrate temperature, with 5% error bars, for $NdAlO_x$ films grown by liquid injection ALD using $[NdAl(OPr^i)_6(Pr^iOH)]_2$ precursor. The inset shows a variation of film thickness with number of ALD cycles at 450°C growth temperature.

The atomic compositions of the $NdAlO_x$ films were determined by Auger Electron spectroscopy (AES) and the data is shown in Table 5.2.2. All the films are of a high purity with carbon not detected at an estimated detection limit of 0.5 at%. The AES data shows that the $NdAlO_x$ films, grown by ALD, are all lanthanide-deficient. The Nd/Al ratio varies from 0.30 to 0.42. A similar compositional effect was observed in $LaAlO_x$ films deposited by liquid injection ALD[177] in which La/Al ratios of 0.50 to 0.61 were observed. The reason for the lanthanide deficiency is not known, but at the relatively low growth temperatures used in ALD (180 –

350 °C), it is unlikely to be due to thermal decomposition of the precursor. It is more likely that the lanthanide deficiency is intrinsic to the deposition process itself, and detailed mechanistic studies would be required fully to elucidate this. In the $NdAlO_x$ films grown by MOCVD, the Nd / Al ratio shows a marked variation with deposition temperature. The $NdAlO_x$ films grown at 300 and 450°C are closest to the target 1:1:3 stoichiometry of $NdAlO_3$. The films grown between these two temperatures are neodymium rich whilst the films grown at substrate temperatures over 450°C are aluminium rich. The compositional data are similar to those seen previously with $LaAlO_x$ films grown by MOCVD.[177] The trends seen may be due to thermal decomposition of the precursor in the gas-phase, leading to partial separation of the Nd and Al components and pre-deposition of non-volatile neodymium oxides.

Temperature (°C)	Technique	Sample	Nd	Al	O	Nd/Al
300	MOCVD	910	16.1	14.4	69.5	1.12
350	MOCVD	909	29.3	13.5	57.2	2.17
400	MOCVD	908	25.1	18.7	56.2	1.34
450	MOCVD	911	20.1	23.2	56.7	0.87
500	MOCVD	912	16	29.5	54.5	0.54
180	ALD	916	10.3	34.5	55.3	0.30
250	ALD	917	9.9	31.8	58.3	0.31
350	ALD	919	12.9	30.7	56.4	0.42

Table 5.2.2. Auger electron spectroscopy data showing the composition (at%) of $NdAlO_x$ films deposited by liquid injection MOCVD and ALD using $[NdAl(OPr^i)_6(Pr^iOH)]_2$.

In order to pursue high quality gate dielectrics, surface passivation prior to the deposition of the alternate dielectric will be necessary. It is very desirable for the dielectric film to remain amorphous up to relatively high temperatures, in other words, to withstand the source-drain

activation anneal steps during CMOS processing. Those previous studies[178,216,217,237,256,257] have demonstrated that nitrogen incorporation can strengthen the immunity against oxygen diffusion by suppressing the interfacial layer formation during processing, thereby reducing the leakage currents. For that reason, the post deposition annealing (PDA) was carried out in an N_2 ambient instead of O_2 ambient, in order to avoid excess oxidation and minimize the interlayer. To investigate this, selective studies on the effects of high temperature post deposition annealing were carried out only on near stoichiometric samples, to that of $NdAlO_3$, achieved by MOCVD. Samples of $NdAlO_x$ films, grown by MOCVD at 450°C, were subjected to high temperature (750-950°C) annealing in pure nitrogen (N_2) ambient for 60 seconds. Subsequently a forming gas anneal (FGA), H_2:N_2 in the ratio 1:9, was carried out together with a control as-deposited sample at 400°C for 30 minutes after post metallization.

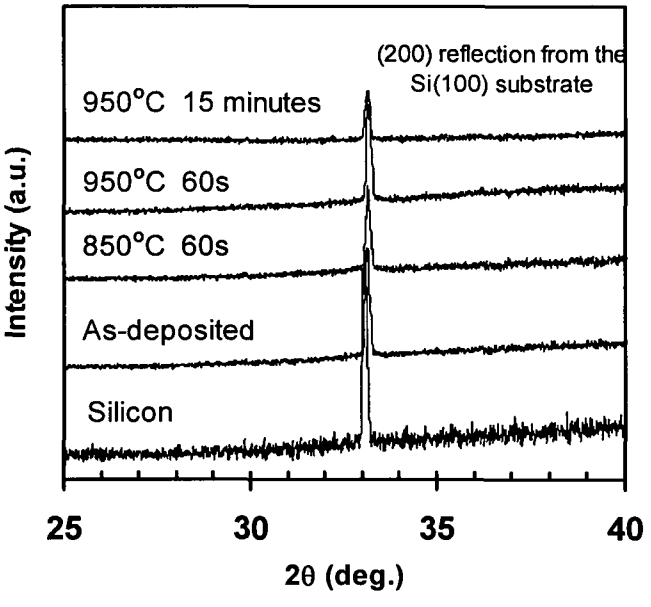

Figure 5.2.3. X-ray diffraction (XRD) data for an $NdAlO_x$ film (Nd/Al = 0.87, $NdAlO_x$ = 11nm) deposited by MOCVD at 450°C and then annealed in N_2 at 750, 850, 950°C for 60 seconds and at 950°C for 15 minutes. For comparison, data from a crystalline silicon sample was used.

To assess the phase transition of the gate dielectric, x-ray diffraction (XRD) was performed on the studied films using nickel-filtered Cu Kα radiation (λ=1.5405Å) with a 2θ increment of 0.2° per second. The x-ray diffraction traces of the as-grown and PDA samples only exhibited background features, similar to that of silicon, devoid of any crystalline diffraction features (Fig. 5.2.3), suggesting that they were essentially amorphous.

Cross section transmission electron microscopy (TEM) samples were prepared by hand-grinding to ≈ 40μm and final thinning using a Gatan precision ion polishing system (PIPS). TEM observations were made using a JEOL 2000FX operated at 500kV. TEM micrographs (Fig. 5.2.4) showed that the high-k thickness and a thin native oxide interlayer, adjacent to the silicon substrate, changed from 11nm and 1.5nm respectively to 10.4nm and 2.5nm respectively after 950°C PDA. This could be due to inter-diffusion of oxygen between SiO_2 and $NdAlO_x$.

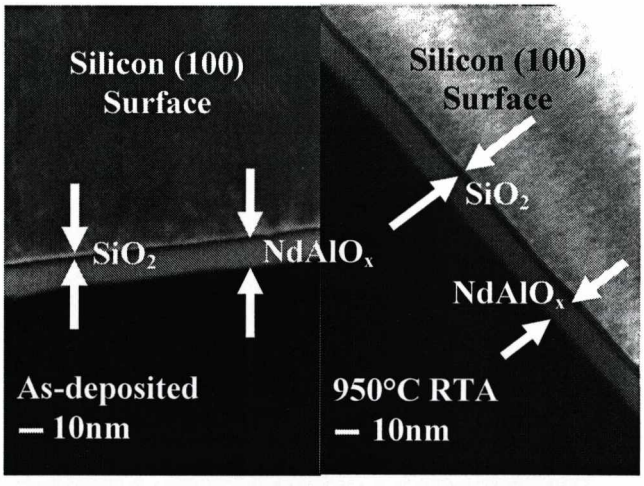

Figure 5.2.4. Cross sectional TEM images, of the as-deposited and 950°C PDA $NdAlO_x/SiO_2$ samples, showing the high-k thickness (11nm and 10.4nm) and a thin (1.5nm and 2.5nm) native oxide interlayer adjacent to the silicon substrate, respectively.

To investigate any inter-diffusion between the $NdAlO_x$ and silicon substrate, medium energy ion scattering (MEIS) experiments were carried out using a nominally 200 keV He^+ ion beam at 70.5° scattering angle. A comparison of MEIS energy spectra between the as-deposited film and the annealed film is shown in Fig.5.2.5. The inelastic scattering of He^+ ions as a function of sample penetration provides an effective depth profile of the different target elements in the sample. MEIS results show that the thickness of the $NdAlO_x$ was found to be ~10nm in both films, which is in a good agreement with TEM cross section analysis (Fig. 5.2.4). After annealing, little change was observed with the layer thickness or the aluminium content from MEIS energy spectra indicating that interdiffusion between the film and substrate was insignificant.

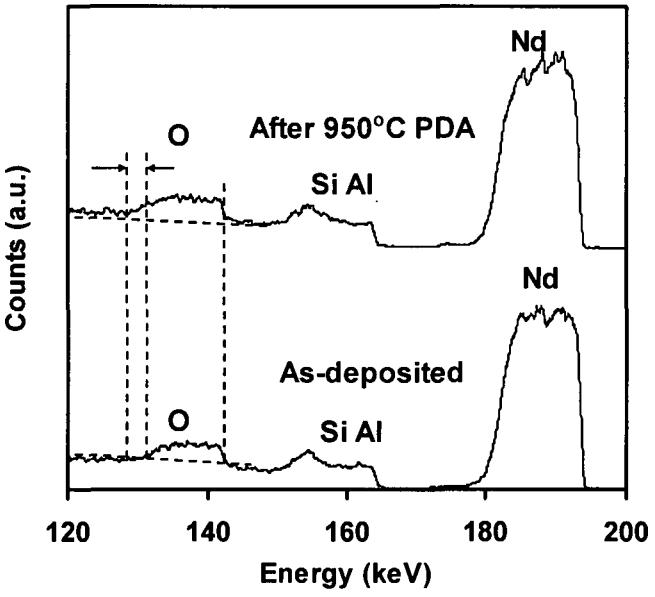

Figure 5.2.5. Medium energy ion scattering spectrums of $NdAlO_x/SiO_2$ stacks before and after rapid thermal annealing at 950°C in N_2 ambient for 60 seconds.

Metal-oxide-semiconductor capacitors ($Au/NdAlO_x/SiO_2/n\text{-}Si$) were fabricated with an area of 4.9×10^{-4} cm^2. The backside contact of Si wafer was cleaned with a buffered HF solution and subsequently a 2000Å

thickness of Al film was deposited by thermal evaporation. High-frequency capacitance-voltage (HFCV) measurements were conducted using a HP4192 impedance analyzer. Measurements were performed in parallel mode from a strong inversion towards a strong accumulation (and vice versa), with a sweep rate of 0.05 V/s at various frequencies (1kHz-1MHz). The HFCV characteristics of as-grown and PDA samples are shown in Fig. 5.2.6. Both as-grown and PDA films exhibited small counter-clockwise hysteresis (< 0.1 V) and no frequency dispersions were observed at any measuring frequencies. A positive shift of flatband voltage (V_{FB}) (ΔV_{FB} = 0.97V) of as-grown samples was observed and contributed to a fixed negative oxide charge. However, a near ideal flatband voltage (V_{FB} = 0.65V) was obtained in the 950°C PDA samples. This may indicate that negative fixed oxide charges could be compensated by nitrogen induced positive fixed oxide charges generated during annealing at the $NdAlO_x$ / SiO_2 interface.[178,216,217,256,257]

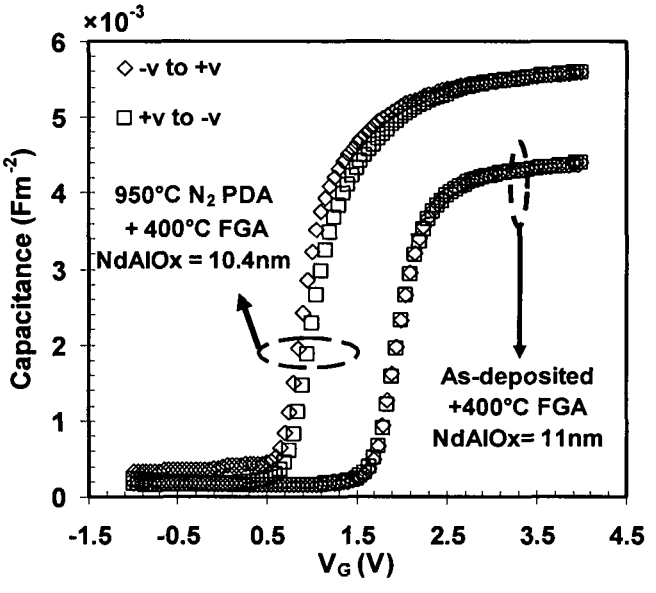

Figure 5.2.6. High frequency capacitance-voltage (C-V) curves at 1MHz for [Au/$NdAlO_x$/ SiO_2/n-Si/Al] capacitors deposited using $[NdAl(OPr^i)_6(Pr^iOH)]_2$ single source precursor. Both as-grown and 950°C PDA samples were post metallization annealed with forming gas (FGA) at 400°C for 30 minutes.

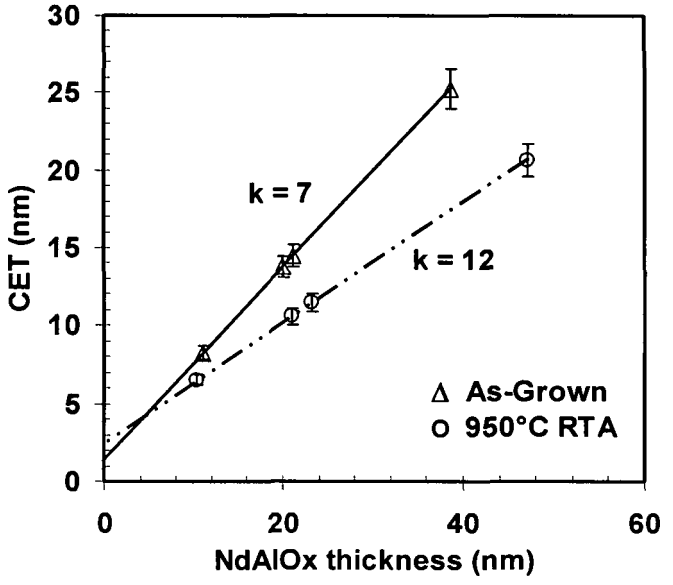

Figure 5.2.7. The plot of capacitance equivalent thickness (CET), extracted from C-V measurements in Fig. 5.2.6, of the $NdAlO_x$ films against the physical thicknesses.

Terman analysis[145] yields an interface density of states, D_{it}, of 1.99×10^{11} $cm^{-2}eV^{-1}$ and 4.49×10^{11} $cm^{-2}eV^{-1}$ at flatband level for as-grown and 950°C PDA samples respectively. This is lower than D_{it} of other recent high-k candidates, D_{it} of 2.5×10^{12} $cm^{-2}eV^{-1}$ found in $La_{1.3}Hf_{1.0}O_{4.1}$,[208] but higher than the D_{it} of 5×10^{10} $cm^{-2}eV^{-1}$ shown by $Y_xHf_{1-x}O_y$ (x = 0.065).[258] Despite an increase of the interfacial layer in PDA samples, the measured capacitance in strong accumulation was found to be higher than that of the as-grown samples. Figure 5.2.7 shows a plot of the high-k dielectric thickness against capacitance equivalent thickness (CET). The slope revealed the $NdAlO_x$ dielectric permittivity (ε_k) to be 7 and 12 in the as-grown and 950°C PDA films respectively, which explained the increased capacitance observed in PDA samples. Furthermore, a small increase (from 1.5nm to 2.5nm from TEM cross sections) of the interfacial layer thickness, after N_2 PDA is apparent.

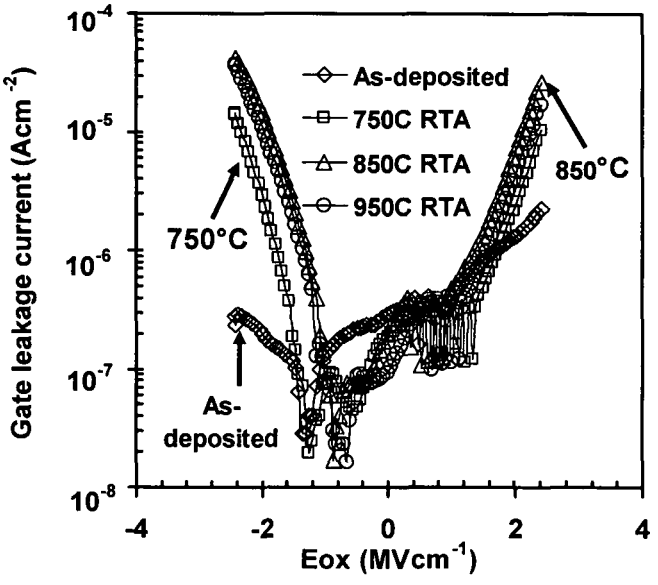

Figure 5.2.8. Gate leakage current density vs. electric field (Eox) applied across the $NdAlO_x/SiO_2$ stacks as a function of PDA temperatures. The $NdAlO_x$ films thickness was $t_{high\text{-}k}$ ~ 10.4 to 11 nm.

The gate leakage current densities (J) at 2MVcm^{-1} in all films, even after 950°C PDA, were below 7×10^{-6} Acm^{-2} (Fig. 5.2.8). This is an order of magnitude lower than hafnium aluminates[259] (at 2MVcm^{-1}) previously reported and also comparable with other leading edge high-k dielectrics.[164,206-208,232] The average breakdown of the $NdAlO_x$ films, regardless the annealing treatment, also occurred at the equivalent field strength of 4MVcm^{-1}. Both increases of I (Fig.5.2.8) and ε_k (Fig.5.2.7) with temperature could be due to a small increment in the film crystallinity after PDA. However, the degree of crystallinity was so insignificant that it is below the detectable level by XRD, TEM and MEIS analysis.

Preliminary C-V results of $NdAlO_x$ film, deposited by liquid injection ALD technique, are demonstrated in Fig. 5.2.9. Excellent electrical characteristics were obtained as depicted by the insignificant hysteresis, near ideal flatband voltage and an interface state density of order ~10^{11}

$cm^{-2}eV^{-1}$. This shows the feasibility and compatibility in using the $[NdAl(O^iPr)_6(Pr^iOH)]_2$ precursor with the ALD process.

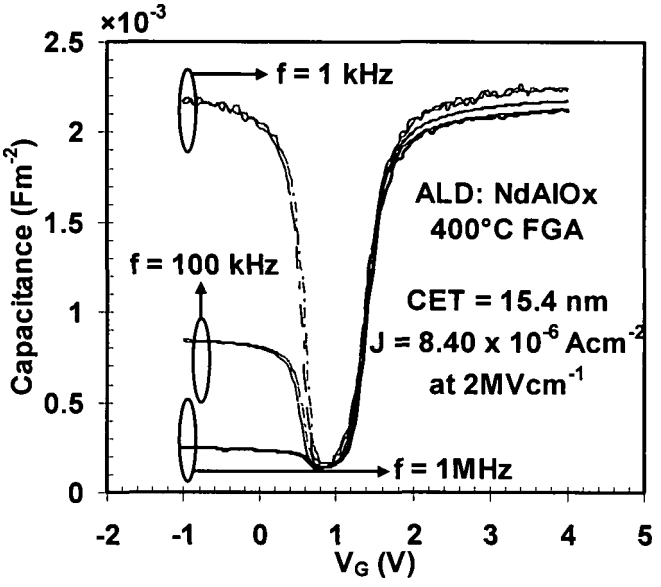

Figure 5.2.9. High frequency capacitance-voltage (C-V) curves at various frequencies (1kHz to 1MHz) for [Au/$NdAlO_3$/ SiO_2/n-Si/Al] capacitors deposited by ALD at 200°C using $[NdAl(OPr^i)_6(Pr^iOH)]_2$ single source precursor. The sample was post metallization annealed with forming gas (FGA) at 400°C for 30 minutes. The $NdAlO_x$ films thickness was $t_{high\text{-}k}$ ~ 17 nm.

In conclusion, neodymium aluminate ($NdAlO_x$) thin films have been deposited by liquid injection MOCVD over the temperature range 250 – 600°C, and by liquid injection ALD over the temperature range 180-300°C using the bimetallic alkoxide $[NdAl(OPr^i)_6(Pr^iOH)]_2$ single source precursor. The MOCVD films were high purity with no carbon detected by AES (est. detection limit ~ 0.5 at.%). The films endured high temperature stress and remained amorphous up to 950°C for 15 minutes as depicted in XRD analysis. No significant level of crystallinity or movements of metal ions were in evidence after annealing treatment at 950°C as indicated in MEIS energy spectra. Electrical properties of $NdAlO_x$ thin films grown by MOCVD, after receiving high temperature stress, were presented for the first time. Good electrical integrity was

maintained even after 950°C PDA as shown by C-V and I-V results, showing the extracted dielectric permittivity of 12, a low leakage density of 4.67×10^{-6} Acm^{-2} at $2MVcm^{-1}$ and a density of interface states at flatband level of 4.49×10^{11} $cm^{-2}eV^{-1}$. These features make the neodymium aluminate a possible candidate for the dielectric replacement.

Chapter 6 – Conclusions and Future work

The future of the semiconductor devices (e.g., transistors and memory capacitors) in the next 5-10 years will rely on the continuing performance and cost performance improvement via the dielectric scaling of the high-k materials. Although many recent high-k gate dielectric candidates may meet many electrical targets, scaling below 1nm capacitance equivalent thickness (CET) remains difficult.[260,261] This is because a SiO_x interfacial layer may be required for reliability and performance. For example, in a material growth perspective, the absence of a native interfacial layer can rougher the dielectric surface. This can be associated with the nucleation of bonding, as the metal atoms do not adhere well to the surface. Therefore, in order to continue the aggressive scaling into the sub-nanometer regime (e.g., memory capacitor dielectrics require CET to be below 2nm, with the leakage current density of $\sim 10^{-8}$ Acm^{-2} and the physical thickness below 10nm), it is necessary to acquire high dielectric permittivity (i.e., $\varepsilon_k > 30$).[260]

In this thesis, the liquid injection MOCVD/ALD processes have been used to investigate the growth characteristic of the metal oxides, rare-earth oxides and its associated alloys. The scope of the work also remains close to the development of new precursors and their associated physical/electrical characteristics. Therefore the thicknesses of the deposited films reported in this work tend to lie in a thicker regime (>10nm) rather than the associated gate dielectric application (<5nm). However, building on the success of the novel precursors investigated here, future work would involve the optimization of films with thickness relevant to the industry.

Despite a well known issue of the existence of intrinsic traps in the crystalline phases, hafnium-based oxides are currently leading candidates for high-k dielectrics in gate insulators and dynamic random access memory capacitors. The suitability of cyclopentadienyl-type precursors, the isopropyl-substituted (^{i}PrO), for the deposition of HfO_2 were examined by both MOCVD and ALD processes. The films obtained from the Cp-type precursor clearly show some advantageous features over its predecessors including: (i) low contamination levels (the highest being 2.1-2.3 at.-%); (ii) amorphous and thermally stable up to 700°C; and (iii) the dielectric permittivity of 19-21. The results obtained in this work show that Cp-type compounds with ^{i}PrO ligands are suitable for HfO_2 depositions via chemical vapour deposition (i.e., MOCVD and ALD). The precursor chemistry, the depositing techniques and the subsequent process treatments are therefore key factors to the success of the development of high quality high-k thin films.

The isopropyl ligand has also been applied in the development of rare-earth alloys, $NdAlO_x$, thin films using the single source precursor. Although neodymium is categorised as one of the rare earth elements, it is in fact abundant in nature and constitutes 38 parts per million of the earth's crust. The films obtained from single source precursor, containing neodymium atoms, were of high purity and shown to endure high temperature stress as high as 950°C for 15 minutes. Good electrical integrity was maintained after 950°C temperature stress as shown by C-V and I-V results. The single source precursor thus offers a viable route to achieve high-quality pseudobinary alloy thin films, not previously successfully processed by chemical vapour deposition.

Material engineering for practical applications of high-k dielectrics has mainly concentrated on preventing crystallization by reducing both the thermal budget and the film thickness. However, as with HfO_2, it has proven difficult to withstand a high thermal budget above 1000°C and

remains amorphous. Therefore an optimization of the crystalline state is crucial. Crystalline HfO_2 exists in the monoclinic phase at normal pressure and temperature below 1700°C, while a transformation into tetragonal phase takes place at higher temperatures. However when the crystal size is reduced to the nanometer range, and by adding suitable dopants such as Si, the increased stability of the tetragonal phase is observed even at lower temperatures.[262,263] An apparent benefit of tetragonal films is a massive increase of a dielectric constant to be as high as ε_k~70 for the predicted tetragonal phase HfO_2.[264] There has been much recent interest in the lanthanide (rare earth) series and the effect of the rare earth doping is not widely known yet. Rare earth doping may help to further stabilize higher symmetry such as the tetragonal (*t*) phase in HfO_2. The followings are the suggested future work: (i) to investigate the effect of neodymium doped hafnium oxide ($Hf_xNd_{1-x}O_y$) on its physical and electrical characteristics; and (ii) to observe the existence of the *t*-phase $Hf_xNd_{1-x}O_y$ and the correlation with its electrical characteristics.

Since the atomic layer deposition (ALD) process is becoming the technique of choice for the semiconductor industry, $Hf_xNd_{1-x}O_y$ thin films are suggested to be prepared by such a method using the organometallic cyclopentadienyl type precursor with the isopropyl-substituted (^{i}PrO) for hafnium and neodymium rich thin films. The deposited films should be divided into sub-categories such as: (a) the control sets, as a function of oxide thickness (e.g., 5-20nm); and (b) the post depositing anneal sets, as a function of annealing temperature (e.g., 400-1000°C) at a specific anneal duration (e.g., 1-5 minutes). The films' composition and crystallinity can be determined by x-ray photoelectron spectroscopy (XPS) and x-ray diffraction (XRD) respectively. The formation of the *t*-phase should be shown as both a function of annealed temperatures and neodymium doping atomic percentage by XRD analysis. To assess electrical characteristics, MOS capacitors should be fabricated [e.g., of the ($Au/Hf_xNd_{1-x}O_y/SiO_x/n$-

Si/Al) structure]. In order to confirm the film's homogeneity, different gate area (i.e. the gate diameter size) should be formed by thermal evaporation. Capacitance-voltage (C-V) and current-voltage (I-V) measurements should be performed on capacitors with different areas and results presented should be representative of ten sites across each wafer. Electrical parameters [e.g., ε_k, CET, leakage current density (J) and the density of interface states (D_{it})] can be extracted from the latter techniques, while physical thickness can be validated with the transmission electron microscopy (TEM) and the spectroscopic ellipsometry (SE). The dielectric permittivity should be extracted from a plot of capacitance equivalent thickness (CET) against physical thicknesses, as a function of neodymium doping (e.g., 0-100 at %). This should lead further to an observation on the variation of the extracted dielectric permittivity against neodymium doping percentage. The leakage current density for $Hf_xNd_{1-x}O_y$ should also be shown as a function of both annealed temperatures and neodymium doping. Remarks should be made upon benefits and drawbacks on the obtained electrical properties of the *t*-phase $Hf_xNd_{1-x}O_y$ thin films. Finally, with a confidence in stabilizing the *t*-phase of $Hf_xNd_{1-x}O_y$, optimized $Hf_xNd_{1-x}O_y$ should be reported in terms of the relevant thickness regime (i.e., CET below 2nm for the highest obtainable ε_k).

Finally, a reconstruction model has been implemented for C-V measurements in order to minimize the measurement errors. This method can be integrated easily into a routine C-V measurement procedure. The origin of frequency dispersion effect was also investigated. Taking into an account of both the presence of back contact imperfection and the lossy interfacial layer, the dielectric relaxation was proposed to be another reason that caused the frequency dependence in the dielectric permittivity. This was attributed to movements of unbounded metal ions or combinations with defects that resulted in the dielectric relaxation, hence the variation of accumulation capacitance leading to the frequency

dependence of dielectric permittivity. However, the mechanism that triggers the dielectric relaxation remains to be further investigated. To clearly investigate the mechanism, the dielectric characteristics of high-k stacks should be carefully measured at cryogenic temperature (10-300 K) where strong relaxation is presented.[176] Capacitance and the dielectric loss (i.e., tan δ) can be measured with an impedance LCR meter (e.g., HP4192A), which is equipped with a liquid nitrogen cryostat and a temperature controller. Upon cooling the sample with liquid nitrogen, measurements should be taken at intermediate frequencies (i.e., from 100Hz to 1MHz). The observation should be made upon: (i) the frequency dependent nature of the dielectric permittivity at various measuring frequencies, as a function of temperature. This is because the decreasing magnitude of dielectric permittivity with increasing frequency and a maximal shifting to higher temperatures demonstrates a typical relaxation effect;[176] and (ii) the correlation between dielectric loss at various measuring frequencies as a function of temperature, in order to identify the hopping effect. It has been suggested that electrons may sometimes cause dielectric relaxation by moving like thermally activated charged particles (i.e., the hopping effect).[265,266] This hopping effect often creates the donor-type extrinsic defects, and upon recombination with the acceptor sites, the dipole moments are generated and induce the dielectric relaxation. This ion hopping effect is also proportional with the dielectric loss values. Also, it would be interesting to see the effect of rare earth doped high-k dielectrics (e.g., $Hf_xNd_{1-x}O_y$ as previously discussed) on the loss tangents, and hence the induced dielectric relaxation mechanism. This may provide a further insight into the understandings of the dielectric permittivity properties, which will lead to a realisation of the future gate dielectric replacement for the future roadmap.

REFERENCES

1 International Technology Roadmap for Semiconductors, Semiconductor Industry Association (2005).

2 S. E. Thompson, R. S. Chau, T. Ghani, K. Mistry, S. Tyagi, and M. T. Bohr, Semiconductor Manufacturing, IEEE Transactions on **18,** 26-36 (2005).

3 Intel, in *http://www.intel.com/technology/mooreslaw/index.htm.*

4 G. Moore, Electronics **38,** 114-117 (1965).

5 E. Vogel, Nat Nano **2,** 25-32 (2007).

6 R. Rios, N. D. Arora, and H. Cheng-Liang, Electron Device Letters, IEEE **15,** 129-131 (1994).

7 A. S. Spinelli, A. Pacelli, and A. L. Lacaita, Electron Device Letters, IEEE **22,** 281-283 (2001).

8 D. A. Muller, Nat Mater **4,** 645-647 (2005).

9 D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, Nature **399,** 758-761 (1999).

10 G. D. Wilk, R. M. Wallace, and J. M. Anthony, Journal of Applied Physics **89,** 5243-5275 (2001).

11 C. M. Garner, G. Kloster, G. Atwood, L. Mosley, and A. C. Palanduz, Microelectronics and Reliability **45,** 919-924 (2005).

12 R. Chau, S. Datta, and A. Majumdar, in *Opportunities and challenges of III-V nanoelectronics for future high-speed, low-power logic applications*, 2005, p. 17-20.

13 L. Chang, Y.-K. Choi, J.Kedzierski, N.Lindert, X. Peiqi, J. Bokor, H. Chenming, and T.-J. King, Circuits and Devices Magazine, IEEE **19,** 35-42 (2003).

14 S. Xiong and J. Bokor, Electron Devices, IEEE Transactions on **50,** 2255-2261 (2003).

[15] J. Chen, C. Klinke, A. Afzali, and P. Avouris, Applied Physics Letters **86,** 123108 (2005).

[16] S.-W. Chung, J.-Y. Yu, and J. R. Heath, Applied Physics Letters **76,** 2068-2070 (2000).

[17] R. H. Chen, A. N. Korotkov, and K. K. Likharev, Applied Physics Letters **68,** 1954-1956 (1996).

[18] C. S. Lent and B. Isaksen, Electron Devices, IEEE Transactions on **50,** 1890-1896 (2003).

[19] Z. Igor, F. Jaroslav, and S. D. Sarma, Reviews of Modern Physics **76,** 323 (2004).

[20] E. W. B. Gerrit, B. Arne, T. Yaroslav, and J. v. W. Bart, Applied Physics Letters **82,** 3928-3930 (2003).

[21] D. E. Nikonov and G. I. Bourianoff, Nanotechnology, IEEE Transactions on **4,** 206-214 (2005).

[22] C. Chaneliere, J. L. Autran, R. A. B. Devine, and B. Balland, Materials Science and Engineering: R: Reports **22,** 269-322 (1998).

[23] A. I. Kingon, J.-P. Maria, and S. K. Streiffer, Nature **406,** 1032-1038 (2000).

[24] I. C. Kizilyalli, R. Y. S. Huang, and R. K. Roy, Electron Device Letters, IEEE **19,** 423-425 (1998).

[25] P. K. Roy and I. C. Kizilyalli, Applied Physics Letters **72,** 2835-2837 (1998).

[26] D. Park, Y.-C. King, Q. Lu, T.-J. King, C. Hu, A. Kalnitsky, S.-P. Tay, and C.-C. Cheng, Electron Device Letters, IEEE **19,** 441-443 (1998).

[27] R. Takahashi, M. Sakashita, A. Sakai, S. Zaima, and Y. Yasuda, Japanese Journal of Applied Physics **43,** 7821-7825 (2004).

[28] M. Koyama, Y. Kamimuta, M. Koike, M. Suzuki, and A. Nishiyama, Japanese Journal of Applied Physics **43,** 1788-1794 (2004).

[29] T. M. Klein, D. Niu, W. S. Epling, W. Li, D. M. Maher, C. C. Hobbs, R. I. Hegde, I. J. R. Baumvol, and G. N. Parsons, Applied Physics Letters **75,** 4001-4003 (1999).

[30] C. I.Li, C. C. Chien, K. T.Huang, P. Y. Chen, H. Y. Wang, S. F.Tzou, S.Chen, J.Lin, T.Fu, R.Tandjaja, S.Ramamurthy, E.Chung, J.Chuang, and W.-S. Chen, in *Superior Spike Annealing Performance in 65nm Source/Drain Extension Engineering*, 2005, p. 163-167.

[31] E. P. Gusev, M. Copel, E. Cartier, I. J. R. Baumvol, C. Krug, and M. A. Gribelyuk, Applied Physics Letters **76,** 176-178 (2000).

[32] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, in *High quality La_2O_3 and Al_2O_3 gate dielectrics with equivalent oxide thickness 5-10Å*, 2000, p. 16-17.

[33] D. A. Buchanan, E. P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M. A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D'Emic, P. Kozlowski, K. Chan, R. J. Fleming, P. C. Jamison, I. Brown, and R. Arndt, in *80 nm polysilicon gated n-FETs with ultra-thin Al_2O_3 gate dielectric for ULSI applications*, 2000, p. 223-226.

[34] D.-G. Park, H.-J. Cho, C. Lim, I.-S. Yeo, J.-S. Roh, C.-T. Kim, and J.-M. Hwang, in *Characteristics of Al_2O_3 gate dielectric prepared by atomic layer deposition for giga scale CMOS DRAM devices*, 2000, p. 46-47.

[35] J. H. Lee, K. Koh, N. I. Lee, M. H. Cho, Y. K. Ki, J. S. Jeon, K. H. Cho, H. S. Shin, M. H. Kim, K. Fujihara, H. K. Kang, and J. T. Moon, in *Effect of polysilicon gate on the flatband voltage shift and mobility degradation for ALD-Al_2O_3 gate dielectric*, 2000, p. 645-648.

[36] L. Manchanda and M. Gurvitch, Electron Device Letters, IEEE **9,** 180-182 (1988).

[37] J. Kwo, M. Hong, A. R. Kortan, K. T. Queeney, Y. J. Chabal, J. P. Mannaerts, T. Boone, J. J. Krajewski, A. M. Sergent, and J. M. Rosamilia, Applied Physics Letters **77,** 130-132 (2000).

[38] J. M. Howard, N. D. Bassim, V. Craciun, and R. K. Singh, Thin Solid Films **453-454,** 411-416 (2004).

[39] Y. Tsuchiya, M. Endoh, M. Kurosawa, R. T. Tung, T. Hattori, and S. Oda, Japanese Journal of Applied Physics **42,** 1957-1961 (2003).

[40] M. Putkonen, T. Sajavaara, L. S. Johansson, and L. Niinistö, Chemical Vapor Deposition **7,** 44-50 (2001).

[41] J. J. Chambers and G. N. Parsons, Applied Physics Letters **77,** 2385-2387 (2000).

[42] K. A. Fleeting, H. O. Davies, A. C. Jones, P. O'Brien, T. J. Leedham, M. J. Crosbie, P. J. Wright, and D. J. Williams, Chemical Vapor Deposition **5,** 261-264 (1999).

[43] M. Putkonen, M. Nieminen, J. Niinisto, L. Niinisto, and T. Sajavaara, Chem. Mater. **13,** 4701-4707 (2001).

[44] P. d. Rouffignac, A. P. Yousef, K. H. Kim, and R. G. Gordon, Electrochemical and Solid-State Letters **9,** F45-F48 (2006).

[45] Z. Xu, A. Daga, and C. Haydn, Applied Physics Letters **79,** 3782-3784 (2001).

[46] J. A. Britten, H. T. Nguyen, S. F. Falabella, B. W. Shore, M. D. Perry, and D. H. Raguin, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films **14,** 2973-2975 (1996).

[47] M. Leskela and M. Ritala, Journal of Solid State Chemistry **171,** 170-174 (2003).

[48] J. A. Gupta, D. Landheer, J. P. McCaffrey, and G. I. Sproule, Applied Physics Letters **78,** 1718-1720 (2001).

[49] J. A. Gupta, D. Landheer, G. I. Sproule, J. P. McCaffrey, M. J. Graham, K. C. Yang, Z. H. Lu, and W. N. Lennard, Applied Surface Science **173,** 318-326 (2001).

[50] Y. Kim, S.-i. Ohmi, K. Tsutsui, and H. Iwai, Solid-State Electronics **49,** 825-833 (2005).

[51] H. J. Osten, J. P. Liu, and H. J. Mussig, Applied Physics Letters **80,** 297-299 (2002).

[52] S. Guha, E. Cartier, M. A. Gribelyuk, N. A. Bojarczuk, and M. C. Copel, Applied Physics Letters **77,** 2710-2712 (2000).

[53] A. C. Jones, H. C. Aspinall, P. R. Chalker, R. J. Potter, K. Kukli, A. Rahtu, M. Ritala, and M. Leskela, Materials Science and Engineering B **118,** 97-104 (2005).

[54] J.-B. Cheng, A.-D. Li, Q.-Y. Shao, H.-Q. Ling, D. Wu, Y. Wang, Y.-J. Bao, M. Wang, Z.-G. Liu, and N.-B. Ming, Applied Surface Science **233,** 91-98 (2004).

[55] Y. H. Wu, M. Y. Yang, A. Chin, W. J. Chen, and C. M. Kwei, Electron Device Letters, IEEE **21,** 341-343 (2000).

[56] J. M. Gaskell, A. C. Jones, H. C. Aspinall, S. Taylor, P. Taechakumput, P. R. Chalker, P. N. Heys, and R. Odedra, Applied Physics Letters **91,** 112912 (2007).

[57] S. Sathyamurthy, M. Paranthaman, H. Y. Zhai, H. M. Christen, P. M. Martin, and A. Goyal, Journal of Materials Research **17,** 2181-2184 (2002).

[58] K. Knoth, R. Huhne, S. Oswald, L. Schultz, and B. Holzapfel, Acta Materialia **55,** 517-529 (2007).

[59] K. Ohmori, P. Ahmet, K. Shiraishi, K. Yamabe, H. Watanabe, Y. Akasaka, N. Umezawa, K. Nakajima, M. Yoshitake, T. Nakayama, K. S. Chang, K. Kakushima, Y. Nara, M. L. Green, H. Iwai, K. Yamada, and T. Chikyow, in *Controllability of flatband voltage in*

high-k gate stack structures - remarkable advantages of La_2O_3 over HfO_2, 2006, p. 376-379.

60 R. L. Nigro, V. Raineri, C. Bongiorno, R. Toro, G. Malandrino, and I. L. Fragala, Applied Physics Letters **83,** 129-131 (2003).

61 H. J. Osten, J. P. Liu, P. Gaworzewski, E. Bugiel, and P. Zaumseil, in *High-k gate dielectrics with ultra-low leakage current based on praseodymium oxide*, 2000, p. 653-656.

62 H. J. Osten, E. Bugiel, and A. Fissel, Solid-State Electronics **47,** 2161-2165 (2003).

63 U. Schwalke, K. Boye, G. Hess, G. Muller, K. Haberle, R. Heller, T. Rulan, G. Tzschockel, J. Osten, A. Fissel, and H. J. Mussig, in *Process Integration of Crystalline Pr_2O_3 High-k Gate Dielectrics*, 2002, p. 407-410.

64 H. C. Aspinall, J. M. Gaskell, P. A. Williams, A. C. Jones, P. R. Chalker, P. A. Marshall, L. M. Smith, and G. W. Critchlow, Chemical Vapor Deposition **10,** 83-89 (2004).

65 H. J. Osten, J. P. Liu, H. J. Mussig, and P. Zaumseil, Microelectronics Reliability **41,** 991-994 (2001).

66 M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, Science **283,** 1897-1900 (1999).

67 D. Goutam Kumar, T. Yi, L. Wei Yip, M. Hoe Keat, and C. Byung Jin, Applied Physics Letters **90,** 183510 (2007).

68 F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, Solid-State Electronics **41,** 1751-1753 (1997).

69 G. Blasse, Chem. Mater. **1,** 294-301 (1989).

70 G. Bonnet, M. Lachkar, J. C. Colson, and J. P. Larpin, Thin Solid Films **261,** 31-36 (1995).

71 A. Kosola, J. Paivasaari, M. Putkonen, and L. Niinisto, Thin Solid Films **479,** 152-159 (2005).

[72] A. Fissel, Z. Elassar, O. Kirfel, E. Bugiel, M. Czernohorsky, and H. J. Osten, Journal of Applied Physics **99,** 074105-6 (2006).

[73] R. B. v. Dover, Applied Physics Letters **74,** 3041-3043 (1999).

[74] D. C. Gilmer, D. G. Colombo, C. J. Taylor, J. Roberts, G. Haugstad, S. A. Campbell, H.-S. Kim, G. D. Wilk, M. A. Gribelyuk, and W. L. Gladfelter, Chemical Vapor Deposition **4,** 9-11 (1998).

[75] S. A. Campbell, D. C. Gilmer, W. Xiao-Chuan, H. Ming-Ta, K. Hyeon-Seag, W. L. Gladfelter, and Y. Jinhua, Electron Devices, IEEE Transactions on **44,** 104-109 (1997).

[76] X. Guo, X. Wang, Z. Luo, T. P. Ma, and T. Tamagawa, in *High quality ultra-thin (1.5 nm) TiO_2-Si_3N_4 gate dielectric for deep sub-micron CMOS technology*, 1999, p. 137-140.

[77] M. Kadoshima, M. Hiratani, Y. Shimamoto, K. Torii, H. Miki, S. Kimura, and T. Nabatame, Thin Solid Films **424,** 224-228 (2003).

[78] C. J. Taylor, D. C. Gilmer, D. G. Colombo, G. D. Wilk, S. A. Campbell, J. Roberts, and W. L. Gladfelter, J. Am. Chem. Soc. **121,** 5220-5229 (1999).

[79] Y. Ma, Y. Ono, and S. T. Hsu, in *Deposition and treatment of TiO_2 as an alternative for ultrathin gate dielectrics*, 1999, p. 355-360.

[80] R. Chau, S. Datta, M. Doczy, J. Kavalieros, and M. Metz, in *Gate Dielectric Scaling for High-Performance CMOS: from SiO2 to High-k* Tokyo, Japan, 2003, p. 124-126.

[81] P. Singer, in *IEDM Focus: Metal Gates/High-k for 45 nm, semiconductor international, http://www.semiconductor.net/article/CA6482837.html* (2007).

[82] Intel, in *http://www.intel.com/technology/architecture-silicon/45nmcore2/index.htm?cid=cim:ggl|corp_us_penryn|k8909|s.*

[83] Y. F. Loo, R. O'Kane, A. C. Jones, H. C. Aspinall, R. J. Potter, P. R. Chalker, J. F. Bickley, S. Taylor, and L. M. Smith, Journal of Materials Chemistry **15,** 1896-1902 (2005).

[84] S. Harasek, A. Lugstein, H. D. Wanzenboeck, and E. Bertagnolli, Applied Physics Letters **83,** 1400-1402 (2003).

[85] S. Taylor, P. A. Williams, J. L. Roberts, A. C. Jones, and P. R. Chalker, Electronics Letters **38,** 1285-1286 (2002).

[86] M. Houssa, V. V. Afanas'ev, A. Stesmans, and M. M. Heyns, Applied Physics Letters **77,** 1885-1887 (2000).

[87] M. Putkonen, J. Niinistö, K. Kukli, T. Sajavaara, M. Karppinen, H. Yamauchi, and L. Niinistö, Chemical Vapor Deposition **9,** 207-212 (2003).

[88] J. Niinisto, M. Putkonen, L. Niinisto, K. Kukli, M. Ritala, and M. Leskela, Journal of Applied Physics **95,** 84-91 (2004).

[89] G. D. Wilk, R. M. Wallace, and J. M. Anthony, Journal of Applied Physics **87,** 484-492 (2000).

[90] M. Zhu, J. Zhu, J. M. Liu, and Z. G. Liu, Applied Physics A: Materials Science & Processing **80,** 135-139 (2005).

[91] J. Zhu, Z. G. Liu, M. Zhu, G. L. Yuan, and J. M. Liu, Applied Physics A: Materials Science & Processing **80,** 321-324 (2005).

[92] C. C. Fulton, T. E. Cook, Jr., G. Lucovsky, and R. J. Nemanich, Journal of Applied Physics **96,** 2665-2673 (2004).

[93] A. K. Jonsson, G. A. Niklasson, and M. Veszelei, Thin Solid Films **402,** 242-247 (2002).

[94] T. Yamaguchi, H. Satake, N. Fukushima, and A. Toriumi, in *Band diagram and carrier conduction mechanism in ZrO_2/Zr-silicate/Si MIS structure fabricated by pulsed-laser-ablation deposition*, 2000, p. 19-22.

[95] M.-T. Wang, T.-H. Wang, and J. Y.-M. Lee, Microelectronics and Reliability **45,** 969-972 (2005).

[96] A. C. Jones, Journal of Materials Chemistry **12,** 2576-2590 (2002).

[97] S. B. Krupanidhi, N. Maffei, M. Sayer, and K. El-Assal, Journal of Applied Physics **54,** 6601-6609 (1983).

[98] K. Sreenivas, M. Sayer, D. J. Baar, and M. Nishioka, Applied Physics Letters **52,** 709-711 (1988).

[99] R. Ramesh, A. Inam, W. K. Chan, F. Tillerot, B. Wilkens, C. C. Chang, T. Sands, J. M. Tarascon, and V. G. Keramidas, Applied Physics Letters **59,** 3542-3544 (1991).

[100] H. Y. Guo and Z. G. Ye, Materials Science and Engineering B **120,** 68-71 (2005).

[101] R. W. Vest and J. Xu, Ferroelectrics **93,** 21 - 29 (1989).

[102] R. J. Potter, P. R. Chalker, T. D. Manning, H. C. Aspinall, Y. F. Loo, A. C. Jones, L. M. Smith, G. W. Critchlow, and M. Schumacher, Chemical Vapor Deposition **11,** 159-169 (2005).

[103] J. M. Gaskell, A. C. Jones, H. C. Aspinall, S. Przybylak, P. R. Chalker, K. Black, H. O. Davies, P. Taechakumput, S. Taylor, and G. W. Critchlow, Journal of Materials Chemistry **16,** 3854-3860 (2006).

[104] J. Niinisto, M. Putkonen, L. Niinisto, K. Arstila, T. Sajavaara, J. Lu, K. Kukli, M. Ritala, and M. Leskela, Journal of The Electrochemical Society **153,** F39-F45 (2006).

[105] A. C. Jones, T. J. Leedham, P. J. Wright, M. J. Crosbie, P. A. Lane, D. J. Williams, K. A. Fleeting, D. J. Otway, and P. O. Brien, Chemical Vapor Deposition **4,** 46-49 (1998).

[106] C. Dubourdieu, E. Rauwel, C. Millon, P. Chaudouët, F. Ducroquet, N. Rochat, S. Rushworth, and V. Cosnier, Chemical Vapor Deposition **12,** 187-192 (2006).

[107] O. Buiu, Y. Lu, S. Hall, I. Z. Mitrovic, R. J. Potter, and P. R. Chalker, Thin Solid Films **515,** 3772-3778 (2007).

[108] L. Niinistö, M. Nieminen, J. Päiväsaari, J. Niinistö, M. Putkonen, and M. Nieminen, physica status solidi (a) **201,** 1443-1452 (2004).

[109] Suntola and J. Antson, in *US Patent 4 058 430* (1977).

[110] T. Seidel, A. Londergan, J. Winkler, X. Liu, and S. Ramanathan, Solid State Technology **46,** 67 (2003).

[111] K. Kukli, M. Ritala, M. Leskela, T. Sajavaara, J. Keinonen, A. C. Jones, and J. L. Roberts, Chem. Mater. **15,** 1722-1727 (2003).

[112] A. W. Ott, J. W. Klaus, J. M. Johnson, and S. M. George, Thin Solid Films **292,** 135-144 (1997).

[113] D. Lenoble, E. Josse, A. Grouillet, F. Arnaud, C. Julien, T. Skotnicki, and M. Haond, in *Investigation of the suitability of spike anneal for advanced CMOS technology*, 2000, p. 392-395.

[114] E. J. H. Collart, S. B. Felch, B. J. Pawlak, P. P. Absil, S. Severi, T. Janssens, and W. Vandervorst, in *Co-implantation with conventional spike anneal solutions for 45 nm n-type metal-oxide-semiconductor ultra-shallow junction formation*, 2006 (AVS), p. 507-509.

[115] J. Niess, S. Paul, S. Buschbaum, P. Schmid, and W. Lerch, Materials Science and Engineering B **114-115,** 141-150 (2004).

[116] R. Lindsay, B. Pawlak, J. Kittl, K. Henson, C. Torregiani, S. Giangrandi, R. Surdeanu, W.Vandervorst, A. Mayur, J. Ross, S. McCoy, J. Gelpey, K. Elliott, X. Pages, A. Satta, A.Lauwers, P.Stolk, and K. Maex, in *A Comparison of Spike, Flash, SPER and Laser Annealing for 45nm CMOS*, San Francisco, 2003, p. D7.4.1.

[117] I. L. Kim, J.-S. Kim, O.-S. Kwon, S.-T. Ahn, J. Chun, and W.-J. Lee, Journal of Electronic Materials **24,** 1435-1441 (1995).

[118] M. Houssa, M. Naili, C. Zhao, H. Bender, M. M. Heyns, and A. Stesmans, Semiconductor Science and Technology, 31 (2001).

[119] J. Petry, W. Vandervorst, and X. Blasco, Microelectronic Engineering **72,** 174-179 (2004).

[120] H. Wong, N. Zhan, K. L. Ng, M. C. Poon, and C. W. Kok, Thin Solid Films **462-463,** 96-100 (2004).

[121] S. Hyunjun and H. Hyunsang, Applied Physics Letters **81,** 4038-4039 (2002).

[122] Z. Zhang, M. Li, and S. A. Campbell, Electron Device Letters, IEEE **26,** 20-22 (2005).

[123] G. D. Wilk and D. A. Muller, Applied Physics Letters **83,** 3984-3986 (2003).

[124] R. Puthenkovilakam, M. Sawkar, and J. P. Chang, Applied Physics Letters **86,** 202902-3 (2005).

[125] S.-W. Huang and J.-G. Hwu, Electron Devices, IEEE Transactions on **50,** 1658-1664 (2003).

[126] C. C. Yeo, M. S. Joo, B. J. Cho, and S. J. Whang, Thin Solid Films **462-463,** 90-95 (2004).

[127] C.-W. Chen, C.-H. Chien, T.-H. Perng, M.-J. Yang, J.-S. Liang, P. Lehnen, B.-Y. Tsui, and C.-Y. Chang, Japanese Journal of Applied Physics **44,** 87-93 (2005).

[128] R. Choi, C. S. Kang, H.-J. Cho, Y.-H. Kim, M. S. Akbar, and J. C. Lee, Applied Physics Letters **84,** 4839-4841 (2004).

[129] M. Yun, M.-S. Kim, Y.-D. Ko, T.-H. Moon, J.-H. Hong, J.-M. Myoung, and I. Yun, Microelectronic Engineering **77,** 48-54 (2005).

[130] K. Hyojune and H. Hyunsang, Applied Physics Letters **74,** 709-710 (1999).

[131] J. G. E. Jellison and F. A. Modine, Applied Physics Letters **69,** 371-373 (1996).

[132] P. Bailey, T. C. Q. Noakes, and D. P. Woodruff, Surface Science **426,** 358-372 (1999).

[133] S. M. Sze, *Semiconductor Devices: Physics and Technology, 2nd Edition* (Wiley, New York, 2001).

[134] F.-C. Chiu, Journal of Applied Physics **100,** 114102 (2006).

[135] Z. Xu, M. Houssa, S. D. Gendt, and M. Heyns, Applied Physics Letters **80,** 1975-1977 (2002).

[136] J. Frenkel, Physical Review **54,** 647 (1938).

[137] A. Campera, G. Iannaccone, and F. Crupi, Electron Devices, IEEE Transactions on **54,** 83-89 (2007).

[138] A. A. Dakhel, Crystal Research and Technology **38,** 968-973 (2003).

[139] D. S. Jeong and C. S. Hwang, Journal of Applied Physics **98,** 113701 (2005).

[140] W. J. Zhu, T.-P. Ma, T. Tamagawa, J. Kim, and Y. Di, Electron Device Letters, IEEE **23,** 97-99 (2002).

[141] D. S. Jeong, H. B. Park, and C. S. Hwang, Applied Physics Letters **86,** 072903 (2005).

[142] A. K. Jonscher, Journal of Physics C: Solid State Physics, 1331 (1971).

[143] J. R. Yeargan and H. L. Taylor, Journal of Applied Physics **39,** 5600-5604 (1968).

[144] A. K. Jonscher, Thin Solid Films **1,** 213-234 (1967).

[145] L. M. Terman, Solid-State Electronics **5,** 285-299 (1962).

[146] K. Lehovec, A. Slobodskoy, and J. L. Sprague, Physical Status Solids **3,** 447 (1963).

[147] A. S. Grove, B. E. Deal, E. H. Snow, and G. T. Sah, Solid-State Electronics **8,** 145 (1965).

[148] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*, Wiley Classic Library ed. (John Wiley & Sons, Inc., New Jersey, 2003).

[149] W. Shockley, Bell System Technical Journal **28,** 435 (1949).

[150] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, IEEE Electron Device Letters **18,** 209-211 (1997).

[151] W. K. Henson, K. Z. Ahmed, E. M. Vogel, J. R. Hauser, J. J. Wortman, R. D. Venables, M. Xu, and D. Venables, Electron Device Letters, IEEE **20,** 179-181 (1999).

[152] K. Ahmed, E. Ibok, G. Bains, D. Chi, B. Ogle, J. J. Wortman, and J. R. Hauser, Electron Devices, IEEE Transactions on **47,** 1349-1354 (2000).

[153] C. L. Huang, J. V. Faricelli, and N. D. Arora, IEEE Transactions on Electron Devices **40,** 1134-1139 (1993).

[154] A. Koukab, A. Bath, and E. Losson, Solid-State Electronics **41,** 635-641 (1997).

[155] J. R. Hauser and K. Ahmed, in *Characterization of ultra-thin oxides using electrical C-V and I-V measurements*, Gaithersburg, Maryland (USA), 1998 (AIP), p. 235-239.

[156] N. Yang, W. K. Henson, J. R. Hauser, and J. J. Wortman, Electron Devices, IEEE Transactions on **46,** 1464-1471 (1999).

[157] R. Clerc, A. S. Spinelli, G. Ghibaudo, C. Leroux, and G. Pananakakis, Microelectronics Reliability **41,** 1027-1030 (2001).

[158] F. Li, L. F. Register, M. M. Hasan, and S. K. Banerjee, Electron Devices, IEEE Transactions on **53,** 2118-2127 (2006).

[159] K. J. Yang and H. Chenming, Electron Devices, IEEE Transactions on **46,** 1500 (1999).

[160] L. Zhijiong and T. P. Ma, Electron Device Letters, IEEE **25,** 655-657 (2004).

[161] C.-H. Choi, Y. Wu, J.-S. Goo, Z. Yu, and R. W. Dutton, Electron Devices, IEEE Transactions on **47,** 1843-1850 (2000).

[162] K. S. K. Kwa, S. Chattopadhyay, N. D. Jankovic, S. H. Olsen, L. S. Driscoll, and A. G. O'Neill, Semiconductor Science and Technology **18,** 82 (2003).

[163] J. L. Zhang, J. S. Yuan, Y. Ma, and A. S. Oates, Solid-State Electronics **45,** 373-377 (2001).

[164] S. V. Elshocht, P. Lehnen, B. Seitzinger, A. Abrutis, C. Adelmann, B. Brijs, M. Caymax, T. Conard, S. D. Gendt, A. Franquet, C. Lohe, M. Lukosius, A. Moussa, O. Richard, P. Williams, T. Witters, P. Zimmerman, and M. Heyns, Journal of The Electrochemical Society **153,** F219-F224 (2006).

[165] T.-M. Pan, J.-D. Lee, and W.-W. Yeh, Journal of Applied Physics **101,** 024110 (2007).

[166] H. Harris, K. Choi, N. Mehta, A. Chandolu, N. Biswas, G. Kipshidze, S. Nikishin, S. Gangopadhyay, and H. Temkin, Applied Physics Letters **81,** 1065-1067 (2002).

[167] V. Venkatesan, K. Das, J. A. v. Windheim, and M. W. Geis, Applied Physics Letters **63,** 1065-1067 (1993).

[168] M. Depas, R. Degraeve, T. Nigam, G. Groeseneken, and M. Heyns, Jpn. J. Appl. Phys. **36,** 1602-1608 (1997).

[169] R. Clerc, B. De Salvo, G. Ghibaudo, G. Reimbold, and G. Pananakakis, Solid-State Electronics **46,** 407-416 (2002).

[170] H. Packard, in *4192A LF Impedance Analyzer Operating and Service Manual* (2000).

[171] H.-T. Lue, C.-Y. Liu, and T.-Y. Tseng, Electron Device Letters, IEEE **23,** 553-555 (2002).

[172] A. Nara, N. Yasuda, H. Satake, and A. Toriumi, Semiconductor Manufacturing, IEEE Transactions on **15,** 209-213 (2002).

[173] C. T. Dervos, Thirios, J. Novacovich, P. Vassiliou, and P. Skafidas, Materials Letters **58,** 1502-1507 (2004).

[174] B. Lee, T. Moon, T.-G. Kim, D.-K. Choi, and B. Park, Applied Physics Letters **87,** 012901 (2005).

[175] A. K. Jonscher, Journal of Physics D: Applied Physics, R57 (1999).

[176] H. Choosuwan, R. Guo, A. S. Bhalla, and U. Balachandran, Journal of Applied Physics **93,** 2876-2879 (2003).

[177] A. C. Jones, H. C. Aspinall, P. R. Chalker, R. J. Potter, T. D. Manning, Y. F. Loo, R. O'Kane, J. M. Gaskell, and L. M. Smith, Chemical Vapor Deposition **12,** 83-98 (2006).

[178] M. H. Cho, Y. S. Roh, C. N. Whang, K. Jeong, S. W. Nahm, D. H. Ko, J. H. Lee, N. I. Lee, and K. Fujihara, Applied Physics Letters **81,** 472-474 (2002).

[179] L. Manchanda, M. D. Morris, M. L. Green, R. B. van Dover, F. Klemens, T. W. Sorsch, P. J. Silverman, G. Wilk, B. Busch, and S. Aravamudhan, Microelectronic Engineering **59,** 351-359 (2001).

[180] C. F. Powell, *Chemically Deposited Nonmetals* (John Wiley & Sons Inc., New York, 1966).

[181] G. Scarel, S. Spiga, C. Wiemer, G. Tallarida, S. Ferrari, and M. Fanciulli, Materials Science and Engineering B **109,** 11-16 (2004).

[182] K. Kukli, M. Ritala, T. Sajavaara, J. Keinonen, and M. Leskela, Thin Solid Films **416,** 72-79 (2002).

[183] E. P. Gusev, C. Cabral, M. Copel, C. D'Emic, and M. Gribelyuk, Microelectronic Engineering **69,** 145-151 (2003).

[184] J. J. Ganem, I. Trimaille, I. C. Vickridge, D. Blin, and F. Martin, Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms **219-220,** 856-861 (2004).

[185] H. B. Park, M. Cho, J. Park, S. W. Lee, C. S. Hwang, J.-P. Kim, J.-H. Lee, N.-I. Lee, H.-K. Kang, J.-C. Lee, and S.-J. Oh, Journal of Applied Physics **94,** 3641-3647 (2003).

[186] D. M. Hausmann, E. Kim, J. Becker, and R. G. Gordon, Chem. Mater. **14,** 4350-4358 (2002).

[187] D. G. Colombo, D. C. Gilmer, V. G. Young, S. A. Campbell, and W. L. Gladfelter, Chemical Vapor Deposition **04,** 220-222 (1998).

[188] K. Kukli, M. Ritala, T. Sajavaara, J. Keinonen, and M. Leskelä, Chemical Vapor Deposition **8,** 199-204 (2002).

189 S. Yoshihide, P. Seung, C. Hood, B. Lawrence, and N. Wesley, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films **22,** 1175-1181 (2004).

190 H. T. Dina, I. H. Rama, Bruce E. White, Jr., and J. T. Philip, Journal of Applied Physics **97,** 124107 (2005).

191 M. Balog, M. Schieber, M. Michman, and S. Patai, Journal of The Electrochemical Society **126,** 1203-1207 (1979).

192 S. V. Pasko, L. G. Hubert-Pfalzgraf, A. Abrutis, P. Richard, A. Bartasyte, and V. Kazlauskiene, Journal of Materials Chemistry **14,** 1245-1251 (2004).

193 R. C. Smith, T. Ma, N. Hoilien, L. Y. Tsung, M. J. Bevan, L. Colombo, J. Roberts, S. A. Campbell, and W. L. Gladfelter, Advanced Materials for Optics and Electronics **10,** 105-114 (2000).

194 E. P. Gusev, E. Cartier, D. A. Buchanan, M. Gribelyuk, M. Copel, H. Okorn-Schmidt, and C. D'Emic, Microelectronic Engineering **59,** 341-349 (2001).

195 J. J. Gallegos, T. L. Ward, T. J. Boyle, M. A. Rodriguez, and L. P. Francisco, Chemical Vapor Deposition **6,** 21-26 (2000).

196 K. P. Bastos, J. Morais, L. Miotti, R. P. Pezzi, G. V. Soares, I. J. R. Baumvol, R. I. Hegde, H. H. Tseng, and P. J. Tobin, Applied Physics Letters **81,** 1669-1671 (2002).

197 S. J. Lee, T. S. Jeon, D. L. Kwong, and R. Clark, Journal of Applied Physics **92,** 2807-2809 (2002).

198 D. C. Bradley, Chem. Rev. **89,** 1317-1322 (1989).

199 P. A. Williams, J. L. Roberts, A. C. Jones, P. R. Chalker, N. L. Tobin, J. F. Bickley, H. O. Davies, L. M. Smith, and T. J. Leedham, Chemical Vapor Deposition **8,** 163-170 (2002).

200 J. Niinistö, M. Putkonen, L. Niinistö, S. L. Stoll, K. Kukli, T. Sajavaara, M. Ritala, and M. Leskelä, J. Mater. Chem. **15,** 2271-2275 (2005).

[201] K. Forsgren, A. Harsta, J. Aarik, A. Aidla, J. Westlinder, and J. Olsson, Journal of The Electrochemical Society **149,** F139-F144 (2002).

[202] K. Kukli, M. Ritala, M. Leskelä, T. Sajavaara, J. Keinonen, A. C. Jones, and N. L. Tobin, Chemical Vapor Deposition **10,** 91-96 (2004).

[203] Y. S. Lin, R. Puthenkovilakam, and J. P. Chang, Applied Physics Letters **81,** 2041-2043 (2002).

[204] Y. Senzaki, S. Park, H. Chatham, L. Bartholomew, and W. Nieveen, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films **22,** 1175-1181 (2004).

[205] K. Kukli, M. Ritala, M. Leskelä, T. Sajavaara, J. Keinonen, A. C. Jones, and J. L. Roberts, Chemical Vapor Deposition **9,** 315-320 (2003).

[206] B. S. Lim, A. Rahtu, P. D. Rouffignac, and R. G. Gordon, Applied Physics Letters **84,** 3957-3959 (2004).

[207] P. de Rouffignac and R. G. Gordon, Chemical Vapor Deposition **12,** 152-157 (2006).

[208] Y. F. Loo, S. Taylor, R. T. Murray, A. C. Jones, and P. R. Chalker, Journal of Applied Physics **99,** 103704 (2006).

[209] H. Kim, P. C. McIntyre, and K. C. Saraswat, Applied Physics Letters **82,** 106-108 (2003).

[210] L. Zhong, W. L. Daniel, Z. Zhang, S. A. Campbell, and W. L. Gladfelter, Chemical Vapor Deposition **12,** 143-150 (2006).

[211] J. Zhu, Y. R. Li, and Z. G. Liu, Journal of Physics D: Applied Physics **37,** 2896 (2004).

[212] K. L. Ng, N. Zhan, C. W. Kok, M. C. Poon, and H. Wong, Microelectronics Reliability **43,** 1289-1293 (2003).

[213] O. Buiu, Y. Lu, I. Z. Mitrovic, S. Hall, P. Chalker, and R. J. Potter, Thin Solid Films **515,** 623-626 (2006).

214 Y. J. Cho, N. V. Nguyen, C. A. Richter, J. R. Ehrstein, B. H. Lee, and J. C. Lee, Applied Physics Letters **80,** 1249 (2002).

215 H. Takeuchi, D. Ha, and T.-J. King, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films **22,** 1337 (2004).

216 S. Maikap, J.-H. Lee, R. Mahapatra, S. Pal, Y. S. No, W.-K. Choi, S. K. Ray, and D.-Y. Kim, Solid-State Electronics **49,** 524 (2005).

217 S.-W. Nam, J.-H. Yoo, S. Nam, H.-J. Choi, D. Lee, D.-H. Ko, J. H. Moon, J.-H. Ku, and S. Choi, Journal of Non-Crystalline Solids **303,** 139-143 (2002).

218 I. Z. Mitrovic, Y. Lu, O. Buiu, and S. Hall, Microelectronic Engineering **84,** 2306-2309 (2007).

219 S. Jeon, K. Im, H. Yang, H. Lee, H. Sim, S. Choi, T. Jang, and H. Hwang, International Electron Devices Meeting (IEDM), 20.6.1-20.6.4 (2001).

220 T. Gougousi, D. Niu, R. W. Ashcraft, and G. N. Parsons, Applied Physics Letters **83,** 3543-3545 (2003).

221 M. Nieminen, M. Putkonen, and L. Niinisto, Applied Surface Science **174,** 155-166 (2001).

222 H. C. Aspinall, J. M. Gaskell, Y. F. Loo, A. C. Jones, P. R. Chalker, R. J. Potter, L. M. Smith, and G. W. Critchlow, Chemical Vapor Deposition **10,** 301-305 (2004).

223 Y. F. Loo, R. J. Potter, A. C. Jones, H. C. Aspinall, J. M. Gaskell, P. R. Chalker, L. M. Smith, and G. W. Critchlow, Chemical Vapor Deposition **10,** 306-310 (2004).

224 B. J. Kennedy, C. J. Howard, A. K. Prodjosantoso, and B. C. Chakoumakos, Applied Physics A: Materials Science & Processing **74,** s1660-s1663 (2002).

225 M. J. Jackson and W. O'Neill, Journal of Materials Processing Technology **142,** 517-525 (2003).

[226] B. Jancar, D. Suvorov, M. Valant, and G. Drazic, Journal of the European Ceramic Society **23,** 1391-1400 (2003).

[227] W. T. Fu and D. J. W. Ijdo, Journal of Solid State Chemistry **177,** 2973-2976 (2004).

[228] S. Cizauskaite, V. Reichlova, G. Nenartaviciene, A. Beganskiene, J. Pinkas, and A. Kareiva, Materials Chemistry and Physics **102,** 105-110 (2007).

[229] C. M. Carlson, J. C. Price, P. A. Parilla, D. S. Ginley, D. Niles, R. D. Blaugher, A. Goyal, M. Paranthaman, D. M. Kroeger, and D. K. Christen, Physica C: Superconductivity **304,** 82-88 (1998).

[230] A. A. Molodyk, I. E. Korsakov, M. A. Novojilov, I. E. Graboy, A. R. Kaul, and G. Wahl, Chemical Vapor Deposition **6,** 133-138 (2000).

[231] G. Malandrino, I. L. Fragala, and P. Scardi, Chem. Mater. **10,** 3765-3768 (1998).

[232] L. Yan, H. B. Lu, G. T. Tan, F. Chen, Y. L. Zhou, G. Z. Yang, W. Liu, and Z. H. Chen, Applied Physics A: Materials Science & Processing **77,** 721-724 (2003).

[233] L. F. Edge, D. G. Schlom, R. T. Brewer, Y. J. Chabal, J. R. Williams, S. A. Chambers, C. Hinkle, G. Lucovsky, Y. Yang, S. Stemmer, M. Copel, B. Hollander, and J. Schubert, Applied Physics Letters **84,** 4629-4631 (2004).

[234] K. Kukli, M. Ritala, V. Pore, M. Leskelä, T. Sajavaara, R. I. Hegde, D. C. Gilmer, P. J. Tobin, A. C. Jones, and H. C. Aspinall, Chemical Vapor Deposition **12,** 158-164 (2006).

[235] M. Nieminen, T. Sajavaara, E. Rauhala, M. Putkonen, and L. Niinistö, Journal of Materials Chemistry **11,** 2340 (2001).

[236] G. Vellianitis, G. Apostolopoulos, G. Mavrou, K. Argyropoulos, A. Dimoulas, J. C. Hooker, T. Conard, and M. Butcher, Materials Science and Engineering B **109,** 85-88 (2004).

[237] B.-E. Park and H. Ishiwara, Applied Physics Letters **82,** 1197-1199 (2003).

[238] J. S. Schweitzer, Nuclear Science, IEEE Transactions on **38,** 497-500 (1991).

[239] G. Suresh, G. Seenivasan, M. V. Krishnaiah, and P. Srirama Murti, Journal of Nuclear Materials **249,** 259-261 (1997).

[240] S. Chevalier, G. Bonnet, and J. P. Larpin, Applied Surface Science **167,** 125-133 (2000).

[241] B. M. Tissue, Chem. Mater. **10,** 2837-2845 (1998).

[242] A. A. Dakhel, physica status solidi (a) **201,** 745-755 (2004).

[243] V. S. Dharmadhikari and A. Goswami, Thin Solid Films **87,** 119-126 (1982).

[244] V. S. Dharmadhikari, Thin Solid Films **103,** 311-317 (1983).

[245] M. D. Kannan, S. K. Narayandass, C. Balasubramanian, and D. Mangalaraj, Journal of Materials Science **27,** 5040-5044 (1992).

[246] D. Xue, K. Betzler, and H. Hesse, Journal of Physics: Condensed Matter **12,** 3113 (2000).

[247] E. A. Nenasheva, L. P. Mudroliubova, and N. F. Kartenko, Journal of the European Ceramic Society **23,** 2443-2448 (2003).

[248] C. Brugnoni, U. Ducati, C. Chemelli, M. Scagliotti, and G. Chiodelli, Solid State Ionics **76,** 183-188 (1995).

[249] M. R. Rao, Thin Solid Films **306,** 141-146 (1997).

[250] S. Mathur, M. Veith, H. Shen, N. Lecerf, and S. Hufner, Scripta Materialia **44,** 2105-2109 (2001).

[251] K. Arai, H. Namikawa, K. Kumata, Y. Ishii, H. Tanaka, and I. Iida, Japanese Journal of Applied Physics **22,** L397-L399 (1983).

[252] A. Ikesue, T. Kinoshita, K. Kamata, and K. Yoshida, Journal of the American Ceramic Society **78,** 1033-1040 (1995).

[253] M. Veith, S. Mathur, N. Lecerf, K. Bartz, M. Heintz, and V. Huch, Chem. Mater. **12,** 271-274 (2000).

254 M. Veith, S. Mathur, H. Shen, N. Lecerf, S. Hufner, and M. H. Jilavi, Chem. Mater. **13,** 4041-4052 (2001).

255 S. Mathur, M. Veith, H. Shen, S. Hufner, and M. H. Jilavi, Chem. Mater. **14,** 568-582 (2002).

256 C.-C. Cheng, C.-H. Chien, C.-W. Chen, S.-L. Hsu, M.-Y. Yang, C.-C. Huang, F.-L. Yang, and C.-Y. Chang, Microelectronic Engineering **80,** 30-33 (2005).

257 J. A. Ng, Y. Kuroki, N. Sugii, K. Kakushima, S. I. Ohmi, K. Tsutsui, T. Hattori, H. Iwai, and H. Wong, Microelectronic Engineering **80,** 206-209 (2005).

258 E. Rauwel, C. Dubourdieu, B. Hollander, N. Rochat, F. Ducroquet, M. D. Rossell, G. V. Tendeloo, and B. Pelissier, Applied Physics Letters **89,** 012902 (2006).

259 S.-H. Kim and S. W. Rhee, Chemical Vapor Deposition **12,** 125-129 (2006).

260 S. Govindarajan, T. S. Boscke, P. Sivasubramani, P. D. Kirsch, B. H. Lee, H. H. Tseng, R. Jammy, U. Schroder, S. Ramanathan, and B. E. Gnade, Applied Physics Letters **91,** 062906 (2007).

261 M. A. Quevedo-Lopez, S. A. Krishnan, P. D. Kirsch, G. Pant, B. E. Gnade, and R. M. Wallace, Applied Physics Letters **87,** 262902 (2005).

262 J. Wang, H. P. Li, and R. Stevens, Journal of Materials Science **27,** 5397-5430 (1992).

263 T. S. Boscke, S. Govindarajan, P. D. Kirsch, P. Y. Hung, C. Krug, B. H. Lee, J. Heitmann, U. Schroder, G. Pant, B. E. Gnade, and W. H. Krautschneider, Applied Physics Letters **91,** 072902 (2007).

264 X. Zhao and D. Vanderbilt, Physical Review B **65,** 233106 (2002).

265 L. A. K. Dominik and R. K. MacCrone, Physical Review **156,** 910 (1967).

[266] W. Jie, X. G. Tang, H. L. W. Chan, C. L. Choy, and L. Haosu, Applied Physics Letters **86,** 152907 (2005).