Leveraging CMOS Aging for Efficient Microelectronics Design

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***Abstract*—Aging is known to impact electronic systems affecting performance and reliability. However, it has been shown that it also brings benefits for power saving and area optimization. This paper presents highlights of those benefits and further shows how aging effects can be leveraged by novel methods to contribute towards improving hardware oriented security and reliability of electronic circuits. We have demonstrated static power reduction in complex circuits from IWLS05 benchmark suite, reaching a noticeable 78% of reduction in ten years of operation. In hardware oriented security, a novel aging sensor has been proposed for detection of recycled ICs, measuring discharge time τ_{dv} of the virtual power (VV_{dd}) network in power-gated designs. This sensor utilizes discharge time of VV_{dd} network through leakage current that is much more sensitive to aging than path delay, exhibiting up to 15.7X increment in 10 years. Furthermore, we show how frequency degradation caused by aging is used for online prediction of remaining useful lifetime (RUL) of electronic circuits. Results show an average RUL prediction deviation of less than 0.1 years. This methodology provides node calculations rather than a mean time to failure (MTTF) of the population. The set of techniques that are presented in this paper takes advantage of aging effects, having a positive impact in various aspects of microelectronic systems.**

Keywords— aging, IC recycling, remaining useful lifetime, machine learning, online prediction, sustainable digital society.

I. INTRODUCTION

Microelectronics designs suffer from reliability reduction due to aging effects, which impact negatively the circuit performance. Previous publications have identified bias temperature instability (BTI) and hot carrier injection (HCI) as main aging effects [1], [2]. Recent studies have demonstrated that BTI aging, together with detrimental effects for reliability and performance, also brings benefits such as reduction in power consumption. As a result, CMOS designs become more energy efficient over time, and this beneficial effect is expected to increase for more scaled technologies [3], [4].

In [4], aging benefits for complex circuits are demonstrated, with optimization of power consumption due to sub-threshold leakage current reduction. Furthermore, [3] exploits this effect by optimizing sleep transistors (STs) for power gated circuits, achieving noticeable beneficial effects for static power and ST switching efficiency by optimizing I_{ON} and I_{OFF} (I_{leak}) ratio, where I_{ON} decreases almost linearly with the increase of ST threshold voltage, whilst I_{OFF} decreases exponentially.

Aging effects can also be used for the detection of recycled ICs [5]-[8], whose counterfeiting as new components can create life threatening scenarios when incorporated in real-time safety critical systems [9]. This phenomenon represents a major concern for electronic industry, since about 80% of total counterfeits are due to recycled and remarked ICs [9], [10]. Many techniques for detection of recycled ICs use monitoring of performance degradation, including path delay and ring oscillator frequency, whose degradations are both due to the linear decrease in active current induced by BTI [5]-[8], [11], [12]. In [13], authors proposed a novel technique using the discharge time of virtual power network in power-gated circuits as a metric to identify recycled ICs. It is based on monitoring of the discharge time increase over time, which is due to the exponential reduction of leakage current induced by BTI degradation of transistor threshold voltage (ΔV_{th}). This exponential dependency of discharge time on ΔV_{th} is a novel metric, which is much more sensitive to aging than path delay or RO frequency.

Our current work on remaining useful lifetime (RUL) estimation further exploits aging effects by proposing a machine learning based online methodology to accurately predict RUL, by monitoring frequency degradation over design's lifetime, whilst factoring in temperature and voltage variations. For a population of microelectronic designs, RUL methodology provides individual time to failure estimation rather than a coarse number generated by mean time to failure (MTTF) model, which estimates the whole population using a single value. This per node RUL estimation is not only beneficial for improving reliability, but can also be used to generate prognostics data for the whole population, and thereby support subsequent design cycles. Moreover, this novel RUL estimation along with existing studies using aging effects [3], [4], [13] are foreseen to ultimately contribute towards reduction in e-waste, and further support sustainable digital society and similar green computing initiatives [14], [15]. For example, by supporting a legal trading framework for CMOS designs by exploiting online RUL estimation method.

II. RESULTS

A. Power reduction

Static power consumption (P_{st}) in aggressively scaled CMOS designs is playing an increasingly bigger role in determining the overall power consumption. It is caused by leakage current flowing from V_{dd} to ground, when a circuit is idle. Leakage current presents two main contributors, sub-

threshold current and gate current, with the former being the dominant due to the control that can be achieved in gate current by using high-k dielectrics. Thus, $P_{st} = V_{dd}\, I_{leak}$ can be expressed as [12]:

$$P_{st} \simeq V_{dd}\mu C_{ox}\frac{W}{L}\left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{gs}-V_{th})}{nkT}}\left(1-e^{\frac{-qV_{ds}}{kT}}\right) \quad (1)$$

where C_{ox} is the dielectric capacitance, W and L are the MOS transistor channel width and length, respectively, q is the electron charge, k the Boltzmann constant, T the temperature, and n a parameter that depends on device fabrication. The increment of threshold voltage (V_{th}) caused by BTI [1], [16] causes static power reduction, confirmed by HSPICE simulation and experimental measurements [4]. Fig. 1 shows the trend over time of P_{st} for 10 cascaded inverters implemented with a 32nm Metal Gate, High-K CMOS technology [4] and different aging temperatures. As can be seen, after only 1 month of operation, P_{st} reduction is well above 40% for all three aging temperatures (T_A), exceeding 60% for T_A = 100°C. It further increases up to 58%-71% after 1 year and, after 10 years of operation, P_{st} reduction is in the range of 70%-81%.

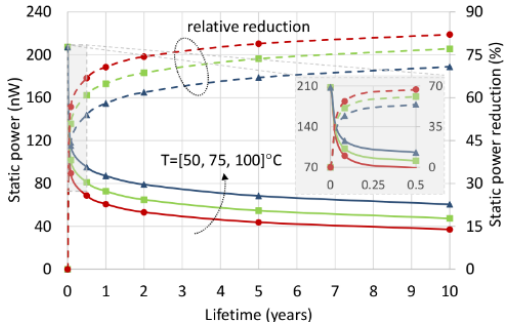


Fig. 1 Trend over time of the static power (P_{st}) for different temperatures (solid lines) and relative reduction over the static power at t=0 [4].

In [4], this aging benefits to static power is assessed for several circuits from IWLS05 benchmark suite. Table I show obtained results, where second column present values of P_{st} exhibited at *t0* for each circuit (used as normalization factor). These results confirm the trends shown in Fig. 1.

TABLE I. STATIC POWER REDUCTION OVER TIME (T_A=75°C) [4]

Circuit	P_{st0} (μW)	Reduction (%)					
		1m	6m	1y	2y	5y	10y
c499	1.198	53.09	62.86	66.85	70.67	75.51	78.94
c1355	1.443	50.45	60.63	64.63	68.50	73.46	77.01
c6288	6.386	54.36	62.90	66.92	70.78	75.67	79.14
c7552	11.30	52.41	62.53	66.51	70.34	75.20	78.65
s38418	85.39	52.07	62.16	66.15	69.99	74.88	78.36
b18	358.8	50.71	60.87	64.88	68.74	73.68	77.23
b20	61.49	50.50	60.69	64.68	68.53	73.45	76.99
Average	75.15	52.15	61.95	65.95	69.79	74.69	78.17

B. Hardware oriented security benefits

A novel technique is presented in [13] to detect recycled ICs. It specifically targets circuits adopting power gating to reduce static power and meet tight energy constraints in applications like autonomous systems, Internet of Things, etc. Nevertheless, this technique can be easily extended to ICs that do not implement any power saving technique.

The proposed technique measures discharge time τ_{dv} of the virtual power network, which occurs through the leakage current of the power-gated circuit. Since BTI causes an increase in transistor V_{th}, and leakage current decreases exponentially, τ_{dv} augments noticeably over time [7], allowing the differentiation between recycled and new ICs.

When an IC operates, different devices may undergo different amount of stress and degradation, depending on their operating condition and switching activity. The proposed technique is based on a coarse-grained aging sensor targeting discharge time of a power-gated [8] core as an aging metric. Therefore, it is able to capture the average trend of aging, with no need to probe specific observation points in the system. The discharge time sensor, shown in Fig. 2, resides in the power-gating controller. It counts the clock rising edges n_c until the virtual voltage VV_{dd} drops to logic-0. The finite state machine (FSM) controls the sensor by asserting the measure signal together with the sleep signal in order to collect the τ_{dV}^{meas} value when the sleep signal is asserted and the circuit is power-gated. The measured discharge time is $\tau_{dV}^{meas} = n_c \times T_{clk}$, where n_c is number of clock cycles, and T_{clk} is the circuit clock period [13].

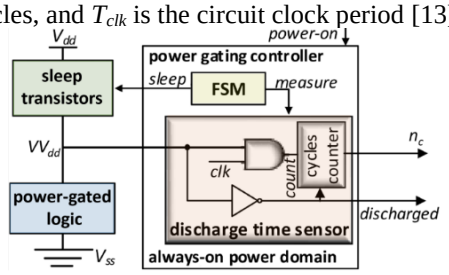


Fig. 2.Power network discharge time sensor architecture [13].

As an example, the HSPICE simulation of a power-gated circuit consisting of 21 cascaded inverters and its power distribution network were synthesized with a 32nm CMOS technology [13]. Fig. 3, shows that path delay (τ_{pd}) increases less than 6% after a month of operation, 22% after a year, and up to 1.43X after 10 years of operation. Conversely, the discharge time τ_{dV} exhibits an increase, exceeding 2X after a month of operation, 5.4X after a year, and escalating up to 15.7X in 10 years. Compared with the traditional path delay monitoring methods, the technique in [13] provides a much higher confidence in recycled IC detection. Indeed, relative increase in discharge time is more than 4 order of magnitude greater than relative increase in path delay.

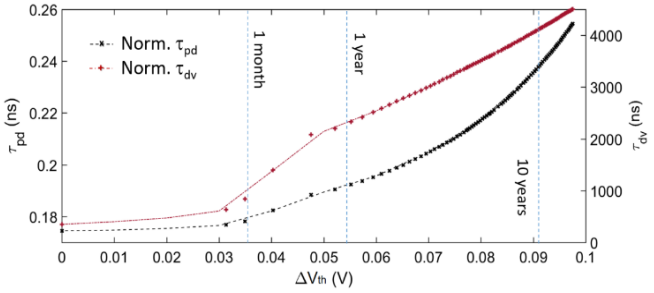


Fig. 3 Propagation delay (τ_{pd}) and discharge time (τ_{dv}) as a function of V_{th} degradation [13].

By means of mote Carlo simulation (Fig. 4), it is demonstrated that proposed discharge time sensor provides high confidence in detection of recycled ICs even when process variation is accounted for. A 15% threshold voltage variation, with a normal distribution is considered and 1000 instances of both the fresh and 1-month aged circuits[13]. The worst case temperature T = 100°C has been considered. The histograms report normalized results against the nominal value exhibited at *t0* (fresh circuit), $\tau_{dV0}^{nom} \cong 207.4$ns. As can be seen, the distribution for a fresh circuit is very narrow, with a worst case discharge time (highest value)

$\tau_{dV0} \cong 225.2$ns, which is approximately 10% higher than τ_{dV0}^{nom}. The aged distribution is much wider, since the threshold voltage shift due to BTI aging depends also on the initial threshold voltage. Nevertheless, in the worst case scenario for our technique (lowest discharge time), it is $\tau_{dV}^{1\,month} \cong 455.6\text{ns} \geq 2\text{x}\tau_{dV0}^{nom}$, which represents a margin of more than 230ns for our technique to distinguish between a fresh and an aged circuit that has been already operating for a month only.

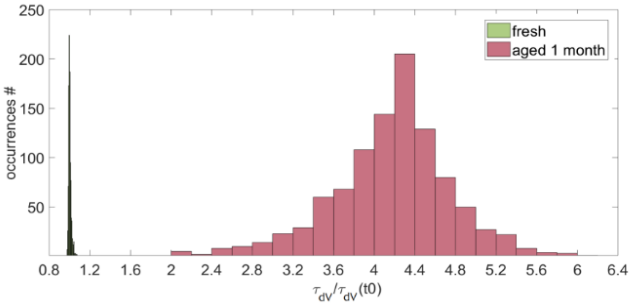


Fig. 4. Normalized distribution of τ_{dV} for fresh and 1-month aged circuits [13].

C. Online remaining useful lifetime

The remaining useful lifetime (RUL) of an integrated circuit is defined as the remaining time from its present condition to failure, which is crucial to ensure reliability and safety of microelectronic designs [17]. The proposed online RUL prediction methodology utilizes the output frequency degradation of a ring oscillator (RO), which is representative of the overall system degradation over lifetime. Considering that correct operating condition of RO is above a certain value (e.g. 20%) of frequency degradation that can be defined by the user according to the application. Fig. 5 presents frequency degradation trend of 13 and 21 stage RO when supply voltage is 0.9V, with four representative temperatures (25, 50, 75 and 100°C). These results show more than 18% frequency degradation in 5 years for all temperatures and close to 50% degradation in 20 years.

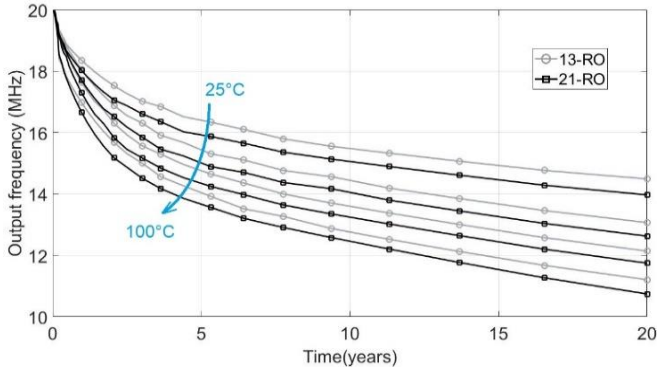


Fig. 5. Frequency degradation for 13-RO (grey) and 21-RO (black) with representative working temperatures 25 (upper curve), 50, 75 and 100 °C (lower curve).

To the best of our knowledge, this is the first study that calculates online RUL for CMOS designs. Previous studies have used RC electric components [18] and gate bipolar transistors (IGBT) [19] performing RUL calculation with neural networks that was shown to suffer from local minima [20].

Proposed technique utilizes 22-nm CMOS technology from GLOBALFOUNDRIES, and carries out detailed SPICE simulations using Cadence SPECTRE with appropriate CMOS aging models provided by GLOBALFOUNDRIES. The data generated by the ring oscillators are used to train a RUL predictor model through support vector regression (SVR), which is a machine learning algorithm chosen due to its capacity to handle local minima. In SVR algorithm, classification of training data is undertaken by calculation of three main parameters, namely Kernel scale, Box constraint and Epsilon. Kernel scale maps data into a higher-dimensional space in which they become separable; Box constraint has a direct impact on the weight of classification of data points, therefore it performs a stricter separation of the data if its value increases; finally, Epsilon affects the number of support vectors used to construct the regression function, with a bigger Epsilon value leading to fewer support vectors [21].

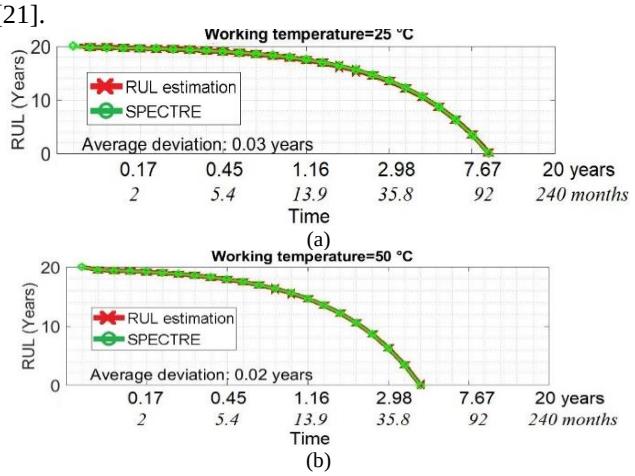
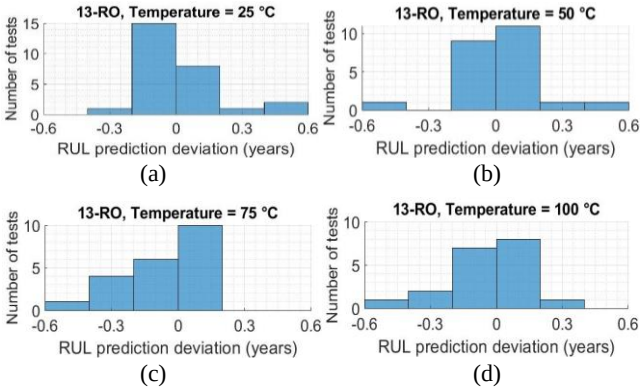


Fig. 6. RUL prediction results with SVR model at 25°C (a) and 50°C (b) for 13-RO, where the time increments according to $0.068e^{0.189*sample}$.

Fig. 6 shows an average online RUL prediction deviation, which is less than 0.1 years when using 13 stage ring oscillator. This demonstrates that RUL follows a clear trend, decreasing progressively as a function of CMOS technology degradation during lifetime, and at higher rate when temperature increases.

More results on individual operating temperatures for each RO demonstrate the accuracy of proposed online RUL prediction methodology. Fig. 7 shows histograms of prediction deviation, where most cases are close to zero. This confirms that output frequency of the RO and temperature are effectively estimated using RUL prediction with the SVR model. In Fig. 7, first four graphs show results for 13 stage RO (a, b, c, d) and the last four for 21 stage RO (e, f, g, h), both tested with four representative temperatures (25, 50, 75, 100 ºC) to show individual RUL prediction deviation in years.



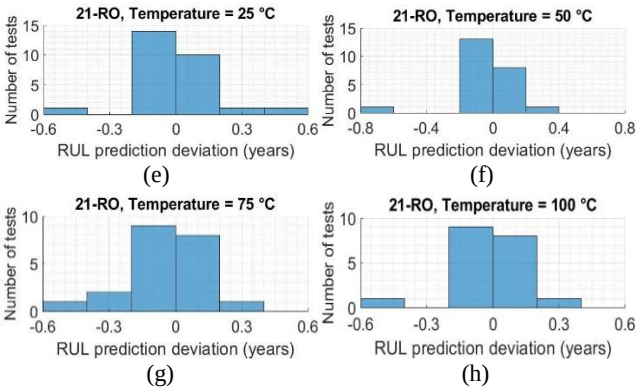


Fig. 7. Tests on individual SVR model for a set of representative temperatures (25, 50, 75, 100 ºC) that demonstrate accuracy of SVR-RUL predictor model for each ring oscillator, 13-RO (a, b, c, d) and 21-RO (e, f, g, h).

In all cases, individually tested SVRs for both ring oscillators demonstrated a high accuracy of RUL prediction. The numbers remain under ±0.8 years of deviation and most of them are close to 0% deviation. Each test results are based on a total of 30 samples taken during the lifetime (20 years) of each RO under specified temperature. The fact that predictions can be performed using signals from the ring oscillator demonstrate that this methodology is suitable in cases where devices work in different stress and operating conditions. Indeed, this demonstrates that RUL estimation may be used in any stage of a device lifetime.

This per node RUL estimation ability, can be used to provide reliability awareness of safety critical designs, and for improving reliability of subsequent design cycles by exploiting prognostics data from all designs. Moreover, this novel RUL estimation and existing studies on CMOS aging [3], [4], [13] will also contribute towards reducing e-waste, and in creation of sustainable digital societies of the future [14], [15].

III. Conclusion

This paper has demonstrated the beneficial effects of CMOS aging on microelectronics design, and how they are exploited in recently developed techniques to benefit a number of key challenges including area and energy efficiency, recycled ICs detection, and reliability.

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