Effect of High-k Passivation Layer on High Voltage Properties of GaN Metal-Insulator-Semiconductor Devices

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ABSTRACT In this paper, the GaN-based MIS-HEMTs with Si_3N_4 single-layer passivation, Al_2O_3/SiN_x bilayer passivation, and ZrO_2/SiN_x bilayer passivation are demonstrated. High-k dielectrics are adopted as the passivation layer on MIS-HEMTs to suppress the shallow traps on the GaN surface. Besides, high permittivity dielectrics passivated MIS-HEMTs also show an improved breakdown voltage characteristic, and that is explained by a 2-D simulation analysis. The fabricated devices with high-k dielectrics/SiN_x bilayer passivation exhibit higher power properties than the devices with plasma enhanced chemical vapor deposition-SiN_x single layer passivation, including smaller current collapse and higher breakdown voltage. The Al_2O_3/SiN_x passivated MIS-HEMTs exhibit a breakdown voltage of 979 V, and the dynamic R_{on} is only 1.14 times the static R_{on} after off-state V_{DS} stress of 150 V. On the other hand, the ZrO_2/SiN_x passivated MIS-HEMTs exhibit a higher breakdown voltage of 1170 V, and the dynamic R_{on} is 1.25 times the static R_{on} after off-state V_{DS} stress of 150 V.

INDEX TERMS Keywords — AlGaN/GaN, MIS-HEMTs, Si_3N_4, high-k, Al_2O_3, ZrO_2, current collapse, dynamic on-resistance, breakdown voltage.

I. INTRODUCTION

GaN-based metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) are expected to be applied in high voltage switching systems, due to their superior characteristics of high critical breakdown field (~3.5 MV/cm), large saturation velocity (~ $2.5x10^7$ cm^2/s), and high electron mobility (~1500 $cm^2/V/s$) [1]. However, despite promising high power properties of GaN-based devices, the reliability issues induced by passivation layer under high electric field and dynamic switching are still a major concern. Most of the conventional passivation materials on MIS-HEMTs are SiO_2 or SiN_x with relatively low relative permittivity (ε_r < 7), wide band gap (E_G > 5 eV) and high critical breakdown field (E_f ~ 20 MV/cm) [2, 3]. The low-pressure chemical vapor deposition (LPCVD) of SiN_x, has been investigated as the passivation of GaN-based MIS-HEMTs to exhibit decent properties (especially in dielectric breakdown and SiN_x/GaN interface) [3]. However, the degradation of ohmic contact electrodes may be occurred during the high temperature (> 650 ℃) deposition process. The plasma enhanced chemical vapor deposition (PECVD) of SiN_x grown with a faster deposition rate at a lower temperature of ~350 ℃ has also long been a common passivation layer for GaN-based MIS-HEMTs [4]. However, the exposure of GaN surface to the plasma in the PECVD process may cause the degradation of SiN_x/GaN interface, resulting in increased density interface states and leakage currents [5]. The high-k materials deposited by thermal atomic layer deposition (ALD) have been commonly researched as the gate dielectric on GaN-based MIS-HEMTs, for example, Al_2O_3 (the relative permittivity ε_r = ~9) [6], HfO_2 (ε_r = ~20) [7], ZrO_2 (ε_r = ~30) [8], and TiO_2 (ε_r = ~55) [9]. Those dielectrics possessed excellent characteristics, such as free of plasma-induced damage, high film qualities, and low deposition temperature. The research of applying high-k dielectrics as the passivation layer on the GaN-based devices has recently begun. As one of the premier investigations on the high-k passivation, the reference [10] conducted a 2-D simulation analysis of breakdown characteristics in HEMTs as a function of ε_r of the passivation layer. This study found that the off-state breakdown voltage is enhanced when ε_r is high. After that, a similar numerical analysis has been performed in the reference [11], which also indicated the breakdown voltage

increased as ε_r increased. This points out that high-k dielectrics show great potential and advantages as a choice for the passivation layer on GaN-based MIS-HEMTs. Meanwhile, there have been few experimental researches reported the high-k passivation layers' effect on the high voltage properties of GaN-based MIS-HEMTs. In this study, the electrical properties of AlGaN/GaN MIS-HEMTs with different passivation layers will be investigated on the base of a preliminary study [12]. The high-k dielectrics, Al_2O_3 and ZrO_2 as the interlayer between GaN cap and PECVD-SiN_x passivation are considered. The devices with or without high-k dielectrics interlayer will be compared. Reduced dynamic on-resistance and improved breakdown voltage are simultaneously exhibited on the MIS-HEMTs with high-k dielectrics interlayer, indicating a potential of the proposed high voltage devices structure. Furthermore, a TCAD simulation of the electric field in MIS-HEMTs as functions of the relative permittivity of the passivation layer will be performed.

II. DEVICE FABRICATION

The investigated AlGaN/GaN heterostructure epitaxial structure included from top to bottom a 2 nm thick GaN cap layer, a 22 nm undoped $Al_{0.25}Ga_{0.75}N$ barrier, a 330 nm GaN channel layer and a 5.1 µm GaN buffer on a Si substrate. The fabrication processes were started from the mesa isolation. Specifically, the mesa isolated region was formed by BCl_3/Cl_2 inductive coupled plasma etching. Then, the Au-free ohmic contacts were formed with electron beam evaporation of Ti/Al/Ni/TiN (30/120/55/50 nm) metal stack and followed by rapid thermal annealing at 870 ℃ in N_2 ambient for 40 s. After organic cleaning processes and a 5 mins HCl surface treatment on the wafer, a 120 nm SiN_x was deposited as the passivation for sample A. An Al_2O_3/SiN_x bilayer passivation with thicknesses of 22/120 nm was deposited for sample B. A ZrO_2/SiN_x bilayer passivation with thicknesses of 22/120 nm was deposited for sample C.

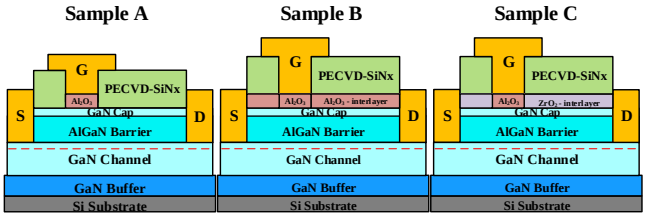


Fig. 1. Cross-sectional schematic view of the fabricated AlGaN/GaN MIS-HEMTs with a 120 nm SiN_x single-layer passivation (Sample A), a 22/120 nm Al_2O_3/SiN_x bilayer passivation (Sample B) and a 22/120 nm ZrO_2/SiN_x bilayer passivation (Sample C).

The thickness of dielectrics were measured by using spectroscopic ellipsometry. All the SiN_x was deposited by PECVD at 350 ℃ with a NH_3 flow of 10 sccm, a SiH_4 flow of 13.5 sccm and a N_2 flow of 1000 sccm. The ALD-Al_2O_3 layer was grown at 230 ℃ with a growth rate of 0.11 nm/cycle. H_2O and Trimethylaluminum (TMA) were used as precursors of oxygen and Al, respectively. The ALD-ZrO_2 layer was grown at 200 ℃ with a growth rate of 0.12 nm/cycle. H_2O and Tetrakis (ethylmethylamino) zirconium were used as precursors of oxygen and Zr, respectively. After the dielectrics deposition, the SiN_x layer in gate regions was removed by reactive ion etching, and the Al_2O_3 and ZrO_2 layers in gate regions were etched away by 2% HF solution. A 22 nm ALD-Al_2O_3 was then deposited as the gate dielectric for three samples. Lastly, Ni/TiN (50/100 nm) metal stack was evaporated as gate electrodes. A schematic cross-sectional view of the three groups of MIS-HEMTs is demonstrated in Fig.1. The fabricated MIS-HEMTs feature a fixed gate-source separation L_{SG} of 3 µm, gate length L_G of 3 µm, and gate-drain separation L_{GD} of 15 µm. The Keysight B1505A power device analyzer was used to measure the electrical properties.

III. RESULTS AND DISCUSSION

Transmission electron microscope (TEM) measurement has been carried out to investigate the cross-section images of the fabricated devices and the cross section TEM micrographs at the passivation region of each sample are shown in Fig. 2. It can be observed that the samples with the ALD dielectric interfacial layer exhibited a sharper passivation/barrier interface morphology.

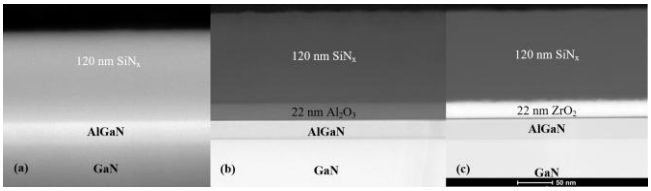


Fig. 2. Cross-sectional TEM micrographs at the passivation region of each sample (a) without and (b) with ALD-Al_2O_3 and (c) with ALD-ZrO_2 interfacial layer

The DC I_D-V_{GS} and I_G-V_{GS} curves of the three samples are plotted in Fig. 3. The transfer characteristics were measured by the gate voltage double-direction sweeping between -12 V and 6 V with a step of 100 m, and the drain bias was set as 10 V. The threshold voltage are extracted to be -9.6 V, -9.5 V and -9.5 V for the samples A, B and C, respectively, at a drain current criterion of 1 µA/mm. The samples A, B and C exhibit a low threshold hysteresis (ΔV_{th}) of ~109 mV, ~106 mV and ~99 mV, respectively, and the subthreshold slope (SS) of ~110 mV/dec, ~101 mV/dec and ~102 mV/dec, respectively. The electrostatics characteristics (e.g., ΔV_{th} and SS) are very similar for the three samples because the gate structures are identical for the three devices. Moreover, the I_{ON}/I_{OFF} ratios of the three samples are calculated to be larger than $1x10^{10}$. The devices B and C with a bilayer passivation are well pinched off at V_{GS} = -12 V with an off-state drain leakage current of ~100 pA/mm, indicating the interlayer would not induce the off-state leakage currents in associated with the leakage component through mesa isolation surface [13]. Note that the variation of the I_D-V_{DS} curves for the three samples has not been found obvious, hence the DC

output characteristics for the samples have been excluded from this paper.

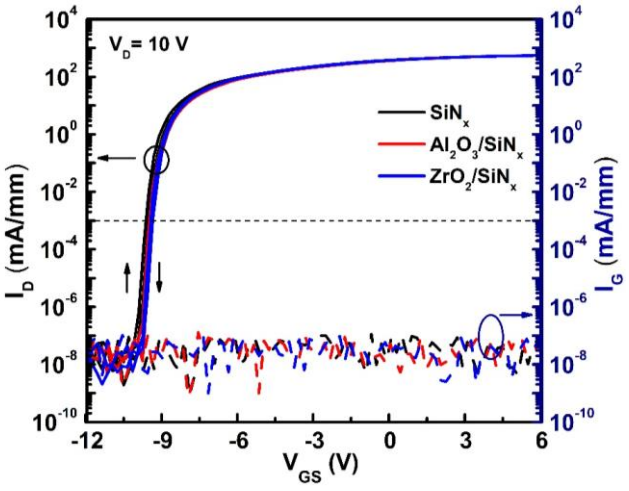
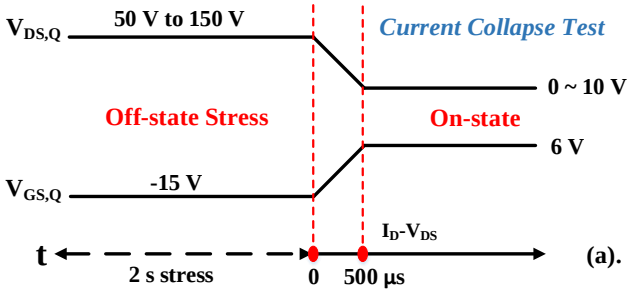


Fig. 3. I_D–V_{GS} and I_G-V_{GS} characteristics of the AlGaN/GaN MIS-HEMTs with PECVD-SiN_x passivation (in black lines), Al_2O_3/SiN_x passivation (in red lines) or ZrO_2/SiN_x passivation (in blue lines).

The dynamic on-state performance of the three samples was evaluated by using a pulsed I_D-V_{DS} measurement under fast switching with different quiescent bias points. The schematic timings of voltage signals in current collapse measurements are demonstrated in Fig. 4(a) [14]. At the off-state, quiescent gate bias ($V_{GS,\,Q}$) was fixed at -15 V and quiescent drain biases ($V_{DS,\,Q}$) were set as 50 V, 75 V, 100 V, 125 V and 150 V. The off-state stress time was 2 s. The pulsed output curves were measured at 500 µs after off-state voltage stresses. The ON-state was chosen to feature V_{GS} = 6 V. Fig. 4(b) shows the DC and pulsed I_D-V_{DS} curves of the three MIS-HEMTs. The DC I_D-V_{DS} curves before the stresses are used as references (solid lines in black). Effective suppression of the current collapse effect by the Al_2O_3/SiN_x passivation is demonstrated with a small difference between the DC and pulsed output curves. Compared with the PECVD-SiN_x passivation, the ALD-dielectrics/SiN_x shows an enhanced dynamic performance with $V_{DS,Q}$ higher than 50 V.



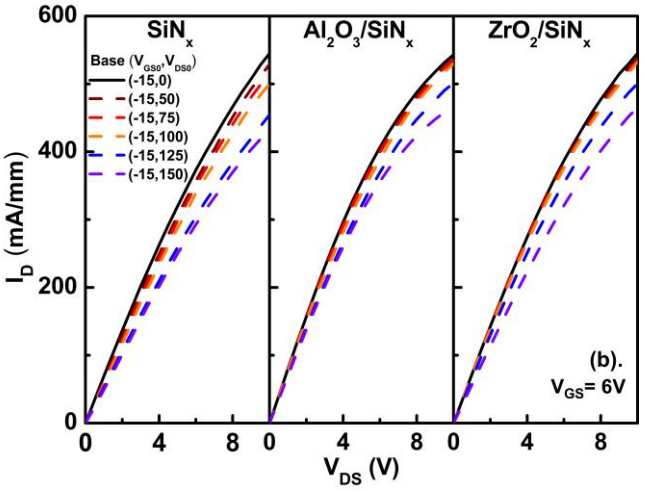


Fig. 4. (a) Parameters and timings setting in current collapse measurements. Pulsed I_D-V_{DS} curves were measured at 500 µs after removing the 2 s stress bias. (b) Behavior of pulsed I_D-V_{DS} curves of the AlGaN/GaN MIS-HEMTs with different passivation layers measured at different quiescent bias points.

The ratios of dynamic on-resistance ($R_{ON,D}/R_{ON,S}$) of three samples are extracted and plotted in Fig. 5. On-state resistance was extracted from the linear region of the output curve, and it was chosen to feature V_{GS} = 6 V and V_{DS} = 0.5 V. A sharp increase of the dynamic R_{on} is observed for the PECVD-SiN_x passivated MIS-HEMTs. Specifically, shown as the black line in Fig. 5, the dynamic R_{on} of the SiN_x is 1.36 times the static R_{on} when the off-state stress $V_{DS,Q}$ is higher than 150 V. By comparison, the dynamic R_{on} of the Al_2O_3/SiN_x and ZrO_2/SiN_x passivated devices are only 1.14 and 1.25 times the static R_{on} after off-state $V_{DS,Q}$ stress of 150 V, respectively. The results point out that the passivation layer with high quality ALD high-k layers could suppress the current collapse effectively. The more significant current collapse effect exhibited in the PECVD-SiN_x passivated sample is possibly caused by the plasma damage or failure to eliminate interface states between GaN and passivation [15, 16].

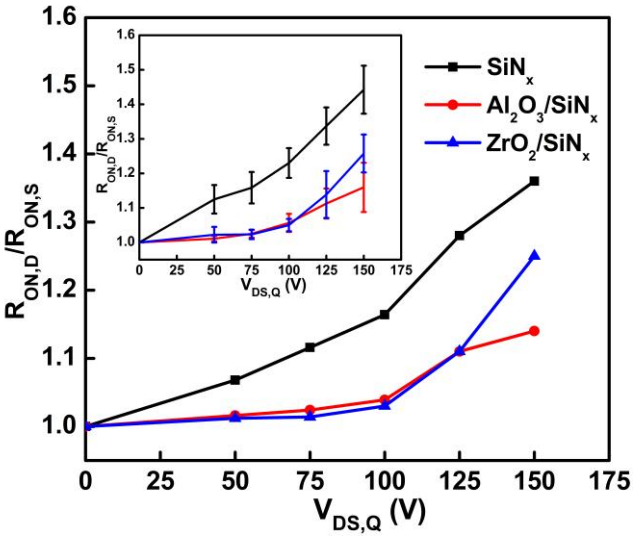


Fig. 5. Ratio of the dynamic on-resistance over the static one ($R_{ON,D}/R_{ON,S}$) of the fabricated AlGaN/GaN MIS-HEMTs at different quiescent drain bias points. (Inset figure: The means value and the standard deviation of $R_{ON,D}/R_{ON,S}$ at different quiescent drain bias points)

The MIS-capacitors with PECVD-SiN_x, ALD-Al_2O_3 or ALD-ZrO_2 as the dielectric have been fabricated to extract the shallow interface state density between the PECVD-SiN_x/GaN or between the ALD-oxides/GaN. The thickness of dielectrics is 22 nm for all samples. Multi-frequency C-V characteristic curves of MIS-capacitors are shown in Fig. 6. The measurement gate bias was swept from -10 V to 5 V with a step of 50 mV, and the frequency was varied from 2 MHz down to 1 kHz. A large bias voltage could act as an electric stress on the gate that would generate more defects at the dielectric/GaN interface and the dielectrics bulk [17]. Therefore, the maximum gate bias was set as 5 V for the CV measurement to estimate the as-grown interface defects. The C-V curves feature two rising edges. The first rising edge at negative V_G corresponds to the formation of the two dimensional electron gas (2DEG) channel, and the second rising edge at positive V_G refers to the spill-over of the 2DEG at the dielectric/GaN interface. The frequency dispersion at the second rising edge has been observed in all samples and a larger frequency dispersion indicates a higher dielectric/GaN interface traps density. Furthermore, when applying a higher gate voltage, electrons start to be accumulated in the AlGaN barrier, leading to an increase of capacitance to the insulators capacitance. Note that the capacitance of the ZrO_2/GaN sample is higher than that of the other two samples, which is due to a higher relative permittivity of the ZrO_2 film. The obvious horizontal frequency dispersion is detected in the second rising edge for the SiN_x/GaN and ZrO_2/GaN samples. In the case of SiN_x/GaN device, the interface includes very high interface trap density (D_{it}), thus the second step at low frequency cannot be observed even at high forward gate bias [18]. The maximum capacitance of SiN_x sample was extracted as 221 nF/cm^2. If using the maximum capacitance value to estimate the dielectric constant of the SiN_x film, the result would be 5.4 that is significantly lower than its theoretical value (~7.5). Moreover, the down-sweep C-V curve at 1 kHz exhibited a much steeper slope at the forward biases (Not shown here). It is speculated that the accumulation capacitance or the second C-V step was not reached in the SiN_x sample, due to a high density of traps at the PECVD-SiN_x/GaN interface. By contrast, a rising edge with a smaller frequency dispersion is observed by using the Al_2O_3 as the dielectric. The dielectrics/GaN D_{it} can be calculated by the second slope onset voltage in the multi-frequency C-V curves.

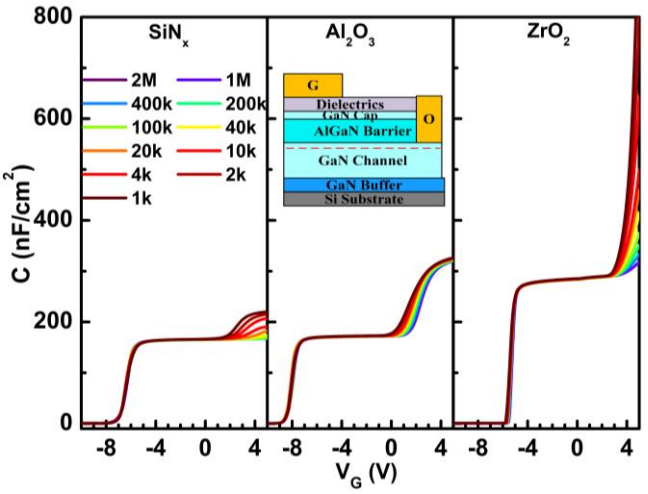


Fig. 6. Multi-frequency C-V characteristics of insulators/GaN/AlGaN/GaN MIS-capacitors structures with the SiN_x (sample A), Al_2O_3 (sample B) and ZrO_2 (sample C) as the dielectric. (Inset figure: cross-sectional schematic of MIS-capacitors with a 22 nm dielectric)

Fig. 7 shows the interface trap density distributions at the dielectrics/GaN interface for the MIS-capacitor structures obtained from the interface state density - energy level mapping method [19]. The means value and the standard deviation of interface trap density were plotted in the inserted figure that were extracted from 8 representative devices for each sample. Note that, the sample C with ZrO_2 dielectric exhibited a significant leakage current (> 0.1 μA/mm) at a forward bias of 5 V, the accumulation C-V plateau at forward biases were not shown up. The capacitance of the ZrO_2 film was extracted from the ZrO_2/Si MOS capacitor structure. For the SiN_x/GaN sample, the D_{it} is calculated to be over 3×10^{13} cm^{-2}eV^{-1} in the energy level range of ~0.38 eV to ~0.47 eV from the conduction band, which can be explained by the plasma damage on the exposed GaN surface during the SiN_x deposition. Moreover, the D_{it} at the shallower energy level cannot be calculated by the C-V method, because the second steps at low frequency have not been observed. For the ZrO_2/GaN sample, D_{it} varies from 9.4×10^{12} cm^{-2}eV^{-1} to 4.7×10^{13} cm^{-2}eV^{-1}, when the energy level depth changes from ~0.28 eV to ~0.47 eV. In comparison, the Al_2O_3/GaN sample shows the lowest D_{it} distribution among the three samples from 1.3×10^{13} cm^{-2}eV^{-1} down to 8.6×10^{12} cm^{-2}eV^{-1}.

It demonstrates that the shallow traps on the GaN surface has been effectively suppressed by the ALD-Al_2O_3. Lower D_{it} at the dielectrics/GaN interface would have a weak electron trapping effect under a quiescent stress. This also supports the suppression of the current collapse effect in the Al_2O_3/SiN_x passivated devices, as illustrated in Fig. 5.

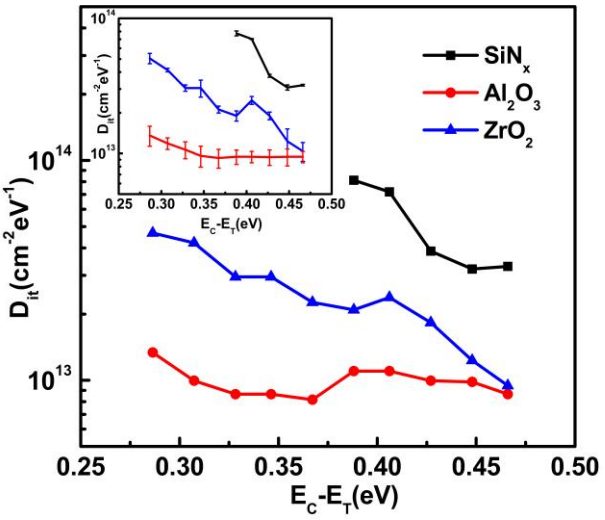


Fig. 7. Distribution of D_{it} vs. (E_C – E_T) at the dielectrics/GaN interface extracted from C-V characteristics. (Inset figure: The means value and the standard deviation of D_{it} at (E_C – E_T) from ~0.28 eV to ~0.47 eV)

Fig. 8 demonstrates the off-state breakdown characteristics of MIS-HEMTs at V_{GS} = -15 V with the floating substrate. The inserted figure shows the off-state I_D and I_G curves of 11 representative devices for each sample. The sample A passivated by PECVD-SiN_x presents a breakdown voltage of 885 V, the sample B with Al_2O_3/SiN_x passivation exhibits a breakdown voltage of 1092 V, which were extracted at drain leakage current criterion of 10 uA/mm. By contrast, for the samples C with ZrO_2/SiN_x passivation, a higher hard breakdown voltage of 1207 V is observed, giving a power figure of merit ($BV^2/R_{on,sp}$) of 447 MW/cm^2. Note that, the gate leakage current is equal to the drain leakage current for all measured devices, thus I_D and I_G curves are overlapped, as shown in Fig. 8. It indicates that MIS-HEMTs with and without high-k dielectrics exhibited similar off-state drain and gate leakage performance, and the drain to gate leakage current dominated the off-state breakdown of devices.

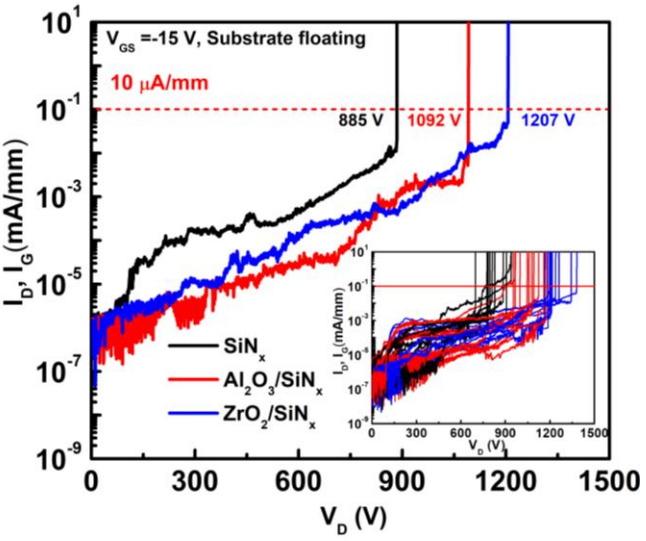


Fig. 8. Off-state breakdown characteristics of the fabricated AlGaN/GaN MIS-HEMTs with PECVD-SiN_x passivation (in black lines), Al_2O_3/SiN_x passivation (in red lines) or ZrO_2/SiN_x passivation (in blue lines). (Inset figure: the off-state breakdown characteristics of 11 representative MIS-HEMTs for each sample).

The 2-D electric field analysis was implemented by using Sentaurus TCAD simulation tools to further explain why the high-k dielectrics passivited devices exhibit a higher breakdown voltage. The gate dielectric is a 20 nm Al_2O_3. The passivation layer is 100 nm thick and its relative permittivity (ε_r) is set as 4.2, 10, 20 and 30 in the simulation evaluation. The donor concentration in the AlGaN barrier and GaN channel layer is set at a low value of 1×10^{15} cm^{-3}. The devices are in an off-state, and their dimension is fixed as a 3 μm L_{SG}, a 3 μm L_G, and a 15 μm L_{GD}. Here, we consider a high acceptor density in the GaN buffer layer of 1×10^{17} cm^{-3}, because a recent research [20] reported that a high acceptor density is required to mitigate the short-channel effects. Fig. 9 plots the electric field (E) profiles along the AlGaN/GaN heterojunction interface at drain biases of 200 V, 400 V and 600 V. When ε_r = 4.2 (in Fig. 9(a)), the increase in V_D is entirely applied along the drain edge of the gate. By contrast, when ε_r = 30 (in Fig. 9(d)), the electric field peak is reduced. The difference in electric fields can be explained by the following: According to Gauss's law, the electric field across a dielectric is inversely proportional to its relative permittivity with a constant voltage applied on. For the devices when the high-k dielectrics passivated on the GaN, the electric field drop becomes weaker from the drain to the gate. Note that, impact ionization effect caused by a high electric field would lead to the generation of electrons and holes. The generated carriers flow to the electrodes would cause a sudden increase in gate leakage current or drain leakage current [10]. Therefore, the passivation layer with a higher ε_r can more reduce electric field peak at the drain edge of the gate, then the improvement of gate hard breakdown voltage becomes more significant. A similar phenomenon has also been reported in Ref. [11].

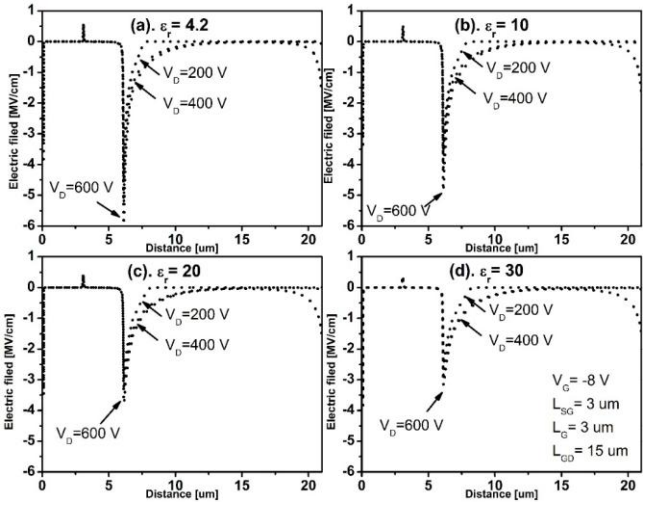


Fig. 9. Electric field profiles along AlGaN/GaN interface. (a) ε_r = 4.2, (b) ε_r = 10, (c) ε_r = 20 and (d) ε_r = 30.

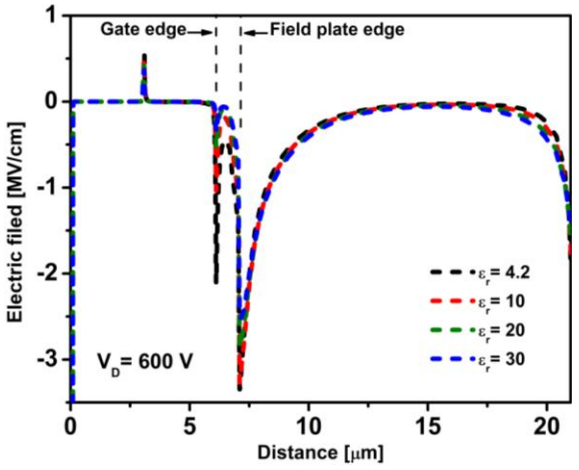


Fig. 10. Electric field profiles along AlGaN/GaN interface for a field plate length of 1 μm.

In the actual case, there was a 1 μm field plate-like hang at the drain side of the gate on the fabricated devices, which was used to avoid the alignment mistake during the photolithography process. Fig. 10 shows a comparison of electric field profiles at the AlGaN/GaN heterojunction interface for a 1 μm field plate at four cases with ε_r = 4.2, 10, 20 and 30. It can be observed that the field plate reduces the electric field peak at the drain edge of gate significantly and causes a new electric field peak at the terminal of the field plate. In the case of ε_r = 4.2 (dashed line in black), the electric fields at the drain-electrode edge as well as at the field-plate edge become very high. By contrast, in the case of ε_r = 30 (dashed line in blue), the electric field profiles in these two regions are weaker. It is also indicated that the high-k passivation would not affect the field plates' function in modulating the electric field. In addition, a more uniform and weaker electric field distribution can be achieved from the drain to the gate for the case with the high-k passivation layer plus the field plate structure.

In Fig. 11, benchmarks of the breakdown voltage versus the specific on-resistance of the three samples were presented and compared with other reported gate recess free GaN based MIS-HEMTs [3-5, 21-26]. The sample C exhibited a specific on-resistance ($R_{ON,SP}$) of 3.26 mΩ•cm^2, taking a 3 μm transfer length for source and drain ohmic contacts into account. The fabricated AlGaN/GaN MIS-HEMTs with the ZrO_2/SiN_x passivation in this paper exhibited a satisfactory breakdown characteristic compared with other mainstream reports of GaN-based MIS-HEMTs. Note that, although insertion of the high-k interlayers is capable of improving the high power performances of GaN-based devices, the additional step of ALD is required to be added into the fabrication process, which would increase the costs of devices fabrication. Further works will be focused on growing the high quality high-k dielectrics with a large thickness by using rapid deposition techniques.

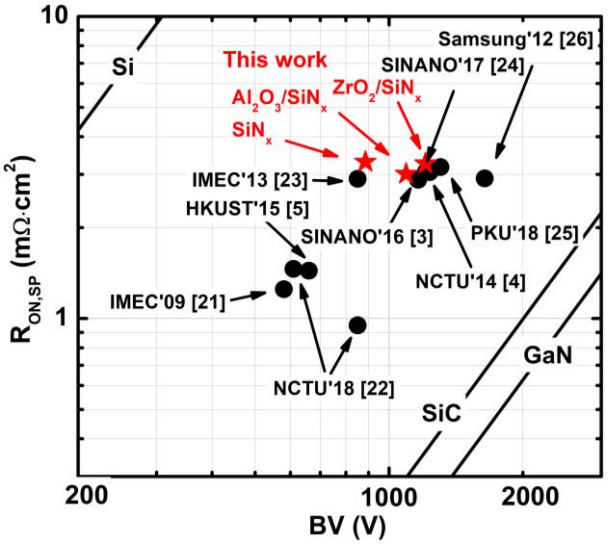


Fig. 11. Benchmark of breakdown voltage (BV) versus specific on-resistance ($R_{ON,SP}$) for devices in this work and state-of-the-art gate recess free GaN based MIS-HEMTs.

IV. CONCLUSION

In summary, the AlGaN/GaN MIS-HEMTs with SiN_x single-layer passivation or with high-k dielectrics/SiN_x bilayer passivation are demonstrated and compared. The Al_2O_3/SiN_x passivated MIS-HEMTs present a breakdown voltage of 939 V, and the ZrO_2/SiN_x passivated MIS-HEMTs present a further high breakdown voltage of 1170 V. Moreover, switching after an off-state $V_{DS,Q}$ stress of 150 V, the current collapse effect of the high-k dielectrics/SiN_x passivated devices are significantly suppressed. This points out that the surface traps on GaN can be passivated by the robust ALD dielectrics effectively. The results show a remarkable improvement in the

breakdown and dynamic characteristics compared with the PECVD-SiN_x passivated MIS-HEMTs. In addition, we have made a 2-D TCAD simulation of electric field profiles in the off-state MIS-HEMTs, where the devices with various relative permittivity of the passivation layer are analyzed. The simulation analysis points out that the high-k passivation is capable of reducing the electric field intensity at the drain edge of the gate in MIS-HEMTs, thus improve the breakdown characteristic. The measured breakdown performance is in accordance with the simulated result, indicating that the breakdown characteristics of MIS-HEMTs can be improved by increasing the relative permittivity of the passivation layer. This shows a significant potential of employing ALD high-k dielectrics as the passivation layer on the GaN-based devices for high voltage switch applications.

ACKNOWLEDGMENT

This work was supported by the Natural Science Foundation of the Jiangsu Higher Education Institutions of China (18KJB470023), Suzhou Industrial Park Initiative Platform Development for Suzhou Municipal Key Lab for New Energy Technology (RR0140), the Key Program Special Fund in XJTLU (KSF-A-05) (KSF-A-12), and the XJTLU Research Development Fund (PGRS-13-03-01 and RDF-14-02-02).

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