# Symbol Splitting-based Simultaneous Wireless Information and Power Transfer System for WPAN applications

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***Abstract*—A compact system design for simultaneous wireless information and power transfer (SWIPT) based on a novel symbol-splitting- technique (SS) is proposed in this letter. A rat-race coupler is adopted between the receiving terminal and the rectifier to facilitate the separation and isolation of the non-information-carrying components of the received signal from the information-carrying components for rectification and data recovery respectively. The maximum conversion efficiency of the design reaches over 60% with -4 dBm input power and remains around 50% down to input powers of -10 dBm in measurements using both continuous wave (CW) signals and modulated signals with different data rates as inputs. The transferred data are correctly received and recovered at the isolation port of the coupler. The design is 51.7 x 49.3 mm$^2$ and all measurement results show good agreement with simulation results.**

***Index Terms*—symbol-splitting (SS), simultaneous wireless information and power transfer (SWIPT), wireless personal area network (WPAN).**

## I. INTRODUCTION

SIMULTANEOUS wireless information and power transfer (SWIPT) has been proposed by the research community as a compact way to concurrently provide power to distributed sensors whilst communicating with them [1]-[3]. Previous studies on SWIPT have structured the information decoding (ID) and power transferring (PT) of receivers separately [2], [3]. However, as the energy consumption in wireless information transfer (WIT) receivers is large due to the use of a downconverter and such systems are cumbersome, integrated receiver architectures which apply rectifying have been considered, such as that presented in [4].

To realize SWIPT practically, such systems separate the received signal into two distinct parts using various splitting methods. Among these, time-splitting (TS), power-splitting (PS) and frequency-splitting (FS) are the most popular ways to achieve SWIPT [5]-[10]. In TS, as shown in Fig. 1(a), a switch is employed at the receiver and the received signal can be used for either ID or PT at any given time. This method is straightforward to employ but requires precise time synchronization and information detection. In the PS technique shown in Fig. 1(b), a power divider component is utilized to divide the received signal into two streams with a designed power ratio. The major merit is that the signal is used for both functions in the same time slot. However, information loss is inevitable as some porting of the information part of the signal to PT occurs. The FS technique, shown in Fig. 1(c), uses two antennas or a dual band rectenna, with each antenna or each port of the rectenna (frequency band) used for a specific purpose (ID or PT). Although information loss is reduced, the non-information carrying component of the transmitted data signal is wasted.

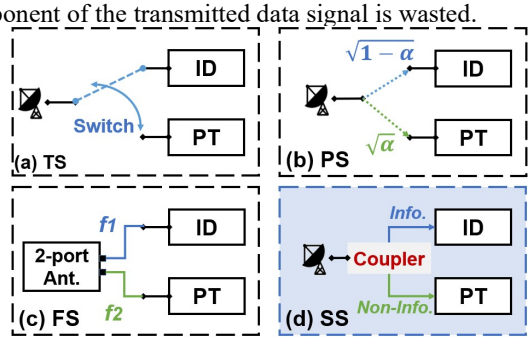


Fig. 1: Splitting techniques for SWIPT: (a) time splitting (b) power splitting (c) frequency splitting and (d) proposed symbol-splitting technique.

In this letter, a compact SWIPT system for wireless personal area network (WPAN) applications based on a novel symbol-splitting (SS) technique is proposed to address the drawbacks of the splitting techniques discussed above. As shown in Fig. 1 (d), this technique achieves SWIPT by splitting the information- and non-information-carrying components of the received signal for ID and PT respectively. A rat-race coupler is employed between the receiving antenna and a full-wave Greinacher rectifying circuit. The receiver operation is introduced in Section II. Section III discusses both simulated and experimental results used to validate the proposed method and conclusions are drawn in Section IV.

## II. OPERATION MECHANISM

Considering WPAN applications, a working frequency of 2.45 GHz is used for in proposed system. The system topology is shown in Fig. 2.

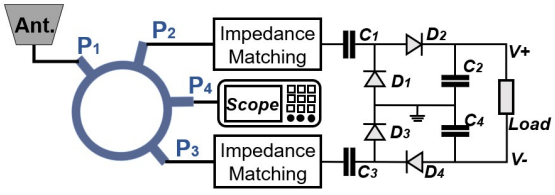


Fig. 2: Block diagram of the proposed topology.

Manuscript received XX, 2019; revised XX; accepted XX. Date of publication XX; date of current version XX. This work was supported in part by the XJTLU Research Development Fund under Grant PGRS-13-03-10 and Grant RDF-14-03-24.

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Digital Object Identifier MWCL-20-0359

### A. Analysis of data extraction

Here a BPSK signal is used as an example to show how SS works. The frequency response of a bit sequence (rectangular function in time domain) is a sinc function, which is continuous in frequency domain. The carrier is a cosine function with carrier frequency ($f_c$) in time domain and its frequency response is an impulse at $f_c$. The frequency response of the corresponding BPSK is then the convolution of those two spectra. The main idea is to extract the impulse at $f_c$ for rectification since carrier does not contain any information, and then retain the remainder of the continuous spectrum (i.e. information) for ID. The rat-race coupler has the *S*-parameter matrix shown in (1) at its operating frequency according to the odd-even mode theory [11]. Based on its principal behavior, the narrow-band band-stop property of the isolation port ($P_4$) at $f_0$ offers a route to SS. The incoming modulated signal from the receiver enters the coupler through $P_1$ and will be equally divided and delivered to $P_2$ and $P_3$ as shown in Fig. 2. The information carrying components will be 'filtered' through $P_4$, which is detected here by an oscilloscope. Validation of this is provided in the next section. The simulated *S*-parameters of a rat-race coupler designed on RT/Duroid 5880 substrate with a relative permittivity of 2.2 and thickness of 1.575 mm are given in Fig. 3, and which show the possibility of differentially distributing the incident signal at $f_c$ from $P_1$ to $P_2$ and $P_3$.

$$S=-\frac{1}{\sqrt{2}}\begin{bmatrix} 0 & j & -j & 0 \\ j & 0 & 0 & j \\ -j & 0 & 0 & j \\ 0 & j & j & 0 \end{bmatrix} \quad (1)$$

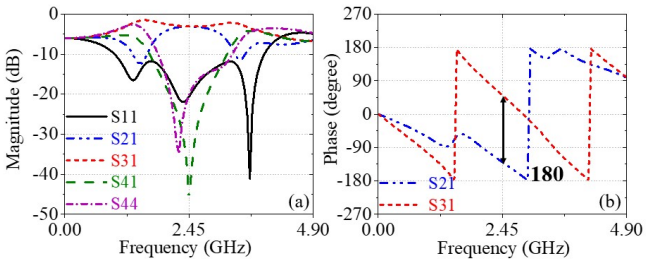


Fig.3: Simulated *S*-parameters of a rat-race coupler designed on RT/Duroid 5880: (a) magnitudes of $S_{11}$, $S_{21}$, $S_{31}$, $S_{41}$, $S_{44}$ and (b) phases of $S_{21}$, $S_{31}$.

### B. Rectifier Performance

A rectifying circuit is the crucial component of a PT sub-system. In this work, a full-wave Greinacher rectifier is selected for rectification, for its power sensitivity and RF-to-DC power conversion efficiency (PCE) [12],[13]. The packaged Schottky diode SMS7630 is adopted as it has a low bias voltage, high saturation current and low power loss, which is favorable for high power rectification (forward bias voltage: 60-120 mV at 0.1 mA) [14]. For modelling purposes, a nonlinear spice model with parasitic elements was used for the Schottky diode, provided by Skyworks Solutions Inc. [14]. Meanwhile, capacitors ($C_1$, $C_2$, $C_3$, and $C_4$) were simulated as their real product models including *S*-parameter files provided by the supplier *Murata* to improve simulation accuracy. In addition, the impedance matching networks shown in Fig. 4 were designed to be matched not only in frequency, but also as a function of input power level and therefore the rectifying circuit can be used over a range of input power levels. The circuit dimensions are listed in Table I and they have been optimized using the Advanced Design System 2017 (ADS2017) software. A load resistance $Z_L$ of 25 kΩ is adopted for the initial study as it is a typical load value for a variety of WPAN sensors [15], [16].

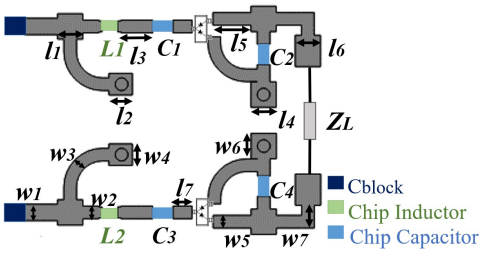


Fig. 4: Topology of the rectifying circuit.

TABLE I

OPTIMIZED DIMENSIONS (LENGTH UNITS: MILLIMETERS)

| Parameter | Value | Parameter | Value | Parameter | Value |
|---|---|---|---|---|---|
| *l1* | 2.00 | *l7* | 1.50 | *w6* | 2.00 |
| *l2* | 1.70 | *w1* | 2.78 | *w7* | 0.79 |
| *l3* | 2.50 | *w2* | 1.30 | $C_1$~$C_4$ | 100 nF |
| *l4, l6* | 2.00 | *w3, w5* | 1.00 | *Cblock* | 20 pF |
| *l5* | 3.00 | *w4* | 1.70 | $L_1$, $L_2$ | 2 nH |

## III. SIMULATION AND EXPERIMENTAL VALIDATION

The proposed system has been simulated in ADS2017 and fabricated on RT/Duroid 5880 substrate. For the purpose of miniaturizing the size of the system, a ring coupler is selected. The overall dimension of the optimized design is 51.7 x 49.3 mm$^2$. For validation, $P_1$ of the system is connected to a signal generator and a Rohde & Schwarz RTO2044 oscilloscope is connected to $P_4$ to observe the output information waveform as illustrated in Fig. 5. A digital multimeter is used to measure the DC output across the load.

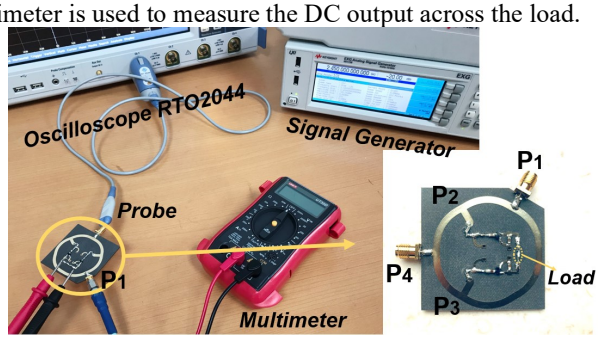


Fig. 5: Realization of experimental validation setup with the fabricated board.

### A. Information Detection

BPSK is adopted in order to validate the ability of the communication link as it is commonly used for WPAN applications [17]. The expression of BPSK is given in (2) where $T_c$ is the carrier period and the rate of data transmission $R_b$ within a period can be expressed by $R_b = (f_c / N)$:

$$s(t)=\begin{cases} \sin(2\pi f_c t), & 0 \le t \le NT_c, \quad k=0 \\ -\sin(2\pi f_c t), & 0 \le t \le NT_c, \quad k=1 \end{cases} \quad (2)$$

The base data sequence is '010110' and the data rate is set to be 245 Mbps. The transmitted modulated signal is shown in

Fig. 6(b). The power is set to 0.2 mW (-7 dBm) and corresponding amplitude of its waveform is 0.281 V. Based on the distribution properties of the coupler, the actual signals flowing to $P_2$ and $P_3$ are shown in Fig. 6(c) each with a power of ≈0.1 mW (-10 dBm). The simulated and measured output signal captured from $P_4$ of the coupler are shown in Fig. 6(d) and Fig. 6(e), respectively. Compared to the transmitted signal, the output signal from the isolation port only contains the phase changes. The measured voltage of the output signal is 0.142 V at the transition point, which is around half of that of the transmitted signal. In addition, with the actual -10 dBm signals at $P_2$ and $P_3$, the corresponding simulated rectified DC output signal in time domain is depicted in Fig. 7(c). The DC voltage reaches 1.095 V when the system reaches steady state.

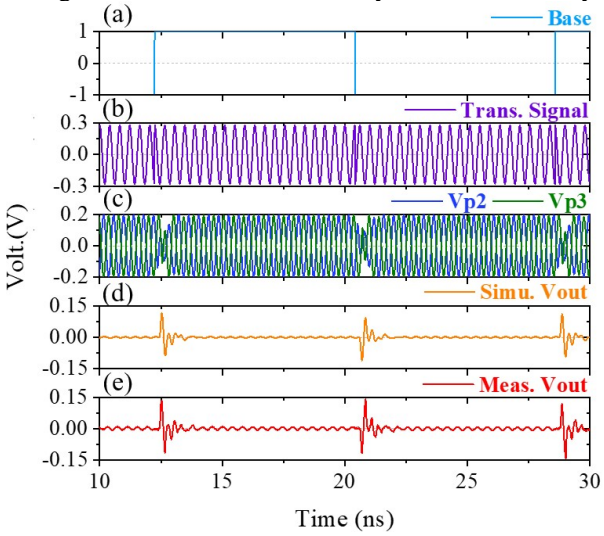


Fig. 6: Voltage waveforms of (a) base signal, (b) transmitted signal, (c) incoming signal at $P_2$ & $P_3$, (d) simulated output signal from $P_4$ and (e) measured output signal from $P_4$ within 20 ns.

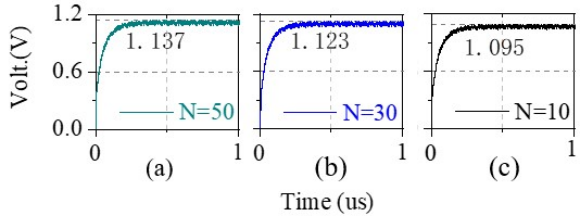


Fig. 7: Simulated waveform of the DC output signal generated by the whole system for $R_b$ = (a) 49 Mbps, (b) 81.6 Mbps and (c) 245 Mbps.

### *B PCEs of the proposed system*

A pre-calibrated RF signal generator KEYSIGHT EXG-N5173B (for CW signals) and Agilent E4438C (for BPSK signals) were used as the input sources. CW signals with different power levels are first used to analyze the performance of the system, as shown in Fig. 8(a) for reference. The PCE can be expressed as (3):

$$PCE = \frac{P_{DC}}{P_{in}} = \frac{V_{DC}^{\ 2}}{P_{in} Z_L} \tag{3}$$

where $P_{DC}$ is the output DC power, $P_{in}$ is the input power and $V_{DC}$ is the output DC voltage.

From Fig. 8(a), PCE increases with $P_{in}$ and the peak value is 64.95% for simulation at -4 dBm and 64.60% at -3 dBm for measurement. After the peak, PCE decreases due to the reverse breakdown voltage of diodes. The differences are probably due to fabrication errors (*e.g.* hand soldering) and the tolerance in parasitic behavior of the SMD components.

Measured PCEs for BPSK input signals at varying data rates are depicted in Fig. 8(b). In general, PCEs for modulated signals is lower than that for CW signals. When the received power is -10 dBm, the measured DC outputs are 1.09 V, 1.12V and 1.13V, for $R_b$ equal to 245 Mbps, 81.6 Mbps and 49 Mbps respectively, which agree well with the simulations depicted in Fig. 7. Corresponding PCEs are around 47.46%, 49.86% and 51.25% respectively. PCEs reach their peak, about 59.19%, 60.34% and 61.39% respectively when $P_{in}$ is -4 dBm. This figure also shows that the PCE of BPSK signals increases as the data rate $R_b$ decreases.

A comparison with other reported SWIPT designs is provided in Table II. The proposed system has a relatively high output voltage at low input powers. PCE in this work is slightly lower than that in [19], but a lower input power range has been focused on here. Meanwhile, this work uses the SS technique which is novel from other works.

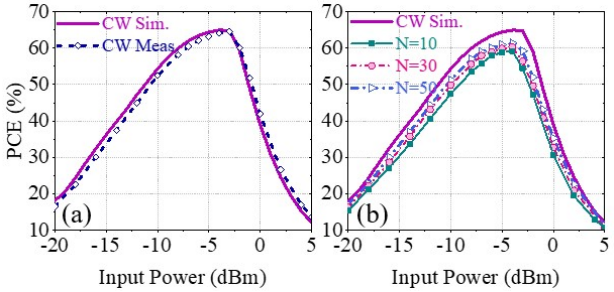


Fig. 8: PCEs versus input power level for (a) CW case, (b) BPSK cases.

TABLE II
Comparison with Other SWIPT Systems

| Ref. | $f$ (GHz) | Waveform | $P_{in}$ (dBm) | Measured PCE (maximum) | $V_{out}$ (V) (at -10 dBm) |
|---|---|---|---|---|---|
| [18] | 2.45 | PSK | -10 | -- | 0.4 ($R_b$=50 kHz) |
| [19] | 2.58 | CW<br>QPSK | 6 to 26 | 74.9%<br>67%<br>(10 MHz BW) | -- |
| **This work** | **2.45** | **CW<br>BPSK** | **-20 to 5** | **64.6%<br>59.19~61.39%<br>(*N*=10/30/50)** | **1.09~1.13<br>(*N*=10/30/50)** |

## IV. Conclusions

In this letter, a compact system for SWIPT has been proposed, analyzed, fabricated, and tested. The main novelty is that a new symbol-splitting technique is proposed utilizing a rat-race coupler to extract the information from the received signal and fulfil the data recovery operation. The maximum measured PCE's are around 65% and 60% for CW and BPSK signals of different data rates, respectively. Meanwhile, the communication capability is verified by monitoring the information extracted. The DC output voltage sustains an amplitude of approximately 1 V at an incident power of 0.2 mW for a 245 Mbps BPSK signal. Data is clearly extracted from the received signal whose voltage amplitude is around half that of the incident signal. Experimental examinations support the simulation results, which certify that this system design can be adapted as a promising candidate for SWIPT.

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