Monolithic comparator and sawtooth generator of AlGaN/GaN MIS-HEMTs with threshold voltage modulation for high-temperature applications

Ang Li, *Student Member, IEEE*, Miao Cui, Yi Shen, Ziqian Li, Wen Liu, Ivona Z. Mitrovic, *Senior Member, IEEE*, Huiqing Wen, *Senior Member, IEEE*, and Cezhou Zhao.

***Abstract*— This paper demonstrates the integrated comparators, hysteresis comparators and sawtooth generators based on AlGaN/GaN metal insulator semiconductor high electron mobility transistors (MIS-HEMTs). The integrated circuits (ICs) exhibit thermal stability from 25 ℃ to 250 ℃ in both static and transient performances. The threshold voltage (V_{th}) in depletion (D)-mode MIS-HEMT is modulated from -8.9 V to -2.4 V to optimize the performance of integrated comparator circuits. The comparator can realize a large and stable comparison range of 3 V–9 V and a high voltage swing of 9.1 V, while the hysteresis comparator exhibits a good noise-immunity ability and stable hysteresis output. The sawtooth generator with the hysteresis comparator features a high amplitude (6.1 V) sawtooth signal at 500 kHz to realize a compact structure applicable to the high-voltage mixed-signal circuits. These results show the feasibility of MIS-HEMT monolithic comparator circuits in conversion systems.**

***Index Terms*— GaN, All-GaN circuit, MIS-HEMTs, threshold voltage modulation, comparator, sawtooth generator.**

I. Introduction

GAN-based devices have emerged as promising candidates in power applications due to high-breakdown field, high-frequency and high-temperature operations [1]-[3]. GaN integrated circuits have generated smart power platform with high-power components and mixed-signal functional blocks. In monolithic ICs, as a fundamental unit for mixed-signal circuits, the comparator has attracted considerable attention recently [4]-[7]. The conventional GaN comparator circuits are based on normally-ON technology which limits the level of integration. There have been GaN comparator-based ICs realized by the F-ion injection technology in pulse width modulation (PWM) [6], protection circuit [8], [9], and the normally-OFF technology eliminates the negative voltage driving and reduces complex. The MIS-HEMT ICs are designed for driving and protection circuits in high-power conversion systems since the voltage swing on the Schottky gate of F-ion injection HEMT can be improved. In particular, compared with HEMT circuits, AlGaN/GaN MIS-HEMTs have superior properties for low leakage current and large gate voltage swing [10], [11], allowing more input tolerance and avoiding the extra gate protection techniques or a level shifter.

In integrated circuit design, the characteristics of threshold voltage matching influence the operating range and performance or power of the circuit. The conventional MIS-HEMT ICs with extra insulator-layer lead to an increased magnitude of threshold voltage in the D-mode device and the mismatch in D-mode and E-mode devices [12], [13], which only meets specific requirements for circuits [14], [15]. The digital etching process in the D-mode gate area by O_2 plasma can facilitate V_{th} modulation [16]-[18], which improves the flexibility and high voltage operation of MIS-gate. The modulated MIS-HEMT ICs are potential for the mixed-signal circuits, especially for the bootstrap comparator and sawtooth generator.

The GaN functional devices exhibit the high-temperature feature, and the logic inverter based on MIS-HEMT has been proven to have thermal stability [19], [20], but a differential pair structure is required to further suppress the temperature variation [21] when implementing sensitive circuits, such as comparators and signal generators. The GaN ICs can allow applications in high-temperature environments, such as the electric vehicle, space application, and oil drilling [22].

In this work, we fabricated the GaN comparator, hysteresis comparator and sawtooth generator with MIS-HEMTs, operating normally from 25 °C to 250 °C. To improve the performance, the gate control of the D-mode device is enhanced by the etching process, which solves the mismatch between the D-mode and E-mode. The threshold voltage modulation extends the comparison range of comparator circuits and high amplitude in the sawtooth generator. The MIS-HEMTs sawtooth generator has a compact topology by eliminating the

This work was supported by the Suzhou Industrial Park Initiative Platform Development for Suzhou Municipal Key Lab for New Energy Technology (RR0140), the Suzhou Science and Technology program (SYG201923), the Key Program Special Fund in XJTLU (KSF-A-05, KSF-A-12 and KSF-T-07), and the XJTLU Research Development Fund (RDF-16-02-11). (*Corresponding authors: Wen Liu; Cezhou Zhao.*)

A. Li, M. Cui, Y. Shen, Z. Li, W. Liu, H. Wen, and C. Zhao are with the Department of Electrical and Electronic Engineering, Xi'an Jiaotong-Liverpool University, Suzhou 215123, China, and also of Electrical Engineering and Electronics, University of Liverpool, Liverpool L69 3GJ, U.K. (e-mail: Wen.Liu@xjtlu.edu.cn; Cezhou.Zhao@xjtlu.edu.cn).

I. Z. Mitrovic is with the Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool L69 3GJ, U.K. (e-mail: ivona@liverpool.ac.uk)

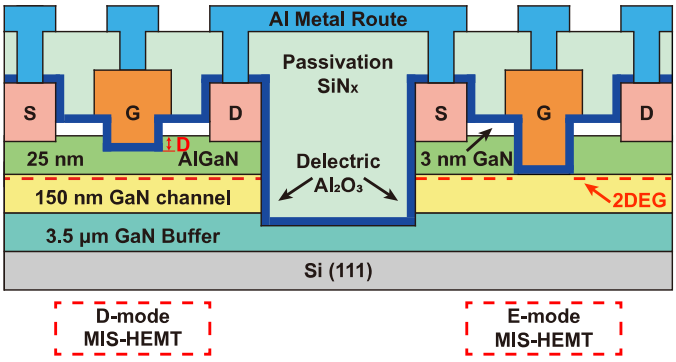

Fig. 1. Schematic cross-section of D/E-mode AlGaN/GaN MIS-HEMTs structure.

level shifter and gate protection. The feasibility of all-GaN integrated comparator circuits has been validated using lateral MIS-HEMTs, especially for high-power and high-temperature circuit applications.

II. Device Fabrication and Characteristics

Fig. 1 shows the AlGaN/GaN MIS-HEMTs structure on a Si(111) substrate. The MIS-HEMTs are composed of the GaN buffer layer (3.5 μm), GaN channel layer (150 nm), AlGaN barrier layer (25 nm), and GaN cap layer (3 nm). The gate-recess process of the E/D-mode devices was defined by photolithography and then etched by O_2 plasma digital etching for 3 minutes at RF power of 100 W at 60 °C by reactive ion etching (RIE). After the etching process, the surface treatment was wet etching in the solution of HCl:H_2O (1:10). The ohmic contact for source and drain of metal Ti/Al/Ni/TiN (22.5 nm/90 nm/60 nm/60 nm) was prepared by electron-beam evaporation, followed by rapid thermal annealing (RTA) at 880 ºC for 30 s. Then, a 20 nm Al_2O_3 gate dielectric layer was deposited by atomic layer deposition (ALD), and Ni/TiN gate metal was deposited using electron-beam evaporation. A 100 nm passivation layer SiN_x can be formed by plasma-enhanced chemical vapor deposition (PECVD) to reduce leakage and Al metal can be used to connect individual devices for the GaN ICs platform.

The threshold voltage is modulated through the etching depth of the AlGaN barrier under the gate in the D-mode device, by implementing O_2 plasma digital etching with different cycles [23]. Three chips (No.1, No.2, and No.3) were fabricated with an etch depth of 10, 14, and 18 nm in D-mode devices, respectively, and E-mode devices in the three chips have the same etch depth of 25 nm to fully recess the barrier. For the electrical characteristics, Fig. 2 shows the transfer characteristics of D/E-mode MIS-HEMTs in No.1/2/3 devices at room temperature of 25 °C (solid line) and a high temperature of 250 °C (dash line). At room temperature, the maximum drain current $I_{D,max}$ of No.1/2/3 device are 608, 424.5, and 97.3 mA/mm (V_G = 0 V), and threshold voltages V_{th} are -8.9, -6.2 and -2.3 V, respectively. The positive shift of V_{th} with increasing the etching depth is caused by the reduced sheet carrier density [24]. The E-mode device shows a maximum drain current of 313 mA/mm and a threshold voltage of +2.7 V. At 250 °C, the V_{th} of D-mode devices in

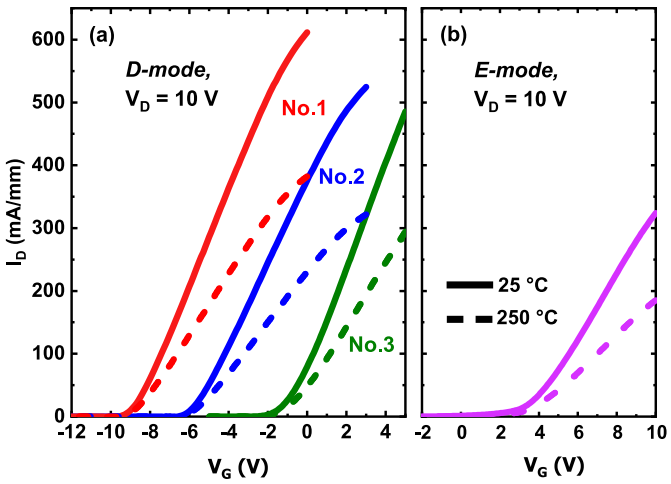

Fig. 2. Transfer characteristics of D/E-mode MIS-HEMTs at room temperature (25 ℃) and 250 ℃. (a) D-mode devices at different etching depths (D = 10/14/18 nm). $V_{th,D}$ of No.1/2/3 = -8.9/-6.2/-2.3 V at 25 ℃, and $V_{th,D}$ of No.1/2/3 = -8.7/-5.8/-2.2 V at 250 ℃. (b) E-mode device (D = 25 nm). $V_{th,E}$ = 2.7 V at 25 ℃ and 2.4 V at 250 ℃.

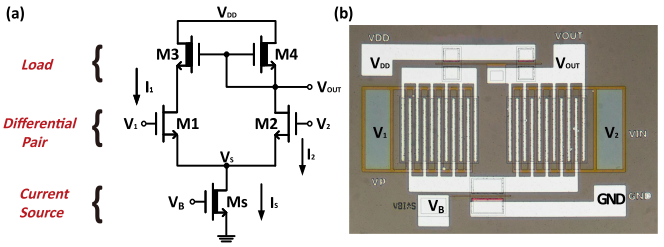

Fig. 3. (a) Circuit schematic, and (b) micro-photograph of the GaN MIS-HEMTs comparator.

No.1/2/3 is -8.7, -5.8, and -2.2 V, and the output drain currents are 382, 265.4 and 79.5 mA/mm (V_G = 0 V), respectively. The E-mode device shows a degraded current of 178.3 mA/mm and a V_{th} of +2.4 V.

III. GaN Comparator

Fig. 3 (a) shows the circuit diagram and Fig. 3 (b) depicts the micro-photograph of the comparator based on GaN MIS-HEMTs. E-mode MIS-HEMTs M1 and M2 work as an input pair while load D-mode MIS-HEMTs M3 and M4 act as an output pair, and the current source Ms is a D-mode MIS-HEMT. The transistors have the gate width W_g = 5/1000/30 μm (M3&M4/M1&M2/Ms).

In the circuit, D-mode loads are modulated by the bootstrapping mechanism with feedback from the output node. Specifically, M3 and M4 have a common gate, which is connected to the output. The sum of left branch current I_1 and right current I_2 is equal to the current of Ms (I_s). When V_1 (reference voltage V_{REF})>V_2 (input voltage V_{in}), I_1 increases, then the output is logic-high. When V_1<V_2 circuit produces logic-low [25], [26].

The GaN comparator is a logic signal circuit, which performance can be determined by the output voltage swing and comparison range. The maximum output voltage at logic-high is V_{OH}, and the minimum output voltage at logic-low is V_{OL}.

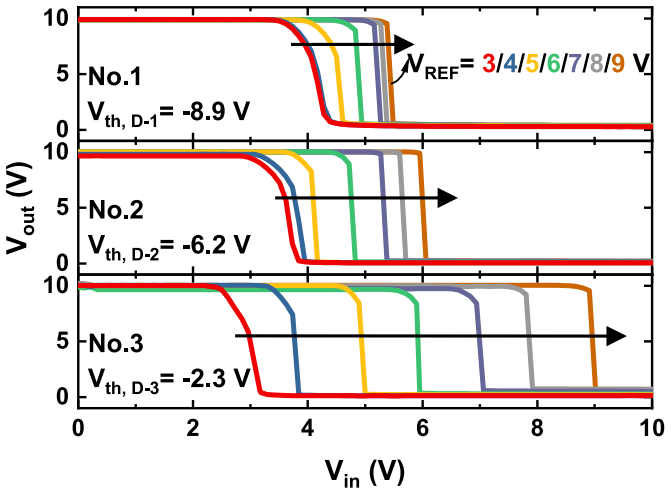

Fig. 4. Static voltage transfer curves of comparators with different V_{th} of D-mode devices at V_{DD} = 10 V. The threshold voltage of No.1/2/3 circuits are $V_{th,D-1}$ = -8.9 V, $V_{th,D-2}$ = -6.2 V and $V_{th,D-3}$ = -2.3 V, respectively. Note: $V_{th,E}$ = +2.7 V for all E-mode devices.

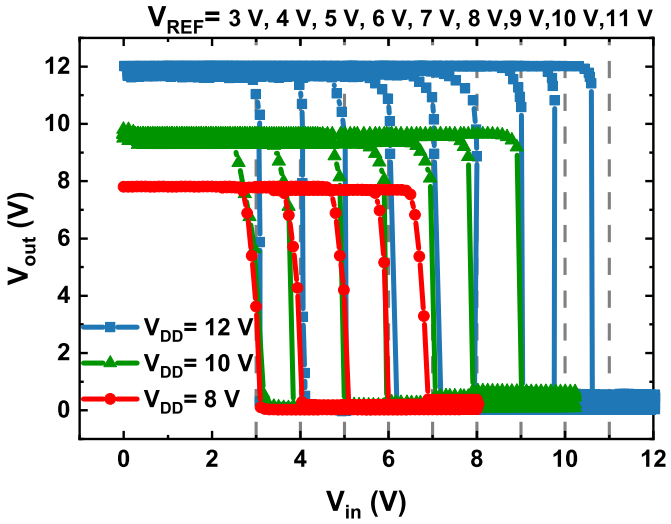

Fig. 5. Voltage transfer characteristics of the comparator in chip No.3 with different supply voltages V_{DD} = 8, 10 and 12 V.

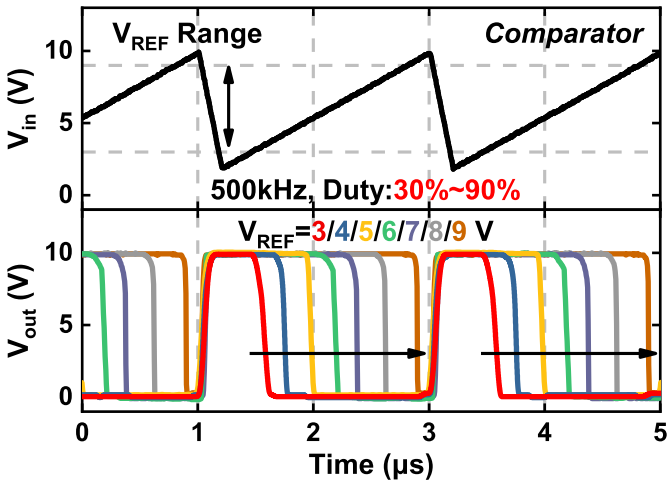

Fig. 6. Transient output waveforms of the comparator for reference voltage V_{REF} = 3/4/5/6/7/8/9 V with V_{DD} = 10 V at 500 kHz. The input voltage V_{in} is a ramp signal at 500 kHz.

The output voltage swing V_{SW} can be shown as

$$V_{SW} = V_{OH} - V_{OL}. \quad (1)$$

In the comparator circuit, the output signals can be fed back to D-mode loads. The V_{OH} is mainly determined by loads (M3 and M4) and supply voltage, and V_{OL} is influenced by the current source. The range indicates the comparison ability in circuits. The gate voltage of the current source needs to be tuned to optimize the value of logic-low. Referring to previous work, for the high input voltage, the HEMT Schottky gate causes an extra gate current which raises V_{OL} [5]. Using MIS-HEMT, its low leakage current can significantly mitigate this phenomenon. Moreover, applying a bias voltage V_B ensures that the Ms works in the linear region when output is logic low. Then, V_S is reduced, and the V_{OL} can be further suppressed for the unnecessary upward trend. The comparison range is a region between minimum input voltage and maximum input voltage, where comparator can switch the output level accurately. During the transition, D-mode and E-mode devices work in the saturation region, and their currents match. The wide input range is important for the accurate operation of the signal generator circuits and conversion system [7], [27].

The tests of the comparator are conducted with an Aglient 1500A semiconductor analyzer. Fig. 4 shows the results of comparators on three chips for No.1/2/3 with different $V_{th,D}$ at V_{DD}=10 V, which demonstrates that the comparison range can be improved by increasing $V_{th,D}$. The operating voltage ranges are 4.5–5.4 V, 4.0–5.8 V and 3.0–9.0 V for No.1, No.2, and No.3 circuits, respectively. The $V_{th,D}$ of -2.3 V is seen with the largest range for No.3 circuit. For comparators No.1 and No.2 which exhibit poor performance, the device Ms needs a large current to reach the saturation region with the over negative $V_{th,D}$, meaning a large minimum input voltage is required to realize level switch. The load is difficult to be saturated with the over negative $V_{th,D}$, hence the maximum input voltage reduces. Therefore, the GaN comparators (No.1 and No.2) exhibit a narrower comparison range.

Fig. 5 shows transfer characteristics of comparators in No.3 circuit with the supply voltages of 8 V, 10 V, and 12 V. The reference voltage V_{REF} is increased by a step of 1 V, while output voltage V_{out} is measured at each step. The comparator can handle a specific comparison range from 3 to 9 V at V_{DD} = 10 V. When V_{REF}<3 V, the reference voltage is approaching the $V_{th,E}$, which cannot operate in the differential pair. When V_{REF}>9 V, the gate overdrive of the input differential pair pushes the transistor into the saturation region, in which the output is not sensitive to V_{REF} anymore. Moreover, the average voltage swing V_{SW} can reach 9.1 V, showing the sharp level conversion from high to low.

The duty cycle of output waveforms can be tuned by the various reference voltages. Fig. 6 shows the transient output waveforms of the No.3 circuit with a 500 kHz sawtooth input signal at V_{REF} = 3/4/5/6/7/8/9 V, and the corresponding duty cycles can be tuned to 30%–90%. The comparator can compare the sawtooth signal with the preset reference voltage and generate square output with accurate control. These AC results

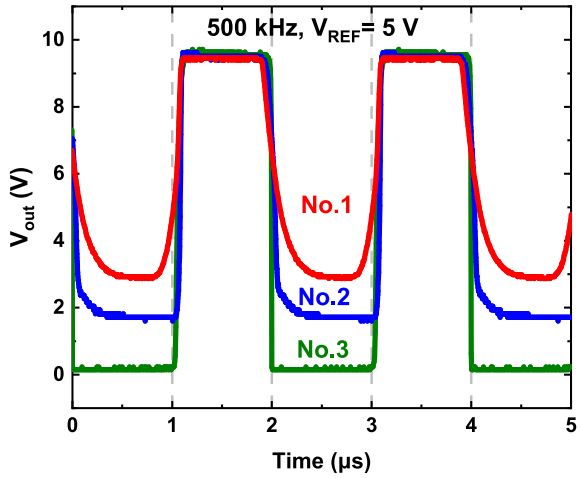

Fig. 7. Transient output waveforms of No.1/2/3 circuits with V_{REF} = 5 V at 500 kHz.

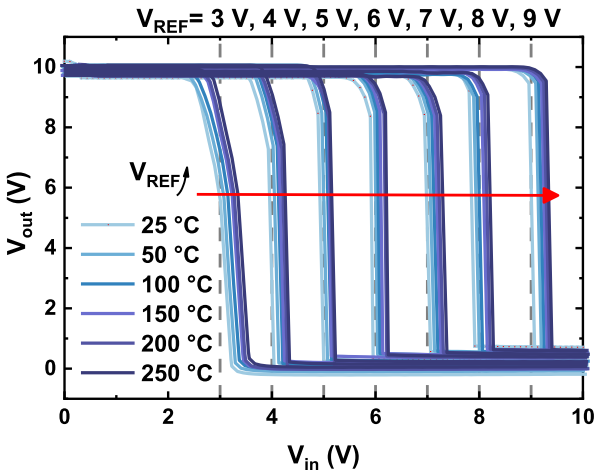

Fig. 8. Transfer curves of GaN comparator in chip No.3 at various temperatures from 25 ℃, 50 ℃ to 250 ℃, with 50 ℃/step. V_{DD} is 10 V, and V_{REF} is varied from 3 V to 9 V with 1 V/step.

of the comparator show a strong capability of wave regulation using GaN MIS-HEMTs. The MIS-based comparator can be tuned in a wide operating range from 3 V to 9 V to obtain the square output because of the large gate swing. In Fig. 7, the No.3 circuit shows better high/low level and pulse waveforms compared to No.1 and No.2 circuits. As a result, the transient output performances are more stable in the higher V_{th} in the D-mode device, which generates output voltage waveforms with a larger voltage swing. For high-temperature tests in the comparator, the circuit shows stable transfer characteristics from 25 °C to 250 °C as displayed in Fig. 8. The MIS-based structure and differential block introduced in the comparator circuit suppresses the temperature drifts. Thus, the comparator circuit demonstrates its thermal reliability and feasibility for high-temperature applications.

Under duty cycle modulation, the circuit exhibits good linearity at high frequency and high temperature, being evidenced by strong gate-control ability at a high $V_{th,D}$. The stable operating state allows further implementation of pulse control on the hysteresis comparator and PWM.

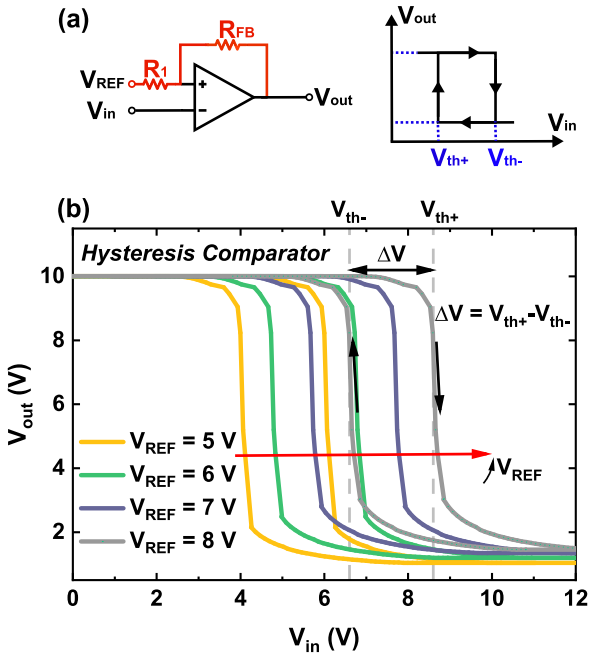

Fig. 9. (a) Hysteresis comparator circuit configuration and theoretical output waveform. (b) Transfer curves measured with R_1/R_{FB} = 100 kΩ/30 kΩ. V_{REF} = 5/6/7/8 V, V_{DD} = 10 V.

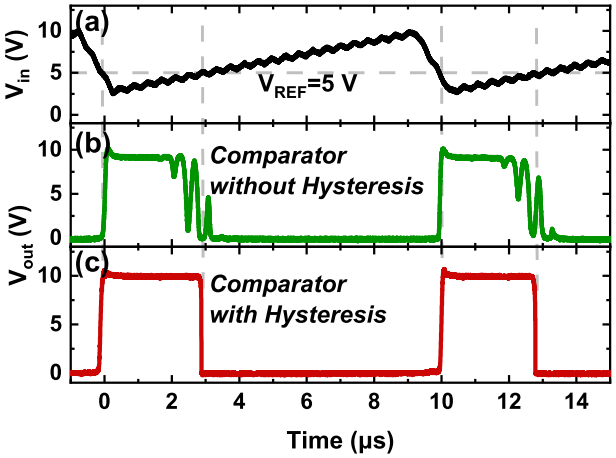

Fig. 10. The noise testing of comparator and hysteresis comparator at V_{REF} = 5 V. (a) Input signal, (b) output signal without hysteresis, and (c) output signal with hysteresis.

IV. Hysteresis Comparator

For the general comparator, the noise signal might lead to an unstable output when V_{in} is near the reference voltage. Thus, a more stable hysteresis comparator is required for noise-sensitive cases, such as signal generating circuits of the gate driver. Its positive feedback provides a bistable characteristic, which overcomes noise interference. A signal cycle of the sawtooth wave can be separated into two stages, the rising and falling stage [28]. The circuit configuration and theoretical characteristics are shown in Fig. 9 (a). The output will toggle at the crossover voltage (V_{th+} or V_{th-}) of each stage, which

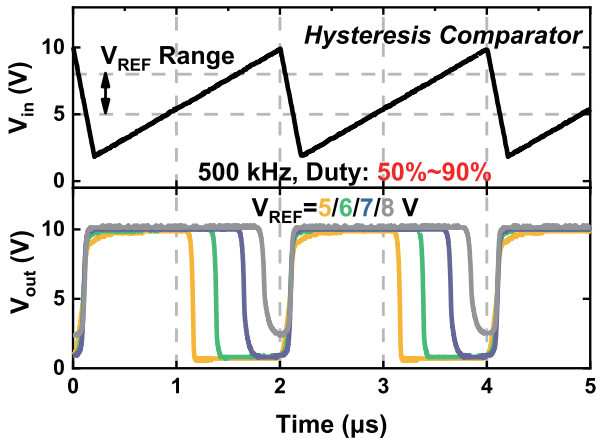

Fig. 11. Transient output waveforms of the hysteresis comparator circuit in different duty cycles at 500 kHz.

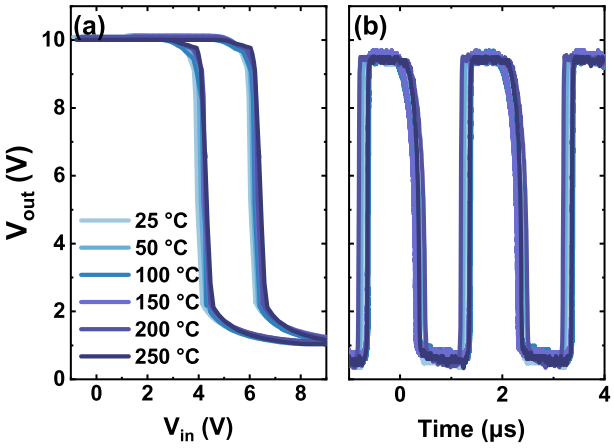

Fig. 12. Output performances of hysteresis comparator at different temperatures from RT to 250 ℃ (a) DC tests (b) AC tests at 500 kHz.

can be expressed as:

$$V_{th+} = \frac{R_1 V_{REF}}{R_1 + R_{FB}} + \frac{R_{FB} V_{OH}}{R_1 + R_{FB}} \tag{2}$$

$$V_{th-} = \frac{R_1 V_{REF}}{R_1 + R_{FB}} + \frac{R_{FB} V_{OL}}{R_1 + R_{FB}} \tag{3}$$

$$\Delta V = V_{th+} - V_{th-} = \frac{R_{FB}}{R_1 + R_{FB}} \left(V_{OH} - V_{OL} \right). \tag{4}$$

The difference of the switching thresholds (ΔV) represents the amount of hysteresis based on equation (4), and this hysteresis band can be tuned by changing the values of R_1 and R_{FB}. The GaN hysteresis comparator is the same as in Fig. 3 but with an external feedback unit.

The voltage transfer curves are shown in Fig. 9 (b) with V_{DD} = 10 V and R_1/R_{FB} = 100 kΩ/30 kΩ. The hysteresis comparator allows the reference to vary from 5 V to 8 V, while the reduced reference voltage range is tuned by positive/negative crossover voltage compared with the comparator circuit. The amount of hysteresis (ΔV) remains steady with the increase of reference voltage, when the crossover voltage shifts forward. This indicates that the hysteresis comparator has the benefit for noise-immunity. Fig. 10 (a) shows the noise-applied sawtooth input signal by function generator Agilent 33120A, and Fig. 10 (b) and (c) are the characteristics of high noise-immunity in comparators without/with hysteresis, respectively. Compared with the normal comparator, the hysteresis comparator shows a stable state and anti-noise ability. Due to the frequency limitation of interference signal generator, the sawtooth noise-signal are produced at 100 kHz.

The AC characteristics of the hysteresis comparator illustrate the pulse modulation with various reference voltages, as shown in Fig. 11. By adjusting V_{REF}, the duty cycle can be tuned from 50% to 90%, due to the limitation of hysteresis. The hysteresis comparator features a wave-shaping ability, that can obtain a steep rectangular wave. This shaping ability provides strong reliability to resist overshoot spikes and signal noise. Moreover, Fig. 12 demonstrates the transfer curves obtained from 25 °C to 250 °C with very small deviation, confirming the thermal reliability of the hysteresis comparator.

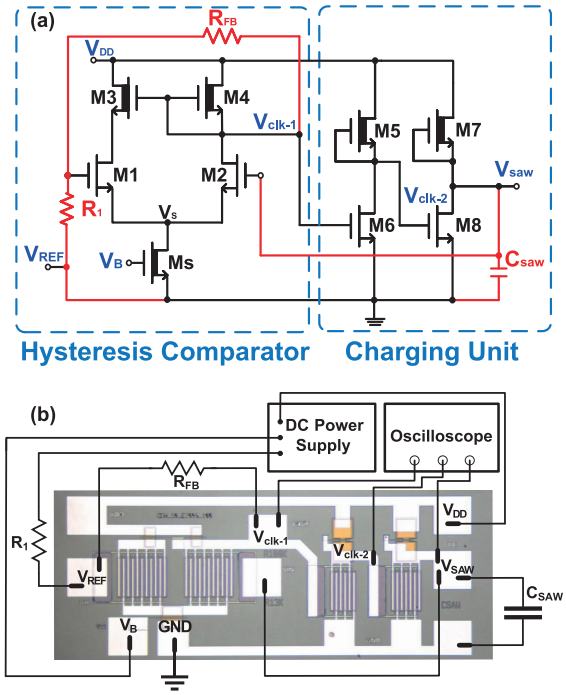

Fig. 13. (a) Circuit schematic of the GaN MIS-HEMTs sawtooth generator and (b) Measurement setup.

Based on the square output characteristics, the hysteresis comparators have been widely used in wave shaping circuits and pulse generator.

V. Sawtooth Generator

The sawtooth generator has two blocks, a hysteresis comparator followed by a charging unit, with positive feedback from comparator output (V_{clk-1}) and negative feedback from sawtooth generator output (V_{saw}), shown in Fig. 13 (a). The measurement setup is illustrated in Fig. 13 (b), where the sawtooth waveform generator is composed of the circuit on GaN chip and off-chip passive part. The GaN comparator in Fig. 13 (b) has the same transistor sizes as in Fig. 3.

The GaN D-mode devices M5 and M7 ($W_g = 10\ \mu m$) work as the loads while the E-mode devices M6 and M8 ($W_g = 1000\ \mu m$) act as input drivers. The output of the hysteresis comparator is applied to the charging unit, and the signal is enhanced by a two-level inverter. When $V_{clk\text{-}1}$ is logic-high, DC supply charges the capacitor until the V_{saw} reaches the crossover voltage (V_{th+}), which toggles the output to logic low. When $V_{clk\text{-}1}$ is logic-low, the capacitor can be discharged, decreasing the V_{saw} to the crossover voltage ($V_{th\text{-}}$), then another charge-discharge cycle starts [6, 28]. Consequently, the periodic sawtooth waveforms are generated, and the charging and discharging speeds are determined by the charging current through M7 and discharging current through M8, respectively. The oscillation generates a specific frequency sawtooth signal, which can be expressed as

$$f = \frac{1}{T_1 + T_2} \tag{5}$$

where T_1 is the charging time and T_2 is the discharging time, which can be deduced as:

$$T_1 = \frac{C_{saw}\Delta V}{\overline{I_c}} \tag{6}$$

$$T_2 = \frac{C_{saw}\Delta V}{\overline{I_{dis}}} \tag{7}$$

where $\bar{I}_c$ is the average charging current determined by M7, and the average discharging current $\bar{I}_{dis}$ is determined by M8. The charging and discharging time ratio can be tuned by output currents of M7/M8 to obtain the sawtooth signals with various shapes. Hence,

$$f = \frac{1}{C_{saw}\Delta V} \cdot \frac{\overline{I_c} \cdot \overline{I_{dis}}}{\overline{I_c} + \overline{I_{dis}}} \tag{8}$$

Based on equation (5)-(8), the increase of current reduces charge/discharge time, leading to a rise in frequency. The symmetry of the sawtooth waveform is related to the charging time T_1 and discharging time T_2.

This approximately 501.2 kHz frequency is tuned by capacitor C = 2.5 nF and $R_1/R_{FB} = 50\ k\Omega/100\ k\Omega$ based on equation (8). The signal amplitude can be adjusted by the ratio, which is equal to ΔV of the hysteresis comparator. A higher ratio achieves greater amplitude but reduces the control ability of reference voltage. Therefore, the sawtooth generator circuit satisfies the measurement to get the high ratio of R_1/R_{FB}. Fig. 14 shows the characteristics of the sawtooth generator, including sawtooth signal V_{saw} and hysteresis output $V_{out\text{-}Hy}$ at 500 kHz. The modulated $V_{th,D}$ ensures the wide comparison range in the comparator circuit and large sawtooth signal amplitude ΔV. The more negative voltages of $V_{th,D}$ in No.1 and No.2 circuits limit the sawtooth-signal operating states, which gives distorted waveforms. By contrast, the more standard and rectangular waveforms in No.3 circuit provide accurate regulation in both the charge and discharge process and thus gives the highest output amplitude of 6.1 V. Moreover, the $V_{th,D}$ can affect the charging time by the current in M7. The increase of $V_{th,D}$ can reduce the charging current of M7 so the charging/discharging ratio varies, resulting in a different symmetry in the output waveform.

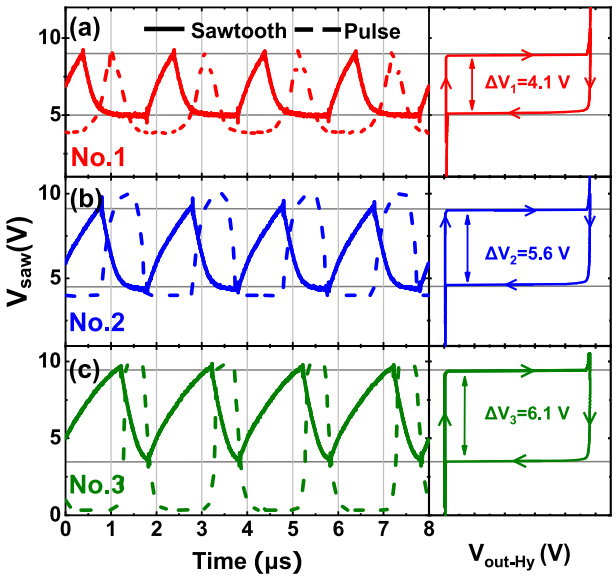

Fig. 14. Dynamic waveforms of the sawtooth generator at 500 kHz (dash line: $V_{clk\text{-}2}$) and DC performance of hysteresis comparator with No.1/No.2/No.3 circuits and hysteresis amount are ΔV_1= 4.1 V, ΔV_2= 5.6 V, and ΔV_3= 6.1 V.

For high-temperature tests in Fig. 15 (a), the signals in the No.3 circuit produce the stable amplitude of 6.1, 6.0, 5.9, 5.7, 5.6, 5.5 V from RT, 50 °C to 250 °C, respectively with 50 °C/step. The modulated comparator circuit shows the suppression temperature drift to produce the stable clock pulse, leading to high amplitude in the sawtooth generator circuit. Although high-temperature tests show a slight reduction of frequency due to the degradation of current, the circuit still maintains a large amplitude for 5.5 V and frequency of 420 kHz at 250 °C, as shown in Fig. 15 (b). Meanwhile, in the charging unit, the ratio of charging and discharging time has a slight variation because of current degradation at different temperatures based on equation (8), which leads to the waveform symmetry varying in an acceptable range. Thus, the logic sawtooth generator shows stable high-temperature output characteristics. For GaN sawtooth generator circuits, a large gate swing in MIS-HEMT allows a high input voltage so that the level shifter between stages is not necessary. This topology provides more compact solution for signal conversion and power converter. The charging unit with a two-level inverter guarantees the same phase and stable output, which isolates two units and provides controllable charging/discharging currents. Moreover, the sawtooth generator shows good thermal reliability, leading to the high-temperature applications in mixed-signal electronic systems.

VI. Conclusion

The comparator, hysteresis comparator and sawtooth generator have been fabricated using E-mode MIS-HEMT technology with successful operation at high temperatures up to 250 °C. The threshold voltage modulation of D-mode MIS-HEMTs improves comparison range as well as voltage swing of associated circuits while producing high amplitude output in the sawtooth generator. The circuits also exhibit

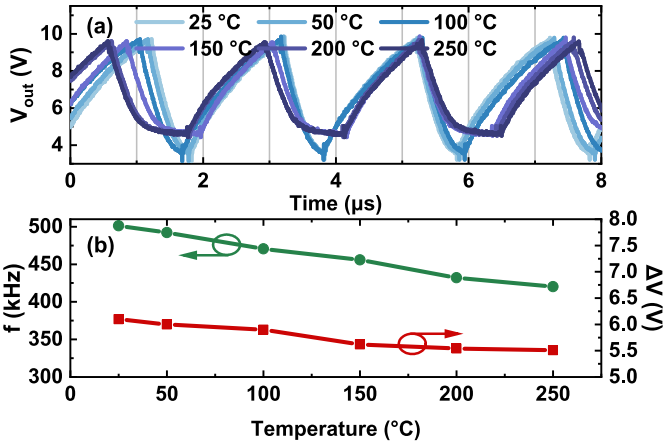

Fig. 15. High-temperature tests (a) GaN MIS-HEMTs sawtooth generator from RT, 50 ℃ to 250 ℃ with 50 ℃/step. (b) The frequency and ΔV versus temperatures. From RT to 250 ℃, the frequencies observed are 501.2, 492.3, 470.5, 455.7, 432.2, and 420.1 kHz; the ΔV are 6.1, 6.0, 5.9, 5.6, 5.5 and 5.5 V.

high-temperature reliability. Furthermore, the results prove the feasibility of GaN MIS-HEMTs for all-GaN monolithic integration to realize compact solutions for power conversion and mixed-signal processing.

REFERENCES

[1] K. J. Chen et al., "GaN-on-Si Power Technology: Devices and Applications," *IEEE Transactions on Electron Devices,* vol. 64, no. 3, pp. 779-795, Mar. 2017, doi: 10.1109/ted.2017.2657579.

[2] R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. A. Khan, and M. S. Shur, "High-temperature performance of AlGaN/GaN HFETs on SiC substrates," *IEEE Electron Device Letters*, vol. 18, no. 10, pp. 492-494, Oct. 1997, doi: 10.1109/55.624930.

[3] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707-719, Sept. 2016, doi: 10.1109/jestpe.2016.2582685

[4] A. M. H. Kwan, X. Liu, and K. J. Chen, "Integrated gate-protected HEMTs and mixed-signal functional blocks for GaN smart power ICs," in *2012 International Electron Devices Meeting*, Dec. 2012, pp. 7.3.1-7.3.4, doi: 10.1109/IEDM.2012.6478997.

[5] X. Liu and K. J. Chen, "GaN Single-Polarity Power Supply Bootstrapped Comparator for High-Temperature Electronics," *IEEE Electron Device Letters*, vol. 32, no. 1, pp. 27-29, Jan. 2011, doi: 10.1109/led.2010.2088376.

[6] H. Wang, A. M. H. Kwan, Q. Jiang, and K. J. Chen, "A GaN Pulse Width Modulation Integrated Circuit for GaN Power Converters," *IEEE Transactions on Electron Devices*, vol. 62, no. 4, pp. 1143-1149, Apr. 2015, doi: 10.1109/ted.2015.2396649.

[7] R. Sun, Y. C. Liang, Y.-C. Yeo, C. Zhao, W. Chen, and B. Zhang, "All-GaN Power Integration: Devices to Functional Subcircuits and Converter ICs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 31-41, Mar. 2020, doi: 10.1109/jestpe.2019.2946418.

[8] A. M. H. Kwan, Y. Guan, X. Liu, and K. J. Chen, "Integrated Over-Temperature Protection Circuit for GaN Smart Power ICs," *Japanese Journal of Applied Physics*, vol. 52, no. 8S, May 2013, doi: 10.7567/jjap.52.08jn15.

[9] J. Roberts, G. Klowak, D. Chen, and A. Mizan, "Drive and protection methods for very high current lateral GaN power transistors," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, May 2015, pp. 3128-3131, doi: 10.1109/APEC.2015.7104798.

[10] Z. Tang et al., "600-V Normally Off SiN_x/AlGaN/GaN MIS-HEMT With Large Gate Swing and Low Current Collapse," *IEEE Electron Device Letters*, vol. 34, no. 11, pp. 1373-1375, Sept. 2013, doi: 10.1109/LED.2013.2279846.

[11] S. Sheppard, "Switch mode power amplifier using MIS-HEMT with field plate extension," ed: Google Patents, 2009.

[12] H. Li, X. Li, Z. Zhang, C. Yao, and J. Wang, "Design consideration of high power GaN inverter," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Dec. 2016, pp. 23-29, doi: 10.1109/WiPDA.2016.7799904.

[13] M. Meneghini et al., "Trapping and Reliability Assessment in D-Mode GaN-Based MIS-HEMTs for Power Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2199-2207, Jul. 2014, doi: 10.1109/TPEL.2013.2271977.

[14] Q. Jiang, Z. Tang, C. Liu, Y. Lu, and K. J. Chen, "A High-Voltage Low-Standby-Power Startup Circuit Using Monolithically Integrated E/D-Mode AlGaN/GaN MIS-HEMTs," *IEEE Transactions on Electron Devices*, vol. 61, no. 3, pp. 762-768, Mar. 2014, doi: 10.1109/ted.2014.2298459.

[15] Y. Wang et al., "High output swing monolithic inverter with E-D mode MIS-HEMTs for GaN power integrated circuits," in *2015 IEEE 11th International Conference on Power Electronics and Drive Systems*, Jun. 2015, pp. 585-588, doi: 10.1109/PEDS.2015.7203460.

[16] Y. Zhang, M. Sun, S. J. Joglekar, T. Fujishima, and T. Palacios, "Threshold voltage control by gate oxide thickness in fluorinated GaN metal-oxide-semiconductor high-electron-mobility transistors," *Applied Physics Letters*, vol. 103, no. 3, p. 033524, Jun. 2013, doi: 10.1063/1.4815923.

[17] Q. Zhou et al., "Threshold voltage modulation by interface charge engineering for high performance normally-off GaN MOSFETs with high faulty turn-on immunity," in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jul. 2016, pp. 87-90, doi: 10.1109/ISPSD.2016.7520784.

[18] C. Chen et al., "Threshold voltage modulation mechanism of AlGaN/GaN metal-insulator-semiconductor high-electron mobility transistors with fluorinated Al2O3 as gate dielectrics," *Applied Physics Letters*, vol. 100, no. 13, p. 133507, Mar. 2012, doi: 10.1063/1.3699029.

[19] Y. Cai, Z. Cheng, Z. Yang, C. W. Tang, K. M. Lau, and K. J. Chen, "High-Temperature Operation of AlGaN/GaN HEMTs Direct-Coupled FET Logic (DCFL) Integrated Circuits," *IEEE Electron Device Letters*, vol. 28, no. 5, pp. 328-331, May 2007, doi: 10.1109/led.2007.895391.

[20] Z. Xu et al., "High Temperature Characteristics of GaN-Based Inverter Integrated With Enhancement-Mode (E-Mode) MOSFET and Depletion-Mode (D-Mode) HEMT," *IEEE Electron Device Letters*, vol. 35, no. 1, pp. 33-35, Dec. 2014, doi: 10.1109/LED.2013.2291854.

[21] B. R. Gregoire Jr, "Bandgap voltage reference using differential pairs to perform temperature curvature compensation," ed: Google Patents, 2003.

[22] C. Buttay et al., "State of the art of high temperature power electronics," *Materials Science and Engineering: B*, vol. 176, no. 4, pp. 283-288, Mar. 2011, doi: 10.1016/j.mseb.2010.10.003.

[23] M. Kanamura et al., "Enhancement-Mode GaN MIS-HEMTs With n-GaN/i-AlN/n-GaN Triple Cap Layer and High- k Gate Dielectrics," *IEEE Electron Device Letters*, vol. 31, no. 3, pp. 189-191, Feb. 2010, doi: 10.1109/LED.2009.2039026.

[24] Y. Cai, Y. Zhou, K. M. Lau, and K. J. Chen, "Control of threshold voltage of AlGaN/GaN HEMTs by fluoride-based plasma treatment: From depletion mode to enhancement mode," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2207-2215, Aug. 2006, doi: 10.1109/TED.2006.881054.

[25] F. Centurelli, R. Luzzi, M. Olivieri, and A. Trifiletti, "A bootstrap technique for wideband amplifiers," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 10, pp. 1474-1480, Nov. 2002, doi: 10.1109/TCSI.2002.803359.

[26] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *2008 IEEE Asian Solid-State Circuits Conference*, Dec. 2008, pp. 269-272, doi: 10.1109/ASSCC.2008.4708780.

[27] M. Cui et al., "Monolithic integration design of GaN-based power chip including gate driver for high-temperature DC–DC converters," *Japanese Journal of Applied Physics*, vol. 58, no. 5, p. 056505, Apr. 2019, doi: 10.7567/1347-4065/ab1313.

[28] X. Li, M. Cui, and W. Liu, "A full GaN-Integrated Sawtooth Generator based on Enhancement-mode AlGaN/GaN MIS-HEMT for GaN Power Converters," in *2019 International Conference on IC Design and Technology (ICICDT)*, Jun. 2019, pp. 1-3, doi: 10.1109/ICICDT.2019.8790928.