Monolithic Integration of GaN DC-DC Converters: Technology and Characterization

by

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Abstract

High-temperature (HT) power converters are increasingly important in extreme environments, such as electric vehicles, aviation, etc. Due to the limited temperature operation beyond 150 °C in Si-based devices, GaN-based power transistors are expected to be excellent candidates for power converters at high temperatures over 200 °C in electric vehicle applications. HT power converters with self-contained functionality (power, driver, microcontroller, sensors, etc.) without external heatsink or cooling systems are increasingly essential owing to reduced size and cost. The lateral AlGaN/GaN-based high electron mobility transistors (HEMTs) have been regarded as promising candidates in high frequency, high power density, and HT applications. GaN smart power integrated circuit (IC) provides an effective solution to achieve a system-on-chip scheme for HT power converters. This thesis uses normally-off GaN transistors with a recessed metal-insulated-semiconductor (MIS) gate, and it focuses on the development of GaN DC-DC converters with integrated gate drivers for HT power converters in extreme environments.

To evaluate the recessed MIS gate for high-temperature GaN power converters, the impact of etch depth on the performance of mobility and R_{ON} is systematically studied at high temperatures. The mechanisms of carrier scattering are discussed at different etch depths, and full recess with dielectric engineering is proposed to improve the stability of GaN IC.

On the lateral GaN smart power IC technology platform, this thesis focuses on three

parts for HT power converters including 1) an integrated gate driver for a GaN boost converter; 2) integrated gate drivers with a half-bridge stage for a synchronous GaN buck converter; 3) an integrated technique of deadtime management for a synchronous GaN buck converter. Firstly, the GaN boost converter with the optimized gate driver exhibits a voltage conversion from 5 to 11 V at 100 kHz, and only 11% reduction of output voltage is observed at high temperatures up to 250 °C. Then, the synchronous GaN buck converter with an integrated half-bridge stage achieves a voltage down-conversion with an input voltage of 25 V, and it shows good thermal stability and almost no reduction of output voltage at temperatures up to 250 °C, with a large gate swing of 10 V. Lastly, an integrated GaN buck converter with a no deadtime technique (NDT) exhibits a maximum efficiency of 80 % at high temperatures up to 250 °C , with an input voltage of 30 V at 100 kHz. At high temperatures, the optimized GaN NDT converter shows better performance than a synchronous GaN buck converter with a fixed deadtime technique (FDT) at high load currents, in terms of smaller voltage overshoots and oscillations of gate drivers and better converter efficiency as well. The proposed GaN NDT converter uses one control signal and provides a simple and effective method of deadtime management for high-temperature power converters.

摘要

发展高温高效功率转换器用于极端高温环境（比如汽车电子、航空等）是目前研究的热点和难点。由于无需外部散热装置或冷却系统可以极大的减小尺寸和降低成本，开发具有独立功能（电源、驱动器、微控制器、传感器等）的高温功率转换器越来越受到科研和产业界的重视。传统 Si 基功率器件的使用温度一般不高于 150 °C，基于横向氮化铝镓和氮化镓异质结的高电子迁移率晶体管（AlGaN/GaN-HEMT）具有更高开关速度、高功率密度和耐高温等优势，被认为是开发工作温度高于 200°C 转换器的有力竞争者之一。同时，氮化镓智能功率集成电路可以实现了单片系统集成和高功率密度的集成，具有高功率密度、耐高温和小型化轻量化等优势。论文采用常关型凹槽栅氮化镓晶体管，主要研究集成驱动的高温氮化镓功率转换器在极端环境的应用。

为了评估凹槽栅氮化镓功率转换器高温性能，该论文首先系统地研究了在高温下蚀刻深度对迁移率和 R_{ON} 性能的影响，讨论了在不同的蚀刻深度下载流子散射的机制。为了提高氮化镓集成电路的稳定性，本论文推荐采用完全势垒刻蚀以及栅介质优化结合的技术。

本文着眼于单片集成更多的功能模块和功率氮化镓器件的高温转换器的研究。采用横向异质结氮化镓功率集成电路系统，本文主要内容着重于三个部分，包括：1）集成栅极驱动电路的氮化镓升压转换器的研究；2）集成驱动电路的氮化镓半桥同步降压转换器的研究；3）集成死区时间控制技术的氮化镓同步降压转换器的研究。首先，集成驱动电路的氮化镓升压转换器实现了 100 kHz 频率下 5 到 11 伏的电压升压转换，在 250 °C 输出电压只有 11%的降低。其次，集成半桥氮化

镓同步降压器可以实现 25 伏的电压降压转换，并且在 250 °C 高温下显示出良好的热稳定性，输出电压基本上没有变化。最后，该论文成功实现了一种单片集成无死区时间技术的氮化镓同步降压转换器，可以实现 30 伏的电压降压转换，并且在 250 °C 时的最高效率可以达到为 80％。该转换器比具有固定死区时间的氮化镓同步降压转换器表现出更好的性能，它具有较小的栅极电压过冲和振荡，并且在高温高负载电流下的转换效率更高。该转换器为高温功率转换器提供了一种简单有效的死区时间管理方法。

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List of Symbols

C_{ox}	Oxide capacitance
C_{br}	AlGaN capacitance
D	Duty cycle
D_{etch}	Etch depth
D_{T1}	First deadtime
D_{T2}	Second deadtime
V_{th}	Threshold voltage
ε_0	Permittivity of vacuum
ε_0	Relative Permittivity
f	Frequency
g_m	Transconductance
I_{DS}	Drain current
$I_{DS,Max}$	Maximum drain current
n_s	2DEG carrier density
k	Boltzmann constant
T	temperature
μ	Mobility
μ_B	Bulk mobility
μ_C	Coulomb scattering
μ_{po}	Polar-optical phonon scattering
μ_{ac}	Acoustic phonon scattering
μ_{ph}	Phonon scattering

μ_{SR}	Surface roughness scattering
μ_D	Effective mobility in D-mode device
μ_E	Effective mobility in E-mode device
η	Converter efficiency
R_{ON}	On-state resistance
M	Conversion ratio
V_{BT}	Bootstrap voltage
V_{IH}	Input logic high voltage
V_{IL}	Input logic low voltage
V_{OH}	Output high voltage
V_{OL}	Output low voltage
V_F	Forward voltage
i_L	Inductor current
$V_{th,D}$	Threshold voltage of D-mode device
$V_{th,E}$	Threshold voltage of E-mode device
V_{PWM}	Voltage of PWM signal
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
τ_{rise}	Rise time
τ_{fall}	Fall time
NM_H	Logic-high noise margin
NM_L	Logic-low noise margin

List of Abbreviations and Acronyms

2DEG	Two-dimensional electron gas
ADS	Advanced design system
AFM	Atomic force microscope
ALD	Atomic layer deposition
AlGaN	Aluminum gallium nitride
C-V	Capacitance-voltage
DCFL	Direct-coupled field logic
D-mode	Depletion mode
E-mode	Enhancement mode
HEMT	High electron mobility transistor
HFET	Heterojunction field effect transistor
MIS	Metal insulator semiconductor
HT	High-temperature
FDT	Fixed deadtime technique
NDT	No deadtime technique
RTA	Rapid thermal anneal
SOI	Silicon on insulator
TDDB	Time dependent dielectric breakdown
PCB	Printed circuit board
PECVD	Plasma enhanced chemical vapor deposition
IC	Integrated circuit
I-V	Current-voltage

WBG	Wide bandgap
VTC	Voltage transfer curve

Chapter 1 Introduction

It is recognized that high-temperature (HT) power converters are becoming increasingly important in applications under extreme environments, such as electric vehicles, aviation, and oil drilling. For electric vehicles, the ambient temperature of the hood is usually 150 °C, and the temperature near the engine can even reach 200 °C. Si-based devices can only work at temperatures below 150 °C. However, the superior material properties of wide bandgap devices are expected to be excellent candidates for power converters at high temperatures over 200 °C in electric vehicle applications. GaN is considered to be an ideal candidate for high-temperature, high-power, and high-frequency applications [1]. The external cooling components like the heat sink, air, or liquid cooling system, can add undesired size and weight to the systems. HT electronics with self-contained functionality (power, drivers, communications, signal processing, microactuator control, etc.) are required [2]. GaN-based power integration provides an effective solution in achieving high frequency, and high power density of power converters for HT electric vehicle applications.

1.1 Background of power DC-DC converters

DC-DC converters are widely used in power electronics, and they are basically used to converter a given DC voltage to a desired value.

1.1.1 Categories of Non-isolated DC-DC converter

Depending on whether or not an output transformer is used, power DC-DC converters are classified as isolated or non-isolated. Non-isolated DC-DC converters can be used to achieve step-up or step-down voltage conversion, which reduce the size, weight, and increase the efficiency of power converters owing to the lack of a high-frequency transformer [3].

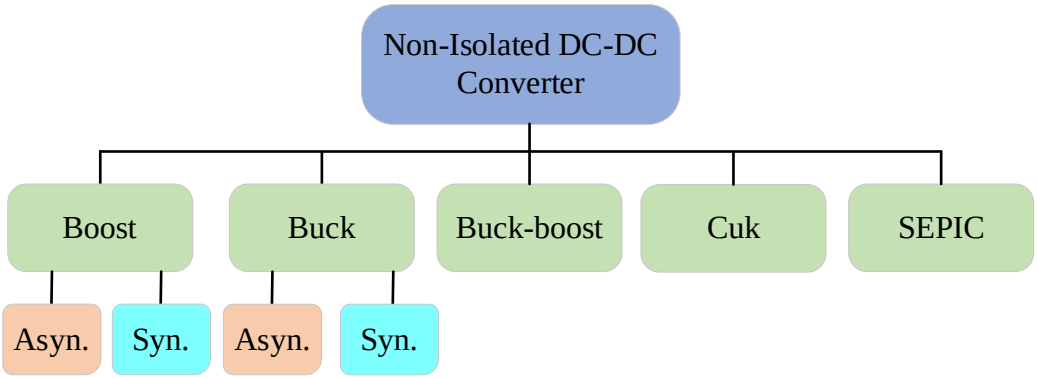


Fig.1.1.1 Classification of Non-isolated DC-DC converter topologies.

The topologies of non-isolated DC-DC converter have boost, buck, buck-boost, Cuk, SEPIC, as shown in Fig.1.1.1. The boost and buck converters are two basic topologies, and the buck-boost, Cuk, and SEPIC converters are based on these two topologies. Fig.1.1.2 shows the circuit diagrams of boost and buck converters.

1) Boost converter

The boost converter in Fig.1.1.2 (a) steps up the low input voltage to a high-level output voltage. During switching-on conduction of power transistor S, the conduction mode capacitor C delivers its energy to the load; during the switching-off time, the energy stored in the inductor L supplies the output consisting of the capacitor C and

the load R.

2) Buck converter

The topology in Fig.1.1.2 (b) is known as a buck converter because it steps down the average output voltage below the input voltage. During the switching-on of the power transistor S, the inductor current i_L will be charging through V_{IN}, and the inductor current i_L will be discharged through the diode D during the switching-off state.

(3) Asynchronous (Asyn.) converter and synchronous (Syn.) converter

In Fig.1.1.2, the asynchronous converter uses only one power switch, the diode D conducts the currents during the switching-off time. Replacing the diode D with a power FET transistor, the synchronous converter with a half-bridge scheme is an important topology and widely used for both its step-up and step-down converters. This synchronous converter has better efficiency owing to smaller conduction loss of the power transistor than the diode. This thesis focuses on the studies of two basic non-isolated buck and boost converters, including asynchronous and synchronous topologies.

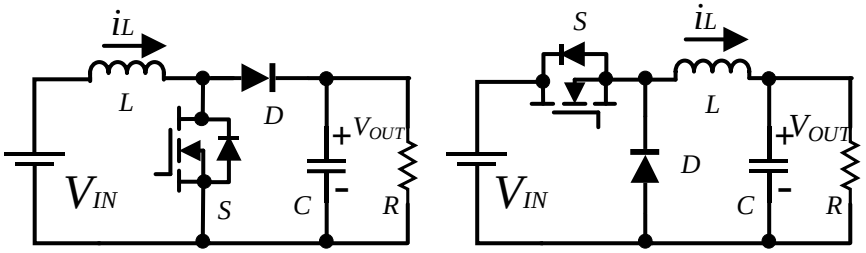


Fig.1.1.2 Circuit diagrams of classic topologies of non-isolated converters. (a) Boost converter, (b) buck converter.

1.1.2 Converter design considerations

In recent years, considerable interest is building up of power DC-DC converters in the industry and research centers in power conversion applications. Great efforts are concentrating towards specialized improvement in conversion efficiency, power density, high frequency, control techniques, simplicity, and cost of converters [4]. Fig.1.1.3 gives the metrics and key parameters of power DC-DC converters. The design of different parameters is the key to the performance improvement of converters. Typically a power DC-DC converter includes the following major components:

1) Active device

Efficiency is one of the key metrics, which determines the effectiveness of power converters. From the device point of view, the power transistor with low on-state resistance (R_{ON}) can reduce conduction loss and improve converter efficiency, and increase power density owing to reduced transistor sizes. The channel mobility is the main factor in achieving high-frequency power converters. The low output capacitance (C_{OSS}) and input capacitance (C_{ISS}) are other factors that impact the efficiency due to reduced switching loss of power converters.

2) Integrated circuits (control and driver circuits, topology, and interconnection parasitics)

Control and driver circuits are essential elements for power converters, and the gate driver should consider the required driving voltage and avoid spurious switching events during both turn-on and turn-off transients. Proper control and driver design are required to improve the efficiency of power converters and avoid false turn-on loss and

short circuits, especially in high-frequency applications. The monolithic integration circuits enable to improve the efficiency of DC-DC converters at a higher frequency, owing to the reduction of parasitics and system size.

There are numerous isolated DC-DC converter topologies proposed in the literature owing to high-voltage gain by increasing the turns ratio of the high-frequency transformer. The non-isolated DC-DC converters without high-frequency transformers are better choices to increase efficiency owing to reduction of size, weight, and volume [3], which are essential for applications where galvanic insulation is not a must. In the synchronous topology, the power field-effect transistor (FET) replaces output diodes and increases the efficiency of DC-DC converters owing to reduced on-state resistance and conduction loss of power transistors.

3) Passive component

Passive filter parameters (L and C) can affect dynamic behavior, efficiency, and weight of a DC-DC converter. The output filter inductor L operates as a filter component to reduce the ripple at the output side, resulting in an increase in the converter efficiency [4]. The sizing and design of the output filter [5-7] were reported to reduce the ripple and weight for power converters. Moreover, core materials-induced inductor losses at high switching frequencies are the main causes of the inductor losses than lower inductance values. Low-pass input filter [8], coupled-magnetic filter [9], and high-frequency transformer [10, 11] are reported to improve the performance of power converters. Inductor L and capacitor C are required to be optimized to achieve stable output voltage with small voltage ripples.

4) Thermal management

As the power density of a power converter is increased, thermal issues play an important role in reliability. The excessive temperatures of critical components cause most equipment failures [12]. Moreover, the high-temperature environment also addresses the importance of thermal management and cooling when designing power transistors and converters in the industry. A detailed power converter design including thermal management is illustrated in [12]. Under extreme environments or high power density applications, external heatsink or cooling system are effective solutions to manage the thermal budget in power converters. However, these cause additional weight and cost, proper thermal design is required according to the required power density or high-temperature applications. The semiconductor with good thermal conductivity is highly required owing to high-temperature characteristics and low cost of thermal management.

This thesis focuses on the design of power DC-DC converters for high-temperature applications in electric vehicles, which is based on two aspects including device and circuit. (1) From characterization of device, the temperature-dependent mobility and on-state resistance R_{ON} are studied to investigate the thermal degradation of power converters at high temperatures. (2) From circuit level, the monolithic integration of gate driver circuit and control circuit is achieved on one chip, which can reduce the parasitics of interconnection; different topologies are designed to improve the performance of power converters.

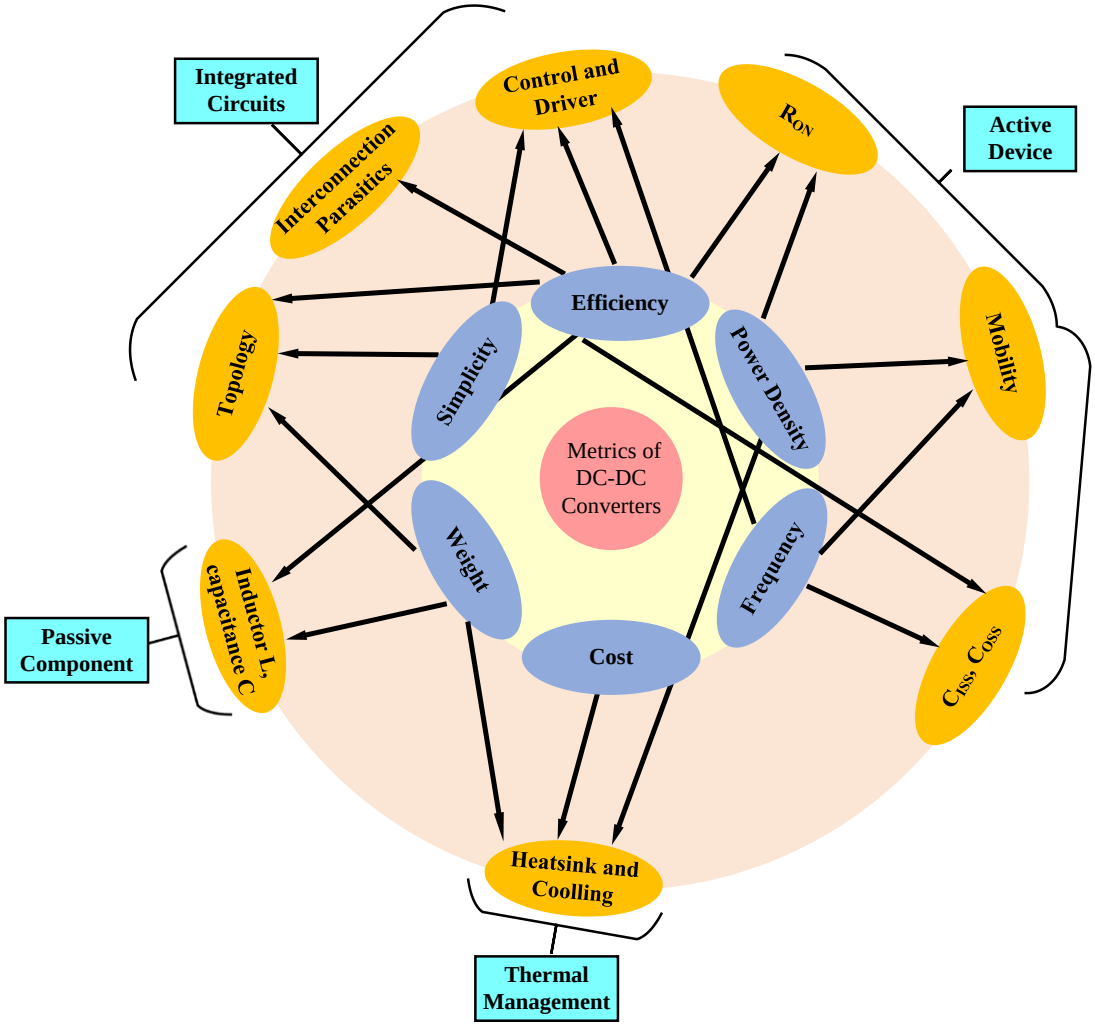


Fig.1.1.3 Illustration of metrics and key parameters of power DC-DC converters.

1.2 Lateral GaN devices for power converters

1.2.1 GaN III-V semiconductors

Compared with Si and SiC materials in Table 1. 1, GaN material is a unique III-V system, which has a large bandgap energy of 3.4 eV. GaN has been extensively used as optoelectronics, such as LEDs and laser diodes, since the invention of high-brightness blue LEDs by Nichia in 1993. GaN has superior electron density (≈ 1 x 10^{13} cm^{-2}) and high electron mobility in hetero-structure (1200~2000 cm^2/Vs), which promotes GaN

to be an attractive candidate for high frequency and high efficiency power electronics.

Table 1. 1 Physics properties of GaN compared with Si, GaAs, and SiC

Material	E_g (eV)	ε	μ_n (cm^2/Vs)	E_c (MV/cm)	V_{sat} (10^7cm/s)	*K* (W/cm.K)
Si	1.12	11.8	1400	0.23	1.0	1.5
GaAs	1.43	13.1	600	0.5	1.0	0.5
SiC	3.26	10	950	2.2	2.0	4.5
GaN	3.4	9.5	1500	3.0	2.5	>1.5

E_g, bandgap energy; ε, dielectric constant; μ_n, electron mobility; E_c, critical electrical field; V_{sat}, saturation velocity; *K*, thermal conductivity.

All semiconductors contain intrinsic electrons and holes, the semiconductor devices can be effective only if the intrinsic carrier concentration is at least one order less than doping carrier concentration. The intrinsic carrier concentration n_i of a semiconductor varies exponentially with temperature [13] using equation (1.1)

$$n_i = \sqrt{N_C N_V}\exp\left(-\frac{E_g}{kT}\right) \tag{1.1}$$

Where N_C is the carrier density in the conduction band, N_V is the carrier density in the valence band, E_g is the bandgap energy of the semiconductor, T is the temperature, and k is Boltzman's constant. Fig.1.2.1 shows the intrinsic carrier concentration versus temperature in various semiconductors. At room temperature, the doping level for Si devices is around 10^{15} cm^{-3}, and the intrinsic carrier concentration is around 10^{10} cm^{-3}. But this intrinsic value is up to 10^{14} cm^{-3} at 150 °C, which indicates that Si devices can only operate below 150 °C. Both SiC and GaN WBG devices can work at high temperatures beyond 600 °C owing to low intrinsic carrier concentration, indicating excellent properties for electric vehicle systems at temperatures over 200 °C.

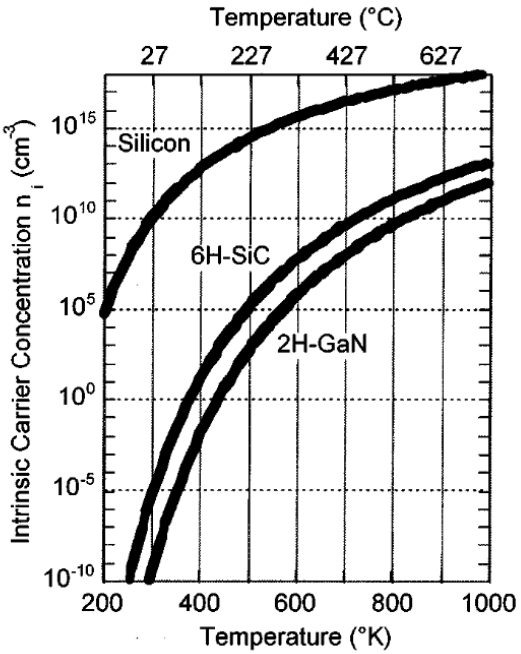


Fig.1.2.1 Intrinsic carrier concentration versus temperature in various semiconductors [2].

The unique hetero-structure GaN high-electron-mobility transistor (HEMT) has been an important technology in GaN power devices since the early beginning of HEMT in GaN by Mimura (1975) and M. A. Khan (1994). The lateral AlGaN/GaN HEMT has a high electron mobility of two-dimensional electron gas (2DEG), owing to the spatial separation of electrons from the body material. So, this combines high breakdown voltage (BV) and low on-state resistance R_{ON} in GaN-based HEMTs compared with Si and SiC devices. GaN-based power devices have been excellent candidates in high frequency, high power density, and high-temperature applications.

1.2.2 GaN E-mode technology

Due to the nature of the polarization of the hetero-structure, most AlGaN/GaN HEMTs demonstrated so far are normally-ON (depletion mode) with a negative threshold

voltage (V_{th}). The power applications require normally-OFF (enhancement mode, V_{th}>0) operation due to safety concerns. Various techniques have been developed to realize E-mode devices, such as gate recess [14], fluorine plasma treatment [15], and P-type cap layer [16]. Fig.1.2.2 shows some gate structures of these techniques to achieve E-mode operation, including P-doped GaN, P-doped AlGaN, F-based plasma treatment, recessed gate, insulated recessed gate, and hybrid MIS heterojunction-field-effect-transistor HFET [17]. Many manufacturers have invested in E-mode power devices, including EPC, GaN System, Panasonic, HRL, Navitas, Exagan, NEC, Powdec, Sanken, TSMC, and IMEC. The detailed parameters and process technology of these manufacturers are listed in Table 1. 2.

Most of these manufacturers have published papers to show their device structures, and explain how their devices achieve a positive threshold voltage. Fig.1.2.2 (a) presents a P-doped GaN structure, which utilizes holes from P-doped GaN to deplete the 2DEG electrons beneath the gate, and the threshold voltage is consequently shifted to a positive value. EPC employs this kind of technique, however, the Schottky gate of its E-mode devices produces a strict gate voltage limitation of no larger than 6 V. The P-doped AlGaN structure in Fig.1.2.2 (b) has a similar mechanism with the P-doped GaN gate, while the difference is that the holes in Fig.1.2.2 (b) are generated from the P-doped AlGaN layer. Panasonic used a P-doped AlGaN gate structure at an earlier stage, however, their latest x-GaN gate injection transistors (GITs) now utilize a P-doped GaN structure as seen in Fig.1.2.2 (a). IMEC also uses a P-doped GaN technique similar to that in Fig.1.2.2 (a), but on a different SOI substrate with trench isolation,

and the gate voltage is only tested at 7 V due to Schottky contact [18].

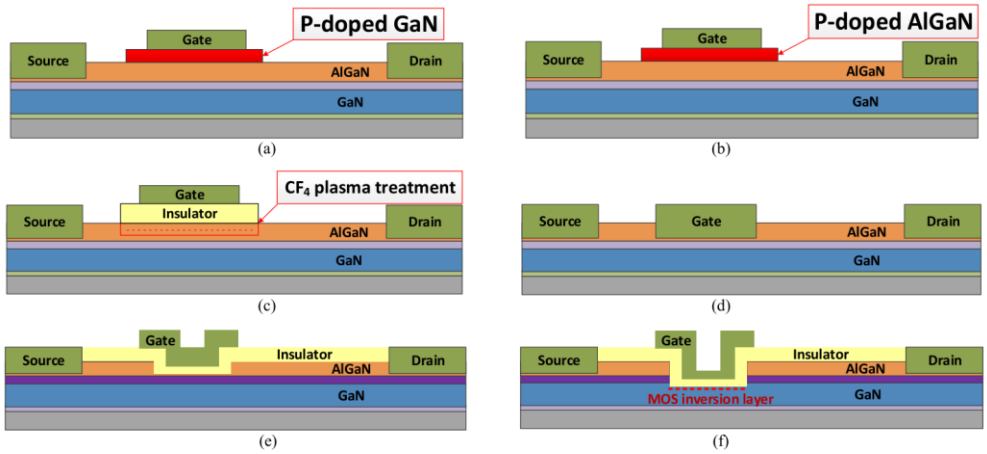


Fig.1.2.2 Gate modification techniques for E-mode GaN HFETs. (a) P-doped GaN, (b) P-doped AlGaN, (c) F-based plasma treatment, (d) Recessed gate, (e) Insulated recessed gate, (f) Hybrid MIS-HFET. [17]

The recessed gate structure is another significant technique to gain normally-OFF operation, and this is attributed to the reduced 2DEG density through the recessed thickness of the AlGaN barrier. Sanke uses a recessed Schottky gate structure, as shown in Fig.1.2.2 (d). The recessed gate is usually accompanied with an insulator, as shown in Fig.1.2.2 (e) and Fig.1.2.2 (f), to increase the threshold voltage and enlarge gate swing voltage. The difference between them is that the hybrid MIS-HFET in Fig.1.2.2 (f) requires full etching of the AlGaN barrier to remove 2DEG beneath the gate. Exagan and NEC make use of a recessed gate with an insulator in Fig.1.2.2 (e), the gate voltage can be performed up to 12 V due to the insertion of a gate insulator. Although HRL's earlier devices used an insulated gate with F-based plasma treatment in Fig.1.2.2 (c), HRL's later devices utilized a recessed gate with an insulator AlN as seen in Fig.1.2.2 (e). Then HRL licensed this technique to Navitas in 2015 [17], so Navitas should also employ a similar insulated recessed gate as shown in Fig.1.2.2 (e), but they focus on

lateral integration circuits of E-mode GaN technology. GaN system has not published its gate structure, but these devices appear to have an insulator [17], and the gate voltage can be operated up to 10 V.

Table 1. 2 Commercial E-mode devices

Manufacturer	**Technology**	**Process**	**Gate structure**	**$V_{GS,Max}$ (V)**	**Voltage rating (V)**	**Current (A)**
EPC **[19]**	GaN-on-Si	P-doped GaN	Fig.1.2.2 (a)	6	15, 30, 40, 60, 65, 80, 100, 120, 150, 200	0.5~ 90
GaN Systems **[20]**	GaN-on-Si	N. A.	N. A.	10	650 100	3.5-90
Panasonic **[16, 21, 22]**	GaN-on-Si	P-doped AlGaN P-doped GaN	Fig.1.2.2 (b) Fig.1.2.2 (a)	N. A.	650 600	5, 10, 15
HRL **[23, 24]**	GaN-on-Si	F-plasma treatment and insulator Recessed MIS gate	Fig.1.2.2 (c) Fig.1.2.2 (e)	3 6	1200 600	10 10
Navitas **[25]**	GaN-on-Si	Recessed MIS gate	Fig.1.2.2 (e)	N. A.	650	N. A.
Exagan**,** NEC **[26-28]**	GaN-on-Si	Recessed MIS gate	Fig.1.2.2 (e)	12	650 1200	100
Powdec **[29]**	GaN-on-Sapphire/ SiC	Integrated LDMOS and recessed gate	Fig.1.2.2 (d)	N. A.	1200	12
Sanken **[30]**	GaN-on-Si	Recessed gate without insulator	Fig.1.2.2 (d)	N. A.	600	N. A.
TSMC **[31, 32]**	GaN-on-Si	Electron-trapping technology with insulator	N. A.	12	100 650	N. A.
IMEC **[18]**	GaN-on-SOI	P-doped GaN	Fig.1.2.2 (a)	7	200	9

Powdec's E-mode devices have a recessed gate but with an integrated LDMOS transistor on the top, which is similar to a cascade structure but with a full integration

scheme. However, their devices are fabricated on a sapphire or SiC substrate with a high voltage rating of 1200 V. TSMC reported their E-mode devices on a CMOS-compatible GaN-on-Si process, they utilized an insulated gate without recessing the barrier layer, and the electron trapping can deplete 2DEG in the channel under high voltage off-state stress.

In Table 1.2, there are mainly three techniques for E-mode GaN power devices, F-plasma treatment, recessed gate, and P-doped GaN or AlGaN technique. For high-temperature power converters in electric vehicles, F-based plasma treatment suffers from high-temperature reliability issues; P-dope GaN or AlGaN gate has a large leakage current at high temperatures due to intrinsic p-n diode. In this thesis, the E-mode power device uses a recessed gate with an insulator owing to its reduced leakage current, especially at high temperatures. It can provide a large gate swing of more than 10 V, which provides strong noise immunity, especially at high switching frequencies.

1.3 GaN Integration Circuit (IC) for power converters

The power system roadmap in Fig. 1.3.1 [33] proposes two approaches toward high frequency, high power density applications. The first solution is called system-in-package (SIP), and it is targeted for high power module; the second monolithic solution system-on-chip (SOC) is recommended for low and mid power in electric vehicles.

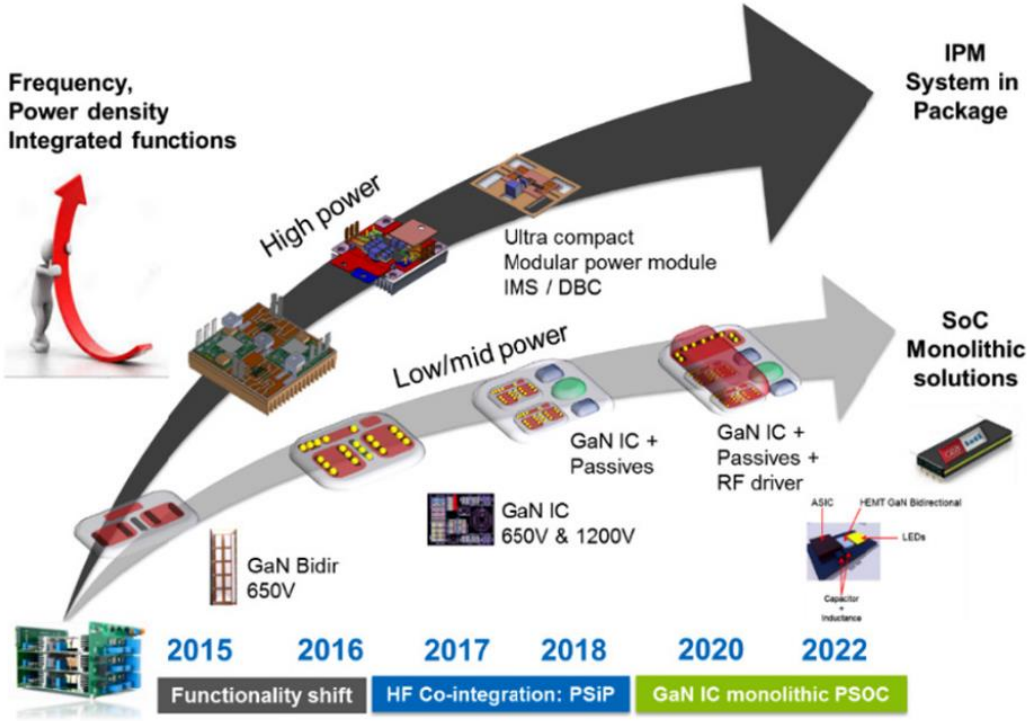


Fig. 1.3.1 Power system roadmap. System-on-chip (SOC) is targeted for low and mid power solutions, and system-in-package (SIP) for high power applications [33].

Power integration is essential for the full utilization of GaN material metrics in power conversion applications owing to high power density, small chip size, and cost reduction. The monolithic integration of GaN driver and GaN FET is critical for the high-frequency operation of larger than 1 MHz. The discrete components can cause noise and oscillation, which can easily damage GaN devices because GaN HEMTs normally have a limited gate voltage tolerance. On the other hand, compared with the Si-based driver, the integrated GaN driver has less power loss, better process compatibility, and a smaller chip size as well. This emphasizes the importance of an all-GaN integrated circuit (IC) on a single chip to deliver the required speed, efficiency, and robustness in power converters.

1.3.1 Status of GaN IC

Unlike Si CMOS technology, only n-type GaN transistors are readily available; the lack of p-type GaN transistors has been the major obstacle for GaN CMOS technology. However, there have been studies on GaN IC using n-type GaN transistors. The lateral channel makes AlGaN/GaN HEMTs good candidates for power IC, a design towards monolithic integration for low and mid-power applications is proposed using Metal Insulator Semiconductor (MIS) gate MIS-HEMTs [33]. A hybrid architecture using the recessed gate and an insulator was reported by many studies [23, 34] for enhancement (E-mode) devices. The recessed E-mode MIS-HFETs are excellent candidates for GaN-based power ICs, which can suppress gate leakage and provide strong immunity to large voltage overshoots or oscillations, especially in high-frequency power switching circuits. In this thesis, the recessed E-mode MIS-HFETs with a high-k Al_2O_3 layer is used to achieve GaN IC for GaN power converters.

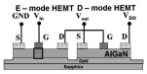
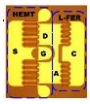
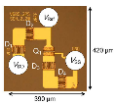
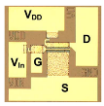
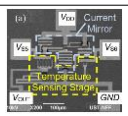
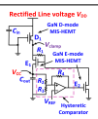
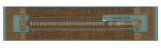
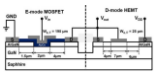
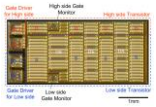
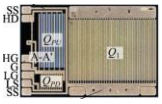
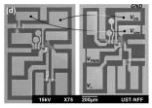
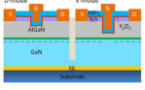
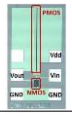
Table 1. 3 [35-65] shows the development of lateral GaN-based IC since 2006. Inverters are basic elements for power IC, and direct-coupled FET logic (DCFL) inverter is a typical inverter, which consists of an E-mode driver transistor and a D-mode transistor acting as an active resistor with source-drain connected. Studies have been reported to realize GaN-based DCFL inverters, and various E-mode techniques were used to fabricate inverters, including CF_4 plasma treatment [35, 36], recessed gate with insulators [44, 45, 49, 51], P-channel [50, 65], P-doped GaN [54], and P-doped GaN with H_2 plasma treatment [58]. Other GaN function blocks, such as voltage reference generator [39], comparator [40], protection circuit [41], start-up circuit [43],

and PWM circuit [48], were achieved by HKUST.

The integration of gate drivers and power transistors is essential to improve the efficiency of GaN power converters, owing to reduced parasitic inductance and chip size. There have been efforts to integrate gate drivers [46, 47, 53, 56, 57, 59, 62], SBD [37], and protection circuits [55, 61, 64] in GaN power converters. However, most of these converters were only measured at room temperature or with limited temperature operation below 150 °C, and this thesis will focus on GaN integrated circuit (IC) for high-temperature power converters above 200 °C, which will be discussed later.

Table 1. 3 indicates that GaN IC is now at the early stage of their development, and most results come from the research labs, and HKUST did a lot of work to achieve GaN function blocks. Since 2014, commercial companies have invested to fabricate GaN IC, and their efforts indicate a transition of GaN IC from lab research to mass production. In the early years, the studies focused on basic function blocks, like inverter, comparator, current/voltage sensors, etc. There have been increasing efforts of integrated converters with gate drivers and other protection circuits in recent 6 years. Table 1. 4 shows the detailed parameters of GaN ICs of commercial companies, and four companies have announced their ability to fabricate GaN ICs for power electronics. They are EPC, Panasonic, Navitas, and IMEC. These GaN ICs are specially designed for power converters including half-bridge, gate drivers, logic circuits, and more function blocks will be integrated into the package to achieve high frequency and high power density applications soon.

Table 1. 3 Development of lateral GaN-based Integrated Circuit (IC)

Year	Figure	Function	Technology	Process	Temperature	Authors
2006 2007		Inverter, oscillator	E-mode GaN-on-Sapphire	CF_4 plasma treatment	375 °C	HKUST [35, 36]
2009		Boost converter w/ SBD	E-mode GaN-on-Si	CF_4 plasma treatment	25 °C	HKUST [37]
2009		Inverters	E-mode GaN-on-Si	P-AlGaN	25 °C	Panasonic [38]
2010		Voltage generator	D-mode GaN-on-Si	HEMT	250 °C	HKUST [39]
2011		Comparator	E-mode GaN-on-Si	F implantation	250 °C	HKUST [40]
2013		Inverter w/ gate protection	E-mode GaN-on-Si	F implantation	25 °C	HKUST [41]
2014		Temperature sensor PTAT	E-mode GaN-on-Si	F implantation	275 °C	HKUST [42]
2014		High voltage start-up circuit	E-mode GaN-on-Si	F implantation and MIS-gate	25 °C	HKUST [43]
2014		Inverter, oscillator	E-mode GaN-on-Sapphire	Recessed MIS-gate	25 °C	NEDI [44]
2014		Inverter	E-mode GaN-on-Sapphire	Recessed MIS-gate	25 °C	PKU [45]
2014		Synchronous converter w/ gate driver	E-mode GaN-on-Si	P-AlGaN	25 °C	Panasonic [46]
2015		Gate driver	D-mode GaN-on-Si	Quasi-normally-off HEMT	25 °C	University of Stuttgart [47]
2015		PWM	E-mode GaN-on-Si	F implantation	200 °C	HKUST [48]
2016		Inverter, oscillator	E-mode GaN-on-SiC	Recessed MIS-gate	25 °C	UESTC [49]
2016		CMOS inverter	CMOS GaN-on-Si	P-channel	25 °C	HRL [50]

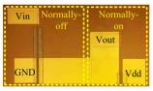
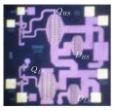
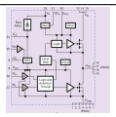
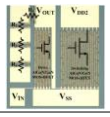
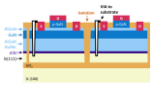
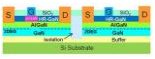
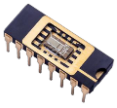
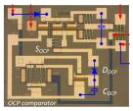
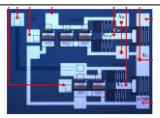
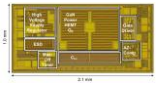
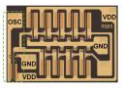
2016		Inverter oscillator	CMOS GaN-on-Si	Recessed MIS-gate	25 °C	NUS [51]
2016		Synchronous converter w/ gate drivers	E-mode GaN-on-SiC	N.A.	25 °C	University of Colorado [52]
2016		Synchronous converter w/ gate drivers	D-mode GaN-on-SiC	Qorvo TQGaN15	25 °C	University of Colorado [53]
2017		Inverter, oscillatior	E-mode GaN-on-Si	P-GaN	250 °C	HKUST [54]
2017		Synchronous converter w/ gate drivers and logic circuits	E-mode GaN FET	E-mode GaN FET	150 °C	Navitas [55]
2017		Gate driver	E-mode GaN-on-Si	Recessed MIS-gate	25 °C	Hongik University [56]
2018		Gate driver	E-mode GaN-on-SOI	P-GaN	25 °C	IMEC [57]
2019		Inverter oscillator	E-mode GaN-on-Si	P-GaN with H_2 plasma treatment	25 °C	SINANO [58]
2019		Converter w/ gate driver	E-mode GaN-on-Si	Recessed MIS-gate	250 °C	XJTLU, UoL [59]
2019		Synchronous converter w/ gate drivers	E-mode GaN-on-SOI	P- GaN	25 °C	IMEC [60]
2019		Converter w/ over-current protection and gate driver	E-mode GaN-on-Si	Recessed MIS-gate	25 °C	UESTC [61]
2019		Synchronous converter w/ gate drivers	E-mode GaN-on-Si	Recessed MIS-gate	250 °C	XJTLU, UoL [62]
2020		Synchronous converter w/ gate drivers and logic circuits	E-mode GaN-on-Si	P-GaN	125 °C	EPC [63]
2020		Buck converter w/ gate driver and control circuits	E-mode GaN-on-Si	P-GaN	25 °C	Leibniz University [64]
2021		Inverter oscillator	E-mode GaN-on-Si	CMOS P-GaN	25 °C	HKUST [65]

Table 1. 4 Status of GaN ICs of commercial companies

Manufacture	Technology	Product No.	Configuration	Voltage (V)
EPC **[63]**	P-doped GaN	EPC2152 EPC2107, 2108 EPC2100, 2101, 2102, 2103, 2104, 2105, 2106 EPC2110	e-power^{TM} stage Dual with Sync Boot Half Bridge Dual Common Source	48 30, 40, 60, 80, 100, 200
Panasonic **[46]**	P-doped AlGaN	N.A.	Half-bridge converter with drivers	48
Navitas **[25, 55]**	Recess gate and insulator	NV6250	Half-bridge converter with logic circuits and drivers	650
IMEC **[60]**	P-doped GaN	N.A.	Half-bridge converter with drivers	48

1.3.2 Challenges of GaN IC

It is increasingly apparent that a transition from the general scheme of power IC using discrete devices to that of a fully integrated system-on-chip. Several scientific, technological, and manufacturing challenges, however, need to be solved before GaN power devices can become mainstream. From the mass production of GaN IC, the fabrication of GaN on large diameter substrates is very challenging due to the large lattice mismatch and thermal expansion coefficient between GaN and Si substrate. 650 V GaN-on-Si E-mode devices have been achieved in a 200 mm CMOS fab, and Si-on-poly-AlN substrates are recommended for E-mode GaN devices targeting 1200 V power applications [33]. Owing to the Si substrates induced crosstalk effect and its limited heat dissipation, GaN-on-silicon-on-insulator (SOI) substrates [18], GaN-on-SiC [66], or GaN-on-diamond [67] are promising candidates to solve these issues.

The P-type channel GaN transistors are the major obstacle for realizing the GaN

CMOS technology. One approach is to use two-dimensional hole gas (2DHG) in GaN, this method is challenging owing to the poor 2DHG hole mobility of 6~43 cm^2Vs^{-1} [68, 69], and great efforts have to be made to demonstrate a reliable operation and manufacturability of P-type devices in GaN IC. However, another alternative approach is to improve P-type doping and selective area growth, the recent demonstration of a GaN CMOS inverter [50] was achieved through regrowth of P-type GaN structure on the same substrate with N-type GaN structure.

The N-channel GaN IC suffers from high on-state resistance of E-mode devices, which degrades the high electron mobility of 2DEG in AlGaN/GaN hetero-structure. Both P-doped GaN and the recessed gate have this concern, so it is essential to improve the on-state resistance of GaN E-mode devices. For recessed E-mode transistors, the recessed barrier can cause an increased R_{ON} and might lead to degradation of GaN IC. In this thesis, the impact of the recessed thickness of AlGaN barrier on the performance of GaN ICs will be systematically studied to give guidance on how much thickness it should be etched away to guarantee the performance of GaN IC.

Reliability at high temperatures is one of the major problems of GaN power devices in extreme environments, such as gate leakage, current collapse. The reliability of devices at high temperatures can affect the thermal reliability of the GaN integrated circuit (IC). For P-doped GaN technique, the Schottky gate has a large leakage current at high temperatures, and this might degrade the performance of P-doped GaN IC or even damage devices.

In this thesis, the lateral n-channel GaN devices are used for the implementation of

GaN IC for power converters, owing to better mobility than P-channel GaN transistors. The recessed GaN MIS-HFETs are proposed to achieve E-mode operation owing to reduced leakage current, especially at high temperatures. The monolithic GaN IC in this thesis is achieved through integration of D-mode MIS-HEMTs and recessed E-mode MIS-HFETs.

1.4 High-temperature (HT) GaN power converters

1.4.1 Status of HT power converters

High-temperature power converters are increasingly required under extreme environments, like aviation, electric vehicles, etc. The Si-based devices can only operate at temperatures below 150 °C, which outstands the advantages of WBG devices for high-temperature power converters. Most reported HT power converters [70-79] are based on SiC power devices, and the operating temperatures range from 105 °C up to 400 °C. These power converters are mainly targeted for high power and low-frequency applications, so they are only based on discrete SiC power transistors for high temperature operation. Moreover, even though SiC WBG devices receive a great deal of attention in high-temperature applications, some factors limit the implementation of SiC integration circuits at high temperatures [1], including their large area, temperature dependence of carrier concentration, and degraded leakage current at high temperatures.

Table 1. 5 GaN converters with integrated gate drivers using GaN E-mode technology

Year	Topology	Technology	Frequency	Temperature	Authors
2009	Boost (integrated diode)	CF_4 plasma treatment	1 MHz	25 °C	HKUST [37]
2014	Half-bridge with gate drivers	P-doped AlGaN	2 MHz	25 °C	Panasonic [46]
2016	Half-bridge with gate drivers	N. A.	400 MHz	25 °C	Univ. of Colorado [52]
2017	Half-bridge with gate drivers	Recessed MIS gate	2 MHz	150 °C	Navitas [55] [80]
2019	Boost with gate driver	Recessed MIS gate	100 kHz	250 °C	This work [59]
2019	Half-bridge with gate drivers	P-doped GaN	500 kHz	25 °C	IMEC [60]
2019	Buck with gate driver and overcurrent protection	Recessed MIS gate	100 kHz	25 °C	UESTC [61]
2019	Half-bridge with gate drivers	Recessed MIS gate	100 kHz	250 °C	This work [62]
2020	Half-bridge with gate drivers	P-doped GaN	3 MHz	125 °C	EPC [63]
2021	Half-bridge with deadtime controller	Recessed MIS gate	100 kHz	250 °C	This work

So far, the studies of GaN-based HT power converters are seldom. The monolithic integration of GaN power converters is still at an early stage, and especially for high temperature operations. The studies of GaN IC [36, 39, 40, 42, 48, 54, 59, 62, 81] at high temperatures validate the advantages of monolithic integration of GaN IC for high-temperature power converters. The monolithic integration of GaN converters [37, 46, 52, 55, 59-63, 80] with gate drivers using E-mode technology has been summarized in Table 1. 5. However, most of the reported GaN converters with integrated gate drivers are only demonstrated at room temperature. Only two converters provide maximum

temperature operation of 150 °C [55, 80] and 125 °C [63], and heatsink [63] is used to manage thermal dissipation based on P-doped GaN technique. This thesis demonstrates monolithic GaN power converters which show the highest temperature operation of 250 °C. This thesis aims at the GaN high-temperature power converters with monolithically integrated gate driver and controller in electric vehicle applications that require temperature above 200 °C.

1.4.2 Challenges of HT GaN power converters

(1) Challenges of HT power devices

From the device level, the main parameters affect the high-temperature operation of semiconductor devices and circuits, including intrinsic carriers, p-n junction leakage, carrier mobility, thermionic leakage, etc [2]. The low intrinsic carrier concentration of GaN power device in Fig.1.2.1 validates its advantage for high-temperature operation. In GaN HEMTs or P-doped GaN HEMTs, the leakage current of Schottky barrier contact and the intrinsic p-n junction leakage current increase with increasing temperatures. The gate insulator is used in this thesis to reduce leakage currents, especially at high temperatures.

The carriers gain more thermal-vibrational energy and thus move slowly through a semiconductor crystal owing to collisions, resulting in a decrease in carrier mobility. Polar-optical phonon scattering dominates the 2DEG channel owing to the presence of polarization charges in GaN HEMTs [82]. For recessed MIS-HFETs, the main contributions of carrier scattering are interface charges induced Columb scattering [82,

83] and acoustic phonon scattering [83]. It is essential to study the degradation mechanisms of mobility with temperatures in both D-mode devices and recessed E-mode devices. This helps understand the temperature-dependent degradation of GaN power converters. In this thesis, the degradation mechanisms of GaN devices with temperature are discussed at various etch depths, including channel mobility, R_{ON}, etc.

(2) HT gate driver and control circuits

Power converters that can function at ambient temperatures higher than 200 °C can greatly benefit applications under extreme environments like aviation, electric vehicles. Gate driver and control circuits are essential components for GaN-based power DC-DC converters, and the mainstream Si-based circuits can not operate properly at high temperatures beyond 150 °C, which is one of the main challenges of HT GaN power converters. This emphasizes the importance of GaN power converters with self-contained functionality like GaN-based driver and control circuits, and this all-GaN solution can greatly reduce the volume, weight, and cost of the power converters without external cooling systems under extreme environments.

On the circuit level, the limited gate voltage swing of existing GaN HEMTs or p-GaN power transistors [84] brings new challenges in gate driver circuit design. This increases the risk of gate breakdown and complexity of gate drivers, which normally requires additional level shifters [47, 48, 85]. To optimize GaN power converters from a design point of review, many factors like gate driver design and circuit topology require careful consideration. In this thesis, the recessed MIS-gate technique with a large gate swing is proposed to monolithically GaN power converters with integrated

gate drivers without additional level shifters, and different gate drivers and topologies are evaluated for high-temperature operation.

Besides the gate driver design, the deadtime circuit design faces challenges. The external micro-controller increases the complexity, weight, and cost of the control system. Most adaptive deadtime techniques are based on Si-based CMOS technology, which limits the converter performance at high temperatures. To take full advantage of GaN power devices, an all-GaN solution is highly required to adjust deadtime from the integration circuit level, especially for high-temperature power converters. To address these challenges, a GaN-based deadtime control circuit is designed in this thesis.

1.5 Thesis goal and organization

It is the increasing trend to integrate more GaN function blocks into one chip, also called system-on-chip, no matter semiconductor industries or scientific institutes have been going on this way. This thesis aims to use recessed MIS gate to demonstrate GaN-based HT converters with integrated power transistors and more function blocks, like gate drivers, logic circuits, and control circuits. The results in this thesis provide effective solutions of high-temperature power converters without external heasink or cooling systems under extreme environments.

Chapter 2 describes SPICE based circuit model using Advanced Design System (ADS) to simulate GaN IC on a circuit level. Then, the fabrication process of GaN IC is introduced, and the measurement of both devices and circuits is introduced lastly.

Chapter 3 systematically studies the impact of etch depths on the performance of GaN devices and integrated circuits at various temperatures, in terms of mobility, R_{ON}, and etc. The different scattering mechanisms of channel mobility under different etch depths are investigated at high temperatures.

Chapter 4 demonstrates an integrated GaN boost converter for HT operation up to 250 °C, and the converter integrates an E-mode power transistor and an optimized gate driver. The proposed gate driver is carefully designed and measured at various temperatures.

Chapter 5 demonstrates a synchronous GaN buck converter for HT applications, which integrates half-bridge transistors and gate drivers. The synchronous GaN converter shows excellent stability at various temperatures up to 250 °C. An asynchronous buck converter with an integrated gate driver is also fabricated and compared with the synchronous buck converters at various temperatures. The integrated converters are also compared with converters with external drivers to emphasize the importance of full integration using GaN devices.

Chapter 6 demonstrates an integrated GaN no deadtime technique (NDT) for HT synchronous DC-DC buck converters. The proposed GaN NDT converter requires only one control signal and provides a simple method for deadtime management. The proposed GaN NDT converter is systematically compared with an integrated converter with a fixed deadtime at various conditions. The results emphasize the advantages of the proposed NDT converter with better efficiency of converter owing to smaller overshoots of gate drivers at high load currents, especially at high temperatures.

Chapter 3 is about high-temperature characteristics under different etch depths of AlGaN barrier, including mobility and R_{ON}. This helps understand thermal behavior and characteristics of GaN-based drivers and converters in the other three chapters. Boost and buck are two basic and essential topologies in Non-isolated DC-DC converters. Chapter 4 focuses on GaN boost converters with integrated gate drivers, and chapter 5 focuses on GaN buck converters with integrated gate drivers, including asynchronous and synchronous converters. The deadtime management of the GaN synchronous DC-DC converter in chapter 5 uses a fixed deadtime technique. In chapter 6, a GaN-based no deadtime technique (NDT) is proposed and evaluated for high-temperature GaN DC-DC power converters.

Chapter 2 Simulation, fabrication, and characterization

This chapter presents the device/circuit simulation, fabrication and characterization. In section 2.1, the simulation of the GaN devices and integrated circuits is introduced. The fabrication flow of the GaN-based direct-coupled field logic (DCFL) inverter is demonstrated in section 2.2. In section 2.3, the characterization of discrete devices is introduced first, and then the characterization of a GaN-based DCFL inverter is demonstrated, including static and dynamic measurement.

2.1 Advanced Design System (ADS) simulation

2.1.1 ADS introduction

Only a few device models have been proposed for GaN HEMTs in power electronics, and the available models can be divided into four categories [86]: numerical model [87, 88], behavioral model [89-91], physics-based model [92, 93], and semiphysics-based model [94-97]. The numerical model is based on numerical simulation tools (SILVACO, Sentaurus TCAD, etc.), and this model needs detailed structure information and material properties. The behavior mode is normally based on PSpice circuit mode [90, 91] or an analytical mode [89], and this mode is suitable for simulation with discrete GaN HEMTs in a GaN PCB. The circuit parameter extraction includes intrinsic and parasitic capacitance, inductance, and resistance. The physics-based model is based on an accurate determination of 2DEG charge density [92, 93]. For GaN integrated circuit

simulation, numerical model and physics-based model are complex, owing to the exact information about material properties, physical structure and parameters. The semiphysics-based model [94-97] is based on SPICE circuit model, and it is simple and suitable for GaN IC simulation. In this thesis, ADS software is used for circuit simulation. GaN MIS-HEMTs are modeled by SPICE-based "Advanced Curtice Quadratic Model [97, 98], this model is based on GaAs FETs and is suitable for use in conventional, time-domain circuit simulation. This model has been used to simulate GaN ICs for GaN power converters [97].

In ADS simulation, the drain current I_{DS} with respect to the gate voltage using the model [97, 98] is calculated with the following expression in the region $V_{DS}> 0$:

$$I_{DS} = \beta_U (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \tanh(\alpha V_{DS}) A$$

$$\beta_U = \beta / \left[1 + (V_{GS} - V_{th}) U_{crit}\right]$$

V_{th} is the threshold voltage, β is the transconductance, λ is the channel length modulation parameter, α is the hyperbolic tangent function, β_U is the degenerated transconductance, and A is the device width parameter and U_{crit} is the degeneration coefficient.

2.1.2 Device calibration

The electrical characteristics of fabricated devices are used to calibrate the models of D-mode and E-mode devices. Table 2. 1 shows the calibrated parameters for ADS simulation. Fig.2.1.1 shows the experiment and simulation results of D-mode and E-mode devices, and the simulation results fit with experiment results in general. But

there are some discrepancies, especially near “knee voltage”. The discrepancies might be caused by the non-optimized model for GaN MIS-HEMTs, since most reported models are designed for GaN HEMTs. The insulator-related interface traps cause dynamic R_{ON} issues or current collapse issues in devices, and these might cause the mismatch between simulation and measurement in this thesis. In addition, for high-temperature power electronic circuit simulation, a full electrothermal model addressing self-heating is required to give accurate simulation. However, this SPICE-based model is suitable to verify the function ability of GaN ICs, and the design and size optimization are based on experimental results in this thesis.

Table 2. 1 Parameter for ADS simulation

Parameter	**Description**	**Units**	**D-mode device**	**E-mode device**
$\mathbf{V_{to}}$	Threshold voltage	V	-8	1
β	Transconductance	A/V^2	7.11E-4	5.67E-4
λ	Channel length modulation	1/V	0	0
α	Hyperbolic tangent function	1/V	0.25	0.16
$\mathbf{U_{crit}}$	Critical field for mobility degradation		8.29	6.28

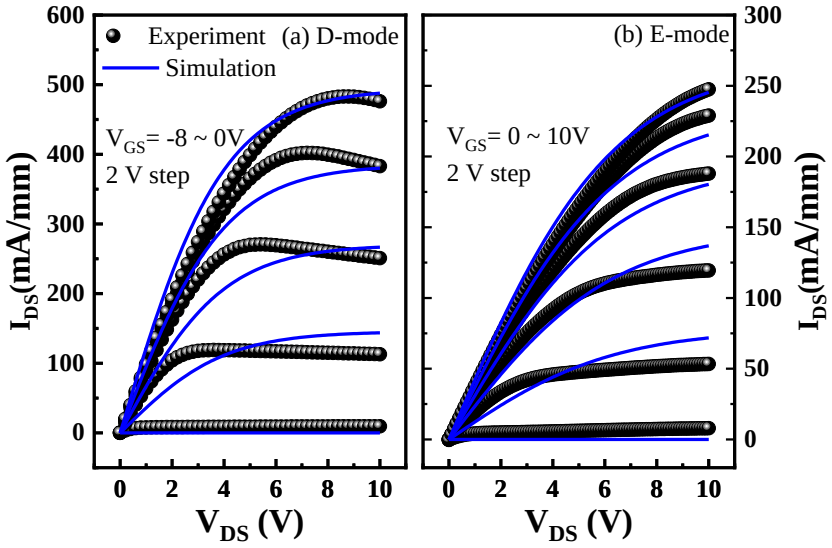


Fig.2.1.1 At room temperature, experiment (symbols) and simulation (lines) of I_{DS}-V_{DS} characteristics of (a) D-mode devices, and (b) E-mode devices.

2.1.3 Simulation of GaN basic logic circuits

The calibrated models are used to simulate GaN-based integrated circuits (ICs), Fig. 2.1.2 shows the simulation and experiment result of a GaN DCFL inverter, the simulation fits well with experimental data in general, especially for some points like V_{IH}, V_{IL}, etc. In addition, there's a small discrepancy during the transition region between V_{IH} and V_{IL}, this is possibly caused by the mismatched current near knee voltage between experiment and simulation of GaN devices. However, it doesn't affect the utilization of this model to simulate GaN IC. The model used in this work can provide the feasibility of the GaN circuit simulation, which guarantees the design of the GaN circuits. The simulated dynamic waveforms of the GaN DCFL inverter are shown in Fig. 2.1.3 with a frequency of 100 kHz. The output signal functions well, when the input signal is high and the output signal is low as expected.

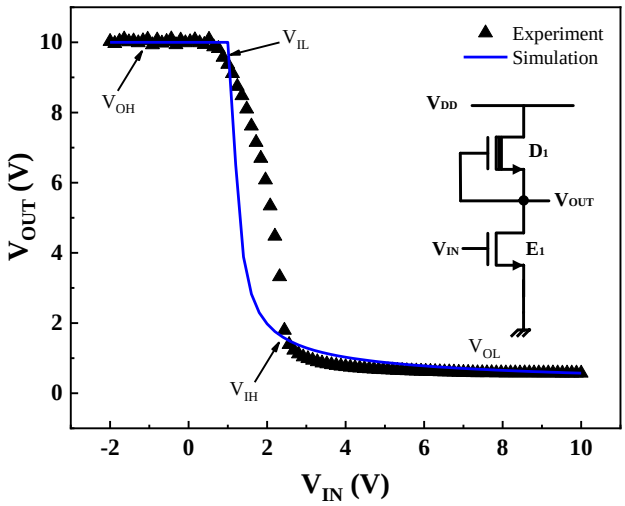


Fig. 2.1.2 Experiment (symbols) and simulation of a DCFL inverter. $W_{G,D}$=25 μm, $W_{G,E}$=1000 μm.

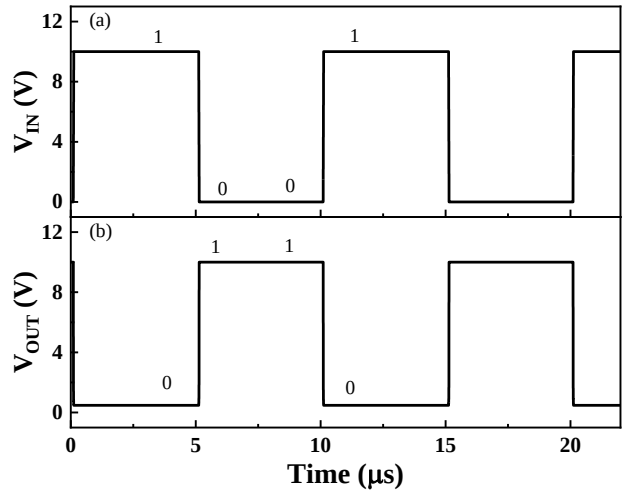


Fig. 2.1.3 Simulated dynamic waveforms of the GaN DCFL inverter. (a) Input signal V_{IN}, and (b) output signal V_{OUT}. V_{DD}=10 V, f=100 kHz. $W_{G,D}$=25 μm, $W_{G,E}$=1000 μm.

The GaN two-input NAND gate is designed as Fig. 2.1.4 (a), which consists of a depletion load D_1 with source-gate connected and two-input E-mode transistors in a series connection. The simulated waveforms are shown in Fig. 2.1.4 (b) and (c), and the circuit functions correctly. The output voltage is low only when two E-mode transistors both turn on. The GaN two-input NOR gate is also designed as Fig. 2.1.5 (a), which consists of two-input E-mode transistors in a parallel connection and a depletion load

D_1. The simulated waveforms are shown in Fig. 2.1.5 (b) and (c), and the output voltage is high only when two transistors both turn off.

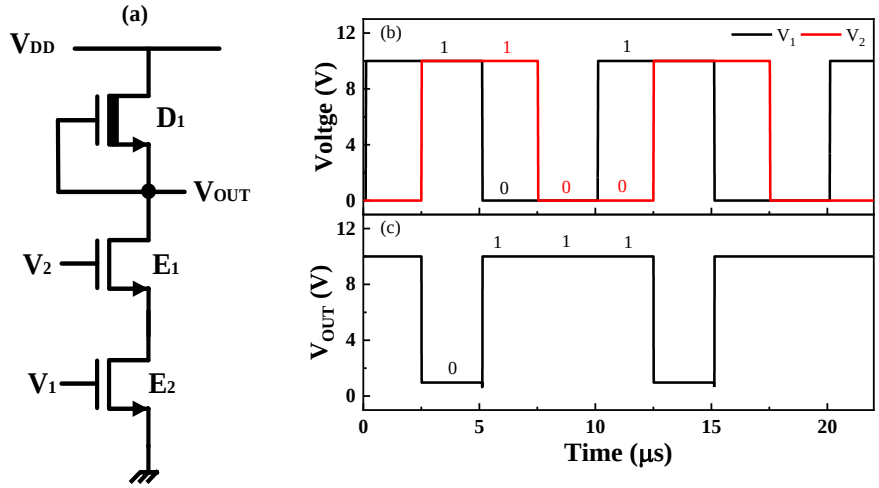


Fig. 2.1.4 Simulated dynamic waveforms of the GaN two-input depletion-load NAND gate. (a) The circuit diagram, (b) input signals, and (c) output signal. V_{DD}=10 V, f=100 kHz. $W_{G,D}$=50 μm, $W_{G,E}$=2000 μm.

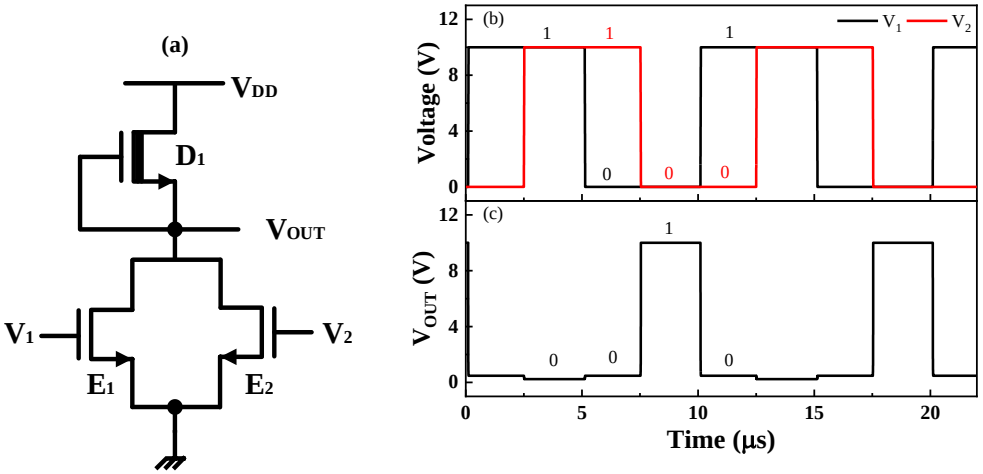


Fig. 2.1.5 Simulated dynamic waveforms of the GaN two-input depletion load NOR gate. (a) The circuit diagram, (b) input signals, and (c) output signal V_{OUT}. V_{DD}=10 V, f=100 kHz. $W_{G,D}$=50 μm, $W_{G,E}$=2000 μm.

2.2 GaN IC fabrication flow

Both depletion (D)-mode MIS- HEMTs and E-mode MIS heterojunction-field-

effect-transistors (HFETs) were fabricated on the same substrate, with the structure shown in Fig.2.2.1. The AlGaN/GaN epitaxy used in this work consists of a 25 nm $Al_{0.25}Ga_{0.75}N$ barrier and a 5 μm GaN buffer on a Si substrate. In D-mode devices, 2DEG electrons are generated at the interface between the AlGaN barrier and GaN layer, resulting in normally-on operation or a negative threshold voltage without applied gate voltage. To achieve normally-off or enhancement-mode operation, the AlGaN barrier is etched away in this work using a digital etching [14], the threshold voltage of E-mode devices can be shifted to a positive value due to the absence of polarization under the gate.

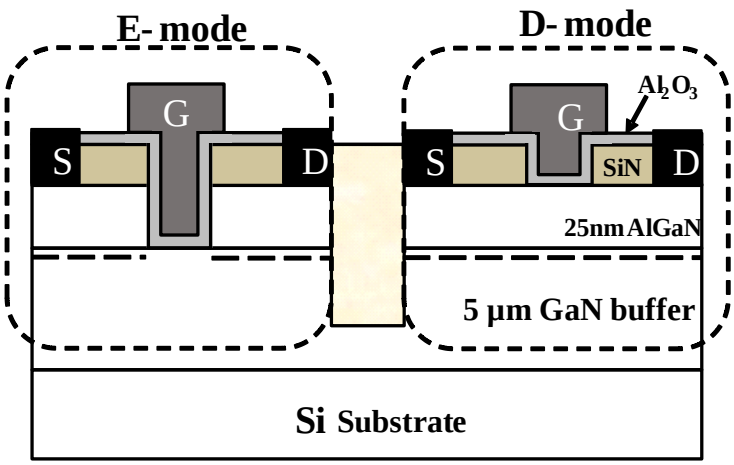


Fig.2.2.1 Schematic diagram of E-mode MIS-HFETs and D-mode HEMTs.

To clearly illustrate the fabrication process of GaN integrate circuit (IC), here we take a GaN inverter as a simple example. Fig.2.2.2 shows the circuit diagram of the GaN DCFL inverter, which consists of a D-mode active resistor with source-gate connected, and an E-mode driver as well.

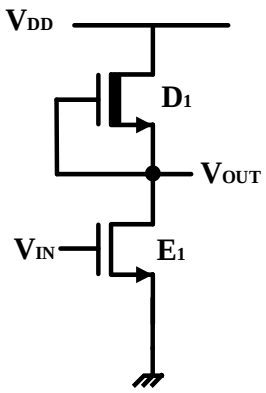


Fig.2.2.2 The circuit diagram of a GaN-based DCFL inverter.

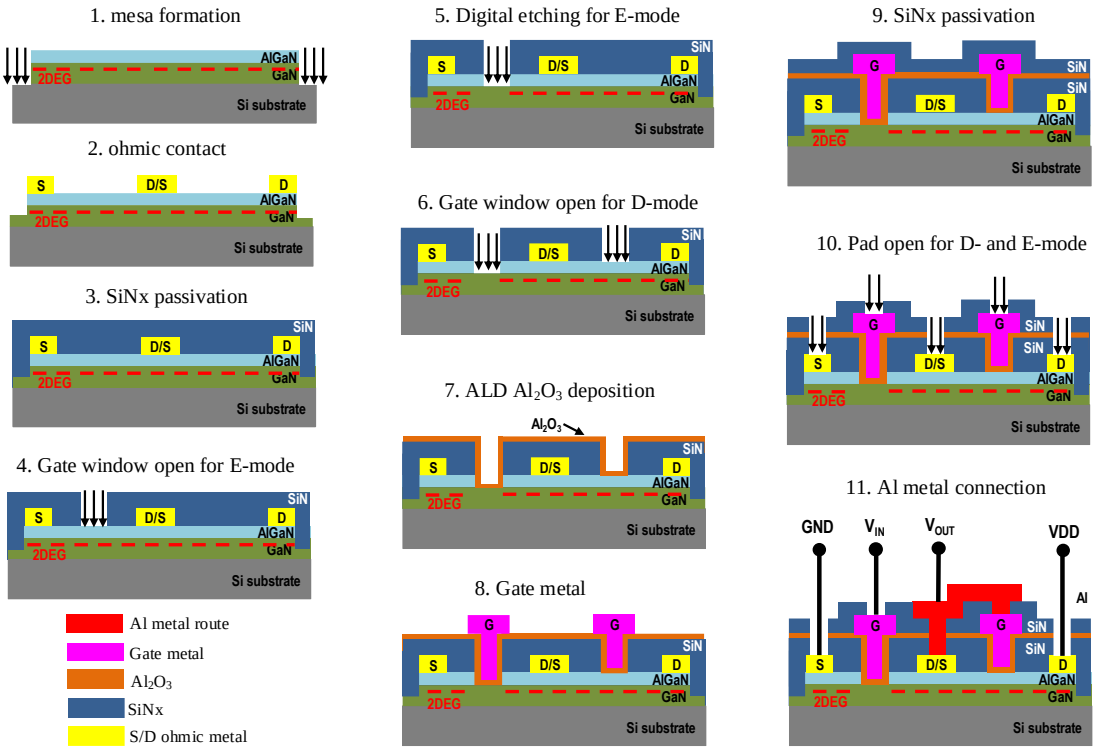


Fig.2.2.3 Fabrication flow of a GaN-based DCFL inverter.

Fig.2.2.3 shows the fabrication flow of a GaN-based DCFL inverter, and the process started with mesa etching to isolate discrete devices or circuits (step 1), and the Au-free source and drain ohmic contacts were formed by Ti/Al/Ni/TiN (25/125/45/100 nm) evaporation followed by a rapid thermal anneal (RTA) at 800 °C (step 2), and the drain

of E-mode device shares the same ohmic contact with the source of D-mode active resistor. The contact resistance R_C is 1.2 Ωmm. Then, 150 nm plasma-enhanced chemical vapor deposition (PECVD) SiN_x was deposited as a passivation layer and an etching hard mask for the E-mode gate recess (step 3); the gate window is open for the E-mode device through the dry etching of SiN_x under the gate (step 4); then the E-mode device was formed by digital etching (step 5). The digital etching was performed by using O_2 plasma treatment at the GaN surface for 3 minutes at 60 °C with an RF (radio frequency) power of 100 W. Afterwards, the oxidation layer was removed by wet etching in 1:10 hydrochloric acid for 1 minute. After 55 cycles of digital etching, the full recess depth of around 25 nm was removed with a small etching rate of 0.45 nm/cycle.

After the gate window is open for the D-mode device (step 6) through dry etching of SiN_x, a 20 nm atomic layer deposition (ALD) Al_2O_3 gate dielectric layer for E/D-mode devices was deposited (step 7). Then, the evaporation of Ni/TiN was performed as the gate metal (step 8), and a 100 nm SiNx was deposited as inter-metal dielectrics (step 9). Lastly, the pad contacts are open for D/E-mode devices through dry etching of SiN_x (step 10), a 200 nm Al metal was finally evaporated as the metal connection to connect the source and gate of the D-mode transistor. The fabricated chip is shown in Fig.2.2.4, with a chip size of 2 cm x 2cm.

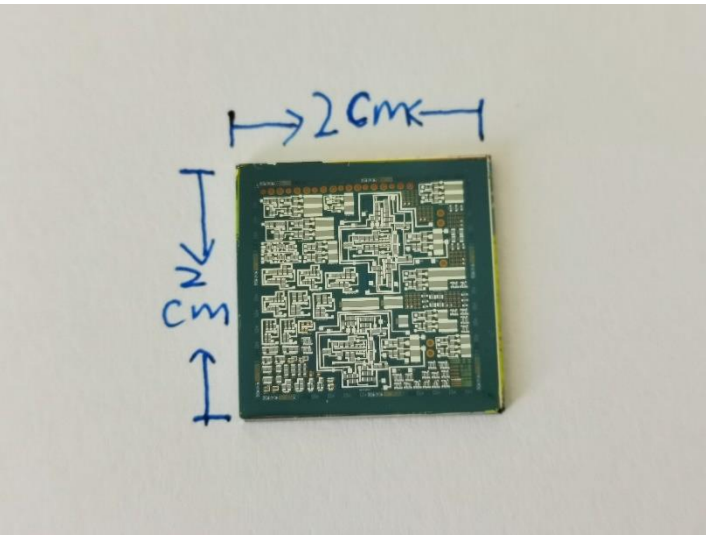


Fig.2.2.4 A photo of the fabricated chip with GaN ICs. (Chip size: 2 cm x 2 cm).

2.3 Characterization methodology

2.3.1 Device characterization

Semiconductor analyzer Keysight B1500A is used to obtain electrical properties of GaN devices, through I_{DS}-V_{DS} and I_{DS}-V_{GS} measurements. These measurements are with two high-resolution source/measure units (HRSMU) and one ground unit (GNDU). For I_{DS}-V_{DS} measurement, at a given gate voltage, the drain current is measured when the drain signal is swept from 0 to 10 V; and then the gate voltage is varied with a step of 1 V. For I_{DS}-V_{GS} measurement, at a given drain voltage, the drain current is measured when the gate signal is swept from a voltage of less than V_{th} to a positive gate bias, and the sweeping resolution is set as a low voltage of 20 mV.

The schematic diagram of high-temperature (HT) characterization of devices under test (DUT) is shown in Fig.2.3.1, high-temperature measurement was carried out for both GaN devices and integrated circuits by Semishare SE-6 probe station, which is

equipped with a temperature hot chuck system. A temperature controller is connected to the chuck on the probe station with a temperature range of 25 °C to 300 °C.

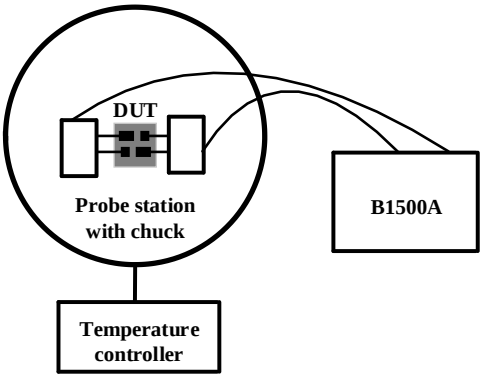


Fig.2.3.1 Schematic diagram of the high-temperature setup.

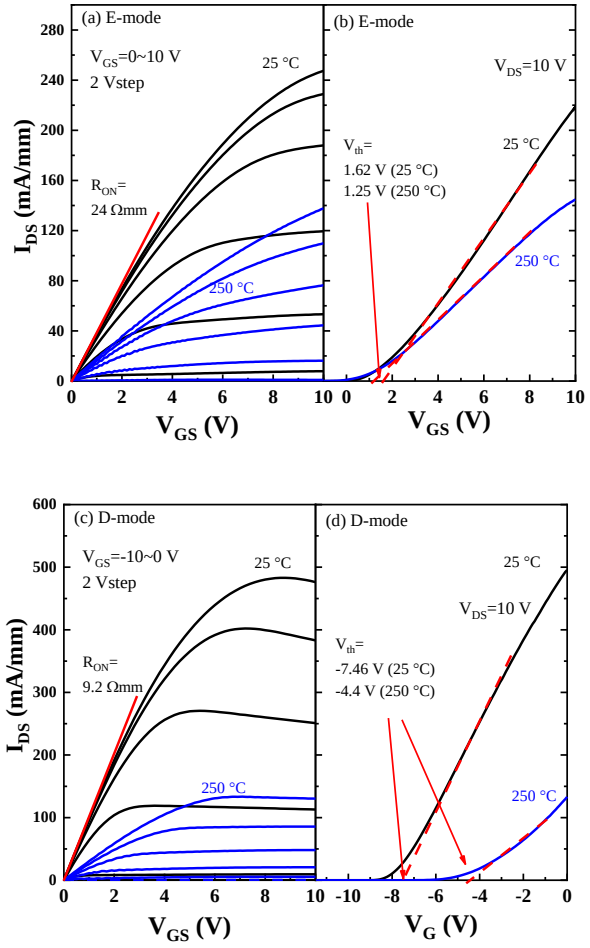


Fig.2.3.2 Output and transfer characteristics of E-mode MIS-HFETs (a) and (b), D-mode MIS-HEMTs (c) and (d) at 25 °C and 250 °C, respectively.

Fig.2.3.2 shows the DC characteristics of discrete E-mode and D-mode devices, which were fabricated on the same chip with GaN gate drivers and power transistors. At 25 °C, E-mode devices show a threshold voltage (V_{th}) of +1.62 V, a maximum output current ($I_{DS,\ max}$) of 247 mA/mm (V_{DS}=10 V), and an on-state resistance (R_{ON}) of 24 Ωmm. The D-mode devices show a V_{th} of -7.46 V, $I_{DS,\ max}$ is 480 mA/mm (V_{DS}= 10 V), and R_{ON} is 9.2 Ωmm. When the temperature is increased up to 250 °C, both D-mode and E-mode devices show degraded performance. At 250 °C, the V_{th} is +1.25 V and the $I_{DS,\ max}$ decreases to 135 mA/mm for E-mode devices, whereas D-mode MIS-HEMTs show a V_{th} of -4.4 V and a decreased $I_{DS,max}$ of 143 mA/mm. The reduction of output current at high temperatures is caused by the degradation of channel mobility [99, 100]. The GaN-based E-mode MIS-HFETs show better V_{th}-thermal stability than D-mode MIS-HEMTs, which might be attributed to the absence of a polarized barrier layer in E-mode MIS-HFETs. The temperature-induced V_{th} instability in D-mode AlGaN/GaN MIS-HEMTs is mainly caused by Al_2O_3/AlGaN interface traps [101, 102], and the positive shift of threshold voltage of D-mode MIS-HEMTs might be caused by the strain relaxation in AlGaN barrier above 250 °C [103]. Efforts should be made to improve the reliability of dielectric at high temperatures and to provide a promising pathway toward reliable and stable insulated GaN-based ICs for high temperature applications.

2.3.2 GaN integrated circuits (ICs) characterization

The static characteristic of a GaN DCFL inverter was measured by B1500A, as shown in Fig.2.3.3. The V_{DD} was provided by an Agilent E3647A power supply, and

the GND node was connected to the GNDU of B1500A. The input signal V_{IN} was connected to the HRSMU1, and the output signal V_{OUT} was connected to the HRSMU2, and the output voltage was measured with the variation of the input voltage.

The dynamic characteristics of the inverter were measured through the below experiment setup, as shown in Fig.2.3.4. The V_{DD} was applied by an Agilent E3647A power supply, and the GND was connected to the ground. The V_{IN} was supplied by a RIGOL DG3061A function generator, and the dynamic waveforms of both V_{IN} and V_{OUT} were simultaneously collected by an Agilent DSO-X 2024 oscilloscope. The high-temperature measurement of integrated circuits was also carried out, and the experimental setup is similar to HT characterization of GaN devices in Fig.2.3.1.

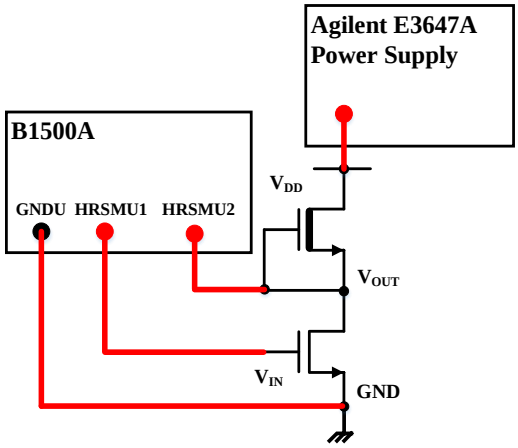


Fig.2.3.3 Experiment setup for static measurement of a GaN DCFL inverter.

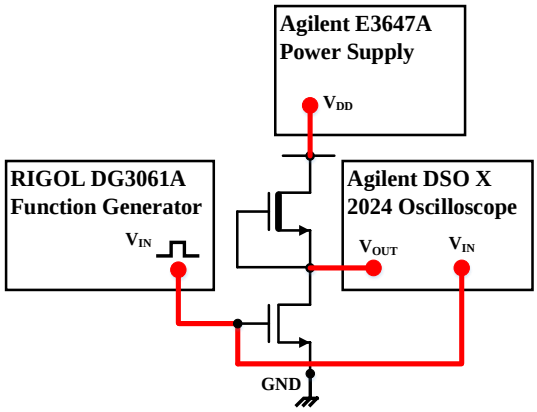


Fig.2.3.4 Experiment setup for dynamic measurement of a GaN DCFL inverter.

Chapter 3 The impact of etch depth of AlGaN barrier on the performance of GaN-based devices and integrated circuits (ICs)

3.1 Motivation

From the converter design point of review, active devices and integrated circuits are two main aspects of this thesis. From the device aspect, mobility and on-state resistance are two key device parameters. As discussed in Section 1.1.2, the mobility can impact the frequency, and on-state resistance can affect the conduction loss and efficiency of power converters. The channel mobility and on-state resistance have a close relationship with the etch depth of the recessed technique, so it is essential to study the impact of etch depth on the performance of channel mobility and on-state resistance at high temperatures. This helps understand the thermal behavior of power converters in chapters 4, 5, and 6.

The recessed MIS gate in this thesis provides good controllability and a large gate swing, owing to smooth digital etching technique and a high-k gate insulator. The channel mobility of AlGaN/GaN heterostructure is normally 1200-2000 cm^2/Vs [104, 105]. The reported mobility of recessed E-mode MIS heterojunction-field-effect-transistors (HFETs) is around 75-300 cm^2/Vs [106, 107], and this limits the mass production of GaN integrated circuits compared with Si-based MOSFETs. There are

two approaches to achieve E-mode recessed MIS-HFETs, partial recess [108] and full recess [109]. In this chapter, we investigate the impact of the etch depth of E-mode devices on the performance of GaN devices (including mobility and R_{ON}) and integrated drivers. Besides, we also study the impact of etch depth of AlGaN thickness on the performance of D-mode devices and GaN-based inverters at various temperatures. The full recess depth of 25 nm is recommended in this thesis to improve the stability of GaN drivers and converters, especially at high temperatures.

GaN material is an excellent candidate for high-temperature (HT) applications above 150 °C owing to its good thermal conductivity, however, the current is reduced at high temperatures owing to the degradation of channel mobility. It is essential to study the mechanisms of carrier scattering and current degradation at high temperatures, especially for power converters in electric vehicle applications above 200 °C. For the unrecessed channel, 2DEG electrons dominate the conducting carriers, and MOS or MIS channel electrons dominate the conducting carriers in the fully recessed channel owing to the absence of the polarization field. There are four main contributions of channel mobility in unrecessed D-mode MIS-HEMTs or recessed E-mode MIS-HFETs, including phonon scattering (μ_{ph}), bulk mobility (μ_B), Coulomb scattering (μ_C), and surface roughness scattering (μ_{SR}).

The presence of polarization charges of the 2DEG channel can provoke some additional deviations from classic MOS theory [110], polar-optical scattering caused by the polarization field plays an important role in the 2DEG channel [82]. For recessed MIS-HFETs, the main contributions of carrier scattering are interface charges induced

Columb scattering [82, 83] or interface induced remote impurity scattering [111, 112], and acoustic phonon scattering as well [83]. Surface roughness can also be important in a recessed HEMT [113]. There is an obvious scattering transition from D-mode MIS-HEMTs to recessed E-mode MIS-HFETs, it is essential to investigate the mechanism transition with the etch depth of the AlGaN barrier. To be specific, to what etch thickness the transition starts to happen. The interface charges induced Columb scattering plays an important role in recessed E-mode MIS-HFETs. When the thickness of AlGaN is reduced by gate recess, the distance between AlGaN/Al_2O_3 interface and 2DEG channel becomes smaller, and this consequently outstands the contribution of Columb scattering caused by interface charges. It is required to know to what etch thickness Columb scattering starts to play an important role. There are limited studies to investigate mechanisms of high-temperature carrier scattering under different etch depths. An etch depth of 3 nm shows a reduced mobility compared with nonrecess structure, and theoretical simulation indicates the important role played by surface roughness [113]. The mobility under different etch depths was measured at various temperatures, but the simulation has some discrepancies with experimental results [114]. The effect of recess depths on mobility was studied experimentally [115] at room temperature without scattering mechanisms discussion at high temperatures. Most reported studies either focused on experimental mobility at different etch depths, or they were lack of accurate theoretical calculations to investigate the underlying scattering mechanisms at high temperatures. Seldom studies were reported to investigate the impact of etch depth on the scattering mechanisms of mobility at high

temperatures. In this chapter, the high-temperature carrier scattering mechanisms are studied at various etch depths of AlGaN barrier over a large range, to study the transition of mobility principle from D-mode MIS-HEMTs to recessed E-mode MIS-HFETs. This can give a clear explanation of how the etch depth affects the channel mobility in GaN-based devices.

In section 3.2, the mechanisms of carrier scattering with different etch depths of AlGaN barrier are experimentally and theoretically studied at high temperatures. Section 3.3 investigates the impact of etch depth on the performance of discrete D-mode MIS-HEMTs and E-mode MIS-HEMTs. Section 3.4 studies the impact of the etch depth on the performance of GaN integrated circuits (ICs). Lastly, section 3.5 gives some conclusions.

3.2 Mechanisms of carrier scattering with different etch depths at high temperatures

3.2.1 Theoretical calculation of mobility

Lombardi *et al.*[116] described the mobility of carriers in the inversion channel of a MOSFET or MISFET using the following:

$$\mu_{FE}(MISFET) = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \right]^{-1} \tag{3.1}$$

1. Bulk material mobility

μ_B is the channel mobility of bulk material, and the temperature dependence of the bulk mobility can be expressed using the model proposed by Caughey and Thomas

[117], and simplified as following for GaN MISFETs [83]:

$$\mu_B = \mu_0 + \frac{\mu_{\max}\left(\frac{T}{300}\right)^{-\gamma} - \mu_0}{1+(N_D / C_r)^{\alpha 1}} \tag{3.2}$$

Where T is the absolute temperature and N_D is the doping concentration of the GaN substrate, which is around 10^{15} cm^{-3} in this work. C_r, α_1, and γ are fitting parameters.

2. Acoustic phonon scattering

The acoustic phonon mobility is caused by crystal lattice vibration, and it can be expressed by [83, 116, 118]:

$$\mu_{ac}(E_\perp, T) = \left(B\frac{T}{E_\perp} + C\frac{N_D^{\alpha 2}}{E_\perp^{1/3}} \right)\frac{1}{T} \tag{3.3}$$

Where B and C are two fitting parameters, the orthogonal component of the electric field ($E_\perp$) is estimated to be 0.5 MV/cm in a recessed MIS-HFET at the peak mobility [83] and an inversion-like MOSFET at room temperature [118]. The dependency of μ_{ac} on the impurity concentration is given by α_2.

Acoustic scattering dominates the phonon mechanism in Silicon material. But for polarized GaN MIS-HEMTs, the polar electronic field can give a contribution to lattice scattering in terms of polar-optical phonon scattering. The acoustic phonon mobility μ_{ac} should be replaced by a combination of μ_{ac} and polar-optical-phonon mobility μ_{po}, so the phonon mobility μ_{ph} can be expressed as $\mu_{ph}^{-1} = \mu_{ac}^{-1} + \mu_{po}^{-1}$. So the 2DEG channel mobility can be modified as:

$$\mu_{FE}(MISHEMT) = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \right]^{-1} \tag{3.4}$$

$$\mu_{ph}^{-1} = \mu_{ac}^{-1} + \mu_{po}^{-1} \tag{3.5}$$

3. Polar-optical phonon scattering

The polar-optical mobility [82, 119] has been proposed using the following:

$$\mu_{po} \simeq \frac{D}{n_s^{\delta_1} T^{\gamma_1}} + \frac{C}{n_s^{\delta_2} T^{\gamma_2}} \simeq \frac{C}{n_s^{\delta_2} T^{\gamma_2}} \tag{3.6}$$

At elevated temperatures above 300 K, the equation (3.6) can be simplified to the last term. The polar-optical mobility is related to polarization-induced 2DEG carrier density n_s, which is 9 x 10^{12}cm^{-2} without recess. Considering that 2DEG mobility is calculated at various etch depths of the AlGaN barrier, here we simplified $C/n_s^{\delta 2}$ as C_0, and C_0 can be obtained by calculating channel mobility at room temperature. So equation (3.6) can be simplified as the following:

$$\mu_{po} \simeq \frac{C_0}{T^{\gamma_0}} \tag{3.7}$$

where γ_0 is the fitting parameter, which is equal to the slope of lnμ~lnT. The C_0 and γ_0 of this work are obtained from Fig.3.2.7 and summarized in Table 3. 1.

4. Columb scattering

In MOSFETs, models [118, 120, 121] have been proposed to describe the carrier scattering caused by Columb scattering effects, which are attributed to fixed charges of ionized traps at the interface, treating the random spatial fluctuations of the charge density as a quantum mechanism perturbation [82]. In insulated GaN FETs, the interface traps are located at nitride/insulator interface, so Columb scattering can be neglected in D-mode GaN MIS-HEMTs due to spatial separation of the interface from the 2DEG channel, and it can be significant in recessed MOS or MIS channels.

The interface charges between Al_2O_3 and GaN affect the movement of carriers under the gate, resulting in Columb scattering. The Colomb mobility depends on the interface

trapped charges Q_{trap}, can be expressed as [82]:

$$\mu_C = T\frac{A}{Q_{trap}} + NT^{\alpha}\frac{Q_{acc}^{\beta}}{Q_{trap}} \simeq NT^{\alpha}\frac{Q_{acc}^{\beta}}{Q_{trap}} \tag{3.8}$$

Where N is a fitting parameter, α and β are empirical constants to describe the screening effect on the free carriers under the gate, and they are experimentally determined to be $\alpha = \beta \approx 1$ [83, 118]. The interface density D_{it} is calculated as 9×10^{12} $cm^{-2}eV^{-1}$ with an energy range from 0.28 eV to 0.47 eV in our previous work [122], so the interface trap concentration Q_{trap} is estimated as 1.71×10^{12} cm^{-2} in this work. The accumulation charge Q_{acc} can be calculated using $Q_{acc}=C_{ox}(V_G-V_{th})$, where C_{ox} is the oxide capacitance and measured as 265 nF/cm^2, and V_G-V_{th} is around 2.74 V at the peak mobility in Fig.3.2.2. The Q_{acc} is estimated to be 4.53×10^{12} cm^{-2} in this work.

5. Surface roughness scattering

The dependence of the roughness mobility on the surface quality and temperature was given by [118]:

$$\mu_{SR}(E_{\perp},T) = \frac{A(\Delta\Lambda)^{-2}}{(E_{\perp}/E_0)^{\alpha 4}}(1-\frac{T}{T_0}) \tag{3.9}$$

Where Δ is the root mean square (rms) surface roughness and Λ is the correction, two parameters are correlated with the physical properties of the insulator/nitride interface structure. The digital recess technique in this thesis has low surface damage, and the roughness is compared with the untreated surface. Meanwhile, the surface roughness is almost the same for different etch depths, so the surface roughness scattering is not considered in this work.

Table 3. 1 Model parameter values for the four mobilities μ_B, μ_{po}, μ_{ac}, and μ_C.

Parameter	D_{etch} (nm)	Value	Units	References
Bulk mobility				
μ_0		100	cm^2/Vs	[83, 118]
C_r		$3x10^{17}$	cm^{-3}	[83, 118]
α_1		0.7		[83, 118]
μ_{max}		1600	cm^2/Vs	[83, 118]
γ		3		[83, 118]
Polar-phonon scattering				
C_0	0	2.45×10^9	$K^{\gamma 0}cm^2/Vs$	This work
γ_0	0	2.51		This work
C_0	10	2.01×10^7	$K^{\gamma 0}cm^2/Vs$	This work
γ_0	10	1.61		This work
C_0	14	4.86×10^6	$K^{\gamma 0}cm^2/Vs$	This work
γ_0	14	1.44		This work
C_0	18	$8.9x\ 10^4$	$K^{\gamma 0}cm^2/Vs$	This work
γ_0	18	0.91		This work
Acoustic phonon scattering				
B		$1.0\ x10^6$	cm/s	[83, 118]
C		$3.23\ x10^6$	$Kcm/s(V/cm)^{-2/3}$	[83, 118]
α_2		0.0284		[83, 118]
Coulomb scattering				
α_3		1		[82, 83, 118]
β		1	$cm^2(VsK)^{-1}$	[82, 83, 118]
N		0.5		0.2~1 [83, 118]

Using equations (3.2)-(3.8) and parameters in Table 3. 1, the calculated peak mobility as a function of temperature is shown in Fig.3.2.1. Both bulk mobility and polar-phonon scattering show a decreasing trend with increasing temperature. Acoustic phonon scattering also shows a slightly decreasing trend, ranging from 371 cm^2/Vs at 300 K to 232 cm^2/Vs at 475 K. However, the mobility of Columb scattering effects caused by interface traps increases with increasing temperature, from 394 cm^2/Vs at 300 K to 627 cm^2/Vs at 475 K. This might be caused by the increased screening effects with T as Q_{inv} increases with T, while Q_{trap} decreases with T due to band-gap narrowing and subsequent reduction of traps [82].

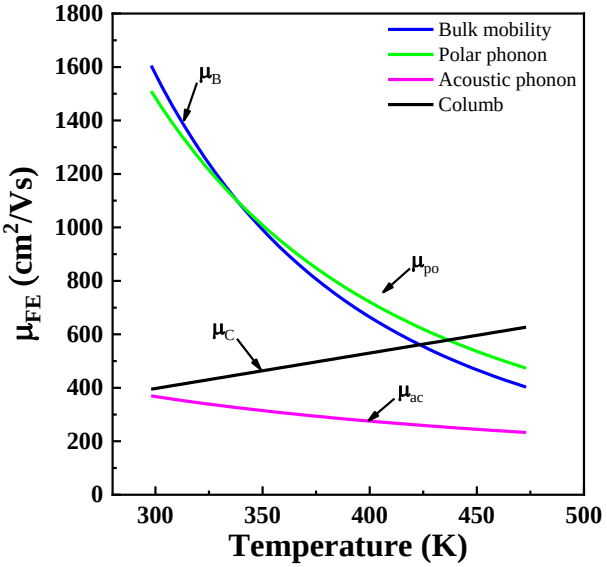


Fig.3.2.1 Calculated peak mobility as a function of temperature with different carrier scattering components (μ_B, μ_{po}, μ_{ac}, μ_C).

3.2.2 Experimental calculation of mobility

Fig.3.2.2 shows the measured transfer curve and calculated mobility at V_{DS}=0.1 V. The channel mobility of GaN HEMTs can be calculated using $\mu = g_m L/(WC_{MOS}V_{DS})$ [83,

111, 123], and a 30-μm-long gate transistor is used to calculate channel mobility at different etch depths of 25 nm AlGaN barrier, varying from 0 nm to 23 nm and an extra over-etch of GaN layer. C_{MOS} should be replaced by $C_{ob} = (C_{ox}^{-1} + C_{br}^{-1})^{-1}$ owing to the contribution of AlGaN barrier capacitance when considering a 2DEG channel as shown Fig.3.2.3 (b). C_{ox} or C_{MOS} is the oxide capacitance, and C_{br} is the AlGaN barrier capacitance. In recessed GaN MIS-HFETs, the C_{MOS} is equal to the capacitance of a GaN MOS capacitor without AlGaN barrier; while in unrecessed GaN MIS-HEMTs, the capacitance C_{ob} can be obtained from the capacitance-voltage measurement of a GaN MOS capacitor with AlGaN barrier. C_{ob} is equal to the capacitance of the first platform from the C-V curve, which is related to the generation of 2DEG electrons. It is reasonable to use it to calculate peak mobility since the maximum of g_m is obtained near the threshold voltage.

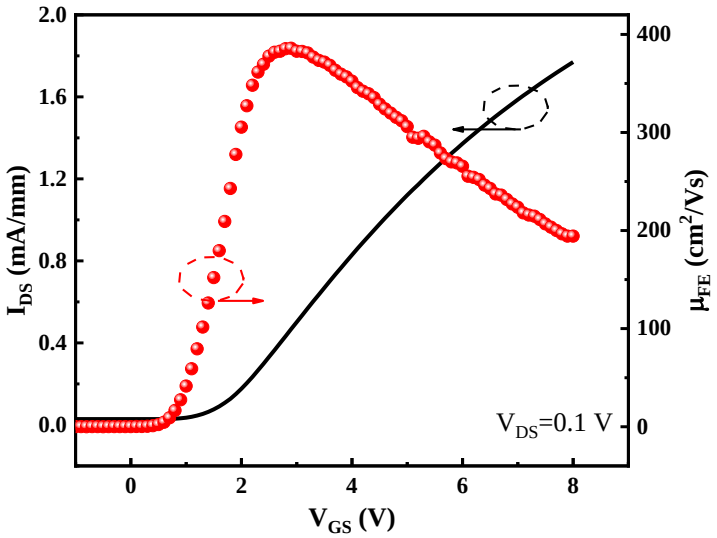


Fig.3.2.2 Transfer curve measured at V_{DS}=0.1 V and the extracted field-effect mobility of a recessed MIS-HFET with 30-μm-long gate length and 100-μm gate width, C_{MOS}=265 nF/cm^2.

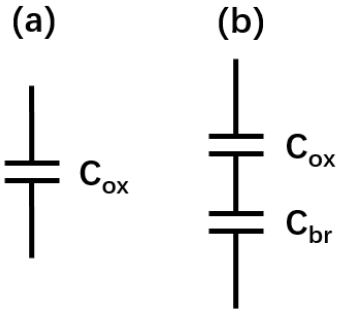


Fig.3.2.3 The circuit diagram of gate capacitance of a GaN MOS capacitor (a) without AlGaN barrier and (b) with AlGaN barrier. C_{ox} is the oxide capacitance and C_{br} is the barrier capacitance of AlGaN layer.

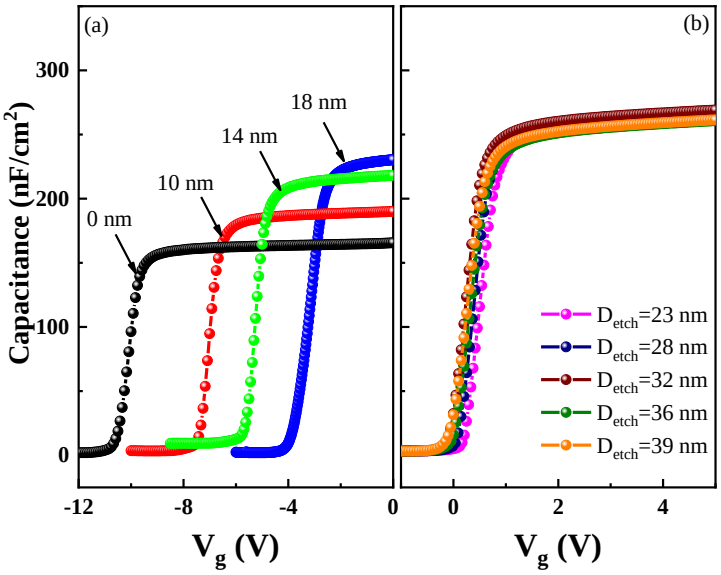


Fig.3.2.4 C-V curves of GaN MOS capacitors with different etch depths at 100 kHz. Etch depth D_{etch} is (a) 0-18 nm, (b) 23-39 nm.

Table 3. 2 Measured C_{ob} or C_{MOS} of GaN MOS capacitors with different etch depths D_{etch}

D_{etch}(nm)	C_{ob} or C_{MOS}	Value (nF/cm^2)
0	C_{ob}	165
10	C_{ob}	190
14	C_{ob}	212
18	C_{ob}	230
23	C_{MOS}	265
28	C_{MOS}	265
32	C_{MOS}	265
36	C_{MOS}	265
39	C_{MOS}	265

To calculate the mobility with different etch depths D_{etch} of AlGaN barrier, C_{ob} or C_{MOS} is measured from GaN MOS capacitors, which were fabricated on the same chip and had the same etch depths with long-gate-length transistors. Fig.3.2.4 gives C-V curves of GaN MOS capacitors with different etch depths, and the C_{ob} or C_{MOS} is summarized in Table 3. 2, which will be used to calculate the channel mobility under different etch depths. The C_{ob} varies from 165 to 230 nF/cm^2 when the etch depth of the AlGaN barrier changes from 0 nm to 18 nm. The C_{MOS} is around 265 nF/cm^2 when the etch depth varies from 23 nm to 39 nm, which is the oxide capacitances and indicates a MOS channel with the removal of barrier and even an over-etch of GaN layer.

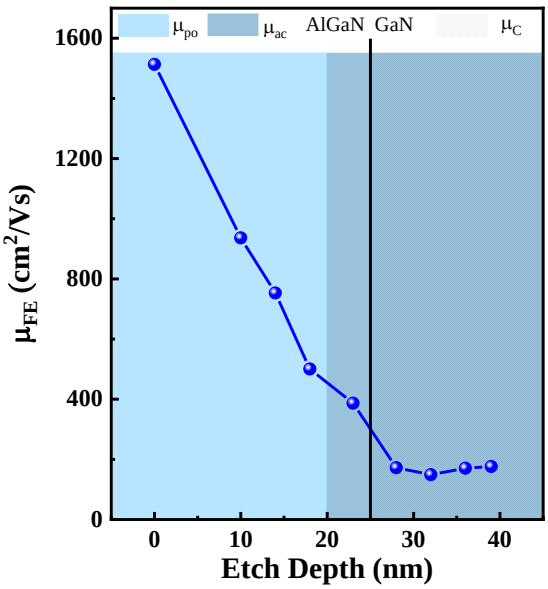


Fig.3.2.5 Peak mobility at different etch depths of AlGaN barrier. (Device with 30-μm-long gate length and 100-μm gate width)

Fig.3.2.5 shows the relationship between field-effect mobility (peak mobility from Fig.3.2.2) and the etch depth at room temperature. As seen in the figure, when the etch depth is 0 nm, the channel mobility is calculated as 1513 cm^2/Vs, which is comparable

with Hall measurement from the commercial data. The channel mobility greatly reduces from 1513 cm^2/Vs to 387 cm^2/Vs when the etch depth varies from 0 nm to 23 nm. The rapid reduction of channel mobility with the etching thickness of AlGaN might be caused by reduced polar-optical-phonon mobility μ_{po} since it is related to the n_s concentration in equation (3.6). The further recess of GaN layer gives relatively stable mobility around 170 cm^2/Vs regardless of etch depths, indicating a different mechanism that is independent on the etch depths. As mentioned before, in the 2DEG channel, the polar-optical-phonon scattering dominates, while interface charges induced Coulomb scattering dominates in the recessed MIS-HFETs. The different colors and regions in Fig.3.2.5 represent different scattering mechanisms under various etch depths, which will be discussed in detail in the next section.

3.2.3 Results and mechanism discussions with different etch depths

Fig.3.2.6 shows the mobility as a function of V_G-V_{th} at various temperatures with different etch depths. When the etch depth D_{etch} is increasing, the peak mobility exhibits a decreasing degradation with temperature. The mobility of the unrecessed channel in Fig.3.2.6 (a) decreases most obviously, from 1513 cm^2/Vs at 25 °C to 437 cm^2/Vs at 200 °C, while the mobility changes slowly with increasing temperature at a depth of 32 nm in Fig.3.2.6 (d). To describe the degree of mobility degradation with the temperature at different etch depths, the log scale of peak mobility μ_{FE} versus T is shown in Fig.3.2.7. The solid lines are linear fitting lines from lnμ~lnT, and the degradation coefficient γ_0 is obtained from the slope of the fitting line. The coefficient γ_0 is calculated to be 2.51,

1.61, 1.44, and 0.91, when the etch depth D_{etch} is 0 nm, 10 nm, 14 nm, and 18 nm, respectively. These fitting parameters are shown in Table 3.1 and used to theoretically calculate the mobility caused by polar-phonon scattering at different etch depths of AlGaN barrier.

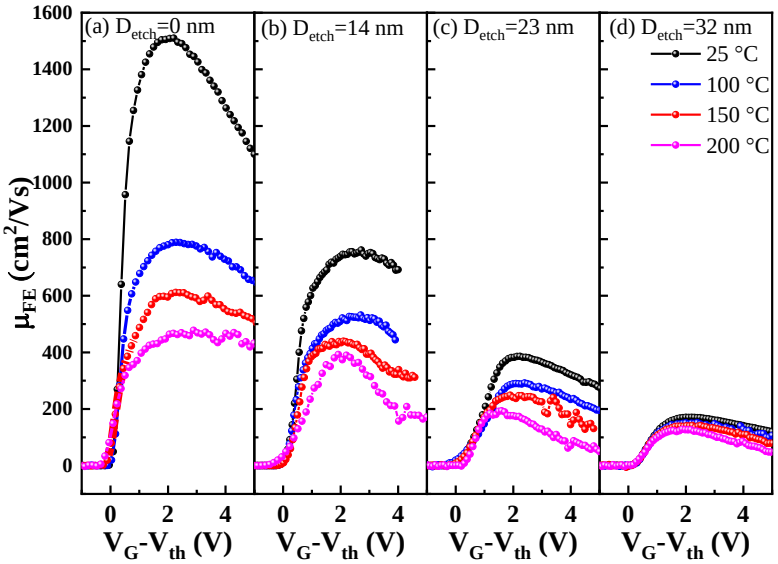


Fig.3.2.6 Mobility as a function of V_G-V_{th} at different temperatures. D_{etch} is (a) 0 nm, (b) 14 nm, (c) 23 nm, and (d) 32 nm.

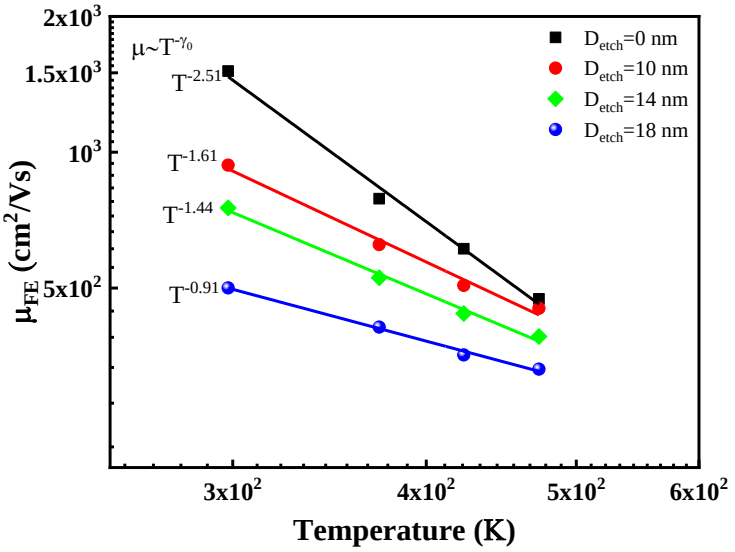


Fig.3.2.7 Log scale of peak mobility versus temperature at different etch depths (D_{etch}) of the AlGaN barrier. Scattering points are experimental results and solid lines are linear fitting lines (lnμ~lnT).

Fig.3.2.8 shows experimental and theoretical peak mobility with different etch depths at various temperatures. Except for the slower mobility degradation with temperature at a larger etch depth of AlGaN barrier, the mobility of over-etched GaN buffer shows similarly small degradation with temperature regardless of the over-etch depths. This indicates large temperature dependence of channel mobility in D-mode devices owing to polar-phonon scattering, however, the recessed channel mobility in E-mode devices exhibits small temperature dependence. The theoretical calculation fits the experimental results very well, indicating good models for different etch depths. Considering a 25 nm thickness of the AlGaN barrier in this work, when the etch is below 20 nm, the polar-phonon model fits well, indicating a dominant scattering mechanism for the 2DEG channel in a wide temperature range, and a wide barrier thickness as well.

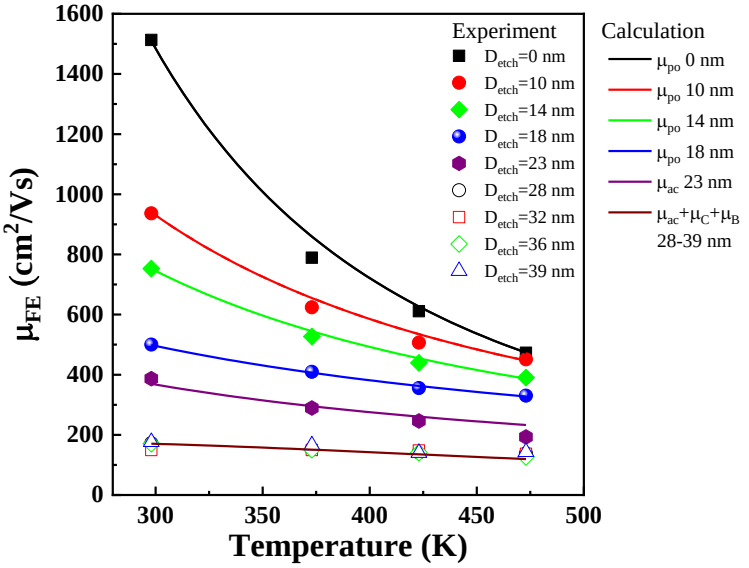


Fig.3.2.8 High-temperature peak mobility of experimental results (scattering points) and theoretical calculation (solid lines) at various etch depths (D_{etch}).

When the etch depth is above 25 nm, the Columb scattering and acoustic phonon

scattering dominate, and the carriers under this situation also can be scattered by bulk material. The bulk mobility μ_B is not a dominant contribution for the recessed channel, since the channel mobility is around 170 cm^2/Vs, much lower than bulk mobility of larger than 1600 cm^2/Vs at room temperature in Fig.3.2.1. The total mobility of combining μ_{ac}, μ_C, and μ_B, fits the experiment well when the etch depth D_{etch} varies from 28 to 39 nm.

When D_{etch} is 23 nm (between 20 and 25 nm), the mobility (as seen in purple points in Fig.3.2.8) is around 387 cm^2/Vs and is slightly higher than 170 cm^2/Vs of the over-recessed channel, which coincides with reference data even with a remaining 2.2 nm barrier [123]. Under this condition, the 2DEG channel does not exist and the polar-optical phonon scattering is not suitable, because the thickness of AlGaN barrier is at least 5-6 nm to form the 2DEG channel [124]. The acoustic scattering model can fit the experiment well, and the Columb scattering is not considered in this situation because the maximum mobility of Columb scattering in Fig.3.2.1 is below 387 cm^2/Vs and not contributed to the total mobility, the detailed explanations are given in the following discussions.

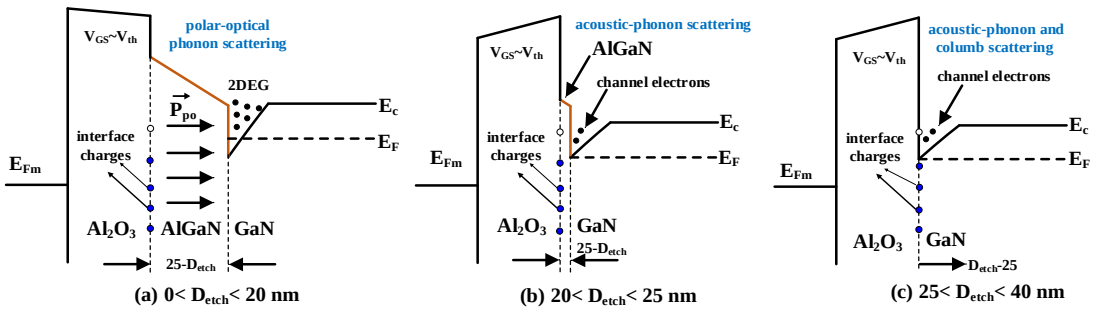


Fig.3.2.9 Schematic band diagrams of different ranges of etch depth D_{etch} (a) 0-20 nm, (b) 20-25 nm, and (c) 25-40 nm.

Fig.3.2.9 gives the schematic band diagrams with different etch depths D_{etch}. When

D_{etch} is at 0~20 nm in Fig.3.2.9 (a), the polarization electric field $\overrightarrow{P_{po}}$ can influence the lattice vibration and scatter the 2DEG carriers, leading to the dominant scattering mechanism. Owing to the spatial separation of interface traps and bulk material from the 2DEG channel, the interface traps induced Columb scattering μ_C , acoustic phonon scattering μ_{ac} , and bulk mobility μ_B are not significant and can be neglected under this situation.

When D_{etch} is at 20~25 nm in Fig.3.2.9 (b), the 2DEG channel no longer exists as mentioned. The interface charges are not dominant factors in this situation owing to the remaining AlGaN barrier and thus the spatial distance from the channel. The conducting carriers are MIS or MOS channel electrons, so acoustic-phonon scattering dominates. When D_{etch} is at 25~40 nm with a further recess of GaN layer in Fig.3.2.9 (c), the barrier is fully removed. The interface traps can influence the movement of channel electrons in terms of Columb scattering, so both acoustic-phonon scattering and Columb scattering are dominant mechanisms. The mapping of mechanisms under different etch depths is also shown in Fig.3.2.5.

3.3. The impact of etch depth on the performance of GaN devices at high temperatures

The metal-insulator-semiconductor (MIS) gate is widely used in GaN power electronic devices owing to reduced leakage current and has been increasingly used in GaN ICs owing to simple integration like CMOS technology. However, the MIS gate scheme has instability issues which are caused by the additional trap states at the

oxide/nitride semiconductor interface. Especially in the process of GaN ICs fabrication, the additional process can increase the instability of GaN devices and ICs. So in this section, the impact of etch depth of barrier on the performance of both discrete D-mode MIS-HEMTs and E-mode MIS-HFETs is studied at various temperatures, and these devices were fabricated on the chips with GaN integrated circuits.

Various papers have been reported to study the temperature-induced instability of D-mode MIS-HEMTs and E-mode MIS-HFETs. However, the results are often contradictory, this might be caused by process differences and thus different effects of trap states in the material structures. A negative V_{th} shift with temperature was observed in D-mode MIS-HEMTs [101, 125] and recessed E-mode MIS-HFETs [125, 126]. A positive threshold shift with temperature was observed in D-mode MIS-HEMTs [127]. The temperature dependence of the threshold voltage exhibited two different regions, a small shift from RT to 100 °C; above 100-150 °C a noticeable negative shift in D-mode MIS-HEMTs with Al_2O_3 [102, 128] and a positive shift with ZrO_2 [102] were observed, indicating different trap mechanisms.

3.3.1 The impact of etch depth on the performance of D-mode MIS-HEMTs

The D-mode MIS-HEMTs were fabricated on three chips with different etch depths (D_{etch}=18 nm, 14 nm, and 10 nm) of the AlGaN barriers, with the structure shown in Fig.3.3.1 (a). The etch depth was verified by atomic force microscopy (AFM) shown in Fig.3.3.1 (b) and (c).

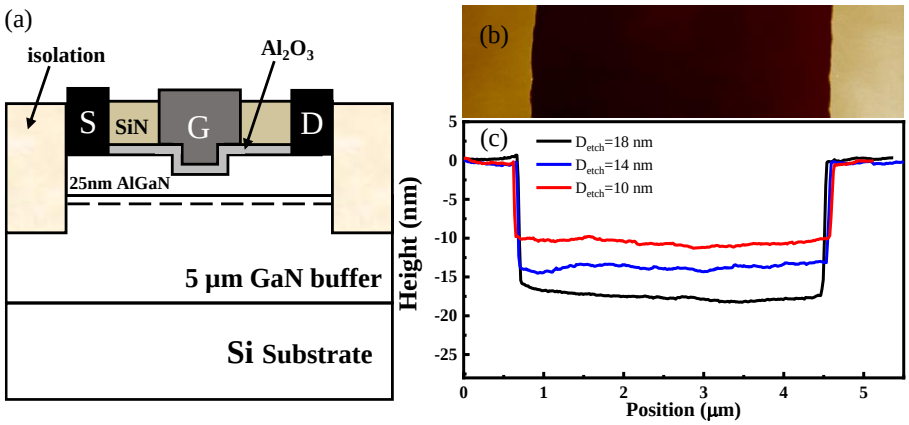


Fig.3.3.1 Schematic diagram of recessed D-mode MIS-HEMTs. (b) Top view of the gate trench, and (c) cross-section profiles of different etch depths of D-mode devices.

Fig.3.3.2 shows the transfer characteristics of recessed D-mode MIS-HEMTs. At room temperature, a positive shift of threshold voltage (linear extrapolation) is observed with increasing etch depth D_{etch}, due to the reduced sheet carrier density [129]. Fig.3.3.3 shows temperature-dependent threshold voltage shift (6 samples) at different etch depths. The difference among the three etch depths can be analyzed through two different temperature regions. From room temperature to 100 °C, the V_{th} of different etch depths changes slowly, which might be caused by traps in the GaN layer [102, 128]. Above 100 °C, the relation between V_{th} and temperature varies a lot at different etch depths. The V_{th} shift (100 °C to 200 °C) is 2.63, 1.86, and 0.67 V when the etch depth D_{etch} is 18, 14, and 10 nm, respectively.

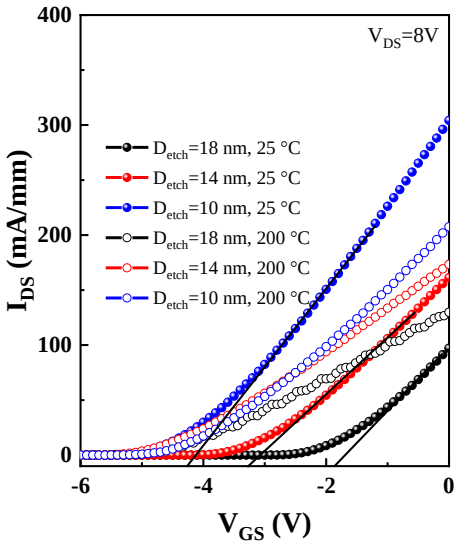


Fig.3.3.2 Transfer characteristics of recessed D-mode MIS-HEMTs with different etch depths. V_{DS}=8 V at 25 °C and 200 °C. (Device dimension: L_{GS} /W_G /L_G /L_{GD} =5/50/3/10 μm).

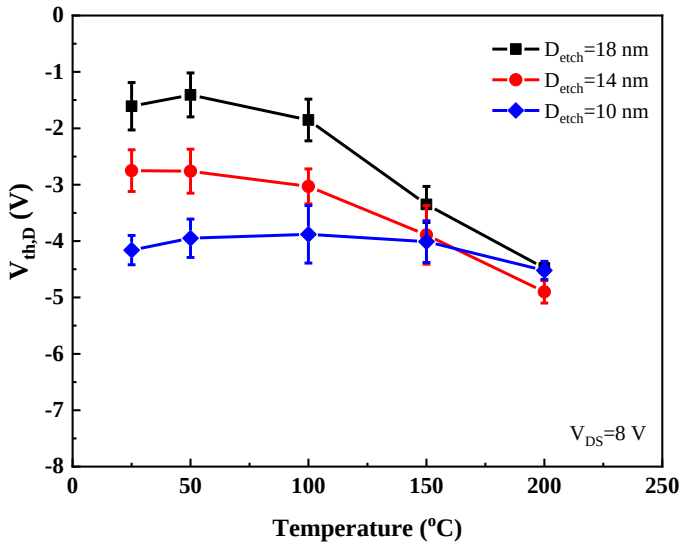


Fig.3.3.3 V_{th} shift of different etch depths of D-mode devices at various temperatures.

Fig.3.3.4 shows the schematic band diagrams of D-mode MIS-HEMTs at different etch depths ($D_{etch,2} > D_{etch,1}$) and different temperatures. At room temperature (T_1), it is reasonable to assume that the interface density is comparable at different etch depths as shown in Fig.3.3.4 (a) and (c). When the temperature increases, the interface traps are thermally sensitive and the electron emission process of the interface traps can be accelerated at higher temperatures [130], as shown in Fig.3.3.4 (b) and (d). Because the

maximum of the gate voltage in Fig.3.3.2 is 0 V, only is the electron emission process considered at elevated temperatures. The relatively deep traps are negatively charged and act like “frozen states” [131], and these deeper charges emit electrons at higher temperatures and result in a reduction of the remained fixed charges. This can reduce the screen effects of fixed charges on 2DEG electrons, and negatively shift the threshold voltage at higher temperatures. With a deeper etch depth of barrier (Fig.3.3.4 (d)), more deep-electrons are emitted, and this can explain the larger V_{th} shift in Fig.3.3.3.

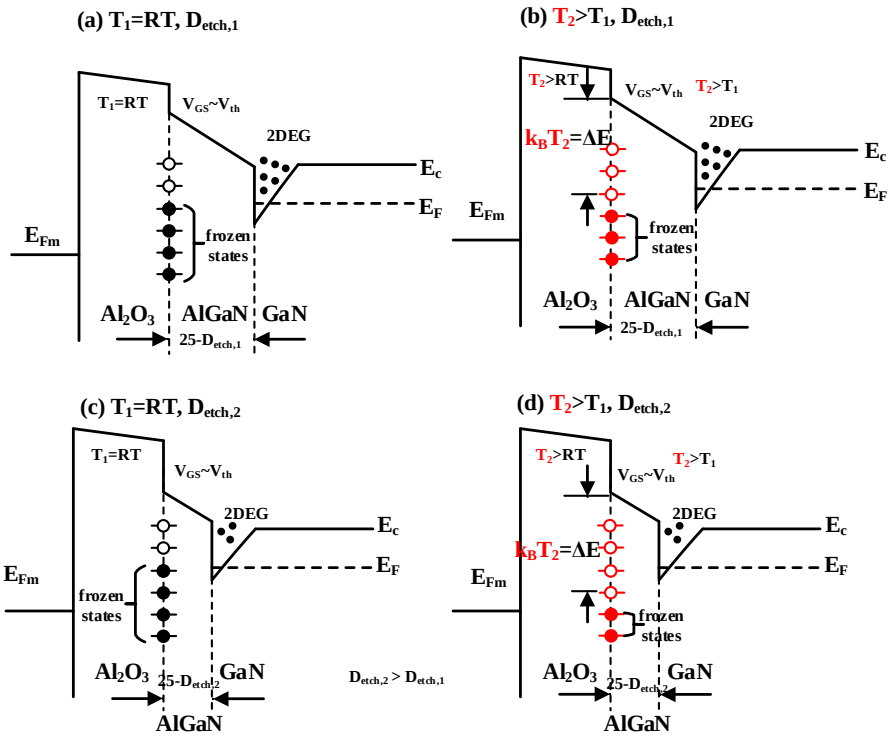


Fig.3.3.4 Schematic band diagrams of recessed D-mode MIS-HEMTs (a) T_1=RT, $D_{etch,1}$, (b) T_2, $D_{etch,1}$, (c) T_1=RT, $D_{etch,2}$, (d) T_2, D_{etch2}. $T_2>T_1$, $D_{etch,2} > D_{etch,1}$.

Fig.3.3.5 shows the maximum drain current $I_{DS,Max}$ (extracted from I_{DS}-V_{DS}) with different etch depths at various temperatures, V_{GS}=0 V. The $I_{DS,Max}$ with a etch depth of 10 nm decreases all over the temperature region, from 282 mA/mm at 25 °C to 150

mA/mm at 200 °C. This is often observed and caused by the thermal degradation of channel mobility [132]. The long-gate-length transistors were fabricated on the same chips with normal size transistors, and the field-effect mobility at different etch depths is systematically studied in section 3.2. The effective mobility of normal size transistors in Fig.3.3.2 should consider the sheet resistance of the access regions in addition to field-effect mobility in Fig.3.2.5. For simplicity, the field-effect mobility in section 3.2 can be used to qualitatively analyze the effective mobility of devices in Fig.3.3.2.

$$I_{DS}\left(\text{sat}\right)=\frac{\mu_D C_{ob}}{2}\frac{W}{L}\left(V_{GS}-V_{th,D}\right)^2 \tag{3.10}$$

Where μ_D is the effective mobility of the D-mode devices, and the drain current-voltage in the saturation region can be expressed using the above equation (3.10). When D_{etch} is 14 nm, the $I_{DS,\,Max}$ first decreases from 187 mA/mm at 25 °C to 153 mA/mm at 100 °C, and then slightly increases to 162 mA/mm at 150 °C, and further decreases to 144 mA/mm at 200 °C. The first decrease at low temperatures might be caused by the degradation of field-effect mobility since the threshold voltage shift is small in Fig.3.3.3. When the temperature increases up to 150 °C, the negative shift of threshold in Fig.3.3.3 will increase the maximum drain current in the equation (3.10). The further decrease of drain current at 200 °C indicates that mobility dominates the drain current and plays a more important role than the threshold voltage shift. When D_{etch} is increased to 18 nm, the $I_{DS,\,Max}$ gradually increases from 106 mA/mm at 25 °C to 142 mA/mm at 150 °C, and then slightly decreases to 130 mA/mm at 200 °C. It can be explained using equation (3.10) as a similar discussion.

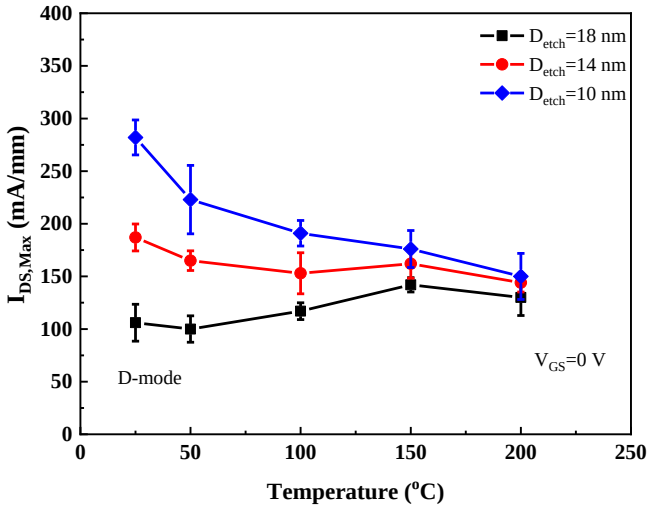


Fig.3.3.5 Maximum drain current (extracted from I_{DS}-V_{DS}) of D-mode devices with different etch depths at various temperatures. V_{GS}=0 V.

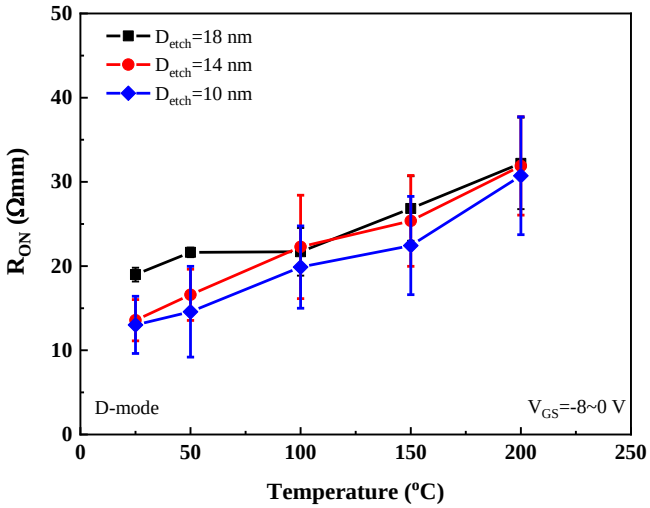


Fig.3.3.6 R_{ON} of D-mode devices with different etch depths at various temperatures. R_{ON} is extracted from I_{DS}-V_{DS}, V_{GS}=-8~0 V.

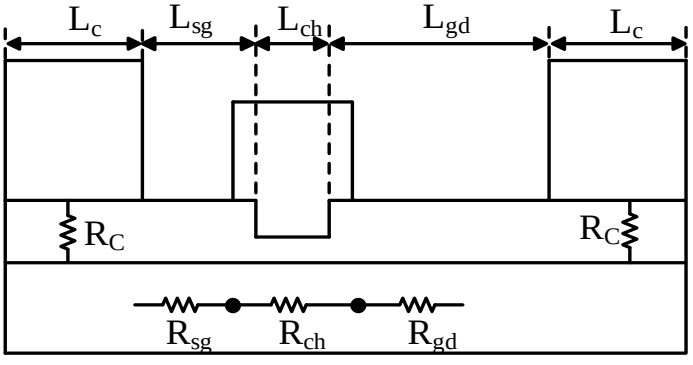


Fig.3.3.7 Schematic of resistance in recessed D-mode gate HEMTs.

Fig.3.3.6 shows on-state resistance R_{ON} (extracted from I_{DS}-V_{DS}, V_{GS} -8~0 V) of

different etch depths at various temperatures. To analyze the impact of etch depth on the R_{ON} of D-mode devices, Fig.3.3.7 shows the schematic of resistance in recessed gate HEMTs, which can also be used in insulated gate MIS-HEMTs. The on-state resistance depends on the resistance and the length of each device region, so R_{ON} can be expressed in the following equation:

$$R_{ON}A = (2R_c + R_{sg} + R_{ch} + R_{gd}) \times (2L_c + L_{sg} + L_{ch} + L_{gd}) \tag{3.11}$$

Where R_C is the contact resistance, R_{ch} is the channel resistance, and R_{sg} and R_{gd} are the source-to-gate and gate-to-drain resistances, respectively. The R_{sg} and R_{gd} can be given by [124]:

$$R_{sg} = \frac{L_{sg}}{q\mu N_{2D}} \tag{3.12}$$

$$R_{gd} = \frac{L_{gd}}{q\mu N_{2D}} \tag{3.13}$$

Where q is an electron charge, μ is electron mobility of 2DEG channel without recess, N_{2D} is 2DEG density at the nonrecessed region. The channel resistance R_{ch} with a recessed MIS gate is given by [124]:

$$R_{ch}(MIS) = \frac{L_{ch}}{\mu C_{gMIS}(V_{gON} - V_{th,MIS} - \phi_{FB})} = \frac{L_{ch}(\frac{t_{ox}}{\varepsilon_0\varepsilon_{ox}} + \frac{t_{AlGaN}}{\varepsilon_0\varepsilon_{AlGaN}})}{\mu(V_{gON} - V_{th,MIS} - \phi_{FB})} \tag{3.14}$$

$$C_{gMIS} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{AlGaN}}} = \frac{1}{\frac{t_{ox}}{\varepsilon_0\varepsilon_{ox}} + \frac{t_{AlGaN}}{\varepsilon_0\varepsilon_{AlGaN}}} \tag{3.15}$$

Where C_{gMIS} or C_{ob} is the MIS gate capacitance, V_{gON} is the on-state gate voltage. Φ_{FB} is the flat-band voltage. $V_{th,MIS}$ is the threshold voltage of the MIS-HEMT. t_{ox}/t_{AlGaN}, and $\varepsilon_{ox}/\varepsilon_{AlGaN}$ are thickness and dielectric constants of the oxide layer/AlGaN layer,

respectively.

As seen in Fig.3.3.6, at room temperature, R_{ON} is 13.02, 13.57 and 18.99 Ωmm with an etch depth D_{etch} of 10, 14, and 18 nm, respectively. The large R_{ON} of 18 nm might be caused by the reduced difference between V_{gON} and V_{th}, and V_{gON} is equal to 0. At low temperatures below 100 °C, the etch depth D_{etch} has some impact on the degradation of R_{ON} with temperature, especially for a large etch depth of 18 nm. When D_{etch} is equal to 10 and 14 nm, the gradual increase of R_{ON} with the temperature might be caused by the degradation of mobility with temperature. However, the much slower increase of R_{ON} with an 18 nm etch depth might be caused by the small V_{gON}-$V_{th,MIS}$ in equation (3.14), which slows down the degradation of R_{ON} with temperature below 100 °C. But above 100 °C, the different etch depths exhibit a similar and comparable increase of R_{ON} with increasing temperatures, despite the V_{th} shift during this temperature region in Fig.3.3.3. This indicates that the etch depth of D-mode devices has little impact on R_{ON}, and resistances in access regions dominate above 100 °C.

3.3.2 The impact of etch depth on the performance of E-mode MIS-HFETs

The E-mode MIS-HFETs were fabricated with different etch depths (23~39 nm) of the AlGaN barriers using digital etching, with the structure shown in Fig.3.3.8 (a). Considering a 25 nm thickness of the AlGaN layer, the digital etching covers a wide range from an under-etch of the AlGaN barrier to an over-etch of GaN layer. The etch depth was verified by AFM as seen in Fig.3.3.8 (b).

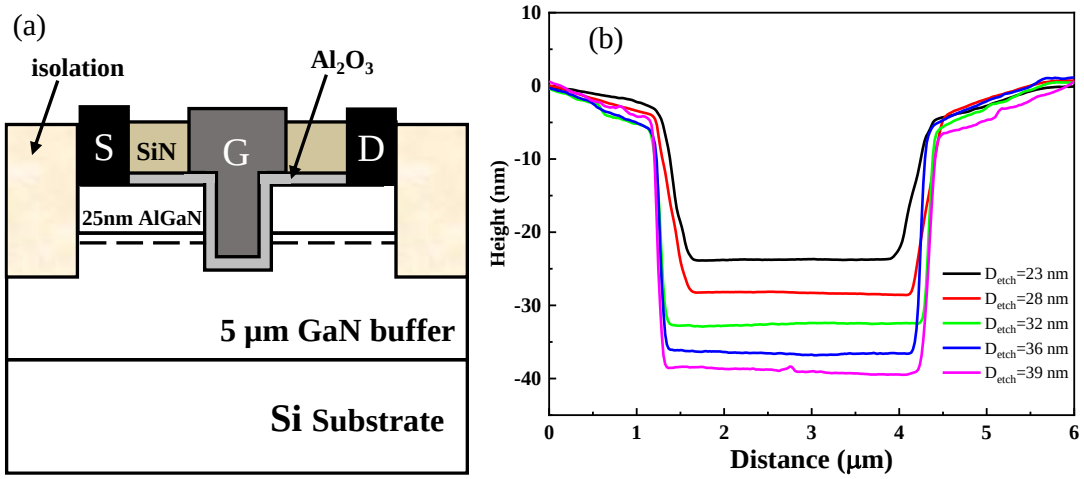


Fig.3.3.8 (a) Schematic diagram and (b) cross-section profiles of different etch depths of recessed E-mode devices.

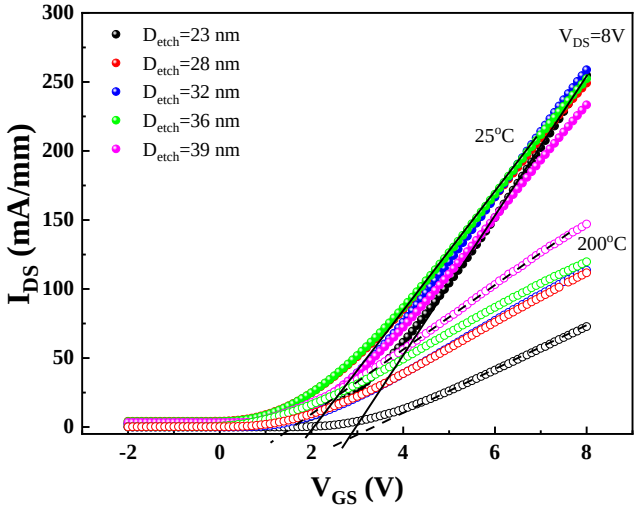


Fig.3.3.9 Transfer characteristics of recessed E-mode MIS-HFETs with different etch depths. V_{DS}=8 V at 25 °C and 200 °C. (Device dimension: L_{GS} /W_G /L_G /L_{GD} =5/50/3/10 μm).

Fig.3.3.9 shows the transfer characteristics of recessed E-mode MIS-HFETs. The threshold voltage is extracted from the linear extrapolation of the I_{DS}-V_{GS}, and the temperature-dependent threshold voltage shift (6 samples) at various etch depths is shown in Fig.3.3.10. The V_{th} shows an increasing trend with temperatures up to 100~150 °C and then decreases at 200 °C. The etch depth of 23 nm shows the overall largest threshold voltages (2.7-3.7 V), and the etch depth of 39 nm shows the lowest

threshold voltages (1.0-1.8V) all over the whole temperature range. The overall temperature-dependent V_{th} shift of E-mode devices is within 1 V and smaller than that of D-mode devices with an etch depth of 14 and 18 nm in Fig.3.3.3.

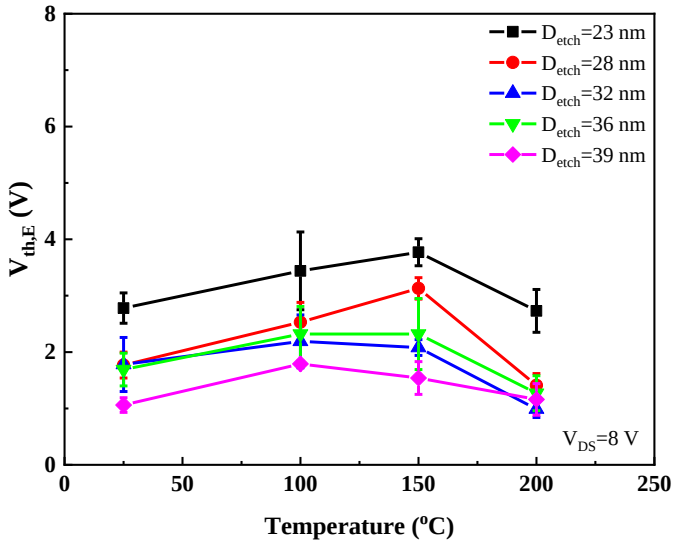


Fig.3.3.10 V_{th} shift of different etch depths of E-mode devices at various temperatures.

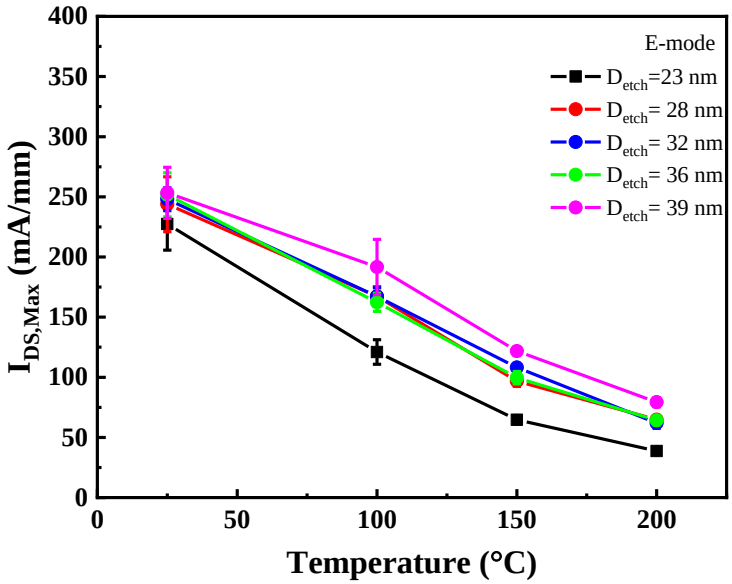


Fig.3.3.11 Maximum drain current (extracted from I_{DS}-V_{DS}) at different etch depths of E-mode devices at various temperatures. V_{GS}=8 V.

The relationship between drain current and gate voltage in recessed E-mode MIS-HFETs can be expressed as:

$$I_{DS}(\text{sat}) = \frac{\mu_E C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{th,E}\right)^2 \tag{3.16}$$

Where μ_E is the effective mobility and $V_{th,\,E}$ is the threshold voltage of E-mode devices. Fig.3.3.11 shows the maximum drain current (extracted from I_{DS}-V_{DS}) at different etch depths of E-mode MIS-HFETs at various temperatures, V_{GS}=8 V. The $I_{DS,Max}$ of different etch depths shows a monotonous decrease with increasing temperatures. According to equation (3.16) with V_{GS}=8 V, a slightly lower drain current of 23 nm etch depth might be caused by smaller V_{GS}-$V_{th,E}$ owing to a large positive threshold voltage in Fig.3.3.10. All devices with different etch depths show a comparable degradation coefficient of 0.85 mA/mm per centigrade (°C), and this might be caused by the thermal degradation of effective channel mobility. This means the etch depth of E-mode MIS-HFETs has little impact on the degradation of drain current at high temperatures. However, the calculated field-effect mobility of recessed E-mode devices with long-gate-length shows small degradation with temperatures owing to reduced screen effects of Columb scattering. This emphasizes the mobility difference between recessed channel only (long gate length) and recessed channel with access regions, and the degradation of drain current with temperature in E-mode devices is attributed to the degradation of resistances in the access regions (source-to-gate and gate-to-drain). So it is required to develop new designs or structures of heterojunction FETs for high-temperature power converters.

In the recessed MIS channel, where AlGaN barrier is supposed to be removed, the channel R_{ch} resistance can be modified from (3.14) as the following equation:

$$R_{ch}(MIS,E) = \frac{L_{ch}}{\mu C_{gMIS}(V_{gON} - V_{th,MIS} - \phi_{FB})} = \frac{L_{ch}t_{ox}}{\mu\varepsilon_0\varepsilon_{ox}(V_{gON} - V_{th,MIS} - \phi_{FB})} \tag{3.17}$$

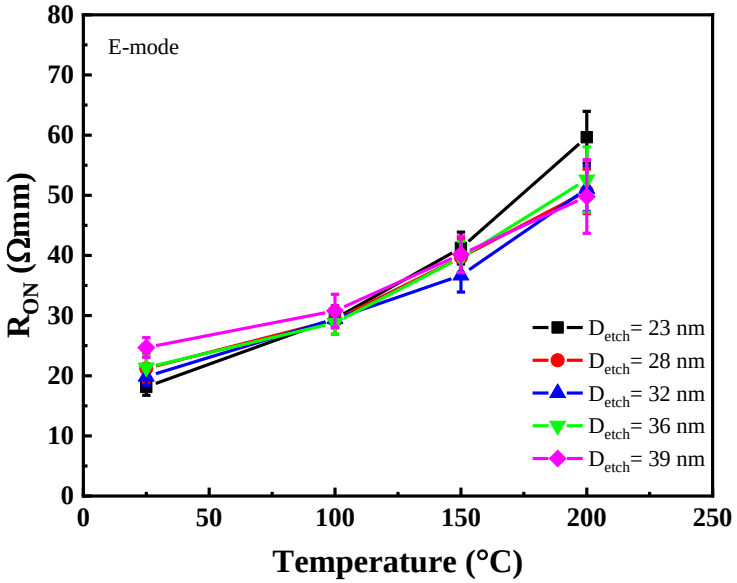


Fig.3.3.12 R_{ON} with different etch depths of E-mode MIS-HFETs at various temperatures. R_{ON} is extracted from I_{DS}-V_{DS}, V_{GS}=0~8 V.

Where the gate capacitance is the oxide capacitance due to the absence of the AlGaN barrier layer. Fig.3.3.12 shows the temperature-dependent R_{ON} with different etch depths of E-mode devices. At room temperature, there's a small difference among different etch depths, however, the discrepancy is much less than the temperature-induced degradation of R_{ON}. At room temperature, the average R_{ON} of five etch depths is 21 Ωmm, and increases up to 52 Ωmm at 200 °C. Considering a small positive threshold voltage of 1~3 V, V_{gON} is equal to 8 V, V_{gON}-$V_{th,MIS}$ in E-mode devices is large enough and has little impact on the degradation of R_{ON} with temperature. The increase of R_{ON} with temperature might be caused by the degradation of effective mobility with temperature in the access regions from equations (3.12) and (3.13) as discussed. The temperature-dependent R_{ON} of D-mode devices in Fig.3.3.6 and E-mode devices in Fig.3.3.12 has no obvious relation with the etch depth of the channel, and it emphasizes the contribution of mobility degradation in access regions.

3.4 The impact of etch depth on characteristics of GaN ICs at high temperatures

The impact of etch depth on the electrical properties of discrete D-mode MIS-HEMTs and E-mode MIS-HFETs is systematically investigated at high temperatures in sections 3.2 and 3.3, in terms of mobility, threshold voltage, drain current, and R_{ON}. The impact of the etch depth on the characteristics of GaN integrated circuits is studied in this section.

3.4.1 The impact of etch depth of D-mode load devices on the performance of GaN DCFL inverters

Fig.3.4.1 (a) shows static voltage transfer curves of the inverters on three chips with different etch depths of D-mode devices, which were fabricated on the same chips with discrete devices in Fig.3.3.1, and all three chips have the same etch depth of 23 nm for E-mode devices. At room temperature, V_{DD}=10 V, three inverters show an output high voltage (V_{OH}) of 10 V and an output low voltage (V_{OL}) around 0.4~0.5 V with an input voltage tolerance of 10 V. This validates the possibility of logic inverters using E-mode GaN-based MIS-HEMTs to be driven by mainstream Si and SiC circuits without any special or additional drivers or level shifters. The etch depth of D-mode devices has less impact on input logic low voltage (V_{IL}). Moreover, the less negative threshold voltage of 18 nm shows a smaller input logic high voltage (V_{IH}) of 1.83 V, which gives a large logic high noise margin ($NM_H=V_{OH}-V_{IH}$) about 8.2 V. Input logic high V_{IH} and input logic low V_{IL} are defined by the voltage at dV_{OUT}/dV_{IN}=-1. However, the low threshold voltage around 1 V of E-mode devices makes the inverter not symmetrical and leads to

a small logic low noise margin ($NM_L=V_{IL}-V_{OL}$) around 0.3 V. So the threshold voltage of E-mode MIS-HEMTs should be at least +4 ~ +5 V to implement 10 V rating GaN inverters.

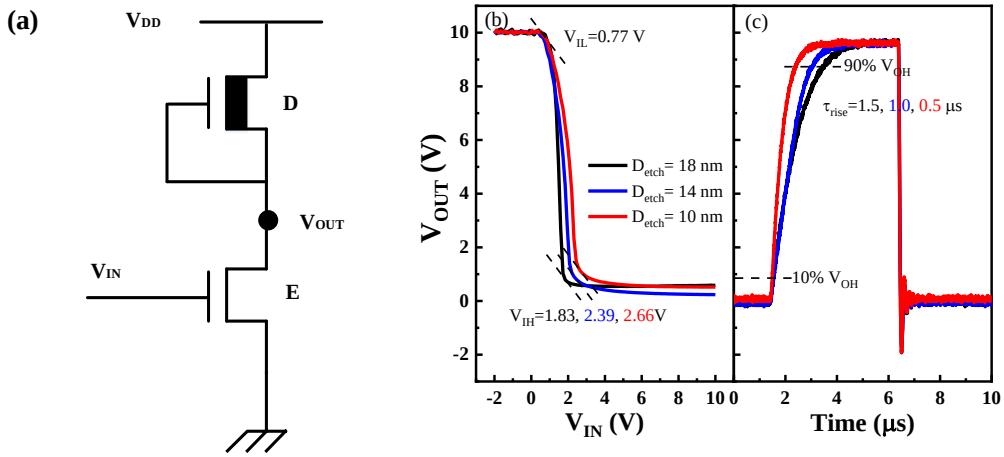


Fig.3.4.1 (a) Circuit diagram, (b) static voltage transfer curve (VTC), and (c) dynamic performance (100 kHz) of a GaN DCFL inverter, D_{etch}=18, 14, 10 nm in D-mode devices. At room temperature, V_{DD}=10 V. (W_D/W_E=5/200 μm).

When D_{etch} is equal to 18 nm in the D-mode device, the dynamic performance of the inverter is seriously degraded in Fig.3.4.1 (c), despite a larger noise margin in Fig.3.4.1 (b). Therefore, careful design should be made to balance the etch depth of D-mode devices and the switching-on speed. At room temperature, the rise times of the DCFL inverters are 1.5 μs, 1 μs, and 0.5 μs for 18, 14, and 10 nm, respectively. The degraded rise times are caused by reduced charging current at V_{GS}= 0 V shown in Fig.3.3.5, where the D-mode devices operate at saturation region. Besides, the etch depth of D-mode devices has small effects on fall times, which are determined by the discharging current of E-mode devices during falling edge.

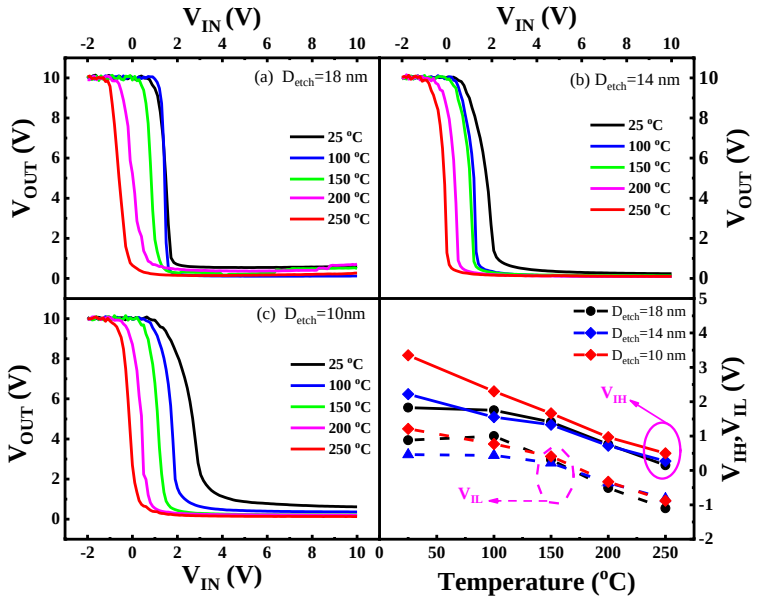


Fig.3.4.2 Static transfer voltage curves of DCFL inverters with different etch depths of D-mode devices from 25 °C to 250 °C, V_{DD}=10 V. D_{etch} is (a) 18 nm, (b) 14 nm, (c) 10 nm, and (d) V_{IH} and V_{IL}.

Fig.3.4.2 shows static VTC of the GaN DCFL inverters with different etch depths of D-mode devices at various temperatures. Both V_{IL} and V_{IH} show negative shifts with temperature. The V_{IL} and V_{IH} of the inverter with depletion-type nMOS load are expressed by [133], can be revised for GaN nMOS inverter as the first order of magnitude approximation:

$$V_{IL} = V_{th,E} + \left(\frac{k_D}{k_E}\right)\cdot\left[V_{OUT} - V_{DD} + \left|V_{th,D}(V_{OUT})\right|\right] \tag{3.18}$$

$$V_{IH} = V_{th,E} + 2\cdot V_{OUT} + \left(\frac{k_D}{k_E}\right)\cdot\left|V_{th,D}(V_{OUT})\right|\cdot\left(\frac{dV_{th,D}}{dV_{OUT}}\right) \tag{3.19}$$

$$\frac{k_D}{k_E} = \frac{\mu_D C_{ob}\left(\frac{W}{L}\right)_D}{\mu_E C_{ox}\left(\frac{W}{L}\right)_E}$$

According to (3.18) and (3.19), the relationship among V_{IH}, V_{IL}, and the temperature is complicated, because $V_{th,D}$, $V_{th,E}$, k_D, and k_E are all temperature-dependent. The detailed relationship between V_{IH}/V_{IL} and temperature in Fig.3.4.2 is hard to explain in

the current study, which will be analyzed in future work.

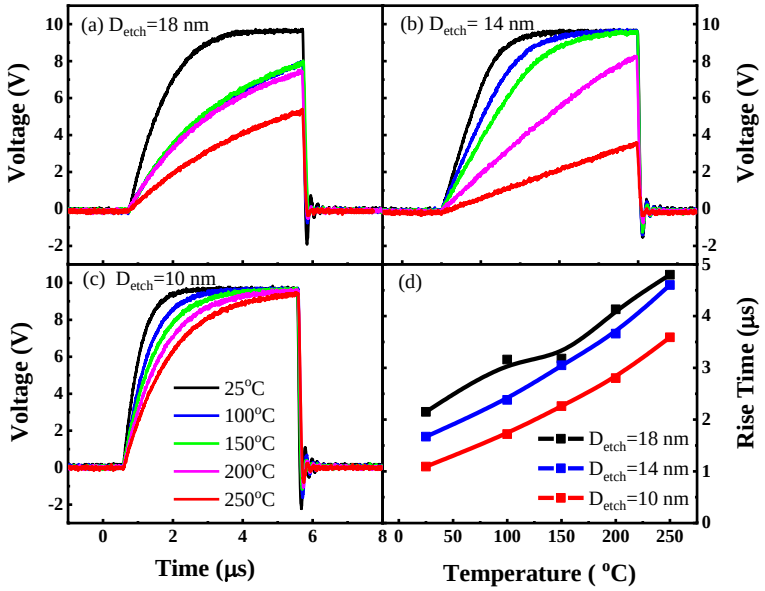


Fig.3.4.3 Dynamic waveforms of DCFL inverters with different etch depths of D-mode devices from 25 °C to 250 °C. f= 100 kHz, V_{DD}=10 V. (a) 18 nm, (b) 14 nm, (c) 10 nm, and (d) rise times (10 % to 90 % V_{OH}) of three chips.

Fig.3.4.3 shows the dynamic characteristics of GaN DCFL inverters with different etch depths of D-mode devices at various temperatures. All the inverters show degraded performances in terms of rise times with increasing temperatures, which might be caused by the degraded current of D-mode devices at high temperatures [59]. The calculated rise times (10% to 90% of V_{OH}) are showed in Fig.3.4.3 (d), the etch depth of 18 nm shows the overall largest rise times all over the temperature region, which might be caused by the reduced charging current of the D-mode active resistor.

3.4.2 The impact of etch depth of driver devices on the performance of GaN DCFL inverter and ICs

A DCFL inverter consists of a D-mode load and an E-mode driver, and the impact of etch depth of the driver device on the performance of GaN DCFL inverters is studied in this section. Fig.3.4.4 shows the static VTC curves of single-stage GaN DCFL inverter with different etch depths of driver transistors (D_{etch}=18, 23 nm), where the D-mode load devices are nonrecessed. When the etch depth is below 20 nm, the VTC curve varies a lot. When the under-etch depth is 18 nm, the logic-high output voltage V_{OH} is 8.4 V, slightly lower than 9 V of V_{DD} power supply, and a negative V_{IL} of -1.8 V is observed as well. The lower V_{OH} and the negative V_{IL} might be caused by the pseudo-E-mode behavior with an under-etch of 18 nm, even though the threshold voltage is positive 0.23 V in Fig.3.4.4 (b). There possibly exists remaining 2DEG carriers when V_{IN} is set as 0 V, and a small current of pseudo-E-mode device pull down a small voltage of V_{OUT} from V_{DD}.

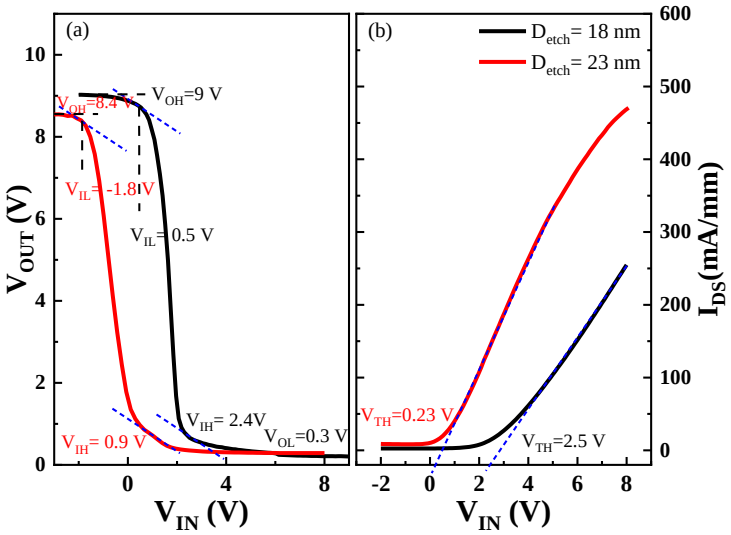


Fig.3.4.4 (a) Static VTC of single-stage DCFL inverter (W_D/W_E, 5/200 μm), (b) transfer characteristics with different etch depths of driver, D_{etch}=18, 23 nm. V_{DD}=9 V.

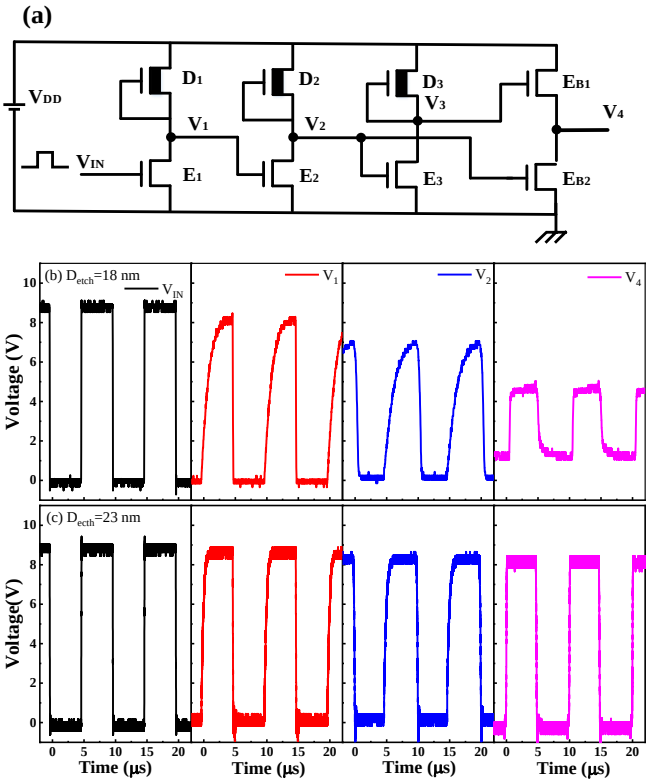


Fig.3.4.5 Dynamic waveforms of one gate driver. (a) circuit diagram, (b) D_{etch}=18 nm, (c) D_{etch}=23 nm. V_{DD}=9 V. f=100 kHz.

To study the impact of etch depth of driver devices on the dynamic performance of gate drivers, a typical driver (Fig.3.4.5 (a)) is used, and the dynamic waveforms of 18 nm under-etch and 23 nm recess are shown in Fig.3.4.5 (b) and (c), respectively. The dynamic waveforms of 18 nm under-etch are greatly degraded after each stage in terms of V_{OH} and V_{OL}, especially for the output signal V_4 of the driver. The 18 nm under-etch can degrade or disable the performance of the GaN drivers, even though the pseudo-E-mode devices have a positive threshold voltage of 0.23 V and a maximum drain current of 471 mA/mm at V_{GS}=8 V in Fig.3.4.4 (b). A 2.2 nm remaining thickness of the AlGaN barrier can also cause an average threshold voltage of negative 0.55 V and V_{th} instability issue [123], owing to the spatial separation between trap states and conducting channel.

So careful attention should be paid when we use recessed MIS gate for integrated GaN converters, under-etch has a great impact on the performance of the drivers. Since the R_{ON} and $I_{DS,Max}$ are not degraded with over-recess of the AlGaN barrier in section 3.3, full-recess of the barrier and interface engineering are recommended in this work to achieve a stable and good performance of integrated GaN drivers. So a full etch depth of 25 nm is recommended in this thesis to improve the stability of E-mode devices and GaN circuits, which is also used in the etching process of GaN ICs in chapters 4, 5, and 6.

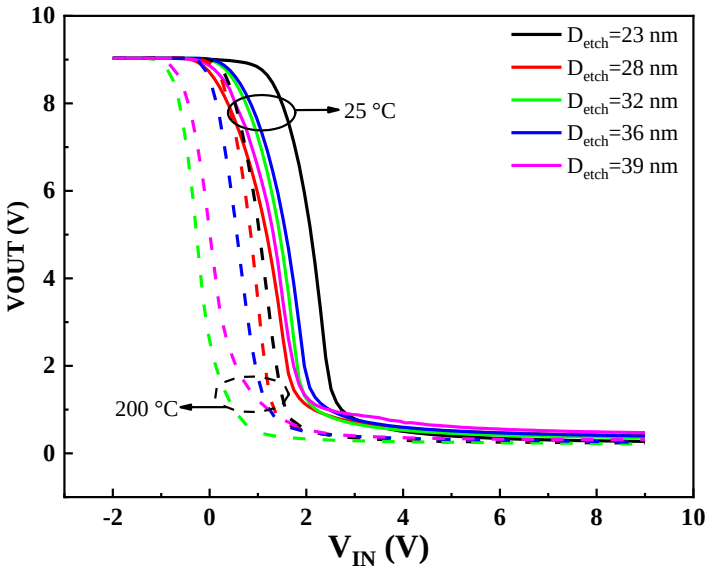


Fig.3.4.6 Static VTC of GaN DCFL inverters of different etch depths (23-39 nm) of E-mode devices at 25 °C and 200 °C. (Inverters: W_D/W_E=5/200 μm).

Fig.3.4.6 shows the impact of etch depths of E-mode devices on the VTC characteristics of GaN DCFL inverters (D_{etch}=23~39 nm). At room temperature, the V_{OH} and V_{OL} of different etch depths are comparable, and there is some difference between V_{IL} and V_{IH}, which might be caused by the threshold voltage difference of E-mode devices in Fig.3.3.10. At 200 °C, all inverters exhibit a negative shift of V_{IL} and

V_{IH} with temperature, which is observed and discussed in Fig.3.4.2. When the etch depth is larger than 23 nm, the etch depth has little impact on R_{ON} and $I_{DS,Max}$, especially at high temperatures as discussed in section 3.3, so the dynamic performance with different etch depths (D_{etch}>23 nm) has no obvious difference.

3.5 Conclusion

The impact of etch depth of AlGaN layer on the performance of GaN-based devices and circuits is systematically studied at various temperatures to evaluate recess MIS gate for HT power converters. The scattering mechanisms with different etch depths are investigated, theoretical models under different etch depths are proposed and fit experiments well, indicating different mechanisms at different etch depths. When the etch depth D_{etch} is less than 20 nm, polar-optical-phonon scattering dominates owing to 2DEG electrons; when D_{etch} is between 20 and 25 nm, the acoustic phonon scattering dominates and starts to play an important role. The interface traps induced Columb scattering starts to affect the channel mobility when D_{etch} is larger than 25 nm. For recessed E-mode devices, the low channel mobility is mainly caused by interface traps caused by Columb scattering and acoustic scattering.

The etch depth (D_{etch}≤20 nm) can affect the performance of D-mode devices, in terms of the threshold voltage V_{th}, R_{ON}, and $I_{DS,Max}$. The etch depth has some impact on R_{ON} at low temperatures below 100 °C owing to the V_{th} shift, however, it has a small impact on R_{ON} above 100 °C. The degradation of R_{ON} above 100 °C is mainly caused by reduced effective channel mobility of the nonrecessed regions. Owing to the removal

of AlGaN barrier, the etch depth (D_{etch}≥20 nm) has small effects on the performance of E-mode devices in terms of R_{ON}, and the degradation at high temperatures is caused by reduced effective channel mobility of access regions.

The etch depth (D_{etch}≤20 nm) in D-mode load devices can influence the performance of GaN DCFL inverters in terms of V_{IH}, rise times, especially at high temperatures. For driver devices, when the under-etch depth D_{etch} is 18 nm (<20 nm), the GaN inverters can be greatly degraded in terms of V_{IL}, V_{OH}, and V_{OL}. The under etch can disable the performance of GaN drivers, even with a positive threshold voltage of driver devices. So full recess with an etch depth of 25 nm is recommended in this thesis to improve the stability of E-mode devices and GaN circuits, and reduce interface traps between Al_2O_3 and the remaining AlGaN barrier.

Chapter 4 Monolithic integration design of GaN-based gate driver for high-temperature DC-DC boost converters

4.1 Motivation

AlGaN/GaN heterojunction-based power transistors have excellent performance in high-frequency and high-temperature operation regimes owing to their superior properties. High-temperature power converters are gaining more and more attention in applications under extreme environments, such as oil drilling, aviation, and hybrid electric vehicles [78, 134-136]. These high-temperature converters require high temperature (HT) gate drivers. The wide bandgap devices, such as SiC or GaN, are promising candidates for HT gate drivers for harsh environmental applications [137]. Commercial gate drivers are normally based on Si Complementary Metal Oxide Semiconductor (CMOS) technology, but these gate drivers cannot operate beyond 125 °C due to the limitation of Si material [136]. Gate driver integrated circuits (ICs) using silicon-on-insulator (SOI) technology can enable SiC converters to operate at temperatures > 200 °C [78]. GaN ICs have shown excellent performance at 250 °C [40, 48, 54] or even higher than 300 °C [36, 45, 81]. For GaN-based power devices, Si and SiC-based drivers do not match GaN fabrication from the process integration point of view. Hence, monolithic integration of GaN-based driver with power switching device on a chip is highly recommended for power high-temperature power converters without heatsink or cooling systems, due to reduced area, parasitic inductances, and

capacitances [56, 85], and low cost as well.

Table 4. 1 Comparison of DC-DC converters with HT gate drivers

Design	**[78]**	**[37]**	**[46]**	**[53]**	**[97]**	**This Work**
Year	2015	2009	2014	2016	2017	2019
Technology	SiC	1.5 μm E-mode GaN-HEMT	0.5 μm E-mode P-AlGaN HEMT	0.15 μm D-mode GaN-HEMT	3 μm E-mode GaN MIS-HFET	3 μm E-mode GaN MIS-HFET
Gate Driver	SOI driver	Not included	GaN driver	GaN driver	GaN driver	GaN driver
Passive	Discrete	Integrated (diode)	Integrated (driver)	Integrated (driver)	Simulated	Integrated (driver)
Converter	Buck	Boost	Buck	Buck	Buck	Boost
V_{IN}/V_{OUT}	600V/N.A	10V/21V	12V/1.8V	20V/14V	100V/50V	5V/11V
$V_{GS,max}$	NR	< 5 V	< 8 V	<5V	15 V	10 V
Temperature	200 °C	RT	RT	RT	200 °C	250 °C
Area	Board	w/o driver	11.7 mm^2	5.52 mm^2	Simulated	2.9 mm^2

Recent studies [37, 46, 53, 78, 97] have been reported to integrate drivers with power transistors for DC-DC converters in Table 4. 1. Although most of these studies exhibit the superior performance of GaN converters at room temperature, seldom reports show converters with integrated GaN drivers for HT applications. Moreover, the GaN boost converter has a large gate swing of 10 V ($V_{GS,max}$) owing to the recessed MIS gate, and this benefits GaN converters in terms of strong noise immunity and less possibility of breakdown. In this chapter, we monolithically integrated GaN-based gate drivers with an E-mode GaN power transistor for HT DC-DC boost converters, to fully exploit the high-temperature performance offered by GaN devices. The E-mode AlGaN/GaN MIS

heterojunction-field-effect-transistors (MIS-HFETs) used in this work can enable strong immunity to large gate overshoots in GaN-based ICs, due to large gate swings [138]. The integrated GaN driver consists of Direct Coupled FET Logic (DCFL) inverters [36, 44-46, 54, 81] and a buffer stage [46, 97, 139]. A detailed study of high-temperature AC performance of integrated GaN drivers and boost converters is presented, and the impact of inverter size and buffer stage width on driving capability is systematically studied. The GaN-based boost converter (V_{IN}/V_{OUT} = 5 V/11 V at 100 kHz) with the optimized gate driver showed good performance even at high temperatures up to 250 °C.

4.2 Design of the proposed GaN DC-DC boost converter

4.2.1 Principle of a DC-DC boost converter

The basic topology of a boost converter using transistor-diode mode is shown in Fig.4.2.1 (a), and the output voltage is higher than the input voltage. When the switch S_0 turns on, the equivalent circuit is shown in Fig.4.2.1 (b). D is the duty cycle when the transistor turns on, the inductor voltage is equal to the input voltage V_{IN}. During the second half cycle (1-D) when the transistor S_0 turns off, the equivalent circuit is shown in Fig.4.2.1 (c). The inductor current goes through the diode, and the inductor voltage is equal to V_{IN} -V_{OUT}-V_F, where V_F is the forward voltage of the diode. The relationship between output voltage V_{OUT} and duty cycle D can be expressed as:

$$V_{OUT} = \frac{V_{IN}}{1-D} - V_F \tag{4.1}$$

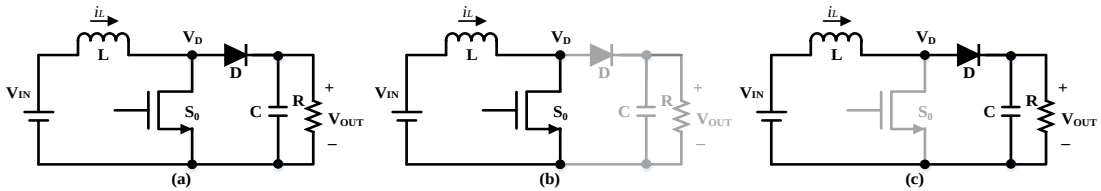


Fig.4.2.1 Boost converter. (a) The circuit diagram, equivalent circuits (b) the switch transistor is on, (c) the switch transistor is off.

To achieve stable output voltage of GaN power converters in continuous conduction mode (CCM), L and C are calculated to obtain small voltage ripples for boost converters. In a boost DC-DC converter, the ratio of voltage ripple to the output voltage can be expressed as [140]:

$$\frac{\Delta V_c}{V_o} = \frac{D}{RCf} \tag{4.2}$$

When D is equal to 0.5, f= 100 kHz, R=500 Ω, choose L=1 mH, C= 10 μF, the voltage ripple using formula (4.2) is calculated as 0.1%.

4.2.2 ADS simulation of the proposed GaN converter

The circuit diagram of the proposed GaN boost converter is shown in Fig.4.2.2. The converter integrates a gate driver. The gate driver is based on driver design from Panasonic Company [46], which consists of DCFL inverters and a buffer stage. A small width of load transistor and a large buffer width can reduce power consumption of gate drivers, in terms of reduced on-state conduction loss of D-mode devices in DCFL inverters, since the buffer only consumes small power at the switching transition and flows no current during on-state operation [46]. Simulation parameters in Fig.4.2.2 will be used to simulate the proposed GaN ICs. At 100 kHz, the simulated results are shown in Fig.4.2.3 at room temperature. The number of GaN DCFL inverters is three, so the

output signal of the driver V_{GS} in Fig.4.2.3 (b) is inversive with the input signal V_G in Fig.4.2.3 (a). When V_{IN} is equal to 5 V, the output voltage of the converter has a start-up time of around 500 μs before stabilization in Fig.4.2.3 (c). The detailed parameters of the proposed gate driver (No.3) are also shown in Table 4. 2. Fig.4.2.4 shows the simulated results and there are some discrepancies between simulation and theoretical calculation (equation (4.1)), which might be caused by the non-optimized model in this work. However, this does not affect the utilization of the model to verify the function ability of the proposed GaN converter.

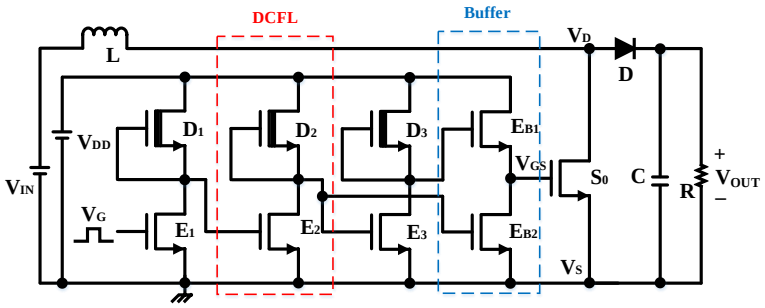


Fig.4.2.2 Circuit diagram of the proposed GaN boost converter with an integrated gate driver. (Simulation parameters: L=1 mH, C=10 μF, R=500 Ω, W_{D1}=W_{D2}=W_{D3}=10 μm, W_{E1}=W_{E2}=W_{E3}=200 μm, W_{EB1}=W_{EB2}=500 μm)

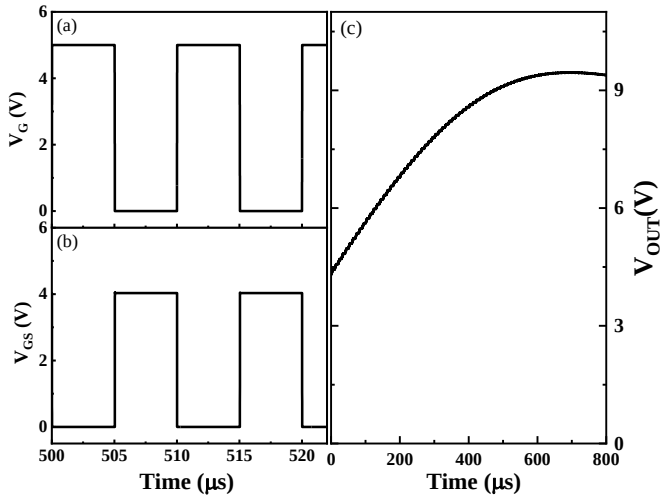


Fig.4.2.3 Simulated waveforms of the GaN boost converter in Fig.4.2.2, f=100 kHz, R=500 Ω.V_{IN}=5 V, D=0.5. (a) Input signal and (b) output signal of the proposed gate driver, (c) output voltage of the GaN boost converter.

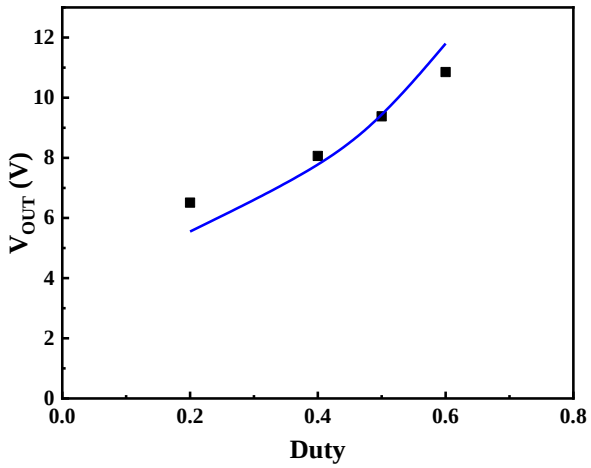


Fig.4.2.4 Simulated output voltages at different duty cycles (theoretical calculation as the blue line) V_{IN}=5 V, R=500 Ω, f=100 kHz.

4.2.3 Different designs of gate drivers and experimental results

Four different gate drivers shown in Table 4. 2 are designed and evaluated in this chapter, to study the impact of driver sizing on the performance of GaN drivers and converters. These drivers include different transistor sizes and the implementation of the buffer stage. In Fig.3.2.5, at room temperature, the peak mobility of the recessed channel is 172 cm^2/Vs, which is almost 9 times less than 1513 cm^2/Vs of the un-recessed channel. This indicates the requirement of large width of the E-mode driver to match the D-mode load current in a GaN DCFL inverter. Using recessed MIS-gate, the width ratio W_E/W_D should be larger than 20 to obtain a smaller rise time [141], where W_E and W_D are E-mode driver width and D-mode load width. In this chapter, the width ratio W_E/W_D is larger than 20 in four drivers. Drivers No.3 and No.4 have the same structure with a buffer stage, which are based on the reported gate driver [46]. Drivers No.3 and No.4 are compared to investigate the impact of driver width on the switching

characteristics of GaN gate drivers and converters.

The four drivers in Table 4. 2 were fabricated on the same chip, and the detailed fabrication process is the same process flow with the GaN DCFL inverter in Fig. 2.2.3. The E-mode devices were achieved through a recessed MIS-gate technique with a full etch depth of 25 nm.

Table 4. 2 A list of four types of integrated drivers

Design	No. 1	No. 2	No. 3	No. 4
D/E mode width (DCFL inverter)	10/200 μm	50/2000 μm	10/200 μm	50/2000 μm
Number of inverters	2	2	3	3
Buffer width (E_{B1} and E_{B2})	No	No	500 μm	2000 μm

The circuit diagram of driver measurement (No.3) is shown in Fig.4.2.5, and the dynamic output waveforms V_{GS} for 4 different drivers are shown in Fig.4.2.6 (a). V_{GS} refers to the voltage between the output voltage of each gate driver and ground, which is equal to the voltage applied to the power switching device. Although the boost converter has a large swing of 10 V in this work, here a maximum gate-to-source voltage ($V_{GS,max}$) of 5 V is used to compare different drivers since the input voltage of the converters is 5 V. At room temperature with a frequency of 100 kHz, all drivers have similar rise and fall times (< 0.5 μs), except No. 1 which has a larger rise time around 2 μs but a relatively small fall time (< 0.5 μs). The large rise time of driver No. 1 is due to the small width of 10 μm in D-mode devices, and has no relationship with the width of E-mode devices as shown in Fig.4.2.6 (b). The rise time of single-stage inverters, which have the same D-mode width (10 μm) as No. 1, is almost unchanged for different

D-mode widths of inverters, ranged from 100 μm to 500 μm. Additionally, increasing the width of D-mode devices (driver No. 2) can reduce the rise time to less than 0.5 μs compared to driver No.1.

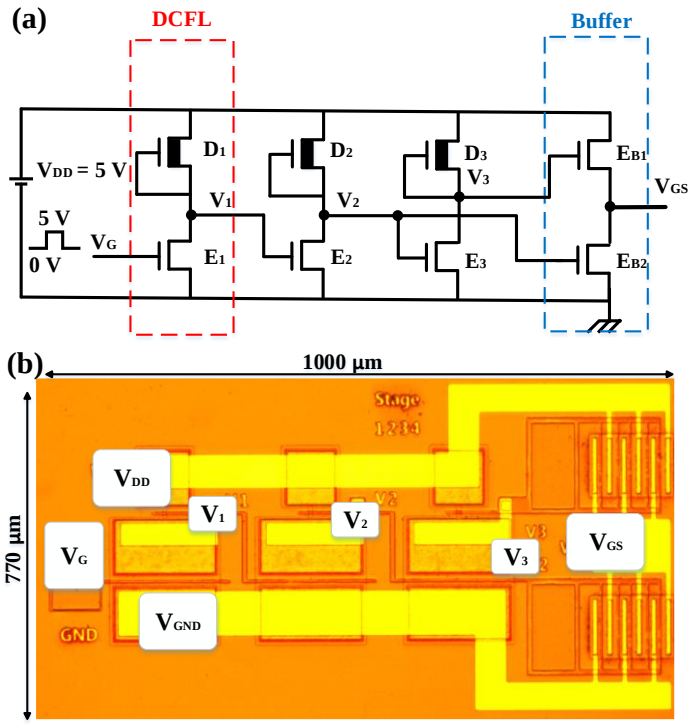


Fig.4.2.5 The circuit diagram and a photograph of fabricated driver No. 3. (a) Circuit diagram, (b) micro-photograph.

With a buffer stage (width=500 μm), the rise time of driver No. 3 can be greatly reduced from 2 μs (V_1, V_2, and V_3) to less than 0.5 μs (V_{GS}) in Fig.4.2.6 (c). A large buffer width of driver No. 4 (width=2000 μm) can further decrease rise time owing to the large gate charging current. However, a very large gate voltage overshoot and an increased oscillation during turn-on transition are observed in Fig.4.2.6 (a) (red line). Unfortunately, the gate voltage overshoot can seriously damage or breakdown switching transistors [17], especially for low gate voltage tolerance transistors, such as HEMTs or P-GaN HEMTs, which usually show $V_{G,\,max}$ less than 7 V [84]. GaN-based

MIS-HEMTs can increase gate overshoot tolerance due to the insertion of the gate dielectric, which can increase gate swing [142]. Additionally, the increased oscillation of driver No. 4 during turn-off transition can cause false turn-on of switching transistor, which can consequently affect the duty cycle and stability of converters. Hence, the balance between switching speed and oscillation requires careful consideration during the design process of the driver.

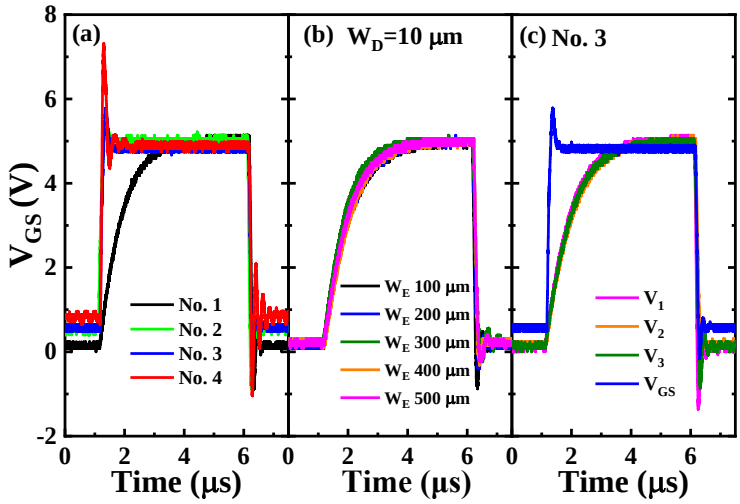


Fig.4.2.6 Experimental results of (a) dynamic V_{GS} waveforms of 4 drivers. (b) Output waveforms with different E-mode widths of discrete single-stage inverters fabricated on the same chip (width of D-mode: W_D=10 µm). (c) Voltage waveforms at each stage of driver No. 3, $V_{G,max}$=5 V, V_{DD}=5 V, f= 100 kHz, and duty cycle=0.5 at room temperature.

4.2.4 Theoretical calculation

The relationship between the size of gate drivers and rise/fall time in Fig.4.2.6 can be qualitatively analyzed by the following discussion. The τ_{rise} and τ_{fall} estimation is derived based on an nMOSFET inverter consisting of an enhancement-mode nMOS driver and a depletion-mode nMOS load [133], the detailed derivation is shown in

Appendix A. The time calculation of GaN drivers with DCFL inverters w/o buffer stage (No. 1 and No. 2) can be expressed by the following formulas:

$$\tau_{rise} = \frac{C_L}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D f\left(V_{DD}, V_{th,D}\right) \tag{4.3}$$

$$f\left(V_{DD}, V_{th,D}\right) = \frac{1}{\left|V_{th,D}\right|}\left[\ln\left(\frac{7.2V_{DD}}{2\left|V_{th,D}\right| - 0.9V_{DD}} + 9\right)\right]$$

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E g(V_{DD}, V_{th,E}) \tag{4.4}$$

$$g\left(V_{DD}, V_{th,E}\right) = \frac{1}{(V_{DD} - V_{th,E})}\left\{\frac{2\left(V_{th,E} - 0.1V_{DD}\right)}{(V_{DD} - V_{th,E})} + \ln\left(\frac{2(V_{DD} - V_{th,E}) - 0.1V_{DD}}{0.1V_{DD}}\right)\right\}.$$

The rise and fall time of drivers with a buffer stage (No. 3 and No. 4) can be obtained by formula (4.5) and (4.6), respectively:

$$\tau_{rise} = \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB1} F\left(V_{DD}, V_{th,E}\right) \tag{4.5}$$

$$F\left(V_{DD}, V_{th.E}\right) = \frac{V_{DD} - 2V_{th,E}}{\left|0.1V_{DD} - V_{th,E}\right|\left(0.9V_{DD} - V_{th,E}\right)}$$

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB2} g(V_{DD}, V_{th,E}) \tag{4.6}$$

$$g(V_{DD}, V_{th,E}) = \frac{1}{(V_{DD} - V_{th,E})}\left\{\frac{2\left(V_{th,E} - 0.1V_{DD}\right)}{(V_{DD} - V_{th,E})} + \ln\left(\frac{2(V_{DD} - V_{th,E}) - 0.1V_{DD}}{0.1V_{DD}}\right)\right\}.$$

C_L is the output load capacitance, C_{ox} is the oxide capacitance, C_{br} is the barrier capacitance leading to the modification of oxide capacitance as $C_{ob} = (C_{ox}{}^{-1} + C_{br}{}^{-1})^{-1}$, C_{int} is the interconnection capacitance, μ_D and μ_E are the effective mobility of D-mode and E-mode devices, respectively. $V_{th,D}$ and $V_{th,E}$ are the threshold voltages of D-mode and E-mode devices, respectively. $\left(\frac{L}{W}\right)_D$ is the gate length/width ratio of D-mode devices, and $\left(\frac{L}{W}\right)_E$ is the gate length/width ratio of E-mode devices. $f(V_{DD,}V_{th,D})$, $g(V_{DD,}V_{th,E})$ and

$F(V_{DD,}V_{th,E})$ are size-independent functions. Considering that the C_L is increasing with the device dimensions, formula (4.3) and (4.4) without (w/o) buffer can be simplified as (4.7) and (4.8), while formula (4.5) and (4.6) with a buffer can be simplified as (4.9) and (4.8), respectively:

$$\tau_{rise} \propto \frac{C_{int}}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D f(V_{DD}, V_{th,D}) \tag{4.7}$$

$$\tau_{fall} \propto \frac{L^2}{\mu_E} g(V_{DD}, V_{th,E}) \tag{4.8}$$

$$\tau_{rise} \propto \frac{2L^2}{\mu_E} F\left(V_{DD}, V_{th,E}\right). \tag{4.9}$$

For drivers w/o buffer stage (No. 1 and No. 2), τ_{rise} is only related to the size of the D-mode active resistor. Considering all drivers share the same gate length, τ_{rise} is thus inversely proportional to the gate width of D-mode devices from formula (4.7). This can explain that driver No. 2 with a larger D-mode width has a smaller rise time compared to driver No. 1 in Fig.4.2.6 (a). In formula (4.8), τ_{fall} is only related to the E-mode transistors due to discharging current during falling edge. τ_{fall} is proportional to L^2 and independent on gate width, which coincides with Fig.4.2.6 (a), where all drivers have a similar fall time of less than 0.5 μs regardless of width difference.

For gate drivers with buffer stage (No. 3 and No. 4) in formulas (4.9) and (4.8), both rise time and fall time are independent of gate width. Additionally, the rise time of driver No. 3 can be obviously reduced due to the high charging current through the upper E_{B1} device during the rising edge, compared to driver No. 1.

4.2.5 Characteristics of drivers at high temperatures

Fig.4.2.7 shows dynamic V_{GS} waveforms at high temperatures from 25 °C, and 100 to 250 °C in 50 °C steps. In Fig.4.2.7 (a), driver No. 1 shows obvious temperature degradation, especially for the rise time. In Fig.4.2.7 (b), the rise time of driver No. 2 has been improved compared to No. 1, but still shows temperature degradation of the rise time to some extent. In Fig.4.2.7 (c), with a buffer stage, driver No. 3 shows negligible rise time degradation even at high temperatures. This indicates the importance of the buffer stage, especially for high-temperature applications, because the gate overshoot will be reduced due to current degradation at high temperatures leading to a low switching-on speed of the driver in Fig.4.2.7 (b). The good thermal stability of driver No.3 might be caused by fast switching speed, low voltage overshoots and oscillations as mentioned. The better thermal stability of E-mode devices than D-mode devices also has some contribution, and this indicates the advantage of the buffer stage on the thermal stability of gate drivers.

However, if the buffer width is too large, such as driver No. 4 in Fig.4.2.7 (d), the gate overshoot and oscillation will be of concern as previously discussed, despite the high switching speed. The low on-state $V_{GS,max}$ around 3 V of driver No. 4 at 250 °C is possibly caused by the large width (2000 μm) of E-mode devices in DCFL inverters, which might lead to a higher V_{OL} of the inverters, and V_{OL} is the voltage when output is low. As shown in Fig.4.2.7, driver No. 1 and No. 3 (E-mode width 200 μm in DCFL inverters) have a V_{OL} of less than 0.25 V, while driver No. 2 and driver No. 4 (E-mode width 2000 μm in DCFL inverters) have a V_{OL} of 0.5~0.8 V. The higher V_{OL} of DCFL

inverters in driver No. 4 might cause the E_{B2} device flow nonnegligible current at on-state, especially at high temperatures due to the negative shift of the threshold voltage [97]. This might consequently cause the lower $V_{GS,max}$ at 250 °C of driver No. 4 at on-state due to voltage division principle.

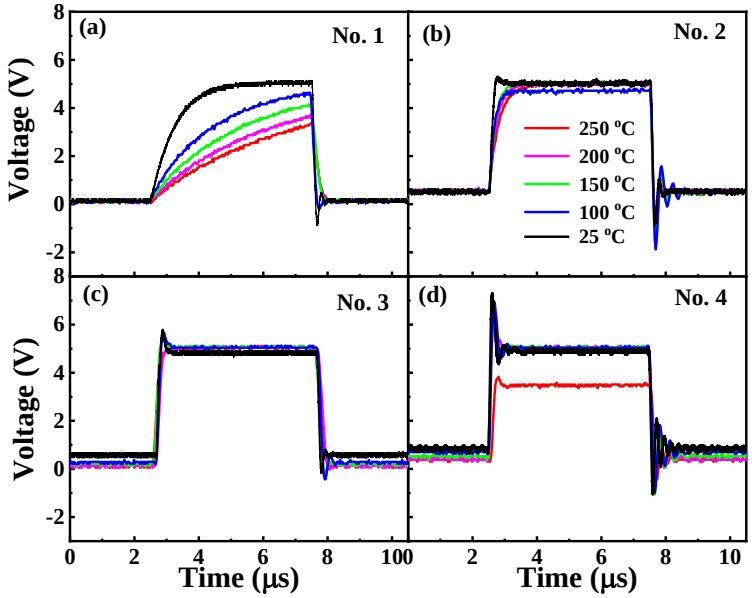


Fig.4.2.7 Dynamic V_{GS} waveforms of different gate drivers at a measured temperature range from 25 °C to 250 °C. (a) Driver No. 1, (b) driver No. 2, (c) driver No. 3, and (d) driver No. 4.

Fig.4.2.8 shows calculated rise times and fall times of four drivers at various temperatures, where the calculation refers to the first slope of rising edge (10 % to 90 % stable V_{OUT}) and falling edge (90 % to 10 % stable V_{OUT}), regardless of oscillation. At room temperature, all drivers show similar fall times around 0.1 μs, hence we use fall time here for simplicity to estimate the load capacitance C_L using either formula (4.6) or (4.8). Given V_{DD}=5 V and $V_{th,E}$=1.5 V, the g(V_{DD}, $V_{th,E}$) is calculated to be 0.89 V^{-1}. Furthermore, μ_E=251 $cm^2V^{-1}s^{-1}$ was reported using a similar digital-etching technique [143]. C_{ox} was measured as 308 $nFcm^{-2}$ from a recessed Al_2O_3/GaN MOS capacitor,

which was fabricated on the same chip with GaN ICs. Using the parameter values above, the calculated C_L is found to be around 6 nF (Fig.4.2.8). Driver No. 1 shows the highest rise and fall times, and driver No. 4 with a large buffer width shows the lowest fall and rise times of less than 0.2 μs due to high current transition. Driver No. 2 shows small fall times but relatively high rise times of more than 0.5 μs at 250 °C, due to the absence of the buffer stage as in the previous discussion. Driver No. 3 shows relatively low rise and fall times of less than 0.25 μs across the whole temperature range.

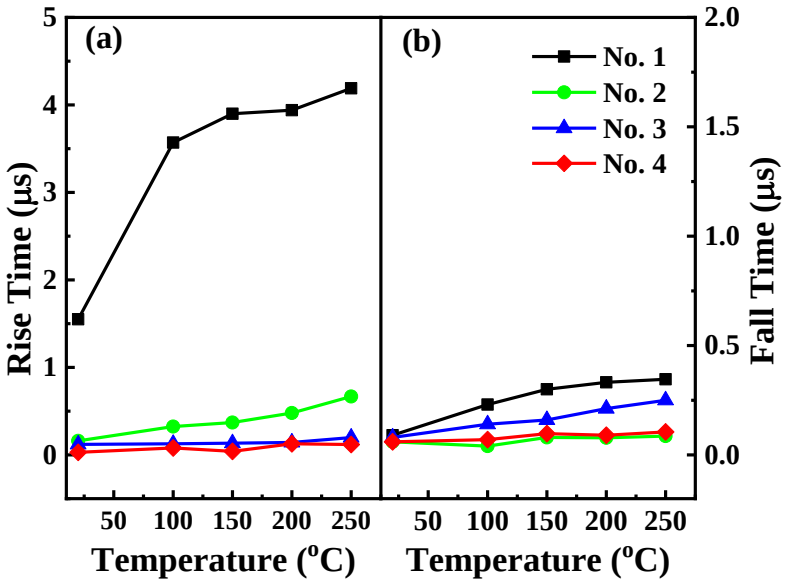


Fig.4.2.8 Rise/fall time of different drivers at various temperatures. (a) Rise time (10 % to 90 % stable V_{OUT}), (b) fall time (90 % to 10 % stable V_{OUT}). The load capacitance C_L is ~6 nF as calculated.

4.3 Results of the proposed GaN converter with an integrated gate driver

4.3.1 Experiment and measurement

Fig.4.3.1 (a) shows the circuit diagram of the boost converter with an E-mode switching transistor S_0 (width =5 mm) and an integrated driver No. 3. The gate drivers

and the power transistor S_0 were fabricated on the same chip, but here we separate them in the diagram in order to distinguish the two parts. Fig.4.3.1 (b) shows the experimental setup for the boost converter. The inductor *L*, diode *D*, capacitor, and load resistor *R* were integrated on a PCB board, the gate drivers and transistor S_0 were externally connected with external components of the PCB board using probes, and the negative electrodes of power supply are connected to the common ground GND. Differential voltage probes were used to detect the dynamic inductance and output voltages in an oscilloscope.

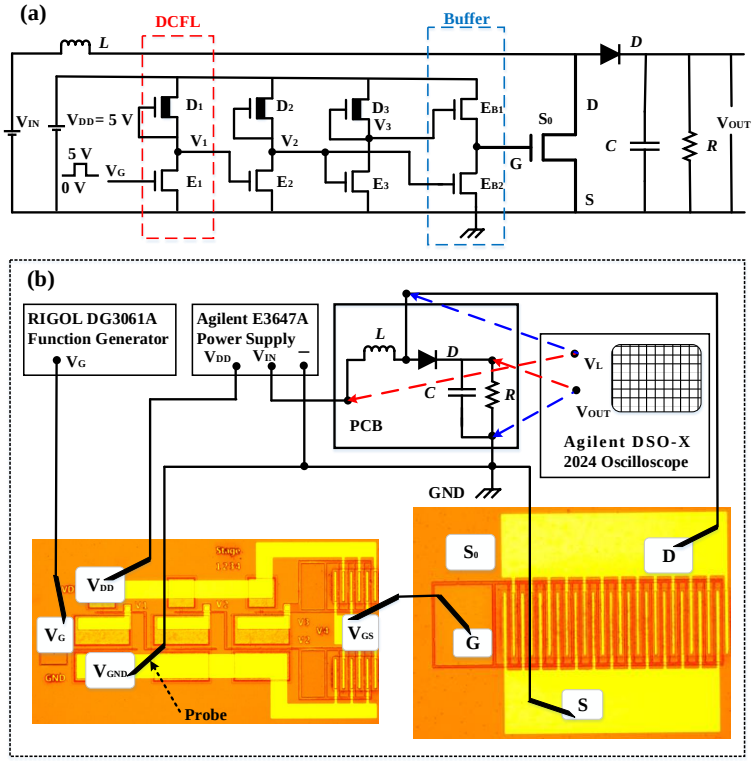


Fig.4.3.1 (a) The circuit diagram of the DC-DC boost converter with the integrated driver No. 3. (b) The experimental setup. (The parameters of discrete components are: L=1 mH, C =10 μF, R=500 Ω. V_{IN}=V_{DD}=5 V, f =100 kHz, the threshold voltage V_F of the discrete diode D (FR107) is +0.7 V, the maximum DC voltage and current are 1000 V and 1 A, respectively).

4.3.2 Converter results at high temperatures

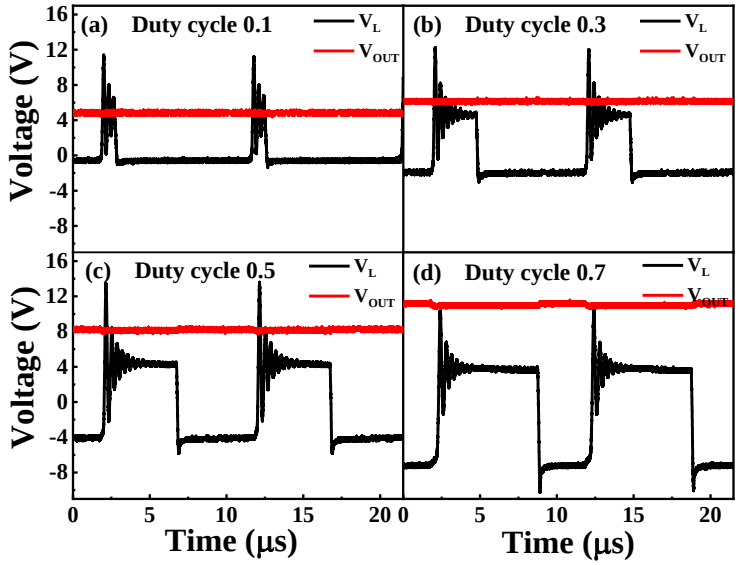


Fig.4.3.2 At room temperature, waveforms of boost converters with integrated gate driver No. 3 at different duty cycles. (a) D= 0.1, (b) D= 0.3, (c) D= 0.5 and (d) D= 0.7. V_L is the voltage at the inductor *L*.

At room temperature, Fig.4.3.2 shows the output voltage and dynamic inductor waveforms of driver No. 3 with duty cycles of 0.1, 0.3, 0.5, and 0.7 at V_{GS}, these corresponding to duty cycles of 0.9, 0.7, 0.5, and 0.3 at V_G, respectively. For direct comparison between four drivers with different numbers of inverter stages, here we use duty cycles of output waveform V_{GS} of each driver. In Fig.4.3.2, the output voltage V_{OUT} is increasing with duty cycles as expected. At room temperature, the converter results of different drivers are shown in Fig.4.3.3. The calculated values using formula (4.1) at different duty cycles are also plotted in the same figure for comparison. The total area under the inductor voltage waveform is zero whenever the converter operates in steady-state, so the following formulas can be obtained:

$$\int_0^{T_s} v_L(t)\,dt = 0$$

$$V_{IN} \times \mathrm{D} + \left(V_{IN} - V_{OUT} - 0.7\right) \times \left(1 - D\right) = 0$$

$$V_{OUT} = \frac{V_{IN}}{1-D} - 0.7 \tag{4.1}$$

In Fig.4.3.3, the experimental results are comparable with calculated values at low duty cycles (D= 0.1 and 0.3), but lower than calculated values at high duty cycles (D= 0.5 and 0.7). The discrepancies increase with duty cycles, which might be caused by reduced inductance voltage at on-state as shown in the inset of Fig.4.3.3 (referring to the enlarged view of Fig.4.3.2). The reduced inductance voltage might be caused by the increased on-state voltage drop between drain and source of the S_0 transistor, owing to not low enough on-state resistance in this work. However, this does not affect the studies of gate drivers because all drivers share the same switching transistor S_0 in this work.

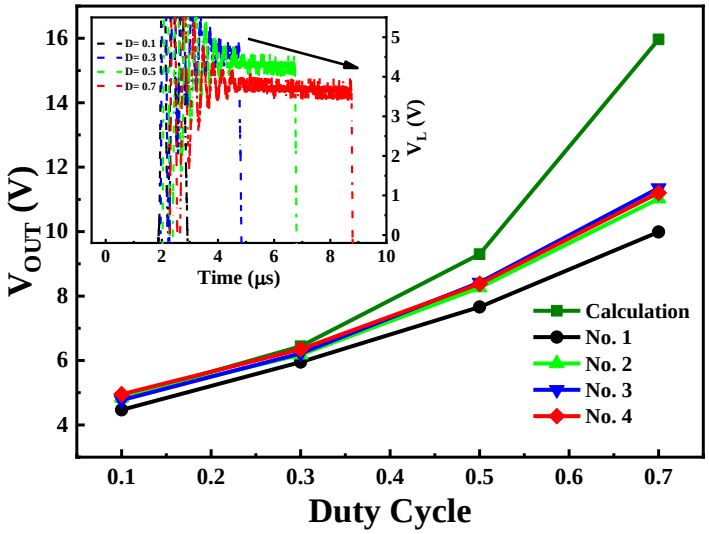


Fig.4.3.3 Experimental and theoretical results of V_{OUT} vs duty cycle from different drivers at room temperature. The inset shows an enlarged view of V_L at different duty cycles from Fig.4.3.2.

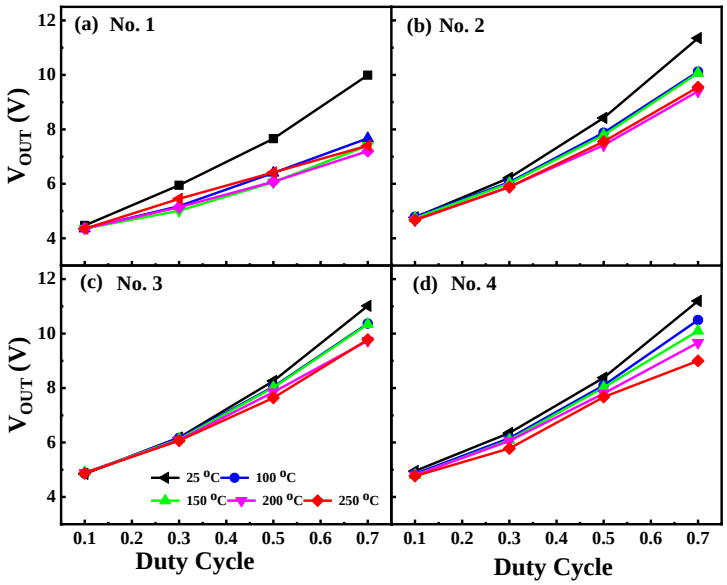


Fig.4.3.4 Temperature-dependent boost results with different gate drivers. (a) Driver No. 1, (b) driver No. 2, (c) driver No. 3, and (d) driver No. 4.

The high-temperature tests of converters were performed on a high-temperature probing stage over a wide temperature range from 25 °C, and 100 to 250 °C in 50 °C steps. Only the GaN chip with integrated gate drivers and power transistor was heated on the hot stage; the PCB board was off the probing stage and was externally connected to GaN power ICs using probes. The converter results at various temperatures are shown in Fig.4.3.4. All drivers show slight degradation at high temperatures even at 250 °C, indicating obvious advantages of GaN-based drivers for HT converters in applications under extreme environments, such as oil drilling, aviation, and hybrid electric vehicles. Among four different drivers, driver No. 1 shows obvious temperature degradation at 100 °C. Driver No. 4 (large buffer width) shows temperature dispersion at a high duty cycle (D= 0.7) due to current degradation caused by the large gate overshoot and oscillation.

The proposed driver No. 3 (small buffer width) shows the smallest temperature

dispersion, which might be attributed to high switching speed and small gate voltage overshoot/oscillation. In Fig. 4.2.7, driver No.3 shows the smallest rise/fall times and small voltage overshoots at various temperatures, this might be caused by better thermal stability of the buffer stage at elevated temperatures. In Fig. 3.2.8, the mobility of fully recessed E-mode devices changes slowly with temperatures, while it reduces obviously with temperatures in unrecessed D-mode devices. This indicates better thermal mobility of E-mode devices than D-mode devices at elevated temperatures. The buffer stage consists of two E-mode transistors, and the good thermal mobility of fully recessed E-mode devices in Fig. 3.2.8 might explain the smallest temperature dispersion in Fig. 4.2.7 (c) and Fig. 4.3.4 (c). However, driver No. 4 with a larger buffer stage shows larger temperature dispersion than No.3, which might be caused by the larger overshoot as previously discussed. This emphasizes the importance of the buffer stage with E-mode devices in achieving good thermal stability of gate drivers at high-temperature applications.

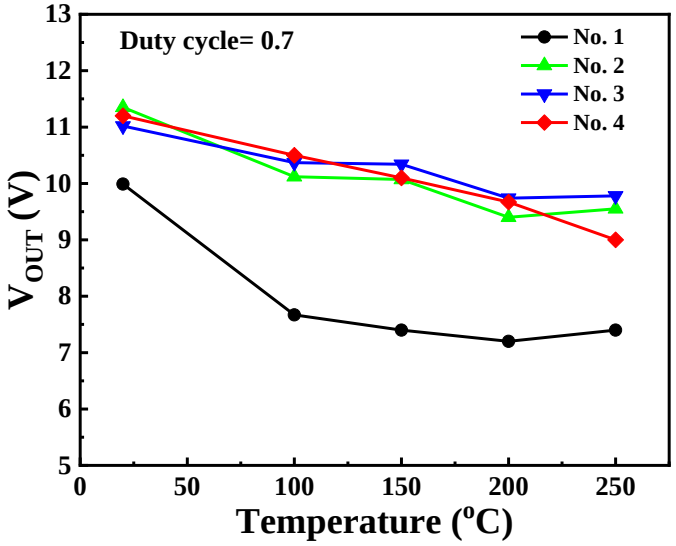


Fig.4.3.5 Temperature-dependent converter results for different drivers at duty cycle D=0.7.

Fig.4.3.5 shows temperature-dependent boost results for different drivers with a duty cycle of 0.7. It is apparent that driver No. 1 has the lowest output voltages through the whole temperature range due to the large rise times shown in Fig.4.2.8 (a). All other drivers show a slight reduction of V_{OUT} with increasing temperature, likely to be due to temperature degradation of rise/fall times or due to current degradation for both D-mode and E-mode devices caused by the degradation of channel mobility of transistors. Another factor is the negative threshold voltage shift at high temperatures, which can increase the output voltage [97]. The latter can explain the slight increase of output voltages at 250 °C in Fig. 3.3.5. Overall, driver No. 3 shows the comparably highest output voltages among the four drivers, especially at high temperatures above 150 °C. At 25 °C, driver No. 3 has an output voltage of 11 V, and only 11% of output voltage reduction has been observed at 250 °C, indicating good thermal stability for HT gate driver applications.

4.4 Converter characterization at high frequencies

Measurements at various frequencies were carried out to evaluate recessed E-mode MIS-HFETs for high-frequency applications. At room temperature, Fig.4.4.1 (a) and (b) show dynamic waveforms of four different gate drivers at 100 kHz and 1 MHz, respectively. Except for driver No. 1, all other three drivers show an acceptable performance at 1 MHz. It is apparent from the figure that driver No. 3 shows better

performance in terms of high switching speed and low oscillation as discussed previously.

At room temperature, the converter results with four gate drivers were compared in Fig.4.4.2, with frequencies of 100 kHz, 500 kHz, and 1 MHz. The parameters of the experiments are the same as those in Fig.4.3.1, and the only difference in Fig.4.4.2 is the measured frequency. In Fig.4.4.2, there is a clear trend of decreasing output voltages with increasing frequency. Take driver No. 3 for example, the output voltage is 7.1 V at 100 kHz, while this value decreases to 6.0 V at 500 kHz and 3.0 V at 1 MHz, which are much lower than the calculated voltage of 9.0 V. Results in Fig.4.4.2 indicate problems of the integrated converters at high frequencies, even though the drivers exhibit good driver performance at 1 MHz in Fig.4.4.1. It is essential to analyze the degradation mechanism of integrated converters using recessed MIS gate technology with increasing frequency, especially for high-frequency applications.

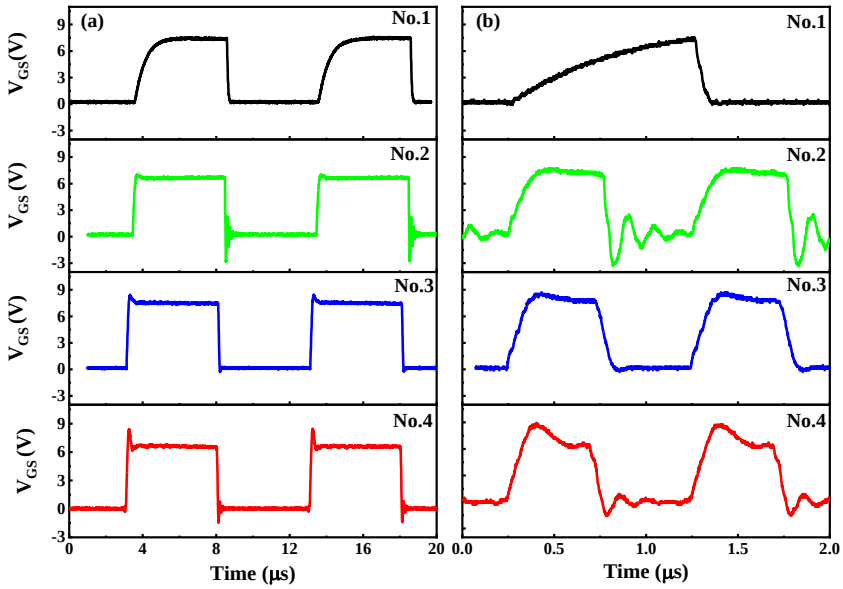


Fig.4.4.1 Dynamic waveforms of four different gate drivers at (a) 100 kHz, and (b) 1 MHz. $V_{G0,min}$=0 V, $V_{G0,max}$=7 V, V_{DD}=7 V.

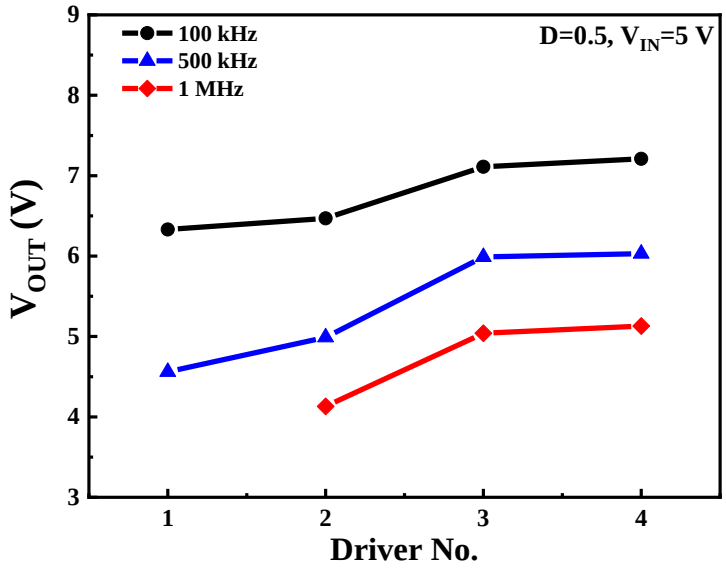


Fig.4.4.2 Converters results of four drivers at different frequencies of 100 kHz, 500 kHz, and 1 MHz. V_{IN}=5 V, duty cycle D=0.5, R=500 Ω.

The dynamic gate-to-source signals and drain-to-source signals of the GaN converter with the gate driver No. 3 were plotted in Fig.4.4.3. One of the differences among 100 kHz, 500 kHz, and 1 MHz, is the lower $V_{DS,\ max}$ at higher frequencies. To be specific, the $V_{DS,\ max}$ is 8 V at 100 kHz, but this value decreases to 7 V at 500 kHz and 6 V at 1 MHz, respectively. This can explain the reduced output voltage at high frequencies, since the $V_{DS,\ max}$ is equal to V_{OUT} when the transistor turns off. The lower V_{OUT} at higher frequencies in Fig.4.4.2 is caused by the reduced $V_{DS,\ max}$ in Fig.4.4.3. Moreover, there is a 0.4 μs V_{DS} delay at the turn-on transient moment, and this delay can be ignored at a low frequency of 100 kHz, but the delay can degrade the converter performance at a high frequency of 500 kHz and 1 MHz due to the changed duty cycles. The reduced duty cycle can lead to a reduction of the output voltage according to equation (4.1), and this can explain the frequency-dependent output voltages in Fig.4.4.2. The detailed analysis of the delay behavior will be discussed in the following part.

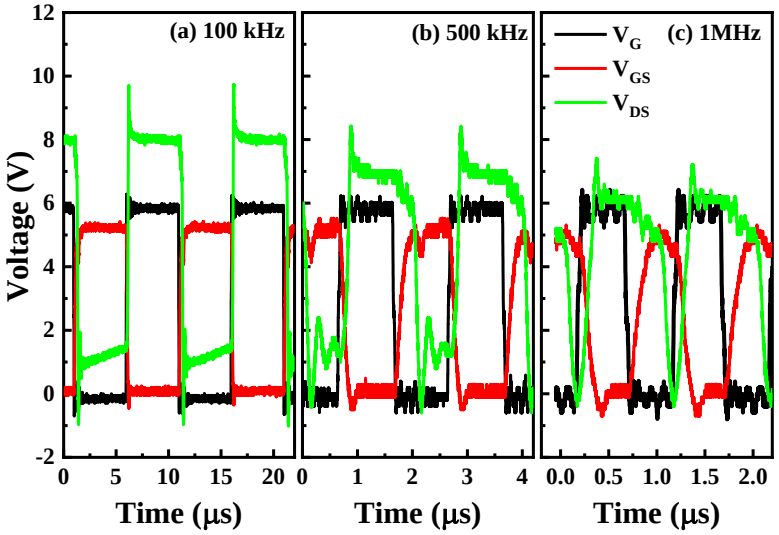


Fig.4.4.3 Dynamic waveforms of driver No. 3 at (a) 100 kHz, (b) 500 kHz, and (c) 1 MHz. D=0.5.

It looks like the delay is frequency independent, and it might be related to a large gate charge Q_G and R_{ON} of GaN MIS-HFETs, the recess-induced R_{ON} of this work is discussed in chapter 3. The dynamic waveforms of GaN converters with four different gate drivers are shown in Fig.4.4.4. Except for driver No.1, the other three drivers exhibit a similar delay of 0.4-0.6 μs. A large delay of 0.89 μs of driver No. 1 in Fig.4.4.4 (a) might be caused by the large rise time, which leads to an extra driver delay. Moreover, the delay depends on the load current, as shown in Fig.4.4.5. At 500 kHz, the delay increases from 0.41 μs at a load resistor of 500 Ω to 0.76 μs at 150 Ω. The increased V_{DS} delay might be caused by R_{ON} or current collapse at higher currents. Owing to the limited frequency of integrated GaN converters using recessed MIS-gate, all the integrated GaN converters are only measured at a frequency of 100 kHz in other chapters.

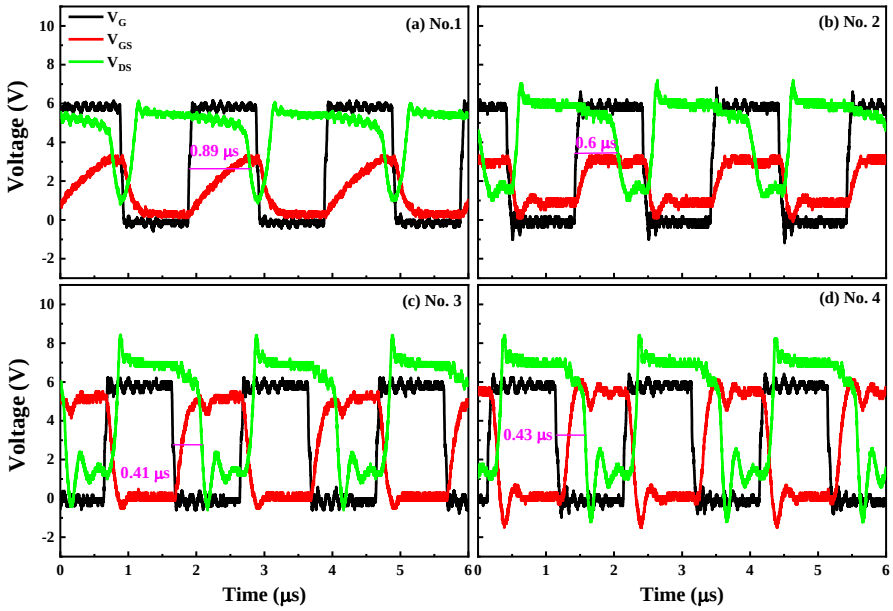


Fig.4.4.4 Dynamic waveforms of GaN converters with four different gate drivers at 500 kHz. (a) No.1, (b) No. 2, (c) No.3, and (d) No.4

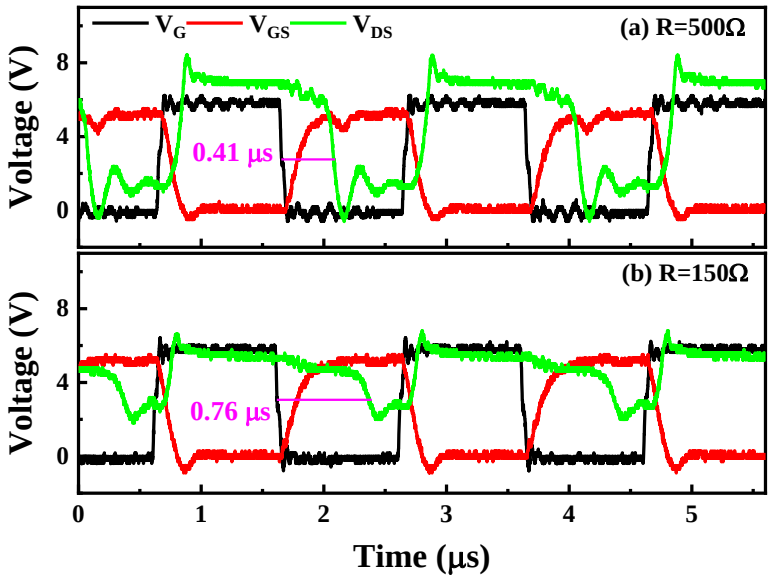


Fig.4.4.5 Dynamic waveforms of the GaN converter with driver No. 3. f= 500 kHz, D=0.5, V_{IN}= 5 V, (a) R=500 Ω, (b) R=150 Ω.

4.4 Conclusion

The GaN-based high-temperature gate driver presented in this chapter is a preliminary research effort to design integrated gate drivers for HT GaN-based DC-DC

converters. A 100 kHz, 5 V/11 V (V_{IN}/V_{OUT}) boost converter with the optimized driver has been proposed in this chapter. The driver can maintain high output voltages over a wide temperature range of up to 250 °C. Only 11% reduction of the output voltage at 250 °C has been observed compared to room temperature value, indicating a novel application of HT gate driver for GaN-based converters under extreme environmental conditions.

The drivers exhibit degraded performance at a high frequency up to 1 MHz, and the degraded output voltage is observed when increasing frequency. A 0.43 μs turn-on delay plays an important role and accounts for the degradation, which might be caused by the large R_{ON} of the recessed channel.

Chapter 5 Monolithic GaN half-bridge stages with integrated gate drivers for high-temperature DC-DC buck converters

5.1 Motivation

High-temperature (HT) power converters are becoming increasingly important in applications under extreme environments, such as electric vehicles, aviation, and oil drilling. For electric vehicles, the ambient temperature of the hood is usually above 150 °C, and the temperature near the engine can even reach 200 °C. Si-based devices can only work at a temperature below 150 °C, however, the superior material properties of wide bandgap (WBG) semiconductors (GaN and SiC) with good thermal conductivity are expected to be excellent candidates for power converters at high temperatures over 200 °C in electric vehicle applications.

Power integration becomes increasingly essential to fully utilize the superior performance of GaN material due to the reduced parasitic inductance, high power density, and HT operation. The lateral channel makes AlGaN/GaN heteroepitaxy structure an excellent candidate for power integrated circuits (ICs), compared with vertical GaN, depletion-mode (dMode) GaN, and SiC technologies [55]. A design towards monolithic integration for low and mid-power applications is proposed using Metal Insulator Semiconductor (MIS) or Metal Oxide Semiconductor (MOS) gate MIS-HEMTs (high-electron-mobility-transistors) [144]. A hybrid architecture using a recessed gate and an insulator was used by many studies [145-147] for enhancement

(E-mode) devices. The recessed E-mode MIS heterojunction-field-effect-transistors (MIS-HFETs) are excellent candidates for GaN-based power ICs, which can suppress gate leakage and provide strong immunity to large voltage overshoots or oscillations, especially in high-frequency power switching circuits. The insulated MIS-gate (V_{GS} over 10 V) could be driven with circuits designed for the mainstream Si and SiC power MOSFETs, without any additional drivers or level shifters.

Monolithic integration of GaN drivers and GaN power transistors is highly recommended for high-frequency operation and shows the advantage of reduced chip size [139]. Recent studies [46, 52, 53, 55] have been reported to monolithically integrate gate drivers with power transistors for GaN based DC-DC buck converters as summarized in Table 5. 1. Most of these studies focus on the low voltage DC-DC converters, especially for point-of-load (POL) devices. However, these integrated GaN converters are only measured at room temperature (RT), or negative drive voltages are needed [52, 53]. Limited reports show HT characteristics of integrated GaN converters, which are essential for electrical vehicle applications at high temperatures over 200 °C. The large gate swing voltage of 10 V in this work provides strong noise immunity and better compatibility with mainstream Si based circuits without any additional designs. In this work, the monolithic GaN synchronous buck converter with integrated gate drivers and a half-bridge stage is proposed and experimentally evaluated, which exhibits good stability at high temperatures up to 250 °C. The small circuit sizes of 3 mm^2 in this work and other converters in Table 5. 1 indicate the advantages of integrated drivers compared with external drivers. Besides, the low frequency in this work is

caused by current or mobility degradation of the recessed channel compared with other works. A fully recessed gate is recommended in this work in GaN ICs platform, and balance should be made between V_{th} of E-mode devices and current degradation using recessed E-mode GaN MIS-HFETs.

Table 5. 1 Recent studies of integrated GaN DC-DC buck converters

Design	[46]	[53]	[52]	[55]	This work
Year	2014	2016	2016	2017	2019
Technology	0.5 μm E-mode P-AlGaN HEMT	0.15 μm D-mode GaN-HEMT	E-mode GaN-on-SiC	E-mode GaN FETs	3 μm E-mode GaN MIS-HFET
Gate Driver	Integrated	Integrated	Integrated	Integrated	Integrated
Topology	Half-bridge	Half-bridge	Half-bridge	Half-bridge	Half-bridge
$^{a}V_{G,max}$	5 V	0 V	2.5 V	N.A.	10 V
$^{b}V_{G,min}$	0 V	-5 V	-2.5 V	N.A.	0 V
V_{IN}/V_{OUT}	12V/1.8V	20V/14V	25V/12 V	650V/N.A.	25V/4V
Temperature	RT	RT	RT	RT	250 °C
Frequency	3 MHz	100 MHz	20-400 MHz	2 MHz	100 kHz
Area	11.7 mm^2	5.52 mm^2	4 mm^2	48 mm^2	3 mm^2

N.A.=Not Applicable. $^{a}V_{G,max}$ and $^{b}V_{G,min}$ are maximum and minimum driving voltages of integrated drivers

In this chapter, the design, fabrication process, and characterization of the integrated gate drivers using E-mode AlGaN/GaN MIS-HFETs are proposed. The fabricated synchronous converter with integrated GaN drivers and one half-bridge power stage (V_{IN}=15 to 25 V at 100 kHz) shows less temperature degradation at 250 °C at various duty cycles and input voltages. Results in this work validate the advantages of E-mode AlGaN/GaN MIS-HFETs for monolithic integration ICs in achieving high temperature, high power density, and high-efficiency power converters.

5.2 Design of GaN half-bridge power stages with integrated gate drivers

The monolithic half-bridge stage shown in Fig.5.2.1 includes a high-side transistor (H_S) and a low-side transistor (L_S). At the first-half period, when the high-side transistor is at on-state (V_{GS_H} is at high voltage and V_{DS_H} is at low voltage) and the low-side transistor is at off-state (V_{GS_L} is at low voltage and V_{DS_L} is at high voltage), the output voltage (V_{OUT}) is obtained by deducting the voltage drop of the inductor L from an input voltage (V_{IN}). At the second-half period, when the high-side transistor is at off-state (V_{GS_H} is at low voltage and V_{DS_H} is at high voltage), while the low-side transistor is at on-state (V_{GS_L} is at high voltage and V_{DS_L} is at low voltage), the V_{OUT} is equal to the voltage drop of the inductor. The total area under the inductor voltage is zero whenever the converter operates in steady states, V_L refers to the voltage of the inductor and D is the duty cycle of the input of the high-side transistor, so equation (5.1) can be obtained:

$$\int_0^{T_s} v_L\,(t)\,dt = 0$$

$$(V_{IN} - V_{OUT}) \times \mathrm{D} + (-V_{OUT}) \times (1 - D) = 0$$

$$V_{OUT} = DV_{IN} \tag{5.1}$$

The synchronous DC-DC converter down-converts the input voltage through changing the duty cycles of the high-side transistor. Both the high-side driver and low-side driver need to provide the required gate to source voltages to switch on the corresponding power transistors. The low-side driver is easy to control since the source of the low-side transistor is grounded. However, since the source voltage of the high-side transistor is switching between zero and input voltage V_{IN}, the high-side driver should provide an

efficient level shift to ensure the required gate to source voltage of the high-side transistor. This section presents integrated gate drivers for DC-DC buck converters, the mechanism of the bootstrapped driver is introduced in section 5.2.1, the proposed synchronous buck converters with integrated gate drivers are illustrated in section 5.2.2, respectively.

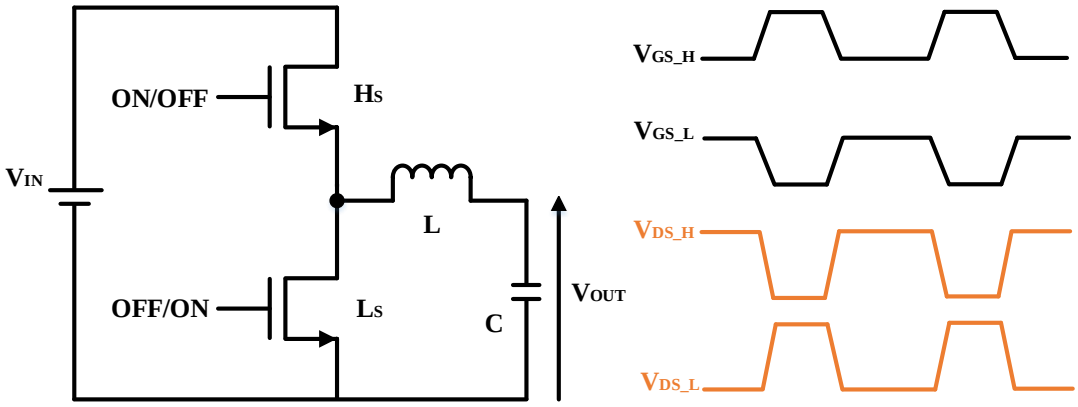


Fig.5.2.1 Circuit diagram and switch timing chart of synchronous DC-DC buck converters with a half-bridge stage [46]. V_{GS_H} and V_{DS_H} are the gate to source voltage and drain to source voltage of the high-side transistor H_S, respectively. V_{GS_L} and V_{DS_L} are the gate to source voltage and drain to source voltage of the low-side transistor L_S, respectively.

In order to achieve stable output voltage of GaN power converters in continuous conduction mode (CCM), L and C are calculated to obtain small voltage ripple buck converters. In a buck DC-DC converter, the ratio of the voltage ripple to the output voltage can be expressed as [140]:

$$\frac{\Delta V_c}{V_o} = \frac{1-D}{8LCf^2} \tag{5.2}$$

Where f is the switching frequency, D is the duty cycle, R is the load resistance. When D is equal to 0.5, f=100 kHz, choose L=1 mH, C= 20 μF, the capacitor voltage ripple using formula (5.2) is calculated as 0.03%.

5.2.1 Bootstrap driver

Fig.5.2.2 shows the circuit diagram of a bootstrap driver, and it operates as followings: when the high-side transistor H_S is at off-state, and the low-side transistor L_S is at on-state, the V_S is pulled down to the ground and the V_{DD} power supply charges the bootstrap capacitor C_{BT} through bootstrap diode D_{BT} (the charging path is shown as the red line). On the other hand, when the V_S is pulled up to a higher voltage by the switching-on process of the high-side transistor H_S (the low-side transistor L_S is at off-state), the increased V_S will reverse the bootstrap diode D_{BT} and block the rail voltage from V_{DD}, and the bootstrap capacitor discharges current through blue line, the floating V_{BS} supply maintains the required gate to source voltage to fully turn on the high-side transistor H_S.

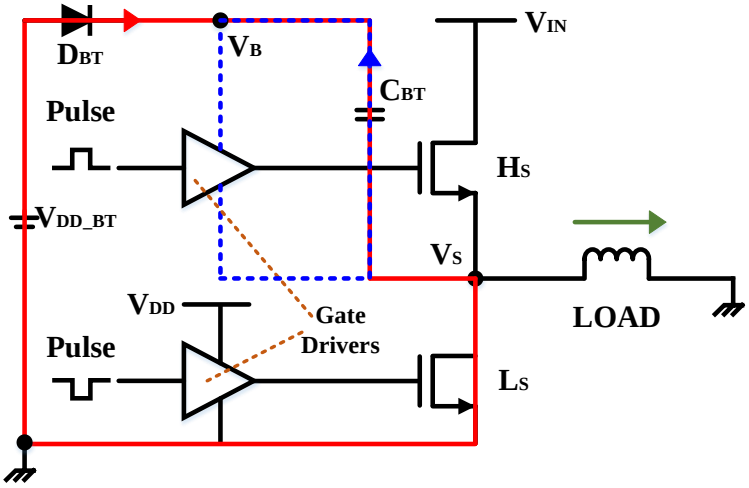


Fig.5.2.2 Circuit diagram of a bootstrap driver with a half-bridge stage (red line and blue line are the charging and discharging current paths of the bootstrap driver, respectively).

5.2.2 The proposed synchronous GaN DC-DC buck converter

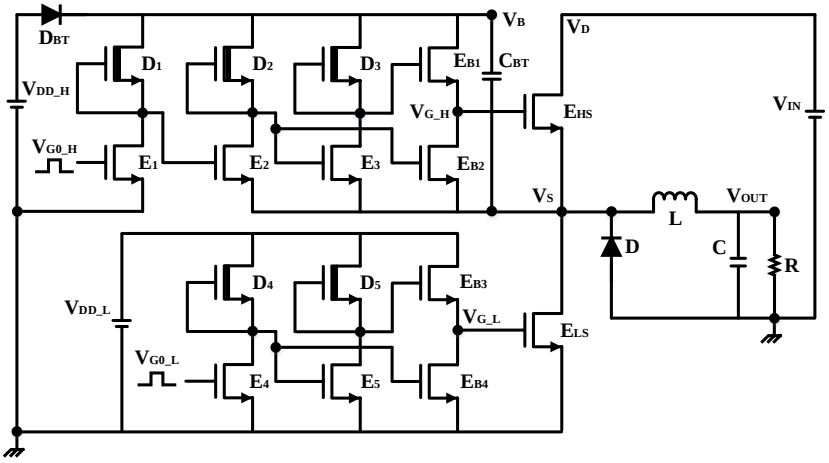


Fig.5.2.3 Circuit diagram of the proposed synchronous GaN DC-DC buck converter with integrated gate drivers. (Simulation parameters: L=1 mH, C=20 μF, R=500 Ω)

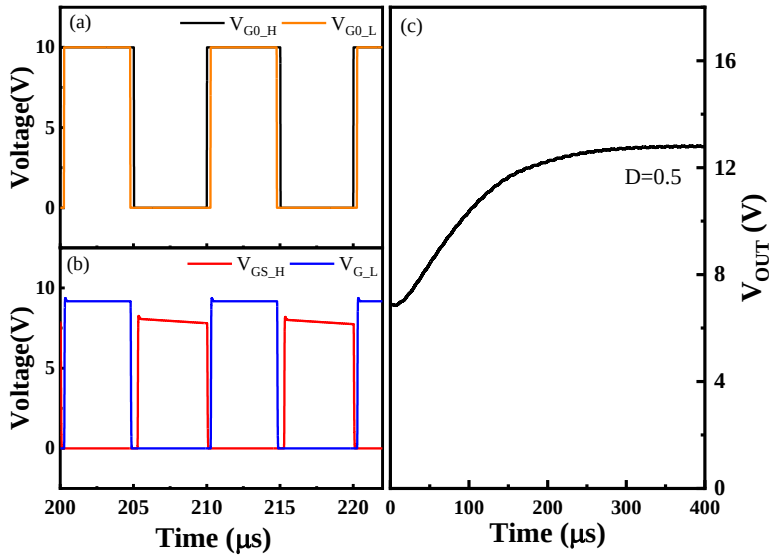


Fig.5.2.4 Simulated waveforms of the proposed synchronous GaN DC-DC buck converter. (a) Input signals of the high/low-side drivers (V_{G0_H}/V_{G0_L}). (b) Output signals of the high/low-side drivers (V_{GS_H}/V_{G_L}, V_{GS_H} is the voltage between V_{G_H} and switching node V_S). D=0.5, f=100 kHz, V_{IN}=25 V, R=500 Ω.

Fig.5.2.3 shows the circuit diagram of the proposed synchronous DC-DC buck converter, which integrates a high-side driver, a low-side driver, and two power transistors E_{HS} and E_{LS}. The device parameters of the simulation are the same with experimental sizes in Table 5. 3. Fig.5.2.4 shows the simulated waveforms, the

synchronous buck converter has a deadtime of 0.25 μs between V_{GS_H} and V_{G_L} to avoid simultaneous conduction of two power transistors E_{HS} and E_{LS}, and 0.25 μs is chosen to prevent the short circuit or shoot-through failure. The output signals of gate drivers are shown in Fig.5.2.4 (b), and the output voltage of the converter is shown in Fig.5.2.4 (c) with a duty cycle of 0.5, in which a startup time of 200 μs is required before stabilization. The simulated output voltages versus duty cycles are shown in Fig.5.2.5, and the theoretical calculation (blue line) using equation (5.1) matches with simulation results.

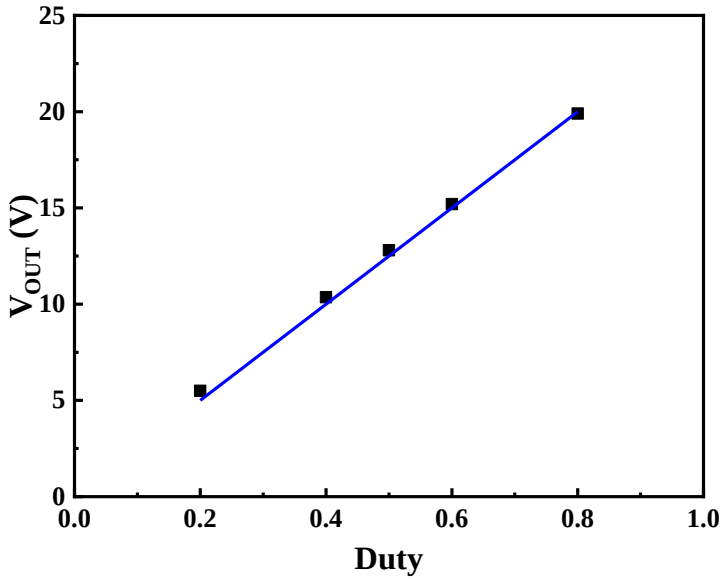


Fig.5.2.5 Simulated output voltages of the proposed converter in Fig.5.2.3 at various duty cycles. (Blue line is the theoretical calculation)

5.3 Circuit design and characterization

In this section, the proposed synchronous converter is compared with an integrated asynchronous DC-DC converter with a single driver at various load conditions and temperatures. The experiment and characterization of two converters are introduced first, and then high-temperature measurements were carried out. The detailed fabrication

process is the same process flow as the GaN DCFL inverter in Fig. 2.2.3. The E-mode devices were achieved through a recessed MIS-gate technique with a full etch depth of 25 nm.

5.3.1 An asynchronous DC-DC buck converter with an integrated gate driver

Fig.5.3.1 (a) shows the circuit diagram of a GaN-based asynchronous DC-DC buck converter with an integrated gate driver. The gate driver and the power transistor E_0 were integrated on one chip. The experimental setup is shown in Fig.5.3.1 (b), the inductor L, diode D, capacitor C, and the load resistor R were integrated on a PCB board, the integrated gate driver and power transistor E_0 were externally connected with the bootstrap diode D_{BT}, bootstrap capacitor C_{BT} and components of PCB board using probes. The high-temperature (HT) tests were also carried out to study the thermal properties of the proposed converters. During the HT tests, the GaN chip with integrated gate drivers and power transistor E_0 were heated on the hot stage, whereas C_{BT}, D_{BT}, and the PCB board were off the probing stage. The parameters of the integrated asynchronous buck converter are shown in Table 5. 2, which are based on our previous work [59]. The integrated driver consists of direct-coupled FET logic (DCFL) inverters and a buffer stage. To be specific, one DCFL inverter contains a D-mode device with gate and source connected, and an E-mode device as well. The buffer stage consists of two E-mode devices E_{B1} and E_{B2} for high-speed switching transition.

Table 5. 2 Device parameters for the asynchronous buck converter

Components	Devices	Width (μm)
DCFL inverters	D_1, D_2, D_3	5
	E_1, E_2, E_3	200
Buffer stage	E_{B1}, E_{B2}	500
Power transistor	E_0	1000

The gate length L_G is 3 μm for all devices.

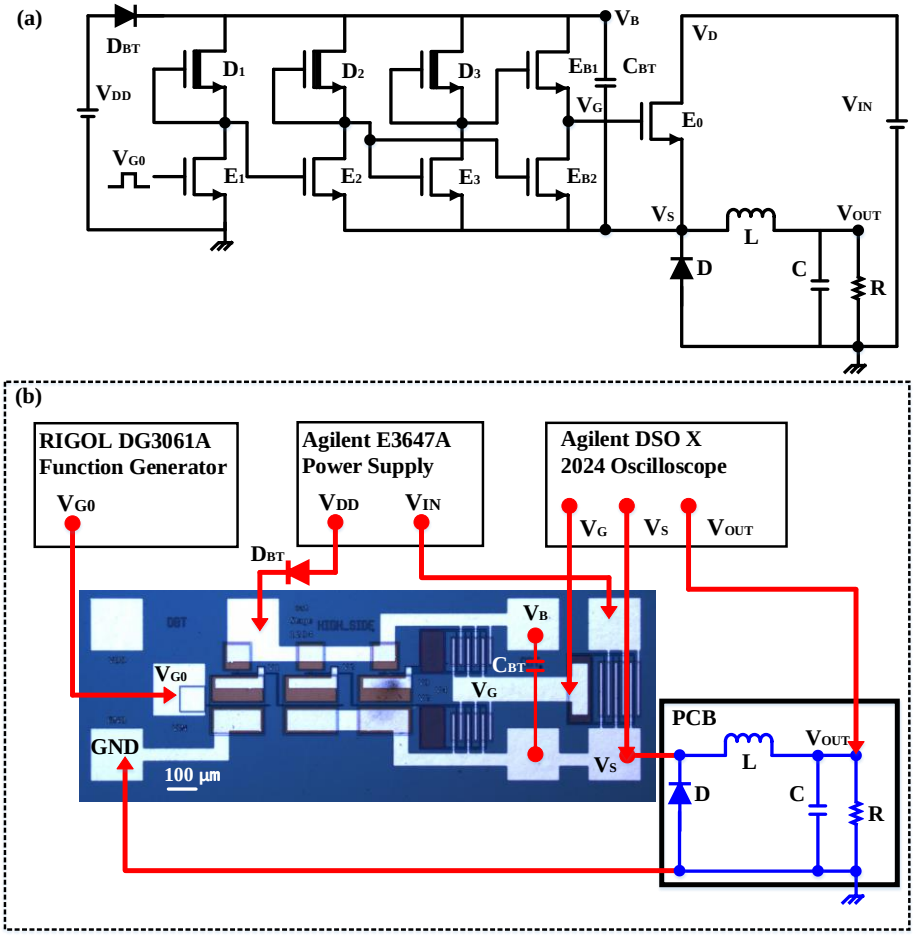


Fig.5.3.1 (a) The circuit diagram of the GaN-based asynchronous DC-DC buck converter with an integrated gate driver. (b) The experimental setup and microphotograph of the integrated circuits. (The parameters of discrete components are: L=1 mH, C=20 μF, R=500 Ω, V_{DD}=10 V, V_{IN}=20 V, f=100 kHz, D=0.5, the threshold voltage of V_F of the discrete diode D and D_{BT} is +0.7 V, C_{BT}=22 nF).

Fig.5.3.2 shows the dynamic waveforms of the integrated buck converter in Fig.5.3.1.

The pull-up voltage V_{DD} is 10 V and the input voltage of the converter V_{IN} is 20 V. When

the input of the gate driver V_{G0} is at a high voltage of 10 V, the output of the driver V_G is at a low voltage around 0 V and the power transistor E_0 is at off-state. Hence, the floating source V_S is pulled down to the ground through the discrete diode D. On the other hand, when the input voltage of the driver V_{G0} is 0 V, the high output voltage of V_G will turn on the power transistor E_0, and therefore V_S is pulled up to V_{IN}=20 V. The bootstrap driver will reverse the bootstrap diode D_{BT} and the floating V_{BS} supply pull up the V_G to a higher voltage, which provides the required gate to source voltage V_{GS} in order to maintain the power transistor E_0 at on-state, as discussed in the previous session. The dynamic waveforms V_{G0}, V_G, V_S, and calculated V_{GS} are shown in Fig.5.3.2 (a) at room temperature and Fig.5.3.2 (b) at 250 °C, respectively. At 100 kHz, the output voltage waveforms of the driver V_{GS} can function well with small voltage overshoots and oscillations even at high temperature 250 °C, owing to full integration of the gate driver and power transistor, this indicates the advantages of using GaN MIS-HFETs technology in GaN ICs platform. Additionally, the maximum voltage of V_{GS} (around 9 V) is slightly lower than V_{DD}=10 V, which is caused by the voltage drop of the diode (V_F=+ 0.7 V) during the charging process of the bootstrap driver, since the open-loop test shows a maximum voltage of 10 V with V_S grounded. Besides, it is found that the etch depth of the barrier layer is essential, when we use the recessed gate with insulators to achieve GaN ICs for power converters, especially for gate drivers with multi-stages. What's more, the full recess of the barrier is recommended, because the output of the drivers with partial recess can easily work at the first stage but might degrade or even not work at the following stages.

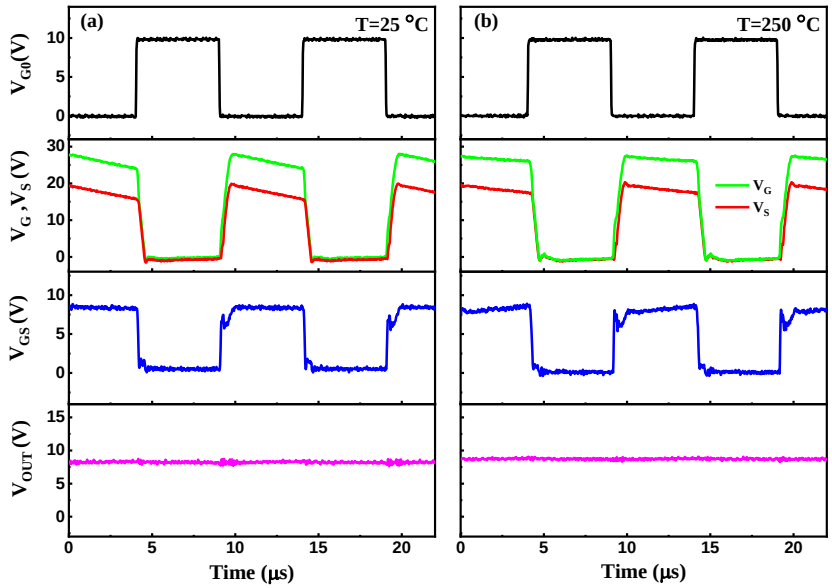


Fig.5.3.2 Dynamic waveforms of the GaN-based asynchronous DC-DC converter in Fig.5.3.1 at room temperature 25 °C (a) and 250 °C (b), respectively, when the duty cycle is 0.5. V_{G0} and V_G are the input and output gate signals of the driver, respectively. V_S is the source of the power transistor E_0, and the V_{GS} voltage between V_G and V_S is equal to the gate to source voltage of the power transistor E_0.

5.3.2 The proposed synchronous DC-DC buck converter with integrated drivers

Table 5. 3 Device parameters for the proposed synchronous GaN buck converter

Components	Devices	Width (μm)
DCFL inverters(HS)	D_1, D_2, D_3	5
	E_1, E_2, E_3	200
Buffer stage(HS)	E_{B1}, E_{B2}	500
DCFL inverters(LS)	D_4, D_5	5
	E_4, E_5	200
Buffer stage(LS)	E_{B3}, E_{B4}	500
Power transistor	E_{HS}, E_{LS}	1000

The gate length L_G is 3 μm for all devices.

The synchronous buck converter with a half-bridge power stage is an important topology in power converter configurations. The detailed parameters of the proposed half-bridge power stage with integrated gate drivers are listed in Table 5. 3.

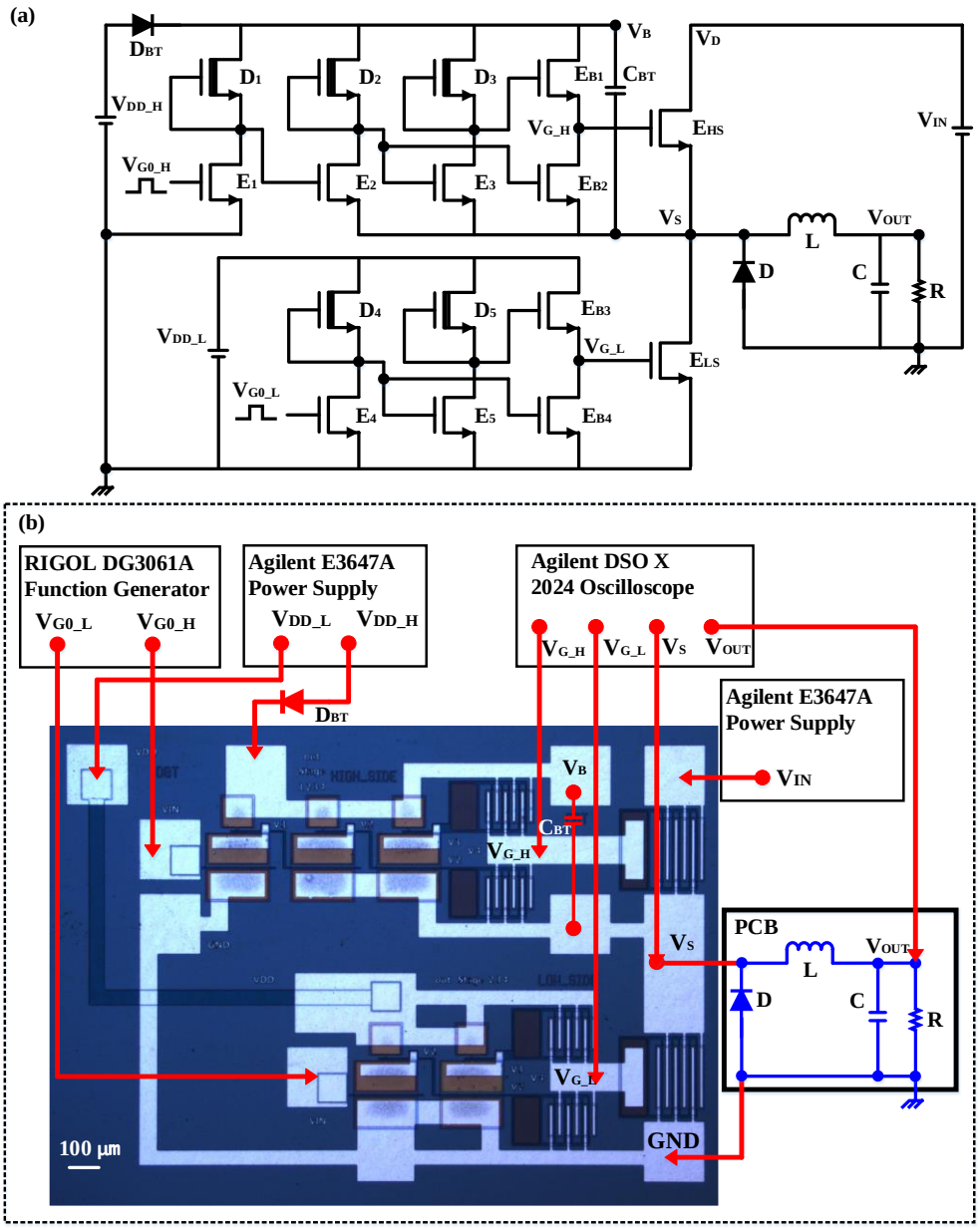


Fig.5.3.3 (a). The circuit diagram of GaN-based synchronous DC-DC buck converter with integrated gate drivers. (b) The experimental setup and microphotograph of the proposed circuit. (The parameters of discrete components are: L=1 mH, C=20 µF, R=500 Ω. V_{DD}=10 V, V_{IN}=20 V, f=100 kHz, duty cycle=0.5, the threshold voltage V_F of the discrete diode D and D_{BT} is +0.7 V, C_{BT}= 22 nF).

The circuit diagram of the proposed synchronous buck converter is shown in Fig.5.3.3 (a), and Fig.5.3.3 (b) shows the experimental setup and a microphotograph of the synchronous buck converter. The photographs of the measurement hardware of the GaN converter are shown in Fig.5.3.4. In order to compare different topologies (asynchronous

and synchronous) of buck converters, we use the same external load side as Fig.5.3.1 in this work, including a discrete diode D, an inductance L, a load capacitor C, and a resistor R in the PCB board. The synchronous buck converter integrates a high-side driver, a low-side driver, a high-side power transistor E_{HS}, and a low-side power transistor E_{LS}. Normally, the inputs of high-side driver V_{G0_H} and low-side driver V_{G0_L} are reversely oriented and have a dead time between them in order to avoid short circuit or shoot-through failure [59, 148]. In this work, the input signals of both high-side and low-side drivers are in the same direction for simplicity due to the different numbers of DCFL inverters (the stage number is odd in the high-side driver and even in the low-side driver). That means the output voltage of the high-side driver V_{G_H} is reverse with the input voltage of the high-side driver V_{G0_H}, whereas the output voltage of the low-side driver V_{G_L} changes in the same direction with the input voltage V_{G0_L}. Meanwhile, the synchronous buck converter has a deadtime of 0.25 μs between V_{G0_H} and V_{G0_L} to avoid simultaneous conduction of two power transistors E_{HS} and E_{LS}, and 0.25 μs is chosen to prevent short circuit or shoot-through failure because the proposed driver in Fig.5.3.1 shows propagation delay times of less than 0.22 μs at various temperatures, similar with rise times and fall times of less than 0.25 μs at various temperatures in chapter 4 [59].

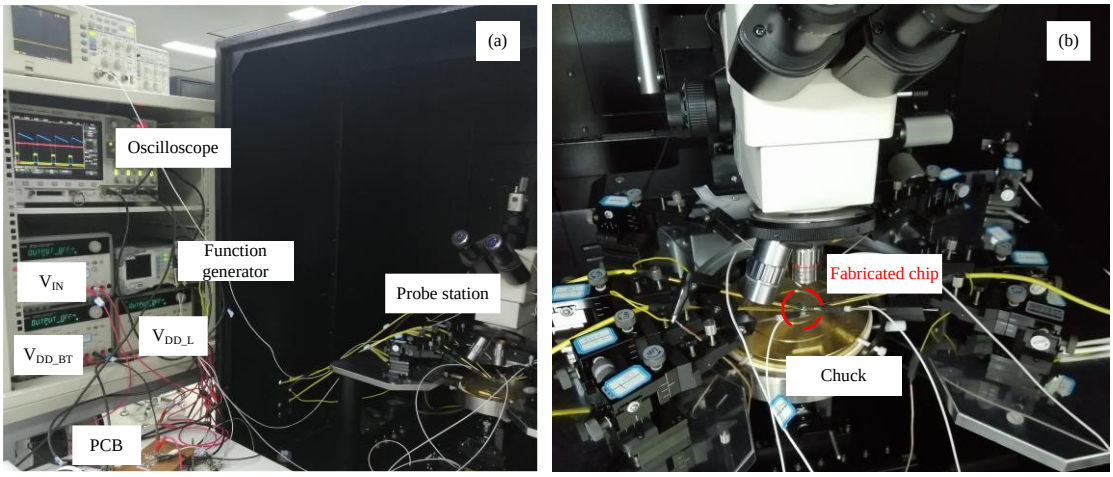


Fig.5.3.4 Photographs of the measurement hardware including probe station, oscilloscope, voltage sources, and PCB.

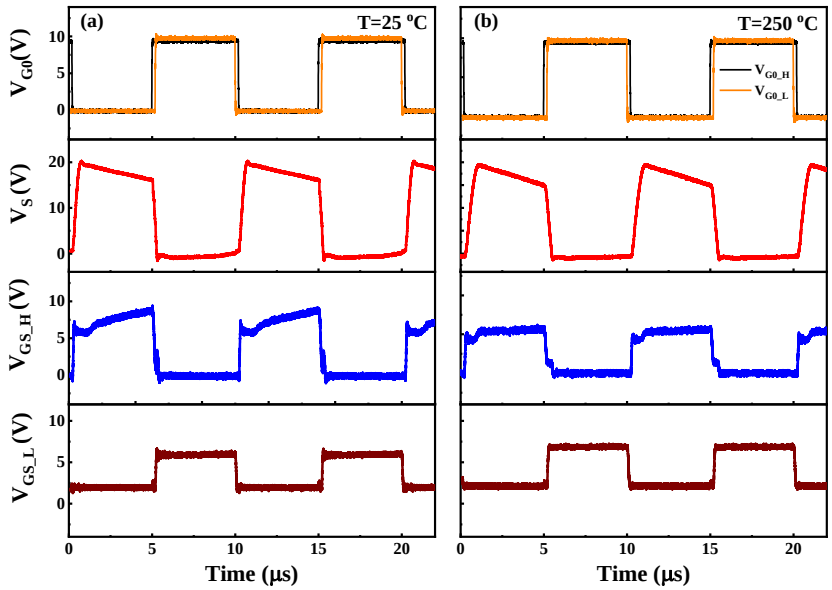


Fig.5.3.5 Dynamic waveforms of the GaN-based synchronous DC-DC converter in Fig.5.3.3 at room temperature 25 °C (a) and 250 °C (b), respectively. V_{G0_H} and V_{G_H} are the input and output voltages of the high-side driver, respectively. V_{G0_L} and V_{G_L} are the input and output voltages of the low-side driver, respectively. V_{GS_H} (voltage between V_{G_H} and V_S) is equal to the gate to source voltage of high-side transistor E_{HS}, whereas V_{G_L} is the gate to source voltage of the low-side transistor E_{LS}.

Fig.5.3.5 (a) and (b) show dynamic waveforms of the GaN-based synchronous buck converter at 25 °C and 250 °C, respectively. The input signal V_{G0_H} has a 0.25 μs extension over V_{G0_L} during switching-on and switching-off transition, this ensures a 0.25

μs deadtime control between the high-side transistor E_{HS} and low-side transistor E_{LS}. As a similar discussion, when the input signals of high-side driver V_{G0_H} and low-side driver V_{G0_L} are both at a high voltage of 10 V, the corresponding V_{G_H} and V_{G_L} are at low voltage and high voltage, respectively. Hence, the high-side transistor E_{HS} is at off-state and the low-side transistor E_{LS} is at on-state, V_S is pulled down to the ground through the low-side transistor E_{LS}. On the other hand, when V_{G0_H} and V_{G0_L} are both equal to 0 V, this leads to a high voltage of 10 V at V_{G_H} and a low voltage at V_{G_L}, respectively. Therefore, the high-side transistor E_{HS} is switched on and the low-side transistor E_{LS} is switched off, and the floating V_S is consequently pulled up to V_{IN}, enabling the bootstrap driver to maintain the specific gate to source voltage of the high-side transistor E_{HS} as the previous discussion. The proposed half-bridge transistors with integrated high-side and low-side drivers work well at 25 °C and 250 °C with small voltage overshoots and oscillations in Fig.5.3.5 (a) and Fig.5.3.5 (b), respectively. Besides, the V_{GS_H} of the high-side driver is a little bit lower than V_{GS} in Fig.5.3.2 due to the additional low-side loop. This is because the maximum voltage of V_{GS} or V_{GS_H} is determined by voltage bias supply V_{BS} of the bootstrap driver. The V_{BS} (during the charging process of the bootstrap) in Fig.5.3.2 is equal to V_{DD}-V_F, V_F is the threshold voltage of the diode D_{BT}, whereas V_{BS} of the synchronous converter in Fig.5.3.5 is equal to V_{DD_H}-V_F-$V_{DS,\ ON\_LS}$ due to the existence of the low-side transistor E_{LS} during the charging process of the bootstrap driver, where $V_{DS,\ ON\_LS}$ is the on-state drain to source voltage of the low-side transistor E_{LS}. This possibly explains the lower V_{GS_H} in Fig.5.3.5, and a lower V_{GS_L} can also be explained by the existence of the high-side loop as a similar discussion. Nevertheless, this does not

affect the switching performance of the power transistors and hence converter performance in the following section 5.3.3.

5.3.3 Converter results and discussions at high temperatures

Fig.5.3.6 shows results of the asynchronous converter in Fig.5.3.1 over a wide temperature range from 25 ℃ to 250 ℃, and the calculated values using equation (5.1) were also plotted for comparison. Here, the duty cycles of output waveforms of the bootstrap driver V_G are used for simplicity. The output voltages of the asynchronous buck converter increase with increasing duty cycles, and the overall performance is close to theoretical lines. Moreover, there is only small degradation of output voltages at high temperatures up to 250 ℃, this indicates the good performance of GaN ICs for high-temperature power converters under extreme environments. Also, there is some dispersion of output voltages at a low duty cycle of 0.2, which might be caused by the asynchronous topology and will be discussed later.

The discrepancies between experimental and calculated values in Fig.5.3.6 are observed and increase with input voltages and duty cycles. At room temperature with V_{IN}=15 V, the discrepancy at a duty cycle of 0.8 is 2 V, this value increases up to 3 V, 4 V at V_{IN}=20 V, 25 V, respectively. The possible cause is due to increased dynamic R_{ON} with increasing V_{IN} and duty cycles, and the increased dynamic R_{ON} or current collapse is mainly caused by defect traps [149-151].

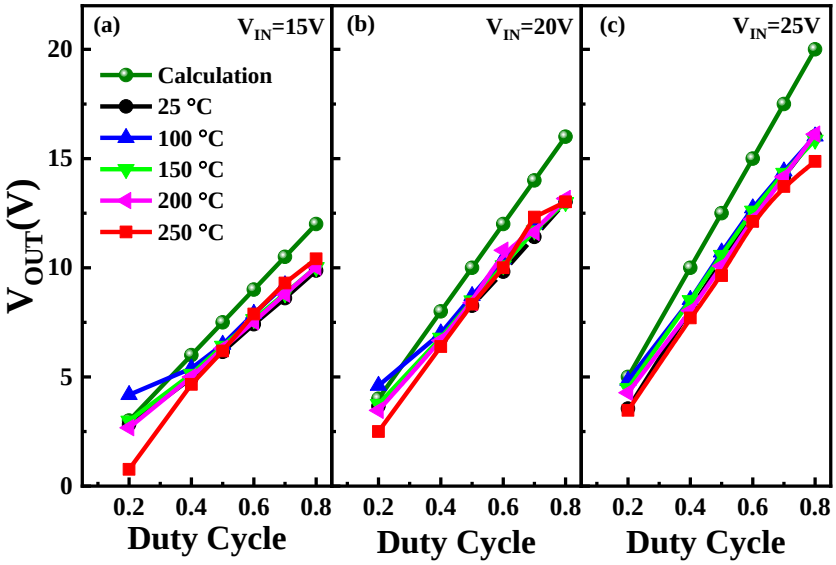


Fig.5.3.6 Experimental results of the asynchronous converter in Fig.5.3.1 at various duty cycles and temperatures, f=100 kHz. (a)V_{IN}=15 V, (b)V_{IN}=20 V and (c)V_{IN}=25 V.

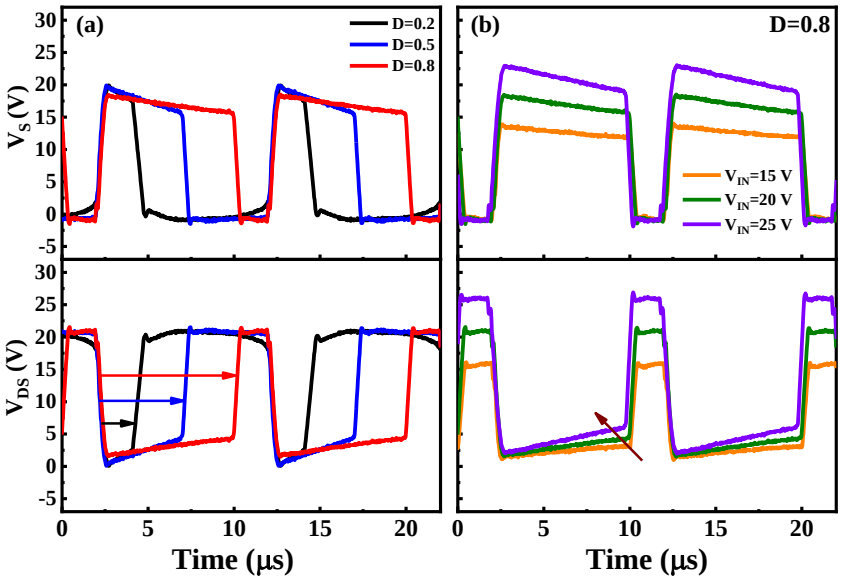


Fig.5.3.7 (a) Dynamic V_S and V_{DS} at different duty cycles 0.2, 0.5, and 0.8 at V_{IN}=20 V. (b) Dynamic V_S and V_{DS} at different input voltages of 15 V, 20 V, and 25 V with a duty cycle of 0.8. Temperature=25 °C, f=100 kHz.

As shown in Fig.5.3.7 (a), V_{IN}=20 V with different duty cycles of 0.2, 0.5, and 0.8, V_{DS} refers to the drain to source voltage of the power transistor E_0 and is normally as low as zero at on-state in an ideal case. However, the increased R_{ON} will change equation (5.1) to equation (5.3) when considering an on-state voltage $V_{DS,ON}$ in a real

condition. Compared with equation (5.1), the output voltage in equation (5.3) decreases at higher duty cycles due to increased R_{ON} or $V_{DS,ON}$, this can explain the decreased output voltages at high duty cycles in Fig.5.3.6. On the other hand, the input voltage can also affect dynamic R_{ON} as shown in Fig.5.3.7 (b), with a duty cycle of 0.8. The on-state voltage $V_{DS,ON}$ or dynamic R_{ON} increases slightly when the input voltage varies from 15 V to 25 V. This might be caused by current collapse of the off-state drain voltage stress, which may promote the trapping of electrons under the gate and in the gate-drain access region [84]. To be specific, when the power transistor is at off-state with a positive drain voltage V_{IN} (V_{DS}=V_{IN}), electrons can be injected from the gate electrode and trapped at the interface in the access region. Once the power transistor switches on, the trapped electrons cannot be emitted fast enough and partially deplete the 2DEG channel, leading to a reduced current or an increased R_{ON}. A higher V_{IN} of 25 V leads to more electron traps at off-state and a larger R_{ON} compared with a lower V_{IN} of 15 V in Fig.5.3.7 (b). This possibly explains the increased discrepancies between calculation and experiment results at higher input voltages in Fig.5.3.6.

$$(V_{IN}-V_{OUT}-V_{DS,ON})\times \mathrm{D}+(-V_{OUT})\times(1-D)=0, V_{OUT}=D(V_{IN}-V_{DS,ON}) \qquad (5.3)$$

Fig.5.3.8 shows the synchronous converter results in Fig.5.3.3 over a wide temperature range from 25 °C to 250 °C, and here we use the duty cycle of the output waveform V_{GS_H} of the high side driver. The output voltages of the synchronous buck converter show similar trends with the asynchronous converter. However, the proposed synchronous buck converter with an integrated half-bridge power stage shows more stable and uniform performance under various temperatures from 25 °C to 250 °C. Meanwhile, it shows less

temperature dispersion not only at different duty cycles, but also at different input voltages compared with the results of the asynchronous converter in Fig.5.3.6. The stable performance at high temperatures outstands the excellent candidate of the synchronous converter with a half-bridge stage in power converter applications under extreme environments.

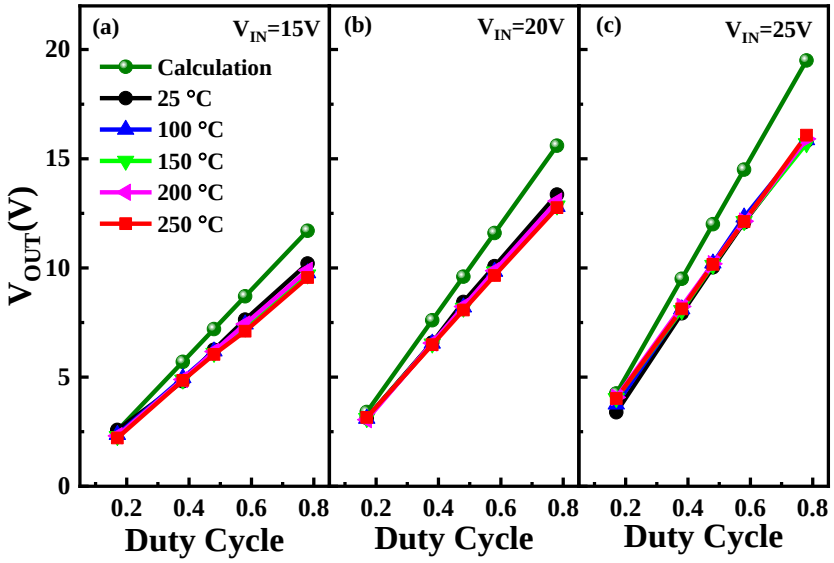


Fig.5.3.8 Experimental results of the synchronous converter in Fig.5.3.3 at various duty cycles and temperatures at f=100 kHz. (a) V_{IN}=15 V, (b) V_{IN}=20 V and (c) V_{IN}=25 V.

The reason why the integrated synchronous converter shows better high-temperature performance than the integrated asynchronous converter can be explained as follows. To analyze the difference between two topologies, here we take a duty cycle of 0.2 as an example. Fig.5.3.9 (a) and (b) present the dynamic V_S and V_{DS} of the asynchronous converter and synchronous converter at various temperatures, respectively. It can be observed that the synchronous converter shows more uniform V_S and V_{DS} waveforms at various temperatures, especially during the switching-on transition of the high-side

transistor. The low-side transistor E_{LS} of the synchronous converter in Fig.5.3.3, conducts load current instead of the discrete diode D of the asynchronous converter in Fig.5.3.1, here we do not consider the small conduction loss of the discrete diode D during deadtimes. When the high-side transistor E_{HS} is at off-state, the large current of the low-side transistor E_{LS} will speed up the discharging process of the converter. On the other hand, the large discharging current of low-side transistor E_{LS} will accelerate to pull up the floating V_S to V_{IN} and speed up the switching-on transition of the high-side transistor E_{HS}. This can explain the good stability of the synchronous converter at various duty cycles and temperatures in Fig.5.3.8.

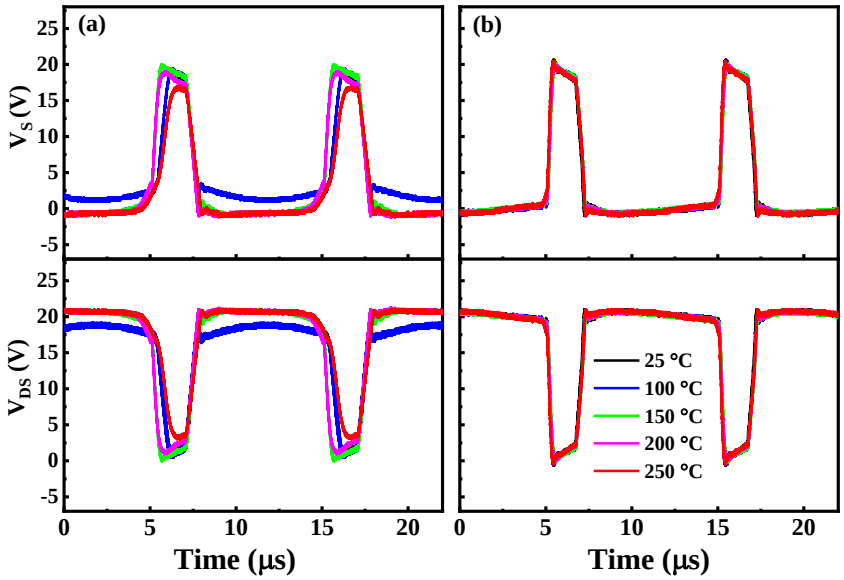


Fig.5.3.9 Dynamic V_S and V_{DS} of (a) asynchronous converter in Fig.5.3.1 and (b) synchronous converter in Fig.5.3.3 at various temperatures (V_{DS} is the drain to source voltage of the high-side transistor E_{HS}). Duty cycle D=0.2, V_{IN}=20 V, f=100 kHz.

5.4 Converter comparison with external gate drivers

The excellent performance of the synchronous buck converter with integrated gate drivers and a half-bridge stage emphasizes the importance of the full integration design

on a single chip, especially for HT operations in electric vehicle applications. To fully understand the advantages of GaN ICs, both asynchronous and synchronous DC-DC buck converters using external drivers were experimentally compared but with discrete GaN-based E-mode MIS-HFETs, which were fabricated on the same chip with the integrated circuits in Fig.5.3.1 and Fig.5.3.3. The external drivers used in this work are Texas Instruments LM5113 as shown in Fig.5.4.1. The size of the integrated driver in Fig.5.3.3 is 2.7 mm^2, which is almost 6 times smaller than 16 mm^2 of the external driver LM5113. The output voltages of logic high V_{OH} and logic low V_{OL} of the LM5113 driver are 5 V and 0 V, respectively.

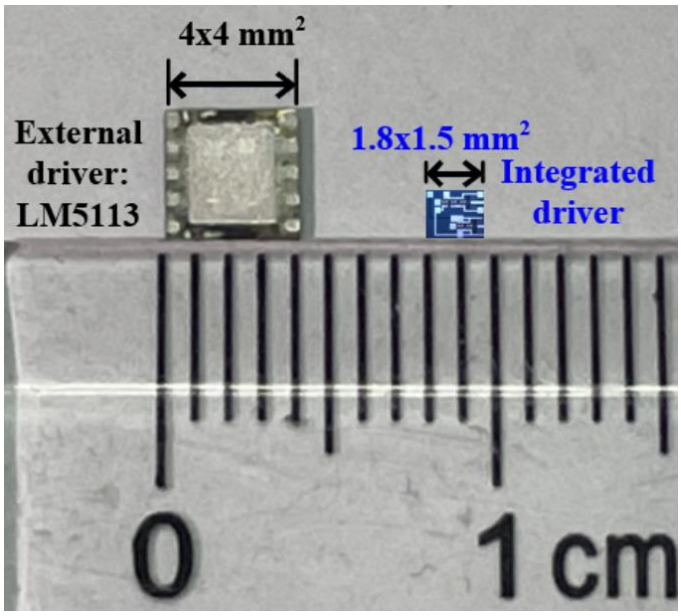


Fig.5.4.1 Photograph of external driver LM5113 (4x4 mm^2). The area of the integrated GaN driver is 1.8x1.5 mm^2.

At room temperature, Fig.5.4.2 compares four different designs of the buck converters, including asynchronous and synchronous converters with external drivers, asynchronous (Fig.5.3.1), and synchronous (Fig.5.3.3) converters with integrated drivers, respectively. The two converters with external drivers were externally

connected with E-mode power transistors, which were fabricated on the same chip with GaN ICs in Fig.5.3.1 and Fig.5.3.3, and they have the same gate width of 1000 μm with power transistors $E_0/E_{HS}/E_{LS}$. In addition, the same PCB board in Fig.5.3.1 and Fig.5.3.3 was used in converters with external drivers to study the impact of different drivers on the performance of the converters. In Fig.5.4.2 (a) and (b), the synchronous converter with integrated drivers shows slightly higher output voltages, owing to high-speed transition and low R_{ON} as the previous discussion. At V_{IN}=25 V in Fig.5.4.2 (c), converters with integrated drivers exhibit higher output voltages than converters with external drivers, and the discrepancies increase with increasing duty cycles. Besides, both asynchronous and synchronous converters with integrated drivers show similar output voltages at 25 V, which is attributed to the role of increased dynamic R_{ON} caused by high input voltages.

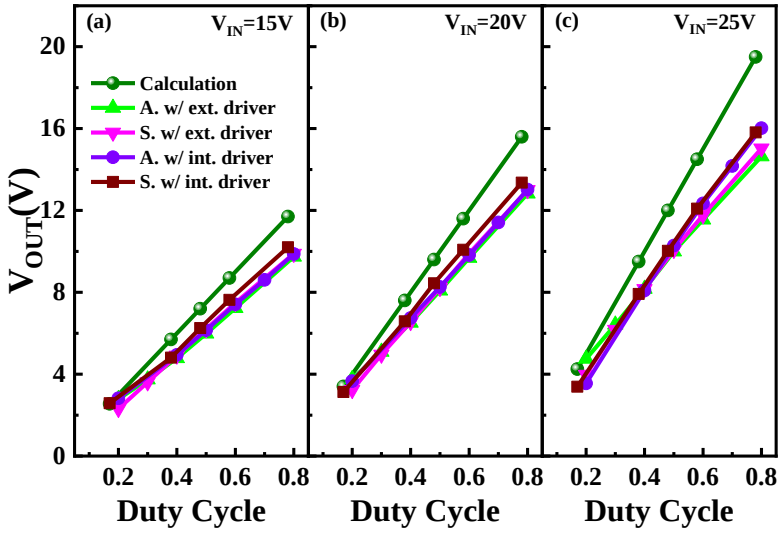


Fig.5.4.2 Converters comparison between integrated drivers and external drivers. (a) V_{IN}=15 V, (b) V_{IN}=20 V and (c) V_{IN}=25 V. Four different designs of converters, including asynchronous converter with external driver (A. w/ ext. driver), synchronous converter with external driver (S. w/ ext. driver), asynchronous converter with integrated driver (A. w/ int. driver in Fig.5.3.1), and synchronous converter with integrated drivers (S. w/ int. driver in Fig.5.3.3).

Even though there are no obvious output voltage differences at low duty cycles among converters with external drivers and integrated drivers in Fig.5.4.2, the dynamic waveforms vary a lot from each other. At room temperature, Fig.5.4.3 shows dynamic V_{GS} and V_{DS} waveforms of the high-side transistor in four different converters with a duty cycle of 0.2 at V_{IN}=25 V. Converters with integrated drivers in Fig.5.4.3 (c) and (d) show small gate overshoots and oscillations, while converters with external drivers in Fig.5.4.3 (a) and (b) exhibit obvious gate voltage V_{GS} overshoots up to 10 V or undershoots around negative -5 V, and obvious voltage oscillations as well. The large gate overshoots or undershoots can seriously damage or break down switching transistors, especially for low gate voltage swing transistors [17], such as HEMTs or P-GaN HEMTs, which usually show $V_{G,max}$ less than 7 V [84]. The voltage overshoots and oscillations in external drivers are caused by the increased parasitic inductance through external connections. Besides, there are serious V_{DS} overshoots due to the overshoots of V_{GS} signal in converters with external drivers, which will impact the accuracy of the output voltages to some extent. What's more, there is obvious waveform distortion of V_{DS} for the asynchronous converter with the external driver in Fig.5.4.3 (a) before the high-side transistor switches on. This might be caused by low charging and discharging currents at a low duty cycle of 0.2, the synchronous converter with external drivers can solve the problem owing to the low-side loop of the synchronous topology in Fig.5.4.3 (b), the high duty cycle D=0.8 of the low-side transistor can maintain the V_S at 0 V through E_{LS} instead of the discrete diode D. However, the asynchronous converter in Fig.5.4.3 (c) does not

have the problem owing to the integrated driver, which acts as a current booster even at low duty cycles.

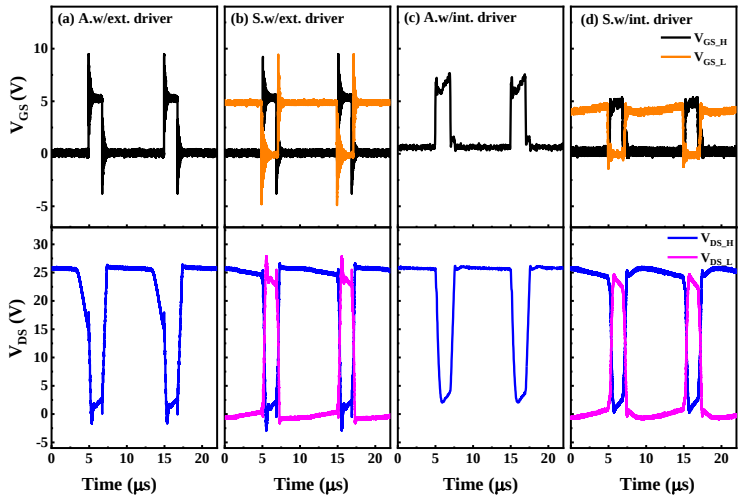


Fig.5.4.3 At room temperature, dynamic V_{GS} and V_{DS} of (a) asynchronous converter w/ external driver, (b) synchronous converter w/ external drivers, (c) asynchronous converter w/ integrated driver in Fig.5.3.1, and (d) synchronous converter w/ integrated drivers in Fig.5.3.3. D=0.2, V_{IN}=25 V, f=100 kHz. V_{GS_H}/V_{GS_L} and V_{DS_H}/V_{DS_L} refer to gate to source voltage and drain to source voltage of high-side/low-side transistors, respectively.

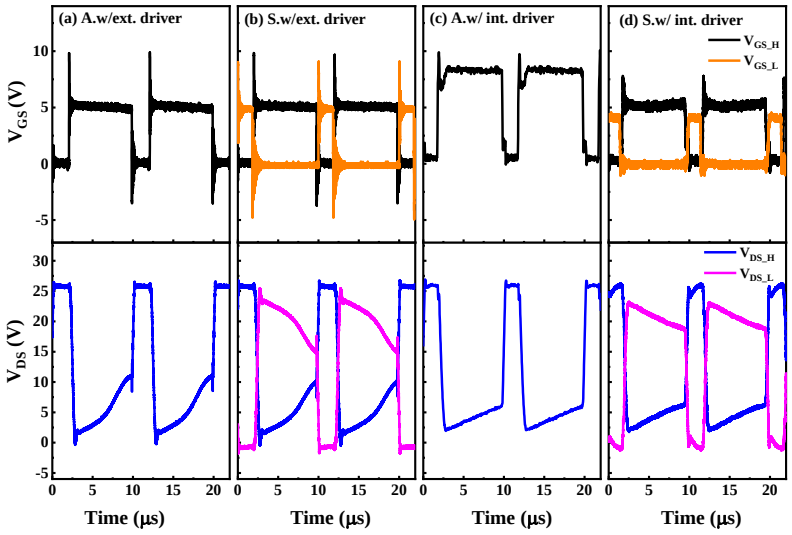


Fig.5.4.4 At room temperature, V_{GS} and V_{DS} of (a) asynchronous converter w/ external driver, (b) synchronous converter w/ external drivers, (c) asynchronous converter w/ integrated driver in Fig.5.3.1, and (d) synchronous converter w/ integrated drivers in Fig.5.3.3. D=0.8, V_{IN}=25 V, f=100 kHz.

Fig.5.4.4 shows dynamic V_{GS} and V_{DS} waveforms of four different converters with a

duty cycle of 0.8 at V_{IN}=25 V. Besides the similar overshoots and oscillations as the previous discussion, converters with external drivers show obvious degradation of dynamic R_{ON} or $V_{DS,\,ON}$ in Fig.5.4.4 (a) and (b). The possible reason might be due to the degradation of dynamic R_{ON} with increased switching loss or increased parasitic inductance by external connection, the increased power loss will be more serious and lead to self-heating problems at a high input voltage of 25 V. This will consequently degrade dynamic R_{ON} and cause output reduction as shown in Fig.5.4.2 (c). Overall, dynamic waveforms in Fig.5.4.3 and Fig.5.4.4 (despite low maximum V_{GS} as the previous discussion) emphasize the importance of the full integration of gate drivers and power transistors, to reduce the parasitic inductance, power loss, and chip size as well.

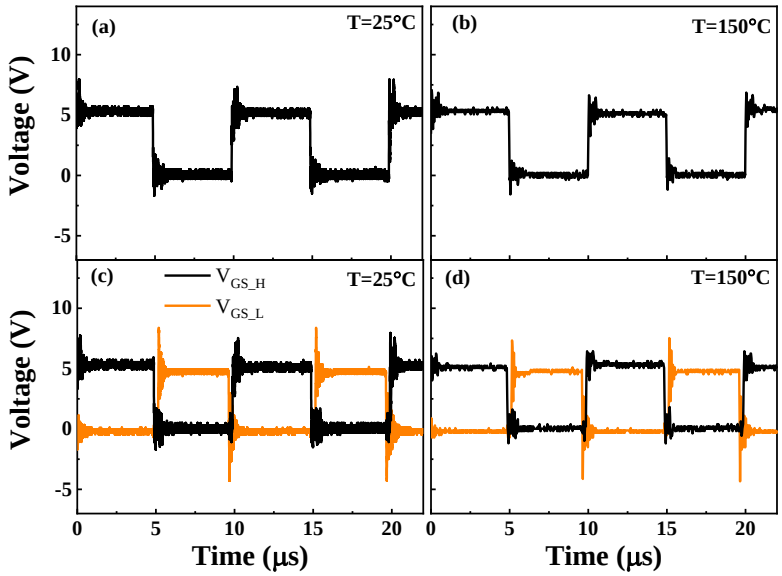


Fig.5.4.5 Dynamic driver waveforms of GaN converters with an external gate driver LM5113. Asynchronous converter (a) 25 ºC and (b) 150 ºC, synchronous converter (c) 25 ºC and (d) 150 ºC, respectively. V_{IN}=25 V, D=0.5, f=100 kHz.

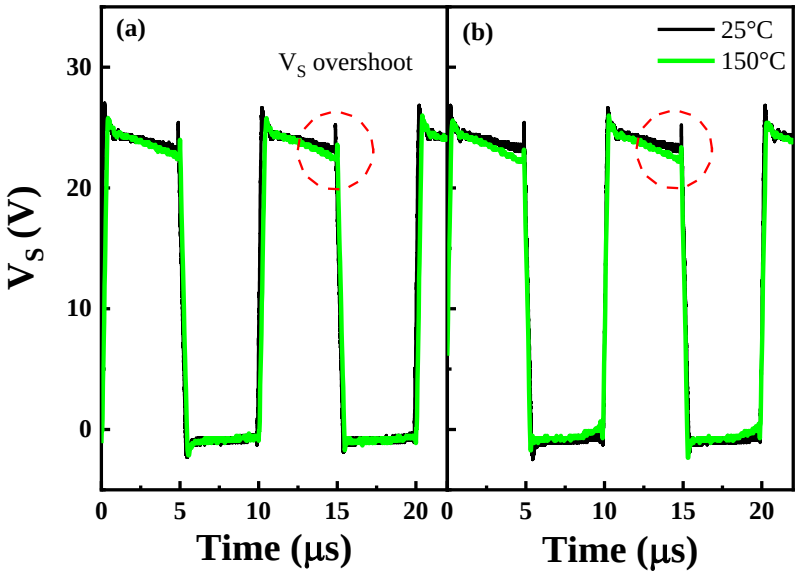


Fig.5.4.6 Dynamic V_S waveforms of GaN converters with the external gate driver LM5113 at 25 ºC and 150 ºC. (a) Asynchronous converter, and (b) synchronous converter. V_{IN}=25 V, D=0.5, f=100 kHz.

The maximum operation temperature of the external driver LM5113 is 150 ºC, so the GaN converters with the external driver were only measured at a high temperature of 150 ºC. The LM5113 PCB was heated using an infrared heater AOYUE883, and the temperature of the external driver was measured using a thermal couple. Fig.5.4.5 shows driver waveforms of GaN converters with the external driver LM5113 at 25 ºC and 150 ºC. The two GaN converters show obvious voltage overshoots and oscillations due to increased parasitic resistance and inductance of external connection as discussed previously. Even though the overshoots and oscillations slightly decrease at 150 ºC in Fig. 5.4.5 (b) and (d), but they are still larger than the GaN converters with integrated gate drivers in Fig.5.3.2 and Fig.5.3.5.

Fig.5.4.6 shows dynamic V_S waveforms of GaN converter with the external driver. At room temperature, both asynchronous converter and synchronous converter show

obvious overshoots, not only at the switching-on transient but also at the switching-off transient. The second overshoot at the switching-off transient of the high-side transistor might be caused by partial co-conduction of two power transistors, which might be caused by the large voltage oscillations of the external driver. However, the GaN converters with integrated gate drivers show almost no overshoot of V_S in Fig.5.3.2 and Fig.5.3.5 in the thesis, indicating the advantages and importance of integrated gate drivers for GaN power converters.

5.5 Conclusion

Monolithic integration of power circuits is essential to fully utilize the advantages of GaN technologies, especially at high temperatures over 200 ℃ for electrical vehicle applications. This chapter addresses the integration of gate drivers with a half-bridge stage based on E-mode GaN MIS-HFETs. The asynchronous and synchronous buck DC-DC converters with integrated gate drivers were evaluated at high temperatures from 25 ℃ to 250 ℃ with a frequency of 100 kHz. Both converters can operate at high temperatures with an input voltage from 15 V to 25 V. However, the synchronous buck converter with a half-bridge stage shows better stability at various temperatures, duty cycles, and input voltages due to the advantages of fast switching transition of the topology. Moreover, the asynchronous and synchronous buck converters with external drivers were also tested and compared, the large voltage overshoots and oscillations were observed and can seriously affect the dynamic waveforms of the converters at low duty

cycles and at a high input voltage of 25 V. These results emphasize the importance of full integration ICs on a single chip in achieving high temperature, high power density, and high-efficiency power converters.

Chapter 6 A GaN no deadtime technique (NDT) for high-temperature (HT) DC-DC buck converters

6.1 Motivation

Deadtime is essential to avoid simultaneous conduction of the high-side power transistor and the low-side synchronous rectifier in half-bridge power converters. Fixed dead-time control [62, 152] is used in many power converters owing to its simplicity of control, and it can be achieved through an external controller to provide two complementary signals. Chapter 5 uses this kind of fixed deadtime technique (FDT), however, it is inflexible when the load conditions vary. A small deadtime can lead to shoot-through currents or even short circuits, while a large deadtime can cause extra power loss during deadtime. The proposed GaN NDT converter uses one pulse width modulation (PWM) signal and provides a simple and effective deadtime method for high-temperature power converters above 200 °C in electric vehicle applications.

Table 6. 1 summarizes the development of deadtime techniques [148, 153-157] for GaN-based converters. Model-based deadtime control methods for GaN converters were reported to optimize deadtime and improve the converter efficiency in [148, 157]. Advanced techniques [153, 155, 156] were developed to optimize deadtime on the gate driver side owing to self-switching techniques, which were based on on-chip CMOS technology. The overlapping driver signals [154] can improve the efficiency of GaN converters without shoot-through current. However, most of these reported techniques

Table 6. 1 Development of Deadtime Techniques for GaN-based Converters

Design	**[153]**	**[154]**	**[155]**	**[148]**	**[156]**	**[157]**	**This Work**
Year	2013	2015	2015	2016	2016	2020	2021
Topology	Synchronous boost	Resonant converter	Synchronous buck	Synchronous boost	Synchronous buck	Synchronous boost	Synchronous buck
GaN technology	E-mode (discrete)	E-mode (discrete EPC2001)	E-mode (discrete EPC2014,2015)	E-mode (discrete EPC2001)	E-mode (discrete EPC2007)	D-mode GaN +Si MOSFET (GaN System GS66508P)	3 μm E-mode GaN
Deadtime technique	On-chip deadtime controller (0.35μm CMOS)	Discrete overlapping driver signals	Deadtime corrector (0.35μm CMOS)	Analytical model	On-chip deadtime controller (0.35μm CMOS)	Adaptive model	Integrated GaN deadtime controller
Gate driver	On-chip	N.A.	On-chip (simulated)	Discrete LM5113	On-chip	Discrete SI8271	Integrated GaN driver
Self switching	Yes	No	Yes	No	Yes	No	Yes
Frequency	1 MHz	500 kHz	1 MHz	400 kHz	100 kHz	500 kHz	100 kHz
Efficiency	99.2%	87.3%	93.6%	95.5%	95%	98%	80%
V_{IN}/V_{OUT}	380V/N.A.	50 V/N.A.	12V/1.2V	24V/80V	45V/10V	250V/400V	30V/15V
$V_{GS,max}$	10 V	5 V	5 V	5 V	5 V	10V	10 V
Temperature	RT	100 °C (junction)	RT	RT	RT	RT	250 °C
Area	N.A.	N.A.	Simulation	N.A.	0.22 mm^2 (CMOS deadtime controller)	N.A.	8.6 mm^2 (all in one)

were based on external management or discrete Si-based CMOS integrated circuits. Seldom studies were reported about GaN-based deadtime management on an integration level. The GaN-based no deadtime technique (NDT) is proposed to provide an all-GaN solution for deadtime management, which shows a maximum efficiency of

80 % at 250 ºC. The integrated GaN circuits have a small chip size of 8.6 mm^2, including a deadtime controller, gate drivers, and power transistors. The all-GaN method provides self-contained functionality for high-temperature converters without external heatsink or cooling systems in electric vehicles.

6.1.1 Fixed deadtime technique (FDT)

Fig.6.1.1 (a) shows the circuit diagram of a GaN-based synchronous DC-DC buck converter, which consists of a bootstrap high-side driver, a low-side driver, a high-side power transistor E_{HS}, a low-side power transistor E_{LS}, two external free wheel diodes, and the load side component. The bootstrap diode D_{BT} and the bootstrap capacitor C_{BT} provide a floating DC power supply V_{BT} when the switching node V_S varies from 0 to V_{IN}. The high-side driver and low-side driver have separate DC power supplies.

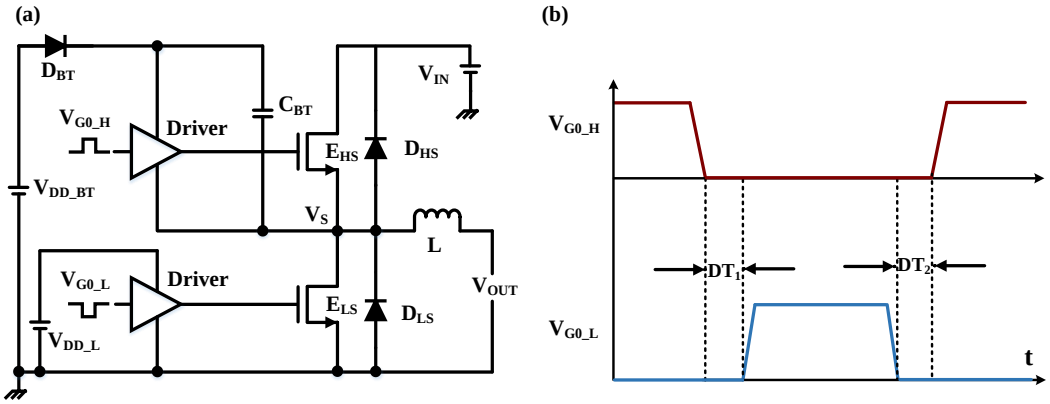


Fig.6.1.1 (a)The circuit diagram and (b) the timing chart of the FDT converter.

In synchronous DC-DC converters, a deadtime is required to avoid simultaneous conduction of two power transistors E_{HS} and E_{LS}. Fig.6.1.1 (b) gives the timing chart of the gate driver signals. Here we define the first deadtime (DT_1) after the high-side transistor E_{HS} turns off, and the second deadtime (DT_2) before the high-side transistor E_{HS} turns on. Fixed deadtime is an easy method for synchronous converters. However,

the fixed deadtime technique requires deadtime optimization when the load conditions vary, and improper design might cause hard switching loss or extra reverse conduction loss during deadtimes.

6.1.2 The proposed GaN NDT

The proposed GaN NDT buck converter is shown in Fig.6.1.2, and the NDT consists of two-stage inverters, two-input AND gates, and two-input NOR gates. The NDT is modified from a Si-based deadtime generator [155] by removing the delay cells to generator two overlapping signals without deadtime. In Fig.6.1.2 (b), one control signal V_{PWM} generates two complementarily overlapping driver signals V_{G0_H} and V_{G0_L} for the high-side driver and low-side driver, respectively. The NDT uses only one control signal and provides a simple way to eliminate deadtime without external control or complex deadtime management.

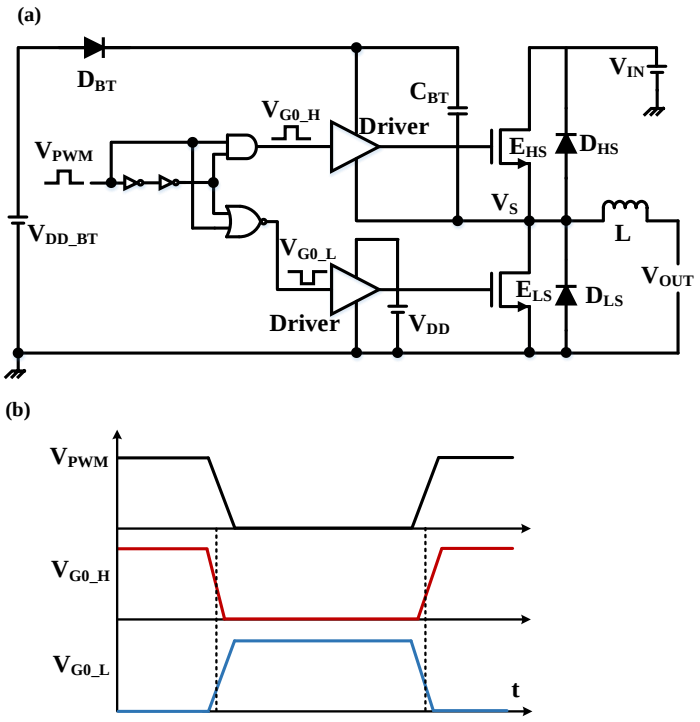


Fig.6.1.2 (a) Circuit diagram and (b) the timing chart of the proposed GaN NDT converter.

In this chapter, the synchronous GaN NDT converter is compared to one synchronous GaN FDT converter with a fixed deadtime control, including the gate driver signals, conversion ratio, and efficiency at various duty cycles and load currents. Then, the impact of driver size on two converters is discussed and the high-temperature measurements were carried out at high temperatures up to 250 °C. At 100 kHz, the integrated GaN converters can achieve a 30 V down conversion. Compared with the FDT converter, the NDT converter exhibits smaller voltage overshoots and oscillations of gate driver signals, and better stability at a high duty cycle of 0.8. The optimized converters with reduced driver sizes can improve the efficiency of converters owing to reduced overshoots and oscillations. At low load currents, both of the optimized GaN buck converters can work at a high temperature up to 250 °C, with a maximum efficiency of 80 %, indicating the excellent performance of recessed E-mode GaN MIS-HFETs for HT converters. At high temperatures with large load currents, the optimized NDT converter shows better efficiency with increasing load currents compared with the optimized FDT converter, owing to its good stability and small voltage overshoots of driver signals at HTs. The results in this chapter provide effective deadtime management for HT power converters in electric vehicle applications.

6.2 Circuit design, simulation, and characterization

6.2.1 Experiment results of GaN NAND gate and NOR gate

Two input GaN NAND and NOR gates are widely used in many areas in digital circuit design. In this chapter, we implement GaN nMOS logic circuits in GaN DC-DC

converters. Two function blocks are fundamental elements of the proposed no-deadtime technique (NDT). Fig.6.2.1 (a) and (b) show the micro-photograph and circuit diagram of GaN two-input NAND gate, respectively. The NAND gate consists of a D-mode active load resistor (50 μm) and two E-mode transistors (2000 μm).

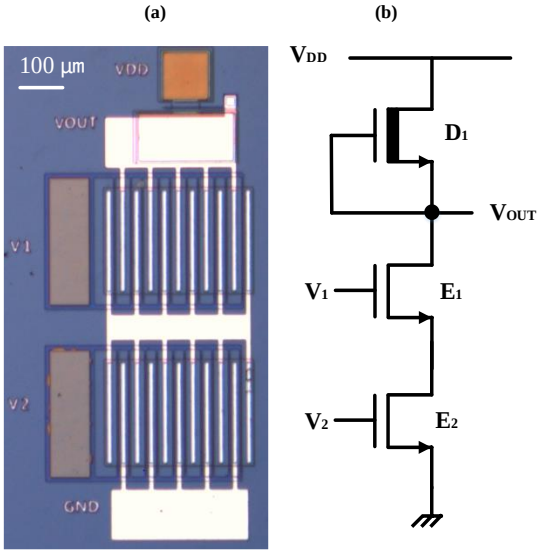


Fig.6.2.1 (a) Micro-photograph and (b) the circuit diagram of GaN NAND gate.

The static voltage transfer curve (VTC) of the GaN NAND gate is demonstrated in Fig.6.2.2 (a). When $V_1=V_2=V_{IN}$, the output high voltage (V_{OH}) is 9 V and the output low voltage (V_{OL}) is 1.12 V. The static logic-low noise margin (NM_L) and logic-high noise margin (NM_H) are 1.03 and 3.78 V, respectively. Fig.6.2.2 (b) shows dynamic waveforms of the NAND gate at 100 kHz. As the figure shows, the function of the GaN NAND gate is logically correct, and the output voltage is low only when both E-mode transistors turn on.

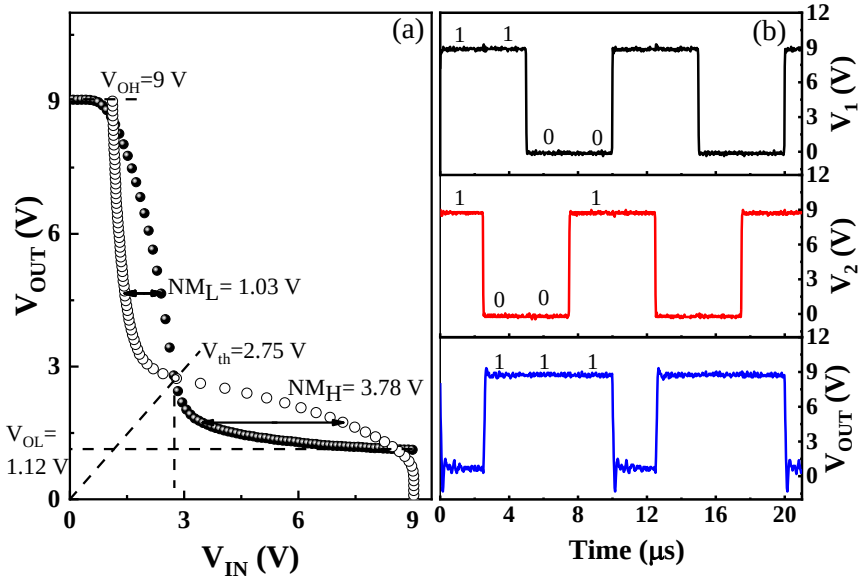


Fig.6.2.2 (a) Static voltage curve (VTC) of GaN NAND gate when V_1=V_2=V_{IN}. (b) Dynamic waveforms at f=100 kHz, V_{DD}=9 V.

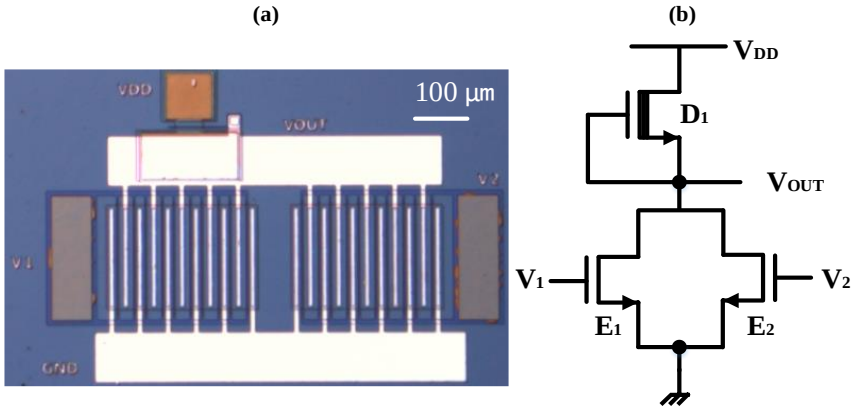


Fig.6.2.3 (a) Micro-photograph and (b) the circuit diagram of GaN NOR gate.

Fig.6.2.3 shows the micro-photograph and the circuit diagram of the GaN two-input NOR gate (W_{D1}=100 μm, W_{E1}=W_{E2}=2000 μm). Fig.6.2.4 (a) shows the VTC characteristic of the GaN NOR gate. When V_1=V_2=V_{IN}, the V_{OH}, and V_{OL} are 9 and 0.47 V, respectively. The lower V_{OL} of the NOR gate is caused by the parallel connection of E-mode transistors, compared with the series connection of NAND gate. The NM_L and NM_H are 1 and 6.7 V, respectively. The dynamic waveforms of the GaN NOR gate is shown in Fig.6.2.4 (b) with a frequency of 100 kHz, and the output voltage

is high only when two E-mode transistors both turn off.

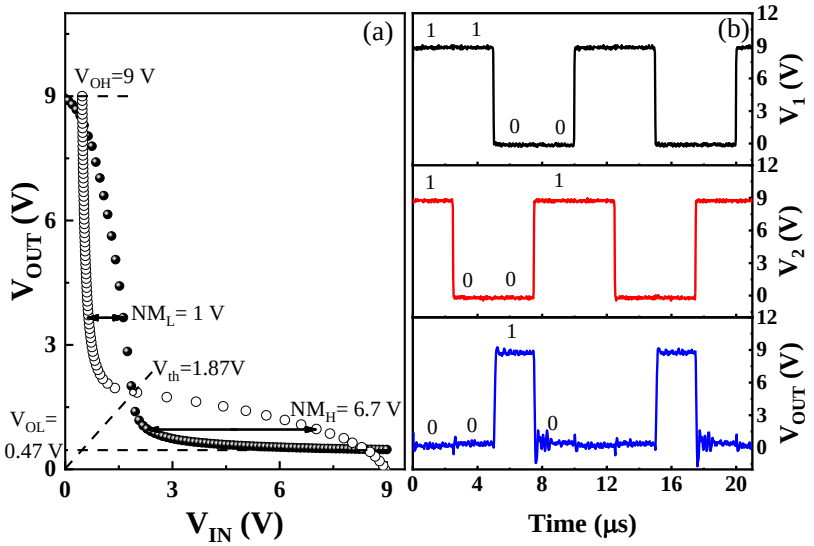


Fig.6.2.4 (a) Static voltage curve (VTC) of GaN NOR gate when V_1=V_2=V_{IN}. (b) Dynamic waveforms. f=100 kHz, V_{DD}=9 V.

6.2.2 Simulation and characterization of the GaN NDT controller

The results of GaN NAND and NOR gates validate the advantages of E-mode MIS-HFETs for GaN ICs and converters. The no deadtime technique (NDT) consists of these basic logic circuits. The micro-photograph and circuit diagram of the proposed GaN NDT are shown in Fig.6.2.5, and the detailed parameters are shown in Table 6. 2.

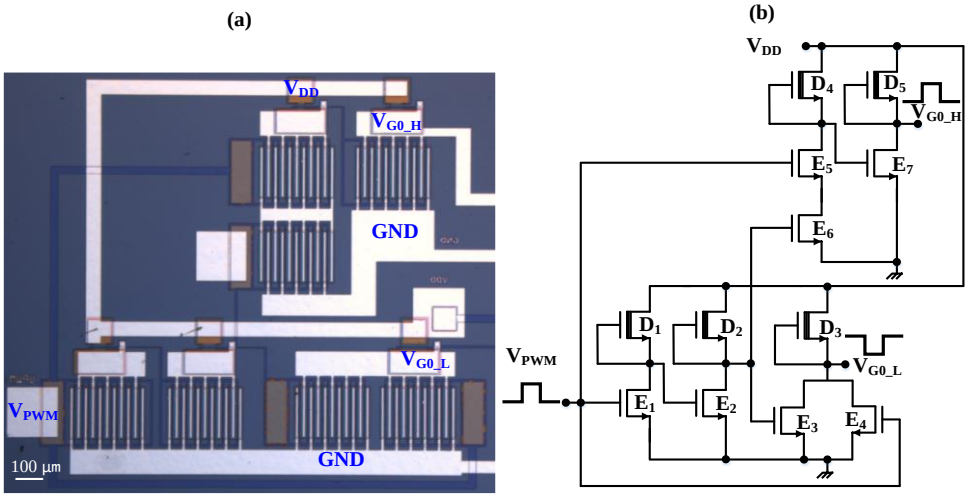


Fig.6.2.5 (a) Micro-photograph and (b) the circuit diagram of the GaN no deadtime technique (NDT).

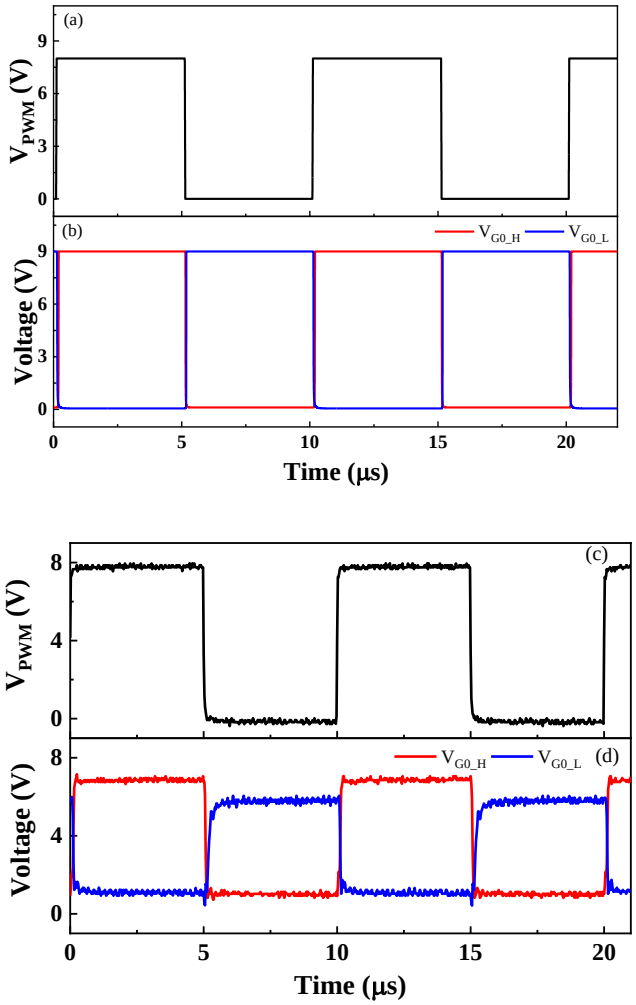


Fig.6.2.6 Dynamic waveforms of the GaN NDT. (a) and (b) simulation, (c) and (d) experiment, f=100 kHz, V_{DD}=9 V.

The simulated and experimental results of the GaN NDT are shown in Fig.6.2.6 (a)-(b) and (c)-(d), respectively. The one control signal V_{PWM} can generate two complementary and overlapping driver signals V_{G0_H} and V_{G0_L}, which are input signals of high-side and low-side drivers, respectively. In this work, the logic high input voltage of the NDT is set as 8 V, and V_{DD} is set as 9 V to avoid unnecessary degradation caused by high gate voltages, even though the GaN-based E-mode MIS-HFET with a high-k gate dielectric has a large gate input swing of more than 10 V. Besides, the logic high output voltages V_{OH} of V_{G0_H} and V_{G0_L} are lower than V_{DD}=9 V, which might be caused

by the interaction between high-side and low-side loops since they share the same power supply voltage V_{DD}. The detailed V_{OH} of gate drivers at various conditions will be discussed later.

6.3 Experiment and characterization of GaN converters

6.3.1 The GaN FDT DC-DC converter

The circuit diagram of the GaN FDT buck converter with a fixed deadtime is shown in Fig.6.3.1 (a), and the detailed parameters are shown in Table 6. 2. One main difference between this work and our previous work [62] in chapter 5 is that the number of DCFL inverter stages is two for both drivers. The experiment setup is shown in Fig.6.3.1 (b), the synchronous buck converter integrated two gate drivers and two power transistors E_{HS}/E_{LS} into one chip. Two external freewheel diodes D_{HS} and D_{LS}, an inductor L, a load capacitor C, and a load resistor R were integrated on a PCB board. The integrated GaN ICs were externally connected with a bootstrap diode D_{BT}, a bootstrap capacitor C_{BT}, and components of the PCB board using probes. The inductor value L is chosen as 1 mH and the load capacitor C is 20 μF, resulting in a small voltage ripple of 0.03 % in buck converters as calculated in chapter 5.

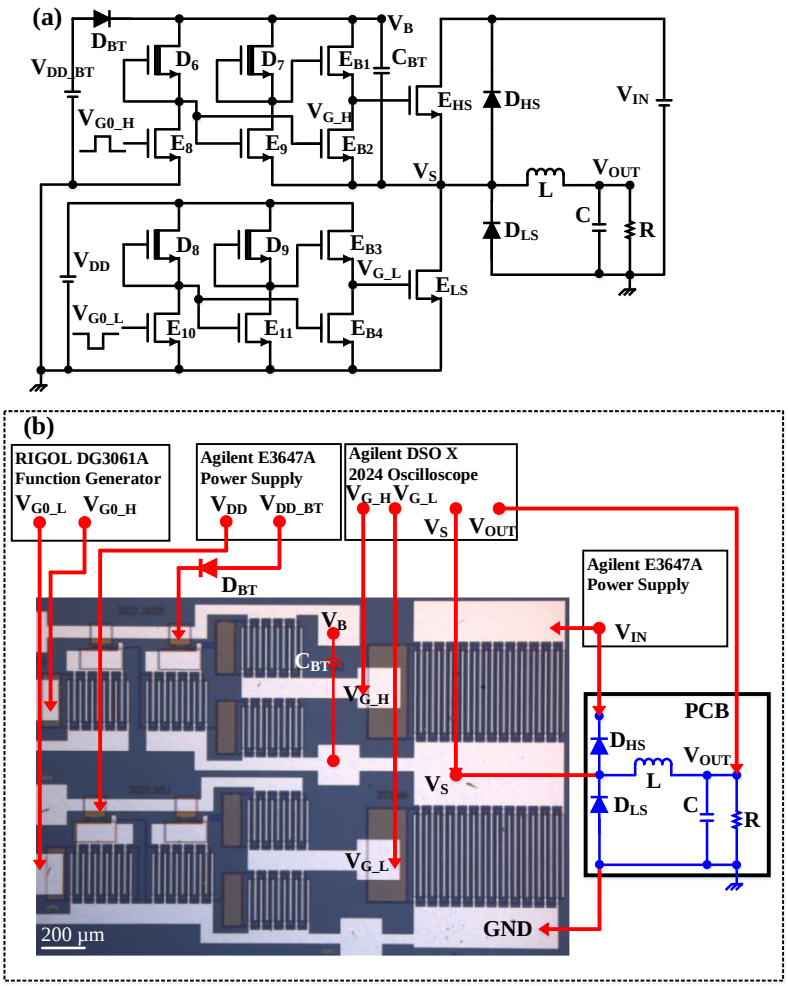


Fig.6.3.1 The circuit diagram of the GaN FDT converter. (b) The experiment setup and microphotograph. (The parameters of discrete components are: L=1 mH, C=20 µF, V_{DD} =V_{DD_BT}=9 V, f=100 kHz. The threshold voltage V_F of the discrete diodes D_{HS}, D_{LS}, and D_{BT} is +0.7 V, C_{BT}= 220 nF.)

Table 6. 2 Summary of device sizes of two converters

	D_1, D_2, D_5 (µm)	D_3 (µm)	D_4 (µm)	D_6~D_9 (µm)	E_1~E_7 (µm)	E_8~E_{11} (µm)	E_{B1}~E_{B4} (µm)	E_{HS}, E_{LS} (mm)
NDT	50	100	25	50	2000	2000	2000	20
FDT	-	-	-	50	-	2000	2000	10

Fig.6.3.2 shows dynamic waveforms at a duty cycle of 0.2, 0.5, and 0.7, where V_{IN} is equal to 25 V with a fixed deadtime of 0.5 µ s. Obvious gate overshoots are observed, and the overshoots of V_{GS_H} (voltage between V_{G0_H} and V_S) are up to 15 V. These large overshoots can be detrimental and even damage power devices using P-GaN E-mode

technology, which has a gate voltage limitation of 7 V [84]. In this work, the recessed gate with a high-k insulator has a large gate swing, exhibiting a dynamic gate voltage tolerance of 20 V. The large overshoots might be caused by the large deadtime in the GaN FDT converter.

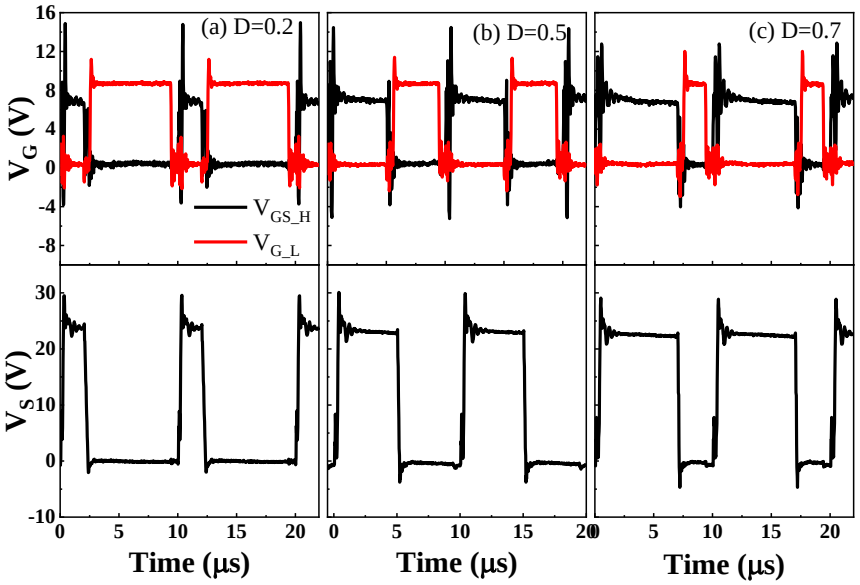


Fig.6.3.2 Dynamic waveforms of the GaN FDT converter in Fig.6.3.1. V_{GS_H}, V_{GL}, and switching node V_S with a fixed deadtime of 0.5 μs. f=100 kHz, V_{IN}=25 V, R=100 Ω. (a) D=0.2, (b) D=0.5, (c) D=0.7.

6.3.2 The GaN NDT converter

A GaN NDT is designed for the synchronous DC-DC buck converter, and the detailed circuit diagram is shown in Fig.6.3.3. The detailed parameters are shown in Table 6. 2. The GaN NDT converter is based on the GaN FDT converter in Fig.6.3.1. The main difference is that the input signal is one control signal V_{PWM} in the GaN NDT converter. The output signals of the GaN NDT are V_{G0_H} and V_{G0_L}, which are similar to the input control signals of two integrated drivers in the GaN FDT converter in Fig.6.3.1.

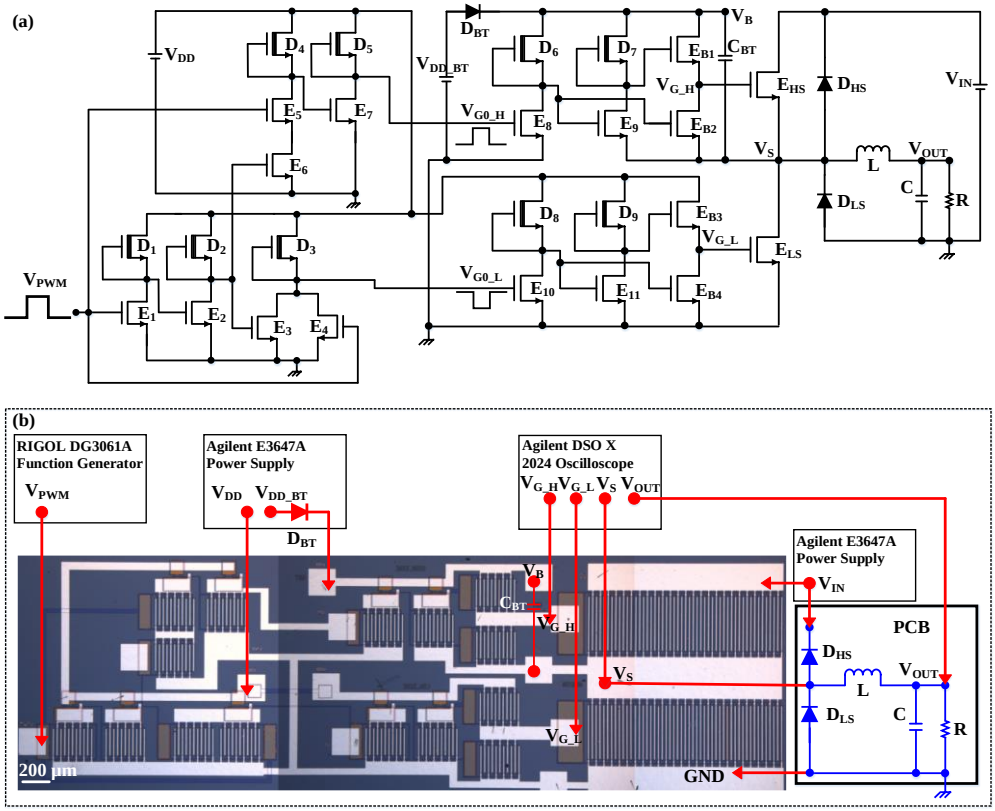


Fig.6.3.3 The circuit diagram of the GaN NDT converter. (b) The experiment setup and microphotograph. (The parameters of discrete components are: L=1 mH, C=20 μF, V_{DD} =V_{DD_BT}=9 V, f=100 kHz. The threshold voltage V_F of the discrete diodes D_{HS}, D_{LS}, and D_{BT} is +0.7 V, C_{BT}= 220 nF.)

Fig.6.3.4 shows ADS simulated results of the proposed GaN NDT converter, which are comparable with theoretical calculation (blue line) using equation (5.1) with an input voltage of 25 V. Fig.6.3.4 (b) shows the transient output voltage with a duty cycle of 0.5, and the output voltage is stable after a startup time of 300 μs. The simulation results validate the function ability of the proposed GaN NDT converter without deadtime. Due to the difference between the simulation model and the real performance of the GaN devices, like trap-induced dynamic R_{ON}, a more accurate model is required to match the results between simulation and experiment on a circuit level.

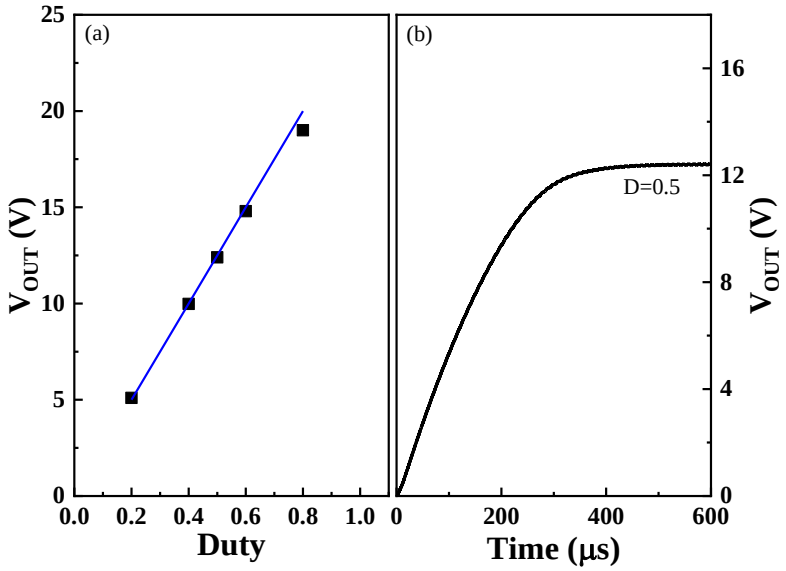


Fig.6.3.4 ADS simulated results of the proposed GaN NDT converter. (a) Output voltages versus duty cycle (theoretical result as the blue line), (b) simulated result with a duty cycle of 0.5. R=500 Ω, f=100 kHz, V_{IN}=25V.

Fig.6.3.5 shows the experimental waveforms of the GaN NDT converter with a duty cycle of 0.2, 0.5, and 0.8. The output signals of gate drivers have smaller voltage overshoots and oscillations than the synchronous FDT converter in Fig.6.3.2. The maximum overshoot voltage in Fig.6.3.5 is 12 V, smaller than 15 V in Fig.6.3.2. Besides, owing to the smaller oscillation, the GaN NDT converter can steadily operate at a high duty cycle of 0.8, while only a 0.7 duty cycle can be steadily achieved in Fig.6.3.2. This outstands the advantages of the NDT converter over the FDT converter, in terms of the small voltage overshoots, oscillations, and capability of operation at high duty cycles as well.

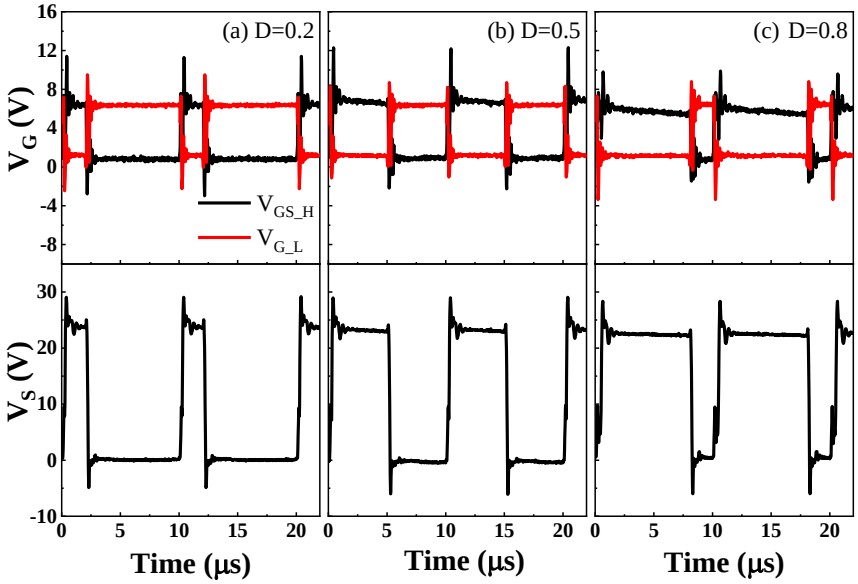


Fig.6.3.5 Experimental waveforms of the GaN NDT converter in Fig.6.3.3. V_{GS_H}, V_{G_L}, and switching node V_S. f=100 kHz, V_{IN}=25 V, R=100 Ω. (a) D=0.2, (b) D=0.5, (c) D=0.8.

6.4 Measurement results and discussions between two converters

6.4.1 The impact of load conditions on the performance of gate drivers

In this section, a detailed comparison is made between the GaN FDT converter in Fig.6.3.1 and the GaN NDT converter in Fig.6.3.3. Firstly, the output signals of gate drivers are compared at various load conditions, duty cycles, and different input voltages, as shown in Fig.6.4.1 (the FDT converter) and Fig.6.4.2 (the NDT converter), respectively. The maximum voltage of stable V_{GS_H} ($V_{GS\_H,Max}$) of the FDT converter in Fig.6.4.1 is around 7~8 V, which is overall larger than the 5~7 V of the NDT converter in Fig.6.4.2. Unlike $V_{GS\_H,Max}$ in Fig.6.4.1, the NDT converter in Fig.6.4.2 shows an obvious increasing trend with increasing load resistance, which might be caused by reduced voltage oscillations at high currents. The reason why $V_{GS\_H,Max}$ of the FDT

converter does not exhibit an obvious trend with load currents in Fig.6.4.1, might be due to the large voltage oscillations. Besides, the $V_{GS\_H,Max}$ of the NDT synchronous converter shows a decreased value at a high duty cycle of 0.8, which might be attributed to increased R_{ON} at a high duty cycle or high current.

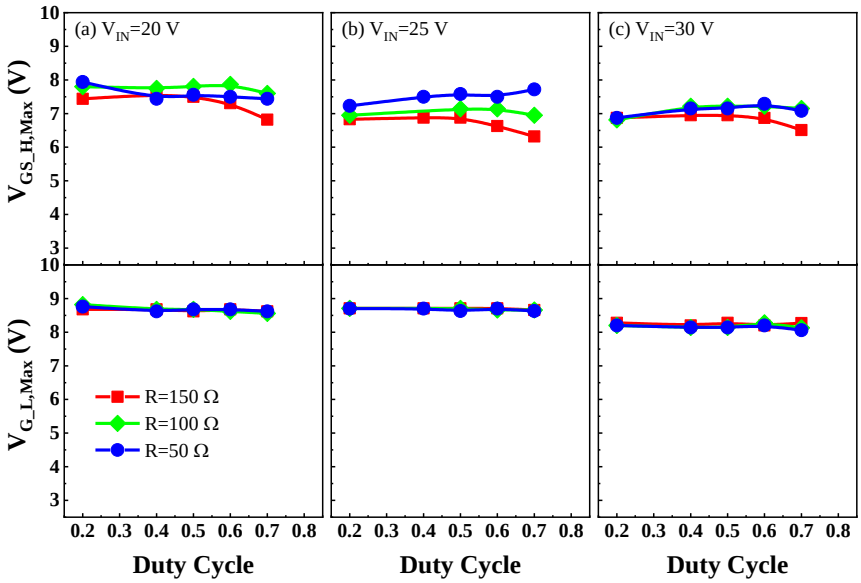


Fig.6.4.1 Measured stable logic-high voltage of V_{GS_H} ($V_{GS\_H,Max}$) and logic-high voltage of V_{G_L} ($V_{G\_L,Max}$) of the FDT converter at various load conditions and duty cycles. DT_1=DT_2=0.5 μ s. (a) V_{IN}=20 V, (b) V_{IN}=25 V, and V_{IN}=30V.

Secondly, for the maximum voltage of stable V_{G_L} ($V_{G\_L,Max}$), both the FDT converter and the NDT converter almost show no relationship with load conditions and duty cycles. $V_{G\_L,Max}$ of the FDT converter in Fig.6.4.1 is around 8.6 V at V_{IN}= 20, 25 V, and this value decreases slightly to 8.2 V at V_{IN}=30 V. Unlike $V_{GS\_H,Max}$, the independence of $V_{G\_L,Max}$ on load currents is attributed to the source-grounded loop of the low-side driver, because $V_{G\_L,Max}$ is determined by the low-side power supply V_{DD}. On the other hand, $V_{G\_L,Max}$ of the NDT converter in Fig.6.4.2 is around 6.3 V at various load currents, input voltages, and duty cycles, and the lower $V_{G\_L,\,Max}$ than 8.6 V of the FDT converter might be caused by the interaction between the high-side and low-side drivers.

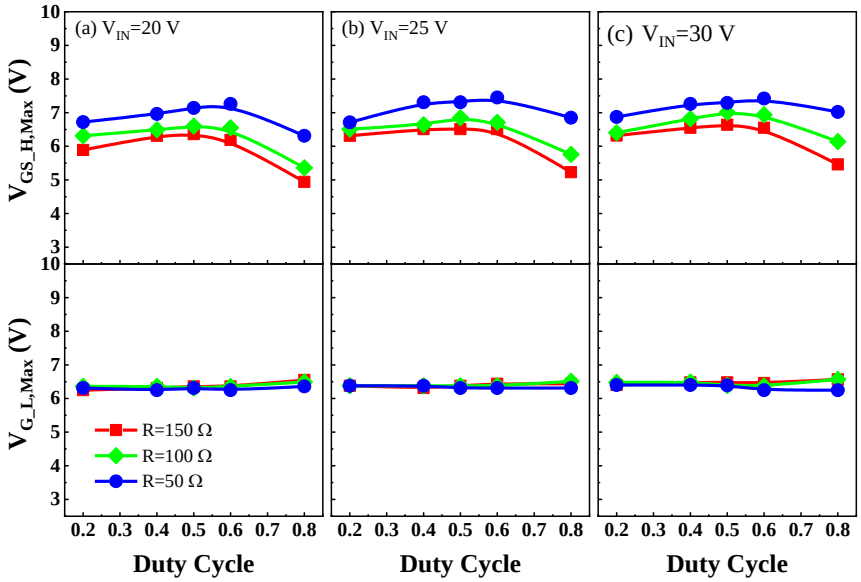


Fig.6.4.2 Measured stable logic-high voltage of V_{GS_H} ($V_{GS\_H,Max}$) and logic-high voltage of V_{G_L} ($V_{G\_L,Max}$) of the NDT converter at various load conditions and duty cycles. (a) V_{IN}=20 V, (b) V_{IN}=25 V, and V_{IN}=30 V.

6.4.2 Converter results comparison at room temperature

The conversion ratio *M* is equal to the ratio of the output voltage to the input voltage of the converter. The converter ratio is compared between the FDT converter in Fig.6.4.3 and the NDT converter in Fig.6.4.4, at various load currents and duty cycles. Ideally, the conversion ratio *M* is equal to the duty cycle. However, both converters show a degraded ratio at high load currents, which might be caused by increased R_{ON} at high load currents. Considering the non-negligible on-state voltage drop of two power transistors due to increased R_{ON} at high currents, the output voltage can be expressed as:

$$\int_0^{T_s} v_L(t)\cdot dt = 0$$

$$(V_{IN} - V_{OUT} - V_{ON,HS})\cdot D + (-V_{OUT} - V_{ON,LS})\cdot(1-D) = 0$$

Where D is the duty cycle of the high-side transistor. $V_{ON,\,HS}$ is the drain-to-source

voltage when the high-side transistor is at on-state, and $V_{ON,\,LS}$ is the on-state drain-to-source voltage of the low-side transistor. Since both transistors have the same width, it is reasonable to assume that $V_{ON,\,HS}$ is equal to $V_{ON,\,LS}$. Here we define V_{ON} as on-state voltage drop of power transistors, $V_{ON}=V_{ON,\,HS}=V_{ON,\,LS}$, then the output voltage of the buck converter can be expressed as formula (6.1):

$$V_{OUT} = V_{IN} \cdot D - V_{ON} \tag{6.1}$$

Then, the conversion ratio M is expressed using formula (6.2) and (6.3):

$$M = D - \frac{V_{ON}}{V_{IN}} \tag{6.2}$$

$$M = D - \frac{I_{OUT} \cdot R_{ON}}{V_{IN}} \tag{6.3}$$

Differentiate both sides of formula (6.3) with respect to I_{OUT}:

$$k_{conversion} = \frac{dM}{dI_{OUT}} = -\frac{R_{ON}}{V_{IN}} \tag{6.4}$$

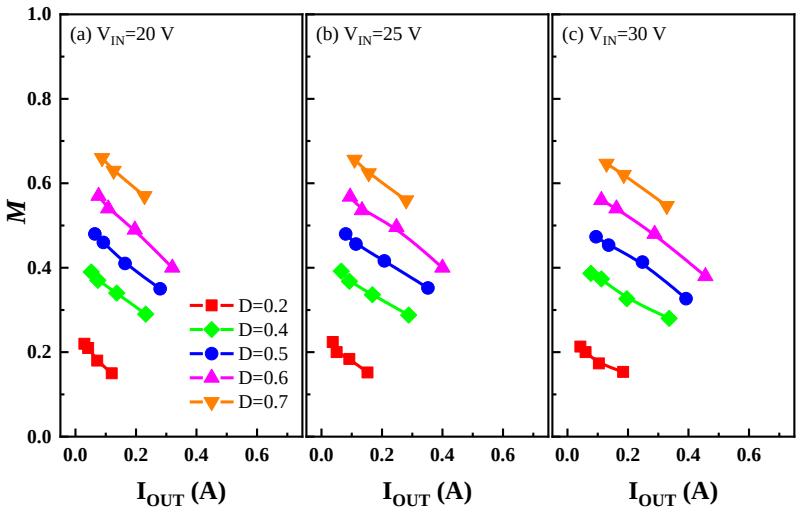


Fig.6.4.3 Voltage conversion ratio (M) of the GaN FDT converter at various conditions. (a) V_{IN}=20 V, (b) V_{IN}=25 V, and (c) V_{IN}=30 V.

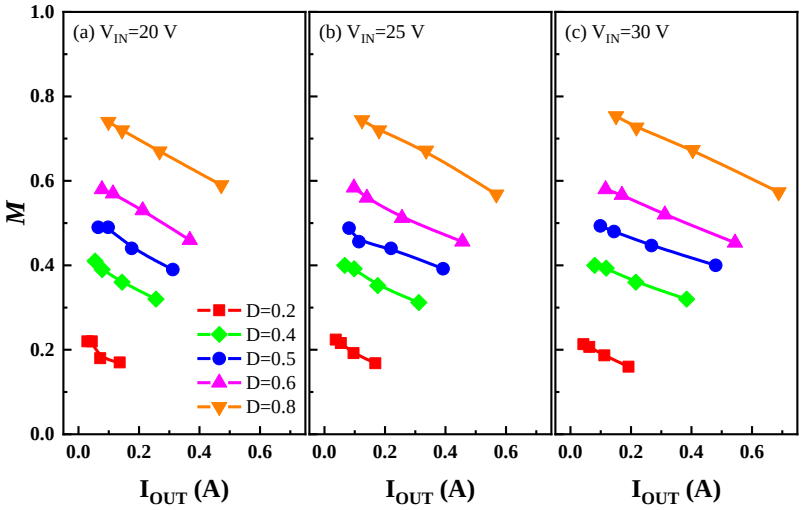


Fig.6.4.4 Voltage conversion ratio (*M*) of the GaN NDT converter. (a) V_{IN}=20 V, (b) V_{IN}=25 V, and (c) V_{IN}=30 V.

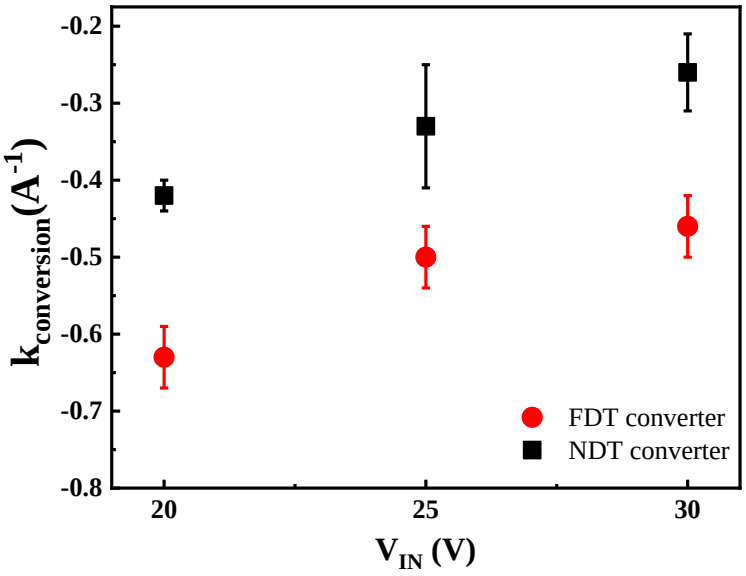


Fig.6.4.5 Calculated $k_{conversion}$ of two converters at various input voltages.

The conversion ratio *M* depends on on-state voltage drop V_{ON}, and this can explain the reduced *M* at high load currents in Fig.6.4.3 and Fig.6.4.4. $k_{conversion}$ is the derivative of *M* to the load current, which is dependent on the ratio R_{ON}/V_{IN}, and independent of the duty cycle as shown in the two figures. The $k_{conversion}$ can be extracted from Fig.6.4.3 and Fig.6.4.4, results as shown in Fig.6.4.5. $k_{conversion}$ increases with V_{IN}, which

coincides with the formula (6.4). Besides, the $k_{conversion}$ of the NDT converter is larger than that of the FDT converter, which is caused by the lower R_{ON} with larger transistor width in the NDT converter in Table 6. 2. Using formula (6.4), the R_{ON} is calculated around 8 Ω and 13 Ω for the NDT converter and FDT converter, respectively.

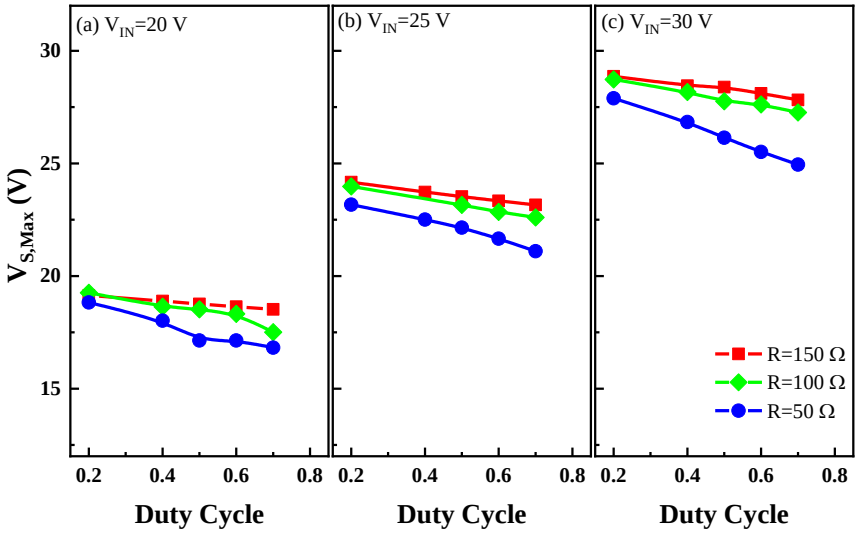


Fig.6.4.6 The maximum voltages of the stable switch node V_S in the GaN FDT converter at various load resistances. (a) V_{IN}=20 V, (b) V_{IN}=25 V, and (c) V_{IN}=30 V.

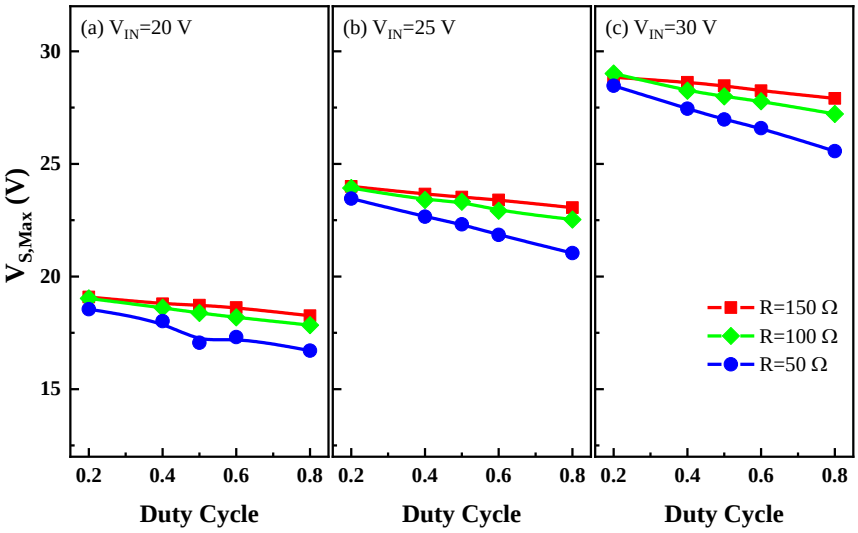


Fig.6.4.7 The maximum voltages of the stable switch node V_S in the GaN NDT converter at various load resistances. (a) V_{IN}=20 V, (b) V_{IN}=25 V, and (c) V_{IN}=30 V.

To analyze the current induced degradation of the conversion ratio *M*, the maximum

voltages of stable V_S (switching node) at various load conditions of the FDT converter and NDT converter are shown in Fig.6.4.6 and Fig.6.4.7, respectively. Ideally, the maximum voltage of the stable switch node V_S ($V_{S,Max}$) is equal to V_{IN}, and $V_{S,Max}$ is lower than V_{IN} when considering R_{ON} in a real condition. The difference between V_{IN} and $V_{S,Max}$ is equal to the drain-to-source voltage when the high-side transistor turns on. From the figures, $V_{S,Max}$ decreases not only with increasing load resistances but also with increasing duty cycles. This might be caused by increased R_{ON} due to current collapse at high currents or high duty cycles, indicating the disadvantages of increased R_{ON} caused by the recessed channel in this work. The recessed channel can affect R_{ON} of power transistors and thus the efficiency of the power converters as well.

At room temperature, Fig.6.4.8 and Fig.6.4.9 show the efficiency of the FDT converter and the NDT converter at various conditions, respectively. Both converters show an overall stable efficiency of 60 % ~70 % at large load currents. The FDT converter shows a maximum efficiency of 71 % at 5.4 W, and the NDT converter shows a maximum efficiency of 73 % at 8 W. Owing to small voltage oscillations, the NDT converter can operate at a high duty cycle of 0.8 and a larger load power of 11.8 W when the input voltage is 30 V with a load resistance of 50 Ω. Besides, at D=0.2, the NDT converter appears to show lower efficiency than the FDT converter, which might be caused by conduction loss of the low-side transistor (1-D=0.8). The FDT converter with a deadtime of 0.5 μs can reduce the duty cycle and thus conduction loss of the low-side transistor. R_{ON}-induced conduction loss of power transistors plays an important role in the total power loss of the GaN converter, and reverse conduction loss

during deadtime is not the main factor in this work.

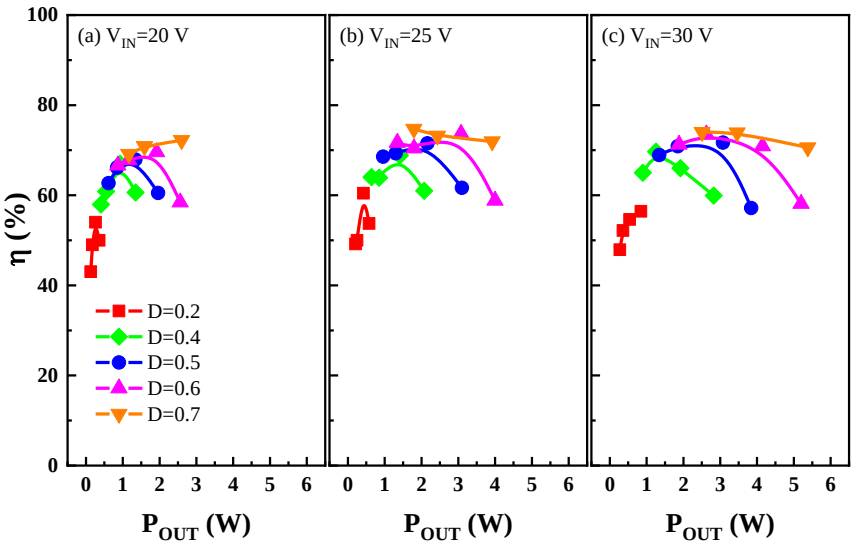


Fig.6.4.8 The efficiency of the GaN FDT converter at various conditions. (a) V_{IN}=20 V, (b) V_{IN}=25 V, (c) V_{IN}=30 V.

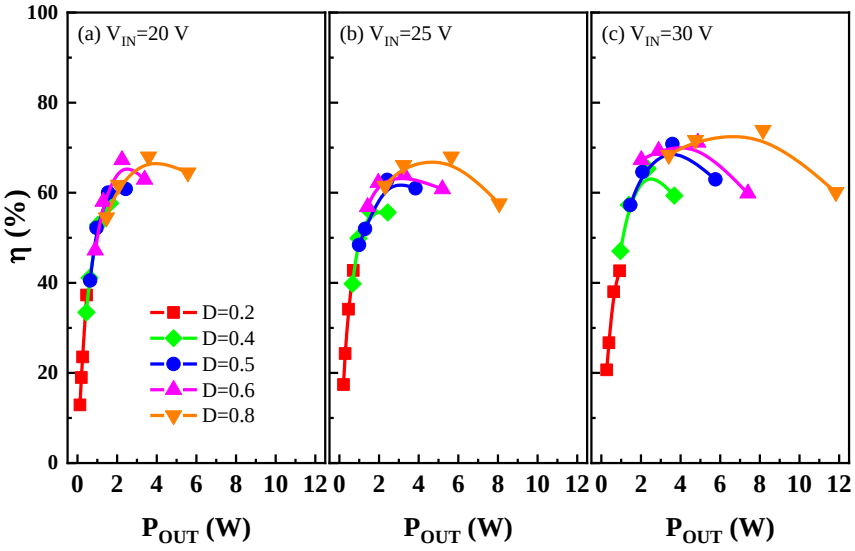


Fig.6.4.9 Efficiency of the GaN NDT converter at various conditions. (a) V_{IN}=20 V, (b) V_{IN}=25 V, (c) V_{IN}=30 V.

6.4.3 The impact of driver sizes on the GaN converters

To study the impact of the driver sizes on the efficiency of GaN converters, two

optimized converters are designed as shown in Table 6. 3. Compared with Table 6. 2, the main difference in Table 6. 3 is the reduction of sizes of the NDT driver and the FDT driver. Both the NDT converter and the FDT converter have the same width of power transistors of 20 mm.

Table 6. 3 Optimized parameters for GaN synchronous DC-DC converters

	D_1, D_2, D_5 (μm)	D_3 (μm)	D_4 (μm)	D_6~D_9 (μm)	E_1~E_7 (μm)	E_8~E_{11} (μm)	E_{B1}~E_{B4} (μm)	E_{HS}, E_{LS} (mm)
NDT	25	50	12.5	25	1000	1000	2000	20
FDT	-	-	-	25	-	1000	2000	20

At room temperature, D=0.5, V_{IN} =25 V, Fig.6.4.10 gives dynamic waveforms of gate drivers of four different converters. The small driver sizes (W_D/W_E=25/1000 μm) in Fig.6.4.10 (c) and (d) show smaller overshoots and oscillations than the large sizes (W_D/W_E=50/2000 μm) in Fig.6.4.10 (a) and (b). The dynamic waveforms V_S and the converter efficiency of four converters are shown in Fig.6.4.11. The optimized converters in Table 6. 3 show an overall increase of power efficiency than the converters in Table 6. 2. A close comparison shows that the larger sizes of DCFL inverters have larger V_S overshoots when the high-side transistor switches on, and larger V_S undershoots when the high-side transistor switches off. Given V_{IN}=25 V, the large V_S overshoots and undershoots can cause extra switching loss. This can explain the efficiency improvement from 52 % to 66 % in the NDT converter, and 69 % to 73 % in the FDT converter, when DCFL sizes (W_D/W_E) decrease from 50/2000 μm to 25/1000 μm.

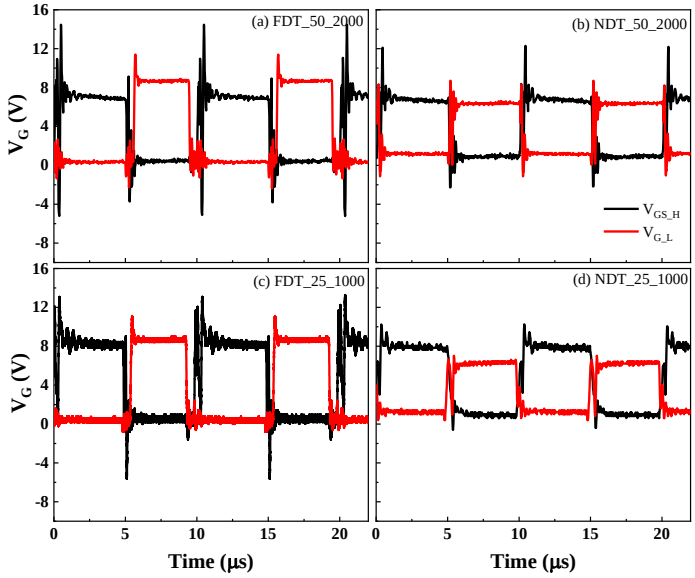


Fig.6.4.10 Dynamic waveforms of gate drivers. (a) FDT converter (DCFL inverter: W_D/W_E=50/2000 μm) in Table 6. 2; (b) NDT converter (W_D/W_E=50/2000 μm) in Table 6. 2; (c) the optimized FDT converter (25/1000 μm); (d) the optimized NDT converter (W_D/W_E=25/1000 μm). D=0.5, V_{IN}=25 V, R=100 Ω, T= 25 °C.

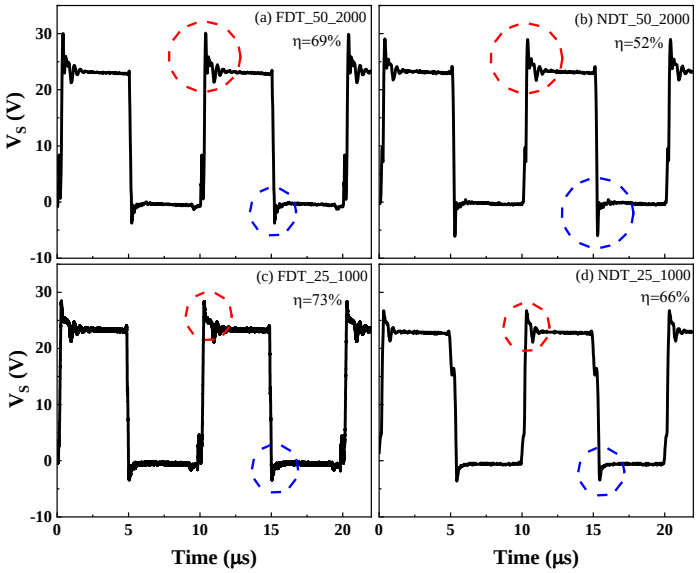


Fig.6.4.11 Dynamic V_S waveforms (a) FDT converter (DCFL inverter: W_D/W_E=50/2000 μm) in Table 6. 2; (b) NDT converter (W_D/W_E=50/2000 μm) in Table 6. 3; (c) the optimized FDT converter (25/1000 μm); (d) the optimized NDT converter (W_D/W_E=25/1000 μm). D=0.5, V_{IN}=25 V, R=100 Ω, T= 25 °C.

6.4.4 Converter results comparison at high temperatures

At room temperature, the comparison of two optimized converters in Table 6. 3 is

similar to the discussion in section 6.4.2, and will not be included here. In this section, the main purpose is to compare two optimized converters at high temperatures, and to evaluate two different deadtime methods for HT power converters in electric vehicle applications that require operation above 200 °C. Fig.6.4.12 shows dynamic waveforms of the optimized GaN NDT at room temperature and 250 °C, where V_{G0_H} and V_{G0_L} are two complementary output signals of the GaN NDT. When V_{DD} is equal to 9 V, the logic-high output voltages of V_{G0_H} and V_{G0_L} are around 8 V.

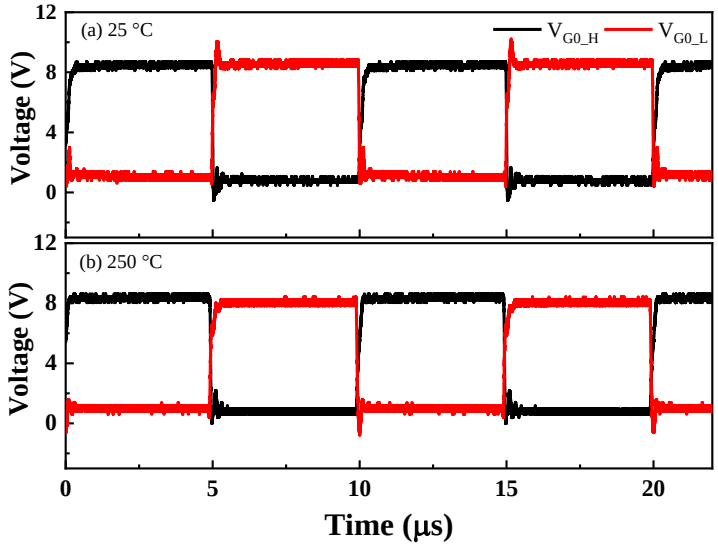


Fig.6.4.12 Dynamic waveforms of the optimized GaN NDT. (a) 25 °C, (b) 250 °C. V_{G0_H} and V_{G0_L} are two complementary output signals of the GaN NDT. V_{DD}=9 V, f=100 kHz.

In synchronous DC-DC converters with a fixed deadtime, the deadtime varies and needs to be optimized at various load currents [158], the GaN-based no deadtime technique (NDT) eliminates deadtimes at various load conditions. In synchronous DC-DC converters with fixed deadtimes, only negative deadtimes cause shoot-through loss [148]. The two overlapping gate driver signals in this chapter are generated through GaN logic circuits, so the complementary driver signals with zero deadtimes cannot be

at logic-high states or two power transistors cannot turn on simultaneously, which avoids short circuit of the GaN NDT power converter. However, there might be partial turn-on concern in the proposed NDT converter. The small deadtimes affect the efficiency of power converters owing to partial turn-on loss, and the optimal deadtime varies at various load currents [148]. In this chapter, the partial turn-on loss has no significant impact on the converter efficiency, since the maximum efficiency of the proposed NDT converter is comparable with the GaN FDT (fixed deadtime technique) converter. Besides, the partial turn-on in the NDT converter can accelerate the switching transition, and this shows obvious advantages at high temperatures than the FDT converter, which will be discussed later.

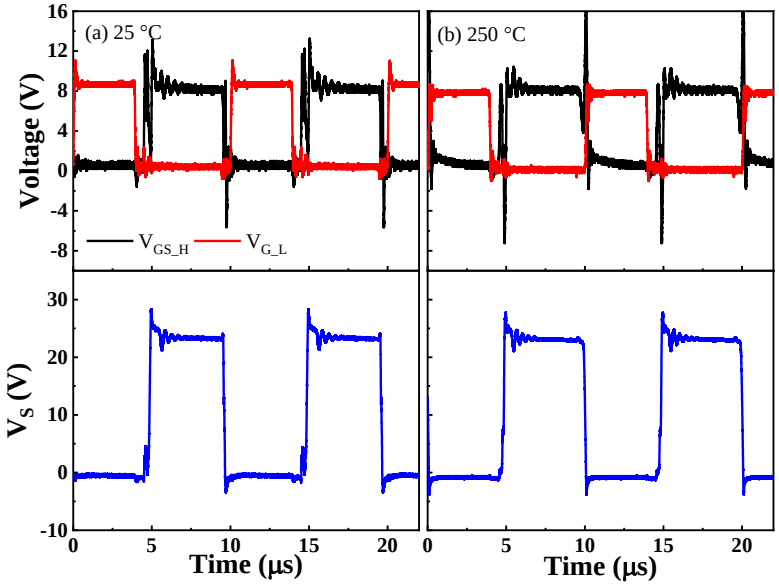


Fig.6.4.13 Dynamic waveforms of the optimized GaN FDT converter. (a) 25 °C, (b) 250 °C. V_{DD}=9 V, f=100 kHz, V_{IN}=25 V, R=100 Ω.

The dynamic waveforms of the optimized GaN FDT converter are shown in Fig.6.4.13 at 25 °C and 250 °C with a fixed deadtime of 0.5 μs, and Fig.6.4.14 shows dynamic waveforms of the optimized GaN NDT converter. From two figures, two

conclusions can be made: (1) at room temperature, compared with large sizes of gate drivers in Fig.6.3.2 and Fig.6.3.5, the optimized GaN FDT and GaN NDT converters show smaller voltage oscillations and overshoots as discussed in Fig.6.4.10. This can be explained by smaller charging and discharging currents with smaller sizes, which reduces the voltage oscillations and overshoots. (2) At a high temperature of 250 °C, the optimized FDT converter shows an obvious voltage overshoot over 16 V during the first deadtime (DT_1) when the high-side transistor turns off, and a reduced deadtime is simultaneously observed in Fig.6.4.13 (b). However, the NDT converter shows smaller oscillations and overshoots at 250 °C in Fig.6.4.14 (b), owing to the contribution of no deadtime topology.

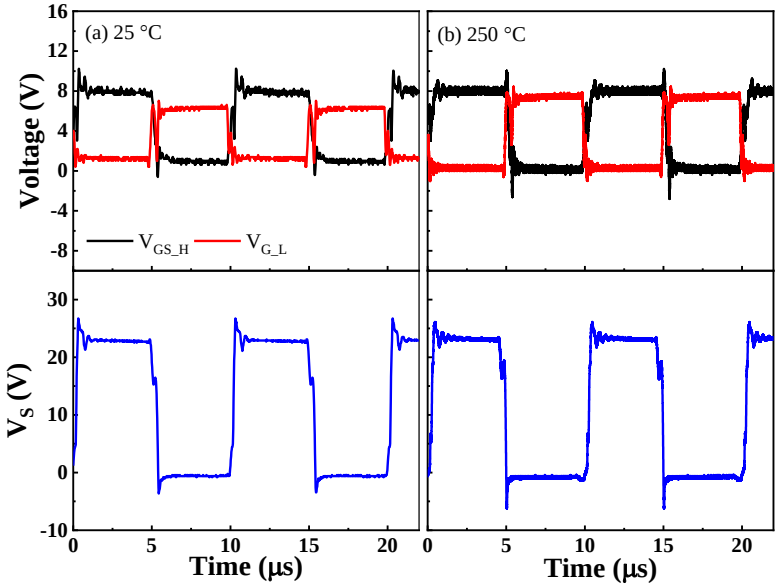


Fig.6.4.14 Dynamic waveforms of the optimized GaN NDT converter. (a) 25 °C, (b) 250 °C. V_{DD}=9 V, f=100 kHz, V_{IN}=25 V, R=100 Ω.

For the second conclusion, in the GaN FDT converter with a fixed deadtime of 0.5 μs, there are two differences between 25 °C and 250 °C during the first deadtime DT_1 in Fig.6.4.13. The first difference is the overshoots of V_{GS_H}, and the second difference

is the delay of V_{GS_H}. The V_{GS_H} delay is related to a delay time t_d between V_{GS_H} and V_{G0_H} and leads to a reduced deadtime of DT_1 even with a fixed value. This delay time t_d is caused by increased R_{ON} of the power transistor and thus a RC delay at high temperatures. Fig.6.4.15 shows the dynamic driver waveforms of the optimized FDT converter with V_{IN}=0 V at 250 °C. The output signal of the high-side driver V_{G_H} (blue line) shows almost no delay from the input signal V_{G0_H}, which indicates that the delay time t_d has no relationship with GaN drivers.

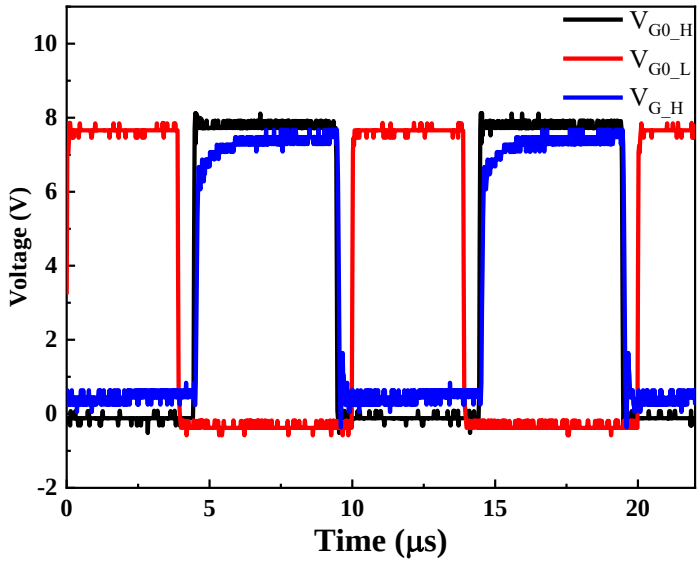


Fig.6.4.15 Dynamic driver waveforms of the optimized FDT converter (Table 6. 3) with V_{IN}=0 V, V_{DD}= 9 V, T=250 °C. V_{G0_H} are V_{G0_L} are input signals of the high-side and low-side drivers, respectively. V_{G_H} is the output signal of the high-side driver.

For the V_{GS_H} delay, the explanation is given as bellows. Fig.6.4.16 (a) and (b) show the more detailed waveforms of Fig.6.4.13, and Fig.6.4.16 (c) and (d) are enlarged images of Fig.6.4.16 (a) and (b), respectively. When the high-side transistor turns off or V_{G0_H} goes low, a small delay t_d between V_{G_H} and V_{G0_H} is observed at 25 °C, and this value increases at 250 °C in Fig.6.4.16 (b). However, the low-side driver does not exhibit such a delay between V_{G0_L} and V_{G_L}, which might be caused by the source-

grounded scheme of the low-side driver and power transistor. The enlarged view in Fig.6.4.16 (c) shows a small delay t_d of 0.14 μs at room temperature, and this value increases to a value of around 0.6 μs at 250 °C in Fig.6.4.16 (d). The t_d delay might be caused by the discharging delay of floating V_S, the high temperature can cause an increased R_{ON} and thus a larger delay t_d in Fig.6.4.16 (d).

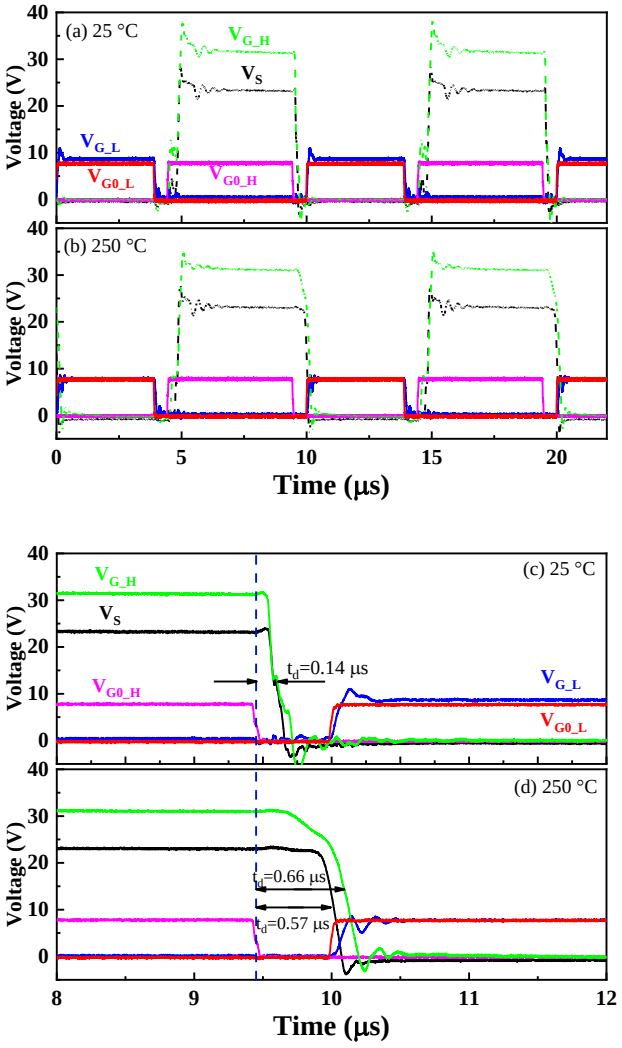


Fig.6.4.16 Dynamic waveforms of the optimized FDT converter (more detailed of Fig.6.4.13). (a) 25 °C, (b) 250 °C, (c) and (d) are enlarged images of (a) and (b), respectively. V_{G0_H}/V_{G0_L} and V_{G_H}/V_{G_L} are input signals and output signals of the high-side/low-side drivers, respectively. f=100 kHz, V_{IN}=25 V, R=100 Ω.

Except for the large t_d at 250 °C, a delay around 0.09 μs between V_{G_H} (green line)

and V_S (black line) is also observed at 250 °C in Fig.6.4.16 (d), while no obvious delay is observed at room temperature in Fig.6.4.16 (c). For an ideal case, V_{G_H} changes simultaneously with V_S, and the delay (between V_{G_H} and V_S) at 250 °C indicates that V_S changes more slowly than V_{G_H} during the first deadtime DT_1, and this delay can explain the large V_{GS_H} overshoots at 250 °C in Fig.6.4.13 (b). The reason why the output driver signal V_{GS_H} (voltage between V_{G_H} and V_S) of the FDT converter has large overshoots at high temperatures can be explained by the slower discharging of V_S owing to increased R_{ON} and delay compared with the V_{G_H} signal. However, the NDT converter without deadtime speeds up the discharging process of switching node V_S owing to the switch-on of the low-side transistor, resulting in smaller overshoots during the first deadtime DT_1.

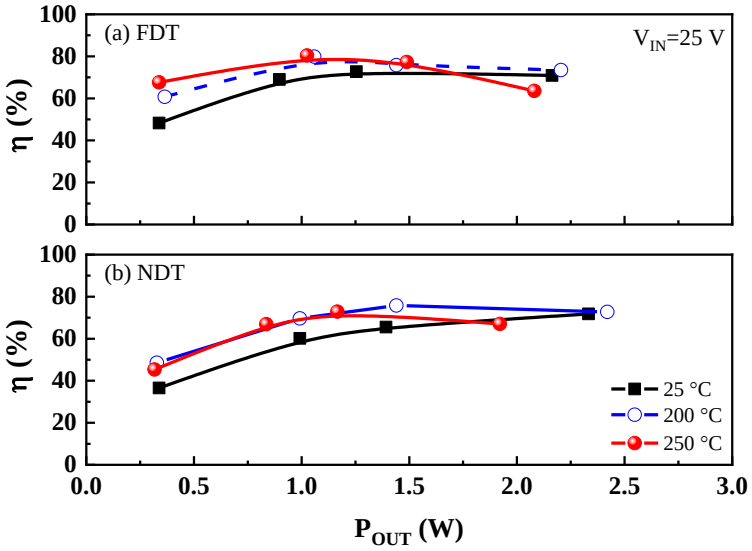


Fig.6.4.17 The efficiency of the optimized FDT converter (a) and the optimized NDT converter (b) in Table 6. 3. D=0.5, V_{IN}=25 V, T=25 °C, 200 °C, and 250 °C.

Fig.6.4.17 shows the high-temperature results of the optimized GaN converters in Table 6. 3. At 100 kHz, V_{IN}=25 V, the GaN FDT converter shows a slight increase of

efficiency at high temperatures, which might be caused by the reduced oscillations and overshoots at high temperatures. At 200 °C and 250 °C, the FDT and NDT converters show a comparable maximum efficiency of 80 % at low load currents. The high efficiency of the GaN converters validates the advantages of the recessed MIS-gate for HT power converters.

Fig.6.4.18 shows the efficiency of two optimized converters at large load currents with a temperature of 200 °C to investigate efficiency degradation at high temperatures, since R_{ON} increases and drain current decreases at high temperatures due to the degradation of the channel mobility [82]. At low load powers, both converters exhibit a maximum efficiency of 80% at 200 °C, indicating good performance of the recessed MIS-gate technology for power converters at high temperatures. The NDT converter without deadtime shows obvious efficiency advantages over the FDT converter at high temperatures, especially at high load powers. Given a fixed input voltage of 30 V, the FDT converter in Fig.6.4.18 (a) shows obvious efficiency degradation with increasing load powers. The efficiency of the FDT converter can decrease down to 54% with a load resistance of 25 Ω, however, the NDT converter in Fig.6.4.18 (b) shows slower degradation with load currents and exhibits an efficiency of 62% with the same load resistance of 25 Ω. Another obvious difference is the maximum load power of the optimized NDT converter is larger than that of the optimized FDT converter, especially at large load currents and high input voltages (V_{IN}=25 V, 30 V). Considering the same sizes of the power transistors in the two converters in Table 6. 3, the efficiency difference between them at high temperatures is related to the different topologies. With

a load resistance of 25 Ω at 30 V, the maximum power is 5.4 W for the optimized NDT converter in Fig.6.4.18 (b) and 3.7 W for the optimized FDT converter in Fig.6.4.18 (a). This might be caused by degraded output voltages of the FDT converter at large currents and high input voltages, and this will be analyzed in the following discussion.

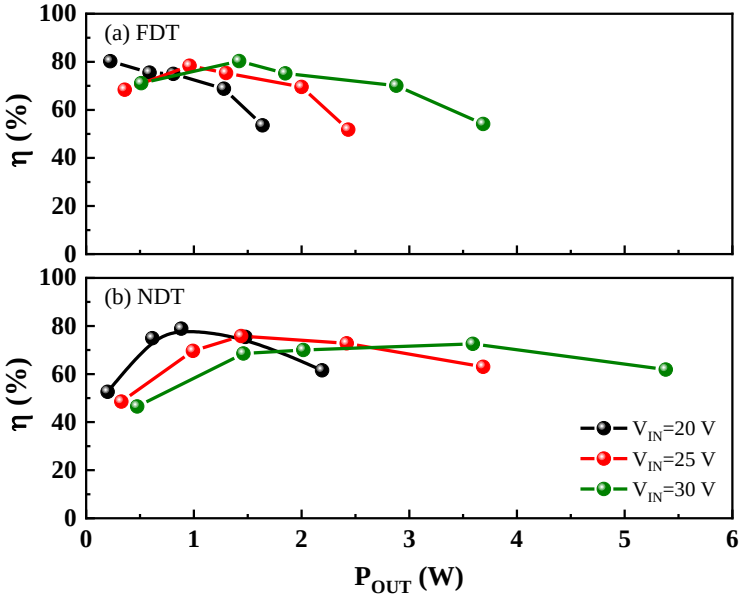


Fig.6.4.18 The efficiency of the optimized FDT converter (a) and the optimized NDT converter (b) in Table 6. 3. D= 0.5, T= 200 °C, V_{IN}=20 V, 25 V, and 30 V. R=500, 150, 100, 50, and 25 Ω.

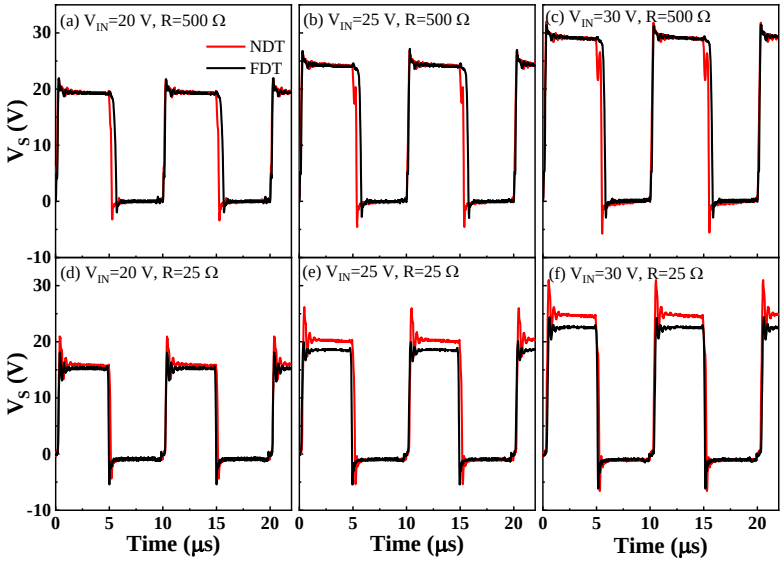


Fig.6.4.19 Comparison of dynamic V_S waveforms between the optimized FDT converter and NDT converter at various load conditions. D= 0.5, T= 200 °C.

To study the efficiency difference between the optimized FDT converter and NDT converter at high temperatures in Fig.6.4.18, Fig.6.4.19 gives a comparison of dynamic V_S waveforms at various load conditions at 200 °C. At a small load current with a load resistor of 500 Ω, the maximum voltage of stable V_S ($V_{S,Max}$) has no big difference between two converters at various input voltages. However, when the load resistor is 25 Ω, the $V_{S,\,Max}$ is higher in the optimized NDT converter than the optimized FDT converter, and the discrepancy increases with increasing input voltages. The higher $V_{S,Max}$ of the optimized NDT converter at large load currents might contribute to higher output voltages than the optimized FDT converter. This can explain the higher efficiency of the optimized NDT converter at large load currents in Fig.6.4.18, indicating a better performance of the NDT converter without deadtime than the FDT converter with a fixed deadtime at high temperatures.

The optimized NDT converter shows higher $V_{S,Max}$ at high load currents than the optimized FDT converter in Fig.6.4.19, and it can be explained in the following figures. At 200 °C, Fig.6.4.20 and Fig.6.4.21 show the gate driver signals of the optimized FDT converter and the optimized NDT converter at various load conditions, respectively. The optimized FDT converter in Fig.6.4.20 shows obvious gate overshoots at the switching-off transient of the high-side transistor, and the overshoots increase with increasing input voltages and load currents. The overshoots might be caused by the delay between switching node V_S and gate driver signal V_{G_H}, and this is attributed to the increased R_{ON} at large load currents and high temperatures as mentioned in the previous discussion. When the input voltage is 30 V with a load resistor of 25 Ω, the

overshoot is up to 21 V, which is detrimental to some Schottky gate GaN devices with a strict gate voltage limitation of 7 V [84]. Owing to the insertion of the high-k insulator Al_2O_3 in this work, the recessed E-mode MIS-gate can withstand a dynamic gate-to-source voltage of more than 20 V at high temperatures. However, the large gate overshoots can degrade the performance of the power transistors at high load currents. The dynamic R_{ON} increases with increasing gate voltages [159], and this can explain the lower $V_{S,Max}$ of the optimized FDT converter at large load currents at 200 °C in Fig.6.4.19. Fortunately, the optimized NDT converter with overlapping gate drivers shows small gate overshoots at various load conditions at 200 °C in Fig.6.4.21, indicating the advantages of small voltage overshoots of driver signals of the proposed NDT method for high-temperature power converters. The small voltage overshoots might be caused by the partial turn-on of the low-side transistor at the switching-off transient of the high-side transistor. This will accelerate the discharging process of the switching node V_S, and thus reduce the delay between V_{G_H} and V_S, resulting in smaller voltage overshoots in Fig. 6.4.21 at HTs. The delay of V_S is dependent on load conditions and increases with input voltages and load currents, since RC delay increases with increased R_{ON} owing to self-heating effects at high input voltages and load currents in the FDT converter in Fig. 6.4.20. The NDT converter with no deadtime can overcome this issue by the fast-switching transition of V_S through the low-side loop, resulting in small overshoots at various load conditions in Fig. 6.4.21.

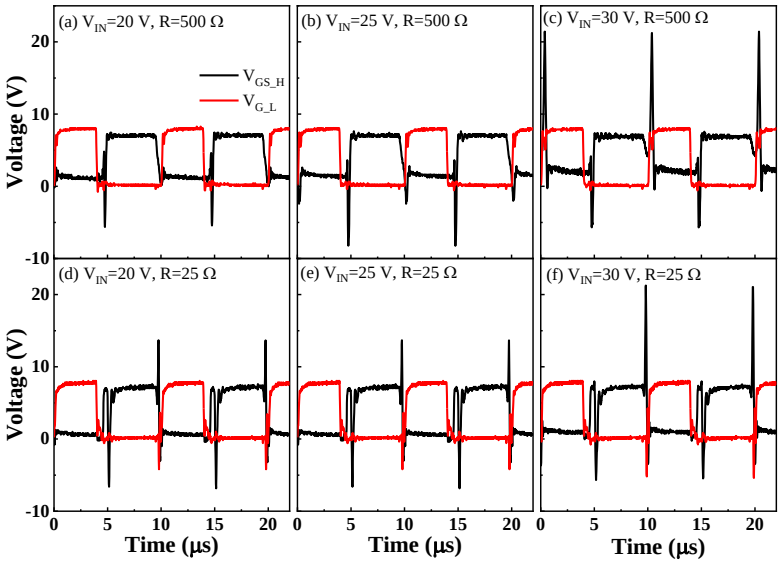


Fig.6.4.20 Gate driver signals of the optimized GaN FDT converter at various load conditions at 200 °C. f=100 kHz, D=0.5.

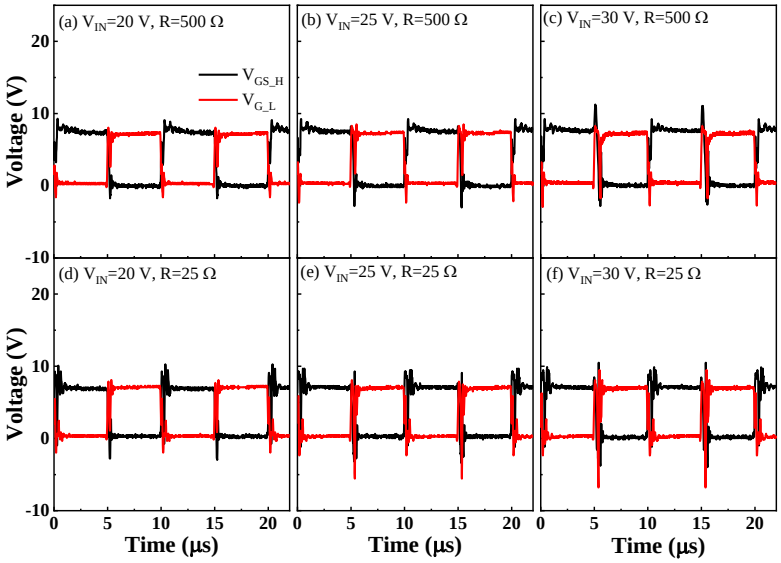


Fig.6.4.21 Gate driver signals of the optimized GaN NDT converter at various load conditions at 200 °C. f=100 kHz, D=0.5.

In this thesis, the large on-state resistance of the recessed technique has a great impact on the performance of GaN power converters. The power transistor conduction loss is mainly caused by on-state resistance R_{ON}. The conduction loss due to on-state resistance $P_{c,Ron}$ can be expressed as [53]:

$$P_{c,Ron} = (I_{load}^2 + \frac{1}{3}\Delta i_L^2)R_{ON} \quad (6.5)$$

Where I_{load} is the average load current, and $\triangle i_L$ is the inductor current ripple.

Fig. 6.4.22 shows the dynamic waveforms V_S and inductor current I_L of the optimized NDT converter. The maximum efficiency is around 80% with a load current of 0.094A, a load power of 0.88 W. The on-state resistance of the NDT converter is estimated as 8 Ω as the previous discussion. According to equation (6.5), the power conduction loss is calculated as 0.095 W and is 43% of the total power loss of 0.22 W. If the R_{ON} is improved and equal to 0.125 Ω using a P-GaN gate HEMT [84], here we take an approximation of the first order, the R_{ON} does not impact other power losses. The calculated power conduction loss is 0.001 W and is 8 % of the total power loss of 0.126 W, and the efficiency is improved to 87%.

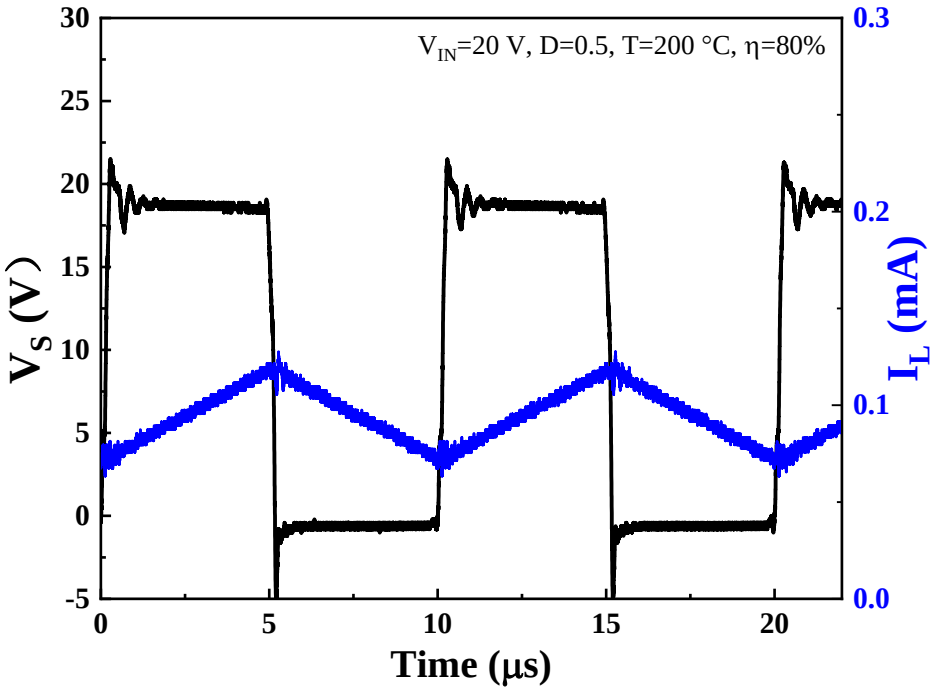


Fig. 6.4.22 Dynamic waveforms of the proposed GaN NDT converter of Fig. 6.4.18. V_{IN}=20 V, D=0.5, T=200 ºC, η=80%, I_{load}=0.094 A.

The increased R_{ON} by the recessed channel can increase conduction loss and reduce

the efficiency of GaN power converters, and the low mobility of the recessed channel can affect the frequency of power converters. The recessed technique often combines an insulator to improve gate leakage and enlarge gate swing. However, the insulator/GaN interface traps have threshold voltage stability issues and gate dielectric reliability issues, which are the main reasons why the commercialization of recessed E-mode devices has been much slower than the P-GaN power transistor. Surface treatment [160], the high-temperature insulator using low-pressure chemical vapor deposition (LPCVD) [161], and low-temperature interfacial layer [162] were reported to achieve low interface trap density. However, the high R_{ON} of 13.2 Ωmm and low mobility of 160 cm^2/Vs [162] are still not good enough for GaN power converter even though the interface density is as low as ~10^{11} to ~$10^{12} cm^{-2} eV^{-1}$.

The advanced high-temperature gate recess [107] was reported to improve the channel mobility up to 180 cm^2/Vs with a maximum drain current of 663 mA/mm. A self-terminated structure [105] was reported to recess the AlGaN barrier of the first channel, leaving a second channel to maintain high electron mobility of 1400 cm^2/Vs. So advanced techniques and structures are proposed in this thesis to improve the mobility and R_{ON} of the recessed channel.

6.5 Conclusion

Deadtime management is essential for power converters to avoid short circuit failure and reduce power loss during deadtimes. This chapter reports a simple method to eliminate deadtime, a no deadtime technique (NDT). The GaN integrated circuits (ICs)

simply use one pulse signal to generate two complementary signals with overlapping gate drivers to achieve no deadtime. The synchronous GaN NDT converter is compared to a fixed deadtime technique (FDT) GaN converter at various load conditions. The deadtime can cause serious voltage overshoots and oscillations of gate drivers in the FDT converters. The GaN NDT converter provides smaller gate voltage overshoots and oscillations owing to the absence of the deadtime, with a compromise of the maximum gate voltage of both high-side and low-side drivers. The smaller sizes of gate drivers give smaller voltage overshoots and oscillations, the optimized converters including NDT and FDT show an increased maximum efficiency of 80% owing to reduced overshoots and oscillations, even at high temperatures up to 250 °C. At high temperatures, the optimized NDT converter shows better efficiency at large load currents than the optimized FDT converter, owing to its good stability and small voltage overshoots of driver signals. The results in this chapter provide effective deadtime management for high-temperature power converters in electric vehicle applications where a high temperature above 200 °C is required.

Chapter 7 Conclusion and future work

7.1 Conclusion

Power integration is essential to fully utilize the advantages of GaN technologies, especially at high temperatures over 200 °C for electrical vehicle applications. This dissertation focuses on GaN IC for high-temperature (HT) power converters without external heatsink or cooling systems, and the results validate the advantage of all GaN for HT power converters in electric vehicle applications. The thesis includes four main parts: the impact of etch depth of AlGaN barrier on the performance of GaN devices and circuits; an integrated gate driver for a GaN boost converter; integrated gate drivers with a half-bridge stage for synchronous GaN buck converters; an integrated technique of deadtime management for synchronous GaN buck converters.

To evaluate the recessed MIS-gate for HT GaN power converters, the impact of etch depth of the AlGaN barrier on the performance of GaN-based devices and circuits is systematically studied at various temperatures. The scattering mechanisms under different etch depths are investigated, the experimental results fit well with theoretical calculation, indicating good models of scattering mechanisms under different etch depths. When the etch depth D_{etch} is less than 20 nm, polar-optical-phonon scattering dominates owing to 2DEG channel by the polarization electric field; when D_{etch} is between 20 and 25 nm, the acoustic phonon scattering dominates and starts to play an important role. The interface traps induced Columb scattering starts to affect the

channel mobility when D_{etch} is larger than 25 nm. For recessed E-mode devices, the low channel mobility is mainly caused by Columb scattering and acoustic scattering, which emphasizes the importance of improving the interface quality of the recessed MIS-gate. Full recess and interface engineering are recommended in this thesis to improve the stability of E-mode devices and GaN circuits.

The design of GaN-based HT gate drivers is a preliminary effort for HT GaN DC-DC converters. Different designs of gate drivers are evaluated at various temperatures, a small size of driver can lead to a slow switching speed, while a large size can cause large voltage overshoots and oscillations. A careful design should be made to balance the switching speed and overshoots. The fabricated GaN boost converter with the optimized gate driver exhibits good performance (V_{IN}/V_{OUT}=5 V/11 V at 100 kHz) at high temperatures up to 250 °C, owing to fast switching speed and small voltage oscillations. The results validate the advantages of recessed E-mode MIS-HFETs for the implementation of HT gate drivers for GaN converters under extreme environments. However, the recess-induced R_{ON} influences the converter performance at a high frequency up to 1 MHz, the reduced output voltage is observed with increasing operating frequency due to a 0.43 μs turn-on delay by the increased R_{ON}.

Half-bridge is an important topology in power converters, the GaN converter with a half-bridge stage has unique advantages of reduced chip size and high efficiency, owing to smaller on-state resistance of GaN transistors than the diode-mode converter. This thesis demonstrates a synchronous GaN DC-DC buck converter with an integrated half-bridge stage and gate drivers. The synchronous GaN buck converter can achieve a voltage

down conversion with an input voltage of 25 V, and exhibits excellent thermal stability at temperatures up to 250 °C. It shows better performance than the asynchronous GaN converter at various temperatures, duty cycles, and input voltage owing to the fast switching transition of the half-bridge topology. Large voltage overshoots and oscillations are observed in the GaN converters with external gate drivers, and these can affect and even deform the dynamic waveforms of the converters at low duty cycles and a high input voltage. These results emphasize the importance of all GaN ICs on a single chip in achieving high temperature, high power density, and high-efficiency power converters.

Deadtime management is essential for power converters to avoid short circuit failure and reduce power loss during deadtimes. This thesis presents a simple method and requires one control signal to eliminate deadtime using overlapping gate drivers, a no deadtime technique (NDT). The proposed GaN NDT converter shows smaller voltage overshoots and oscillations of gate drivers than the integrated GaN converter with a fixed deadtime technique (FDT). The large overshoots and oscillations degrade and even disable the performance of the GaN FDT converter at a high duty cycle of 0.8. The smaller sizes of gate drivers give smaller voltage overshoots and oscillations, and thus lead to an increased efficiency with a maximum efficiency of 80 % at 250 °C. At high temperatures with a large load current, the optimized GaN FDT converter shows large overshoots at the switching-off transition of the high-side gate driver due to temperature-induced R_{ON}, while the optimized GaN NDT shows smaller gate overshoots at various load conditions owing to the fast transition speed of the switching node V_S. This

consequently outstands the better efficiency and load powers of the optimized GaN NDT converter over the optimized GaN FDT converter at high temperatures. The results in this thesis provide effective deadtime management for high-temperature power converters.

7.2 Suggestions for future work

Based on the contributions and findings in this thesis, some suggestions about future work are listed as follows:

(1) Limited models have been reported for GaN simulation on a circuit level so far, especially for HT GaN IC. A more accurate GaN model is required to match the experimental results with simulations. Firstly the optimized model needs to reflect the transient behavior of discrete GaN devices, like transient V_{th}, dynamic R_{ON}, etc. This helps to simulate GaN ICs and thus GaN converters in a time domain. Then, the device model should include the thermal behavior at high temperatures, and it is essential to understand the HT characteristics of the GaN converters, and this helps guide the design of GaN ICs for HT power converters as well.

(2) To improve the frequency and efficiency of the GaN converters with a recessed MIS gate, efforts have to be made to provide a high-quality gate dielectric. This helps improve the R_{ON} performance of E-mode devices and the thermal stability of GaN MIS-HEMTs and MIS-HFETs. This is essential to enable MIS GaN IC to make significant progress in HT power converters. The recessed MIS-gate

technique is a simple process and compatible with CMOS process, so it is cost effective. The MIS-gate transistors are especially attractive in high-frequency and high-temperature power switching applications owing to strong noise immunity and reduced leakage current. However, the dielectric/III-nitride interface traps and dielectric body traps present the biggest challenges to GaN MIS-HEMTs and MIS-HFETs. Great efforts have to be made to overcome the gate dielectric reliability issue before the commercialization of E-mode GaN-based MIS-HFETs.

(3) An accurate and theoretical calculation is required to explain the negative shift of V_{IH}, V_{IL} with increasing temperatures in GaN DCFL inverters, and a negative value of V_{IL} as well.

(4) An accurate calculation is required to identify the contribution of each component to the total R_{ON} at various temperatures, including contact resistance R_C, sheet resistance in access regiongs R_{sg} and R_{gd}, and recessed channel resistance R_{ch}. This can give a clear image of the resistance distribution at various temperatures and provides guidance how to improve R_{ON} of transistors in HT converters.

(5) Accurate power loss models are required to further understand the power loss mechanisms of the integrated GaN power converter, especially at high temperatures.

Appendix A

The rise and fall time are derived based on an nMOSFET inverter consisting of an enhancement-mode nMOS driver and a depletion-mode nMOS load. As the first order of magnitude approximation, the drain current formula of a silicon nMOSFET is employed. The current-voltage equations to be used for the depletion-mode load transistor are identical to those of the enhancement-mode device, with the exception of the sign of threshold voltages [133]. At room temperature, the current-voltage equations of an enhancement nMOSFET can be expressed as:

$$I_D(\text{lin}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS}-V_{th})V_{DS}-V_{DS}^2\right] \qquad V_{GS}>V_{th},\ V_{DS}<V_{GS}-V_{th} \qquad \text{(A.1)}$$

$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{th})^2 \qquad V_{GS}>V_{th},\ V_{DS}>V_{GS}-V_{th} \qquad \text{(A.2)}$$

C_{ox} of D-mode Al_2O_3/AlGaN/GaN MIS-HEMTs should be replaced by C_{ob} due to the contribution of AlGaN barrier to gate capacitance [130]. C_{ox} is the oxide capacitance, C_{br} is the barrier capacitance and $C_{ob} = (C_{ox}^{-1} + C_{br}^{-1})^{-1}$. The gate capacitance of the E-mode Al_2O_3/GaN MIS-HFETs is only determined by C_{ox} due to the absence of the barrier layer.

Four different drivers can be classified into two types, DCFL inverters without (w/o) buffer and DCFL inverters with buffer. Assume that all D-mode and E-mode devices have the same threshold voltages $V_{th,D}$ and $V_{th,E}$, respectively. The diagrams of DCFL inverters w/o buffer are shown in Fig.A.1.

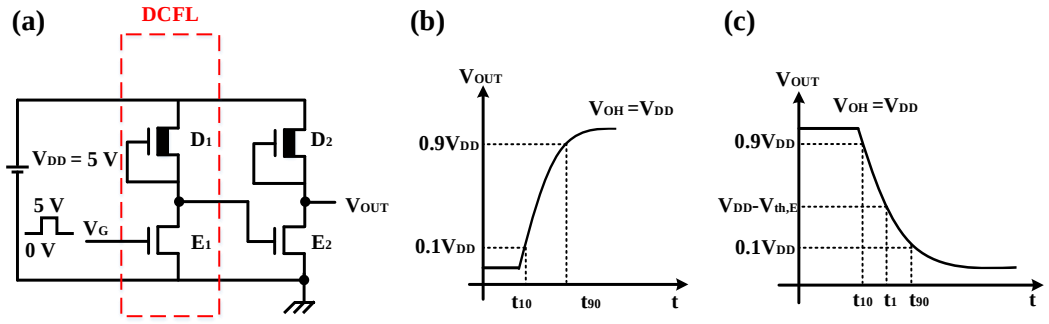


Fig.A.1 (a) The circuit diagram of a gate driver with DCFL inverters w/o buffer (No. 2). The diagrams of rise time (b) and fall time (c).

Fig.A.1(b) shows the diagram of the rise time. E_2 device operates in off-state and flows negligible current, V_{DD} is charging output through D_2. For D_2 device, $V_{OUT}=V_{DD}-V_{DS}$, $V_{GS}=0$ V, $V_{DS} < V_{GS} - V_{th} = 0-(-8) = 8V$. So D_2 device always operates in linear region during the rise time (0.1 V_{OH} to 0.9 V_{OH}).

$$\mathrm{dt} = -\frac{C_L}{i_{ds}(t)} dV_{out}$$

$$\int_{t_{10}}^{t_{90}} dt = -\int_{0.1V_{DD}}^{0.9V_{DD}} \frac{2C_L}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D \frac{dV_{out}}{\left[2(V_{GS}-V_{th})V_{DS}-V_{DS}^2\right]}$$

$$\tau_{rise} = \frac{C_L}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D \frac{1}{(V_{GS}-V_{th,D})} \left[\ln\left(\frac{7.2V_{DD}}{2(V_{GS}-V_{th,D})-0.9V_{DD}}+9\right)\right]$$

So the rise time of DCFL inverters w/o buffer can be expressed by:

$$\tau_{rise} = t_{10-90} = \frac{C_L}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D f\left(V_{DD}, V_{T,D}\right) \tag{A.3}$$

$$f\left(V_{DD}, V_{\mathrm{th},D}\right) = \frac{1}{|V_{th,D}|}\left[\ln\left(\frac{7.2V_{DD}}{2|V_{th,D}|-0.9V_{DD}}+9\right)\right].$$

Fig.A.1 (c) shows the diagram of fall time. D_2 device operates in the linear region; note that here we do not consider the small current of D_2 device during fall time. The output is discharging through E_2. For E_2 device, $V_{OUT}=V_{DS}$, $V_{GS} \approx V_{DD}$. When $V_{OUT}<V_{DD}-V_{th,E}$, E_2 device operates in the linear region, while when $V_{OUT} > V_{DD}-V_{th}$, E_2 device

operates in the saturation region. Fall time (0.9 V_{OH} to 0.1 V_{OH}) can be obtained by the following formulas:

$$\mathrm{dt} = -\frac{C_L}{i_{ds}(t)} dV_{out}$$

$$t_{90-1} = \int_{t_{90}}^{t_1} dt = -\int_{0.9V_{DD}}^{V_{DD}-V_{th,E}} \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \frac{dV_{out}}{\left(V_{GS}-V_{th,E}\right)^2}$$

$$t_{90-1} = \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \frac{\left(V_{th,E}-0.1V_{DD}\right)}{\left(V_{DD}-V_{th,E}\right)^2}$$

and,

$$t_{1-10} = \int_{t_1}^{t_{10}} dt = -\frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \int_{V_{DD}-V_{th,E}}^{0.1V_{DD}} \frac{dV_{out}}{\left[2\left(V_{GS}-V_{th,E}\right)V_{DS}-{V_{DS}}^2\right]}$$

$$t_{1-10} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \frac{1}{(V_{DD}-V_{th,E})} \left[\ln\left(\frac{2(V_{DD}-V_{th,E})-0.1V_{DD}}{0.1V_{DD}}\right)\right].$$

So the total fall time of DCFL inverters w/o buffer can be expressed as:

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \frac{1}{(V_{DD}-V_{th,E})} \left\{\frac{2\left(V_{th,E}-0.1V_{DD}\right)}{(V_{DD}-V_{th,E})} + \ln\left(\frac{2(V_{DD}-V_{th,E})-0.1V_{DD}}{0.1V_{DD}}\right)\right\}$$

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E g(V_{DD}, V_{th,E}) \qquad \text{(A.4)}$$

$$g(V_{DD}, V_{th,E}) = \frac{1}{(V_{DD}-V_{th,E})} \left\{\frac{2\left(V_{th,E}-0.1V_{DD}\right)}{(V_{DD}-V_{th,E})} + \ln\left(\frac{2(V_{DD}-V_{th,E})-0.1V_{DD}}{0.1V_{DD}}\right)\right\}.$$

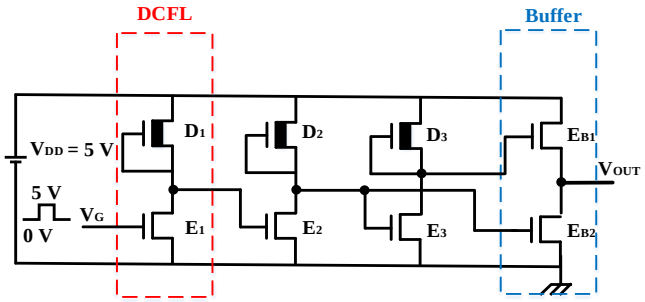


Fig.A.2 The circuit diagram of a gate driver with DCFL inverters with buffer (No. 3).

Fig.A.2 shows the circuit diagram of a gate driver with DCFL inverters with buffer

stage. According to the diagram of rise time in Fig.A.1 (b) shows the diagram of rise time. Assuming that E_{B2} flows negligible current and operates in pinch-off region, V_{DD} is charging output through E_{B1}. For E_{B1}, V_{th}>0 V, $V_G \approx V_{DD}$, V_{GS}-V_{th}=V_{DD}-V_{OUT}-V_{th}. So V_{DS}=V_{DD}-V_{OUT}>V_{GS}-V_{th}, so E_{B1} operates in saturation region during rise time (0.1 V_{OH} to 0.9 V_{OH}). Hence,

$$\mathrm{dt} = -\frac{C_L}{i_{ds}(t)} dV_{out}$$

$$t_{10-90} = \int_{t_{10}}^{t_{90}} dt = -\int_{0.1V_{DD}}^{0.9V_{DD}} \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB1} \frac{dV_{out}}{\left(V_{GS} - V_{th,E}\right)^2}$$

$$t_{10-90} = \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB1} \frac{V_{DD} - 2V_{th,E}}{\left|0.1V_{DD} - V_{th,E}\right|\left(0.9V_{DD} - V_{th,E}\right)}.$$

So the rise time of DCFL inverters with buffer stage can be expressed as:

$$\tau_{rise} = \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB1} F\left(V_{DD}, V_{th,E}\right) \tag{A.5}$$

$$F\left(V_{DD}, V_{th,E}\right) = \frac{V_{DD} - 2V_{th,E}}{\left|0.1V_{DD} - V_{th,E}\right|\left(0.9V_{DD} - V_{th,E}\right)}.$$

Following the similar discussion of fall time in Fig.A.1 (c), the output is discharging through E_{B2} and the fall time of DCFL inverters with buffer stage can be expressed by:

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB2} g(V_{DD}, V_{th,E}) \tag{A.6}$$

$$g(V_{DD}, V_{th,E}) = \frac{1}{(V_{DD} - V_{th,E})} \left\{ \frac{2\left(V_{th,E} - 0.1V_{DD}\right)}{(V_{DD} - V_{th,E})} + \ln\left(\frac{2(V_{DD} - V_{th,E}) - 0.1V_{DD}}{0.1V_{DD}} \right) \right\}.$$

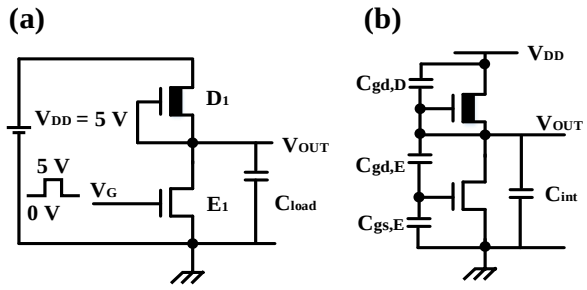


Fig.A.3 (a) Circuit diagram of a DCFL inverter, and (b) parasitic device capacitances. $C_{gd,D}$ is the gate-to-drain capacitance of D-mode devices, $C_{gd,E}$ is the gate-to-drain capacitance of E-mode devices, $C_{gs,E}$ is the gate-to-source capacitance of E-mode devices, and C_{int} is the interconnect capacitance.

Fig.A.3 shows the capacitance of a single DCFL inverter, C_L or C_{load} consists of intrinsic and extrinsic capacitances. C_{int} is the interconnect capacitance. Note that since GaN transistors do not have gate overlap capacitances unlike Si-MOSFETs, we only consider oxide capacitances over the gate area:

$$C_L = C_{gd,D} + C_{gd,E} + C_{gs,E} + C_{int}$$

$$C_L = C_{ob} W_D L_D + C_{ox} W_E L_E + C_{int}$$

We assume that $C_{int} \leq C_g$, so the load capacitance is mainly dominated by gate capacitances and normally $C_{gs} > C_{gd}$, so gate-source capacitance C_{gs} dominates gate capacitance [98].

During rise time, the E-mode transistor is in off-state, V_{DD} is charging C_L through the D-mode device, so the impact of $C_{ox}W_EL_E$ on the τ_{rise} can be ignored, $C_{gs} \approx 0$ F due to gate-source connection, so C_L is dominated by C_{int} during rise time, and equation (A.3) can be simplified as:

$$\tau_{rise} \propto \frac{C_{int}}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D f(V_{DD}, V_{th,D}) . \qquad (A.7)$$

During fall time, C_L is discharging mainly from the E-mode device, so $C_{gs,E}$

dominates the gate capacitance. Thus formula (A.4) for fall time can be simplified as:

$$\tau_{fall} \propto \frac{C_{ox} W_E L_E}{\mu_E C_{ox}} \left(\frac{L}{W} \right)_E g(V_{DD}, V_{th,E})$$

$$\tau_{fall} \propto \frac{L^2}{\mu_E} g(V_{DD}, V_{th,E}). \tag{A.8}$$

Similarly, we take the first order of magnitude approximation for DCFL inverters with the buffer stage, considering the width of the buffer stage to be larger than the width of inverters. So formulas (A.5) and (A.6) can be simplified as (A.9) and (A.8), respectively:

$$\tau_{rise} \propto \frac{2L^2}{\mu_E} F\left(V_{DD}, V_{th,E}\right). \tag{A.9}$$

Here, $f(V_{DD,} V_{th,D})$, $g(V_{DD,} V_{th,E})$, and $F(V_{DD,} V_{th,E})$ are size-independent functions.

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Papers, 2016.

Appendix B Publication List

Journal Papers:

[1] Miao Cui, Ang Li, Qinglei Bu, Ivona Z. Mitrovic, Huiqing Wen, Wen Liu, and Cezhou Zhao, "A Monolithic GaN No Deadtime Technique (NDT) for High-Temperature (HT) DC-DC Buck Converters", ***IEEE Journal of Emerging and Selected Topic in Power Electronics***, 2021, (under review).

[2] "Characterization and Modeling of Channel Mobility with Different Etch Depths in GaN-based D-mode MIS-HEMTs and E-mode MIS-HFETs", ***Journal of Applied Physics***, 2021, (to be submitted).

[3] **Miao Cui***, Ruize Sun*, Qinglei Bu, Wen Liu, Huiqing Wen, Ang Li, Yung C. Liang, Cezhou Zhao. "Monolithic GaN Half-Bridge Stages with Integrated Gate Drivers for High Temperature DC-DC Buck Converters," ***IEEE Access***, vol. 7, p. 184375, 2019. (*Co-first author)

[4] **Miao Cui**, Qinglei Bu, Yutao Cai, Ruize Sun, Wen Liu, Huiqing Wen, Sang Lam, Yung C. Liang, Ivona Z. Mitrovic, Stephen Taylor, Paul R. Chalker, Cezhou Zhao. "Monolithic integration design of GaN-based power chip including gate driver for high-temperature DC-DC converters," ***Japanese Journal of Applied Physics***, vol. 58, no. 5, p. 056505, 2019.

Conference Papers:

[4] **Miao Cui**, Qinglei Bu, Yutao Cai, Ruize Sun, Wen Liu, Huiqing Wen, Sang Lam, Yung C. Liang, Ivona Z. Mitrovic, Stephen Taylor, Paul R. Chalker, Cezhou Zhao.

"AlGaN/GaN Metal-Insulator-Semiconductor (MIS)-HFETs based DC-DC Boost Converter with Integrated Gate Driver," ***10th International Conference on Power Electronics and ECCE Asia (ICPE 2019-ECCE Asia)***, 27th-30th, May, Busan, Korea, 2019.

[5] **Miao Cui**, Yutao Cai, Qinglei Bu, Wen Liu, Huiqing Wen, Ivona Z. Mitrovic, Stephen Talyor, Paul R. Chalker, Cezhou Zhao. "The Impact of Etch Depth of D-mode AlGaN/GaN MIS-HEMTs on DC and AC Characteristics of 10 V Input Direct-Coupled FET Logic (DCFL) Inverters," ***2019 International Conference on IC Design and Technology (ICICDT)***, 17th-19th, June, Suzhou, China, 2019.

Co-authored journal papers:

[6] Y. Cai, W. Liu, **M. Cui**, R. Sun, Y. C. Liang, H. Wen, L. Yang, S. N. Supardan, I. Z. Mitrovic, S. Taylor, P. R. Chalker, and C. Zhao. "Effect of Surface Treatment on Electrical Properties of GaN Metal-Insulator-Semiconductor Devices with Al2O3 Gate Dielectric," ***Japanese Journal of Applied Physics***, vol. 59, no.4, pp. 041001, 2020.

Co-authored conference papers:

[7] Xueteng Li, **Miao Cui**, Wen Liu, "A full GaN-integrated Sawtooth Generator based on Enhancement-mode AlGaN/GaN MIS-HEMT for GaN Power Converters". ***2019 International Conference on IC Design and Technology (ICICDT)***, 17th-19th, June, Suzhou, China, 2019.

[8] Bohan Lu, **Miao Cui**, Wen Liu, "The Impact of AlGaN Barrier on Transient Vth Shifts and Vth Hysteresis in Depletion and Enhancement mode AlGaN/GaN MIS-HEMTs". ***2019 International Conference on IC Design and Technology (ICICDT)***, 17th-19th, June, Suzhou, China, 2019.

[9] Y. Cai, Y. Wang, **M. Cui**, W. Liu, H. Wen, C. Zhao, I. Z. Mitrovic, S. Talyor, and P. R. Chalker, "Effect of High-k Passivation Layer on Electrical Properties of GaN Metal-Insulator-Semiconductor Devices," ***2019 International Conference on IC Design and Technology (ICICDT)***, 17th-19th, June, Suzhou, China, 2019.