A Sodium Fluoride Doping Approach to CdTe Solar Cells

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Abstract

Sodium is a common impurity in CdTe solar cells, yet there are relatively few reports investigating its effect on complete device structures. There is the potential for uncontrolled sodium incorporation, either from impurities in the CdTe material itself or contaminants introduced during device processing, which can affect the optoelectronic properties of CdTe. Therefore, it is important to consider the impact of sodium incorporation on device performance. In this work, we show that the deposition of a thin layer of NaF at the back surface of CdS/CdTe devices prior to metallisation is an effective strategy to form a highly doped back surface and improve contact quality. High temperature (~300°C) annealing is required to effectively incorporate sodium throughout the device and improve the bulk doping density, however this also leads to sodium accumulation in the CdS layer and the formation of a TeO_2 layer at the back surface. We also find evidence of out-diffusion of sodium from commonly used TEC glass substrates at typical CdTe processing temperatures, despite the presence of an alkali diffusion barrier layer. Understanding this prevalent sodium diffusion in this class of solar cells is vital for further improvement of CdTe structures.

Keywords: CdTe, Solar Cells, Sodium, Doping, NaF

1. Introduction

Cadmium telluride (CdTe) solar cells have reached a record efficiency of 22.1%, with recent gains mainly resulting from increases in short circuit current density (J_{sc}) [1]. The open circuit voltage (V_{oc}) of record devices remains around ~850 mV, with little improvement in the past 20 years. These record devices have historically relied on depositing a thin (~1 nm) layer of copper at the back surface prior to metallization [2, 3] to both dope the bulk CdTe layer and form a p^+ region at the back surface to facilitate a quasi-ohmic contact. To further improve efficiencies, there has been a shift of research focus away from using copper doping due to strong self-compensation effects which limit hole densities to around 10^{15} cm^{-3}, and fast diffusivity which causes long term stability concerns [3, 4]. Much of this research has focused on Cd rich growth and doping on the Te site using Group V elements. Phosphorous and arsenic have been effective in achieving high doping densities ($>10^{16}$ cm^{-3}) with long carrier lifetimes in single crystal CdTe due to high activation ratios despite self compensation by AX centres [5, 6], and more recent efforts have achieved similar doping densities in polycrystalline devices [7, 8].

Whilst Group V doping has shown promise, there has been comparatively few reports of the effects of Group 1A alkali metals on CdTe device performance. An understanding of the effect of sodium is especially relevant from a CdTe module manufacturing perspective, since soda lime glass substrates are typically used to lower

production costs. These substrates contain around 16% Na_2O [9] which can diffuse through to subsequently deposited adjacent layers. Although alkali barriers such as SiO_2 are typically used to prevent this [10], they are not fully effective and diffusion of sodium has been measured despite their presence, especially at high temperatures such as those seen during typical CdTe deposition processes [11]. Therefore, it is vital to understand the effect sodium has on device performance.

Substitution of Na onto Cd sites results in *p*-type doping with an acceptor level 59 meV above the valence band, which is more favourable for achieving high doping densities compared to 160 meV in the case for copper [12]. Although interstitial incorporation of sodium would cause compensation and potentially limit the ability to dope highly *p*-type, this donor level is similarly close to the conduction band, and is therefore not likely to be a lifetime limiting defect [12]. The doping efficacy of sodium has been demonstrated in single crystal CdTe devices, where a doping density of 7×10^{15} cm $^{-3}$ enabled a V_{oc} of 929 mV [13]. However, incorporating sodium into polycrystalline films has had mixed success, with efforts focused on combining the chloride treatment and doping process. Whilst an increased doping density was measured to $\sim 10^{15}$ cm $^{-3}$ upon sodium inclusion, this also has deleterious effects on film morphology. This includes agglomeration of CdS window layer leading to a poor diode response, and widening of CdTe grain boundaries thereby shorting contacts, which has so far limited study at a device level [14–18].

Here we report on the incorporation of sodium into CdS/CdTe devices by thermally evaporating a thin layer of NaF prior to contacting. By depositing NaF after the chloride treatment, the excessive recrystallisation which has been problematic in previously reported attempts is avoided [14–18]. In this work, this has improved the back contact as shown by the absence of 'rollover' in current density - voltage (JV) curves, implying a more highly doped region localised at the back surface. Annealing these devices in air at temperatures greater than 300°C causes sodium to diffuse into the bulk CdTe region, whereby a small increase in acceptor concentration is measured.

2. Experimental Methods

Devices were fabricated on TEC 15M commercial soda-lime glass substrates which are coated by the manufacturer with an alkali blocking layer, as well as SnO_2:F (FTO) which acts as a transparent front contact, and a nominally undoped SnO_2 buffer layer. After cleaning, 100 nm CdS was deposited via sputtering at a power density of 0.32 W cm^{-2} in 5 mTorr of Ar at a substrate temperature of 200°C. CdTe was then deposited by close spaced sublimation (CSS), with a source and substrate temperature of 610°C and 510°C respectively. This is performed in a two step process, with the main deposition occurring under 30 Torr nitrogen yielding a thickness of 4 - 5 μm after 25 min, followed by a short 30 s deposition under vacuum in order to encourage nucleation and fill any pinholes. Samples were etched in a dilute nitric-phosphoric acid (NP etch) for 30 s prior to $MgCl_2$ treatment at 410°C in air [19]. A second NP etch was then performed for 15 s before rinsing in deionised water. For samples which included an NaF layer, this was deposited by thermal evaporation, with thickness monitored by a quartz crystal microbalance. Copper was intentionally omitted from the device structure to minimise the number of variables under study and hence we anticipate a lower overall cell performance, yet this allows for a clearer comparison of devices. Devices which were subject to annealing were placed onto a pre-heated hotplate in air for 20min before

being removed and allowed to cool to room temperature. A 50 nm Au back contact was then thermally evaporated through a mask to define nine 0.25 cm^2 contacts per device. Front contacts are made by mechanically scraping the CdTe layer, and removing CdS with HCl to expose the underlying FTO front contact.

Test structures to examine out-diffusion of sodium from soda-lime glass substrates were fabricated by depositing CdTe directly onto cleaned TEC 15M substrates. The growth rate was controlled by varying the nitrogen pressure in the CSS chamber between 5 - 400 Torr, with higher pressures acting to reduce the Cd and Te partial pressures and therefore slow the growth rate [20]. This resulted in growth times between 4 - 262 min to deposit a 7 μm CdTe layer, during which time the substrate temperature was maintained at 550°C.

JV measurements taken with a Keithley 2400 source meter and TS Space Systems solar simulator (class AAA) calibrated to AM1.5G spectrum at 1000 W m^{-1}. EQE measurements were taken using a Bentham PVE300 characterisation system. Capacitance - voltage (CV) measurements were taken in the dark using a Solartron SI1260 impedance analyser with an AC perturbation amplitude of 30 mV and frequency of 100 kHz, and varying DC bias between -0.5 to +0.5 V. Secondary ion mass spectroscopy (SIMS) was used to obtain elemental depth profiles. An ION-TOF ToF-SIMS V instrument was used for time of flight SIMS measurements of NaF treated CdTe devices, and compared to ion implanted reference samples to quantify elemental concentrations of sodium, fluorine and chlorine. The depth profiling beam was 1 keV Cs^+ operated with a raster size of 200 μm^2. Qualitative SIMS measurements of sodium diffusion from TEC glass substrates into CdTe films were performed using a Hiden Analytical gas ion gun and quadrupole detector. A beam of O^{2-} ions rastered over a 500 × 500 μm^2 area (with an 11% gating to reject side wall effects) was used to sputter the sample using a beam energy of 5 keV at a current of 300 nA.

SEM images showing the back surface of sample were obtained using a JEOL7001F electron microscope, whilst cross-sections were prepared via focused ion beam milling using a FEI Helios Nano Lab 600 Dual Beam system, equipped with a focused 30 keV Ga liquid metal ion source. XPS was used to investigate the surface chemical composition using an Al Kα x-ray source (hν = 1486.6 eV) operating at 200 W and a hemispherical Scienta SES200 electron energy analyser comprised of a double channel plate and phosphor screen with a CCD camera. The resolution was determined to be 0.7 eV, allowing binding energy determination with a precision of ±0.1 eV, by fitting the Fermi edge of a reference Ag sample. Core level spectra were fitted with a Gaussian/Lorentzian product function to approximate a Voigt function after removal of a Shirley background.

3. Results and Discussion

3.1. NaF post deposition treatment

A series of 8 CdS/CdTe devices were initially fabricated in an identical manner to each other. Following $MgCl_2$ treatment and NP etching, 1 nm NaF was evaporated onto the back surface of 7 of these devices, and either left unannealed, or annealed on a hotplate for 20 mins in air at temperatures between 100°C and 350°C before contacting with Au. The remaining device was left without any NaF layer or anneal to serve as a reference for comparison. The 1nm NaF thickness was chosen based on preliminary experiments (Figures S1 and S2). This contacting process, whereby a few nm of a *p*-type dopant is evaporated onto the back surface prior to annealing in air, matches closely to that of typical copper-contacted CdTe solar cells [21][22].

Figure 1 shows JV curves from the highest efficiency cell of each of these devices subject to different anneal conditions compared to a control device without NaF. There is little difference between the shape of curves corresponding to the NaF treated devices, although the device annealed at 350°C shows noticeably poorer performance. Since it is difficult to observe trends directly from these JV curves, a more detailed discussion of the effect of anneal temperature on device performance is deferred to Figure 2. However, there are some obvious differences in the shape of JV curves with and without NaF treatment, irrespective of the annealing temperature. Most notably, there is a striking difference between the shape of the curves in forward bias. The control device shows rollover above V_{oc}, which is characteristic of a secondary barrier at the back contact, and is typical for a simple CdTe/Au contact structure [23]. In contrast, all devices with NaF applied at the back contact do not show such behaviour regardless of whether they are annealed or not, which suggests these devices have a reduced Schottky barrier. There is also a lower series resistance for NaF treated devices which can be observed from a steeper gradient around V_{oc} leading to an improved fill factor which is consistent with a lower contact barrier.

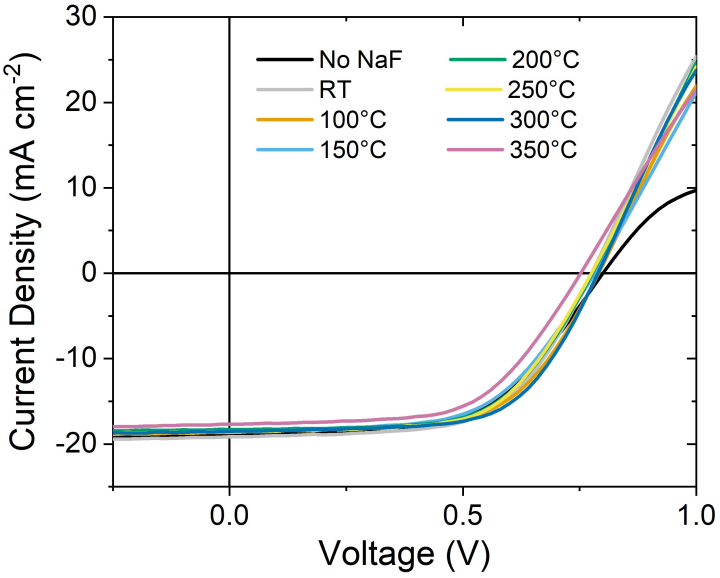

Figure 1: JV curves for the highest efficiency cell from devices with 1 nm NaF deposited prior to contacting and either left unannealed (RT), or annealed in air for 20 min at temperatures up to 350°C, compared to a device without NaF

This improvement in contacting is attributed to a highly doped back surface which results in a narrower barrier through which carriers can tunnel through to be extracted. In this case, it is unsurprising that the doping of the back contact is less dependent on anneal temperature since it is not necessary to redistribute the sodium into the bulk of the device at an elevated temperature, whilst the Te rich region formed at the back surface during etching means there are plenty of available Cd site to form Na_{Cd} acceptors. A similar strategy is commonly employed for copper doping in CdTe, whereby the back contact region is highly doped to form a p^+ region to assist the formation of an ohmic contact [2]. Replacing copper at the back contact with a different p-type dopant such as sodium is highly desirable, since copper can also incorporate on interstitial sites and form deep level defects in CdTe which are detrimental to device performance, and also cause long-term stability issues [4, 24]. On the other hand, DFT calculations suggest the interstitial sodium defect level is much shallower, albeit similarly acting as a donor [12]. Therefore, whilst Na_i defects are ideally avoided entirely since they compensate p-type doping, they

are not expected to act as strong recombination centres and so will be less harmful. The reduced rollover shown in Figure 1 following NaF treatment is therefore encouraging as this shows potential as a copper-free contact to CdTe. There are indications from literature reports that the presence of sodium in a CdTe device structure may pose long-term stability issues [13, 25], although preliminary tests show no accelerated degradation relative to NaF-free reference devices (Figure S3).

Figure 2 shows the average performance parameters as well as those of the highest efficiency cell for devices with 1 nm NaF as a function of annealing temperature compared to a control device without NaF. For all devices with NaF there is a decrease in both the average and peak V_{oc} and J_{sc} with increasing annealing temperature. However, there does appear to be a small reversal of this trend around 300 °C that is especially visible in the highest efficiency cell series. In contrast, the fill factor tends to be increased for those devices containing NaF. This can mainly be attributed to a reduction in the series resistance of devices with NaF compared to the control device. This is most apparent for the un-annealed device but is evident for all NaF treatments, since the series resistance of the best cell remains lower in all cases than the control device, albeit with more variation with higher anneal temperatures. The shunt resistance appears to initially increase before peaking before around 200°C, and although increased shunt resistance will lead to a higher fill factor, the increase in this device series is dominated by the lower series resistance. The combined effect of all these parameter changes with temperature means there is little overall change in the efficiency. Some of the higher temperature anneal devices suffered from several 'shunted' cells, which lowers the average efficiency, however in general the peak efficiency of cells tends to be slightly increased for most anneal temperatures, especially at 300°C.

Despite the large spread of values common for laboratory made solar cells with various processing steps, it is clear that the addition of NaF is not causing a drastic reduction in device efficiency as seen previously [14, 18], whilst improving the quality of the back contact. This suggests that the excessive recrystallisation which proved detrimental to device performance in previous attempts at sodium incorporation in CdTe devices is avoided by depositing NaF after the chlorine treatment. This is supported by x-ray diffraction measurements (Figure S4) and electron microscopy (Figure S5) of films with thicker (5 nm) NaF layers, which is expected to exaggerate the influence of NaF incorporation, yet show no indication of significant structural changes.

Figure 3 shows external quantum efficiency (EQE) data for the highest efficiency cells from the NaF treated devices described previously. The EQE curves shown in Figure 3a are normalised to maximum collection efficiency for ease of comparison in Figure 3b, and show very little difference in the CdS shoulder region at short wavelength. In previous attempts which have incorporated sodium into CdS/CdTe devices prior to the chlorine treatment, there has been significant recrystallization at the interface [14, 15, 18], consuming the CdS layer which manifests itself as an increase of EQE in the short wavelength region. Since there is no such effect observed here, it is likely that the CdS layer remains intact and therefore can create a suitable junction with CdTe which can effectively separate charge carriers.

The long wavelength region of the normalised EQE curves shows a subtle trend with anneal temperature. This can be seen more easily in Figure 3c which focuses on the shoulder region whereby collection efficiency decreases as the photon energy decreases below that of the CdTe band gap. To show the effect of NaF treatment on this long wavelength region more clearly, Figure 3d plots the gradient along the top of the normalised EQE curves between

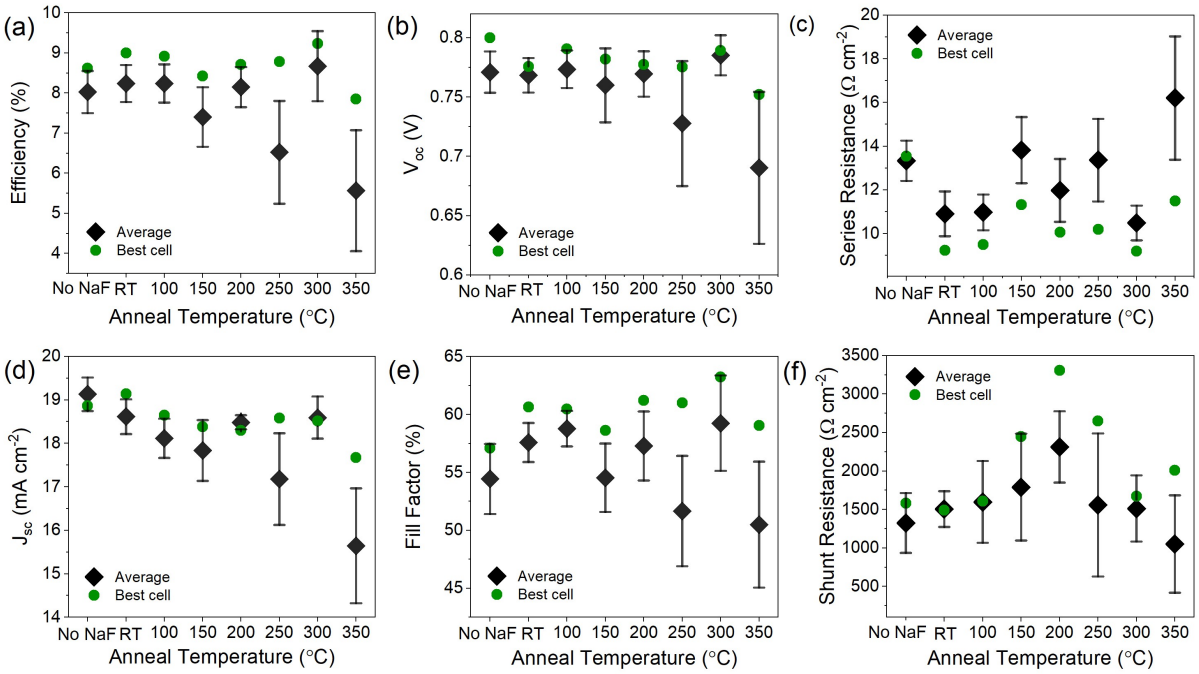

Figure 2: JV parameters showing (a) efficiency, (b) open circuit voltage (V_{oc}), (c) series resistance, (d) short circuit current density (J_{sc}), (e) fill factor and (f) shunt resistance of devices with 1 nm NaF evaporated prior to contacting and annealed for 20 min at various temperatures. Average values are shown with error bars corresponding to the standard deviation from nine 0.25 cm^2 cells per device, as well as the parameters for the highest efficiency cell from each device.

650-800 nm, and the gradient corresponding to the CdTe bandgap cut-off between 825-850 nm, as a function of NaF anneal temperature. Together these values give an indication of the 'squareness' of the EQE response at long wavelengths which corresponds to how well carriers are separated from deeper in the CdTe layer. With increasing anneal temperature, the top of the EQE curves become flatter (i.e. 650-800 nm gradient is less negative), whilst the CdTe bandgap cut-off becomes steeper (825-850 nm gradient is more negative). This means there is more efficient collection at long wavelength with increasing anneal temperature up to 250°C, where the trend is then reversed. This could result from a number of changes in the device, but given the results from capacitance-voltage measurements shown later in Figure 4, this is likely caused by a changes in depletion width allowing more efficient collection further into the CdTe layer.

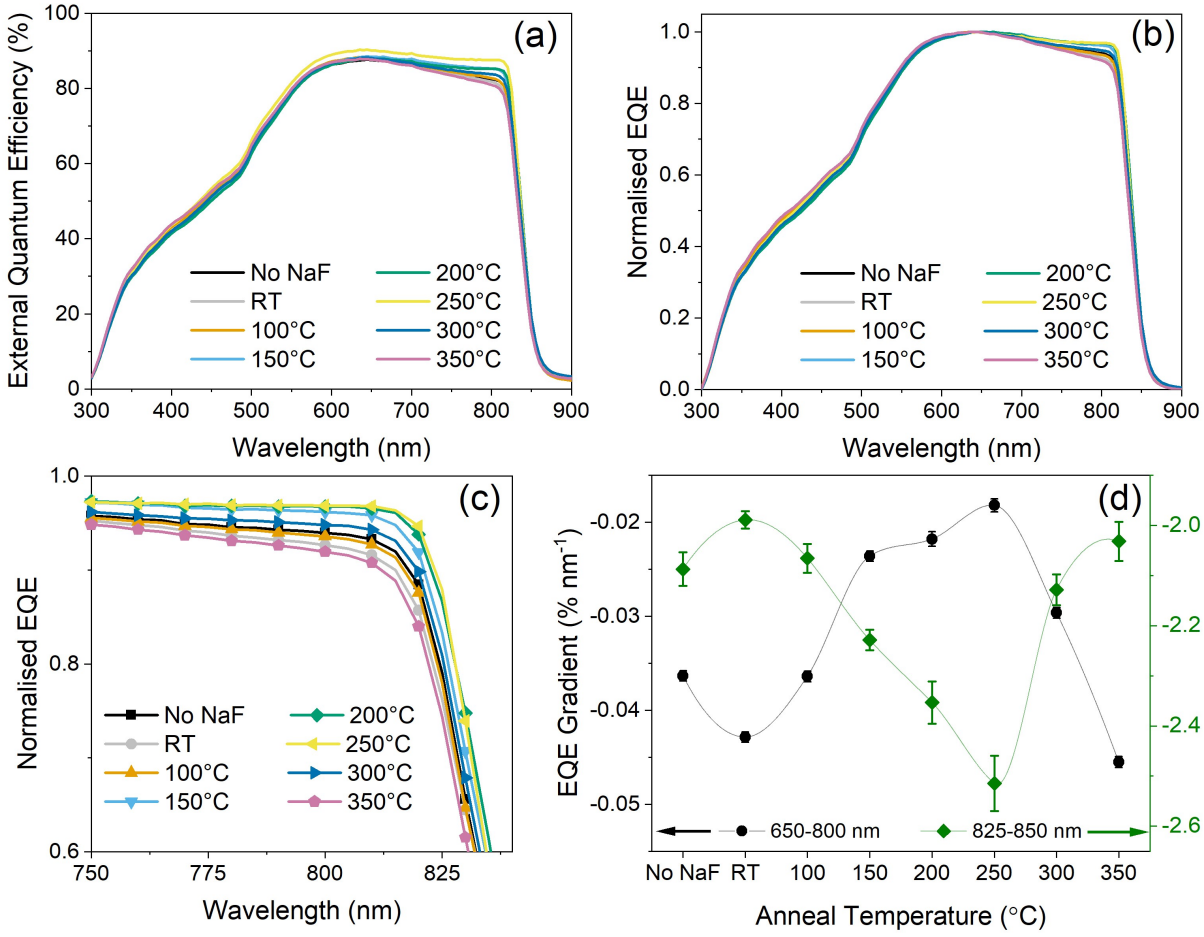

Figure 3: (a) Raw and (b) normalised EQE curves for champion cells from devices with 1 nm NaF deposited prior to contacting and annealed up to 350°C, compared to a control device without NaF. (c) shows the long wavelength region between 750-840 nm in more detail. (d) shows the gradient of the curves at long wavelength corresponding to the flat top and bandgap cut-off, representing the 'squareness' in this region with lines connecting datapoints shown as a guide to the eye.

Capacitance-voltage measurements were performed on the best performing cell on each device, from which the doping density as a function of depletion width can be determined as shown in Figure 4a. There is a change in both doping density and depletion width with annealing temperature, which can be seen clearer in Figure 4b. With the addition of NaF at the back surface and subsequently annealing at temperatures up to 250°C there is a decrease in the bulk acceptor concentration, which implies that rather than forming acceptor levels by occupying Cd sites, it is instead forming compensating defects that act to reduce the overall doping density, likely by incorporating interstitially into the CdTe lattice. Above 250°C there is a sharp reversal of this trend with the acceptor concentration increasing with anneal temperature, reaching a maximum of a 50% increase compared to the control device without NaF. At this temperature, it appears the incorporation onto Na_{Cd} sites is energetically favourable compared to Na_i incorporation, thereby increasing the doping density. Since the maximum temperature used in this study was limited to 350°C it remains unclear whether higher temperatures would facilitate higher doping densities, however preliminary test devices showed reduced performance due to the presence of a heavily oxidised back surface that accompanies the higher anneal temperatures.

The depletion width varies inversely with acceptor concentration, since lower doping density requires a larger

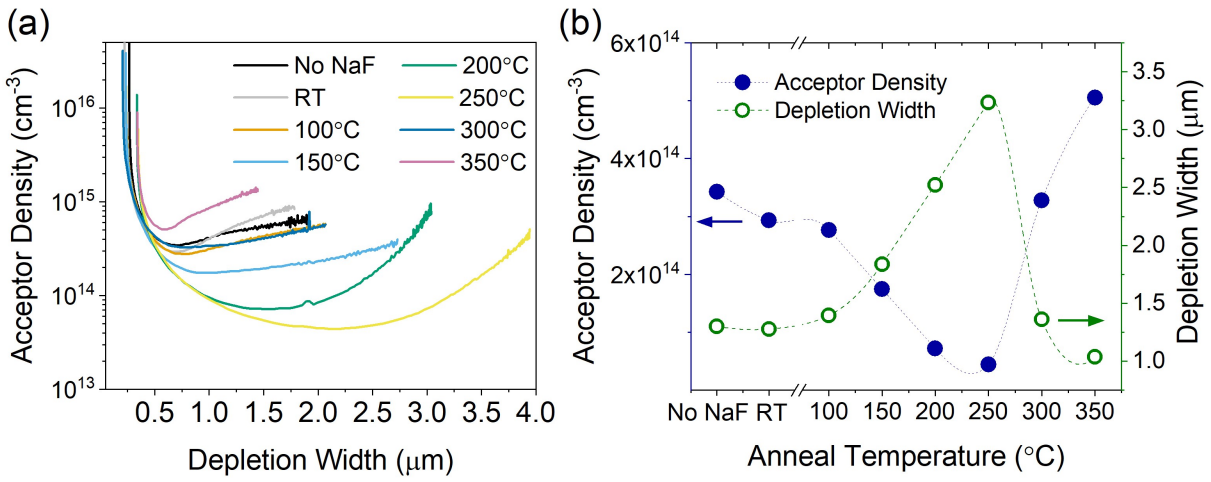

Figure 4: (a) Acceptor density versus depletion width extracted from Mott-Schottky plots for devices with 1 nm NaF annealed up to 350°C compared to a device without NaF, (b) bulk acceptor density taken from the minima of curves in Figure 4a, and the depletion width at zero bias

volume of CdTe to balance the overall charge. The change in depletion width with anneal temperature can be seen to roughly match the trend in Figure 3d which can explain the improvement in EQE response at long wavelengths up to 250°C. Devices which have the largest depletion width allow more efficient collection of carriers further into the device, which long wavelength photons are more likely to reach. Since depletion width scales inversely with acceptor concentration, it is necessary to find a balance between a highly doped absorber to increase V_{oc}, whilst maintaining a sufficient electric field in the bulk of the device. That balance depends on a range of material properties such as carrier lifetime, mobility and absorber thickness, and is typically around 10^{16} cm^{-3} for CdTe [26]. This is much higher than observed here and therefore despite the reduced depletion width, annealing devices with NaF above 250°C is likely necessary for effective doping.

3.2. Chemical composition of NaF treated devices

Having looked at how annealing NaF affects CdTe at a device level, the effect of processing conditions on the elemental profiles and back surface is now considered. The anneal temperature has been found to influence the extent of sodium incorporation into the device, with temperatures above 250°C required to increase the carrier concentration. A control device without NaF or annealing was compared to devices with 1 nm NaF annealed for 20 min in air at either low (200°C) or high (300°C) temperature. Figure 5 shows the distribution of sodium, fluorine and chlorine measured via ToF-SIMS analysis and quantified by comparing these devices to ion-implanted reference standards for each element in CdTe.

Sodium is present in significant quantities in the control device without the intentional addition of NaF. There are several potential sources of sodium, as described further in Section 3.3, and the concentration of $\sim 10^{17}$ cm^{-3} in the bulk of the CdTe layer is consistent with previously reported values [27–29]. Upon the addition of 1 nm NaF at the back surface and annealing at 200 °C there is a large increase in the sodium signal at the back surface, which gradually decreases further into the bulk following a typical in-diffusion profile, before increasing again at the front on the device near the CdS layer. The Te rich back surface resulting from the NP etch [30] may account for the relative ease of incorporation at the back contact, however sodium does not appear to incorporate effectively

into the bulk of the CdTe with only a minor increase in comparison to the control device. Nonetheless it would appear to be mobile throughout the device, since there is increased accumulation at the front surface towards the CdS window layer. This could be accounted for if transport is dominated by rapid diffusion along grain boundaries which is expected to be far quicker than through the grain interior [31]. This would allow sodium to reach the CdS layer relatively easily, where its effect on device performance remains unclear. Sodium would be expected to compensate native *n*-type CdS doping by occupying a cadmium site through the formation of Na_{Cd} acceptors, which would lower the built-in voltage (V_{bi}) due to a lower net doping density. However, CdS is natively *n*-type due to sulphur vacancies [32] and therefore it is unclear whether this Cd rich composition would lend itself to the formation of Na_{Cd} acceptors or would sit interstitially. Nonetheless it appears that, similar to copper [3], sodium shows a strong preference to segregate at the junction position, consistent with previous observations by other authors [29].

For the 300°C annealed sample there is a further increase in sodium content at the front contact, however there is also a near-uniform incorporation throughout the bulk CdTe. This indicates that the higher anneal temperature is required to drive the sodium into the grain interior, which would be consistent with the sharp change in the trend of doping density observed at this temperature in Figure 4. There is also a small peak in the sodium profile near the back surface for the 300°C anneal, which again could result from Na incorporating more effectively in the Te rich region left by the NP etch, or alternatively be due to a difference in sputtering yield due to surface oxidation.

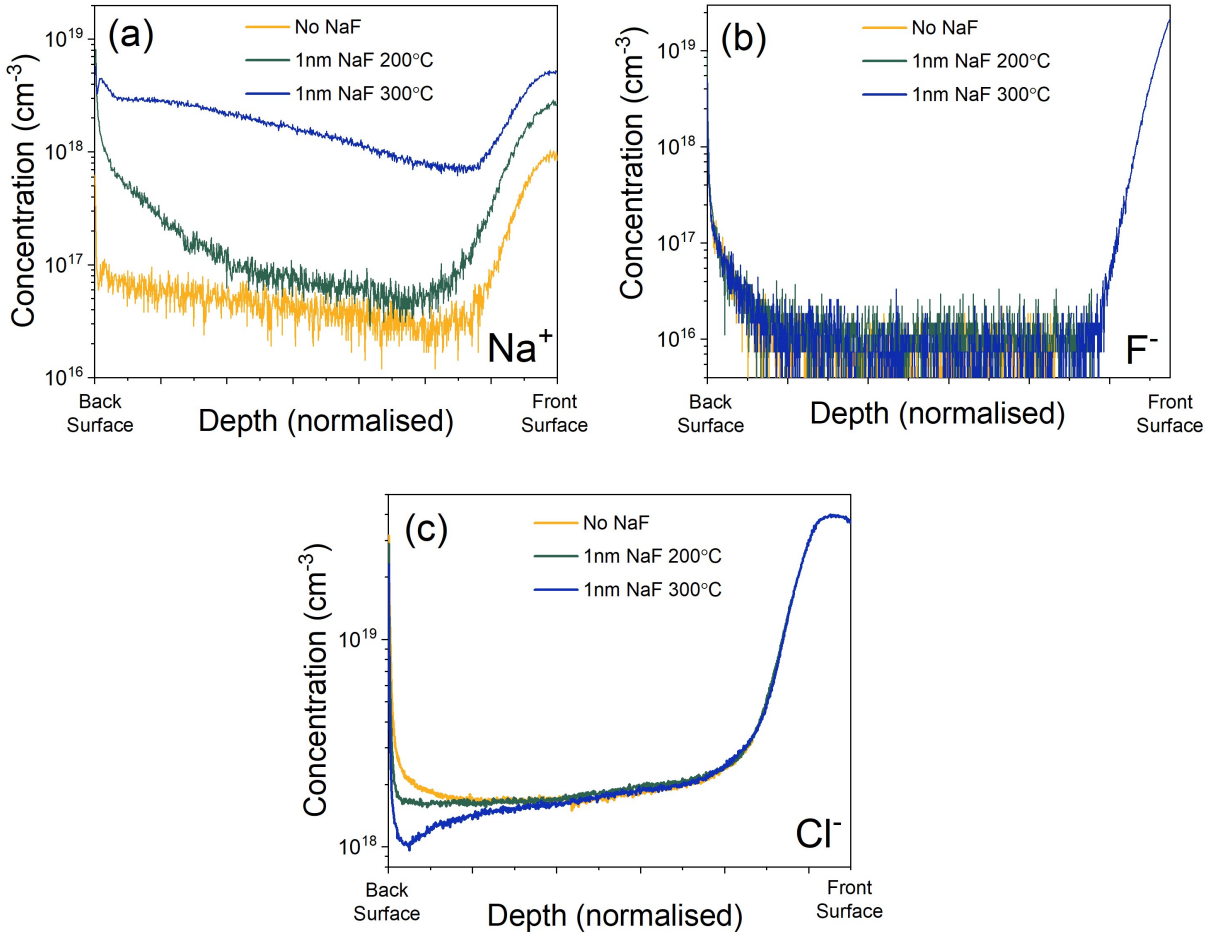

Figure 5: Distribution of (a) sodium, (b) fluorine and (c) chlorine obtained from ToF-SIMS measurements of devices with 1 nm NaF deposited following $MgCl_2$ treatment annealed at 200°C and 300°C compared to a reference device without NaF.

The fluorine signal shown in Figure 5b shows an identical trend for all three devices regardless of the addition of NaF or the anneal temperature. Whilst fluorine would be expected to be an *n*-type dopant in CdTe when occupying Te sites, chlorine is in the same group and appears to aid *p*-type doping via the formation of the shallow A-centre defect complex $(V_{Cd}$ - $Cl_{Te})^{-1}$ [33][34]. It is unclear whether fluorine would act in a similar manner, although it is noteworthy that there is preliminary evidence of fluorine inclusion during chlorine treatment having a beneficial effect [35, 36]. In any case, the absence of any additional fluorine from the NaF treatment is favourable for achieving a high doping density with a simpler defect structure, and suggests NaF is a suitable source of sodium. Diffusion of fluorine into CIGSSe solar cells during NaF treatment is inhibited by the formation of volatile SeF_6 [37]. A similar reaction to form TeF_6 might occur here and would offer a plausible explanation for the lack of excess F signal in the bulk of the CdTe layer upon NaF treatment. Despite no additional fluorine contribution in the CdTe layer from the NaF layer within the instrumental detection limits, there is a clear increase in signal towards the back surface for all devices. This could result from out-diffusion from the SnO_2:F layer at the front contact, whereby fluorine segregates out of the CdTe layer towards the back surface during device processing as seen previously by Emziane et al [38]. Impurities in the $MgCl_2$ solution and NP etch could also offer potential sources of fluorine contamination.

Figure 5c shows a similar chlorine content for the three devices towards the front surface and most of the bulk CdTe layer, however there is a small change at the back surface for the three devices. All samples show a very rapid increase in chlorine concentration within the first few nanometres from the back contact which likely indicates oxychlorides remaining on the surface following the activation treatment [39]. The control device without NaF shows a large, gradual increase in Cl concentration at the back surface which is not surprising given the $MgCl_2$ activation process is likely to leave a chlorine rich region. The low temperature NaF annealed device shows a much flatter region with no gradual increase in Cl signal. Higher anneal temperature leads to a further reduction of the back-surface Cl content, leaving a slightly chlorine deficient region. It is unclear what causes this loss of chlorine and whether it has an impact on device performance, but since the chlorine deficient regions overlap with the excess sodium, some reaction involving both elements seems plausible. Considering the improvement in contacting with NaF implied in Figure 1, this change in chemical composition at the back surface could be beneficial for device performance.

XPS was used to determine the chemical composition of the back surface of a reference CdTe device without NaF compared to one with 1 nm NaF deposited prior to a 20 min anneal at 300°C in air, which was expected to show the most significant change from previous analysis. The $3d_{5/2}$ core level peaks are given in Figure 6 (a) for Cd and (b) for Te. The cadmium spectra in both cases can be fit with a single peak and therefore atoms are bonded only to tellurium with no contribution from sodium, fluorine, magnesium, or chlorine (within the limits of detection). While the tellurium peak for the reference device is similar, in that there is only one bonding environment, in the case of the NaF device there is a secondary peak appearing at higher binding energy corresponding to the formation of a TeO_2 oxide phase at the back surface. This oxidation is caused by the annealing step required to effectively distribute the sodium throughout the CdTe and increase the doping density, however is likely to be detrimental to device performance as it will hinder the formation of an ohmic contact [40, 41]. In this case it appears the beneficial effects of doping outweigh the effects of this oxidation as this does not show the rollover observed for the reference device in Figure 1, however the series resistance does increase with anneal temperature which is likely caused by increasing the thickness of TeO_2. This might be overcome by annealing the devices either in an inert atmosphere or under vacuum, so that high doping densities might be obtained as well as an oxide free surface.

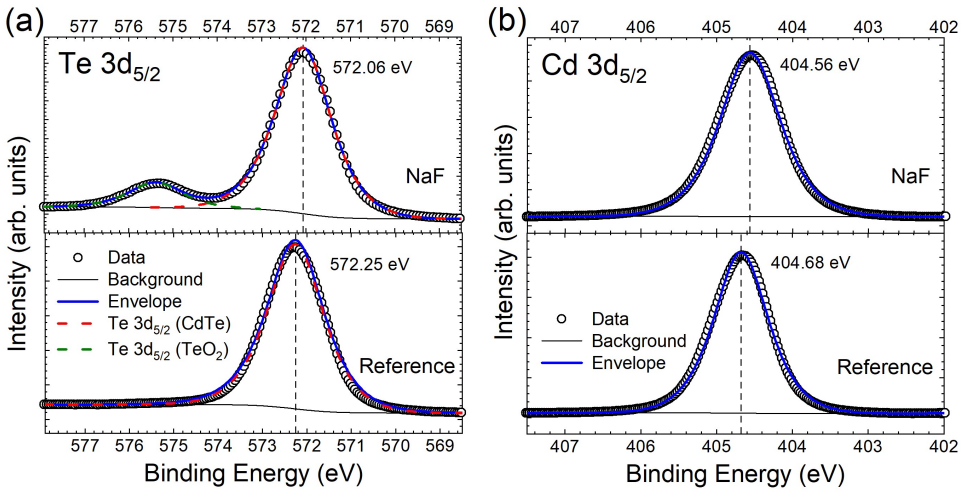

Figure 6: Core level XPS spectra showing the (a) Te $3d_{5/2}$ and (b) Cd $3d_{5/2}$ peaks comparing a standard CdTe device to one with 1 nm NaF evaporated at the back surface and annealed at 300°C for 20 min in air

3.3. Unintentional sodium in CdTe solar cells

The presence of unintentional dopants in source materials can have a significant influence photovoltaic device performance, and have been documented to go as far as changing the carrier type of absorber materials from *p*-type to *n*-type [42]. Whilst copper is typically considered to be a common impurity even in nominally undoped CdTe films [4], since tellurium is manufactured as a byproduct of copper refinement, far less attention is paid to the sodium contamination. However, given the measurement of $> 10^{16}$ cm^{-3} Na atoms in 'NaF free' reference devices (Figure 5a), it is important to consider the potential sources of unintentional sodium incorporation during device processing. Impurity analysis via ICP-OES of the 5N purity (Alfa Aesar) CdTe source material used in this work is detailed in Table S1, and shows sodium to be present in a concentration of $(4.2 \pm 0.2) \times 10^{17}$ cm^{-3}. This is much higher than for copper, which was barely detected on the limits of the instrument implying a concentration around $\sim 10^{14}$ cm^{-3}. Sodium has previously been shown to strongly affect the electronic and structural properties of CdTe films [14, 16], yet there are few reports considering what role this level of contamination might play in a device structure.

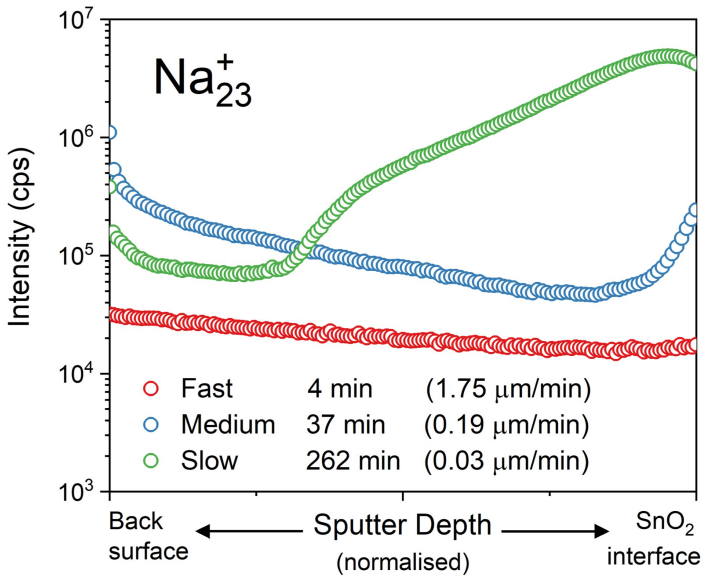

Figure 7: SIMS depth profile showing the relative distribution of sodium in CdTe films grown on TEC15M substrates at different growth rates, thereby exposing the substrates to high temperatures (550°C) for 4 min (fast), 37 min (medium) and 262 min (slow) during deposition

Although impurities within the source material might be avoided relatively easily with further purification of CdTe, other sources of contamination such as diffusion from glass substrates may be more challenging to prevent whilst remaining compatible with low-cost, high-volume manufacturing. Figure S6 shows a CdTe film deposited onto a TEC 15M substrate, which consists of soda lime glass coated with series of layers, including a nominally 30nm SiO_2 film which acts as an alkali diffusion barrier layer [43]. Such substrates are ubiquitous in CdTe literature as they are convenient, low-cost and produced commercially in high volumes. The ability of the SiO_2 layer to effectively prevent out-diffusion of sodium was examined by depositing CdTe onto these substrates at different growth rates, thereby varying the amount of time the samples are subject to elevated temperatures. This was achieved by adjusting the chamber pressure during CSS deposition, which in turn changes the sublimation rate and therefore controls the CdTe growth rate [20]. During this time, the substrate is held at 550°C, which is typical for CdTe processing to encourage a large grain structure.

Figure 7 shows the distribution of sodium throughout a CdTe film deposited on TEC 15M substrates at three different growth rates, measured via non-quantitative SIMS profiling. Fast deposition (4 mins) of the CdTe layer results in uniform incorporation of sodium throughout the absorber layer, with a slight decrease in signal intensity as the measurement proceeds from the back surface of the CdTe layer towards the SnO_2 substrate. As the growth in slowed down to a 37 min deposition, the count rate of the sodium ions increases by roughly an order of magnitude, with a sharp increase towards the SnO_2 layer suggesting out-diffusion from the substrate. This is in agreement with observations by Emziane *et al* who found comparable levels of sodium contamination in CdTe films, which was similarly ascribed to diffusion from the glass substrates [29, 38]. Further slowing the growth rate leads to a large increase in the sodium content in the bulk CdTe region close to the substrate, decreasing towards the back surface. The increased count rate for longer depositions, especially towards the substrate interface, shows that slowing the growth rate the increases the concentration of sodium in the CdTe layer. This is presumably due to more impurity diffusion out of the soda-lime glass caused by the higher thermal budget of the deposition process.

Although CSS grown CdTe layers are typically deposited at high growth rates, this demonstrates the potential for sodium migration from glass substrates despite the use of alkali blocking layers. Whilst sodium is expected to increase *p*-type doping and therefore may be beneficial to device performance, uncontrolled incorporation from source material and diffusion during processing is not likely to be an effective, nor reproducible, doping strategy. Instead we have found that depositing a thin layer of NaF at the back surface of CdTe solar cells prior to metallisation, analogous to how copper is often incorporated, offers a controllable method of sodium incorporation. However, given the already considerable levels of sodium present in the control devices, additional study of CdTe devices deposited on alkali free substrates with higher purity source material would allow the effect of sodium to be isolated further.

4. Conclusions

Sodium has been shown to be present in significant quantities for CdTe samples of commercially available 5N polycrystalline lumps, as well as in thin films deposited onto soda lime glass due to out-diffusion from the substrate. Given sodium is an an active *p*-type dopant in CdTe, this work highlights the importance of identifying unintentional impurities and the role they may have in CdTe solar cells.

The evaporation of a thin layer of NaF prior to contacting CdTe solar cells has been shown to be an effective strategy for intentionally incorporating sodium into the device structure without the adverse structural effects observed by previous authors [14, 16–18]. However, the improvement in device performance has been modest even for optimised treatment conditions. This is likely due to several overlapping processes occurring during the evaporation of NaF and subsequent annealing of devices, such as oxidation of the back contact and sodium accumulation in the CdS layer. It may also be that given the high sodium content already present in the control device, the additional sodium is of limited benefit to device efficiency overall. However, at the back surface an improved contact is readily achievable regardless of specific processing steps, requiring only the presence of 1 nm NaF. This produces a highly doped region at the back surface which thereby lowers the contact barrier, leading to an increased fill factor due to lower series resistance. Increasing the bulk doping density requires annealing devices to redistribute the sodium throughout the device, and from the grain boundaries into the grain interior. This occurs for annealing temperatures above 300°C, whereby the doping density increases above that of the reference device. Optimised processing conditions lead to a minor overall improvement for devices annealed at 300°C compared to a reference device without NaF, which is primarily a result of an increased fill factor caused by an improved back contact. This work highlights the importance of sodium as impurity in CdTe solar cells, and shows the potential for intentional sodium doping to improve device performance without recrystallisation of the CdTe layer.

5. Supplementary Information

JV performance parameters and CV measurements of CdTe devices with different NaF thickness, JV data for stability of devices over two month period, XRD of NaF coated CdTe films as a function of anneal temperature, electron microscopy of CdTe films with and without NaF, ICP-OES of CdTe source material, cross section electron microscopy of CdTe/TEC15M device stack.

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7. Author Contributions

TPS fabricated samples and prepared the manuscript with JDM. HS and VRD conducted XPS analysis. OSH and GZ carried out SIMS measurements while electron microscopy was performed by LB.

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