High Step-Up Switched-Capacitor Active Switched-Inductor Converter with Self-Voltage Balancing and Low Stress

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***Abstract*—High step-up DC-DC converters are widely used in new energy applications such as photovoltaic cell, fuel cell, DC microgrid etc. Active switched-inductor (ASL) converter has simple operation and low stress on switches. To further increase the voltage gain, some SC (switched-capacitor)/ASL step-up converters have been proposed recently. However, these SC/ASL step-up converters have voltage oscillation on switches, which leads to the voltage stress on switches is higher than the theoretical value. In this paper, a novel high step-up SC/ASL converter is proposed. Compared with other SC/ASL step-up converters, the proposed converter has lower voltage stress on the switches, output diodes and output filter capacitors, and the efficiency is higher. In addition, the proposed converter can achieve self-voltage balancing on switches. This paper analyzes the proposed converter from operation principle, continuous conduction mode (CCM) analysis, CCM operation with unbalanced inductors, input current ripple analysis, discontinuous conduction mode (DCM) and boundary conduction mode (BCM) analysis, switches self-voltage balancing characteristic, voltage stress, current stress, comparison analysis, and design considerations. Finally, a 200W, 25-45V/380V, 50kHz experimental prototype has been established in the laboratory to evaluate the proposed converter, which reached a peak efficiency of 97.3%.**

***Index Terms*—Active switched-inductor (ASL), switched-capacitor (SC), high step-up DC-DC converters, self-voltage balancing.**

I. INTRODUCTION

IN recent years, high step-up DC-DC converters have been widely used, and their applications mainly include solar photovoltaic (PV) cell, fuel cell (FC), DC microgrid, electric vehicle, uninterruptible power supply (UPS) etc. [1]-[6].

High step-up DC-DC converters are divided into two types: isolated type and nonisolated type. Isolated high step-up converters can obtain high voltage gain by adjusting the transformer turn ratio, however, high voltage spike usually could be produced during switch transition process because of the leakage inductor. In addition, isolated type converters have many shorts, such as large volume, large weight, and high costing [7]-[9]. Nonisolated high step-up converters are widely used in the applications which electrical isolation is not required. Nonisolated converters can be mainly classified into many different categories, such as cascading, coupled inductor, SC (switched-capacitor) and SL (switched-inductor). The cascade converters achieve high voltage gain by cascading multiple boost converters. However, due to large quantities of components of the cascade converter, the system efficiency is usually low, and cascade converter requires more control circuits, which increases the complexity of the system [10], [11]. Coupled inductor high step-up converters are similar to isolated type converters, the high voltage gain can be achieved by adjusting the turn ratio of the coupled inductor. But the leakage inductor of the coupled inductor could cause voltage spikes and it may increase the voltage stress on the power semiconductor device, therefore, coupled inductor converters need more snubber circuits which increase the complexity of the converter [12], [13]. Using multiple SC cells or SL cells are the other two methods to achieve high voltage gain, however, this may reduce the efficiency of the converter because of a large number of components [14]-[17].

Active switched-inductor (ASL) is another effective boost structure, which obtains voltage gain by charging the inductors in parallel and discharging in series [18]. Compared with the above four types, ASL has the characteristics of simple structure and low voltage and current stresses on the switches. But the voltage gain of ASL converter is difficult to exceed 10 times. In order to further increase the voltage gain, the ASL converter with different types of single-stage SC cells were proposed in [19]-[21], [24]. The ASL converter with two-stage SC cells were proposed in [23], [25], [27], compare with single-stage SC/ASL converters, the two-stage SC/ASL converters have higher voltage gain and lower stresses on switches and diodes. A hybrid switched-inductor/SC converter was proposed in [22], which based on the symmetrical hybrid switched inductor (SH-SLC) in [33]. In [26], a hybrid switched-inductor/SC converter with an auxiliary switch was proposed to improve the voltage gain and efficiency. However, for these SC/ASL step-up converters, there is usually a problem of overvoltage on the switches. When the inductor values are not identical, the junction capacitors of the switches resonate with inductors, which may cause voltage oscillation on two switches. Although the theoretical value of the voltage stress on

the switches is low, the actual voltage stress on the switches is higher than the theoretical value because of the voltage oscillation on switches. In order to reduce the voltage oscillation, some snubber circuits like RC need to be added, which increases the complexity of the system. In brief, the present existing SC/ASL step-up converters still have the problem of overvoltage on switches, which needs to be solved.

A novel high step-up SC/ASL converter is proposed in this paper, named ASL-SC-2OD. The features of the proposed converter are as follows: 1) It has high voltage gain. 2) simplicity of operation (only two modes in CCM). 3) the proposed converter can achieve self-voltage balancing on two switches due to the capacitors clamp structure. 4) the switches voltage stress is reduced, which leads to lower voltage stress MOSFETs with smaller ON-resistance (R_{on}) can be selected. 5) the output diodes voltage stress is reduced and lower voltage stress output diodes can be utilized, also the one output diode can help form a capacitor clamp loop to clamp the voltage of switch. 6) The output capacitors are not only the output filters, but also a part of the capacitors clamp structure, and the output capacitors have lower voltage stress. 7) The proposed converter has lower cost. 8)higher efficiency (peak efficiency is 97.3%).

In order to comprehensive introduce the proposed converter in detail, the remaining of this paper is organized as follows. In section II, the structure of the proposed converter is introduced, then the operation principle, CCM analysis, CCM operation with unbalanced inductors, input current ripple analysis, DCM and BCM analysis, switches self-voltage balancing characteristic, voltage stress on the power components, current stress across the power components. The comparison of the proposed converter with other similar nonisolated step-up converters is presented in section III. Design considerations are discussed in section IV. Section V presents the experimental waveforms and the experimental results. Finally, the conclusions have been drawn in Section VI.

II. Theoretical Analysis of Proposed Converter

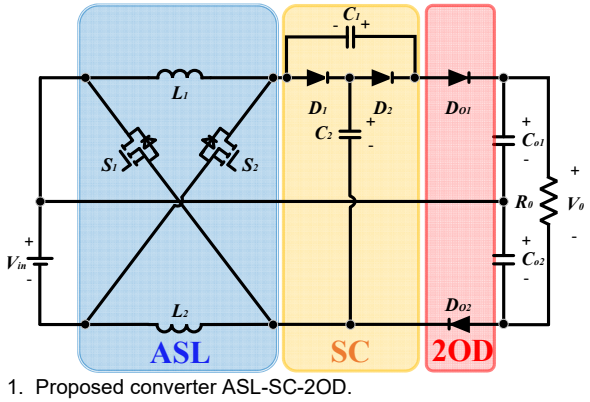


Fig. 1. Proposed converter ASL-SC-2OD.

The structure of the proposed converter is shown in Fig. 1, the proposed converter is composed of ASL network (two switches S_1&S_2, two inductors L_1&L_2), SC cell (two capacitors C_1&$C2$, two diodes D_1&D_2), two output diodes D_{O1}&D_{O2} and two output capacitors C_{o1}&C_{o2}. So, the proposed converter can be named ASL-SC-2OD. The components position of the proposed converter is an important feature to increase the voltage gain, reduce their voltage stress and also maintain the

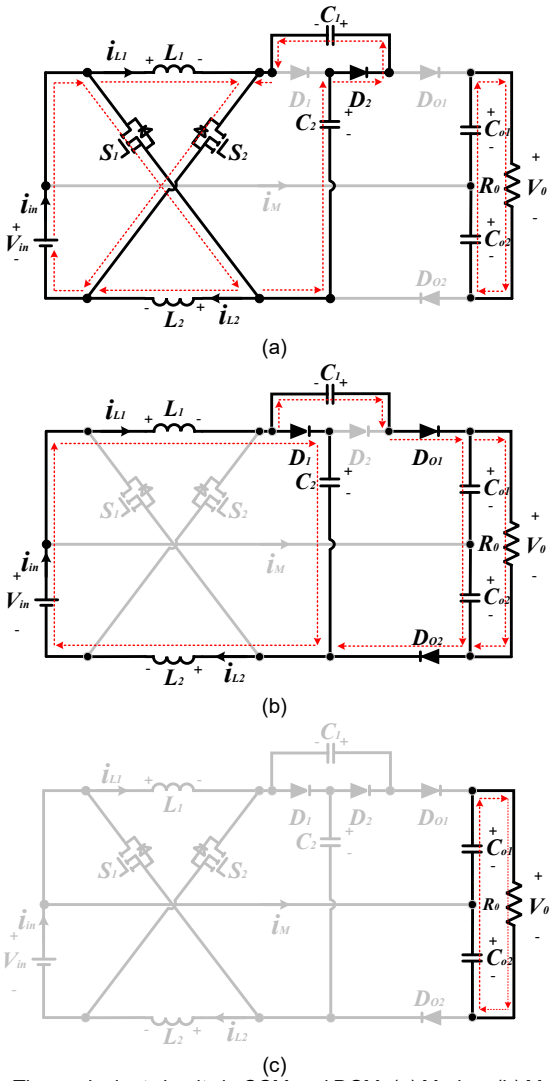


Fig. 2. The equivalent circuits in CCM and DCM. (a) Mode I. (b) Mode II. (c) Mode III.

simple operation. In addition, the ASL-SC-2OD converter can achieve self-voltage balancing on switches due to the capacitors C_1, C_{o1} and C_{o2}. The voltage of S_1 is clamped by C_{o2} and the voltage of S_2 is clamped by C_1 and C_{o1}. The output capacitors C_{o1} and C_{o2} are not only the output filters, but also a part of the capacitors clamp structure. In order to verify the above characteristics, the proposed converter is theoretically and experimentally analyzed in detail in the following sections.

A. Operation Principle

The ASL-SC-2OD converter can be divided into two modes of operation: CCM and DCM. The equivalent circuits in CCM and DCM are shown in Fig. 2. In one switching cycle, the equivalent circuits in CCM are mode I and mode II, as shown in Fig. 2(a)&(b), and the typical waveform in CCM is shown in Fig. 3(a). In DCM, the equivalent circuits are mode I, mode II and mode III, as shown in Fig. 2(a)-(c), and the typical waveform in DCM is shown in Fig. 3(b). To simple the analysis, the following assumptions are made: all components are ideal; both input and output voltages are constant; L_1=L_2=L; The detailed analysis of the three modes is presented in the following part.

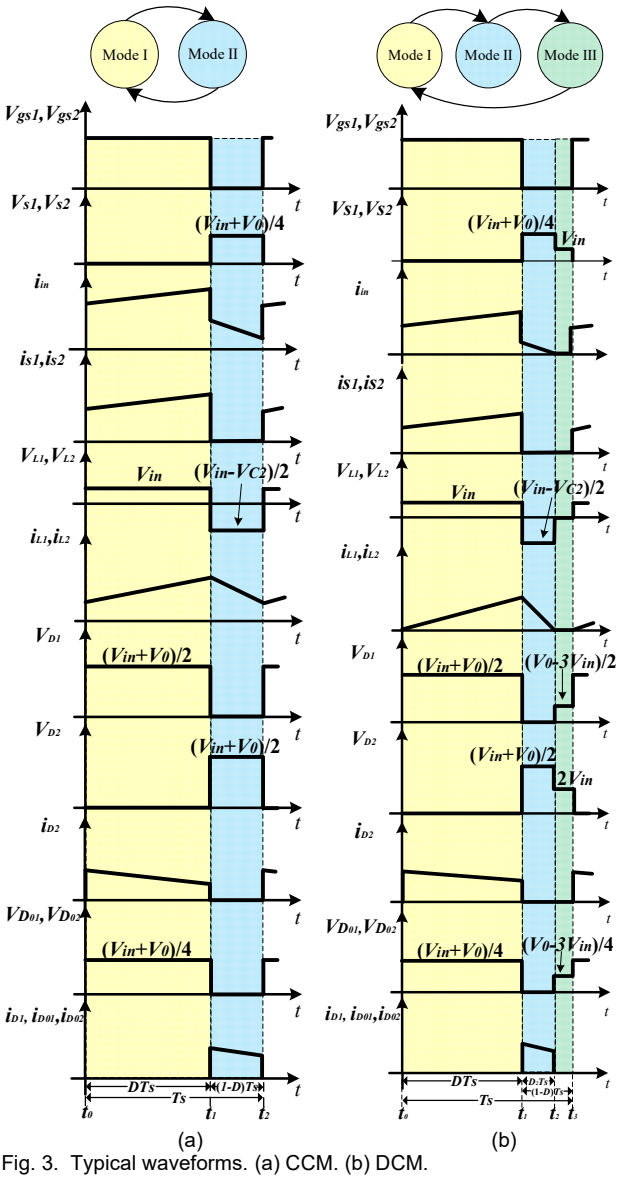


Fig. 3. Typical waveforms. (a) CCM. (b) DCM.

1) Mode I [t_0-t_1, Fig. 2(a)]: In mode I, the two switches S_1 and S_2 are turned on simultaneously. Two inductors L_1&L_2 are connected in parallel and charged by input voltage V_{in}, the currents of two inductors i_{L1} and i_{L2} are increased linearly, the peak value of inductor current i_L can be expressed as

$$i_{L1(t)}=i_{L2(t)}=i_{L(t0)}+\frac{V_{in}}{L}(t_1-t_0) \tag{1}$$

where $i_{L(t0)}$ is value of i_L at t_0.

The diodes D_1, D_{O1}, D_{O2} are reverse-biased, the diode D_2 is forward-biased. The DC source and C_2 charge C_1, and the capacitor C_2 is discharged. The energy stored in capacitors C_{o1} and C_{o2} is released to the load R_0. According to Kirchhoff Voltage Law (KVL), the relationship between the voltage on the capacitor C_1 and the capacitor C_2 is given by

$$V_{in}+V_{C2}=V_{C1} \tag{2}$$

2) Mode II [t_1-t_2, Fig. 2(b)]: In mode II, the two switches S_1 and S_2 are turned off altogether, the two inductors L_1 and L_2 are connected in series and discharged to post-stage circuit. The currents of two inductors i_{L1} and i_{L2} are decreased linearly, the peak value of inductor current i_L can be expressed as

$$i_{L1(t)}=i_{L2(t)}=i_{L(t0)}+\frac{V_{C2}-V_{in}}{2L}(t_2-t_1) \tag{3}$$

The diode D_2 is reverse-biased, the diodes D_1, D_{O1}, D_{O2} are forward-biased. The capacitor C_1 is discharged and the capacitor C_2 is charged. According to KVL, the relationship between the voltage across the capacitor C_1 and the capacitor C_2 is given by

$$V_{C1}+V_{C2}=V_0 \tag{4}$$

3) Mode III [t_2-t_3, Fig. 2(c)]: In mode III, the two switches S_1 and S_2 are turned off, the inductor current is always zero and this mode is only for DCM. The diodes D_1, D_2, D_{O1}, D_{O2} are all reverse-biased, all semiconductors of the proposed converter are blocked. The energy stored in capacitors C_{o1} and C_{o2} is released to the load R_0.

B. CCM Analysis

In CCM, the ASL-SC-2OD converter is divided into mode I and mode II. According to the equivalent circuits in CCM, as shown in Fig. 2(a) and Fig. 2(b), in mode I, the voltage across the inductors can be expressed as

$$V_{L1}^{\ \mathrm{I}}=V_{L2}^{\ \mathrm{I}}=V_{in} \tag{5}$$

In mode II, the voltage across the inductors can be expressed as

$$V_{L1}^{\ \mathrm{II}}=V_{L2}^{\ \mathrm{II}}=(V_{in}-V_{C2})/2 \tag{6}$$

Combining (2) and (4), the voltages across the capacitors C_1&$C2$ are given by

$$V_{C1}=(V_0+V_{in})/2 \tag{7}$$

$$V_{C2}=(V_0-V_{in})/2 \tag{8}$$

According to (6) and (8), in mode II, the voltage across the inductors can be derived as

$$V_{L1}^{\ \mathrm{II}}=V_{L2}^{\ \mathrm{II}}=\frac{3}{4}V_{in}-\frac{1}{4}V_0 \tag{9}$$

The voltage-second balance principle on the inductors is shown in (10).

$$\begin{cases}\int_{t_0}^{t_1}V_{L1}^{\mathrm{I}}dt+\int_{t_1}^{t_2}V_{L1}^{\mathrm{II}}dt=0\\ \int_{t_0}^{t_1}V_{L2}^{\mathrm{I}}dt+\int_{t_1}^{t_2}V_{L2}^{\mathrm{II}}dt=0\end{cases} \tag{10}$$

Combining (5), (6) and (10), the voltage gain of the proposed converter in CCM is derived as

$$G_{CCM}=\frac{V_0}{V_{in}}=\frac{3+D}{1-D} \tag{11}$$

The charge balance principle on the capacitors is shown below

$$\int_{t_0}^{t_2}i_C(t)dt=0 \tag{12}$$

So, in one switching cycle, according to Kirchhoff's Current Law (KCL), the average current of diodes is given by

$$I_{D_1}=I_{D_2}=I_{D_{O1}}=I_{D_{O2}}=I_0=\frac{V_0}{R_0} \tag{13}$$

Because the diode D_2 is only forward-biased in mode I, the diodes D_1, D_{O1}, D_{O2} are only forward-biased in mode II, the average current of diode D_2 in mode I is given by

$$I_{D_2}^{\mathrm{I}} = \frac{I_0}{D} \tag{14}$$

The average current of diodes D_1, D_{O1}, D_{O2} in mode II is

$$I_{D_1}^{\mathrm{II}} = I_{D_{O1}}^{\mathrm{II}} = I_{D_{O2}}^{\mathrm{II}} = \frac{I_0}{1-D} \tag{15}$$

The inductor current I_L is equal to the sum of the average current of diodes D_1 and D_{O1} in mode II, as shown in Fig. 2(b), so

$$I_L = I_{D_1}^{\mathrm{II}} + I_{D_{O1}}^{\mathrm{II}} = \frac{2I_0}{1-D} \tag{16}$$

C. CCM Operation with Unbalanced Inductors

In practice, it is difficult to keep the two inductors consistent, this paper assumes that L_1 is less than L_2. In CCM with unbalanced inductors, the operation of mode I will not change, the main difference is mode II. Fig. 4 shows the operation of mode II with unbalanced inductors, and the key waveforms in the condition of unbalance inductors are shown in Fig. 5. Due to the values of two inductors are different, the rising slope and decreasing slope of both two inductor currents are not the same. In mode II, during $t_1 - t'$, the current flowing path is shown in Fig. 4 and the direction of i_M is from the output side to the input side; during $t' - t^2$, the direction of i_M is from the input side to the output side.

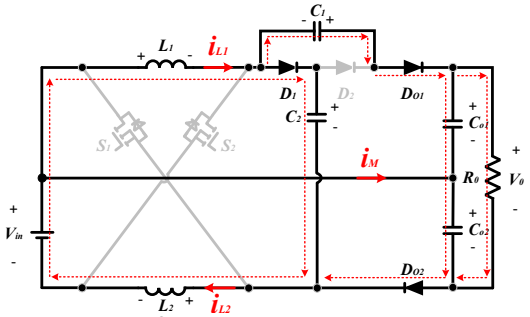


Fig. 4. The operation of mode II with unbalanced inductors.

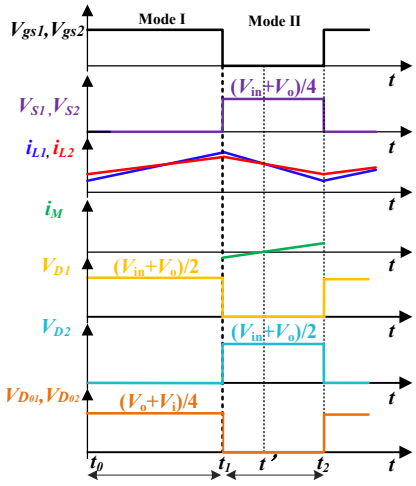


Fig. 5. Key waveforms in the condition of unbalance inductors.

When the values of two inductors are slightly different, their slopes are also slightly different, and the middle line current is very small. Under high frequency, the current in the middle line only affects the voltage ripple of the input and output capacitors, the voltage ripple is very small, and it has very little impact on the average voltage of the input and output capacitors. Therefore, the voltage balance of the input and output capacitors can be remained, and the voltage stress of the switches can be derived as

$$\begin{cases} V_{S1} = V_{C_{O2}} \\ V_{S2} = V_{in} + V_{C_{O1}} - V_{C_1} \end{cases} \tag{17}$$

D. DCM and BCM Analysis

In DCM, the ASL-SC-2OD converter is divided into mode I, mode II and mode III, as shown in Fig. 2(a)-(c), and the operation principles of the three modes are analyzed in detail in section A. According to (1), the peak inductor current in mode I is given by

$$i_{L1p} = i_{L2p} = i_{L(t0)} + \frac{V_{in}}{L} DT_s \tag{18}$$

According to (2) and Fig. 3(b), the peak inductor current in mode II is given by

$$i_{L1p} = i_{L2p} = i_{L(t0)} + \frac{V_0 - 3V_{in}}{4L} D_2 T_s \tag{19}$$

where D_2T_s is the duration time between t_1 and t_2.

Because the peak currents in two modes are equal, combining (18) and (19), the relationship between D_2 and D can be derived as

$$D_2 = \frac{4V_{in}}{V_0 - 3V_{in}} D \tag{20}$$

Combining (13), (18) and (20), the voltage gain in DCM is derived as

$$G_{DCM} = \frac{V_0}{V_{in}} = \frac{3}{2} + \frac{1}{2}\sqrt{9 + \frac{4D^2}{\tau}} \tag{21}$$

where

$$\tau = \frac{Lf_s}{R_0} \tag{22}$$

The ASL-SC-2OD converter can be operated in Boundary Conduction Mode (BCM) when the voltage gain in CCM and DCM is equal. Combining (11) and (21), the boundary condition between CCM and DCM can be derived as

$$\tau_B = \frac{D(1-D)^2}{4D+12} \tag{23}$$

The boundary condition is shown in Fig. 6. The ASL-SC-2OD converter is operated in CCM when τ is larger than τ_B, the ASL-SC-2OD converter is operated in DCM when τ is less than τ_B.

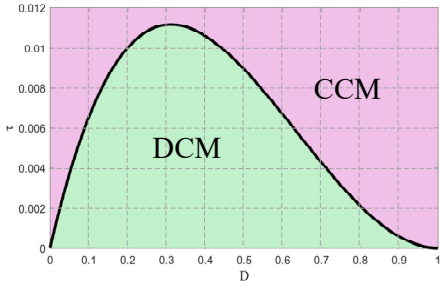


Fig. 6. Boundary condition.

E. Input current ripple analysis

The diagram of input current i_{in}, inductor current i_{L1}& i_{L2}, midline current i_M is shown in Fig. 2. And the current

waveforms of the proposed converter are shown in Fig. 7.

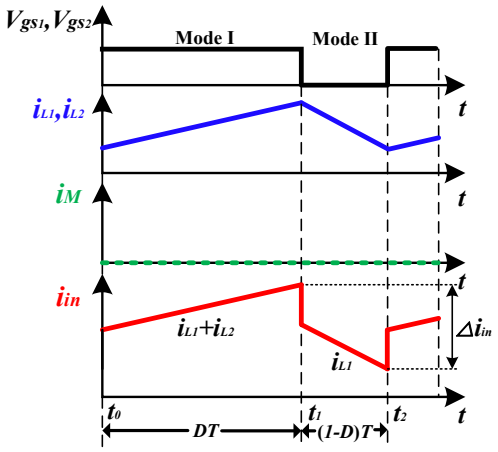


Fig. 7. Current waveforms of the proposed converter.

According to the current waveforms of the proposed converter. The current through inductors L_1, L_2 can be expressed as

$$i_{L1}=i_{L2}=\begin{cases} i_L(t_0)+\dfrac{V_{in}}{L}(t-t_0) & t_0\le t<t_1 \\ i_L(t_1)+\dfrac{3V_{in}-V_0}{4L}(t-t_2) & t_1\le t<t_2 \end{cases} \tag{24}$$

The midline current is given by

$$i_M=0 \tag{25}$$

The input current is given by

$$i_{in}=\begin{cases} i_{L1}+i_{L2} & t_0\le t<t_1 \\ i_{L1} & t_1\le t<t_2 \end{cases} \tag{26}$$

From (24) and (26), the input current can be obtained

$$i_{in}=\begin{cases} \dfrac{4I_0}{1-D}-\dfrac{V_o(1-D)D}{f_sL(3+D)}+\dfrac{2V_o(1-D)}{L(3+D)}(t-t_0) & t_0\le t<t_1 \\ \dfrac{2I_0}{1-D}+\dfrac{V_o(1-D)D}{2f_sL(3+D)}-\dfrac{DV_0}{(3+D)L}(t-t_1) & t_1\le t<t_2 \end{cases} \tag{27}$$

And then, the ripple of input current can be expressed as:

$$\Delta i_{in}=\frac{2I_0}{1-D}+\frac{3V_o(1-D)D}{2Lf_s(3+D)} \tag{28}$$

F. Switches self-voltage balancing characteristic

Several high step-up DC-DC converters which combining ASL structure with SC cell were introduced in literature [19]-[21], [23]-[25], [27]. These SC/ASL step-up converters can be classified into the structure which is shown in Fig. 8. In actual conditions, the parallel parasitic capacitor exists in the MOSFET. So, V_{in}, L_1, C_{p2} and V_{in}, L_2, C_{p1} forms a resonant circuit respectively when the two switches are turned off, the resonant voltage will cause unbalance voltage stress across the switches when the values of the two inductors L_1&L_2 are unequal, which results in overvoltage stress across the switches. However, this problem does not appear in the proposed converter. Considering the existence of parasitic capacitors, the equivalent circuit of the proposed converter in mode II is shown in Fig. 9 and Fig. 10.

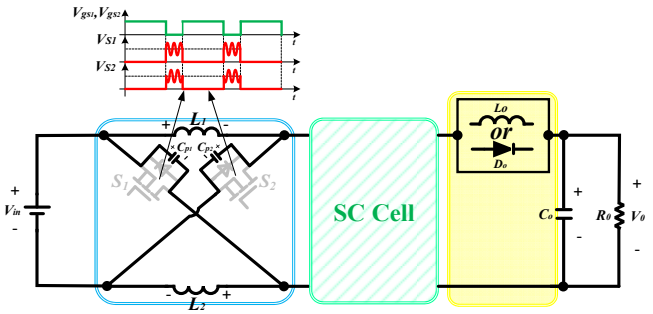


Fig. 8. Voltage unbalance problem on switches S_1&S_2 of the converters in [19]-[21], [23]-[25], [27].

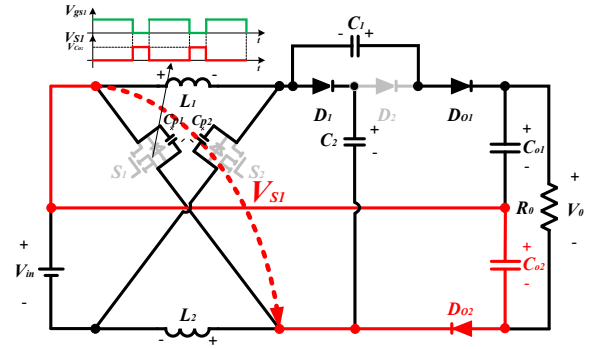


Fig. 9. The principle of voltage balance on switch S_1.

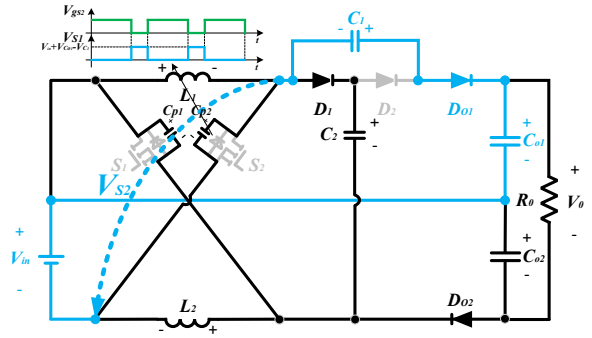


Fig. 10. The principle of voltage balance on switch S_2.

Because the voltage of the capacitors cannot be changed suddenly, the voltage of S_1 is clamped by C_{o2} when the two switches are turned off, which is shown in the red circuit loop of Fig. 9. The principle of voltage balance on switch S_2 is shown in Fig. 10 (blue circuit loop), the voltage of S_2 is clamped by C_1 and C_{o1} when the two switches are turned off. So, the voltages of S_1 and S_2 in mode II are given by

$$\begin{cases} V_{S1}=V_{C_{O2}} \\ V_{S2}=V_{in}+V_{C_{O1}}-V_{C_1} \end{cases} \tag{29}$$

In addition, due to the capacitors clamping structure, whether the values of the two inductors L_1 and L_2 are the same or not, the voltages of the two inductors in two modes can be written as

$$\begin{cases} V_{L1}^{\mathrm{I}}=V_{in},\ V_{L1}^{\mathrm{II}}=V_{C1}-V_{Co1} \\ V_{L2}^{\mathrm{I}}=V_{in},\ V_{L2}^{\mathrm{II}}=V_{in}-V_{Co2} \end{cases} \tag{30}$$

Combining (10) and (30), the voltage-second balance principles on two inductors are given by

$$\begin{cases} V_{in}\cdot D+(V_{C1}-V_{Co1})\cdot(1-D)=0 \\ V_{in}\cdot D+(V_{in}-V_{Co2})\cdot(1-D)=0 \end{cases} \tag{31}$$

By simplifying (31)

$$V_{Co2}=V_{in}+V_{Co1}-V_{C1} \tag{32}$$

According to (29) and (32), the relationship between the voltage of S_1 and the voltage of S_2 can be derived as

$$V_{S1}=V_{S2} \tag{33}$$

Also, as shown in Fig. 9 and Fig. 10, the voltages of junction capacitors C_{p1} and C_{p2} are given by

$$\begin{cases} V_{Cp1}=V_{Co2} \\ V_{Cp2}=V_{in}+V_{Co1}-V_{C1} \end{cases} \tag{34}$$

The voltages of inductors L_1 and L_2 are given by

$$V_{L1}=V_{L2}=\left(V_{in}-V_{C2}\right)/2 \tag{35}$$

Due to the voltages of capacitors C_1, C_2, C_{o1}, C_{o2} and input voltage are constant, according to (34) and (35), the voltages of two inductors and two capacitors are constant. Therefore, there is no resonance occur between junction capacitors and inductors, the voltages of two switches are constant in mode II and there is no voltage oscillation on two switches.

Therefore, in CCM, the proposed converter has the characteristic of voltage balance on two switches whether the two inductors are the same or not.

In DCM, according to the equivalent circuit of the proposed in mode III, it can be concluded that the theoretical voltage of the two switches is equal to V_{in}, and equivalent circuit of the proposed converter is similar to the converter in [21]. In mode III, the switches voltage will not be clamped by the capacitors clamp structure, the source voltage, inductor and the parasitic capacitor across the switch will be in resonance and spikes will occur. However, although the self-balancing will be lost in mode III, the voltage oscillation amplitude will not exceed the voltage of the switch $[(V_{in}+V_0)/4]$ of mode II, this is because the output diode will turn on when the switches voltage is higher than the switch voltage $[(V_{in}+V_0)/4]$ of mode II, and the capacitors clamp loop can be worked, which leads to the voltage of switches can be clamped again. The switches voltage stress depends on the maximum voltage, due to the voltage oscillation amplitude will not exceed the voltage stress value in mode II, so the voltage stress of switches in CCM and DCM are the same. In DCM, the switches voltage stress is not affected by the voltage oscillation in mode III, the switches voltage stress is also equal to $(V_{in}+V_0)/4$.

G. Voltage stress on the power components

Based on the analysis of the operation principle in section A, the voltage stresses on two switches S_1 and S_2 are given by

$$V_{S1}=V_{S2}=\frac{V_{in}}{1-D}=\frac{V_0}{3+D} \tag{36}$$

The voltage stresses on two diodes D_1 and D_2 are given by

$$V_{D1}=V_{D2}=\frac{2V_{in}}{1-D}=\frac{2V_0}{3+D} \tag{37}$$

The voltage stresses on two output diodes D_{o1} and D_{o2} are given by

$$V_{D_{O1}}=V_{D_{O2}}=\frac{V_{in}}{1-D}=\frac{V_0}{3+D} \tag{38}$$

From (36)-(38), we can deduce that the voltage stresses on all the power components in the proposed converter are much lower than output voltage V_0.

H. Current stress across the power components

In order to facilitate the analysis and calculation, internal resistors of all components and the current ripple are neglected. According to the analysis of CCM operation, the rms current value of power components can be approximately written as

$$I_{rms}\approx\sqrt{\frac{1}{T_s}\left(\int_0^{DT_S}\left(I_{avg}^{\mathrm{I}}\right)^2dt+\int_{DT_S}^{T_S}\left(I_{avg}^{\mathrm{II}}\right)^2dt\right)} \tag{39}$$

Combining (14), (16) and (39), the rms current values across the switches S_1 and S_2 are given by

$$\begin{aligned} I_{S1(rms)}=I_{S2(rms)}&\approx\sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(I_L+I_{D_2}^1\right)^2dt} \\ &=\sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(\frac{2I_0}{1-D}+\frac{I_0}{D}\right)^2dt}=I_0\sqrt{D}\left(\frac{2}{1-D}+\frac{1}{D}\right) \end{aligned} \tag{40}$$

The detailed calculation process for the rms current value of the switch is given in Appendix A.

Combining (14) and (39), the rms current value across the diode D_2 is given by

$$I_{D_2(rms)}\approx\sqrt{\frac{1}{T}\int_0^{DT_s}\left(I_{D_2}^1\right)^2dt}=\sqrt{\frac{1}{T}\int_0^{DT_s}\left(\frac{I_0}{D}\right)^2dt}=I_0\sqrt{\frac{1}{D}} \tag{41}$$

Combining (15) and (39), the rms current values across the diode D_1 and output diodes D_{o1}& D_{o2} are given by

$$I_{D_1(rms)}=I_{D_{o1}(rms)}=I_{D_{o2}(rms)}\approx\sqrt{\frac{1}{T}\int_{DT_s}^{T_s}\left(\frac{I_0}{1-D}\right)^2dt}=I_0\sqrt{\frac{1}{1-D}} \tag{42}$$

III. Comparison Analysis

Table. II shows the comparison of the proposed converter with other similar nonisolated step-up converters in the aspects of voltage gain, ideal switches voltage stress, output diodes voltage stress, components count and voltage oscillation on switches. As can be seen in Table. II and Fig. 11(a)&(b)&(c), the voltage gain of the proposed converter is the highest among these similar nonisolated step-up converters for the whole duty cycle range and the proposed converter has the lowest voltage stress on switches and lowest output diodes voltage stress.

As shown in Table. II, for traditional ASL converter [18] and its derivative hybrid SL/ASL converters [33], SC/ASL converters [19-21], [24], when the values of inductors L_1 and L_2 are different, resonant voltage occurs across two switches, which results in unbalanced voltage stress across the switches and voltage oscillations on the switches appear. The switches voltage stress values are higher than their ideal theoretical values. However, the proposed converter has no voltage oscillations on two switches due to the capacitors clamp structure composed of its own input and output capacitors. The resonant can be suppressed and the switches voltage stress of the proposed converter is equal to the ideal theoretical value. Therefore, although the switches voltage stress of the proposed converter, the SC-ANC converter [20] and ASL-SU2C-VO converter [21] are all the lowest, in practice, the proposed converter has lower voltage stress on switches.

It should be noted that the SC-ANC [20] and ASL-SU2C-VO [21] converters have the same voltage gain as the proposed converter. However, these two converters have voltage oscillation on switches, which leads to the voltage stress on switches is higher than proposed converter. Also, the output

diodes voltage stress of the proposed converter is half of that of these two converters.

In the aspect of cost comparison, the costs of the inductors, diodes and capacitors the proposed converter are similar to that of converter [21]. However, due to the proposed converter has lower voltage stress on switches, so, a lower voltage stress MOSFETs with smaller ON-resistance (R_{on}) can be used in the proposed converter, which leads to the switches cost of the proposed converter is less than that of the converter [21]. Also, to reduce the switches voltage oscillation in converter [21], the RC snubber circuits are needed, however, the RC snubber circuits are not used in the proposed converter, the proposed converter uses its own input and output capacitors to suppress the voltage oscillation. Because of this, the proposed converter reduces the cost of using the snubber circuits. Due to the voltage stress on switches and output diodes are reduced, the created heat is decreased, and the cost of radiator is reduced.

The proposed converter has one more output capacitor than converter [21], but in general, because the output voltage is high, two low voltage stress capacitors in series can be used in place of one high voltage stress capacitor. Therefore, the capacitor count of both two converters is similar. Also, the two output capacitors of the proposed converter are not only the output filters, but also a part of the capacitors clamp structure. The switches voltage can be clamped by the input voltage and the voltages of two output capacitor, the capacitor clamp structure is composed of its own input and output capacitors without adds additional capacitors. Therefore, the stacked capacitor architecture in the proposed converter will not affect the controller of the converter, the proposed converter can use the same digital controller as the converter [21].

In brief, the merits of the proposed converter are high voltage gain, lower voltage stress on switches, lower voltage stress on output diodes, and lower costs.

IV. Design Considerations

In order to verify the performance of the proposed converter accurately in the experiment, some design considerations need to be discussed. The proposed converter is designed to operate in CCM operation, and the detailed designs of all components are as follows.

(1) Selection of Duty cycle: according to the CCM voltage gain expression (11), the selection of duty cycle is given by

$$D = \frac{G_{CCM} - 3}{G_{CCM} + 1} \tag{43}$$

(2) Inductors Design: the inductor current ripple Δi_L can be written as

$$\Delta i_L = \frac{V_{in} D}{L f_S} = \frac{V_0 (1-D) D}{(3+D) L f_S} \tag{44}$$

where f_S is switching frequency.

Therefore, the inductor values of L_1 and L_2 are given by

$$L_1 = L_2 \geq \frac{V_0 (1-D) D}{(3+D) \Delta i_L f_S} \tag{45}$$

(3) Capacitors Design: according to the theoretical analysis in section II, the capacitors voltage stresses are given by

$$\begin{cases} V_{C_{O1}} = \dfrac{(2+D)V_0}{3+D}, V_{C_{O2}} = \dfrac{V_0}{3+D} \\ V_{C1} = \dfrac{2V_0}{3+D}, V_{C2} = \dfrac{(1+D)V_0}{3+D} \end{cases} \tag{46}$$

According to ref. [34], the power loss of the switched-capacitor can be reduced when the current level is decreased. Also, the two capacitors of SC cell are charged and discharged in two operation modes, therefore, the switched capacitors should be designed in the operation of partial charge.

In mode I, the capacitor C_1 is charged, according to the analysis in ref. [34], the capacitor C_1 can be calculated by

$$C_1 \geq \frac{0.1}{R_{eq1} f_S} \tag{47}$$

where R_{eq1} is the sum of resistor of switches, capacitors and diodes in mode I.

In mode II, the capacitor C_2 is charged, the capacitor C_2 can be calculated by

$$C_2 \geq \frac{0.18}{R_{eq2} f_S} \tag{48}$$

where R_{eq2} is the sum of resistor of capacitors and diodes in mode II.

Finally, the output capacitors can be given by

$$\begin{cases} C_{O1} \geq \dfrac{I_0 (1-D)}{\Delta v_{C_{O1}} f_S} \\ C_{O2} \geq \dfrac{I_0 (1-D)}{\Delta v_{C_{O2}} f_S} \end{cases} \tag{49}$$

where $\triangle v_{CO1}$, $\triangle v_{CO2}$ are capacitors voltage ripples.

(4) Selection of power components: the voltage stresses on power components are discussed in section G, the current stresses across power components are discussed in section H. Therefore, power components can be selected according to expression (36)-(42).

Based on the above analysis, the values of storage components and the selection of power components are shown in Table. I.

TABLE I
Experiment Parameters

Components	Parameters
Input voltage V_{in}	25-45V
Output voltage V_o	380V
Rated power P_0	200W
Switching frequency f_s	50kHz
Inductors L_1, L_2	240μH (both two converters)
MOSFETs S_1, S_2	150V-SE150180GTS (proposed converter) 200V-NCE0275T (converter in ref. [21])
Diodes D_1, D_2	300V-SFAF805GC0G (both two converters)
Output diodes D_{01}, D_{02}	150V-MBR20H150CTG (proposed converter)
Output diodes D_0	300V-SFAF805GC0G (converter in ref. [21])
Input capacitors	820μF/50V &CBB 2μF (both two converters)
Capacitors C_1, C_2, C_{o1}, C_{o2}	22μF (film capacitor, proposed converter)
Capacitors C_1, C_2, C_o	22μF (film capacitor, converter in ref. [21])

TABLE II
COMPARISON WITH OTHER SIMILAR NONISOLATED STEP-UP CONVERTERS

Converters	Voltage Gain (G_{CCM})	Ideal Switches voltage Stress (V_S/V_0)	Output Diodes voltage Stress (V_D/V_0)	Switches Count	Diodes Count	Inductors Count	Capacitors Count	Voltage Oscillation on Switches
Proposed	$\frac{3+D}{1-D}$	$\frac{1}{3+D}$	$\frac{1}{3+D}$	2	4	2	4	No
Converter I in [18]	$\frac{1+D}{1-D}$	$\frac{1}{1+D}$	$\frac{1}{1+D}$	2	2	2	4	Yes
Converter III in [18]	$\frac{3-D}{1-D}$	$\frac{1}{3-D}$	$\frac{2}{3-D}$	2	3	2	3	Yes
ASL-SU2C-CO [19]	$\frac{1+3D}{1-D}$	$\frac{1}{1+3D}$	—	2	2	3	3	Yes
SC-ANC [20]	$\frac{3+D}{1-D}$	$\frac{1}{3+D}$	$\frac{2}{3+D}$	2	3	3	3	Yes
ASL-SU2C-VO [21]	$\frac{3+D}{1-D}$	$\frac{1}{3+D}$	$\frac{2}{3+D}$	2	3	2	3	Yes
Converter [24]	$\frac{1+3D}{1-D}$	$\frac{1}{1+3D}$	—	2	2	3	3	Yes
SC-Boost [28]	$\frac{2}{1-D}$	$\frac{1}{2}$	$\frac{1}{2}$	2	3	2	3	No
SL-Boost [29]	$\frac{1+D}{1-D}$	1	1	1	4	2	1	No
HBC [30]	$\frac{3-D}{1-D}$	$\frac{1}{3-D}$	—	1	4	1	4	No
Group E (N=2) in [31]	$\frac{3}{1-D}$	$\frac{1}{3}$	$\frac{1}{3}$	2	3	2	3	No
Converter in [32]	$\frac{2}{1-D}$	$\frac{1}{2}$	—	4	0	2	4	No
SH-SLC [33]	$\frac{1+3D}{1-D}$	$\frac{1+D}{1+3D}$	$\frac{2+2D}{1+3D}$	2	7	4	1	Yes
AH-SLC [33]	$\frac{1+2D}{1-D}$	$\frac{\frac{1+D}{1+2D}}{\frac{1}{1+2D}}$	$\frac{2+D}{1+2D}$	2	4	3	1	Yes

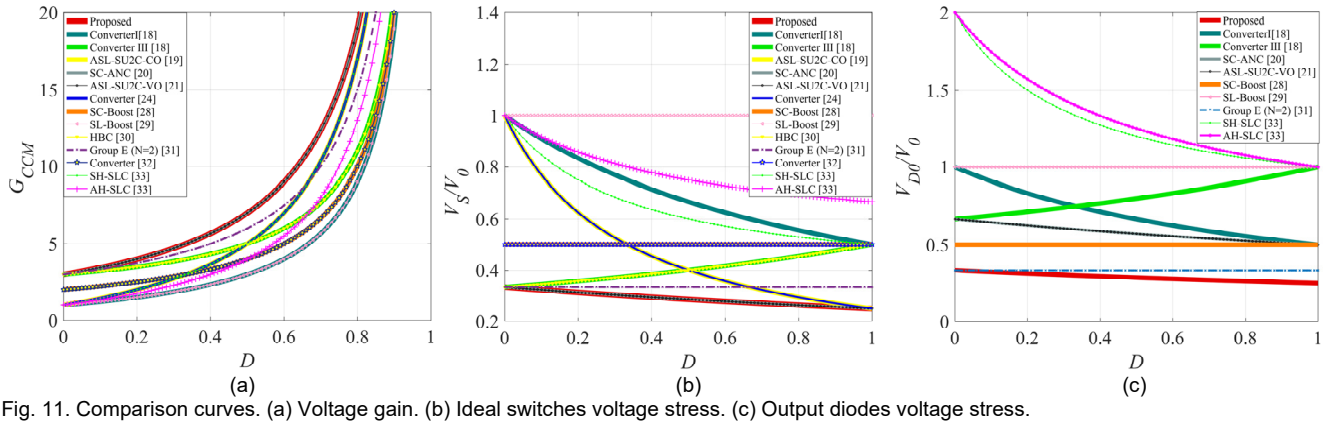


Fig. 11. Comparison curves. (a) Voltage gain. (b) Ideal switches voltage stress. (c) Output diodes voltage stress.

V. EXPERIMENTAL RESULTS

To evaluate the performance of the proposed ASL-SC-2OD converter, an experimental prototype (Fig. 12) was built in the laboratory, and the experimental prototype of ASL-SU2C-VO converter in [21] was also built to compare with the proposed converter. The two experimental prototypes were tested in the same experimental conditions: input voltage V_{in} that ranges from 25 to 45V, the output voltage V_0 is 380V, the switching frequency f_s is 50 kHz, and the rated power is 200W. According to the analysis in section II, both two converters have the same voltage gain and the same voltage stress on SC diodes, the switches voltage stress and output diodes voltage stress of both two converters are different. So, 150V MOSFET SE150180GTS and 150V output diodes MBR20H150CTG are utilized for the proposed converter, 200-V MOSFET NCE0275T and 300V output diode SFAF805GC0G are utilized for the ASL-SU2C-VO converter in [21]. 300V SC diodes SFAF805GC0G are utilized for both two converters. The main

components and parameters of the converters are summarized in Table I.

The proposed converter has simple operation and the ability to realize self-balance on switches. Therefore, the proposed converter does not need complicated closed loop control logic. The proposed converter adopts the closed-loop control strategy of single voltage loop, as shown in Fig. 13, the voltage Vo is controlled by the voltage controller with the reference voltage V_{ref} in the voltage loop, and the digital signal is transmitting to the PI regulator, then output the synchronous PWM gate signals of S_1 and S_2 by PWM generator.

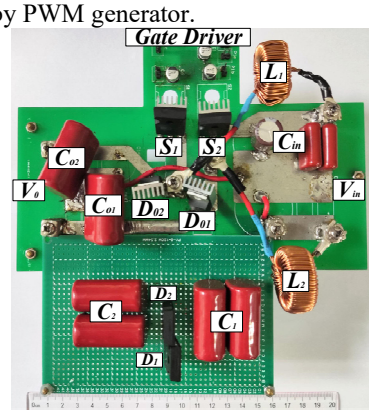


Fig. 12. Experimental prototype.

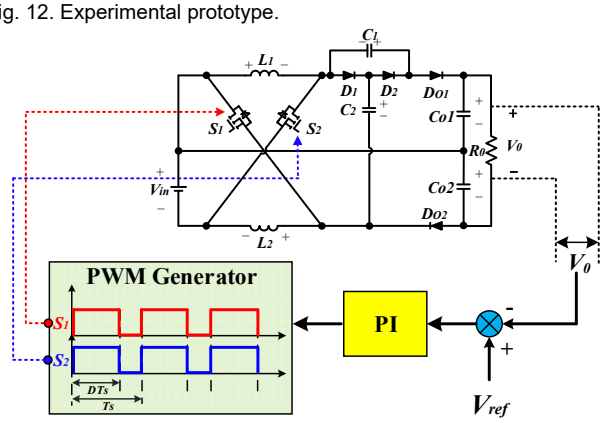
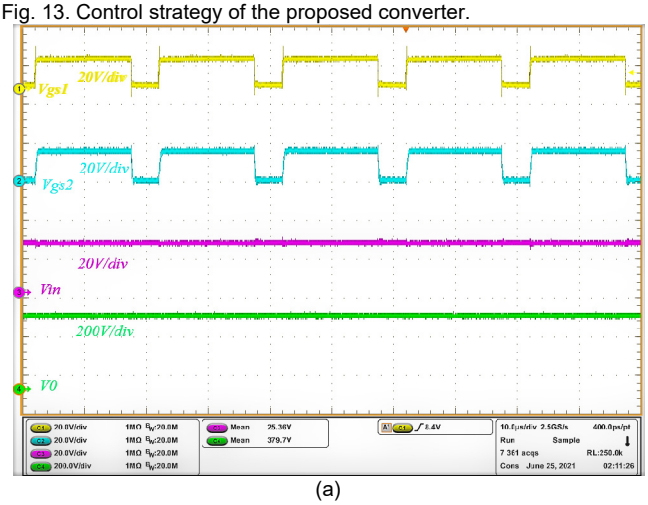
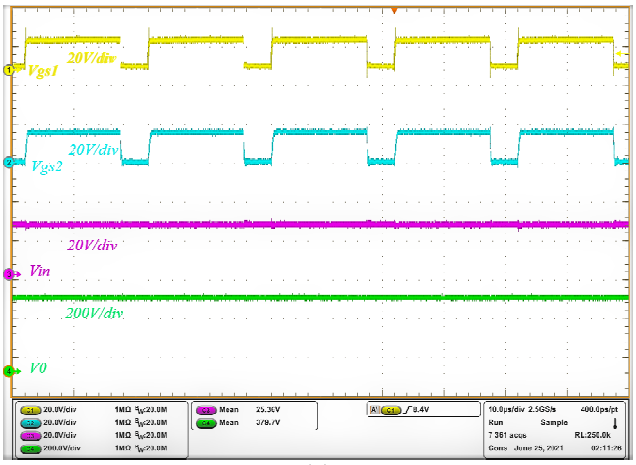


Fig. 13. Control strategy of the proposed converter.

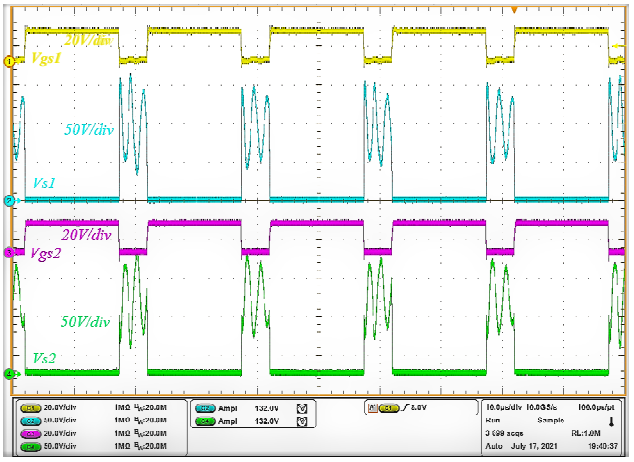


(a)

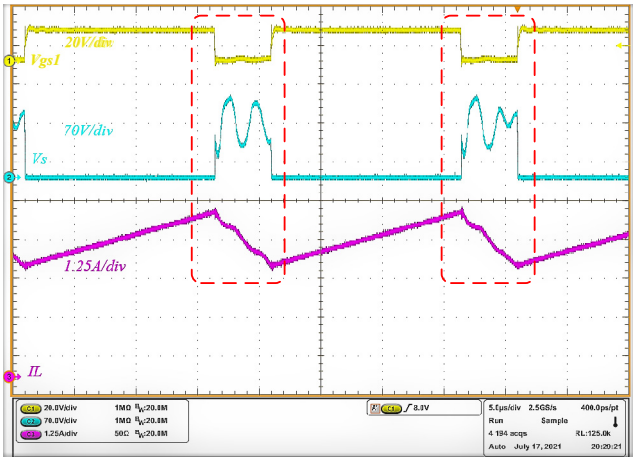


(b)

Fig. 14. (a) Gate-source signals (V_{gs1}, V_{gs2}) and input and output voltage (V_{in} and V_0) of the converter in [21]. (b) V_{gs1}, V_{gs2} and input and output voltage (V_{in} and V_0) of the proposed converter. Time (10 μs/div).

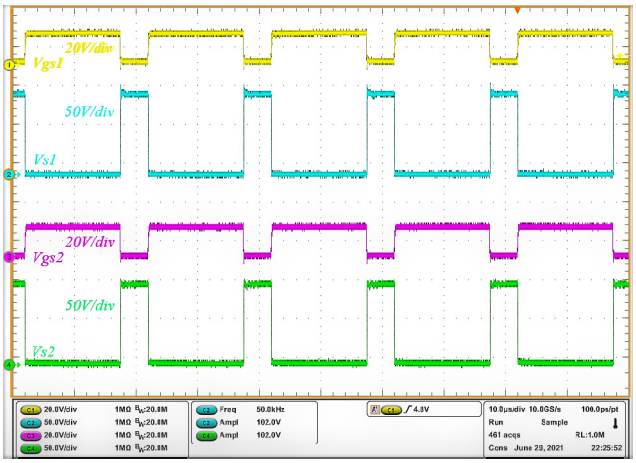


(a)

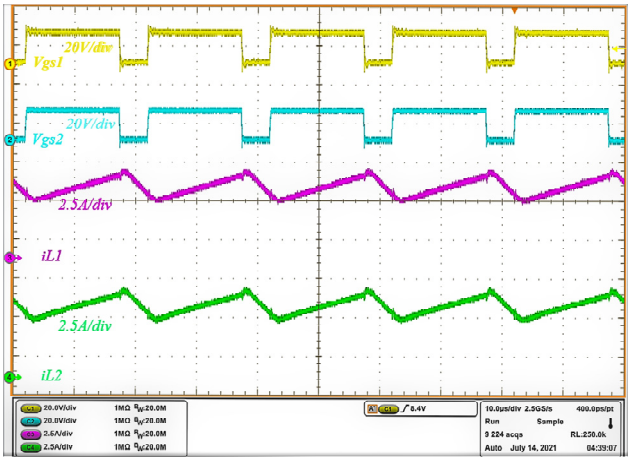


(b)

Fig. 15. (a) Gate-source signals (V_{gs1}, V_{gs2}) and Drain-source voltages (V_{S1} and V_{S2}) of the converter in [21]. (b) V_{gs1}, V_S and inductor current i_L of the converter in [21].



(a)



(b)

Fig. 16. (a) Gate-source signals (V_{gs1}, V_{gs2}) and drain-source voltages (V_{S1} and V_{S2}) of the proposed converter. (b) V_{gs1}, V_{gs2} and inductor currents (i_{L1} and i_{L2}) of the proposed converter.

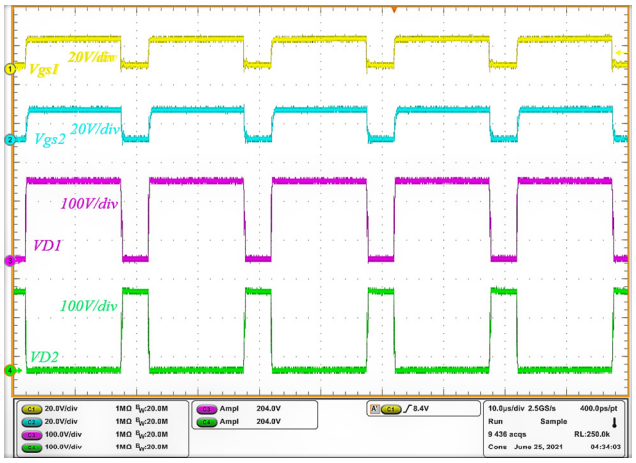


Fig. 17. Gate-source signals (V_{gs1}, V_{gs2}) and diodes voltages (V_{D1} and V_{D2}) of the proposed converter. Time (10 μs/div).

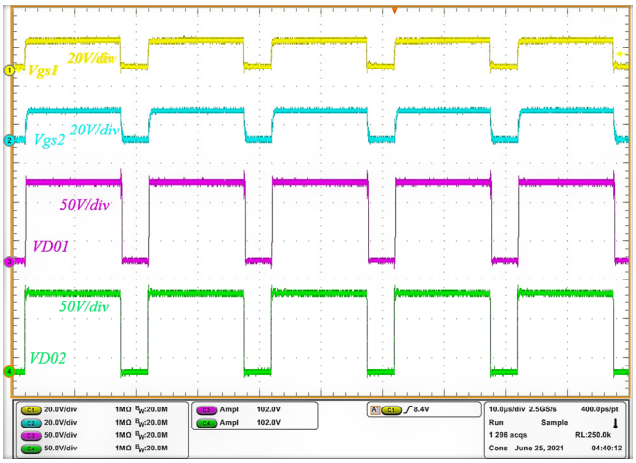


Fig. 18. Gate-source signals (V_{gs1}, V_{gs2}) and output diodes voltages (V_{D01} and V_{D02}) of the proposed converter. Time (10 μs/div).

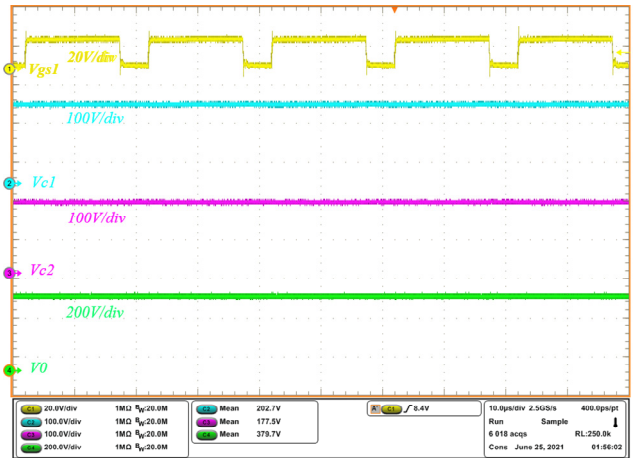


Fig. 19. Gate-source signal V_{gs1}, capacitors voltages (V_{C1} and V_{C2}) and output voltage V_0 of the proposed converter. Time (10 μs/div).

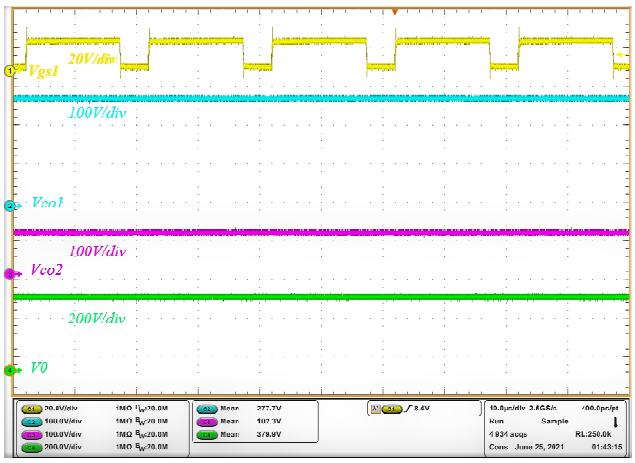


Fig. 20. Gate-source signal V_{gs1}, capacitors voltages (V_{CO1} and V_{CO2}) and output voltage V_0 of the proposed converter. Time (10 μs/div).

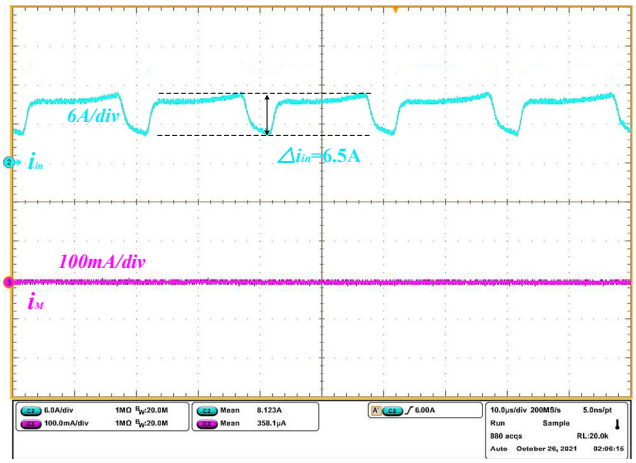


Fig. 21. The experiment waveforms of input current i_{in} and the middle line current i_M.

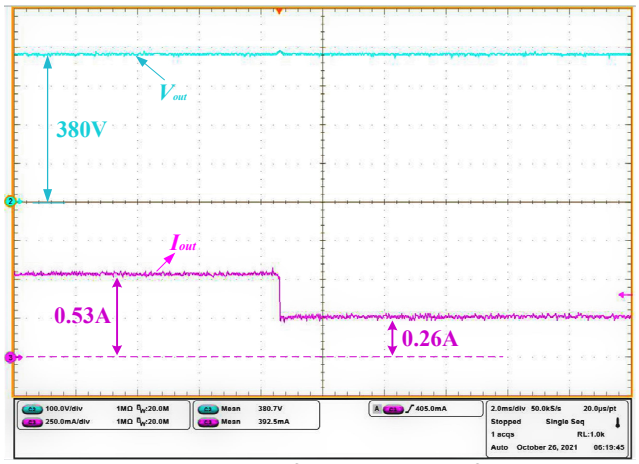


Fig. 24. The dynamic response of the output voltage for changes in load from 200W to 100W.

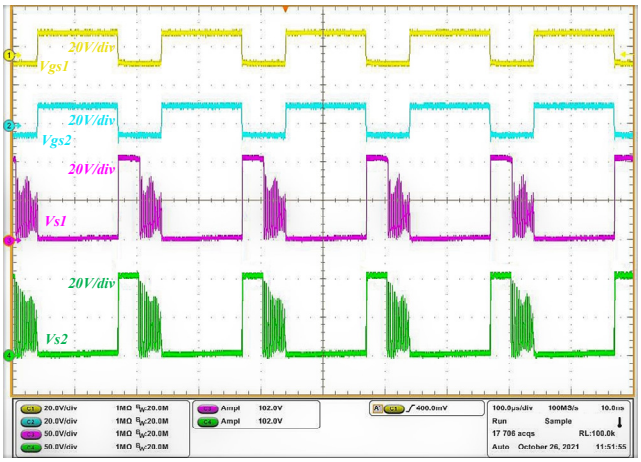


Fig. 22. Gate-source signals (V_{gs1}, V_{gs2}) and drain-source voltages (V_{S1} and V_{S2}) of the proposed converter in DCM.

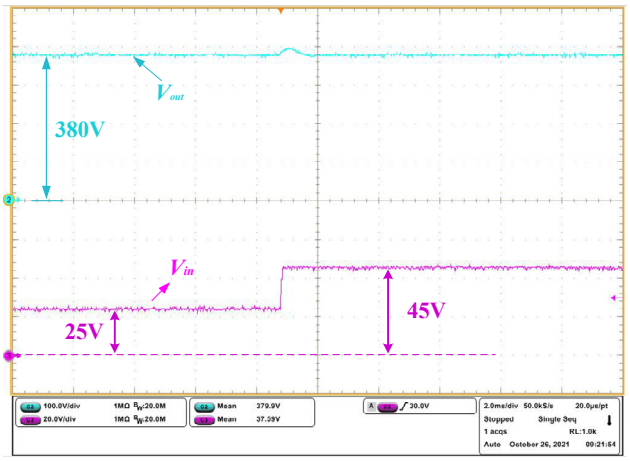


Fig. 25. The dynamic response of the output voltage for changes in load from input voltage 25V to 45V.

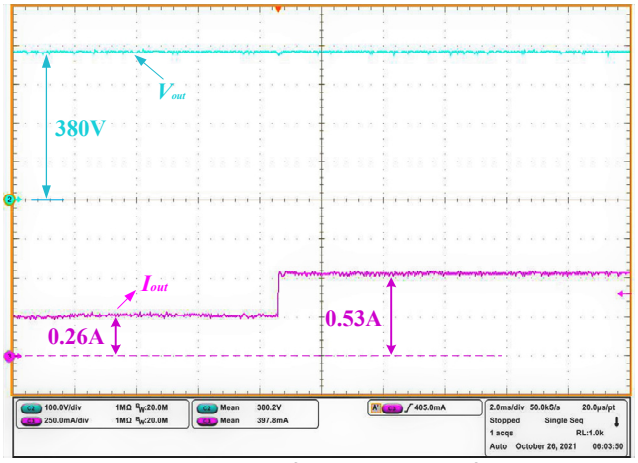


Fig. 23. The dynamic response of the output voltage for changes in load from 100W to 200W.

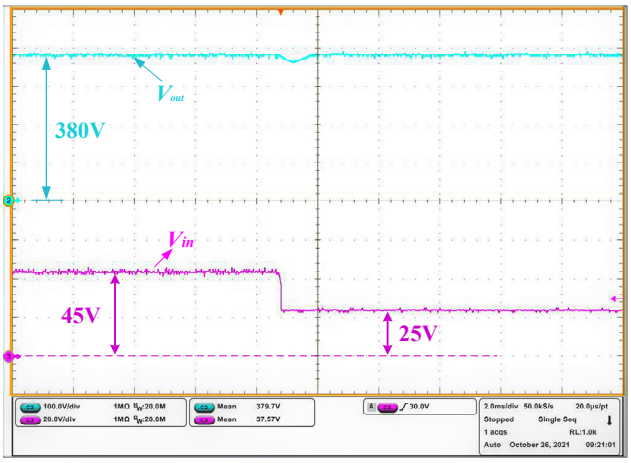


Fig. 26. The dynamic response of the output voltage for changes in load from input voltage 45V to 25V.

As shown in Fig. 14(a)&(b), the converter in [21] and the proposed converter were tested in the same duty cycle, and the two switches are turned on and off simultaneously. The output voltage V_0 of both converters is 380V when the input voltage is 25V, so both converters have the same voltage gain.

Fig. 15(a) shows gate source signals (V_{gs1} and V_{gs2}) and drain source voltages (V_{S1} and V_{S2}) of the converter in [21]. The experimental conditions are the input voltage is 25V and the output voltage is 380V. Obviously, the converter in [21] has voltage oscillation on switches, and the voltage stress on switches is 132V, which is higher than 102V (ideal switches voltage stress is $(V_{in}+V_0)/4$). Fig. 15(b) shows gate source signals V_{gs1}, drain source voltages V_S, and the inductor current i_L of the converter in [21], the inductor current is also in the resonance obviously.

Fig. 16(a) shows gate source signals (V_{gs1} and V_{gs2}) and drain source voltages (V_{S1} and V_{S2}) of the proposed converters. The proposed converter has no voltage oscillation on switches, the switches voltage stress $V_{S1}=V_{S2}=102$V, which is equal to ideal switches voltage stress ($(V_{in}+V_0)/4$). So, the voltage stress on switches is lower and the proposed converter can achieve self-voltage balance on two switches. Fig. 16(b) shows V_{gs1} and V_{gs2}, the inductor currents (i_{L1} and i_{L2}) of the proposed converter. Obviously, the resonate of inductor currents is also suppressed. It should be noted that the shown resonance frequency in ref. [21] is lower than the resonance frequency in this paper. We have analyzed the resonance frequency values mathematically and the mathematical procedures are shown in Appendix B.

Fig. 17 shows V_{gs1} and V_{gs2} and the diodes voltages (V_{D1} and V_{D2}), $V_{D1}=V_{D2}=204$V. Fig. 18 shows V_{gs1} and V_{gs2} and the output diodes voltages (V_{D01} and V_{D02}), $V_{D01}=V_{D02}=102$V. Fig. 19 shows V_{gs1}, capacitors voltages (V_{C1} and V_{C2}) and output voltage V_0, $V_{C1}=203$V, $V_{C2}=177$V and $V_0=380$V. Fig. 20 shows V_{gs1}, capacitors voltages (V_{CO1} and V_{CO2}) and output voltage V_0, $V_{CO1}=278$V, $V_{CO2}=102$V and $V_0=380$V, so the voltage stresses on two output capacitors are lower than output voltage.

As can be seen in Fig. 21, the input current waveform is consistent with the theoretical analysis in section E, the input current ripple value is 6.5A, and the middle line current is approximately zero.

Fig. 22 shows the waveforms of two gate-source signals and the voltage of two switches in DCM operation in the condition of input voltage is 25V and output voltage is 380V. The voltage stress on the two switches is $V_{S1}=V_{S2}=102$V, which is equal to switches voltage stress in CCM. Although the self-balancing is lost in mode III, the voltage oscillation amplitude will not exceed the voltage of the switch 102V [$(V_{in}+V_0)/4$] of mode II, so the voltage oscillation in DCM will not affect the switch voltage stress value.

The dynamic response of the output voltage for changes in load from half load 100W to the nominal load 200W is shown in Fig. 23. The dynamic response of the output voltage for changes in load from nominal load 200W to the half load 100W is shown in Fig. 24. As can be seen from the waveforms of output current and output voltage, the output current changes in a step wise manner and the output voltage can be maintained at 380V when the load sudden changes under the designed voltage closed-loop control.

The dynamic response of the output voltage for changes from input voltage 25V to 45V is shown in Fig. 25, the output voltage for changes from input voltage 45V to 25V is shown in Fig. 26. Also, the output voltage can be maintained at 380V when the input voltage sudden changes under the designed voltage closed-loop control. Therefore, the proposed converter has good dynamic characteristics.

The experimental waveforms are all similar to the theoretical waveforms and the experimental values are equal to the theoretical values, which verifies the correctness of theoretical analysis in section II.

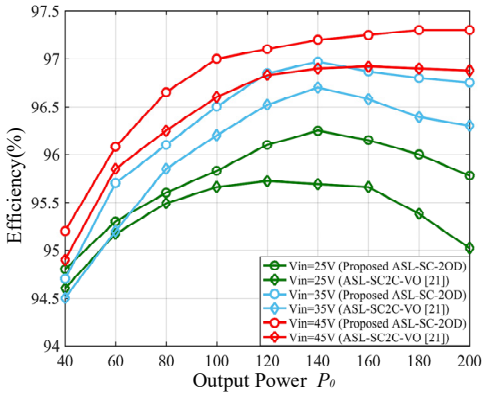


Fig. 27. Experimental efficiency curves.

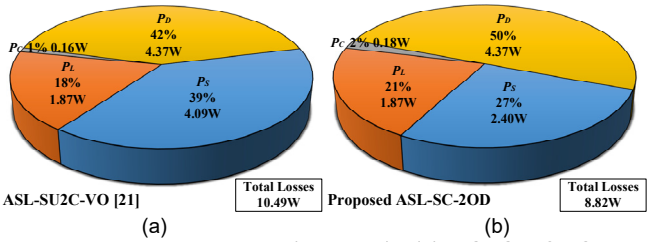


Fig. 28. Losses distribution (P_0=200W). (a) ASL-SU2C-VO [21], efficiency≈95.02%. (b) Proposed ASL-SC-2OD, efficiency≈95.78%.

Fig. 27 shows the experimental efficiency curves in the condition that input voltage is 25V, 35V, or 45V, output voltage is 380V. The experimental efficiency is measured by a Yokogawa power analyzer WT1800. The peak efficiency value of the ASL-SU2C-VO converter [21] is 96.92%, while the peak efficiency value of the proposed ASL-SC-2OD converter is 97.3%. The efficiency of ASL-SU2C-VO [21] at rated power 200W is 95.02%, 96.30% and 96.88% for input voltages of 25 V, 35 V and 45V, respectively, while for the proposed ASL-SC-2OD, these values are 95.78%, 96.75% and 97.30%.

Fig. 28 shows the calculated losses distribution for both converters in the condition that V_{in}=25V, V_0=380V and P_0=200W. The theoretical calculation method of the loss distribution is shown in Appendix. C. Although the proposed converter has one more capacitor and one more output diode than the ASL-SU2C-VO converter, the capacitor loss value is very low, and the output diode voltage stress (102V) of the proposed converter is half of that (204V) of the converter [21], so a lower forward voltage Schottky diodes MBR20H150CTG (v_f=0.45V) can be utilized in the proposed converter, the diodes loss for both converters is approximately equal. Compared with the ASL-SU2C-VO converter, the switches loss of the proposed converter is reduced by 1.69W, this is because the switches voltage stress (102V) of the proposed converter is lower than that (132V) of ASL-SU2C-VO converter, and lower voltage stress MOSFETs with smaller ON-resistance (R_{on}) are utilized in the proposed converter.

VI. Conclusion

In this paper, a novel high step-up SC/ASL converter was proposed (named ASL-SC-2OD). The proposed ASL-SC-2OD converter was analyzed in detail from operation principle, CCM analysis, CCM operation with unbalanced inductors, input current ripple analysis, DCM and BCM analysis, switches self-voltage balancing characteristic, voltage stress, current stress, comparison analysis, and design consideration. Finally, the correctness of the theoretical analysis was verified by experiments.

The proposed ASL-SC-2OD converter has high voltage gain (more than 15 times), and the operation principle is also simple. Compared with other similar nonisolated step-up converters, the proposed converter has lower voltage stresses on switches and output diodes, which leads to MOSFETs with smaller ON-resistance $R_{ds(on)}$ and lower voltage stress output diodes can be utilized, and the efficiency of the proposed converter can be improved. Also, the one output diode can help form a capacitor clamp loop to clamp the voltage of switch. In addition, unlike other SC/ASL step-up converters [19]-[21], the proposed converter can suppress the resonance and achieve self-voltage balancing on two switches due to the capacitors clamp structure. Meanwhile, the output capacitors are not only the output filters, but also a part of the capacitors clamp structure, and the output capacitors have lower voltage stress. The proposed converter also has the advantage of lower cost.

Based on the above merits, the proposed converter is more suitable for high step-up applications.

Appendix A. Calculation of rms Value of Switch Current

The inductor L_1 current, diode D_2 current and switch S_2 current of mode I is shown in Fig. 29. The simplified key waveforms in switching period are shown in Fig. 30.

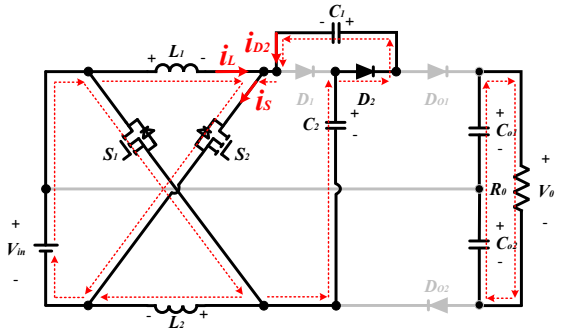


Fig. 29. Inductor L_1 current, diode D_2 current and switch S_2 current in mode I.

(1) The calculation of average current of diodes

In one switching cycle, the avg current of capacitor C_1, C_1, C_{o1}, C_{o2} is zero. Through the analysis of mode I and mode II, according to Kirchhoff's Current Law (KCL), the average currents of four diodes are equal and can be given by

$$I_{D_1} = I_{D_2} = I_{D_{O1}} = I_{D_{O2}} = I_0 \tag{50}$$

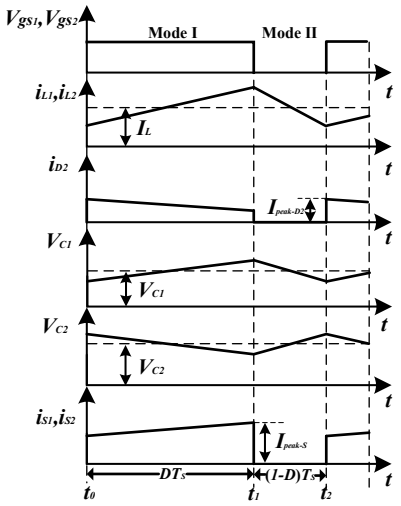


Fig. 30. Key waveforms in switching period.

(2) The calculation of rms current of the switches

According to Fig. 29, the switches current can be given by

$$i_S = i_L + i_{D2} \tag{51}$$

From the analysis of Fig. 29 and Fig. 30, the current of D_2 reaches its maximum at $t=nT_S$ (n is an integer), and the peak current of D_2 is given by

$$i_{peak-D2} = i_{D2(DT_S)} = \frac{V_{C1} + \Delta V_{C1} - (V_{C2} - \Delta V_{C2}) + V_{in} - V_d}{R} = \frac{\Delta V_{C1} + \Delta V_{C2} - V_d}{R} \tag{52}$$

where V_d is the forward voltage of D_2; R is the resistor of the circuit loop which is formed of V_{in}, S_1, S_2, C_1, D_2, and C_2. Compared with the internal resistance of the diode and the switches, the resistance of the capacitor is small and can be ignored, so the resistor of the circuit loop can be given by

$$R = 2R_{ds} + R_d \tag{53}$$

where R_{ds} is the resistor of the switches and R_d is the resistor of the diodes. From (50) and (52), we can deduce i_{D2} during the time interval $[nTs \sim (n + D)Ts]$.

$$i_{D2} = i_{D2(nT_S)} - 2 \cdot \frac{i_{D2(nT_S)} - \frac{I_0}{D}}{DT_s} \cdot (t - nT_S) \tag{54}$$

The inductor current during the time interval $[nTs \sim (n + D)Ts]$ can be given by

$$i_{D2} = I_L - \frac{1}{2}\Delta i_L + \frac{\Delta i_L}{DT_S}(t - nT_S) \tag{55}$$

In mode I, the current pass the switches, and from (51) and (55), the rms switches current is given by (56) as shown at the top of the next page.

Assuming the values of C_1, C_2, and L are large enough, the voltage and current ripples are small. According to (52) and (53), the current through D_2 during the time $[nTs \sim (n + D)Ts]$ can be considered as a constant value, and the current value of D_2 can be simplified in (57).

$$I_{\mathrm{S1(rms)}} = I_{\mathrm{S2(rms)}} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_S^2 dt} = \sqrt{\frac{1}{T_S}\int_0^{T_S} \left(i_L + i_{D2}\right)^2 dt}$$
$$= \sqrt{D\left[\frac{4I_0^2}{(1-D)^2} + \frac{1}{12}\Delta i_L^2 + \frac{1}{3}\Delta i_L i_{D2(T_S)} - \frac{1}{3}\Delta i_L \frac{I_0}{D} + 2\frac{2I_0}{1-D}\frac{I_0}{D} + \frac{1}{3}i_{D2(T_S)}^2 - \frac{2}{3}i_{D2(T_S)}\frac{I_0}{D} + \frac{4}{3}\frac{I_0^2}{D^2}\right]} \quad (56)$$
$$= \sqrt{D[4I_0^2\frac{D^2+D+1}{3D^2(1-D)^2} + \frac{1}{12}\frac{D^2(1-D)^2V_0^2}{(3+D)^2L^2f_S^2} + \frac{1}{3}\frac{D(1-D)V_0}{(3+D)Lf_S}i_{D2(T_S)} - \frac{1}{3}\frac{D(1-D)V_0}{(3+D)Lf_S}I_0 + \frac{1}{3}i_{D2(T_S)}^2 - \frac{2}{3}i_{D2(T_S)}\frac{I_0}{D}}$$

$$i_{peak-D2} = i_{D2(nT_S\sim(n+D)T_S)} = \frac{I_0}{D} \quad (57)$$

Therefore, from above, the rms current of switches is given by

$$I_{S1(rms)} = I_{S2(rms)} = \sqrt{\frac{1}{T_S}\int_0^{T_S} i_S^2 dt} = \sqrt{\frac{1}{T_s}\int_0^{DT_s} \left(i_L + i_{D2}\right)^2 dt}$$
$$\approx \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(I_L + \frac{I_0}{D}\right)^2 dt} = I_0\sqrt{D}\left(\frac{2}{1-D} + \frac{1}{D}\right) \quad (58)$$

Appendix B. Calculation of The Resonant Frequency of the Converter [21]

The experimental resonance frequency in ref. [21] is lower than the resonance frequency in this paper. We have analyzed the resonance frequency values mathematically and the mathematical procedures are as follows.

(1) The resonance frequency of converter [21] in this paper

In this paper, the inductors and switches junction capacitors values are shown below.

$$\begin{cases} L_1 = L_2 = 240\mu\mathrm{H} \\ C_{p1}{=}C_{p1}{=}476\mathrm{pF} \end{cases}$$

According to the formula of resonance frequency, the calculated resonance frequency of converter [21] which is shown in this paper is given by

$$f_{calculated} = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} = \frac{1}{2\pi}\sqrt{\frac{1}{C_{p1}+C_{p2}}\cdot\frac{L_1+L_2}{L_1L_2}} = 4.71\times10^5\ \mathrm{Hz} \quad (59)$$

According to Fig. 15(a), as can be seen, the resonant period is 2.1μs, so the resonance frequency is given by

$$f_{experimental} = \frac{1}{T} = \frac{1}{2.1\times10^{-6}} = 4.71\times10^5\ \mathrm{Hz} \quad (60)$$

Therefore, the mathematical calculated value of resonant frequency is equal to the experimental resonant frequency value.

(2) The resonance frequency of converter [21] in ref. [21]

In ref. [21], the voltage waveforms of switches S_1 and S_2 are shown in Fig. r6, the resonant period is about 3μs. Therefore, the experimental resonant frequency is given by

$$f_{experimental} = \frac{1}{T} = \frac{1}{3\times10^{-6}} = 3.33\times10^5\ \mathrm{Hz} \quad (61)$$

So, compare with (60), the shown resonance frequency in ref. [21] is lower than the resonance frequency in this paper. In ref. [21], the experiment parameters of the inductors and junction capacitors values are

$$\begin{cases} L_1{=}L_2{=}223\mu\mathrm{H} \\ C_{p1}{=}C_{p1}{=}390\mathrm{pF} \end{cases}$$

The calculated resonance frequency of converter [21] which is shown in ref. [21] is given by

$$f_{calculated} = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} = \frac{1}{2\pi}\sqrt{\frac{1}{C_{p1}+C_{p2}}\cdot\frac{L_1+L_2}{L_1L_2}} = 5.40\times10^5\ \mathrm{Hz} \quad (62)$$

From (61) and (62), it can be deducted that the calculated resonance frequency is higher than the experimental resonant frequency. This is because the RC snubber circuit may be added in converter [21] in ref. [21], the actual equivalent capacitor is larger than junction capacitor, therefore, the calculated resonance frequency is higher than the experimental resonant frequency in ref. [21]

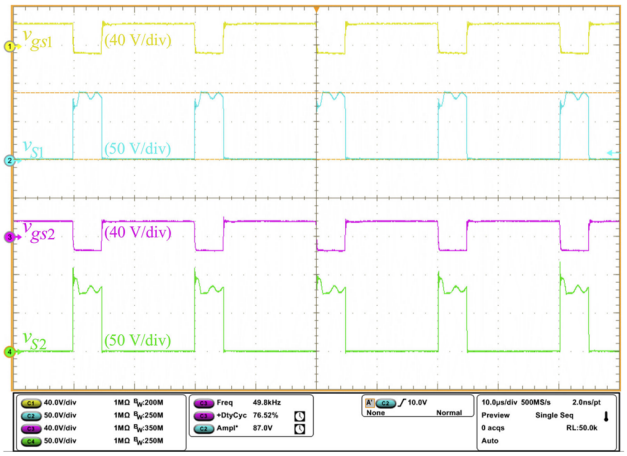


Fig. 31. Gate-source signals (V_{gs1}, V_{gs2}) and Drain-source voltages (V_{S1} and V_{S2}) of the converter in [21] in ref. [21].

Appendix C. Theoretical Calculation Method of The Loss Distribution

① Losses distribution analysis of the converter in ref. [21]

1) The losses of the switches can be divided into switching loss and conduction loss, and they can be calculated by:

$$P_S = 2[I_{S(rms)}{}^2 R_{on} + \frac{1}{2}f_S V_S I_S (t_{on} + t_{off})] \quad (63)$$

where Is(rms) is the RMS current of the switches and R_{on} is on-state resistor of the switches; fs is switching frequency; t_{on} and t_{off} are Turn-on time and Turn-off time, respectively; Vs is voltage stress of the switches and Is is the current of the switches during switching time.

2) The diodes loss distribution can be divided into conduction loss and reverse recovery loss. The diodes losses are given by

$$P_D = 2\left(I_{D_1(avg)} v_{D_1 f} + Q_{rD_1} V_{rD_1} f_S\right) + \left(I_{D_0(avg)} v_{D_0 f} + Q_{rD_0} V_{rD_0} f_S\right) \quad (64)$$

where I_D is the average current of the diodes and v_{Df} is the diode forward voltage, Q_r is the diode reverse recovery charge, V_r is the diode reverse turn-off voltage, and f_s is the switching frequency.

3) The inductors losses are given by

$$P_L = 2[r_L {I_{L(rms)}}^2 + (a {B_{pk}}^b {f_S}^c) A_e l_e] \quad (65)$$

where I_L(rms) is the RMS current of the inductor; r_L is copper resistance; B_{pk} is the AC magnetic flux density of the magnetic core; a, b, c are constants determined from the curve fitting of the core; l_e is the core medium path length and A_e is the transversal core area.

4) The capacitors losses can be given by

$$P_C = 2{I_{C_1(rms)}}^2 \cdot ESR + {I_{C_0(rms)}}^2 \cdot ESR \quad (66)$$

where $I_{C(\mathrm{rms})}$ is the RMS current of the capacitor and ESR is the resistor of capacitors.

So, the total losses P_{loss} can be written as

$$P_{loss} = P_S + P_D + P_L + P_C \quad (67)$$

② Losses distribution analysis of the proposed converter

Similarly, the loss calculation process of the proposed converter is shown below.

1) The losses of the two switches are given by

$$P_S = 2\left[{I_{S(rms)}}^2 R_{DS(on)} + \frac{1}{2} f_S V_S I_S (t_{on} + t_{off})\right] \quad (68)$$

2) The diodes losses are given by

$$P_D = \left(I_{D_1(avg)} v_{D_1 f} + Q_{rD_1} V_{rD_1} f_S\right) + \left(I_{D_2(avg)} v_{D_2 f} + Q_{rD_2} V_{rD_2} f_S\right) + 2 I_{D_{01}(avg)} v_{D_{01} f} \quad (69)$$

3) The inductors losses are given by

$$P_L = 2[r_L {I_{L(rms)}}^2 + (a {B_{pk}}^b {f_S}^c) A_e l_e] \quad (70)$$

4) The capacitors losses can be given by

$$P_C = 2{I_{C_1(rms)}}^2 \cdot ESR + 2{I_{C_0(rms)}}^2 \cdot ESR \quad (71)$$

The total losses P_{loss} can be written as

$$P_{loss} = P_S + P_D + P_L + P_C \quad (72)$$

The efficiency (η) can be determined as follows:

$$\eta = \frac{P_0}{P_0 + P_{loss}} \quad (73)$$

REFERENCES

[1] S. Arun, A. T. P. Imthias and Z. V. Lakaparampil, "Review and performance analysis of high step-up DC/DC converters for photovoltaic application," *2017 IEEE International Conference on Electrical, Instrumentation and Communication Engineering (ICEICE)*, DOI 10.1109/ICEICE.2017.8191853, pp. 1-5, 2017.

[2] A. J S, S. Suresh Kumar, J. P and U. Subramaniam, "Design and Analysis of a High Step-Up DC-DC Converter Fed Grid Connected Fuel Cell System," *2020 International Conference on Power Electronics and Renewable Energy Applications (PEREA)*, DOI 10.1109/PEREA51218.2020.9339787, pp. 1-6, 2020.

[3] M. A. Mamun, M. A. Hasan and E. Khan, "High voltage conversion DC-DC step up converter for fuel cell applications," *2017 3rd International Conference on Electrical Information and Communication Technology (EICT)*, DOI 10.1109/EICT.2017.8275127, pp. 1-4, 2017.

[4] K. Tseng and J. Lin, "High step-up DC/DC converter for fuel cell hybrid electric vehicles," *2013 International Symposium on Next-Generation Electronics*, DOI 10.1109/ISNE.2013.65124072013, pp. 498-501.

[5] G. Krzywinski, "Integrating storage and renewable energy sources into a DC Microgrid using high gain DC DC Boost Converters," *2015 IEEE First International Conference on DC Microgrids (ICDCM)*, DOI 10.1109/ICDCM.2015.7152049, pp. 251-256, 2015.

[6] R. P. T. Bascopé, L. D. S. Bezerra, C. G. C. Branco, C. M. T. Cruz and G. J. M. Sousa, "A step-Up DC-DC converter for non-isolated on-line UPS applications," *2010 IEEE International Symposium on Industrial Electronics*, DOI 10.1109/ISIE.2010.5637235, pp. 602-607, 2010.

[7] Lee, T. Liang and J. Chen, "Isolated Coupled-Inductor-Integrated DC–DC Converter With Nondissipative Snubber for Solar Energy Applications," in *IEEE Transactions on Industrial Electronics*, vol. 61, DOI 10.1109/TIE.2013.2278517, no. 7, pp. 3337-3348, July 2014.

[8] S. Changchien, T. Liang, J. Chen and L. Yang, "Novel High Step-Up DC–DC Converter for Fuel Cell Energy Conversion System," in *IEEE Transactions on Industrial Electronics*, vol. 57, DOI 10.1109/TIE.2009.2026364, no. 6, pp. 2007-2017, June 2010.

[9] R. Sharma and Hongwei Gao, "Low cost high efficiency DC-DC converter for fuel cell powered auxiliary power unit of a heavy vehicle," in *IEEE Transactions on Power Electronics*, vol. 21, DOI 10.1109/TPEL.2006.872380, no. 3, pp. 587-591, May 2006.

[10] J. Yang, Z. He, H. Pang and G. Tang, "The Hybrid-Cascaded DC–DC Converters Suitable for HVdc Applications," in *IEEE Transactions on Power Electronics*, vol. 30, DOI 10.1109/TPEL.2015.2420666， no. 10, pp. 5358-5363, Oct. 2015.

[11] D. Vinnikov, I. Roasto, R. Strzelecki and M. Adamowicz, "Step-Up DC/DC Converters With Cascaded Quasi-Z-Source Network," in *IEEE Transactions on Industrial Electronics*, vol. 59, DOI 10.1109/TIE.2011.2178211, no. 10, pp. 3727-3736, Oct. 2012.

[12] K. I. Hwu and Y. T. Yau, "High Step-Up Converter Based on Coupling Inductor and Bootstrap Capacitors With Active Clamping," in *IEEE Transactions on Power Electronics*, vol. 29, DOI 10.1109/TPEL.2013.2289387, no. 6, pp. 2655-2660, June 2014.

[13] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti and F. Blaabjerg, "High-Efficiency High Step-Up DC–DC Converter With Dual Coupled Inductors for Grid-Connected Photovoltaic Systems," in *IEEE Transactions on Power Electronics*, vol. 33, DOI 10.1109/TPEL.2017.2746750, no. 7, pp. 5967-5982, July 2018.

[14] Y. Hsieh, J. Chen, T. P. Liang and L. Yang, "Novel High Step-Up DC–DC Converter With Coupled-Inductor and Switched-Capacitor Techniques for a Sustainable Energy System," in *IEEE Transactions on Power Electronics*, vol. 26, DOI 10.1109/TPEL.2011.2160876, no. 12, pp. 3481-3490, Dec. 2011.

[15] M. Chen, J. Hu, K. Li and A. Ioinovici, "A new switched-capacitor based hybrid converter with large step-up DC gain and low voltage on its semiconductors," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, DOI 10.1109/ISCAS.2016.7527459, pp. 1190-1193, 2016.

[16] Fang Lin Luo and Hong Ye, "Positive output super-lift converters," in *IEEE Transactions on Power Electronics*, vol. 18, DOI 10.1109/TPEL.2002.807198, no. 1, pp. 105-113, Jan. 2003.

[17] L. Schmitz, D. C. Martins and R. F. Coelho, "Generalized High Step-Up DC-DC Boost-Based Converter With Gain Cell," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, DOI 10.1109/TCSI.2016.2603782, no. 2, pp. 480-493, Feb. 2017.

[18] L. Yang, T. Liang and J. Chen, "Transformerless DC–DC Converters With High Step-Up Voltage Gain," in *IEEE Transactions on Industrial Electronics*, vol. 56, DOI 10.1109/TIE.2009.2022512, no. 8, pp. 3144-3152, Aug. 2009.

[19] M. A. Salvador, T. B. Lazzarin and R. F. Coelho, "High Step-Up DC–DC Converter With Active Switched-Inductor and Passive Switched-Capacitor Networks," in *IEEE Transactions on Industrial Electronics*, vol. 65, DOI 10.1109/TIE.2017.2782239, no. 7, pp. 5644-5654, July 2018.

[20] Y. Tang, T. Wang and Y. He, "A Switched-Capacitor-Based Active-Network Converter With High Voltage Gain," in *IEEE Transactions on Power Electronics*, vol. 29, DOI 10.1109/TPEL.2013.2272639, no. 6, pp. 2959-2968, June 2014.

[21] M. A. Salvador, J. M. de Andrade, T. B. Lazzarin and R. F. Coelho, "Nonisolated High-Step-Up DC–DC Converter Derived from Switched-Inductors and Switched-Capacitors," in *IEEE Transactions on Industrial Electronics*, vol. 67, DOI 10.1109/TIE.2019.2949535, no. 10, pp. 8506-8516, Oct. 2020.

[22] Y. Almalaq, A. Alateeq and M. Matin, "A Non-Isolated High Gain Switched-Inductor Switched-Capacitor Step-Up Converter for Renewable Energy Applications," *2018 IEEE International Conference*

on Electro/Information Technology (EIT), DOI 10.1109/EIT.2018.8500142, 2018, pp. 0134-0137.

[23] A. M. S. S. Andrade, T. M. K. Faistel, A. Toebe and R. A. Guisso, "Family of Transformerless Active Switched Inductor and Switched Capacitor Ćuk DC–DC Converter for High Voltage Gain Applications," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 2, DOI 10.1109/JESTIE.2021.3091419, no. 4, pp. 390-398, Oct. 2021.

[24] Y. Almalaq, A. Alateeq and M. Matin, "A Transformerless High Gain Switched-Inductor Switched-Capacitor Cuk Converter in Step-Up Mode," *2018 IEEE International Conference on Electro/Information Technology (EIT)*, DOI 10.1109/EIT.2018.8500104, 2018, pp. 0138-0141.

[25] A. M. S. S. Andrade, T. M. K. Faistel, R. A. Guisso and A. Toebe, "Hybrid High Voltage Gain Transformerless DC-DC Converter," in *IEEE Transactions on Industrial Electronics*, DOI 10.1109/TIE.2021.3066939.

[26] B. Faridpak, M. Bayat, M. Nasiri, R. Samanbakhsh and M. Farrokhifar, "Improved Hybrid Switched Inductor/Switched Capacitor DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 36, DOI 10.1109/TPEL.2020.3014278, no. 3, pp. 3053-3062, March 2021.

[27] M. Mellincovsky and S. Tapuchi, "Input stage enhancement of a switched-capacitor switched inductor circuit," *2012 IEEE 27th Convention of Electrical and Electronics Engineers in Israel,* DOI 10.1109/EEEI.2012.6377038, 2012, pp. 1-5.

[28] J. C. Rosas-Caro, J. M. Ramirez and P. M. Garcia-Vite, "Novel DC-DC Multilevel Boost Converter," 2008 *IEEE Power Electronics Specialists Conference*, DOI 10.1109/PESC.2008.4592260, pp. 2146-2151, 2008.

[29] B. Axelrod, Y. Berkovich and A. Ioinovici, "Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC–DC PWM Converters," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, DOI 10.1109/TCSI.2008.916403, no. 2, pp. 687-696, March 2008.

[30] B. Wu, S. Li, Y. Liu and K. Ma Smedley, "A New Hybrid Boosting Converter for Renewable Energy Applications," in *IEEE Transactions on Power Electronics*, vol. 31, DOI 10.1109/TPEL.2015.2420994, no. 2, pp. 1203-1215, Feb. 2016.

[31] A. Alzahrani, M. Ferdowsi and P. Shamsi, "A Family of Scalable Non-Isolated Interleaved DC-DC Boost Converters With Voltage Multiplier Cells," in *IEEE Access*, vol. 7, DOI 10.1109/ACCESS.2019.2891625, pp. 11707-11721, 2019.

[32] Y. Zhang, Y. Gao, J. Li and M. Sumner, "Interleaved Switched-Capacitor Bidirectional DC-DC Converter With Wide Voltage-Gain Range for Energy Storage Systems," in *IEEE Transactions on Power Electronics*, vol. 33, DOI 10.1109/TPEL.2017.2719402, no. 5, pp. 3852-3869, May 2018.

[33] Y. Tang, D. Fu, T. Wang and Z. Xu, "Hybrid Switched-Inductor Converters for High Step-Up Conversion," in *IEEE Transactions on Industrial Electronics*, vol. 62, DOI 10.1109/TIE.2014.2364797, no. 3, pp. 1480-1490, March 2015.

[34] B. Wu, S. Li, K. M. Smedley and S. Singer, "Analysis of High-Power Switched-Capacitor Converter Regulation Based on Charge-Balance Transient-Calculation Method," in *IEEE Transactions on Power Electronics*, vol. 31, DOI 10.1109/TPEL.2015.2466095, no. 5, pp. 3482-3494, May 2016.