Low On-state Resistance Normally-OFF AlGaN/GaN MIS-HEMTs with Partially Recessed Gate and ZrO_x Charge Trapping Layer

Yutao Cai, Yuanlei Zhang, Ye Liang, Ivona Z. Mitrovic, Huiqing Wen, Wen Liu, and Cezhou Zhao

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***Abstract*—Novel normally-off AlGaN/GaN MIS-HEMTs with a ZrO_x charge trapping layer is proposed. The deposition of ZrO_x charge trapping layer on the partially recessed AlGaN in conjunction with the Al_2O_3 gate dielectric has been accomplished. The developed MIS-HEMTs exhibit a threshold voltage of 1.55 ±0.4 V and a maximum drain current of 730 ±6 mA/mm, while associated low on-resistance of 7.1 ±0.2 Ω·mm, for a gate to drain separation of 3 μm. The TCAD simulation results are presented to explore the charge trapping and de-trapping behaviors. Moreover, the devices exhibit a high breakdown voltage. The results indicate the merits of employing ZrO_x charge trapping layer to realize the normally-off GaN devices with low on-state resistance.**

***Index Terms*—AlGaN/GaN, Normally-off, MIS-HEMTs, ZrO_x, On-resistance, Breakdown voltage.**

I. Introduction

GaN-based high electron mobility transistors (HEMTs) are considered as promising devices for the high power application, owing to their superior characteristics of high breakdown voltage and high current density. In power electronics applications, normally-off (E-mode) HEMTs are preferred for the safety consideration. To realize the E-mode operation of devices, several approaches have been explored, such as fully recessed gate [1], thin AlGaN barrier [2], p-type GaN [3], fluorinated-gate [4], and oxide charge engineering [5]. Among these techniques, the devices combing fully recessed gate with high-quality gate dielectric techniques [6] demonstrate the normally-off operation and good threshold voltage (V_{th}) stability, but the current density is low due to the damaged 2-D electron gas channel (2DEG). Even though the p-type GaN normally-off devices [7] exhibit low on-state resistance, low V_{th} and low gate breakdown voltage are two obvious limitations. The E-mode devices with fluorinated-gate [8] demonstrate a very high $V_{th,}$ however, the devices lack enough stability.

The GaN-based MIS-HEMTs using charge storage gate structure have been proposed to forward shift the V_{th} to achieve the normally-off operation without serious current degradations. A simulation analysis has indicated that the negative charges in a floating gate or an oxide layer are capable of depleting the 2DEG beneath the gate region, resulting in a normally-off operation [9]. In addition, some experimental studies indicated that normally-off MIS-HEMTs can be realized by using charge storage structures, such as the TaN floating gate [10], the HfO_2 [11], and the Al_2O_3 charge storage layer [12]. Furthermore, high V_{th} normally-off MIS-HEMTs with high drain current density by the combination of ferroelectric and charge storage layers have been demonstrated [13]. Even though the reported MIS-HEMTs with charge trapping structure can achieve outstanding normally-off device properties, the complex gate structures and the limited charge storage capacity are still important issues for their fabrication and application in high voltage devices.

In this work, the deposition of ZrO_x charge trapping layer on the partially recessed AlGaN in conjunction with Al_2O_3 layers is developed. The deployment of the ZrO_x layer is capable of capturing electrons after a gate bias initialization that deplete the 2DEG beneath to realize the E-mode devices. A larger V_{th} shift of ~9.76 V between the E-mode and D-mode operations implies an enormous potential of charge storage capacity in the ZrO_x layer we proposed. Moreover, the electrical properties of normally-off MIS-HEMTs indicate highly desired performance including positive V_{th} and low on-state resistance. On the other hand, we analyze the threshold voltage instability of the proposed devices. The effects of illumination, high-temperature and off-state drain bias stress on the stability of the threshold voltage are demonstrated. The TCAD simulations are carried out to explore the charge trapping and de-trapping behaviors.

II. Device Fabrication

The investigated HEMT structure consists of a 2 nm undoped GaN cap layer, a 22 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer and a 5.4 μm GaN buffer layer. The fabrication started from the mesa isolation by using BCl_3/Cl_2 gas reactive ion etching. Then, the Au-free source and drain were formed by e-beam evaporation of Ti/Al/Ti/TiN (22.5/90/50/70 nm), and annealed at 900 ℃ in N_2 ambient for 30 s. The ohmic contact resistance was extracted as 1.4 ±0.1 Ω·mm. The AlGaN beneath the gate area was partially removed by 40 cycles of low power O_2 plasma

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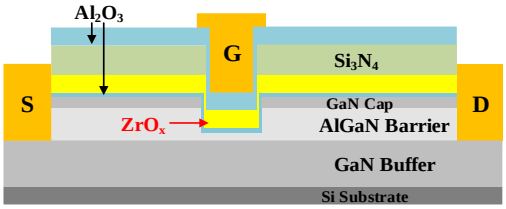

Fig. 1. Cross-sectional schematic of the MIS-HEMTs with a 4 nm Al_2O_3 tunneling layer, 16 nm ZrO_x trapping layer and 12 nm Al_2O_3 barrier layer.

oxidation and HCl-based oxide removal. The low damage digital etching with an etching rate of 0.4 nm/cycle is beneficial to control the etching depth precisely. The gate recess depth is 16 nm measured by atomic force microscopy. After the surface clean processes on the wafer, a 4 nm Al_2O_3 tunneling layer was deposited by atomic layer deposition (ALD). Then, a 16 nm ZrO_x charge trapping layer was deposited on top of the Al_2O_3 by ALD at 300 ℃. Tetrakis (ethylmethylamino) zirconium and H_2O were used as precursors of Zr and oxygen, respectively, with a growth rate of ~0.1 nm/cycle. Specifically, the pulse time of tetrakis (ethylmethylamino) zirconium was 130 ms, the pulse time of H_2O was 50 ms. The 300 nm Si_3N_4 insulator layer was then deposited above the ZrO_2 layer by plasma enhanced chemical vapor deposition at 350 ℃. After removal of the Si_3N_4 passivation in gate regions, a 12 nm Al_2O_3 was then grown by ALD as a barrier layer to suppress the gate leakage current. The two layers of Al_2O_3 were deposited at 230 ℃ with a growth rate of ~0.11 nm/cycle. The thickness of films was evaluated by spectroscopic ellipsometry. Finally, the devices were completed by Ni/TiN (50/100 nm) gate formation. Fig. 1 shows a schematic cross-sectional view of the fabricated devices.

III. Device Results and Discussion

The transfer characteristics of the fresh and the initialized MIS-HEMTs with V_{DS} = 1 V are plotted in Fig. 2 (a). The devices feature a source-gate space (L_{SG}) of 3 μm, a gate length (L_G) of 2 μm, a gate-drain space (L_{GD}) of 3 μm, and a gate width of 50 μm. The fresh devices exhibited the D-mode operation with a V_{th} of -8.25 ±0.14 V. A high voltage of 12 V was applied on the gate for 1 min as the initialization process. All the initialization process in this study was carried out at room temperature (RT) with both drain and source grounded. The corresponding transient gate current during the 1 min initialization is plotted in Fig. 2 (b). The initialized transfer curves were measured by gate sweeping from 0 V to 9 V with a step of 100 mV. The V_{th} was shifted to 1.55 ±0.4 V after the initialization, at a drain current criterion of 1 μA/mm, which validates the presence of negative charges in the gate stack layers. A V_{th} difference of ~9.8 V between the E-mode and D-mode operations implies an enormous potential for charge storage capacity. The initialized devices exhibited a trans-conductance of 54 mS/mm, a V_{th} hysteresis of -38 mV and a subthreshold slope (S.S) of 87 mV/dec. The devices were well pinched off at V_{GS} = 0 V, indicating a normally-off operation. Moreover, the gate leakage was lower than 27 nA/mm at a V_{GS} of 12 V, indicating that the robust Al_2O_3 barrier layer could suppress electrons tunneling to the gate. The V_{th} distribution histogram of 25 initialized MIS-HEMTs is shown in Fig. 2 (c). The V_{th} exhibited a narrow distribution with an average value

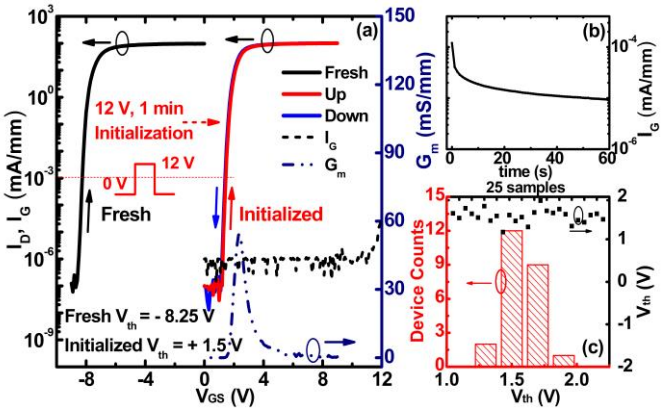

Fig. 2. (a) Transfer characteristics of the devices with an $Al_2O_3/ZrO_x/Al_2O_3$ gate stack. (b) The transient gate current during the 1 min initialization. (c) Threshold voltage uniformity of 25 initialized MIS-HEMTs.

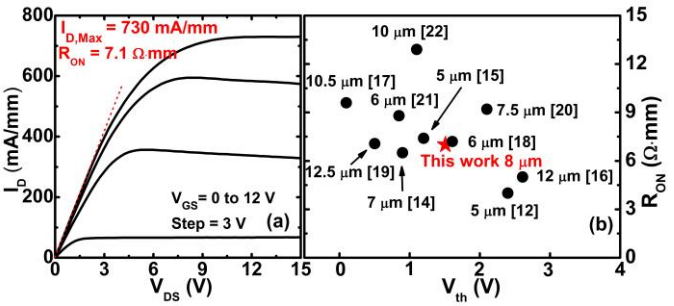

Fig. 3. (a) DC I_D–V_{DS} characteristics of the initialized MIS-HEMTs. (b) A benchmark of R_{ON} with the drain to source dimension (L_{DS}) versus V_{th} for the state-of-the-art E-mode GaN-based transistors.

of 1.55 V and a standard deviation of 0.17 V, indicating satisfied uniformities of the charge storage structure.

The output curves of the initialized devices are depicted in Fig. 3 (a) where V_{GS} was swept from 0 V to 12 V with a step of 3 V and V_{DS} was swept from 0 V to 15 V. The devices feature an $L_{SG}/L_G/L_{GD}$ dimension of 3/2/3 μm. The maximum drain current density was extracted to be 730 ±6 mA/mm at V_{GS} = 12 V. The on-resistance (R_{ON}) was 7.1 ±0.2 Ω·mm under V_{GS} = 12 V and V_{DS} = 0.25 V. The channel mobility and carrier concentration were extracted to be 1450 $cm^2/V•s$ and $1.1×10^{13}$ cm^{-2}, respectively. The high output current density and low R_{ON} were well achieved likely to be due to the damage-free 2DEG channel. Fig. 3 (b) benchmarks the R_{ON} with the drain to source dimension versus V_{th} of normally-off devices in this work with state-of-the-art reports [12, 14-22]. Our devices exhibit a competitive V_{th} as well as a high $I_{DS,max}$. It is noticeable that the R_{ON} in this work has a small value compared, which demonstrates the merits of realizing normally-off MIS-HEMTs by employing the ZrO_x charge trapping layer.

The Sentaurus TCAD simulations were carried out to understand the charge trapping behavior. The device structure analyzed in the simulations was the same as that of the fabricated device, and the schematic band profiles of $Al_2O_3/ZrO_x/Al_2O_3$/ AlGaN/GaN stack at the cross section of the gate region was extracted. Note that, the material parameters of ZrO_2 were used for presenting the ZrO_x charge trapping layer in the simulations. As shown in Fig. 4 (a), in fresh devices, the shallow bulk traps in the ZrO_x are empty due to the deep Fermi

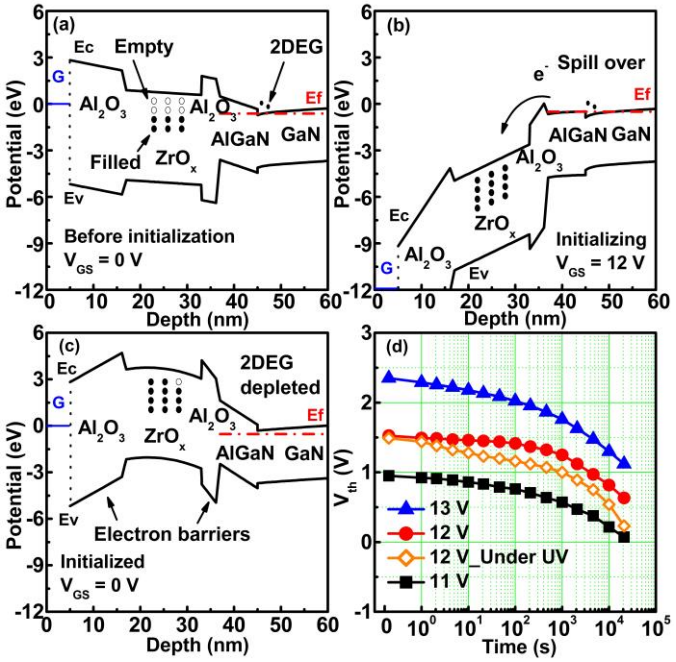

Fig. 4. The simulated schematic band profiles at the vertical cross section of $Al_2O_3/ZrO_x/Al_2O_3$/AlGaN/ GaN gate stack (a) before, (b) during, (c) after the 12 V initialization, (d) Retention curves of the MIS-HEMTs after 11 V, 12 V and 13 V initialization, and the 12 V initialized devices under a 365 nm UV illumination.

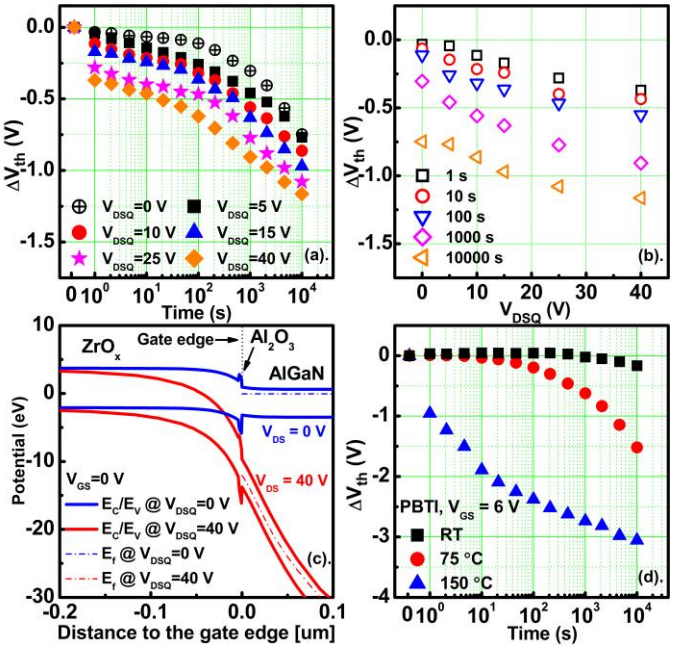

Fig. 5. (a) V_{th} shift of the initialized devices during the 10000 s drain biases at RT. (b) The extracted V_{th} shift with different drain biases at 1 s, 10 s, 100 s, 1000s, 10000 s, at RT. (c) The simulated schematic band profiles at the horizontal cross section of the ZrO_X dielectric with drain biases of 0 and 40 V. (d) V_{th} shift of the initialized devices during the 10000 s PBTI measurements at RT, 75 °C and 150 °C.

layer due to a high electric field. A number of electrons would level. Here, the 2DEG channel exists at the AlGaN/GaN interface due to the polarization effect, and the devices exhibit the normally-on operation. As shown in Fig. 4 (b), in the 12 V initialization process, the flat potential of the AlGaN layer leads to electrons spilling-over from the 2DEG. Electrons would tunnel through the 4 nm thin Al_2O_3 and then enter into the ZrO_x be trapped by the high density acceptor-like traps in the ZrO_x layer. At the same time, the 12 nm Al_2O_3 barrier would stop electrons tunneling to the gate electrode. As shown in Fig. 4 (c), after removal of the gate bias, most traps in the ZrO_x bulk were still filled due to a high conduction band offset (~ 1.15 eV) between Al_2O_3 and ZrO_x thin films, and the Al_2O_3 layers work as barriers to stop the de-trapping of electrons. It is worth noting that the filled bulk traps in the ZrO_x layer act as negative fixed charges. These high density negative charges are capable of bending the conduction bands to a higher potential, and then deplete the 2DEG at a gate bias of 0 V. Here, a positive gate bias is required to form the 2DEG channel, and thus the devices exhibit the E-mode operation. The experimental retention characteristics of the initialized devices at RT and under 365 nm ultra-violet (UV) light illumination are shown in Fig. 4 (d). Here, the V_{th} was monitored by an I_D–V_{GS} test with a V_{GS} varied from -2 V to 6 V and a V_{DS} of 1 V after certain time intervals (0, 1, 2.1, 4.6, 10, 21, 46, 100, 210, 460, 1000, 2100, 4600, 10000 and 21000 s). All electrodes were grounded before V_{th} extractions. The initialization voltages were set as 11 V, 12 V and 13 V. In the case of a 12 V initialization, the total V_{th} shift showed a low value of -0.9 V, while the V_{th} kept positive for 21000 s indicating a weak charge de-trapping phenomenon. Moreover, the total V_{th} shift was extracted to be -1.28 V for the case with the UV illumination. It indicates that the UV illumination would cause a more obvious de-trapping behavior at the gate oxides stack.

The drain bias induced V_{th} instability of the initialized MIS-HEMTs was experimentally investigated. The devices with an $L_{SG}/L_G/L_{GD}$ dimension of 3/3/20 μm were stressed with different drain voltages (V_{DSQ}) of 0, 5, 10, 15, 25 and 40 V, at RT. Both gate and source were grounded during the drain biases referring to an off-state condition, and the total bias time was set as 10000 s. The I_D-V_{GS} test was carried out to extract threshold voltage after certain time intervals. The V_{th} shift (ΔV_{th}) measured during the 10000 s drain biases are plotted in Fig. 5 (a), and the ΔV_{th} corresponding to the drain biases at 1, 10, 100, 1000 and 10000 s are extracted in Fig. 5 (b). Large negative ΔV_{th} shifts are observed at 1 s when the initialized devices are stressed with a high drain voltage. In addition, the total ΔV_{th} shift at 10000 s increases with the increase of V_{DSQ}, and it is extracted as -1.17 V for the case with a V_{DSQ} of 40 V. The results indicate that a high drain bias is capable of speeding up the de-trapping behavior at the gate stack. Another Sentaurus TCAD simulation was carried out to understand the drain bias induced V_{th} instability. In the simulation, the initialized device with an L_{GD} of 20 μm was set as same as that in Fig. 4 (c), where the electron traps in the ZrO_x layer were filled and the 2DEG channel was depleted. Both gate and source were grounded, and a V_{DSQ} of 40 V was set as the drain bias. The schematic band profiles at the horizontal cross section of the ZrO_x dielectric were analyzed. Here, the horizontal cross section was extracted 3 nm above the Al_2O_3 tunneling layer, and the schematic band profiles close to the drain edge of the gate were plotted in Fig. 5 (c). It is worth noting that most filled traps in the ZrO_x bulk are above the Fermi level in the initialized devices. In the case without a drain bias (V_{DSQ} = 0 V), the Al_2O_3 layer at the sidewall of the gate edge acts as a barrier to stop the de-trapping of electrons. However, when a high bias of 40 V is applied on the

drain, the bands of $ZrO_x/Al_2O_3/AlGaN$ layers are bent to a deeper energy level, which is known as the drain-induced barrier height lowering (DIBL) effect [23]. The sharply dropping of potential energy close to the gate terminal would cause electrons emitted from the filled acceptor-like traps in the ZrO_x layer, and then lead to a negative V_{th} shift. Here, with a drain bias of 40 V, a high electrical field peak of ~ 3.5 MV/cm is also observed at the drain edge of the gate [24] of the devices.

The positive bias temperature instability (PBTI) test was performed to assess the drain gate induced V_{th} instability of the initialized devices at high temperatures. A gate bias of 6 V was applied on the devices. Both drain and source were grounded during the gate bias, and the corresponding electric field in the $Al_2O_3/ZrO_x/Al_2O_3$ gate stack was 1.9 MV/cm. The threshold voltage was monitored by an I_D-V_{GS} test after certain bias time intervals, and the total bias time was set as 10000 s. The measurements were carried out at RT, 75 and 150 ℃. The ΔV_{th} measured during the 10000 s gate bias are plotted in Fig. 5 (d). It can be observed that at RT, the V_{th} has a slight negative shift of 0.22 V at 10000 s. By comparison, the negative V_{th} shift becomes more significant at higher temperatures of 75 ℃ and 150 ℃. When subjected to a positive gate bias, the initialized MIS-HEMTs suffer from a negative V_{th} shift, which is ascribed to the de-trapping charges within the gate insulators. It is worth pointing out that compared with state-of-the-art GaN-based devices with p-GaN gate [25], the proposed devices were more sensitive to the high temperature. Moreover, It is noticeable that the V_{th} distribution for the fresh devices was relatively narrower (±0.14 V) than that of the initialized devices (±0.4 V). The sensitive charge trapping and de-trapping behaviors could be the main factors that lead to the large V_{th} variation in the initialized devices.

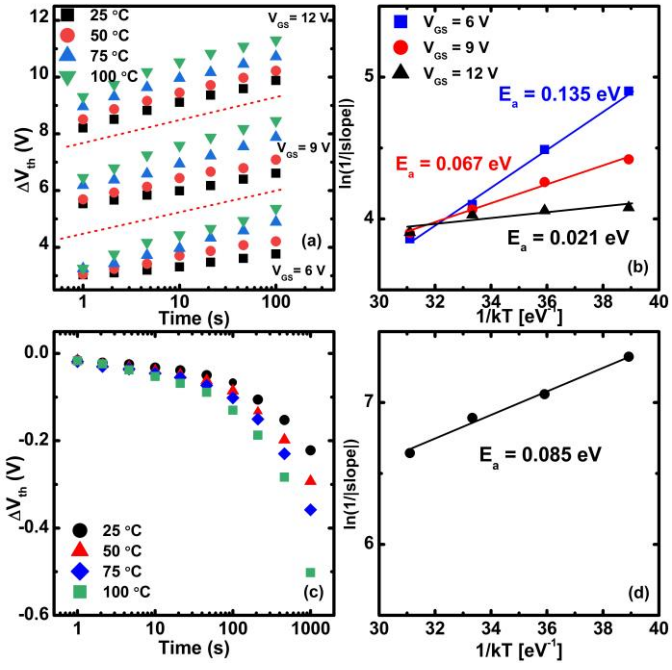

Fig. 6. (a) V_{th} shift of the fresh MIS-HEMTs with 6 V, 9 V and 12 V gate biases at RT, 50, 75 and 100 ℃. (b) Arrhenius plot of the 100 s PBTI characteristics with 6 V, 9 V and 12 V gate biases. (c) Retention curves of the 12 V initialized MIS-HEMTs at RT, 50, 75 and 100 ℃. (d) Arrhenius plot of the 100 s retention characteristics.

Activation energies for trapping and de-trapping charges in the gate oxide layers were analyzed to evaluate the threshold voltage stability under different gate biases. For the analysis of the activation energy of electrons trapping behavior in the gate stack, the ΔV_{th} during the PBTI test was monitored. Here, the PBTI measurements were carried out on the fresh devices at RT, 50, 75, and 100 ℃. Three different gate voltages of 6 V, 9 V and 12V were applied as the gate biases. The ΔV_{th} was extracted during the 100 s initialization process (1, 2.1, 4.6, 10, 21, 46, and 100 s). The statistics of ΔV_{th} at 6 V, 9 V and 12 V gate biases are plotted in Fig. 6 (a). The positive shift of V_{th} in the PBTI measurement indicates the thermal- and gate voltage-dependent electron trapping behaviors in the devices. Fig. 6 (b) shows the Arrhenius plots of the 100 s PBTI characteristics. The activation energy for trapping charge was obtained from the slope of the linear fit of the Arrhenius equation [26]. Note that, for each bias, the ΔV_{th} from 1 s to 100 s was extracted as the changing rate parameter. The linear-fitted trapping activation energies at 6 V, 9 V and 12 V were extracted to be 0.135 eV, 0.067 eV and 0.021 eV, respectively. It can be observed that the activation energy for trapping charges decreases with the increase of gate bias. This indicates that a higher initialization voltage or a higher gate bias causes electrons captured by the gate oxides more readily. On the other hand, due to the V_{th} of initialized devices being dependent on the density of trapped charges, the observed V_{th} shift during the retention measurement was considered as the de-trapping process [12]. For the analysis of the activation energy of electrons de-trapping behaviors in the gate stack, the retention characteristics of the 12 V initialized devices were measured at RT, 50, 75, and 100 ℃. The ΔV_{th} was extracted after certain time intervals. The retention characteristics of the initialized MIS-HEMTs at different temperatures are presented in Fig. 6 (c). The Arrhenius plot of retention characteristics at 100 s is plotted in Fig. 6 (d) with the linear-fitted activation energy of 0.085 eV. Here, the temperature-dependent ΔV_{th} during the 100 s retention measurements were extracted as the changing rate parameters in the analysis. Note that, the activation energy for de-trapping charges in the initialized devices (0.085 eV) is lower than that for trapping charges with a gate bias of 6 V (0.135 eV, Fig. 6 (b) line in blue). It implies that more charges tend to be de-trapping from the gate stack in this condition, and this explains the negative V_{th} shift observed in the 6 V PBTI characteristics in Fig. 5 (d).

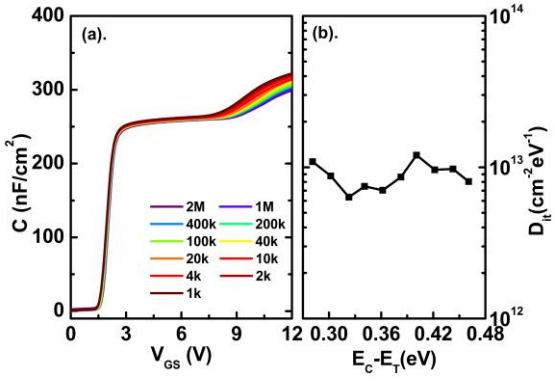

Fig. 7. (a) Multi-frequency C-V characteristics of the initialized devices. (b) Distribution of D_{it} vs. (E_C – E_T) at the gate oxide/AlGaN interface extracted from C-V characteristics.

The trap density (D_{it}) at Al_2O_3/AlGaN interface was estimated by implementing C-V measurements on the 12 V initialized devices. Typical multi-frequency C-V characteristic curves of the MIS-capacitor are shown in Fig. 7 (a). The measurement gate bias was swept from 0 V to 12 V with a step of 50 mV, the frequency was varied from 2 MHz down to 1 kHz, and the measurement temperature was RT. Note that, the C-V curves feature two rising edges. The first rising edge at $V_G \sim 1.5$ V corresponds to the formation of the 2DEG channel, implying a normally-off operation. The second rising edge at higher V_{GS} refers to the spill-over of the 2DEG to the Al_2O_3/AlGaN interface. The D_{it} at Al_2O_3/AlGaN interface can be calculated by the second slope onset voltage (V_{ON}) in the C-V curves [27]. The onset voltage dispersion (ΔV_{ON}) occurs at two measurement frequencies (f_1, f_2) due to interface traps existing in the energy range from $E_{Trap}(f_1)$ to $E_{Trap}(f_2)$. The detectable energy of the interface trap $E_{Trap}(f_m)$ as a function of measurement frequency f_m can be represented by:

$$E_{Trap}(f_m) = E_C - E_T = kT\ln\left(\frac{v_{th}\,\sigma_n N_c}{2\pi f_m}\right) \qquad (1)$$

where k is the Boltzmann's constant, T is the measurement temperature, $N_C = 2.2\times10^{18}$ cm^{-3} is the effective density of states in the conduction band of AlGaN, σ_n is the electron capture cross section, and $v_{th} = 2\times10^7$ cm·s^{-1} is the thermal velocity of electrons [28]. According to the interface state density - energy level mapping method proposed by Yang *et al* [27], distribution of the Al_2O_3/AlGaN interface states can be obtained by Eq. (2):

$$D_{it}(E = E_{AVG}) = \frac{C_{OX}\cdot}{q\Delta E_{Trap}} - \frac{C_{OX}+C_B}{q^2} \qquad (2)$$

where C_{OX} is the capacitance of the gate oxide stack, C_B is the capacitance of the AlGaN barrier layer, ΔE_{Trap} is the interface trap frequency dependent energy difference. The value of C_{OX} can be extracted as maximum capacitance observed in C-V plots, and it is found to be 328 nF/cm^2. C_B is extracted to be 1023 nF/cm^2, and it is calculated from the first plateau capacitance, as the latter refers to the series capacitance connection between C_{OX} and C_B. Fig. 7 (b) shows the D_{it} distribution at the Al_2O_3/AlGaN interface. The electron capture cross section at the interface σ_n was assumed to be 1×10^{-14} cm^2, which gives values of D_{it} in the energy level range of 0.28 eV to 0.46 eV from the conduction band edge. Here, the extracted D_{it} is calculated to be from 1.2×10^{13} cm^{-2}eV^{-1} to 6.3×10^{12} cm^{-2}eV^{-1} in this energy range.

The time-dependent dielectric breakdown (TDDB) tests were performed at constant V_{GS} biases of 14 V, 15 V, 16 V, and 17 V (gate hard breakdown voltage was ~19 V) with source and drain grounded, respectively. The gate leakage currents recorded with time are shown in Fig. 8 (a). The breakdown time (t_{BD}) was defined at the time when the sudden increase in gate leakage occurred. The t_{BD} at a constant stress voltage shows a Weibull distribution with a slope of 3.5 (Fig. 8 (b)), indicating a tight breakdown time distribution and a small variability in breakdown behavior. In Fig. 8 (c), the maximum V_{GS} is predicted to be ~7.5 V for a 10-year lifetime of gate oxides stack at a failure level of 63% by using combined TDDB models [29].

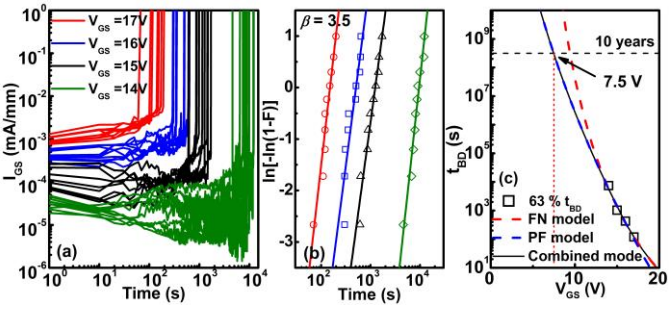

Fig. 8. (a) t_{BD} of the devices for gate stress of 14, 15, 16, and 17 V. (b)Weibull plot of the electric field-dependent t_{BD} distribution. (c) Lifetime prediction of the 63% failure level using combined TDDB models over a wide range of field.

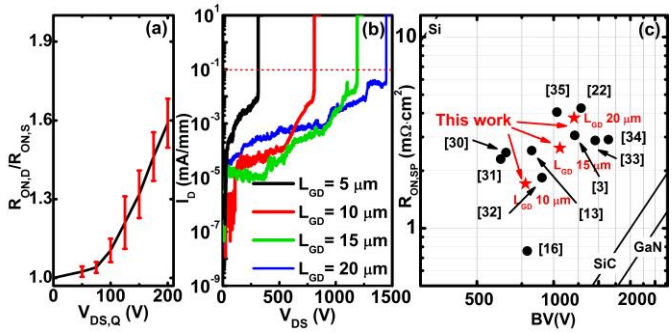

Fig. 9. (a) The ratio of dynamic/static on-resistance for the MIS-HEMTs at different quiescent drain biases. (b) Breakdown characteristics of the fabricated MIS-HEMTs with different L_{GD} values. (c) A benchmark of BV versus $R_{ON,SP}$ for the normally-off GaN-based devices in this work and state-of-the-art reports.

The dynamic on-state performance of the devices was evaluated under fast switching with different quiescent bias points. Here, the devices feature an L_{GD} of 20 μm. The quiescent gate bias ($V_{GS,Q}$) was fixed at 0 V, the off-state stress time was 1 s, and the off-state to on-state switching time was 500 μs. The ratio of dynamic R_{ON} ($R_{ON,D}$/ $R_{ON,S}$) was plotted in Fig. 9 (a), and the R_{ON} value here were extracted at V_{DS} = 0.25 V. The devices exhibit a $R_{ON,D}$/ $R_{ON,S}$ of 1.6±0.1 when the off-state stress $V_{DS,Q}$ is 200 V. Fig. 9 (b) depicts the off-state breakdown characteristics of MIS-HEMTs at a V_{GS} of -9 V with the floating substrate. Note that, because high drain biases would cause negative V_{th} shifts on the initialized devices, the -9 V negative gate bias smaller than the V_{th} of the fresh devices (-8.25) was used in the breakdown voltage extraction for safety consideration. It also implies a not true normally-off operation of the proposed devices under the high voltage stress. The devices with an $L_{SG}/L_G/L_{GD}$ = 3/3/20 μm exhibited a $R_{ON,SP}$ of 3.78 mΩ•cm^2, taking into account a 3 μm transfer length of the source and drain ohmic contacts. Moreover, a high breakdown voltage (BV) of 1447±32 V was extracted at drain leakage current criterion of 100 μA/mm, which associated a power figure of merit (BV^2/Ron,sp) of 554 MW/cm^2. Fig. 9 (c) summarizes the state-of-the-art E-mode GaN-based devices compared to devices fabricated in this work providing a benchmark of $R_{ON,SP}$ versus breakdown voltage metric. [3, 13, 16, 22, 30-35].

IV. Conclusion

The normally-off AlGaN/GaN MIS-HEMTs with partially recessed gate and ZrO_x charge trapping layer has been demonstrated in this study. The ZrO_x layer enables the E-mode operation as a result of the storage of electrons. The devices exhibit a V_{th} of 1.55 ± 0.4 V, a maximum drain current density of 730 ± 6 mA/mm, and a low on-resistance of 7.1 ± 0.2 Ω·mm. The threshold voltage has been able to maintain positive for 21000 s indicating a weak charge de-trapping phenomenon. However, the thermal- and drain bias stress-induced negative shift of V_{th} in proposed devices suggest further improvements are needed. Moreover, the $R_{ON,D}/R_{ON,S}$ ratio was extracted as 1.6 ± 0.1, and the devices exhibited a high breakdown voltage of 1447 ± 32 V. Although further optimization in the V_{th} stability is necessary for practical use, employing the ZrO_x charge trapping layer still demonstrates a significant potential to realize the normally-off MIS-HEMTs with both high V_{th} and low resistance.

V. References

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