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Recent depleted CMOS developments within the CERN-RD50 framework

Eva Vilella[1][l]
University of Liverpool
Department of Physics, Oliver Lodge Laboratory, Oxford Street, L69 7ZE Liverpool, United Kingdom
E-mail: vilella@hep.ph.liv.ac.uk

Depleted CMOS sensors are groundbreaking position sensitive detectors that offer a competitive and cost-effective solution for a large range of particle tracking applications. In spite of their substantial advantages, these sensors require further research to become even more performant and meet the ever more demanding requirements of particle physics experiments planned for the near future. In this context, the CERN-RD50 collaboration has started a new R&D programme to study and develop depleted CMOS sensors as one of its main priorities.

This article presents the depleted CMOS R&D programme within the CERN-RD50 collaboration. It describes the design aspects of the two prototype ASICs developed so far, which are in a 150 nm High Voltage-CMOS (HV-CMOS) process and manufactured on high resistivity substrates. The first prototype ASIC, named RD50-MPW1 and delivered after fabrication in April 2018, integrates a matrix of 50 μm x 50 μm pixels with all the analogue and digital readout electronics for column drain readout embedded in their sensing areas. The second prototype ASIC, named RD50-MPW2 and delivered after fabrication in January 2020, integrates a matrix of 60 μm x 60 μm pixels with analogue readout electronics to reduce the sensor response time. RD50-MPW2 incorporates new methods to optimise the leakage current of the sensor. The article discusses laboratory measurements of the performance evaluation of RD50-MPW1, while those of RD50-MPW2 will be published elsewhere.

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[1]Speaker
[l]On behalf of the CERN-RD50 collaboration. See https://rd50.web.cern.ch/rd50/db/report/authors-list.asp for full authors list.

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1. Introduction

Depleted CMOS sensors are position sensitive detectors in CMOS or High Voltage-CMOS (HV-CMOS) processes. This allows integrating the sensing diode and the readout ASIC in a single layer of silicon, which removes the need for interconnection with complex and expensive solder bump technology, and provides fast charge collection and high radiation tolerance [1]. Because of these significant advantages, depleted CMOS sensors are emerging as a prime candidate for future particle tracking applications. However, these sensors require further research to become even more performant and meet the extreme requirements on granularity, time resolution and radiation tolerance of future particle physics experiments. To address this, the CERN-RD50 collaboration has started a new R&D programme to study and develop depleted CMOS sensors as one of its main priorities. The design of the two prototype ASICs developed so far, which are in the 150 nm HV-CMOS process from LFoundry and named RD50-MWP1 and RD50-MPW2, together with the laboratory measurements of the performance evaluation of RD50-MPW1 are presented in the next sections.

2. Design of RD50-MPW1

The goal of RD50-MPW1 is to gain in-depth knowledge and first-hand expertise in the development of depleted CMOS sensors within the CERN-RD50 collaboration. Following from state-of-the-art work carried out in the wider community, RD50-MPW1 integrates one pixel matrix aimed at particle physics experiments, another pixel matrix for photon counting applications and test structures for characterising the sensor depletion region. The two matrices are fully monolithic, while the test structures are passive (i.e., diodes). The matrices and the test structures are completely independent, as they only share the silicon substrate. The prototype ASIC, which has an approximate size of 5 mm x 5 mm, has been fabricated in two high resistivity substrates with nominal values of 500 Ω·cm – 1.1 kΩ·cm and 1.9 kΩ·cm (measured to be 600 Ω·cm and 1.1 kΩ·cm respectively) to achieve large depletion regions. It is a much improved version of a previous design that was developed outside the CERN-RD50 collaboration [2]. The following paragraphs will focus on the matrix aimed at particle physics experiments only.

Figure 1 shows the layout views of the full ASIC and of the pixel of the matrix for particle physics experiments. This matrix integrates 40 rows x 78 columns of pixels, a global and programmable bias circuit with 6-bit Digital-to-Analogue Converters (DACs), 40 horizontal and 78 vertical configuration registers, 78 End Of Column (EOC) circuits, an untriggered state machine and 50 pads. It incorporates the so-called column drain readout architecture, which is similar to that of the FEI3 readout ASIC developed for the hybrid pixels used in the ATLAS Inner Detector [3]. The pixels, which have a size of 50 μm x 50 μm, integrate all the analogue and digital readout electronics for column drain readout in their sensing areas. This represents a considerable improvement in comparison to another state-of-the-art depleted CMOS detector prototype in the same technology node, where a pixel size of 50 μm x 250 μm was achieved with similar readout electronics also integrated in the sensing area of the pixel [4]. However, the smaller pixel size of RD50-MPW1 is only possible after sacrificing some features. These are related to the sensor breakdown voltage and the number of transistors of the readout electronics.

Figure 2 shows the typical cross-section of a pixel in the 150 nm HV-CMOS process from LFoundry. In this process, the sensor is implemented by means of a p-substrate/deep n-well

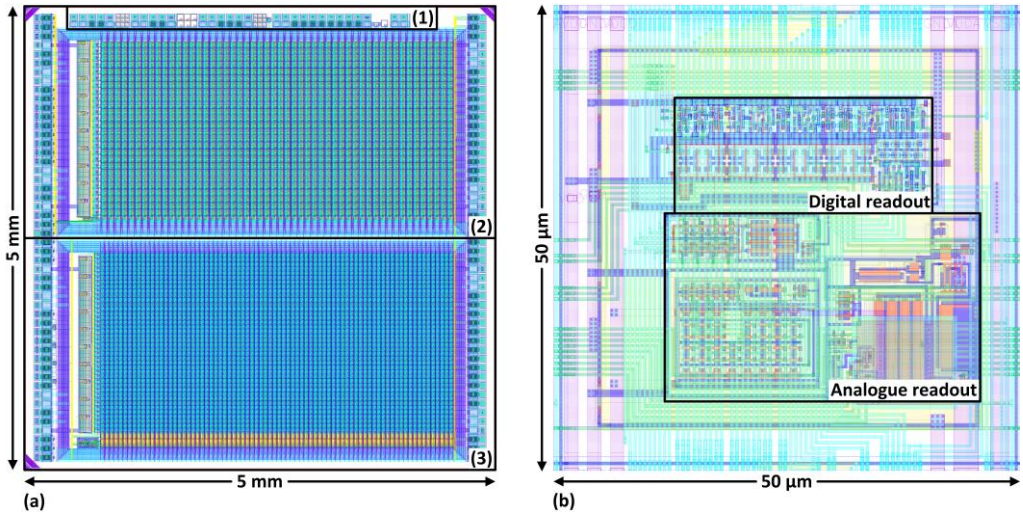

Figure 1 Layout views: RD50-MPW1 (a) and pixel of the matrix for particle physics experiments (b). Regions (1), (2) and (3) in (a) correspond to the test structures, the matrix for photon counting applications and the matrix for particle physics experiments respectively.

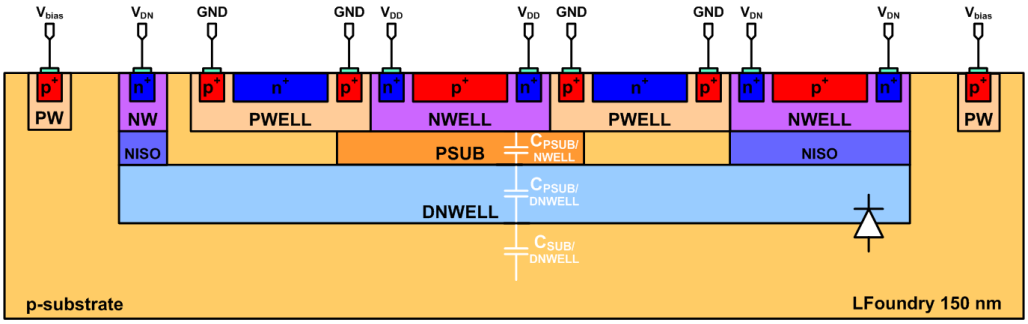

Figure 2 Schematic cross-section of a pixel in the 150 nm HV-CMOS process from LFoundry. The drawing is not to scale.

junction. To create a considerable depletion region, the p-substrate is biased at a large reverse voltage using a topside p-well implant. The deep n-well (DNWELL in figure 2), which is the collecting electrode, is implanted a few µm down in the silicon substrate. It is biased at approximately 1.75 V by means of a stack of two shallower n-type layers, namely an n-well and a niso implant. Niso is also a buried layer, but shallower than the deep n-well and typically used to isolate p-wells from the p-substrate. The spacing between the p-type implant to bias the p-substrate and the n-type implants to bias the collecting deep n-well is 3 µm, which fixes the breakdown voltage of the sensor at around -60 V. The implants to bias the sensor electrodes and the necessary spacing between them limit the area of the pixel that can be occupied by the readout electronics to 57% of the total, although only 43% is used in this particular design. The pixel has multiple n-well and p-well pairs, where each one of these pairs hosts one of the several circuits of the readout electronics (i.e., analogue, CMOS comparator and purely digital). To embed the CMOS comparator and digital readout electronics in the sensing area of the pixel, buried deep p-wells (PSUB) are used to provide electrical isolation between the n-wells and the collecting deep n-well. There is a 1 µm overlap between each deep p-well and its neighbouring p-wells to avoid punch-through between the n-wells and the deep n-well [5]. The total parasitic capacitance of the pixel is around 250 fF at -50 V of bias voltage, with contributions from the p-substrate/deep n-well ($C_{SUB/DNWELL}$) and deep p-well/deep n-well ($C_{PSUB/DNWELL}$) junctions being 79 fF and 171 fF

respectively. The larger parasitic capacitance of the deep p-well/deep n-well junction is due to the large parasitic capacitance per area of this type of junction. The presence of deep p-well in the sensing area of the pixel is therefore as minimal as possible, with one deep p-well dedicated to the CMOS comparator and another one dedicated to the digital readout electronics. The parasitic capacitance of the deep p-well/deep n-well junction for the CMOS comparator ($C_{PSUB/DNWELL-COMP}$) is 80 fF, while that for the digital readout electronics ($C_{PSUB/DNWELL-DIG}$) is 91 fF.

The schematic of the analogue readout electronics is shown in figure 3. These include a high impedance circuit to bias the collecting electrode (R_{BIAS} in figure 3), a Charge Sensitive Amplifier (CSA) based on a single-ended folded cascode amplifier with a pMOS transistor as input and continuous reset, low-pass and high-pass filters, and a CMOS comparator with a 4-bit DAC to locally tune small threshold voltage variations due to offset. The sensing diode is AC coupled to the CSA (C_{AC}) to allow the deep n-well and the input node of the CSA to be at different DC voltages. The feedback capacitor of the CSA (C_{FB}) is implemented by means of the drain-bulk capacitance of the pMOS transistor of the cascode stage (M1). The 4-bits for trimming the threshold voltage (V_{TH}) of the CMOS comparator are stored in an in-pixel SRAM. For performance evaluation purposes, the readout electronics include a charge injection circuit. By applying a voltage pulse generated off-chip (V_{INJ}) to the injection capacitor (C_{INJ}), the equivalent charge is sensed and amplified by the CSA. One pixel flavour only with linear transistors has been implemented in this matrix. The simulated Equivalent Noise Charge (ENC) of the pixel is around 100 e^-, while the time-walk for an input charge between 1k and 20k e^- is 11 ns. The power consumption of this pixel is 23 μW.

The digital readout electronics include an edge detector, processing electronics based on flip-flops and other logic gates, an 8-bit ROM to store the pixel address and two 8-bit DRAMs to store the Leading Edge (LE) and Trailing Edge (TE) time-stamps. The pixel address is hard-wired in the pixel, while the time-stamp is generated by an 8-bit Gray-encoded counter that runs at a maximum speed of 40 MHz at the periphery of the matrix. The output of the CMOS comparator (COMPOUT) is fed into the edge detector. When there is an event in the pixel, the edge detector generates two short pulses that correspond to the LE and TE of COMPOUT. These enable the ROM to store the pixel address, and the DRAMs to store the corresponding time-stamps. The time difference between the TE and LE time-stamps gives the Time-over-Threshold (ToT), which ranges from 100 ns to 300 ns for an input charge between 1k and 20k e^- respectively, but this can only be obtained off-chip. Simultaneously to the LE and TE generation, a hit flag is asserted to prevent any new events from being processed in the pixel until the current event has been read out.

The pixel address, LE and TE are sent to an EOC circuit placed at the periphery of the matrix through a 24-bit bus that is shared by all the pixels within a column. To avoid overwriting this bus with information from pixels of the same column that have sensed events while the bus is busy, the pixels include a priority system based on a NAND-NOR chain. With this priority system, the pixels with the largest address (i.e., closest to the EOC circuit) are read out first. Each column of the matrix has one EOC circuit, which stores the pixel address, LE and TE in two 16-bit registers. The 78 EOC circuits of the matrix function as two 16-bit parallel-in parallel-out shift registers (i.e., one shift register for the pixel address and another one for the LE and TE time-stamps). The two 16-bit parallel outputs of the shift registers are connected to two readout serializers that are designed to run at a maximum speed of 640 MHz provided by an externally generated clock. Like

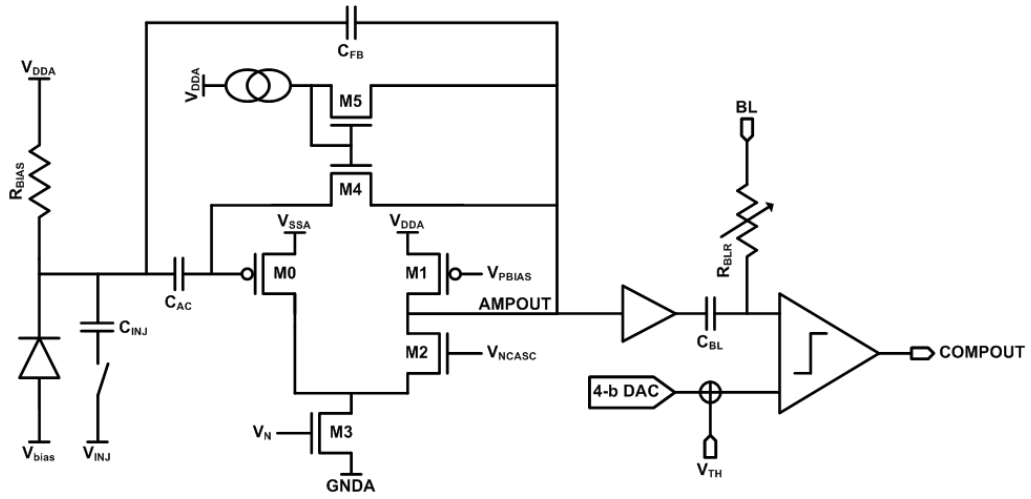

Figure 3 Schematic of the analog readout electronics of RD50-MPW1.

that of the FEI3 readout ASIC the architecture of RD50-MPW1 is untriggered, but it cannot do on-chip time-walk compensation, buffering or zero suppression. The global bias circuit, and horizontal and vertical configuration registers, are accessed through a low-speed serial input stream.

3. Experimental evaluation of RD50-MPW1

Figure 4 (a) shows the current-to-voltage (I-V) curves of RD50-MPW1. These I-V curves were measured with the passive test structures for characterising the sensor depletion region, specifically using the central pixel of a 3 x 3 matrix. The pixels of this matrix have the same size and cross-section as the pixels of the matrix for particle physics experiments. The measurements were carried out with a probe station, placing the naked dies directly on a chuck and contacting the pads of the sensor electrodes with needles. A Keithley K2410 was used as Source Measure Unit (SMU). The dies were non-irradiated, at room temperature and in complete darkness during the measurements. The breakdown voltage of the sensor is -56 V, as expected from the design. The leakage current, however, reaches the μA order before -20 V of bias voltage. This result is unexpected and extremely higher than the usual nA values before the breakdown voltage [4]. Further investigation revealed that the high leakage current is due to the lack of guard ring structures enclosing the ASIC and other issues that will be discussed in detail in the next section.

Several RD50-MPW1 samples were irradiated with neutrons in the TRIGA reactor in Ljubljana to fluences ranging from $1 \cdot 10^{13}$ 1 MeV n_{eq}/cm^2 to $2 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 [6] and measured with the edge-Transient Current Technique (e-TCT) to study the depletion region of the sensor [7]. In e-TCT measurements, the edge of the detector is typically scanned with a laser beam of infrared light (λ = 1064 nm) to create electron-hole pairs at a known depth. The generated charge carriers drift in the electric field of the sensing diode and induce current in the collecting electrode, which is amplified and recorded. By integrating this signal over the collecting time with an analysis script, the collected charge can be mapped as a function of the position at which the charge was generated in the sensor bulk and therefore the depletion depth can be obtained. The laser beam is focused, collimated and pulsed in the sub-nanosecond range. High-precision motorized XYZ stages control the position of the laser beam and the detector. In the measurements described here, the test structure that consists of a 3 x 3 matrix of 50 μm x 50 μm passive pixels

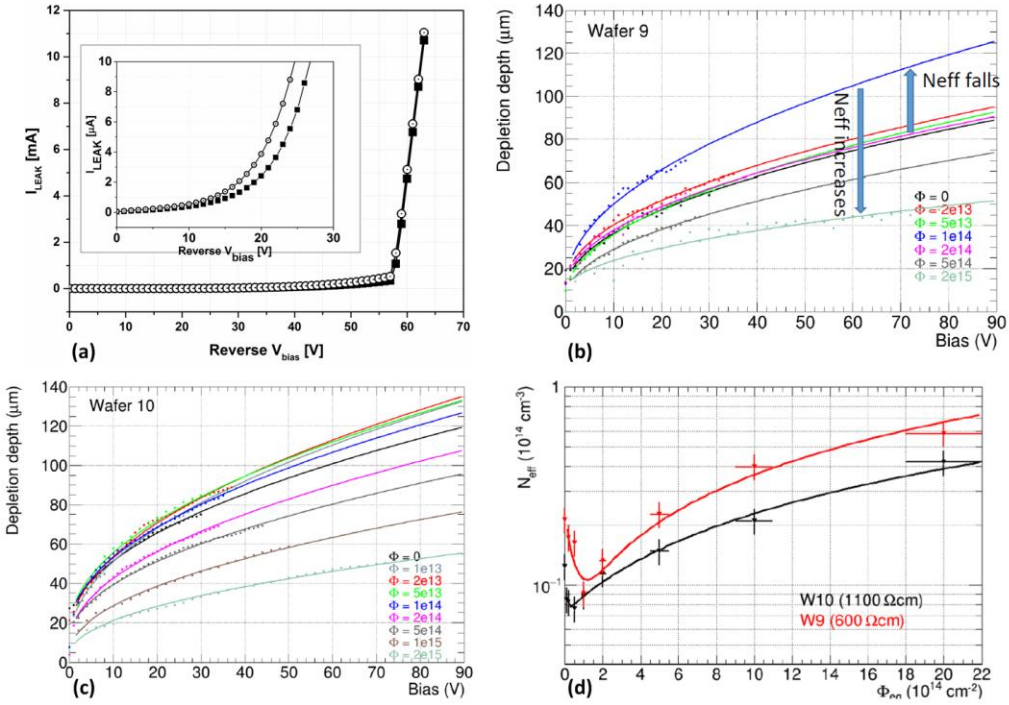

Figure 4 Performance evaluation of RD50-MPW1: I-V curves of the 600 Ω·cm (squares) and 1.1 kΩ·cm (circles) wafers (a), depletion depth before and after neutron irradiation of the 600 Ω·cm (b) and 1.1 kΩ·cm (c) wafers [8], and initial doping concentration as a function of 1 MeV neutron equivalent fluences (d) [8].

was evaluated. In particular, the depletion region of the central diode of this matrix was characterised while the outer diodes were connected to ground. Figure 4 (b) and (c) show the depletion depth as a function of the sensor bias voltage for the different neutron fluences to which the samples were irradiated and the two high resistivity substrates in which RD50-MPW1 was fabricated. The depletion depth w is defined as the FWHM of the measured charge collection profile and fitted with:

$$w = w_0 + \sqrt{\frac{2\varepsilon_0\varepsilon_r}{e_0 N_{eff}} V_{bias}} \quad (1)$$

where w_0 is the depletion depth at zero bias voltage, ε_0 the dielectric constant, ε_r the relative permittivity of silicon, e_0 the elementary charge, N_{eff} the effective space charge concentration and V_{bias} the bias voltage. The depletion depth grows with the bias voltage before and after irradiation in accordance with equation (1). Before irradiation, depletion depths greater than 60 μm and 90 μm are achieved at -50 V with the 600 Ω·cm and 1.1 kΩ·cm resistivity substrates respectively. After irradiation to low fluences, the depletion depth gradually increases due to initial acceptor removal effects. This phenomenon is commonly observed in silicon sensors with relatively low resistivity substrates [9]. After irradiation to higher fluences, the depletion depth decreases due to radiation induced deep acceptors. The depletion depth of RD50-MPW1 has a value of more than 40 μm after a fluence of $2 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 at -50 V for both resistivity substrates. Figure 4 (d) shows N_{eff} as a function of the neutron fluence, which was estimated from the fit to equation (1). This plot reveals that the fluence at which the initial acceptor removal finishes is larger for the detector in the 600 Ω·cm resistivity substrate than that for the 1.1 kΩ·cm resistivity substrate, as found in other detectors. The behaviour of N_{eff} is described by the function:

$$N_{eff} = N_{eff0} - N_C \cdot \left(1 - exp\left(-c \cdot \Phi_{eq}\right)\right) + g_C \cdot \Phi_{eq} \quad (2)$$

where N_{eff0} is the initial doping concentration, N_c the concentration of acceptors that are removed, c the acceptor removal constant, g_c the deep acceptor introduction rate and ϕ_{eq} the 1 MeV equivalent neutron fluence. This function was fitted to the neutron irradiation data. The acceptor removal constant c is found to be larger in the less doped bulk [10]. In particular, its value is $1 \cdot 10^{-14}$ cm^2 and $14 \cdot 10^{-14}$ cm^2 for the 600 Ω·cm and 1.1 kΩ·cm resistivity substrates respectively.

To evaluate the performance of the monolithic matrices, a Data AcQuisition (DAQ) system was developed. This consists of a dedicated chip carrier board, a general purpose Control and Readout (CaR) mother board [11], an FPGA Mezzanine Card (FMC) and a Xilinx ZC706 evaluation board. There exists another DAQ available to measure RD50-MPW1 [12], but this will not be discussed here. An Agilent E3547A power supply was used to power the ASIC and satellite readout electronics, and a Keithley K2410 SMU was used to bias the substrate of the chip. Figure 5 (a) shows the hit map of the matrix for particle physics experiments, where the pixels were stimulated by applying a square voltage pulse with amplitude V_{INJ} = 1.8 V to the in-pixel charge injection circuit. The voltage pulse was generated off-chip by the CaR and evaluation boards, applied to one pixel at a time a certain number of times (22 times in this hit map) and read out. The hit map shows the number of times that the pixels sensed an event (i.e., they provided their address) when they were stimulated. This measurement was carried out with a 1 MHz clock speed. Ideally, the number of voltage pulses applied to the pixels and the number of times the pixels sensed an event should match. However, the hit map reveals there is mismatch in some pixels. This issue is being investigated at the moment.

To evaluate the noise performance of the matrix for particle physics experiments, threshold scans were performed. Figure 5 (b) shows the so-called S-curve of one pixel of this matrix. This plot was obtained by keeping the threshold voltage of the CMOS comparator constant at V_{TH} = 0.8 V and varying the amplitude of the voltage pulse in steps of 3 mV. For each amplitude, 1000 voltage pulses were injected to the pixel and the number of times the pixel sensed an event was recorded. The S-curve plots this last number against the amplitude of the voltage pulse. The width of the S-curve gives the total noise of the pixel, which is 49.69 mV (i.e., 0.26 fC) with an input signal of 2.52 fC in this case. The hit map and the S-curve were obtained with non-irradiated samples in the 1.1 kΩ·cm resistivity substrate.

4. Design of RD50-MPW2

The main motivation behind RD50-MPW2 is to develop new methods to minimize the leakage current of RD50-MPW1, as well as faster CSAs to improve the response time of the sensor and peripheral readout electronics. RD50-MPW2 integrates one matrix with two active pixel flavours for fast response times, a Single Event Upset (SEU) tolerant memory array with eight cell flavours, a bandgap reference voltage and test structures with several passive pixel flavours. The prototype ASIC, which has a size of 3.2 mm x 2.1 mm, is in the standard resistivity substrate of 10 Ω·cm and in 3 high resistivity substrates with nominal values of 100 Ω·cm, 1.9 kΩ·cm and 3 kΩ·cm. The following paragraphs will present the design of the new methods to minimize the leakage current and of the matrix with active pixels for fast response times.

RD50-MPW1 has a seal ring with a p-well that encloses the ASIC (i.e., located outside the pad frame) for protection against mechanical stress and contamination originated during the die

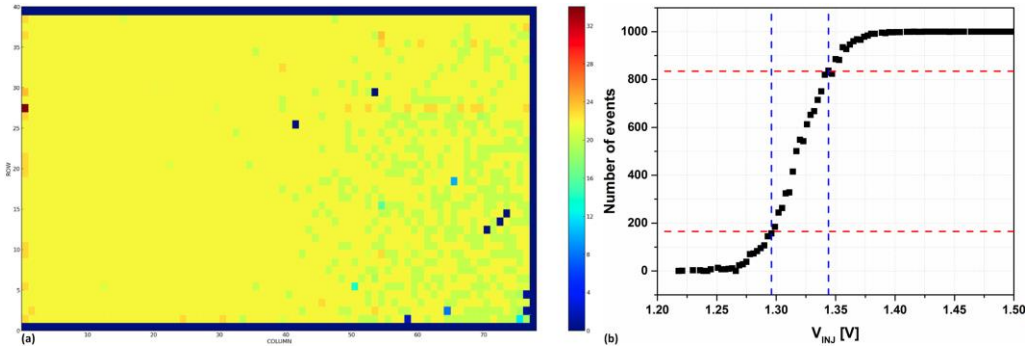

Figure 5 Performance evaluation of RD50-MPW1: Hit map (a) and S-curve (b).

sawing process. However, it lacks any guard rings to specifically prevent the depletion region of the sensing diodes from coming into contact with the edge of the device. It is well known that this has a negative effect on the leakage current and breakdown voltage, and therefore also on the noise level and radiation tolerance of the detector [13]. To develop an optimised guard ring frame for RD50-MPW2, extensive Technology Computer-Aided Design (TCAD) simulations were performed. The effects on the leakage current by the large presence of filling layers that the foundry typically adds in certain regions of the ASIC for the ease of the manufacture process, as well as on the breakdown voltage by the geometry of the pixels, were also simulated.

RD50-MPW2 has a guard ring frame that consists of one n-well ring, several p-type rings with constant width and increasing spacing towards the edge of the ASIC and a seal ring. It has a total width of 150 µm. The n-well ring, located in the inner part of the guard ring frame and connected to the power supply voltage, acts as a current collecting ring. The p-type rings, which surround the n-well ring and can be either connected to the sensor bias voltage or floating, control the termination of the lateral depletion region of the sensing diodes towards the edge of the ASIC. RD50-MPW2 implements 6 p-type rings, as TCAD simulations revealed that the lateral depletion region reaches its minimum value at this number. Each p-type ring consists of a p-well in a deep p-well. The deep p-well further reduces the lateral depletion region, as shown in figure 6. The filling layers added by the foundry involve conductive material and contribute significatively to the large leakage current of RD50-MPW1. They were eliminated in all the p-n junctions of RD50-MPW2 with a high voltage drop between their electrodes (i.e., in the pixels, the peripheral readout circuits and the pads). In other regions where it was not possible to eliminate these structures, they were placed in a p-well to minimize their effects. In relation to the geometry of the pixel, two improvements were made in RD50-MPW2. The spacing between the implants of the p-n junction was increased to 8 µm to achieve a breakdown voltage better than -100 V and the corners of the sensing layers were round shaped to avoid electric field peaks.

Figure 7 shows the layout views of RD50-MPW2 and of one of the pixel flavours for fast response times to resolve particles at higher rates. The matrix with these pixels integrates 8 rows x 8 columns of pixels, a global and programmable bias circuit with 6-bit DACs, 8 horizontal and 8 vertical configuration registers, 8 End Of Column (EOC) circuits and 49 pads. The pixels, which have a size of 60 µm x 60 µm and the same cross-section as the pixels of RD50-MPW1 (see figure 2), integrate analogue readout electronics only. These are very similar to those in RD50-MPW1, however RD50-MPW2 integrates two new CSA flavours that optimise the response time (i.e., the rise and fall times) of the amplified sensor signal without increasing the power consumption. In one of the CSA flavours the reset is continuous like in RD50-MPW1, while in the other one it is

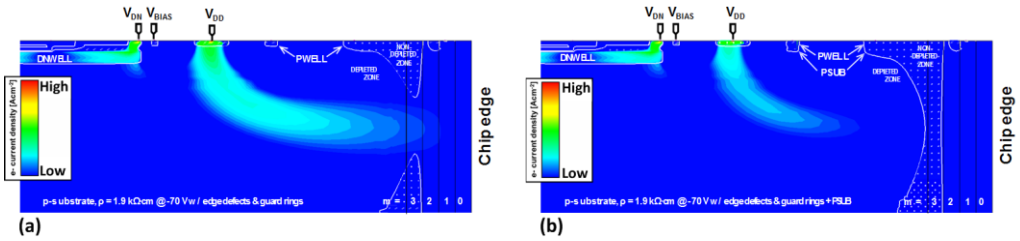

Figure 6 TCAD simulations of one pixel and the edge of the chip with a guard ring frame: without deep p-well (a) and with deep p-well (b) in the p-type guard rings.

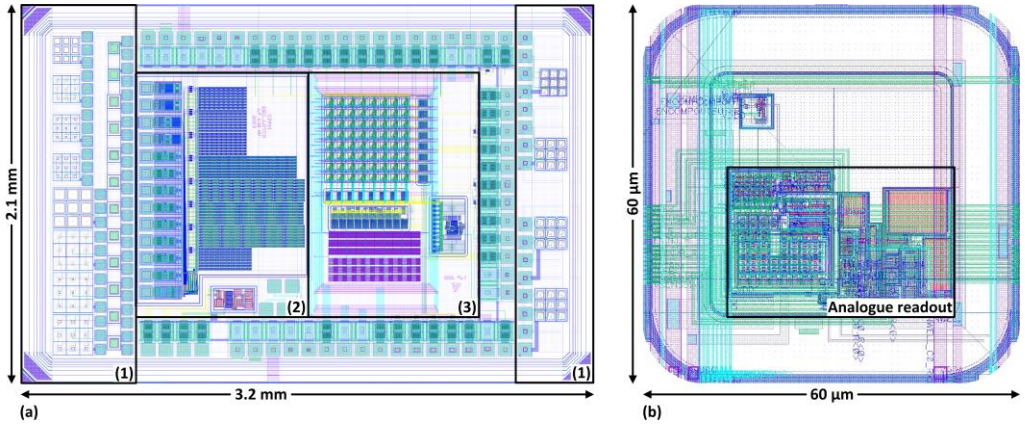

Figure 7 Layout views: RD50-MPW2 (a) and pixel of the matrix for fast response time (b). Regions (1), (2) and (3) in (a) correspond to the test structures, the peripheral readout electronics and the matrix for for fast response times respectively.

switched. In the continuous reset flavour there is a constant current flowing through the feedback branch of the CSA, which discharges the pixel in a linear way after each event. In the switched reset flavour, in contrast, for a very short time interval there is a larger current in addition to the constant feedback current. The larger current, which is controlled by the output of the CMOS comparator and switched on every time this one is high (i.e., COMPOUT = V_{DD}) after having sensed an event, discharges the pixel in a non-linear and sharp way. To reduce the rise time, the transconductance (g_m) of the CSA input transistor (M0 in figure 3) was optimised in both flavours. To reduce the fall time, the switched reset flavour was developed. Switched reset pixels have been explored in previous works, but the reset frequency was limited to the speed of the clock signal that is used to control the switched feedback current [14]. The outputs of the CSA and of the comparator of all the pixels of the matrix can be read out via dedicated pads or through an analogue buffer. As RD50-MPW2 is a prototype ASIC aimed at testing the leakage current and response time of the sensor, it does not integrate any digital readout electronics. RD50-MPW2 was delivered in January 2020 and is being tested at the moment. Table 1 compares the performance of the pixel flavour of RD50-MPW1 with the two pixel flavours of RD50-MPW2. This table shows that the optimisation of the response time of the amplified signal results in an improvement of the time resolution or time-walk in both pixel flavours.

5. Conclusion

Two prototype ASICs named RD50-MPW1 and RD50-MPW2 have been developed within the CERN-RD50 collaboration to further improve the performance of depleted CMOS sensors. The pixel size of 50 µm x 50 µm of RD50-MPW1 with all the analogue and digital readout

Input signal: 5 ke$^-$	Gain (μV/e$^-$)	ENC (e$^-$)	Response time (ns)	Time-walk (ns)	Consumption (μW)
RD50-MPW1 – Continuous	30	115	125	11	23
RD50-MPW2 – Continuous	50	120	53	7.8	24
RD50-MPW2 – Switched	80	100	32	6.4	25

Table 1 Simulated performance of the pixels in RD50-MPW1 and in RD50-MPW2.

electronics for column drain readout in the sensing area of the pixels is unprecedented. RD50-MPW2 integrates new methods to optimise the leakage current and response time of the sensors.

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