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Time resolution and radiation tolerance of depleted CMOS sensors

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Depleted Monolithic Active Pixel Sensors (DMAPS), also known as depleted CMOS sensors, are extremely attractive for particle physics experiments. As the sensing diode and readout electronics can be integrated on the same silicon substrate, DMAPS remove the need for hybridization. This results in thin detectors with reduced production time and costs. To achieve high speed and high radiation tolerance, DMAPS are manufactured in High Voltage (HV) processes on High Resistivity (HR) wafers. Today's most performant DMAPS are 50 µm thin and have 50 µm x 50 µm cell size with integrated mixed analog and digital readout electronics, 11 ns time resolution and 5 x 10^{15} 1 MeV n_{eq}/cm^2 radiation tolerance. DMAPS in HR/HV-CMOS have been adopted as the sensor technology for the pixel tracker for the Mu3e experiment and are under consideration for the ATLAS detector Phase-II Upgrade. However, in spite of the major improvements demonstrated by DMAPS, further research to achieve even more performant sensors is needed to realize the full potential of these sensors to meet the most challenging requirements for particle physics experiments planned for the future. This article describes the state-of-the-art of DMAPS in terms of time resolution and radiation tolerance, and presents specific work done by the CERN-RD50 collaboration to further develop the performance of these sensors.

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1. Introduction

The much increased luminosity expected at the next generation of experiments in particle physics requires tracker detectors with ever finer segmentation and time resolution to successfully resolve the much larger number of tracks. Radiation tolerance is critical as well, as detectors need to survive many years of operation. The Future Circular Collider for proton-proton collisions (FCC-hh), for example, requires tracking detectors with approximately 25 μm x 50 μm cell size, better than 100 ps time resolution and 10^{16} - 10^{17} 1 MeV n_{eq}/cm^2 radiation tolerance [1, 2]. Despite the substantial progress made during the last years in the development of novel tracking detectors, such as thin planar active-edge sensors [3], Low Gain Avalanche Detectors (LGADs) [4], 3D sensor technologies [5, 6], Monolithic Active Pixel Sensors (MAPS) [7] and Depleted MAPS (DMAPS) [8, 9], these requirements are still beyond the reach of state-of-the-art detectors and further research is needed.

DMAPS, which offer a competitive and cost-effective radiation tolerant solution in comparison to hybrid silicon sensors over a large range of applications, can become the sensor technology of choice for the next generation of experiments in particle physics. This article addresses the time resolution and radiation tolerance of DMAPS and summarizes the techniques that are available or under development to improve these parameters, including the work done by the CERN-RD50 collaboration to develop these sensors [10].

2. DMAPS

DMAPS, also known as depleted CMOS sensors, are position sensitive detectors in industry standard CMOS processes. These sensors are extremely attractive for experiments in particle physics as they integrate the sensing element and the readout electronics in a single layer of silicon, which removes the need for interconnection with complex and expensive solder bump technology. DMAPS also benefit from faster turnaround times and lower production costs when compared to the planar silicon sensors used in hybrids.

To achieve substantial depletion in the sensing volume and improve the speed and radiation tolerance of the detector, DMAPS implementations can follow two different approaches known as low fill-factor and large fill-factor. Low fill-factor DMAPS benefit from High Resistivity (HR) substrates and thick epitaxial layers accessible from CMOS imaging processes, while large fill-factor DMAPS exploit the High Voltage (HV) option developed by CMOS foundries for power electronics. Recently, HR wafers have also become available in the production line of foundries that manufacture HV-CMOS processes, and DMAPS in HR/HV-CMOS are now also possible to further improve the performance of the sensor [11-13]. Today's most performant DMAPS detectors are 50 μm thin and have 50 μm x 50 μm cell size with integrated mixed analog and digital readout electronics [14], 11 ns time resolution [15] and 5 x 10^{15} 1 MeV n_{eq}/cm^2 radiation tolerance [16].

The typical cross-section of a large fill-factor DMAPS pixel, in a HR/HV-CMOS process, is shown in figure 1. The deep n-well, which together with the p-substrate makes the sensing junction, also hosts the low-voltage readout electronics. A high-voltage is applied to the p-substrate to create a strong electric field and large depletion region below the deep n-well. When

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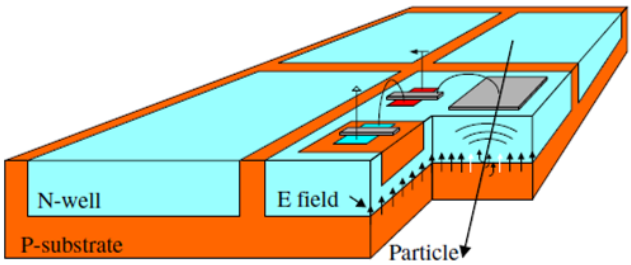

Figure 1 Cross-secton of four large fill-factor DMAPS pixels [8].

a particle traverses the detector, electron-hole pairs are created along the particle path. The electrons drift towards the deep n-well under the influence of the strong electric field. This generates the input signal, which is amplified and processed by the in-pixel readout electronics. As the electrons move by drift, the charge collection is fast and less sensitive to increased noise and trapping effects related to radiation damage when compared to traditional MAPS where charge collection is by diffusion. DMAPS in HR/HV-CMOS processes have been adopted as the sensor technology of choice for the pixel tracker for the Mu3e experiment at the Paul Scherrer Institute (PSI) in Switzerland [17]. DMAPS are also developed for the Inner Tracker (ITk) of the ATLAS detector Phase-II Upgrade, for which the final decision on whether to use them is expected in 2019, and the vertex detector of the proposed Compact Linear Collider (CLIC) [18].

3. Time resolution

The time resolution is defined by the accuracy of the measurement of the time of arrival or time at which a particle traverses the detector. The time of arrival is typically measured by setting a threshold voltage and recording the time at which the signal induced by a traversing particle exceeds the threshold. Its accuracy is limited by the charge collection time of the sensor and the response time of the readout electronics. In DMAPS the main charge collection mechanism is drift and lasts a few hundred ps only. The response time of the readout electronics depends mostly on the rate at which the amplifier can react to a change at its input. Particles that deposit different amounts of energy in the detector induce signals with different amplified amplitudes but also with different rise times, as shown in figure 2. Consequently, they surpass the threshold voltage and are detected at different times. This detection time difference is known as time-walk and dominates the time resolution.

The intrinsic time resolution of the most advanced DMAPS at present ranges between approximately 15 and 60 ns, depending on the process technology. However, to meet the requirements of planned and future experiments in particle pysics, this parameter needs to be improved. Traditionally, the time-walk is corrected offline using time measurements or time-stamps that correspond to the leading and trailing edges of the signal induced by the particle when this crosses the threshold voltage in the positive and negative transitions. Various studies, discussed in more detail in the next subsections, have shown that on-chip time-walk correcting methods improve the time resolution of DMAPS substantially. Other studies have also been performed to evaluate the dependence of the time resolution on the resistivity of the substrate of the detector [19]. The very small dependence observed further confirms that the time resolution is predominantly determined by the response of the readout electronics.

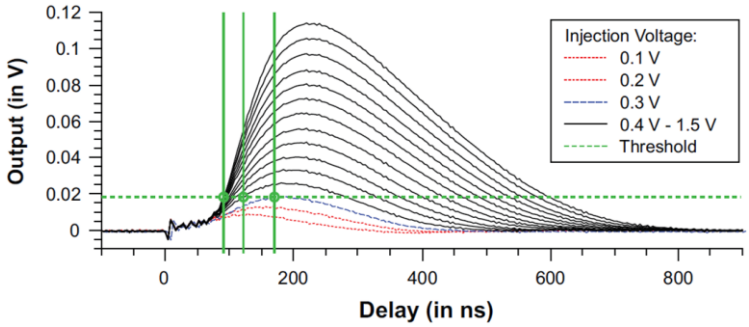

Figure 2 Time-walk on signals of different amplitudes [22].

3.1 Increasing the response rate of the amplifier

The easiest solution to improve the time resolution is to increase the response rate of the amplifier, but the higher bias current typically needed for this also increases the power consumption of the sensor. One example is the CMOS Active Timing μSensor (CACTUS) chip, a 1 cm x 1 cm monolithic pixel sensor chip dedicated to timing measurements [20]. This prototype uses very large pixels of 1 mm pitch with large power consumption per pixel, but acceptable in terms of the power consumption per unit area (145 mW/cm^2), to achieve in simulations very fast signal amplification with less than 1 ns rise time and accurate time resolution of better than 100 ps per Minimum Ionizing Particle (MIP). This solution works well for certain applications that require high accuracy on timing but are more relaxed on position resolution, like the High-Granularity Timing Detector (HGTD) [21]. It is not suitable, however, for tracking detectors for most future experiments in particle physics where small pixel size is essential.

3.2 Time-walk compensated comparator

The main idea behind the Time-Walk Compensated Comparator (TWCC) method is to use more time to improve the time resolution [22]. This method is implemented with two comparators with different threshold voltages and additional circuitry based on a dynamic voltage divider discharging a capacitor. A threshold crossing in the first comparator triggers the additional circuitry, which uses the amplitude of the amplified signal to control how much delay is added. Larger signals, with faster rise times, induce longer delays. The second comparator digitizes the time-walk compensated amplified signal and delivers the time-stamp. This method has been implemented in a few chips with depleted CMOS sensors, such as the HVStripV1 and H35DEMO (50 μm x 250 μm pixel size, and approximately 200 mW/cm^2 analog power consumption) prototypes for the ATLAS upgrade. The TWCC method has proved to be efficient in improving the time resolution to below 25 ns, as required by the High Luminosity-Large Hadron Collider (HL-LHC), for input signals that generate between 1k and 10k electrons in the sensor.

3.3 2-threshold method

The 2-threshold method also uses two comparators with different threshold voltages, as shown in figure 3 (a), but the mechanism behind it is different from that of the TWCC [13]. The first threshold voltage is very low, close to the noise level, to deliver a time-stamp with small

time-walk. However, given its proximity to the noise level, a higher second threshold voltage is needed to confirm that the flagged time-stamp corresponds to a real signal and not to noise. This method has been implemented in the MuPix8 prototype for the Mu3e experiment, a 1 cm x 2 cm monolithic sensor chip with 80 μm x 81 μm pixel size and 215 mW/cm^2 power consumption. The MuPix8 prototype has a measured intrinsic time resolution of about 11 ns for the whole chip. This value can be further improved to 6 ns afer time-walk corrections with the 2-threshold method and compensations of the delay effect [15, 17]. A limiting factor on the time resolution of this chip is the delay effect, as pixels with a higher column or row address have a larger latency due to voltage drops along the pixel matrix. This effect is relevant in DMAPS that have analog readout electronics inside the sensing area of the pixel and the comparator and digital readout electronics at the periphery of the detector chip. Note that in this method the time-walk corrected time resolution includes offline Time over Threshold (ToT) corrections with data acquired on-chip with the lower threshold voltage. While the improved time resolution of 6 ns meets the requirement of 20 ns needed for the Phase-I of the Mu3e experiment, this value is still far from the better than 1 ns time resolution that is necessary for the Phase-II.

3.4 Ramp method

The ramp method uses one comparator with a constant threshold voltage and another comparator with a dynamic threshold voltage, as shown in figure 3 (b). The dynamic threshold voltage is a linearly rising voltage, or ramp, with adjustable delay and slope. When the amplified signal exceeds the constant threshold, the time-stamp is recorded and the dynamic threshold is triggered. When the amplified signal drops below the dynamic threshold, a second time-stamp is recorded. The time difference between these two time-stamps gives the ToT. Knowing the ToT, in addition to the delay and slope of the linearly rising voltage, the ramp method can be used to obtain the amplitude of the amplified signal. This method has been implemented in the MuPix8 prototype as well, allowing to improve the time resolution to around 8 ns in the best case after ToT correction [15]. Here the improvement of the time resolution is less than that achieved with the 2-threshold method due to power distribution and implementation issues in the digital part of the chip [17]. Note that this method does not constitute an on-chip time-walk correcting method, but an alternative way of generating ToT information for offline corrections. However, it has advantages over more traditional ways of generating ToT information, as the time-stamps are sampled faster and the noise distribution is lower due to the angle of the dynamic threshold to the baseline voltage.

3.5 Sampling method

An alternative way of minimizing the time-walk typical of DMAPS consists in sampling the leading edge of the amplified signal and fitting a linear equation to the obtained data points. The intersection between the fitted leading edge and the baseline voltage gives the time of arrival with high accuracy. There are different proposals for the on-chip implementation of this method.

A first proposed method uses a number of Sample and Hold (S/H) circuits with analog memories implemented as capacitors that follow the output voltage of the amplifier, until stop sampling signals are issued after a particle hit [12]. When that happens, the capacitors retain their

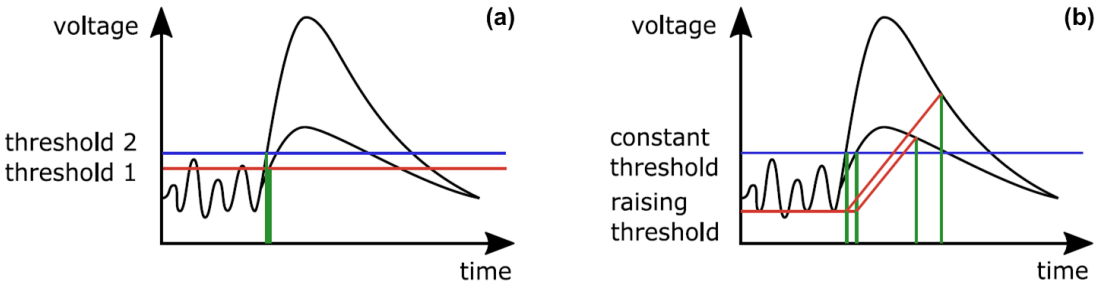

Figure 3 Schematic representations of the 2-threshold (a) and ramp (b) methods [13].

charges. These charges correspond to specific voltage points of the leading edge of the amplified signal. The control signals for the S/H circuits, which are shifted in time by multiples of the sampling period, are generated at the periphery of the detector chip and combined with a trigger signal inside the pixel to stop the sampling and enter the hold mode. To fit all the points on the leading edge, the sampling frequency has to be high enough. For readout and digitization of the stored charges, this method uses simple ramp Analog-to-Digital Converters (ADCs) that inject a constant current to the capacitors. The times at which the discharging voltages intersect a reference voltage are stored as time-stamps. The discharging times give the voltage points of the amplified signal. This sampling concept with 6 sampled voltage points has been implemented in the LF-ATLASPix chip for the ATLAS upgrade, achieving a time-walk of less than 10 ns in measurements [22]. However, this sampling method seriously increases the amount of information to be read out from the sensor. In LF-ATLASPix, the sampling information requires 48 additional bits (6 samples with 8 bits each) that need to be read out in addition to the typical hit information of 32 bits (8 bit column address, 8 bit row address and 16 bit time-stamp). To minimize this issue, future prototypes could include logic to calculate the time of arrival on-chip. In spite of this, the sampling method provides important benefits as it improves the time resolution significantly.

A second proposed method also uses S/H circuits to follow the leading edge of the output of the amplifier and store a number of voltage points, however these circuits include a chain of delay elements to generate the stop sampling signals inside the pixel and not at the periphery of the detector chip. The delay elements are triggered initially by a fast comparator and include means to program the period that separates the stop sampling signals between them. The real novelty of this method relies on using the S/H circuits in combination with a Time-to-Digital Converter (TDC) to further improve the time resolution. The TDC involves the generation of a high frequency clock signal, while keeping the power consumption at an acceptable level. The detection of a particle hit triggers the fast comparator and consequently the chain of delay elements, such that the capacitors enter the hold mode. The first sampled voltage point is tagged with its corresponding time-stamp, which is provided by the TDC generated clock signal. The time tags for the subsequent sampled voltage points are obtained by adding to the time-stamp the corresponding number of periods between stop sampling signals. Time resolutions of approximately 2 ns have been achieved in simulations with 5 sampled voltage points [23]. A DMAPS matrix with electronics that implement this sampling method inside the sensing area of the pixel is foreseen to be included in a future submission in the 150 nm HR/HV-CMOS node

from LFoundry, currently being designed by the CERN-RD50 collaboration. This matrix will also include a high-speed ADC to digitize the analog values at the end of each column.

4. Radiation tolerance

Radiation tolerance studies of DMAPS in 150 nm and 180 nm processes have been conducted mostly in the context of the ATLAS upgrade. Several test and demonstrator chips have been irradiated to doses and integrated particle fluences of up to several hundred MRad and several 10^{15} 1 MeV n_{eq}/cm^2 respectively. The next subsections describe the results of these studies.

4.1 150 nm HR/HV-CMOS node from LFoundry

Unthinned devices of 700 μm with topside biasing and thinned devices of 200 μm with backside biasing in the 150 nm HR/HV-CMOS node from LFoundry have been irradiated with neutrons for a range of fluences [24]. Measured results show that the depletion depth of unirradiated devices grows with the bias voltage very similarly in both cases, until the thinned devices reach full depletion. Despite the steady decrease of the depletion depth with increasing fluence, typical of high-resistivity p-type substrates due to radiation introduced deep acceptors, large depletion depths of more than 50 μm are maintained up to the highest measured fluence of 2 x 10^{15} 1 MeV n_{eq}/cm^2. This behaviour differs from that observed in devices with low resistivity p-type substrates, where the depletion depth first increases and then decreases as a result of initial acceptor removal dominating the behaviour of the depletion depth at fluences below 10^{15} 1 MeV n_{eq}/cm^2. At very high fluences, when acceptor removal is finished, the effective doping concentration is similar in all substrates regardless of the initial resistivity [25]. Measurements of the charge collection efficiency with a ^{90}Sr source to emulate MIPs reveal a signal reduction of approximately 30% after neutron irradiation to 10^{14} 1 MeV n_{eq}/cm^2 for the unthinned devices. In contrast, for the thinned devices, more than 4k electrons are collected after irradiation to a fluence of 2 x 10^{15} 1 MeV n_{eq}/cm^2 as a voltage of over 350 V can be used to bias the device [24]. The effects of ionizing radiation on the performance of the readout electronics have been evaluated using X-rays up to doses of 50 Mrad [26]. The measurements show a degradation of the gain of the readout electronics of less than 30% at the maximum measured dose. The hit efficiency of LF-Monopix1, a fully monolithic demonstrator for the ATLAS upgrade, has been measured to be 98.9% after neutron irradiation to 10^{15} 1 MeV n_{eq}/cm^2 [26].

4.2 180 nm HR/HV-CMOS node from ams and TSI

Measurements to study the depletion depth of devices in the 180 nm HV-CMOS node from ams are available in [27]. The hit efficiency of ATLASPix1, a fully monolithic demonstrator for the ATLAS upgrade, has been measured to be better than 99% after neutron irradiation to 10^{15} 1 MeV n_{eq}/cm^2 [28]. The chip prototypes MuPix7 for the Mu3e experiment and ATLASPix2 for the ATLAS upgrade, which were originally fabricated in the ams process, have been fabricated in the TSI process as well. Preliminary results of the TSI produced MuPix7 sensors are consistent with those obtained with previous samples in the ams process.

4.3 180 nm HR-CMOS node from TowerJazz

Although the 180 nm HR-CMOS node from TowerJazz only allows low voltages to bias the substrate, devices fabricated in this process achieve a radiation tolerance of 10^{13} 1 MeV n_{eq}/cm^2 due to the utilization of substrate materials with very high resistivities [29]. Aimed at improving the radiation tolerance of devices in this process for their application in high radiation environments, an innovative modification that consists in adding a uniform n-implant in the epitaxial layer to extend the lateral depletion has been developed in collaboration with the foundry. First results obtained with sensors implemented on the Investigator test chip using the modified process are encouraging, as the sensors remain fully functional even after irradiation to 10^{15} 1 MeV n_{eq}/cm^2 [9]. However, more recent results with the demonstrator TJ-Monopix also in the modified process show a decrease of its hit efficiency from 97.09% before irradiation to 69.42% after neutron irradiation to 10^{15} 1 MeV n_{eq}/cm^2 [30]. Other studies conducted with another demonstrator chip, named MALTA, show low in-pixel efficiency due to the inability to achieve full depletion at the corners of the pixels [30]. A test chip with a solution to fix this problem by adding a very deep p-well implant at the pixel edges to increase the lateral field has been fabricated and measured results are expected soon.

5. Development of DMAPS with the CERN-RD50 collaboration

Given the huge potential of DMAPS for future experiments in particle physics, it is a high priority for the CERN-RD50 collaboration to develop and study these sensors. Following from work in the wider community, the CERN-RD50 collaboration has started specific developments in the 150 nm HR/HV-CMOS process from LFoundry. Two test chips, named RD50-MPW1 and RD50-MPW2, have been designed and submitted for fabrication by the collaboration [14]. A large area demonstrator, named RD50-ENGRUN1, with several large matrices of pixels is being designed. Laboratory measurements of RD50-MPW1 reavealed a leakage current of the sensors that is higher than expected. This has motivated extensive device simulations using TCAD to understand the problem [31]. To minimize the leakage current, certain filling layers added by the foundry during the post-processing stage have been blocked and a series of guard rings have been included around the device to prevent the sensor depletion region from coming into contact with the edge of the chip. These modifications have been adopted in the design of RD50-MPW2, which has been submitted for fabrication recently [32]. Targeting a radiation tolerance beyond 10^{16} 1 MeV n_{eq}/cm^2, the optimized structures to minimize the leakage current and backside biasing will be used in RD50-ENRGUN1 to further improve the radiation tolerance of DMAPS. An extensive irradiation campaign is foreseen to evaluate the performance of the developed chips.

5. Conclusion

This article describes recent work on the development of DMAPS to study and improve the time resolution and radiation tolerance of these sensors for future experiments in particle physics, including work done within the CERN-RD50 collaboration. Today's most performant DMAPS detectors have 11 ns time resolution and 5 x 10^{15} 1 MeV n_{eq}/cm^2 radiation tolerance. However, several ongoing studies have revealed the time resolution can be improved substantially by adding

dedicated readout circuits to minimize the time-walk on-chip. Amongst these studies, the 2-threshold method and sampling method with a TDC have proved to be the most efficient, as they improve the time resolution to 6 ns (measured) and 2 ns (simulated) respectively. The radiation tolerance can be improved significantly by using optimized structures to minimize the leakage current and backside biasing, as currently investigated by the CERN-RD50 collaboration.

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