# Characterisation of analogue front end and time walk in CMOS active pixel sensor

B. Hiti<sup>*a*,1</sup>, V. Cindro<sup>*a*</sup>, A. Gorišek<sup>*a*</sup>, M. Franks<sup>*b*\*</sup>, R. Marco-Hernández<sup>*c*</sup>, G. Kramberger<sup>*a*</sup>, I. Mandić<sup>*a*</sup>, M. Mikuž<sup>*a*,*d*</sup>, S. Powell<sup>*b*</sup>, H. Steininger<sup>*e*</sup>, E. Vilella<sup>*b*</sup>, M. Zavrtanik<sup>*a*</sup>, C. Zhang<sup>*b*</sup>

<sup>a</sup> Jožef Stefan Institute, Ljubljana, Slovenia

<sup>b</sup>University of Liverpool, Department of Physics, Liverpool, UK

<sup>c</sup>IFIC (CSIC-UV), Valencia, Spain

<sup>d</sup>University of Ljubljana, Faculty of Mathematics and Physics, Ljubljana, Slovenia

<sup>e</sup>HEPHY, Vienna, Austria

\*now FBK, Trento, Italy

*E-mail:* bojan.hiti@ijs.si

ABSTRACT: In this work we investigated a method to determine time walk in an active silicon pixel sensor prototype using Edge-TCT with infrared laser charge injection. Samples were investigated before and after neutron irradiation to  $5 \cdot 10^{14} n_{eq}/cm^2$ . Threshold, noise and calibration of the analogue front end were determined with external charge injection. A spatially sensitive measurement of collected charge and time walk was carried out with Edge-TCT, showing a uniform charge collection and output delay in pixel centre. On pixel edges charge sharing was observed due to finite beam width resulting in smaller signals and larger output delay. Time walk below 25 ns was observed for charge above  $2000 e^-$  at a threshold above the noise level. Time walk measurement with external charge injection yielded identical results.

KEYWORDS: Charge induction, Radiation-hard detectors, Particle tracking detectors (Solid-state detectors)

<sup>&</sup>lt;sup>1</sup>Corresponding author.

#### Contents

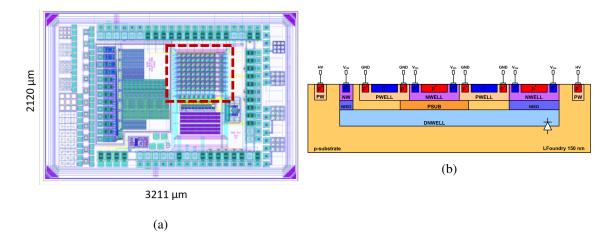
1	Introduction	1
2	Samples and measurement setup	2
3	Front end threshold, noise and calibration	3
4	Edge-TCT measurement setup	6
5	Time walk measurements with Edge-TCT	6
6	Conclusions	10

#### 1 Introduction

Active silicon tracking detectors with fully integrated readout electronics manufactured in a large volume industrial CMOS process are a potential alternative for hybrid silicon detectors at future particle colliders, promising similar performance at a simplified production and a smaller amount of material in the tracking volume. In recent years several prototypes capable of withstanding high radiation fields of the order of  $10^{15} n_{eq}/cm^2$  have been developed [1–3]. These designs, called *depleted monolithic active pixel sensors* (DMAPS), feature a depleted sensing layer providing a drift based, fast and radiation tolerant charge collection.

The efficiency of charge collection after irradiation in these sensors is determined by two main factors. The first factor is the degradation of charge collection due to displacement damage in silicon bulk caused by non-ionising energy losses (NIEL), which leads to charge trapping and reduced depletion depth at a given bias voltage due to build up of space charge. These effects have been evaluated in numerous studies with DMAPS [4–8]. Another important requirement for efficient charge collection is the so called in-time efficiency, which describes the ability of the detector to correctly match hits with the original collision event. In the LHC environment particle collisions occur every 25 ns and only hits resolved within this time window are considered as signals. The factors limiting the in-time efficiency are the speed of charge collection from the bulk and the time walk of the electronics, which describes the response delay spread for varying size signals crossing a fixed threshold level.

Typically the time walk of a chip is determined from the output delay after injecting a varying test charge directly into the front end electronics. This method does not provide in-pixel positional sensitivity which is usually determined by a complementary measurement of particle detection efficiency in a test beam (such as [9]). In this work we investigated a new approach to evaluate spatial dependence of in-time efficiency using Edge-TCT method, which employs a focused laser beam to inject charge into different parts of the pixel. This method can be carried out in a laboratory



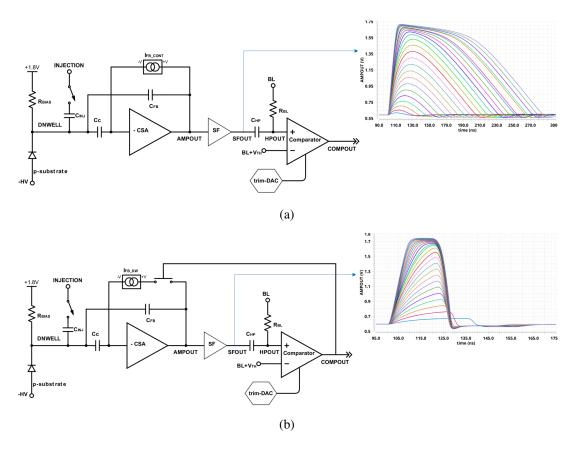
**Figure 1**: Schematics of the RD50-MPW2 sample: (a) chip with marked  $8 \times 8$  active pixel matrix; (b) pixel cross section showing nested p- and n-wells containing readout electronics.

environment and can potentially simplify sample characterisation. This study was introduced in the scope of characterising the properties of the analogue front end in an active silicon pixel detector prototype which is also described in this paper.

### 2 Samples and measurement setup

The active silicon pixel detector prototype investigated in this work has been developed within the CERN RD50 collaboration which aims to evaluate different aspects of radiation tolerance of industrial CMOS processes [10]. The investigated sample called RD50-MPW2 has been manufactured in a 150 nm CMOS process by LFoundry on a 280  $\mu$ m thick p-type substrate with an initial resistivity of 1900  $\Omega$  cm. The bias voltage for sensor depletion is applied to dedicated p-type rings surrounding each pixel on the top side of the chip and reaches the breakdown value at 120 V. The back side of the substrate is not processed. The electric field configuration resulting from the described biasing scheme may lead to a reduced charge collection efficiency after irradiation [7]. However, the investigated response delay at a given collected charge is not affected. Detectors for practical applications will have metallised back plane to avoid this feature.

The chip houses several test structures including an  $8 \times 8$  active pixel matrix with a pixel size of  $60 \,\mu\text{m} \times 60 \,\mu\text{m}$ . Each pixel contains a charge sensitive amplifier and a discriminator circuit integrated within several nested p- and n-wells embedded in an n-type collection electrode (Figure 1). The schematics of the in-pixel circuit is shown in Figure 2. The pixels come in two variants with different reset mechanisms for discharging the feedback capacitance – the first four matrix columns, called continuous reset, use a constant current source, while the other four columns use a transistor switch which resets the inputs much faster (called switched reset). In continuous reset pixels the duration of the comparator output signal (*time over threshold* – ToT) scales with the signal size and can be used to measure the amount of input charge. For this reason the continuous reset type was selected for this study. Both pixel types also contain a so called calibration circuit with a node for injecting test charge directly into the amplifier input via a MOS capacitor with



**Figure 2**: Schematics of the in-pixel amplifier and comparator circuit in (a) continuous reset pixel and (b) switched reset pixel. Simulated analogue pulses after the source follower (SF) for input charge between  $1 \text{ ke}^-$  and  $25 \text{ ke}^-$  illustrate the difference between the pixel flavours.

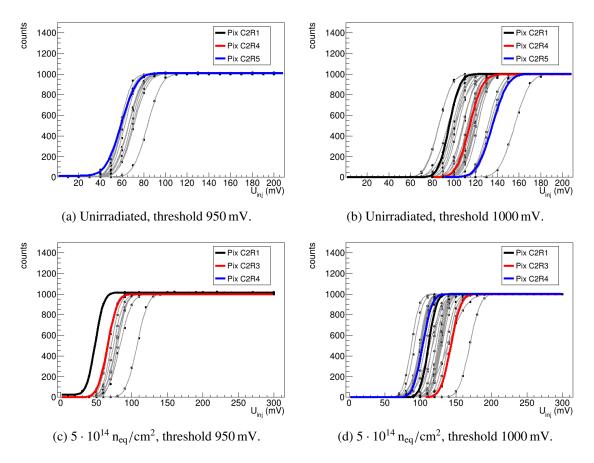
a capacitance of  $C_{inj} = 2.8$  fF. The pixel discriminator output is routed out of the chip via an analogue multiplexer allowing reading out one pixel output at a time.

The chip is configured with several global DACs as well as an independent four bit threshold tuning DAC in each pixel. The configuration and DAQ system for the chip is based on Caribou DAQ platform [11] controlled by an FPGA evaluation kit (Xilinx ZC706). Discriminator output signals can be recorded either with the Caribou setup or with an external oscilloscope via an intermediate buffer circuit.

This study was made with two samples: one unirradiated and one irradiated with neutrons at JSI TRIGA reactor in Ljubljana to an equivalent fluence of  $5 \cdot 10^{14} n_{eq}/cm^2$  and a reactor background total ionising dose (TID) of 5 kGy [12, 13].

#### **3** Front end threshold, noise and calibration

Threshold and noise properties of the pixel front end circuit were characterised by analysis of activation curves (S-curves) of the continuous reset pixels using the calibration circuit. The amplifier input was connected via the built in injection capacitance  $C_{inj} = 2.8$  fF to an external pulse generator providing a voltage step function with variable amplitude U. The amount of injected charge



**Figure 3**: S-curve measurements on samples before and after irradiation. Data for noisy pixels with more than 1100 counted pulses is not shown. Threshold is set with respect to comparator baseline of 900 mV.  $U_{inj} = 100 \text{ mV}$  corresponds to a charge of  $1750 \text{ e}^-$ . Highlighted S-curves indicate pixels which were used in subsequent measurements.

*q* was calculated from the formula  $q = C_{inj}U$ , which evaluates to  $17.5 \text{ e}^-/\text{mV}$ . The comparator baseline was set to 900 mV and the comparator threshold to two different values of 950 mV and 1000 mV, which are around expected threshold levels from design simulation. A sweep over a range of injection pulse amplitudes was made with 1000 pulses injected at each amplitude and the number of comparator output pulses was counted with the Caribou and FPGA readout chain. The in-pixel threshold tuning DAC (trim-DAC) was not used in this test and was set to zero. All measurements were made at room temperature with the leakage current in the pixel matrix of 20 nA and 1µA before and after irradiation respectively at -100 V reverse bias voltage. The resulting S-curves for all 32 continuous reset pixels are shown in Figure 3. In several pixels the low threshold setting of 950 mV was within the noise range, hence a large number of noise hits was detected – these pixels are excluded from the figure. Measurements were fitted with an error function and the fit parameters sigma (the measure of noise) and the 50 % point (VT50) were extracted from the fit. The VT50 and noise distributions are shown in Figure 4. The thresholds of 950 mV and 1000 mV correspond to  $1200 \text{ e}^- \pm 100 \text{ e}^-$  and  $2000 \text{ e}^- \pm 200 \text{ e}^-$  respectively, with the pixel-to-pixel

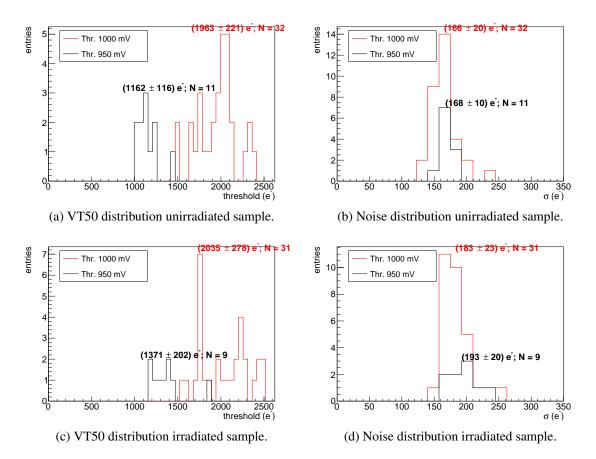


Figure 4: Threshold (VT50) and noise distribution before and after irradiation at 0 V bias voltage.

variance due to manufacturing variations in the front end electronics. These variations have many contributions from different elements of the front end circuit, with the most significant coming from the variance of the feedback capacitance in the charge sensitive amplifier, which has a large influence on the circuit gain. The impact on signal shape is not significant. The mean noise level is below 200 e<sup>-</sup> and does not vary with respect to threshold setting. The mean VT50 and noise values increase slightly after irradiation, although statistics is limited. Based on measurements with and without applied biased voltage, around 25 % of this change is caused by shot noise due to increased leakage current. The remaining contribution is probably due to degradation of front end electronics with irradiation. For subsequent studies three pixels featuring a low, medium and high VT50 were selected. Their corresponding S-curves are highlighted in Figure 3. The pixels are situated in the third matrix column (column 2) and are surrounded by at least one pixel on each side to avoid any edge effects.

The calibration of the comparator pulse duration (ToT) with respect to the amount of injected charge was performed for the selected three pixels. The results are shown in Figure 5. The variation between pixels is significant due to channel to channel variance in gain. At lower threshold signals stay above the threshold level longer, resulting in a 5-10% increase in ToT.

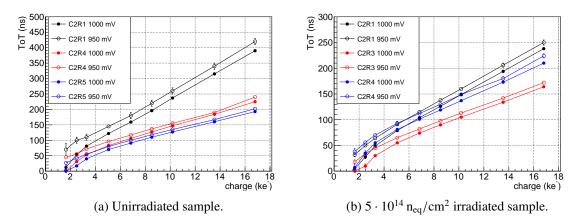


Figure 5: Time over threshold calibration in unirradiated and irradiated sample.

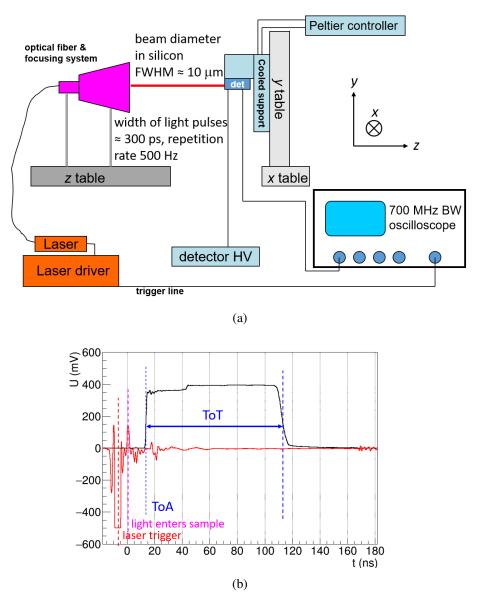
### 4 Edge-TCT measurement setup

Spatially sensitive timing measurements were carried out with the *edge transient current technique* (Edge-TCT) which employs a pulsed laser to generate free charge carriers within the sensor. The schematics of the setup, produced by Particulars[14], is shown in Figure 6a. Laser beam with a pulse duration of < 1 ns, a wavelength of 1064 nm and corresponding absorption depth of 1 mm in silicon is tightly focused to a full width at half maximum of FWHM < 10  $\mu$ m in the beam waist. The sample is mounted on motorized precision placement stages and can be probed with a sub pixel resolution. The sample is oriented in edge configuration with the laser beam entering the silicon bulk from the side, which allows probing the pixel laterally as well as along its depth. The edge of the samples was not polished for this measurement.

The signal of free charge carriers drifting within the depletion zone is propagated through the front end and the comparator output is digitised with an oscilloscope. To reduce noise 100 waveforms are averaged at each step and the resulting average waveform is recorded. A typical comparator output pulse from a continuous reset pixel is shown in Figure 6b. The nominal output voltage level is in the range of 0 V - 1.8 V, however when using the  $50 \Omega$  oscilloscope channel termination the pulse is clipped at 400 mV due to the limited power of the current drivers in the intermediate buffer. This does not affect the underlying signal shape. The acquisition is triggered by the trigger output signal from the laser. The relative delay between the trigger signal and the light entering the sample, including delays due to cable length, is  $7.5 \pm 0.5$  ns, which was determined using a passive silicon diode that produces prompt signals. The leading edge of the waveform, called *time of arrival* (ToA), is measured at an arbitrarily selected voltage level of 120 mV and is used to determine the time walk. The time over threshold (ToT) is used for measuring the signal size.

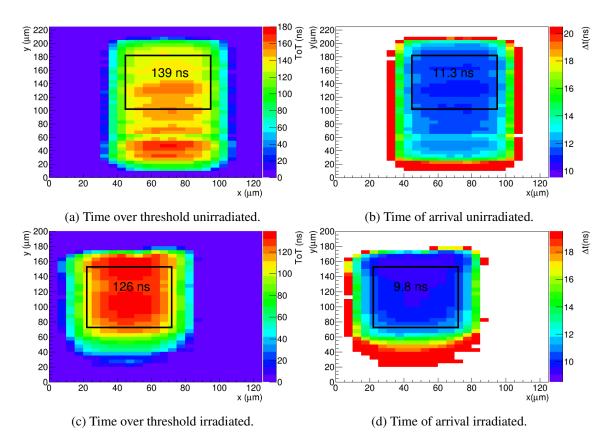
## 5 Time walk measurements with Edge-TCT

Edge-TCT measurements were taken with the sample biased to a voltage of 100 V with corresponding depletion depth exceeding 100  $\mu$ m. Laser pulse energy was varied in up to five steps to inject



**Figure 6**: Edge-TCT measurement setup: (a) Setup schematics; (b) Typical pulse (black waveform) with indicated time of arrival (ToA) and time over threshold (ToT). Red waveform is the laser trigger pulse.

different amount of charge, ranging from approximately  $2 \text{ ke}^-$  to  $10 \text{ ke}^-$  based on ToT calibration from Figure 5. Space maps of pixel response were obtained by moving the sample in steps of 5 µm in x- and y-directions where the x-direction is parallel to the chip surface and y-direction is along the sample depth. At each step the collected charge (ToT) and the signal delay (ToA) were measured. An example of ToT and ToA maps is shown in Figure 7 which shows a pixel in unirradiated and irradiated sample seen from the side. With unirradiated sample the sensor surface is located at  $y = 200 \,\mu\text{m}$  and with irradiated sample at  $y = 170 \,\mu\text{m}$ . The collected charge distribution in the unirradiated sample shows some modulations along the y-direction, which probably come from



**Figure 7**: Example of Edge-TCT measurements with unirradiated sample (top, pixel C2R1, signal  $\approx 6 \text{ ke}^-$ ) and irradiated sample (bottom, pixel C2R4, signal  $\approx 10 \text{ ke}^-$ ): (a, c) Map of collected charge measured in ToT; (b, d) Time of arrival map. Chip surface is at y = 200 µm (170 µm) and depletion zone grows in negative y-direction towards the back side of the sample. The framed area indicates the volume for extracting the average ToT and ToA.

varying light absorption on chip edge damaged by wafer dicing (the edges were not polished). The time of arrival is uniform on a 1 ns level in the entire pixel, except on pixel edges. The reconstructed width of the pixel is around 60  $\mu$ m which is in agreement with the nominal pixel pitch. The width of the transition region between inefficient and fully efficient volume on pixel edges is dominated by the laser beam spot size of FWHM  $\approx 10 \,\mu$ m. This resolution does not allow a precise study of charge sharing on pixel edges. The depth of the depletion zone after irradiation is reduced due to the increased space charge concentration caused by displacement damage.

For evaluation of the time walk ToT and ToA were averaged over a centred volume 50  $\mu$ m wide and 80  $\mu$ m deep starting 20  $\mu$ m below the sensor surface, as indicated in Figure 7. These boundaries were selected to contain the most efficient volume of the pixel. This measurement was repeated for each of the three investigated pixels for different laser pulse energies and comparator thresholds. The signal size was converted into electrons using the calibration in Figure 5. The obtained time walk curves are shown in Figure 8.

The measured delay ranges from the minimal value of 8 ns at a signal size above ~  $10\,000\,e^-$  (ToT 150 ns) up to  $\approx 20\,\text{ns}$  at signal size of ~  $2\,000\,e^-$  (ToT 20 ns). The time walk curves for

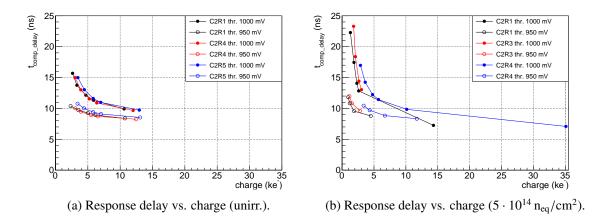
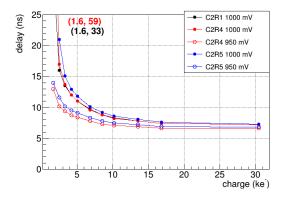


Figure 8: Time walk curves measured with Edge-TCT in unirradiated and irradiated sample.



**Figure 9**: Time walk curve measured with external charge injection (unirradiated sample). Pixel C2R1 could not be operated at low threshold due to noise.

different pixels at a fixed threshold coincide relatively well, which indicates that a universal time walk dependence could be applicable for all pixels. The delay at a given signal size increases by a few ns with increasing comparator threshold, which is expected, since the level crossing at a higher threshold occurs later. The agreement between the curves of unirradiated and irradiated sample is also reasonable.

The measurement with the unirradiated sample was additionally validated by measuring the time walk with external charge injection directly into the front end through the injection circuit using a pulse generator. This method bypasses the charge carrier drift in the silicon bulk. The additional latency introduced this way is negligible, since injection circuit is purely passive. The time walk curve shown in Figure 9 is in a good agreement with Edge-TCT measurements. At charge above  $10\,000\,e^-$  (ToT >  $100\,ns$ ) the delay measured with Edge-TCT is about 1 ns longer than with external injection. This difference comes from the charge carrier drift in silicon bulk, which takes place on this time scale.

In practical applications the relevant aspect determining in-time efficiency is the response delay relative to the asymptotic value for the fastest possible response occurring at large collected charge.

Our measurements show that in the irradiated detector the relative output delay is less than ~ 10 ns at a deposited charge of 2000 e<sup>-</sup>, even at a high comparator threshold of 1000 mV. At the threshold of 950 mV, which the detector is aiming to operate at, the delay is even smaller. With the unirradiated sample the measurements with external charge injection similarly indicate a full in time efficiency for a charge above 2000 e<sup>-</sup> at the threshold of 1000 mV, while at the threshold of 950 mV this is true even for a charge of 1600 e<sup>-</sup>. Given that even after irradiation to  $5 \cdot 10^{14} \text{ n}_{eq}/\text{cm}^2$  a depletion depth exceeding 100 µm can be achieved – corresponding to a most probable charge deposition of > 8 000 e<sup>-</sup> – the in-time efficiency in pixel centre is guaranteed. On pixel edges and corners, where charge can be shared by up to four pixels, this is more critical and fine tuning of pixel front end is necessary.

# 6 Conclusions

In the scope of this work tests were carried out with an active CMOS pixel detector RD50-MPW2 before irradiation and after neutron irradiation of  $5 \cdot 10^{14} n_{eq}/cm^2$  and TID of 5 kGy. The tests have demonstrated the basic functionality of the active pixel array. External charge injection into the analogue front end has shown all pixels can be operated above noise at a threshold level of  $2000 e^- \pm 200 e^-$ , and a noise level below  $200 e^- \pm 20 e^-$ . A new method to evaluate time walk with Edge-TCT was investigated, providing a spatial sensitivity in different parts of the pixel. A uniform output delay was observed in the centre of the pixel. In a 5–10 µm wide band on pixel edges the charge was spread between neighbouring pixels due to a finite beam width of the laser, resulting in reduced signal size and correspondingly longer delay. Delays significantly below 25 ns was observed for collected charge above 2000 e<sup>-</sup>. No significant variations with irradiation were observed. Validation with charge injection through the calibration circuit has generated nearly identical time walk curves, showing that the methods are compatible.

# Acknowledgments

This work has been partly performed in the framework of the CERN RD50 collaboration. The authors would like to thank the crew at the TRIGA reactor in Ljubljana for help with irradiations of detectors. The authors acknowledge the financial support from the Slovenian Research Agency (research core funding No. P1-0135 and project ID PR-06802).

#### References

- [1] M. Kiehn et al., *Performance of the ATLASPix1 pixel sensor prototype in ams aH18 CMOS technology for the ATLAS ITk upgrade*, 2019 JINST 14 C08013.
- [2] T. Wang et al., Depleted fully monolithic CMOS pixel detectors using a column based readout architecture for the ATLAS Inner Tracker upgrade, 2018 JINST 13 C03039.
- [3] M. Dyndal et al., *Mini-MALTA: radiation hard pixel designs for small-electrode monolithic CMOS sensors for the High Luminosity LHC*, 2020 JINST 15 P02005.
- [4] A. Affolder et al., *Charge collection studies in irradiated HV-CMOS particle detectors*, 2016 JINST 11 P04007.
- [5] B. Hiti et al., Charge collection properties in an irradiated pixel sensor built in a thick-film HV-SOI process, 2017 JINST 12 P10020.
- [6] E. Cavallaro et al., *Studies of irradiated AMS H35 CMOS detectors for the ATLAS tracker upgrade*, 2017 JINST 12 C01074.
- [7] I. Mandić et al., Charge-collection properties of irradiated depleted CMOS pixel test structures, 2018 NIM A 903 P126–133.
- [8] B. Hiti et al., Charge collection in irradiated HV-CMOS detectors, 2019 NIM A 924 P214–218.
- [9] M. Barbero et al., *Radiation hard DMAPS pixel sensors in 150 nm CMOS technology for operation at LHC*, 2020 JINST 15 P05013.
- [10] R. Hernández et al., Latest Depleted CMOS Sensor Developments in the CERN RD50 Collaboration, Proceedings of VERTEX2020, 2021 JPS Conf. Proc., 010008.
- T. Vanat. Caribou A versatile data acquisition system. Proceedings of TWEPP 2019, 2020 PoS 370 P100.
- [12] L. Snoj, G. Žerovnik and A. Trkov, Computational analysis of irradiation facilities at the JSI TRIGA reactor, 2012 Appl. Radiat. Isot. 70 P483.
- [13] K. Ambrožič, G. Žerovnik, L. Snoj. *Computational analysis of the dose rates at JSI TRIGA reactor irradiation facilities*. 2017 Appl. Radiat. Isot. 130 P140–152.
- [14] Particulars webpage, http://www.particulars.si/