Study of neutron irradiation effects in Depleted CMOS detector structures *

I. Mandić^{*a*,1} V. Cindro^{*a*} J. Debevc^{*a*} A. Gorišek^{*a*} B. Hiti^{*a*} G. Kramberger^{*a*} P. Skomina^{*a*} M. Zavrtanik^{*a*} M. Mikuž^{*a*,*b*} E. Vilella^{*c*} C. Zhang^{*c*} S. Powell^{*c*} M. Franks^{*c**} R. Marco-Hernandez^{*d*} H. Steininger^{*e*}

^q Jožef Stefan Institute, Jamova 39, Ljubljana, Slovenia

^b University of Ljubljana, Faculty of Mathematics and Physics, Jadranska 19, Ljubljana, Slovenia

^c University of Liverpool, Department of Physics, Liverpool, UK

*now FBK, Trento, Italy

^dIFIC (CSIC-UV), Valencia, Spain ^eHEPHY, Vienna, Austria

IILI III, vienna, Masinia

E-mail: igor.mandic@ijs.si

ABSTRACT: In this paper the results of Edge-TCT and I-V measurements with passive test structures made in LFoundry 150 nm HV-CMOS process on p-type substrates with different initial resistivities ranging from 0.5 to 3 k Ω cm are presented. Samples were irradiated with reactor neutrons up to a fluence of 2·10¹⁵ n_{eq}/cm². The depletion depth was measured with Edge-TCT. The effective space charge concentration N_{eff} was estimated from the dependence of the depletion depth on bias voltage and studied as a function of neutron fluence. The dependence of N_{eff} on fluence changes with initial acceptor concentration in agreement with other measurements with p-type silicon. A long term accelerated annealing study of N_{eff} and detector current up to 1280 minutes at 60°C was made. It was found that N_{eff} and current in reverse biased detector behave as expected for irradiated silicon.

KEYWORDS: Particle tracking detectors (Solid-state detectors), Radiation-hard detectors, DMAPS

^{*}The work was partly done in the framework of the RD50 collaboration.

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1 Introduction

Monolithic charged particle detectors in depleted CMOS technology offer several advantages over hybrid detectors, such as higher granularity, lower detector mass, simplified assembly, production in industrial process on large wafers in high volume foundries, etc. Usage of high voltage CMOS technology enables charge collection from the depletion volume and therefore higher speed and radiation hardness necessary for operation in a hadron collider environment. Development of depleted CMOS detectors for hadron colliders has been very intense in recent years and is still keeping its momentum [1–4]. RD50 collaboration [5] has joined the efforts and produced two detector prototypes in 150 nm LFoundry HV-CMOS process [6] containing several test structures for various radiation hardness studies. In this work, measurements with passive pixel detector structures on RD50-MPW1 and RD50-MPW2 chips are described.

2 Samples

As the name suggests, RD50-MPW1 was the first chip designed by the RD50 collaboration and details about its functionalities and performance can be found in [7]. Due to imperfections in the design of the RD50-MPW1 chip, pixel current was higher than expected and already started to rise rapidly above a reverse bias voltage of ~ 30 V. This initiated the submission of RD50-MPW2 [8] with the shortcomings corrected so taht the pixels could be biased with over 110 V.

The designs of the pixels and pixel arrays are very similar in RD50-MPW1 and RD50-MPW2. In RD50-MPW1 the pixels are 50 μ m × 50 μ m and the spacing between PW and NW implants (see Figure 1a) is 3 μ m while in RD50-MPW2 the dimensions are 60 μ m × 60 μ m with an inter-electrode



Figure 1. Figure a) shows a simplified scheme of a HV-CMOS pixel. The definition of coordinate system can be seen and the direction of the laser beam scan in E-TCT is shown. Figure b) represents the 3x3 pixel array in which DNWELLs of the outer 8 pixels are connected to one bond-pad and DNWELL of the central pixel is contacted to a separate bond pad. The substrate is contacted via the PW implants, all connected to the same bond pad.





spacing of 8 μ m. Larger spacing is one of the main reasons for better breakdown performance of structures on MPW2.

Wafer	Chip version	Initial resistivity		
		[kΩcm]		
W8	RD50-MPW2	0.5		
W9	RD50-MPW1	0.7		
W10	RD50-MPW1	1.3		
W14	RD50-MPW2	2.2		

Table 1. List of samples and initial resistivities of the substrates

Chips were produced on p-type substrates with different initial resistivities. In this work measurements with chips from RD50-MPW1 and RD50-MPW2 are described and the samples are listed in table 1. Figure 1a) shows a simplified cross section of a HV-CMOS pixel. DNWELL is the charge collecting electrode covering a large part of the pixel cross section. Shallow wells above DNWELL, named PWELLs and NWELLs, contain analogue readout electronics in active pixels. These include a high impedance circuit to bias the collecting electrode, a charge sensitive amplifier and a CMOS comparator with a 4-bit DAC to locally tune small threshold voltage variations due to offset (for more detail please see [7]). In a passive test structure, shallow wells are left without any elements. In this work only passive pixels were used with an external amplifier connected to DNWELL. Measurements were made with 3x3 passive pixel arrays. In these arrays, DNWELLs of the outer 8 pixels are connected to one bond-pad and DNWELL of the central pixel is contacted to a separate bond pad as sketched in Figure 1b). The substrate is contacted via the PW implants.

Figure 2a) shows the layout and dimensions of the RD50-MPW1 and Figure 2b) of RD50-MPW2 chips containing various test structures. Arrows in Fig. 2 point to the 3x3 arrays used in this work. The structures are placed near the edge of the chip to enable Edge-TCT measurements.

3 Irradiation

Samples were irradiated with neutrons in the TRIGA reactor in Ljubljana [9, 10] to 1 MeV neutron equivalent fluences ranging from $1 \cdot 10^{13} n_{eq}/cm^2$ to $2 \cdot 10^{15} n_{eq}/cm^2$. The maximum power of the TRIGA reactor in Ljubljana is 250 kW and at this power the 1 MeV neutron equivalent flux in the irradiation tube used for this work is $1.5 \cdot 10^{12} n_{eq}/cm^2/s$. Irradiation to $1 \cdot 10^{14} n_{eq}/cm^2$ therefore takes slightly over one minute. Reactor power, which is proportional to neutron flux, is reduced for irradiation to lower fluences because it is easier to handle irradiation times longer than one minute. The neutron flux in the irradiation channel was determined with a precision of about 10% by measurements of leakage-current increase in dedicated silicon diodes [11].

4 Measurements

The depletion depth was estimated with Edge TCT (E-TCT) [12] using Particulars measurement system [13]. In E-TCT a pulsed narrow laser beam is directed to the side of the chip. The chip is moved in a direction perpendicular to the laser beam in 5 μ m steps as sketched in Figure 1a). Laser light with a wavelength of $\lambda = 1064$ nm and absorption length of about 1 mm in silicon is used to release electron-hole pairs along the laser beam line inside the investigated test structure. If the

light crosses the depleted region of a pixel, a current pulse is induced on the pixel electrodes which is observed by the E-TCT measurement system. E-TCT measurements were made with 3 x 3 pixel arrays shown in Fig. 1. The central pixel was connected to the wide-bandwidth amplifier of the E-TCT system and to the high voltage using a bias-T circuit. This circuit enables DC connection of the high voltage source to the pixel electrode and AC/RF connection to the amplifier via a capacitor. To come closer to the conditions of a larger pixel array, the surrounding 8 electrodes were connected to the same high voltage potential but not to the E-TCT system amplifier. Induced currents on the central pixel were recorded by the oscilloscope and saved to the computer. The time integral of the induced current in the 10 ns time window was a measure of collected charge. In this work the focus is on the charge collected from the depletion region which is necessary for application in hadron collider environments. The chosen integration time is sufficient for charge collection from the depletion region and longer integration time would increase the noise on measured charge values because of oscillations, reflections and baseline fluctuations in the tail of the recorded pulses. With the E-TCT method, collected charge can be measured as a function of the detector depth (distance from the chip surface) providing charge collection profiles. The depleted depth is estimated from the width of the charge collection profiles measured in the scan along the edge of the chip as indicated in Fig. 1a). Similar types of measurements are described in several publications [14–19] and more details can be found therein.

Figure 3 shows measurements of depletion depth vs. bias voltages for chips with different initial resistivities listed in table 1. The graphs show measurements before irradiation and after irradiation with neutrons to equivalent fluences indicated in the figures. Before measurements samples were annealed for 80 minutes at 60 °C. In all samples except for the highest initial resistivity (W14 in Fig 3b), an increase of the depletion depth compared to that before irradiation can be observed. For the lower initial resistivity samples (W8 and W9) the depletion depth is larger than before irradiation up to the fluence of about $2 \cdot 10^{14} \text{ n}_{eq}/\text{cm}^2$, while for W10 increased depletion is measured up to $1 \cdot 10^{14} \text{ n}_{eq}/\text{cm}^2$. This increase is the consequence of the initial acceptor removal [11, 14, 20] resulting in a lower effective space charge concentration than before irradiation.

The lines fitted to the measured depletion depth in Fig. 3 are a result of a fit of the function 4.1:

$$w(V_{\text{bias}}) = w_0 + \sqrt{\frac{2\epsilon_r \epsilon_0}{e_0 N_{\text{eff}}}} V_{\text{bias}}$$
(4.1)

where w is the depletion depth, N_{eff} is the effective space charge concentration, V_{bias} the bias voltage, e_0 the elementary charge, ϵ_0 the dielectric constant and ϵ_r the relative permittivity of silicon. Parameter w_0 is introduced to account for effects of finite laser beam diameter, intrinsic depletion etc. contributing to depletion measured at 0 V bias voltage. Parameters w_0 and N_{eff} are free and their values are extracted from the fit. Values of parameter w_0 vary between 5 and 25 μ m. Every fluence point was measured with different chip and the value of w_0 depends on the details of sample mounting and laser light focus etc. It can be seen in Fig 3 that the function 4.1 can be fitted to measurements relatively well with some discrepancies seen at low voltages for W14 (3b)) for lowest fluences. This effect is not fully understood but it indicates that describing all of the effects contributing to the measured depth at low voltages by a single constant w_0 is not sufficient. But function 4.1 fits the data over a wide interval of bias voltages so it can be used to estimate N_{eff} .

Dependence of N_{eff} on neutron fluence can be described with [14]:



Figure 3. Depletion depth measured as a function of bias voltage for samples from RD50-MPW1 and RD50-MPW2 chips with different initial resistivities - see table 1: a) W8 (RD50-MPW2, b) W14 (RD50-MPW2), c) W9 (RD50-MPW1) and d) W10 (RD50-MPW1). Measurements were made before irradiation and after irradiation to 1 MeV neutron equivalent fluences written in the graphs

$$N_{\rm eff} = N_{\rm eff,0} - N_{\rm c} \cdot (1 - e^{-c\Phi_{\rm eq}}) + g_c \cdot \Phi_{\rm eq}$$

$$\tag{4.2}$$

where $N_{\text{eff},0}$ is the initial acceptor concentration of the substrate, N_c the concentration of the removed acceptors, *c* the removal constant and g_c the introduction rate of stable deep acceptors for irradiation with neutrons.

Figure 4a) shows the evolution of effective space charge concentration on fluence with the theoretical curve described in equation 4.2 fitted to measured points. A decrease of N_{eff} after the first fluence steps can clearly be seen for the three lower initial resistivities followed by the increase at the same rate for all samples after higher fluences. Similar behaviour was measured in several other experiments [15, 17, 19]. Table 2 summarizes the parameters obtained from the fit of function 4.2. There are large uncertainties but the values are not in contradiction with the literature [15, 19, 21, 22] stating that removal constant *c* is higher for higher initial resistivities. Stable damage introduction rate g_c is somewhat larger than typical for neutron irradiated silicon but this is consistent with similar types of measurements [15, 17, 19]. In table 2 only statistical errors



Figure 4. Figure a) measured N_{eff} (points) and result of the fit (lines) of equation 4.2 as a function of fluence. Figure b) shows depletion depth measured at 100 V as a function of fluence for the four samples.

calculated in the fitting procedure are listed. Systematic uncertainties of the parameters were not evaluated although they might be significant. The aim of this work was to check if the behaviour of the substrate after irradiation is roughly within expectations. For more accurate measurements of parameters in equation 4.2 a dedicated experiment would be needed.

For the sample with highest initial resistivity, W14, the parameters N_c and c could not be estimated in the range of fluences investigated in this work. As mentioned above, higher initial resistivity is associated with higher value of c which means that acceptor removal process is finished at lower fluences. To observe acceptor removal and estimate the parameters N_c and c measurements would have to be made at fluences below $1 \cdot 10^{13} \text{ n}_{eq}/\text{cm}^2$ with W14. Therefore, only the values of parameters $N_{eff,0}$ and g_c could be estimated from the fit of equation 4.2.

The number of free carriers released by the passage of a charged particle is proportional to the depletion depth so it is one of the crucial parameters determining the detector performance. Fig. 4b) shows the depletion depth measured at $V_{\text{bias}} = 100 \text{ V}$. RD50-MPW1 chips (W9 and W10) could not be biased with 100 V so the depletion depths were estimated from the extrapolation of the fitted function at 100 V (see Fig. 3). A bias of 100 V was chosen for this figure because it is a realistic value at which detectors made in this technology might be operated in an application. One can see that there are significant differences before irradiation and at low fluences, while above $\approx 2 \cdot 10^{14} \text{ n}_{eq}/\text{cm}^2$ a similar depletion depth is measured in all samples. The sample W10 exhibits a somewhat higher depletion depth at fluences between $2 \cdot 10^{14} \text{ n}_{eq}/\text{cm}^2$ and $1 \cdot 10^{15} \text{ n}_{eq}/\text{cm}^2$, however these values were obtained from extrapolation to 100 V and have therefore significant uncertainties.

5 Annealing effects

The measurements shown above were made with samples annealed for 80 minutes at 60°C. The measurements were made before and after annealing and it was observed that the depletion depth increased and N_{eff} decreased confirming the beneficial effect of short term annealing. With samples from W8 and W14 irradiated to $\Phi_{\text{eq}} = 2 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ a long term annealing study was made in which measurements were taken after annealing for 80, 160, 320, 640 and 1280 minutes at 60°C.

Wafer	Chip version	$N_{\rm eff,0}[10^{14} cm^{-3}]$	$N_c/N_{\rm eff,0}$	$c[10^{-14}cm^2]$	$g_c[10^{-2}cm^{-1}]$
W8	RD50-MPW2	0.25 ± 0.04	0.39 ± 0.14	3.5 ± 3.2	3.3 ± 0.6
W9	RD50-MPW1	0.23 ± 0.03	0.72 ± 0.10	2.5 ± 0.9	3.9 ± 0.6
W10	RD50-MPW1	0.13 ± 0.02	0.43 ± 0.10	8.1 ± 5.4	1.8 ± 0.3
W14	RD50-MPW2	0.07 ± 0.01	/	/	2.9 ± 0.4

Table 2. Parameters of fit of fluence dependence of effective space charge concentration N_{eff} described in equation 4.2.



Figure 5. Effective space charge concentration N_{eff} measured with W8 and W14 irradiated to $\Phi_{\text{eq}} = 2 \cdot 10^{15}$ $n_{\text{eq}}/\text{cm}^2$ as a function of annealing time at 60°C. Dotted lines show annealing function with parameters measured by RD48 collaboration.

The dependence of N_{eff} on annealing time is shown in Figure 5. A significant effect of the first (80 minutes) annealing step can be seen, while the measured points at longer annealing times are scattered and do not exhibit a significant annealing effect. For comparison, curves of RD48 annealing model [11] for neutron irradiated silicon are added in the plot. It may be noted that the increase of effective space charge concentration at long annealing times (reverse annealing) is somewhat smaller than expected from the model. For the curves drawn in Figure 5, parameters describing float zone silicon are used. It was measured in [23] that neutron irradiated diodes fabricated on magnetic Czocharlski substrate show less reverse annealing compared to diodes from float zone silicon. RD50-MPW1(and 2) chips are made on Czochralski substrate and this may be the reason for the discrepancy seen in Figure 5.



Figure 6. I-V measured after 80 minutes annealing for samples W8 in (a) and W14 in (b). Points show measurements and lines show current values calculated from depletion volume measured with E-TCT and with constant $\alpha(80 \text{ min}) = 4 \cdot 10^{-17} \text{ A/cm}$.

6 Leakage current

Reverse current in the central pixel of the test structure was measured as a function of bias voltage. The bond pads were contacted on in a probe station and the current measured with a Keithley 6517A. The current of the central pixel was measured (see Figure 1) while the outer pixels were kept at the same potential as the central one forming an effective guard ring. Samples were temperature stabilized at $20^{\circ}C \pm 0.5^{\circ}C$. Figure 6 shows I-V curves for W8 and W14 irradiated to different fluences after annealing for 80 minutes at $60^{\circ}C$.

The standard parametrization of the thermally generated current in the depleted volume in irradiated silicon is [24]: $I = \alpha(t) \cdot V \cdot \Phi_{eq}$ where $\alpha(80 \text{ min}) = 4 \cdot 10^{-17}$ A/cm is the value of the constant after annealing for 80 minutes at 60°C, V is depleted volume and Φ_{eq} equivalent fluence. The depleted volume V can be estimated from E-TCT measurement of the depletion depth d vs. bias voltage shown in Figure 3 as $V = d \cdot S$ where S is the pixel surface $60 \times 60 \ \mu\text{m}^2$. The values of the calculated current can be seen in Figure 6 showing that such simple estimation can describe the measured values to within a factor of 2 over almost two orders of magnitude.

The effect of long term annealing at 60°C on the leakage current was studied with samples W8 and W14 irradiated to $\Phi_{eq} = 2 \cdot 10^{15} \text{ n/cm}^2$. In Figure 7 the value of parameter $\alpha = I/(V \cdot \Phi_{eq})$, where *I* is the current measured at 20°C at a bias of 60 V and *V* is the depleted volume estimated from the E-TCT measurement, is shown as a function of annealing time at 60°C. The measured α is compared with the RD48 current annealing model from [24]. The decrease of current with increasing annealing time can clearly be seen but the deviations from the model are significant and they originate mainly from a large uncertainty on the estimation of the depleted volume.

7 Conclusions

In this paper measurements with irradiated passive pixels on RD50-MPW1 and RD50-MPW2 chips manufactured in LFoundry 150 nm HV-CMOS process are presented. Measurements were made



Figure 7. Annealing of current constant α measured with W8 and W14 irradiated to $2 \cdot 10^{15} \text{ n/cm}^2$. The measured value of α is extracted from the curent measured at a bias voltage of 60 V and from the depletion volume measured with E-TCT. Annealing curve of the RD48 model ([24]) is also shown for comparison.

with chips made on wafers with four different resistivities irradiated with reactor neutrons to fluences ranging from $1 \cdot 10^{13} n_{eq}/cm^2$ to $2 \cdot 10^{15} n_{eq}/cm^2$. The depletion depth, measured with E-TCT, and leakage current were measured at different bias voltages and after different times of annealing at 60°C.

The effective space charge concentration N_{eff} was estimated from the dependence of the depletion depth on bias voltage. The observed change of N_{eff} with neutron fluence was in agreement with previous measurements - an effect of initial acceptor removal was observed on all but the highest initial resistivities. Measurements indicate that the material with higher initial resistivity should be chosen to achieve a larger depletion depth in the whole fluence range.

It was shown that the acceptor removal constant is larger in materials with higher initial resistivities and that stable damage introduction rate is approximately as expected for neutron irradiated silicon. Annealing studies show an expected beneficial effect (i.e. drop of N_{eff} and consequent increase of depletion depth) of annealing for 80 minutes at 60°C. With two samples irradiated to the highest fluence, measurements were made up to a cumulative annealing time of 1280 minutes. No significant long term annealing effect was observed which could be the consequence of the detector material being Cz grown silicon instead of Float Zone. Significant differences between measured and calculated values of the leakage current as a function of bias voltage, fluence and annealing time were seen but the source of differences are uncertainties of the size of depletion volume.

With usual model describing irradiated silicon detectors only very rough predictions of the depletion depth and reverse current as a function of fluence, bias voltage and annealing time can be made for investigated devices.

8 Acknowledgments

The authors would like to thank the crew at the TRIGA reactor in Ljubljana for help with the irradiation of the detectors. Part of this work was performed in the framework of the CERN-RD50 collaboration. The authors acknowledge the financial support from the Slovenian Research Agency (research core funding No. P1-0135 and project ID PR-06802).

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