Wide-gain Boost Converter Based on LCD Cell

Yinghao Song[1] · Yu Tang[1*] · Jiarong Kan[2] · Lin Jiang[3]

Abstract

A wide-gain boost converter based on *LCD* cell is proposed in this study. The proposed topology is suitable for the fuel cells of electric vehicles that generate a specific bus voltage in power generation systems. It has none of the drawbacks of other reported *LCD* cell-based topologies, such as highly pulsating source current, lack of common ground, inverted load voltage polarity, and numerous switching devices. By integrating the classic boost converter with the *LCD* cell, the voltage gain is improved, and the features of single switch, low voltage and current stress, common ground, and continuous input current are satisfied simultaneously under the condition of using few components. Continuous input current is a desirable characteristic of DC-DC converters that is necessary for practical applications. After working principle and steady-state analyses, the salient features are compared in detail. Then, the performance of the converter and the correctness of the analysis are verified through the results of the experimental prototype.

Keywords Fuel cell, Continuous input current, Wide voltage gain, Voltage stress.

1 Introduction

Energy issues have recently received continuous attention from humans. With the depletion of fossil fuel, renewable-energy power generation systems, such as fuel cells, have been developed rapidly [1]. Fuel cells for electric vehicles, with their advantages of high power density, good stability, environmental protection, and energy saving, are increasingly favored by countries all over the world. However, the output terminal voltage of fuel cell power generation units is generally only tens of volts and easily varies with load changes. Studying converters with a wide voltage gain is necessary to achieve voltage matching between the low-voltage output fuel cell side and the internal high-voltage bus side of electric vehicles [2]. Compared with isolated step-up converters [3-4], non-isolated step-up converters have a transformerless structure, and they have no leakage inductance and excessive volume issues caused by transformer operation in high-power applications. Therefore, non-isolated converters are more in line with the actual needs of electric vehicles than isolated converters, and they can reduce system costs and size and improve efficiency.

Conventional boost converters use only two passive elements and have a single-switch topology. However, the gain is limited to three to four times of the input voltage [5]. Therefore, various boost technologies in which basic energy storage elements (inductance and capacitance), transformers, switches, and diodes are used have been proposed in literature. These technologies include voltage multipliers, switched capacitors (SCs), and multistage topology [6]. Although multistage boosting and multi-element-based topologies [7] achieve high boosting, they greatly increase the number of storage components and the complexity of circuits. With a relatively small duty cycle, voltage gain can be further improved by coupled inductors [8-10]. However, the active switches of these converters are subject to high voltage stress.

Topologies to reduce the voltage and current stress on active switches were proposed in [11] and [12]. However, many active and passive elements are used in these topologies. Moreover, the size and cost of the system are increased because of the multiple multiplier cells. As a result, many topologies with only a few elements have been developed [13-16]. Single switch, minimum ripples on the source side, and common ground are some of the desirable performance goals of converters. In [13], a transformerless high-boost converter was proposed. The converter reduces the voltage and current stresses on active switches, and it uses two main switches and requires two isolated gate driver circuits. In [14], a classic SC converter with four energy storage elements in the circuit was developed. The voltage gain is increased, but the input and output have no common ground. Another simple step-up converter that solely uses a switched inductance Unit was also presented

* Yu Tang
ty8025@hotmail.com

1 State Key Laboratory of Reliability and Intelligence of Electrical Equipment, Hebei University of technology, Tianjin, China

2 Electrical engineering college, Yancheng Institute of Technology, Jiangsu, China

3 Electrical Engineering and Electronics Brownlow Hill Liverpool, University of Liverpool, England, UK

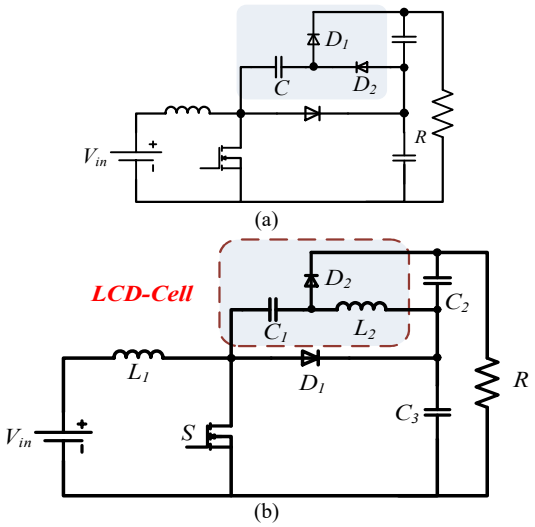


Fig. 1 **a** switched-capacitor-based boost converter [19]; **b** proposed boost converter integrated with an *LCD* cell

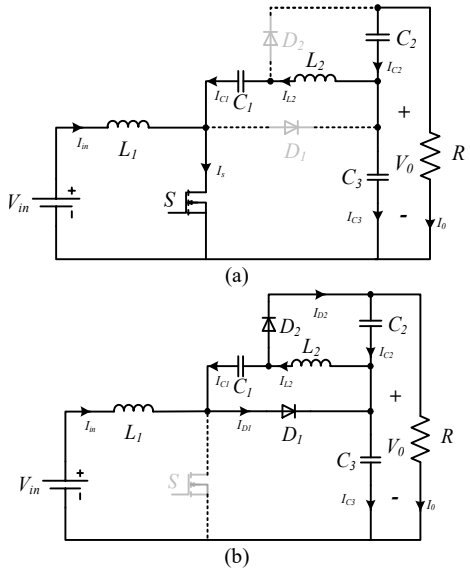


Fig. 2 Operation modes in CCM: **a** mode I; **b** mode II

in [15]. However, its main limitation is that it has discontinuous source current, and the voltage stress of the switch is equal to the load voltage. A modified SI boost converter that maintains the same voltage gain was proposed in [16], but the diode voltage stress is high, and many switches are used. The structures of the converters [13-16] mentioned above are simple, and they have the advantages of reliability, low cost, and simplified design implementation and manufacturing. However, these converters cannot simultaneously satisfy the requirements of having a single switch, low voltage and current stress, common ground, and continuous input current under the condition of achieving a wide gain.

To address the inherent shortcomings of existing step-up topologies based on the simple boost topology, in the current study, an inductor–capacitor–diode cell (*LCD* cell) is suitably added based on the classic boost circuit; the topology is called *LCD*-cell-based boost converter (*LCDBC*). The number of components in *LCDBC* is similar to that in the converters reported in [17-19]. As shown in Fig. 1a, a capacitor and two diodes are arranged in the boost topology [19]. However, the inrush current when the switch is on worsens the electromagnetic interference (EMI) and affects circuit reliability. The inrush current can be eliminated using diode D_2 with an inductor instead. This study analyzes the working principle and circuit performance of the proposed converter in detail and verifies the correctness of the theoretical analysis through experiments. The main advantages of the proposed converter are as follows:

1) The voltage gain is higher than that in the classic boost converter, and the stress of the power component is reduced;
2) The input current is continuous;
3) Only one switch is utilized;
4) The converter can work in a wide range of duty cycles and has positive output voltage polarity;
5) The input and output have a common ground.

2 Operating Principle of *LCDBC*

The circuit topology of the proposed boost converter is shown in Fig. 1b. It combines an *LCD* cell and a basic boost converter and is thus named *LCDBC*. The *LCD* cell composed of capacitor C_1, diode D_2, and inductor L_2 is connected in parallel across the diode of a traditional converter, which includes a single switch S, diode D_1, inductor L_1, and capacitors C_2 and C_3. The *LCD* circuit utilizes parallel charging and series discharging to achieve an increased boost gain. Therefore, without increasing the number of components, a slight modification is made to the classic boost circuit to reduce the voltage stress of the switch and obtain high gain. The converter can work in continuous conduction mode (*CCM*) and discontinuous conduction mode (*DCM*). The following assumptions are made to simplify the circuit analysis.

1) The active and passive elements are ideal and lossless.
2) All capacitances are taken as large enough.
3) The current of the inductor changes linearly.

2.1 *CCM* Operation

The converter has two operating modes in one switching period under *CCM*: switch *ON* and switch *OFF*. Both operation modes of *LCDBC* are shown in Fig. 2, and the key waveforms are given in Fig. 3. An analysis of the operating modes is presented as follows.

Mode I [t_0–t_1]: When switch S is turned on, diodes D_1 and D_2 are reverse-biased. The current flow path in this mode is shown in Fig. 2a. The source energy is transferred to inductor L_1, and the currents of inductors L_1 and L_2 increase

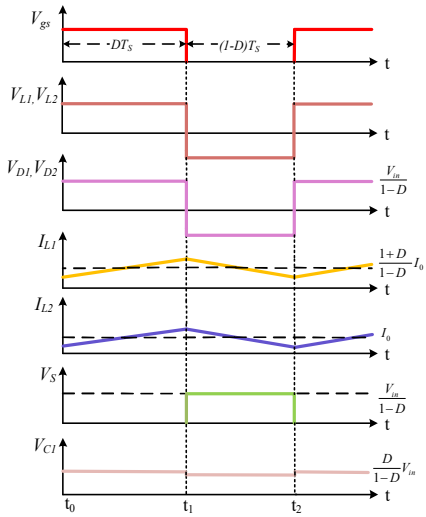


Fig. 3 Some waveforms of the proposed converter in CCM

linearly in the positive direction. At the same time, the energy saved in capacitors C_2 and C_3 is released to capacitor C_1 and load R. Therefore, the voltages of the inductors can be expressed as follows:

$$\begin{cases} V_{L1} = V_{in} \\ V_{L2} = V_0 - V_{C1} - V_{C2} \end{cases}. \tag{1}$$

Mode II [t_1–t_2]: When switch S is turned off, D_1 and D_2 are forward-biased as shown in Fig. 2b. In this interval, the energy stored in L_1 and the input power source is delivered to C_2 and C_3 through diodes D_1 and D_2. Meanwhile, C_3 is charged by inductor L_2 and capacitor C_1 through diode D_1. Hence, the following relationships can be obtained:

$$\begin{cases} V_{L1} = V_{in} + V_{C1} - V_0 \\ V_{L2} = -V_{C1} \\ V_{C1} = V_{C2} \end{cases}. \tag{2}$$

2.2 *DCM* Operation

The equivalent circuit of *LCDBC* in *DCM* is shown in Fig. 4, and the characteristic waveforms are illustrated in Fig. 5. Assume that the inductor current reaches zero at time t_2, and D_M is the PWM turn-off demagnetization ratio.

Mode I [t_0–t_1]: The equivalent circuit is similar to that in Mode I operated in *CCM*. The difference is that the current of L_2 flows in both directions, and i_{L2} falls from the reverse peak to the forward peak until all the diodes are turned on in t_1. The maximum current through L_1 and L_2 can be obtained as

$$\begin{cases} V_{L1} = V_{in}, \ V_{L2} = V_{in} \\ I_{L1\text{–pk}} = \dfrac{V_{in} D T_S}{L_1}, \ I_{L2\text{–pk}} = \dfrac{V_{in} D T_S}{L_2} \end{cases}, \tag{3}$$

where $I_{L1\text{-pk}}$ and $I_{L2\text{-pk}}$ are the peak currents of L_1 and L_2, respectively.

Mode II [t_1–t_2]: The equivalent circuit is similar to that in

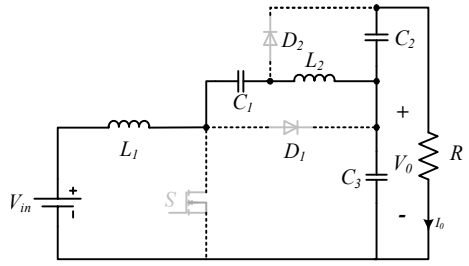


Fig. 4 Operation modes of the converter in Mode III under DCM operation

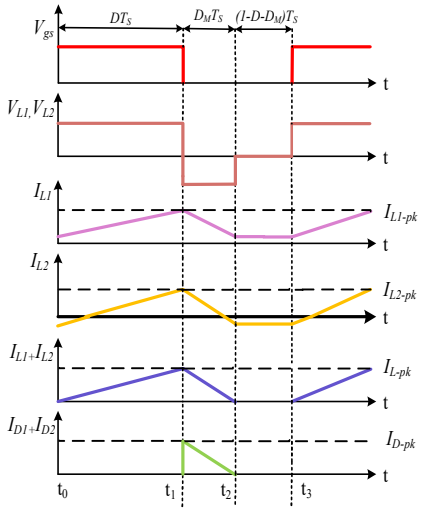


Fig. 5 Some waveforms of the proposed converter in DCM

Mode II operated in *CCM*. The time interval in this mode is $D_M T_S$. However, the current of L_2 still flows in both directions, and i_{L2} falls from the forward peak to the reverse peak. In this state, the current of the diodes decreases. At the end of Mode II, i_{L1} and i_{L2} have the same amplitude but opposite directions. The sum of the average currents of diodes D_1 and D_2 is

$$I_{D1} + I_{D2} = I_{L1} + I_{L2}. \tag{4}$$

Mode III [t_2–t_3]: As shown in Fig. 4, switch S and diodes D_1 and D_2 are turned off, and the currents of L_1 and L_2 flow in reverse. Therefore, the load is powered by C_3, and the inductor voltage in this mode is zero.

3 Steady-state Analysis of the Converter

3.1 Voltage and Current Stress

Assuming that *LCDBC* works in switching period T_S, the on-time of S is DT_S, and the off-time is $(1\text{-}D)T_S$. In accordance with the balancing of inductances L_1 and L_2 in volt-seconds in a switching period, the voltage stress of the capacitors and the voltage gain can be obtained from Equations (1) and (2) as follows:

$$\begin{cases} V_{C1} = \dfrac{D}{1-D} V_{in} = V_{C2}, \ V_{C3} = \dfrac{1}{1-D} V_{in} \\ M = \dfrac{V_0}{V_{in}} = \dfrac{1+D}{1-D} \end{cases}. \tag{5}$$

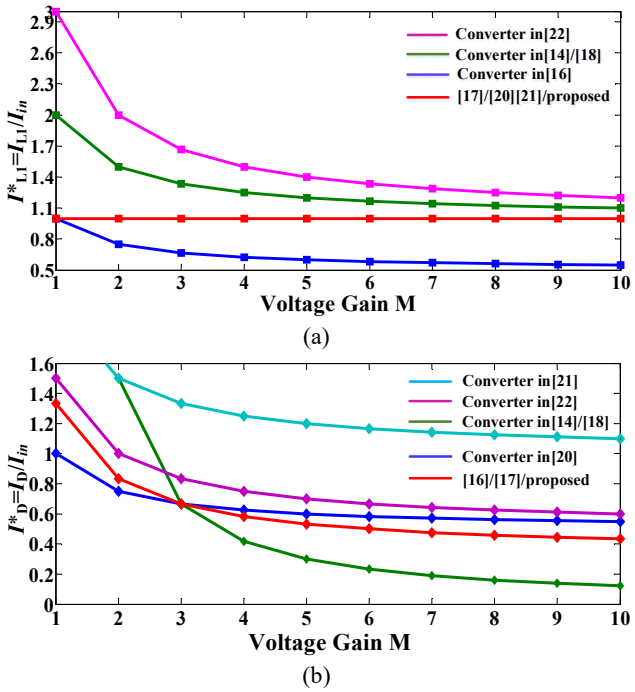


Fig. 6 **a** variation of the average current stress of inductor L_1 with voltage gain; **b** variation of the average current stress of diode D

Compared with the voltage gain of the traditional boost converter, the voltage gain of *LCDBC* is increased by (1-*D*) times, and it has better boost capability. The voltage stresses of the switch and diodes are as follows:

$$\begin{cases} V_{D1} = V_{D2} = \dfrac{1}{1-D} V_{in} \\ V_S = V_{in} - V_{L1} = \dfrac{1}{1-D} V_{in} \end{cases} . \tag{6}$$

The input current of *LCDBC* is determined by I_0 and the duty ratio (D). Assuming that the loss is negligible, the source current (I_{in}) can be obtained from the power balance ($V_{in}I_{in}$= V_0I_0) as follows:

$$I_{\text{in}} = I_{L1} = \frac{V_{in}(1+D)^2}{R(1-D)^2} . \tag{7}$$

At State I, the average currents of capacitors C_1, C_2, and C_3 are expressed as

$$\begin{cases} I_{C1,\text{on}} = I_{L2} \\ I_{C2,\text{on}} = -I_0 \\ I_{C3,\text{on}} = -2I_0 \end{cases} . \tag{8}$$

The average currents of C_1, C_2, and C_3 in State II are expressed a:

$$\begin{cases} I_{C1,\text{off}} = I_{L2} - I_0 - I_{C2,\text{off}} \\ I_{C3,\text{off}} = I_{C1,\text{off}} + I_{L1} - I_{L2} + I_{C2,\text{off}} \end{cases} . \tag{9}$$

Applying the ampere-second balance to the capacitors yields the average currents of L_2(I_{L2}), C_1, and C_2 ($I_{C1,on}$ and $I_{C2,on}$).

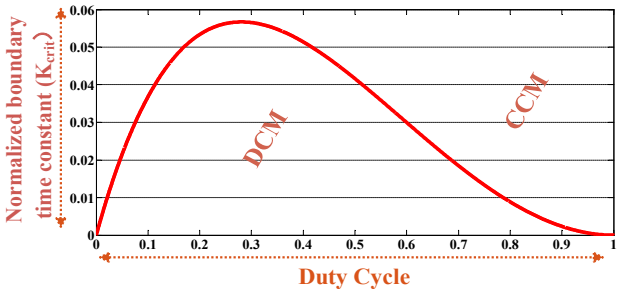


Fig. 7 Boundary normalized inductor time constant versus duty cycle

$$\begin{cases} I_{L2} = \dfrac{V_{in}(1+D)}{R(1-D)} \\ I_{C1,\text{on}} = \dfrac{V_{in}(1+D)}{R(1-D)} \\ I_{C2,\text{on}} = -\dfrac{V_{in}(1+D)}{R(1-D)} \end{cases} \tag{10}$$

From Fig. 2, the current stress of diodes D_1 and D_2 (I_{D1} and I_{D2}) and switch S (I_S) can be obtained as

$$\begin{cases} I_S = \dfrac{V_{in}(2+2D)}{R(1-D)} \\ I_{D1} = \dfrac{V_{in}(1+D)}{R(1-D)^2} \\ I_{D2} = \dfrac{V_{in}(1+D)}{R(1-D)^2} \end{cases} . \tag{11}$$

The average current stresses normalized by I_{in} of the proposed converter and other boost converters are shown in Fig. 6. As indicated in Figs. 6(a) and 6(b), the converter has low average current stress of inductor L_1 and diode D, respectively. Although the converter in [16] has the lowest inductor current stress, it has high voltage stress across diode D_0 and requires two active switches, which make the drive control design highly complicated. Moreover, the converters in [14] and [18] have no common grounding between the input and output, as shown in Fig. 6b.

3.2 *DCM* Operation

Assuming that DT_S and D_MT_S are the time intervals of States I and II, respectively, and the time interval in *DCM* corresponding to State III is obtained as $(1-D-D_M)$ T_S. According to the current waveform in Fig. 5 and Equation (4), the relationship between the average currents of diodes D_1 and D_2 can be determined as follows:

$$I_{D1,av} = I_{\text{D2,av}} = \frac{V_0}{R} , \tag{12}$$

$$\begin{cases} I_{D1,av} + I_{\text{D2,av}} = \dfrac{1}{2} \times D_M \times I_{D-\text{pk}} \\ I_{D-pk} = I_{L1-pk} + I_{L2-pk} = \dfrac{V_{in}DT_S}{L_1} + \dfrac{V_{in}DT_S}{L_2} \end{cases} , \tag{13}$$

where $I_{D\text{-}pk}$ is the sum of the peak currents of inductors L_1

and L_2. By using volt-second balance on inductors L_1 and L_2, the duty cycle in State II (D_M) and the voltage gain of the converter under *DCM* can be obtained as

$$\begin{cases} D_M = \dfrac{(1+D)V_{in}}{V_0} \\ M_{DCM} = \sqrt{\dfrac{D(1+D)}{2K}} \end{cases}, \tag{14}$$

where the normalized inductor time constant is obtained as follows:

$$\begin{cases} K = \dfrac{2L}{RT_S} \\ \dfrac{1}{L} = \dfrac{1}{L_1} + \dfrac{1}{L_2} \end{cases}. \tag{15}$$

3.3 Boundary Conduction Mode

When the converter is operated in boundary conduction mode (*BCM*), the voltage transfer gain in *CCM* is equal to the voltage transfer gain of *DCM*. Hence, by combining Equations (5) and (14), the boundary-normalized inductor time constant is

$$K_{crit} = \frac{D(1-D)^2}{2(1+D)}, \tag{16}$$

where K_{crit} is the boundary-normalized inductor time constant, as shown in Fig. 7.

When K is less than K_{crit}, the converter operates in *DCM* mode. A comparison of the inductor time constants of different converters is shown in Fig. 8. The converters are the proposed converter; the converters in [20], [21], and [22]; and the conventional boost converter. The proposed *LCDBC* is less likely to work in *DCM* compared with the other converters, as shown in Fig. 8.

3.4 Comparative Analysis

To reveal the salient features of the proposed converter, a comprehensive comparison of *LCDBC* with other similar boost topologies with the same voltage gain is provided in Tables 1 and 2. The comparison is conducted based on component numbers, component stress level, nature of source current, and current ripple on semi-conductors. This comparative analysis can reflect the feasibility of the topology and help in the selection of a proper topology that meets the performance requirements of specific applications. In addition to having the same voltage gain, the converters in [14], [16], [17], and [18] have another common feature: simple in structure with fewer passive components compared with a high-gain network [9] and easy to implement in step-up voltage applications.

The structure in [16] has the least passive components (three), but it needs two active switches, which increases

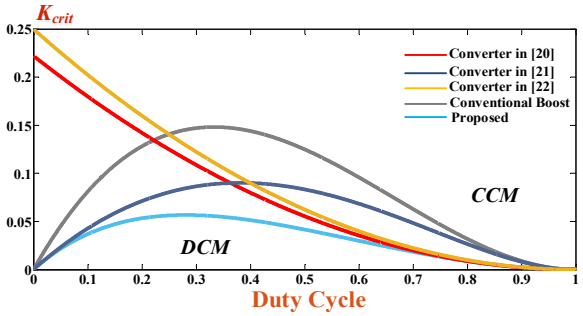
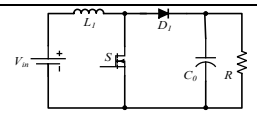
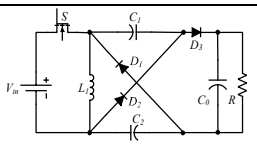
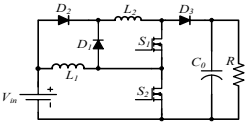
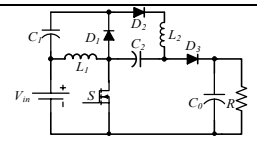
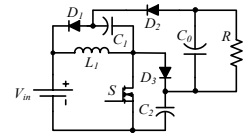
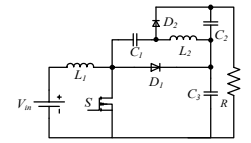


Fig. 8 Comparison of the curves of boundary inductor time constants of the proposed converter and other converters

Table 1 Topologies of *LCDBC* and other converters

Converter types	Topologies	Load voltage polarity
Boost converter		Non-inverting
Converter in [14]		Non-inverting
Converter in [16]		Non-inverting
Converter in [17]		Non-inverting
Converter in [18]		Inverting
Proposed topology		Non-inverting

the circuit complexity. Interference also occurs between the two switches, resulting in voltage spikes, and the voltage stress on D_0 is high. The proposed converter has the advantage of common ground, which is unavailable in topologies [14]and [18]. The capacitor voltage stress in the converter in [18] is high and equal to the voltage stress of the switch and diode, whereas the voltage stress of the capacitors in *LCDBC* is comparatively low. Additionally, a significant reduction in the source current ripples can be seen in the proposed circuit mainly due to the presence of inductor L_1 at the source side. Although the converters in [14], [17], and [18] have an identical voltage gain, they have a discontinuous input current and thus need additional filtering components.

Table 2 Comparison of *LCDBC* with other boost converters

Topologies	Conventional converter	Converter in [16]	Converter in [14]	Converter in [17]	Converter in [18]	Proposed Topology
Number of L/C	1/1	2/1	1/3	2/3	1/3	2/3
Number of S/D	1/1	2/3	1/3	1/3	1/3	1/2
TNC	4	8	8	9	8	8
NSC	Smooth	Non-pulsating	Pulsating	Non-pulsating	Non-pulsating	Smooth
(CG)	CG	CG	NO-CG	CG	NO-CG	CG
Voltage gain	$1/(1-D)$	$(1+D)/(1-D)$	$(1+D)/(1-D)$	$(1+D)/(1-D)$	$(1+D)/(1-D)$	$(1+D)/(1-D)$
NSVS (V_s/V_{in})	G_1	S_1 S_2 G_2 G_1	G_1	G_1	G_1	G_1
NDVS(V_D/V_{in})	G_1	D_1 D_0 G_2 M	G_1	G_1	G_1	G_1
NCVS (V_C/V_{in})	—	—	C_1 C_2 G_2 G_2	C_1 C_2 G_2 G_2	C_1 C_2 G_2 G_1	C_1 C_2 G_2 G_2
ICS	L_1 $\left[\frac{M+1}{2}\right]I_0$	L_1 $\left[\frac{M+1}{2}\right]I_0$	L_1 $(M+1)I_0$	L_1 L_2 MI_0 I_0	L_1 $(M+1)I_0$	L_1 L_2 MI_0 I_0
SCS	$\left[P_1+\frac{P_2}{2L_1}\right]$	$\left[P_1+\frac{P_2}{2L_1}\right]$	$\left[\frac{1+D}{D}P_1\right]$	$\left[2P_1+\frac{P_2}{2L_e}\right]$	$\left[\frac{1+D}{D}P_1\right]$	$\left[2P_1+\frac{P_2}{2L_e}\right]$
DCS	$\left[P_1+\frac{P_2}{2L_1}\right]$	$\left[P_1+\frac{P_2}{2L_1}\right]$	$\left[\frac{I_0}{D}+\frac{P_2}{2L_1}\right]$	$\left[P_1+\frac{P_2}{4L_e}\right]$	$\left[\frac{I_0}{D}+\frac{P_2}{2L_1}\right]$	$\left[P_1+\frac{P_2}{4L_e}\right]$
SCR	$\left[\frac{P_2}{L_1}\right]$	$\left[\frac{2P_2}{L_1}\right]$	$\left[\frac{1+D}{D}P_1\right]$	$\left[(1+D)P_1+\frac{P_2}{2L_e}\right]$	$\left[P_1+\frac{3P_2}{4L_1}\right]$	$\left[\frac{P_2}{L_1}\right]$
OCCR	$\left[P_1+\frac{P_2}{2L_1}\right]$	$\left[(1+D)P_1+\frac{P_2}{2L_1}\right]$	$\left[\frac{I_0}{D}+\frac{P_2}{2L_1}\right]$	$\left[(1+D)P_1+\frac{P_2}{2L_e}\right]$	$\left[\frac{I_0}{D}+\frac{P_2}{2L_1}\right]$	$\left[2P_1+\frac{P_2}{2L_e}\right]$
Features	▪ Common ground ▪ Smooth source current	▪ Common ground ▪ Low voltage stress on S_1	▪ Low voltage stress on C_1 and C_2	▪ Common ground ▪ Low voltage stress on C_1 and C_2	▪ Low voltage stress on C_1	▪ Common ground ▪ Smooth source current ▪ Low voltage stress on C_1 and C_2 ▪ One main switch
Limitations	▪ Low voltage gain ▪ High current ripple in output capacitor ▪ Voltage stress is equal to the output voltage	▪ Utilizes two switches ▪ High source current ripple ▪ High current ripple in output capacitor ▪ High voltage stress on D_0	▪ No common ground ▪ High source current ripple	▪ High source current ripple ▪ High current ripple in output capacitor	▪ No common ground ▪ High source current ripple ▪ High voltage stress on C_2 ▪ Inverting output voltage	▪ High current ripple in output capacitor

Note: TNC–Total number of components, NSC–Nature of source current, CG–Common ground, NSVS–Normalized switch voltage stress, NDVS–Normalized diode voltage stress, NCVS–Normalized capacitor voltage stress, ICS–Inductor current stress, SCS–Switch current stress, DCS–Diode current stress, SCR–Source current ripple, OCCR–Output capacitor current ripple, $G_1=1/(1-D)$, $G_2=D/(1-D)$, $M=(1+D)/(1-D)$, $p_1=I_0/(1-D)$, $p_2=V_{in}D_1/f_s$, $L_e=L_1L_2/(L_1+L_2)$

The other converters presented in Table 2 have many limitations. Converters with a simple structure cannot simultaneously have the features of single switch, low voltage and current stress, common ground, and continuous input current under the condition of using few components. However, *LCDBC* with the *LCD* structure not only retains the advantages of conventional boost converters, such as common ground and continuous input current, but also improves the voltage gain and reduces the voltage stress. Therefore, it can simultaneously satisfy all the requirements mentioned above.

The normalized current stress across the switch is shown in Fig. 9a. The current stress of the proposed converter is lower than those of the converters in [14] and [18]. The topology in [16] has a slightly lower device stress, but it requires two drivers to drive the switches and has some of the disadvantages mentioned above. The normalized source current ripple bar graph shown in Fig. 9b is drawn for all the converters listed in Table 1 with the same rated power (55→380 V, 200 W).

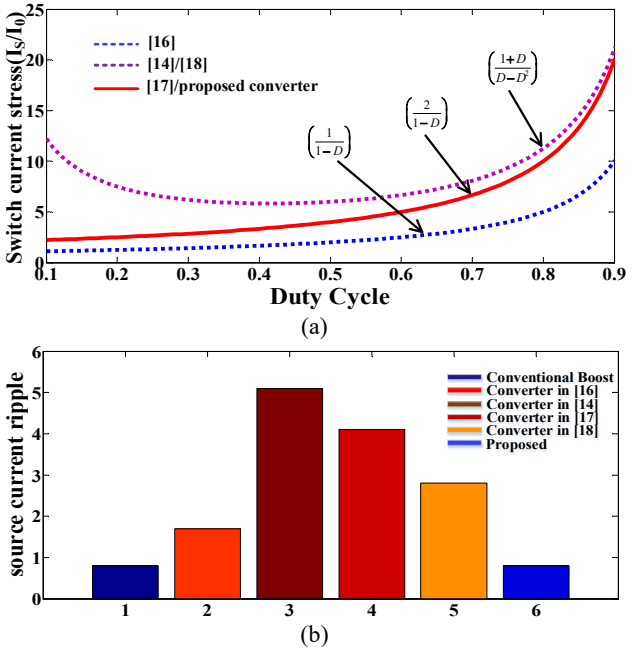


Fig. 9 **a** normalized switch current stress of the converters versus duty cycle; **b** normalized source current ripple

Evidently, the proposed *LCDBC* has the lowest source current ripple among all the converters.

3.5 Efficiency Analysis

Efficiency depends on the internal characteristics of all components of converters, and it includes switching, diode, inductance, and capacitance losses. Assuming that the on-resistance of the MOSFET is $R_{s(on)}$, t_{on} and t_{off} are the device static features of manufacturing data sheet information and $I_{s(rms)}$ is the *RMS* current of switch *S*. The losses of switch *S* are as follows:

$$\begin{cases} P_{sw} = I^2_{s(rms)} R_{s(on)} + \dfrac{1}{2} f_S V_S I_S (t_{on} + t_{off}) \\ P_{sw} = \dfrac{4D}{(1-D)^2} I_0^2 R_{s(on)} + \dfrac{1}{(1-D)^2} f_S V_{in} I_0 (t_{on} + t_{off}) \end{cases}, \quad (17)$$

The RMS current and average current through the diodes are $I_{D(rms)}$ and I_D, respectively. R_F and V_F are the forward resistance and threshold voltage of the diodes, respectively, and they are considered based on the characteristics provided in the datasheet. The losses are as follows:

$$P_D = I^2_{D(rms)} R_F + V_F I_D = \frac{1}{1-D} (I_0^2 R_F + V_F I_0). \quad (18)$$

The losses of inductors L_1, L_2 and capacitors C_1, C_2, C_3 can be derived as follows:

$$\begin{cases} P_{RL1} = I^2_{L1(rms)} R_{L1} = \left(\dfrac{1+D}{1-D}\right)^2 I_0^2 R_{L1} \\ P_{RL2} = I^2_{L2(rms)} R_{L2} = I_0^2 R_{L2} \end{cases}, \quad (19)$$

$$\begin{cases} P_{rC1} = I^2_{C1(rms)} r_{C1} = \dfrac{D}{1-D} I_0^2 r_{C1} = P_{rC2} \\ P_{rC3} = I^2_{C3(rms)} r_{C3} = \dfrac{4D}{1-D} I_0^2 r_{C3} \end{cases}, \quad (20)$$

where R_{L1} and R_{L2} are the ESRs of inductors and r_{C1}, r_{C2}, and r_{C3} are the ESRs of capacitors. $I_{L(rms)}$ is the RMS current through the inductors. The total losses in the converter can be calculated from Equations (17), (18), (19), and (20) as follows:

$$P_{loss,total} = P_{sw} + 2P_D + \sum_{u=1}^{2} P_{RLu} + \sum_{u=1}^{3} P_{rCu}. \quad (21)$$

The efficiency of the proposed converter (η) can be derived as follows:

$$\eta = \frac{1}{1 + \dfrac{P_{loss,total}}{P_0}}. \quad (22)$$

Hence, the efficiency of the converter can be determined with Equation (23) as follows:

$$\eta = \frac{1}{1 + \dfrac{A}{R(1-D)^2} + \dfrac{B}{R(1-D)^2 I_0}}, \quad (23)$$

where

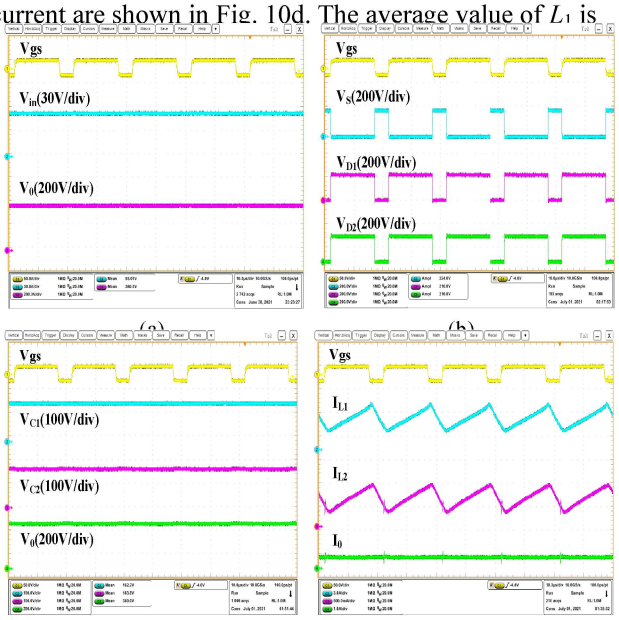
$$\begin{cases} A = 4DR_{s(on)} + (1+D)^2 R_{L1} + (1-D)^2 R_{L2} + D \\ \quad \times (1-D)(r_{C1} + r_{C2} + 4r_{C3}) + 2R_F(1-D) \\ B = f_S V_{in} (t_{on} + t_{off}) + 2V_F (1-D) \end{cases}. \quad (24)$$

4 Experiment Results

A 200 W, 50 kHz prototype circuit is built to validate the steady-state analysis of the proposed converter on the basis of the specifications and parameters in Table 3. The aim is to increase the source voltage of 55–165 V to 380 V at load.

The significant advantages of the proposed *LCDBC* are verified by experiments, and the measured observation results are presented in Figs. 10–11. Fig. 10 shows the experimental waveform when the input voltage is 55 V and the output voltage is 380 V, and the theoretical voltage gain is validated with the experimental results. Fig. 10b indicates that the voltage stress of switch *S* is 224 V, but it is still lower than the output voltage. The voltage stress of diodes D_1 and D_2 is less than 216 V, which is consistent with the theoretical calculation values and indicates that the theoretical derivation is correct. A notable feature of the proposed topology is that it reduces the voltage stress on all capacitors. Fig. 10c presents the voltage waveform across capacitors C_1 and C_2. When the output voltage gain is high enough, capacitors C_1 and C_2 are only charged to three times the source voltage. The waveforms of inductor

current are shown in Fig. 10d. The average value of L_1 is

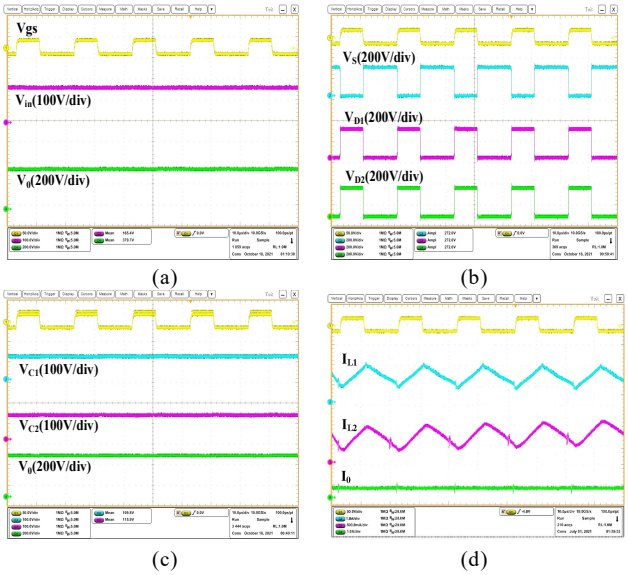


(c) (d)

Fig. 10 Experiment results with $V_{in} = 55$ V: **a** voltage gain; **b** voltage across switch S_1 and diodes D_1 and D_2; **c** voltage stress across capacitors C_1 and C_2; **d** current across inductors L_1 and L_2 and output current

Table 3 Components and their parameters

Components	Parameters
Rated Output Power P_0	200 W
Output Voltage V_0	380 V
Input Voltage V_{in}	55–165 V
Switching Frequency	50 kHz
Switch	IRFP4868PBF
Diodes D_1 and D_2	SDUR530
Input Inductor L_1	0.47 mH
Inductor L_2	1.5 mH
C_1/C_2 (Capacitors)	47 μF
C_3 (Capacitors)	100 μF



(a) (b)

(c) (d)

Fig. 11 Experiment results with $V_{in} = 165$ V: **a** voltage gain; **b** voltage across switch S_1 and diodes D_1 and D_2; **c** voltage stress across capacitors C_1 and C_2; **d** current across inductors L_1 and L_2 and output current

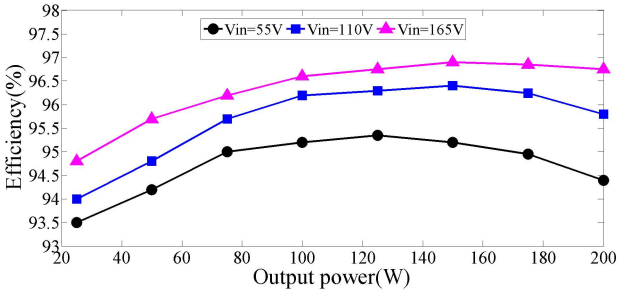


Fig. 12 Measured efficiency curves of the proposed converter

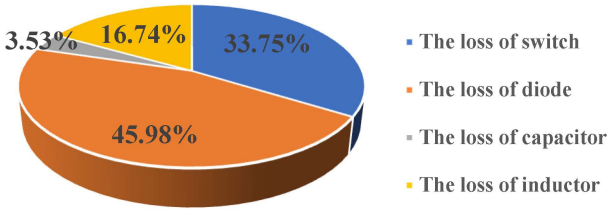


Fig. 13 Power loss distributions in the proposed converter

equal to the average value of input current, and the average value of L_2 is equal to the average output current. Source current I_g is smooth, and the ripple is low (Δi_g=0.81 A).The average values of the currents of inductors L_1 and L_2 are 3.68 and 0.52 A, respectively, and the current ripples are within the allowable range.

The experiment results for 165 V are shown in Fig. 11. The correctness of the theoretical analysis and the wide voltage gain of the converter are confirmed. The relationship between the measured efficiency of the proposed converter and the output power under different source voltage values is plotted in Fig. 12. An increment in input voltage improves the efficiency of the converter. When the input voltage is 165 V, the peak efficiency of the proposed converter is greater than 96.65%. The power loss distributions across each component of the proposed converter are also calculated and graphically shown in Fig. 13. When $V_{in} = 55$ V, $P_0 = 200$ W.

5 Conclusion

A novel wide-gain boost converter based on *LCD* cell was proposed in this study. The proposed topology has none of the drawbacks of other reported *LCD* cell-based topologies, such as lack of common ground, highly pulsating source current, inverted load voltage polarity, and numerous switching devices. A detailed analysis of the converter revealed that it simultaneously possesses the features of single switch, low voltage and current stress, common ground, and continuous input current under the condition of achieving a wide gain. Operation principle and steady-state analyses were also performed. The experimental results verified the analyses. The proposed converter achieves an efficiency of 96.65% at 200 W of power, so it is suitable for

fuel cells and electric vehicles.

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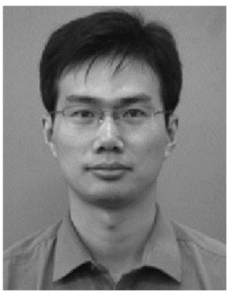
Yinghao Song received her B.S. degree in electrical engineering from Taiyuan University of Science and Technology, Shanxi, China, in 2020. She is currently pursuing her M.S degree in power electronics at Hebei University of Technology, Tianjin, China. Her current research interests include DC-DC converters and renewable power conversion systems.

Yu Tang received his B.S. and Ph.D. degrees from the Department of Electrical Engineering, Nanjing University of Aeronautics and Astronautics (NUAA), China, in 2003 and 2008, respectively. He joined the Electrical Engineering Department of NUAA in 2008 and the State Key Laboratory of Reliability and Intelligence of Electrical Equipment, Hebei University of Technology, in 2018. He has published more than 80 papers in journals and conference proceedings. His research area includes power electronics in renewable energy generation.



Jiarong Kan received his M.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), China, in 2007. In 2007, he joined the School of Electrical Engineering, Yancheng Institute of Technology, Yancheng, China, where he is currently an associate professor. He is the holder of seven patents and the author or co-author of more than 40 technical papers. His current research interests include power electronics in renewable energy generation.

Lin Jiang received his B.S. and M.S. degrees in electrical engineering from Huazhong University of Science and Technology (HUST), Wuhan, China, in 1992 and 1996, respectively, and his Ph.D. degree in electrical engineering from the University of Liverpool, Liverpool, U.K., in 2001. From 2001 to 2003, he was a postdoctoral research assistant at the University of Liverpool, and from 2003 to 2005, a postdoctoral research associate at the Department of Automatic Control and Systems Engineering, The University of Sheffield, Sheffield, U.K. From 2005 to 2007, he was a senior lecturer at the University of Glamorgam, Wales, U.K., and in 2007, he joined the University of Liverpool. He is currently a Reader at the University of Liverpool. His current research interests include control and analysis of power systems, smart grids, and renewable energy.