An Investigation into the Optimal Device Design for Selenium Solar Cells

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Despite a resurgence in recent years, the optimal device design for selenium solar cells is still not known with individual studies using significantly different window layers, hole transport layers and selenium absorber thicknesses. In this work we present results comparing the effect of each of these on device performance and propose that the ideal absorber thickness is influenced by the specific device structure being utilized. A TiO_2 window layer and P3HT hole transport layer with a 200 nm Se absorber layer was found to produce the best performance of 2.1% from materials investigated in this study, however performance remains limited due to the presence of an interfacial charge extraction barrier apparent from current-voltage analysis.

1.   Introduction

The photoconductivity of elemental Selenium was discovered in 1873 by Smith [1] and 10 years later the world's first solid state photovoltaic devices were created by coating metal foils with selenium and thin layers of gold [2]. Despite this early work, PV research began to focus on silicon due to the rise of the microelectronics industry and propelled it from efficiencies of 6% in the 1950's to efficiencies greater than 20% today [3]. In comparison, Se solar cells displayed efficiencies below 1% in the late 19th century and performance plateaued in the 1980's with a peak efficiency of 5% [4].

Despite the relatively low efficiency compared to some emerging PV technologies, selenium has several attractive advantages. It is an earth abundant material with a high absorption coefficient [5] and therefore has the potential for low cost large-scale future deployment. The melting point of Se at 220°C allows processing at comparatively low temperatures which reduces costs of fabrication. Since Se cells are based on a single-element absorber, the fabrication process is simplified and highly reproducible compared to other more complex PV technologies such as CZTS and CIGS, offering another potential route to cost saving. Selenium is an air stable and largely non-toxic material, in contrast to the heavy metal content of Cd in CdTe and the Pb content and stability issues in perovskite solar cells [6]. Whilst the reported 1.83 eV band gap of Se [7] is not ideal for application as a sole absorber under AM1.5 illumination, it may have long-term potential for indoor applications [8] or as a top cell in tandem devices. The leading efficiency of Si cells has increased by less than 2% in the last 20 years as they approach their Shockley-Queisser limit [9], and therefore tandem approaches with Si are now receiving wider attention.

During the 1980's Se research focused predominantly on different window layers such as CdO [10], ITO [11, 12], CdSe [13] and TiO_2 [4], with almost all of these using a thin (<30 nm) Te wetting layer to aid adhesion between the window layer and Se absorber layer. The device efficiency varied from 3.04% with CdO [10], 3.30% with ITO [12], 4.20% with CdSe [13] and peaked at 5.01% with the use of TiO_2 [4]. In addition to the variation of window layer, each study also utilized different Se absorber thicknesses ranging from 1–8 μm, making direct comparison difficult. In more recent years research has been focused on various hole transport layers (HTL) used to aid charge collection and transportation from Se to an external circuit. These have included poly(3-hexylthiophene-2,5-diyl) (P3HT) [14], poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) [14], spiro-OMeTAD [14], poly(triaryl amine) (PTAA) [15], phenyl-C61-butyric acid methyl ester (PCBM) [16] and molybdenum oxide (MoO_x) [17]. The current highest efficiency Se device reported employed a ZnMgO (MZO) window layer and a MoO_x HTL, but with only a 100 nm Se absorber to attain as efficiency of 6.50% [17]. In contrast to these results, Hadar *et al.* achieved an efficiency of 5.20% with a TiO_2 window layer, no HTL and a much thicker 1 μm Se layer [18]. They found that J_{SC} decreased with decreasing

Se thickness and propose that this occurs due to lower absorption near the band edge and hence a thicker film is required to absorb the light.

Comparing the prior work it is difficult to determine what is the key performance limiting factor for Se solar cells, and the optimal device design for a Se solar cell is clearly reliant on several factors; a) the ideal window layer, b) the ideal hole transport layer and c) the ideal absorber layer thickness. In this work we directly compare the influence of each of these on device performance in attempt to identify the crucial limiting aspects of the Se device structure.

2.   Experimental

TiO$_2$ was deposited on NSG Ltd. TEC15 SnO$_2$:F coated soda-lime glass by spin coating 250 μl of solution onto the substrate at 3000 rpm for 30 seconds. Two layers were deposited with each layer dried at 120°C for 10 minutes and allowed to cool prior to the next deposition. The solution consisted of TTIP in ethanol at a concentration of 0.3 M, this gave a thickness of about 60 nm. The coated substrates were then sintered at 500°C for 30 minutes in air. CdS and CdSe were both deposited on identical TEC15 substrates via RF-magnetron sputtering at a substrate temperature of 200°C with 60 W and 5 mTorr pure Ar for 30 minutes. Sputtered TiO$_2$ layers were deposited at 150 W under 3 mTorr Ar with 1% O$_2$. Layers of Te and Se were deposited by thermal evaporation from the powders (both 5N, Alfa-Aesar) onto unheated substrates. The thicknesses of all evaporated samples were monitored using a quartz crystal microbalance (QCM) calibrated with an Ambios XP-200 surface profilometer. All annealing was done on a hot plate under an N$_2$ atmosphere. P3HT was dissolved in chlorobenzene at 1mg:ml for "low concentration" and 10mg:ml for "high concentration" (the latter was used unless stated) and heating at 70°C for 1 hour whilst stirring. This was then deposited onto cells by dynamic spin coating at 1000 rpm for 10 seconds and 4000 rpm for 30 seconds. Gold contacts were deposited by thermal evaporation with an active area of 0.1 cm^2.

Current-voltage (J-V) measurements were done under AM1.5 illumination by a TS Space Systems solar simulator. External quantum efficiency measurements were done using a Bentham PVE300 characterization system. X-ray diffraction (XRD) measurements were performed with a Rigaku Smartlab X-ray diffractometer with a rotating copper anode under ambient conditions. θ-2θ scans were carried out with monochromated incident radiation (Cu Kα$_1$) between 20° and 80° in parallel beam geometry.

3.   Results & Discussion

Evaporated Se films as-deposited are usually amorphous and have low optical absorption. Post-growth annealing is required to recrystallize the film from amorphous "a-Se" to trigonal "t-Se" [18] which decreases the band gap and increases optical absorption. The optimal annealing conditions for best performance, defined by highest device efficiency, were found to be 200°C for 2 minutes following a range of testing between 160-220°C and 1-10 minutes (further information is shown in Fig. S1 and S2). As in previous work [10-13] we found a thin layer of Te to be essential to aid adhesion between the window layer and Se layer during the post-growth anneal. Figure 1a shows optical transmission curves for identical samples of 200nm Se on FTO/TiO$_2$ with and without a 3nm Te wetting layer following a post-growth anneal at 200°C for 2 minutes, with the inset showing images of the samples before and after annealing. It is clear that there is very little absorption in the ideal region for PV devices in the sample without a Te wetting layer. Fig. 1b and 1c provide insight into the effect of the Te wetting layer during the post-growth anneal; without Te the Se layer appears to form discrete islands (c) rather than a cohesive film (b) which severely impacts its absorption capability as demonstrated in Fig. 1a inset. Figure 1d shows Tauc plots calculated from optical spectroscopy measurements for both as-grown and annealed 200 nm Se films on FTO-coated glass. The band gap of the film decreases from 2.06 eV to 1.67 eV following annealing, with the values being significantly below the 2.17 eV and 1.95 eV band gap reported by Todorov et al. [17]. Trigonal selenium (t-Se) has been reported to have a band gap as low as 1.60 eV [19] hence this may be the cause of the smaller band gap for the annealed sample and may be beneficial as the lower band gap is much more suitable for an absorber under AM1.5 illumination. It is also possible that the lower values for the as-deposited sample are due to partial Se recrystallization during deposition caused by heat from the evaporation source inducing low temperature annealing of the substrate. This is evident from the XRD spectra shown in Fig. 1e which compares as-deposited and annealed films; the as-deposited material shows weak (110), (200) and (210) peaks rather than fully amorphous character. The annealed spectra shows the main reflections typical of t-Se phase at 23.50° (100), 29.70° (101), 41.36° (110), 45.40° (111) and 51.76° (201) [18], implying significant recrystallization and a strong (100) preferred orientation.
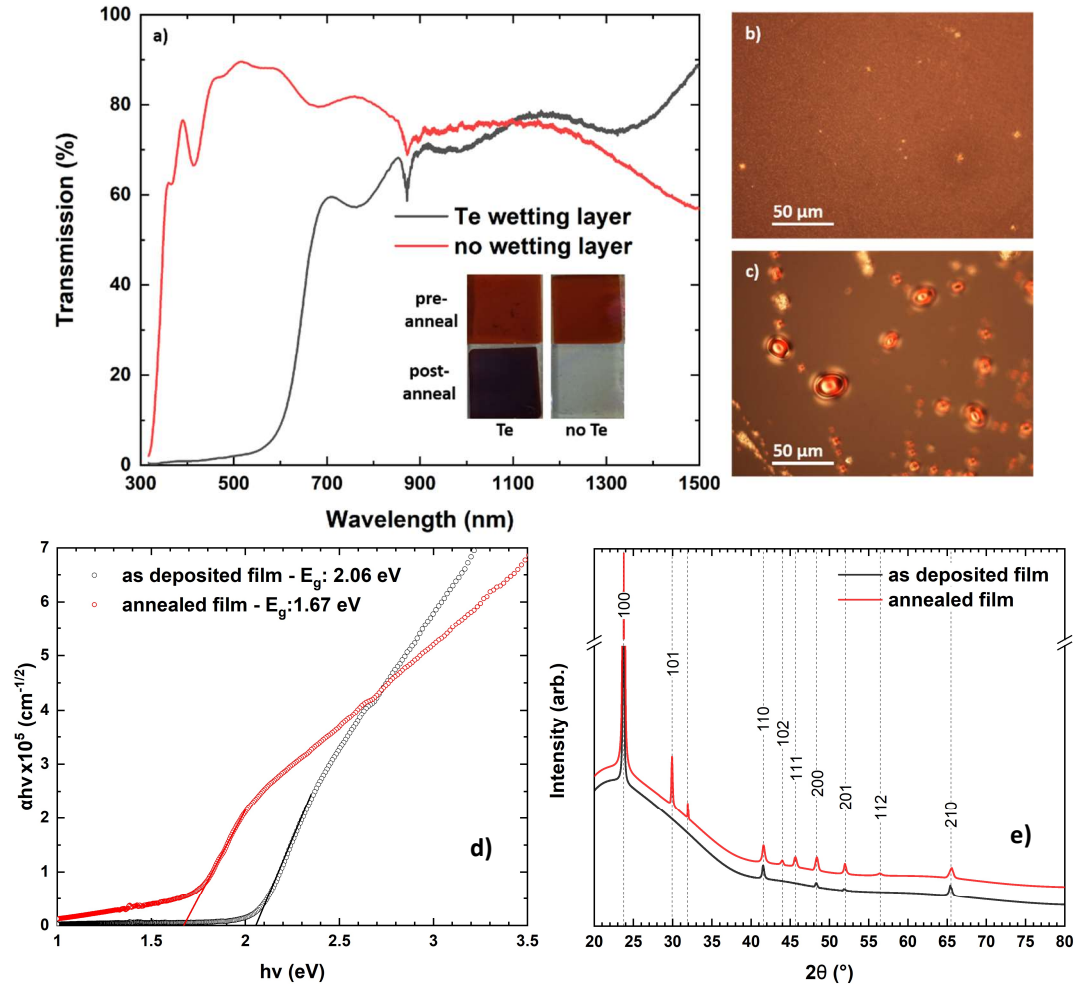
Fig. 1: Effect of Te wetting layer and post-growth annealing on evaporated Se films. a) Optical transmission data for 200nm Se films on TiO_2 following a post-growth anneal at 200°C for 2 minutes, with and without a 3nm Te wetting layer. 50x optical microscope images showing post-growth annealed films with (a) and without (b) a 3nm Te wetting layer. Effects of annealing with d) Tauc plots showing the shift in band gap and d) XRD spectra showing the increase in crystallinity.
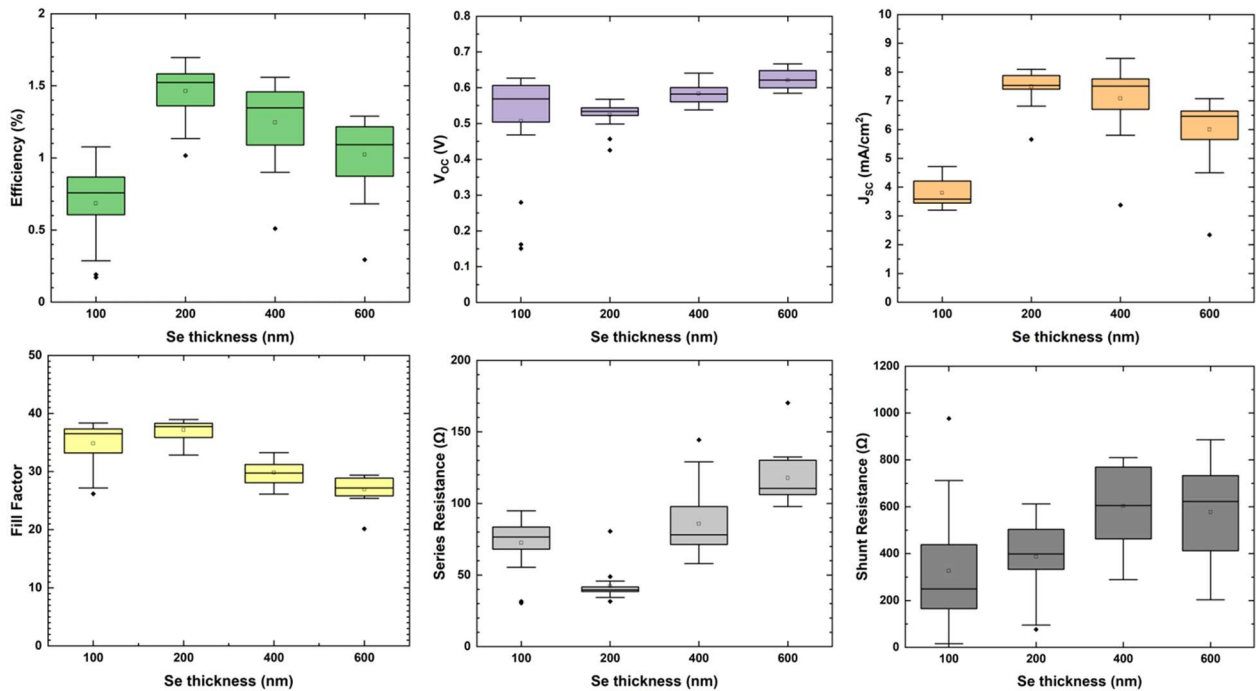

Fig. 2: Device performance parameters calculated from JV data for FTO/TiO_2/Se/P3HT/Au devices with different Se absorber thicknesses.

Figure 2 shows solar cell performance parameters for devices with the structure FTO/TiO_2/Se/P3HT/Au with a range (100-600 nm) of Se absorber thickness, all having had a 200°C 2 minute post-deposition anneal. A 3nm Te wetting layer was included on-

top of the TiO$_2$ layer prior to Se deposition as initial testing determined it essential to achieving good Se coverage. Without the inclusion of this layer Se formed discrete islands with poor coverage and low optical absorption [12]. The highest performing absorber thickness was found to be 200 nm, attaining a peak performance of 1.70% efficiency, 0.57 V V_{OC}, 8.09 mA/cm^2 J_{SC} and 39% fill factor. Our J_{SC} values are comparable to that of the best performing devices in other work [17, 18], however our V_{OC} values are lower, likely due to issues at the interface as discussed further in Fig. 3b. With thicknesses above 200 nm J_{SC} began to decrease whereas V_{OC} stayed fairly constant, this being in agreement with work by Liu *et al.* [16]. To achieve maximum performance a balance must seemingly be struck between the resistance of thicker layers and the lower absorption of thinner layers. Our optimised absorber thickness lies between the ultra-thin 100 nm layer used by Todorov *et al.* and the micron thick layer used by Kanatzidis *et al.* This demonstrates that Se thickness must be carefully optimised for changes in device architecture or Se deposition process. Alteration of underlayers will significantly impact the growth and processing of the Se layer, with the final grain structure of the material playing a key role in determining the carrier transport properties and thereby resistivity. This factor could potentially be used as an avenue to tune the Se layer properties and subsequently device performance.
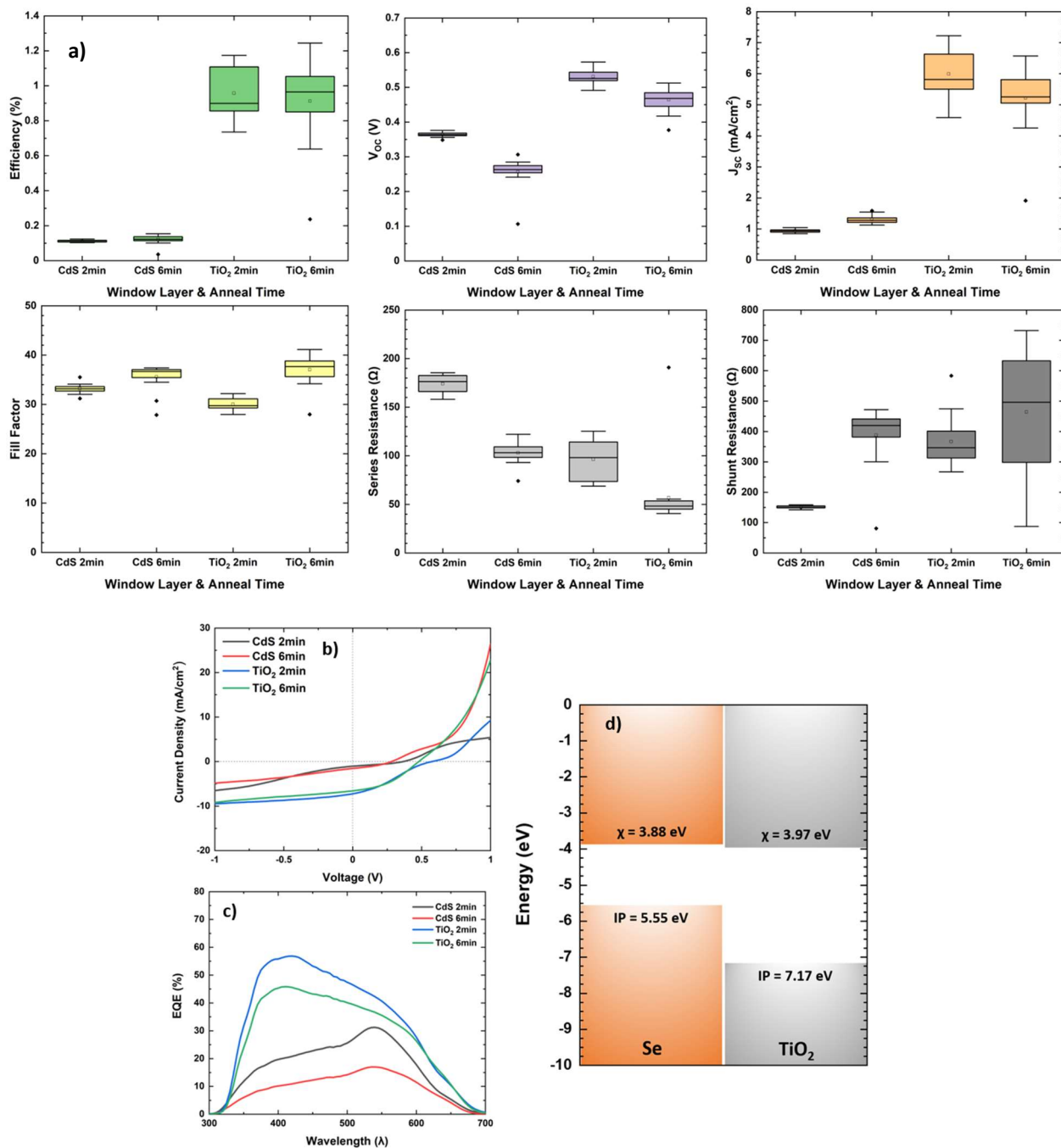

Fig. 3: a) Device performance parameters calculated from JV data for Se devices with either TiO$_2$ or CdS window layers and 2 or 6 minutes post-deposition Se anneal with b) JV curves and c) EQE curves for the highest efficiency contacts. d) Shows the natural band alignment for TiO$_2$/Se.

Having established a suitable 200 nm Se layer thickness, the impact of the device window layer was assessed by replacing TiO_2 with CdS in the same structure, allowing a direct comparison between the performance of the two window layers. Devices also were annealed post-deposition at 200°C for either 2 or 6 minutes, in an attempt to separate the influence of the window layer from the post-growth processing influence. Fig. 3a shows device performance parameters for the four cell types compared, along with JV (Fig. 3b) and EQE (Fig. 3c) curves for the best performing contacts from each device. Devices with a TiO_2 window layer performed similarly to prior devices in Fig. 2 and outperformed the CdS devices irrespective of annealing time. TiO_2 devices with the shorter 2 minute anneal time had increased J_{SC} and V_{OC}, which was in part attributed to some observed delamination of the Se layers for the longer 6 minute annealing time. Devices with CdS performed poorly, with very low efficiency and particularly low J_{SC}; for both annealing conditions, possibly due a large conduction band offset (0.39 eV) between CdS and Se [20].

However illuminated JV curves in Fig. 3b show s-shaped curves present in both devices with CdS and TiO_2 window layers, which could be due to several reasons. Typically, s-shaped curves result from charge accumulation at the interface and in literature this is reported as being attributable to either misalignment of the conduction band or poor conductivity. Whilst poor band alignment is a possibility, given prior reports of functioning devices with TiO_2 it seems unlikely the TiO_2 itself is the cause. We can also discount the TiO_2 layer having poor conductivity as the process is established for other cell platforms such as our Sb_2Se_3 process [21]. Fig. 3d shows the natural band alignments of Se and TiO_2 with values taken from the literature for Se [22] and from our own measurements for TiO_2 [23]. Whilst the natural band alignment does not justify the pronounced s-shaped curve, the band alignment could vary due a number of factors. Firstly the band gap of the TiO_2 has been reported between 3.2 eV [24] and 3.5 eV [25], and secondly the addition of Te to Se is known to reduce the band gap [22], both of these factors could potentially cause a barrier at the TiO_2/Se interface. However the most likely possibility is a thin poor quality layer existing at the interface, either due to a lack of type conversion during annealing or potential damage to the layers. This lowers the carrier transport properties in the near interface region causing charge accumulation and hence the s-shape curve.

The EQE measurements in Figure 3c offer additional insight for the low J_{SC} values. For the TiO_2 device, although collection is lower than ideal across the absorption range (<60%), collection peaks near the TiO_2 band edge at ~385 nm [24] and shows good collection until the Se band edge. For the CdS device parasitic absorption from the CdS layer is observed up to 525 nm [26], narrowing the peak absorption region of Se due to its high band gap being relatively close to that of CdS. It is worth noting that even factoring in the parasitic absorption for the CdS the overall collection for the CdS device is lower meaning both the parasitic absorption and poor band alignment are likely responsible for the extremely low J_{SC} values obtained.
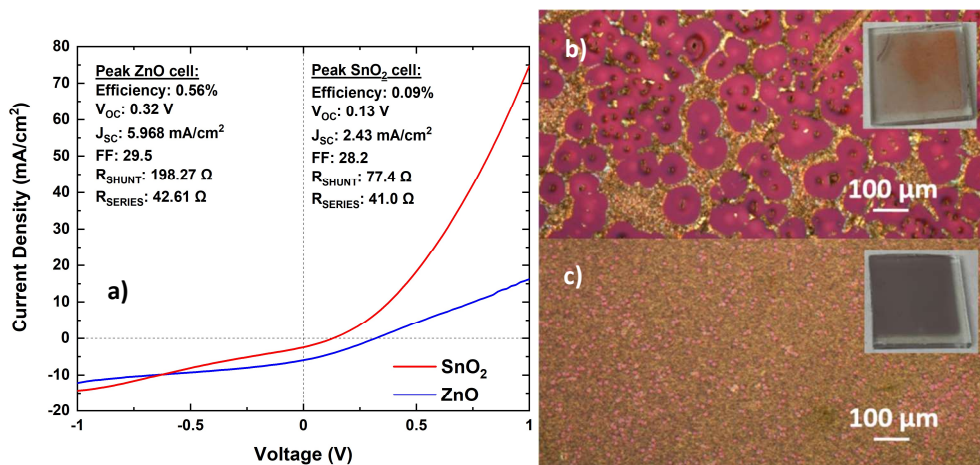

Fig. 4: a) Illuminated JV curves of FTO/window layer/Se/P3HT/Au devices with ZnO or SnO_2 window layers. b) 10x image of Te/CdSe/Se film following post-deposition anneal c) 10x image of Te/Se film following identical post-deposition anneal.

CdS and TiO_2 are arguably the two most widely employed window layers for thin film PV but there are a number of feasible alternatives that can be tested. Using the same device structure; SnO_2, ZnO and CdSe were also explored as potential window layers as these have been reported as successful options in other thin film PV technologies [27-29]. Devices with an undoped 100 nm SnO_2 buffer layer showed very weak performance, with low V_{OC}, low R_{SH} and high R_S via JV data in Figure 4a. A 200 nm ZnO layer showed more promise as a window layer, with improved V_{OC} compared to SnO_2 but performance was lower than that of TiO_2, due to high R_S, and the s-shaped JV curves still persisted so this route was not explored in further detail.

Full devices were unable to be produced using CdSe window layers as it was found that Se failed to effectively adhere to a 5 nm sputtered layer during the post-deposition anneal. Figure 4b and 4c show identical Se films deposited on FTO-coated glass post-anneal at 10x with CdSe (4b) and without CdSe (4c). For the sample including the CdSe layer the Se film appears to recrystallize into large discrete grains before re-evaporating from the substrate entirely following further annealing. Ito *et al.* reported a similar structure but did not note any particular Se adhesion issues [13], hence the lack of adhesion here is somewhat unexpected. One possible reason for this discrepancy is in the difference in surface morphology between the sputtered CdSe used

here and the thermally evaporated CdSe used by Ito *et al.* Thermally evaporated CdSe has been reported to have a hexagonal structure up to substrate temperatures of 350°C [30] whereas sputtered CdSe is reported to have a cubic structure when deposited at a substrate temperature of 200°C [31]. This variation from hexagonal to cubic CdSe seems the most probably cause of the poor adhesion observed here.
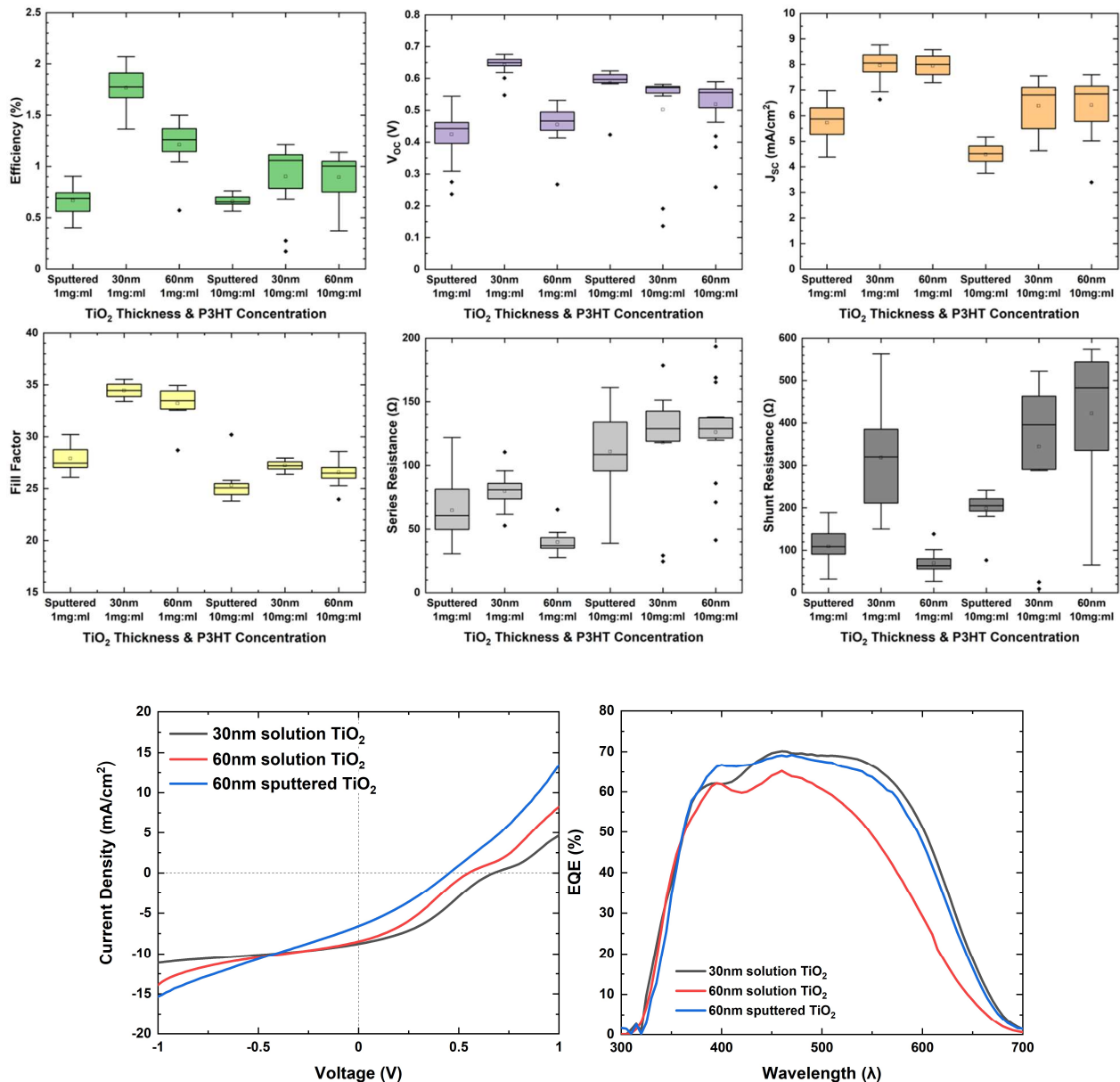

Fig. 5: a) Device performance parameters calculated from JV data for FTO/TiO₂/Se/P3HT/Au with various TiO₂ thicknesses and P3HT concentrations including b) illuminated JV curves and c) EQE spectra for the highest efficiency contacts from 1:1mg:ml P3HT devices.

As no improved window layer compared to TiO₂ was identified, a series of optimization steps were undertaken to improve the s-shaped JV performance. As this is attributable to an interface charge barrier focus was placed on both the front and back interfaces. The TiO₂ layer was adjusted by comparing a 60 nm solution processed TiO₂ layer, a 30 nm solution processed TiO₂ layer and a 60 nm sputtered TiO₂ layer. Sputtered TiO₂ gives a conformal coating to the FTO surface whereas solution processed TiO₂ in-fills the roughness of the FTO leading to a smoother surface. These factors are expected to affect the growth and recrystallization of Se, however any influence they may have over optimal processing conditions has not been investigated in this work. For each TiO₂ window layer we additionally compared cells with either a high concentration (10mg:ml) or low concentration (1mg:ml) of a P3HT hole transport layer, giving 6 cell structures compared in total with device performance parameters as well as JV and EQE curves for the highest performing 1mg:ml P3HT devices shown in Figure 5.

It was found that device performance was predominantly controlled by the nature of the TiO₂ window layer. A thinner 30nm solution processed TiO₂ layer significantly outperformed both the thicker solution process and TiO₂ equivalent, which had particularly low performance. The thinner TiO₂ device had noticeably higher V_{OC} up to 0.68 V and 2.07% efficiency, but there was

still significant s-shape behavior noticeable in the JV curves of even the best devices. Whilst high concentration P3HT generally resulted in higher V_{OC} but lower J_{SC} compared to its low concentration counterpart as shown in Figure 5a, this is likely due to a thicker layer causing an increase in series resistance but improving pinhole blocking and overall device performance was reduced through the use of the higher concentration. There was also no evidence of it improving the s-shape curve behavior noted in the JV analysis.

Overall, for all structures compared device performance is limited by V_{OC} compared to other studies which report values up to 0.86 V with similar structures [17], however our J_{SC} values are comparable to the best performing devices in other studies as previously mentioned. This lower V_{OC} could be in part due to the lower band gap of our Se absorber (Figure 1a) but is also likely due to the presence of an interfacial barrier caused by sub-optimal band alignment and an offset between TiO_2 and Se. This could potentially be rectified by altering the band positions of TiO_2, which has been demonstrated with the introduction of a zinc halide surface treatment [28]. Alternatively, a window layer with a more suitable band alignment to TiO_2 could be identified, for example oxygenated CdS (CdS:O) is known to increase the optical band gap and shift the CBM upwards compared to CdS and could offer a solution [20].

4.   Conclusion

In this work we have compared several device aspects in attempt to understand the factors which most control device performance, whilst further optimization of the Se processing and thickness may ultimately benefit device efficiency, identifying and addressing the cause of the interface charge barrier evidenced from s-shaped JV curves is the primary route to improved performance. We found a 200 nm thick Se absorber layer yielded the highest efficiency device of 2.1%, thicker than the prior champion device absorber thickness of 100 nm but still significantly below the majority of prior work. Our inference from this is that the optimal absorber thickness is likely highly variable, dependent on not only the deposition and post-growth processing but also on the device partner layers used. The primary limiting factor of device performance was determined to be the presence of an interfacial charge barrier, evidence by s-shaped JV curves. TiO_2 was the best window layer trialed, but performance was still limited. Other window layers trialed in this work included CdS, SnO_2, ZnO and CdSe all of which produced worse performance, often due to poor band alignment with Se or adhesion issues in the case of CdSe. Overcoming this extraction barrier will greatly improve performance of this device platform as fill factor in particular is significantly compromised. It is believed that the extraction barrier results from band misalignment rather than the TiO_2 being overly resistive, hence future work may focus on shifting TiO_2 band positions with a halide treatment [32] or identifying an alternative window layer for Se with better alignment.

5.   References

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