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Design and Characterization of Depleted Monolithic Active Pixel Sensors within the RD50 Collaboration

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Design and Characterization of Depleted Monolithic Active Pixel Sensors within the RD50 Collaboration

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Abstract

The CERN RD50 CMOS working group is designing and characterizing depleted monolithic active pixel sensors (DMAPS) for use in high radiation environments fabricated in the LFoundry 150 nm HV-CMOS process. The first iteration of this chip, RD50-MPW1, suffered from high leakage current, low breakdown voltage and crosstalk. In order to mitigate these shortcomings, an improved version with improved pixel geometry was designed. The RD50-MPW2 integrates a matrix of 8x8 pixels with analog front-end, but no digital readout. It was delivered in early 2020 and characterized within lab-measurements, an irradiation campaign and test beams. To read out the chips the Caribou DAQ system is used with a custom chipboard as well as specific firmware and software modules. A third iteration of the chip, the RD50-MPW3, has been submitted to LFoundry in December 2021 and is expected to be delivered in May 2022. It will keep the well working analog part of its predecessor, completed by an in-pixel digital logic and an optimized peripheral readout for effective pixel configuration and fast serial data transmission. The chip will comprise a matrix of 64x64 pixels arranged in 32 double-columns. We will present an overview of the RD50 HV-

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[1] Given his role as Guest Editor, Thomas Bergauer had no involvement in the peer-review of this article and has no access to information regarding its peer-review. Full responsibility for the editorial process for this article was delegated to the other guest editors of this volume.

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Key words: CERN-RD50, depleted monolithic active pixel sensor, future hadron colliders, high voltage-CMOS technology, high voltage pixel detector, monolithic CMOS detector

1. Introduction

The RD50-MPW series comprises three DMAPS designed in a high voltage CMOS (HV-CMOS) process, with RD50-MPW3 being the latest developed chip. All of them are fabricated in the 150 nm HV-CMOS process by LFoundry S.r.l.[2] and target a use in harsh radiation environments with high spatial granularity. The first part of the paper shows relevant results of RD50-MPW2 which will be repeated with its successor, RD50-MPW3. The second part deals with the design of RD50-MPW3. The focus is put on digital data processing inside the chip and is concluded by a section covering readout and trigger ideas, which are currently developed and tested. Detailed information about the motivation for the RD50-MPW series and additional results can be found in [1].

2. RD50-MPW2 Measurements

RD50-MPW2 has been well characterised enough to suit our needs, including sensor tests such as IV and CV curves, timing measurements performed as eTCT studies and radiation tests done with a radioactive Sr90 source. Moreover, test beams have been conducted at the Rutherford Cancer Center and MedAustron, a center for ion therapy and research in Wiener Neustadt, Austria. This section focuses on measurements at MedAustron, as those results are the baseline for digital readout developments of the successor chip RD50-MPW3. An introduction to the facility as well as the available beam settings

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can be found in [2].

2.1. Analog Behaviour of the Chip

The aim of the initial test beams was to evaluate the performance of the testbeam DAQ, newly developed for the RD50-MPW chips. Figure 1 shows the simulated pulse shapes of a switched-reset pixel flavor, which discharges the preamplifier almost instantly leading to a pulse width independent from deposited charge which allows evaluating the DAQ. Details about analog pixel design and pixel flavours can be found in [3]. For measuring the pulse width in test beams, the digital signal after the comparator in the pixel is captured with an ADC on the readout PCB. The results are plotted for two energies in figure 2. In both cases, the measured pulse width is about 33 ns and thus matches very well with the simulation.

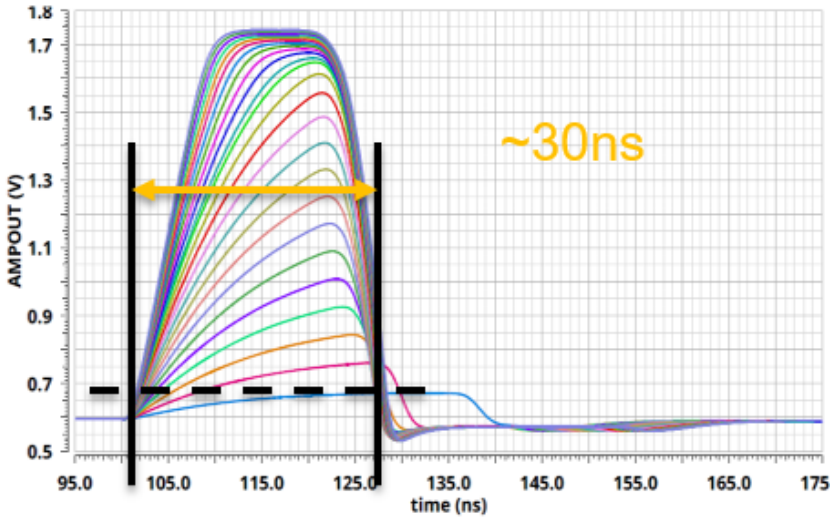

Figure 1: Simulation of the analog output after the preamplifier. Different colors represent different deposited charges ranged from 1 ke^- to 25 ke^-. Instead of measuring the analog output directly, the pulse is discriminated and a digital output of the same length is measured. The dashed line represents the chosen discriminator threshold. For signals below the discriminator threshold the switched feedback is not activated and thus the pulse is wider (light blue curve).

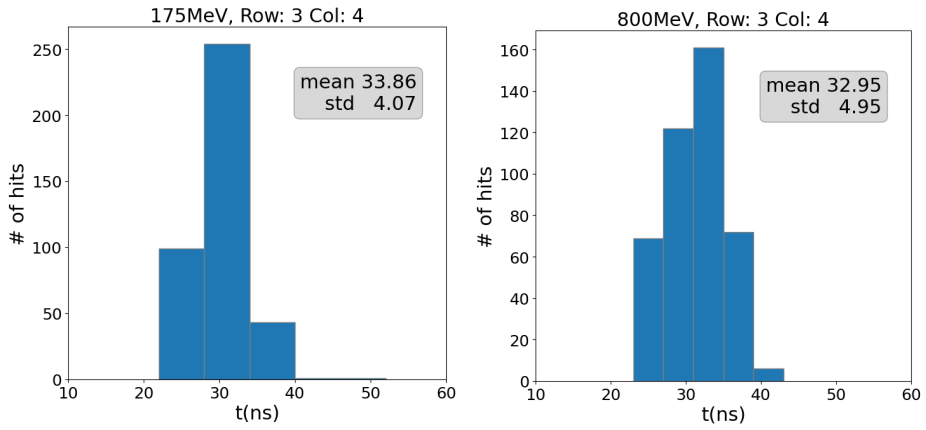

Figure 2: Measured pulse widths of the digital output for 175 MeV (left) and 800 MeV(right).

2.2. Digital Readout Integration

Further test beam campaigns were performed to get familiar with digital data acquisition, triggering and synchronization. Thus, a firmware upgrade capable of receiving a trigger was written as described in [4]. At these test beams it has been confirmed that the synchronization between the RD50-MPW2 readout and a telescope made from double-sided silicon strip detectors (DSSD) [5] including the upgraded firmware is working. Figure 3 shows the DSSD telescope with the RD50-MPW2 chip mounted in the middle. Synchronization of the two systems was achieved by an AIDA trigger logic unit (AIDA-TLU) [6]. Moreover, reconstruction of tracks including hits from the device under test (DUT) is also possible, but statistics is rather low, since for RD50-MPW2 only one pixel at a time can be read out, while the reference sensor planes of the telescope are much larger (60 µm × 60 µm pixel size versus 50 mm × 25 mm telescope plane). The result of a so-called window scan is shown in figure 4. In this plot, pixel 3/4 (row/column) is read out and used as trigger source. All other pixels are also active, but not read out. Due to charge sharing, it is expected to measure a portion of the signal from surrounding pixels as well. Thus, the data set used for this analysis are all hits of pixel 3/4 and hits in neighboring pixels, which also produce a signal in pixel 3/4. From this data set, tracks are reconstructed

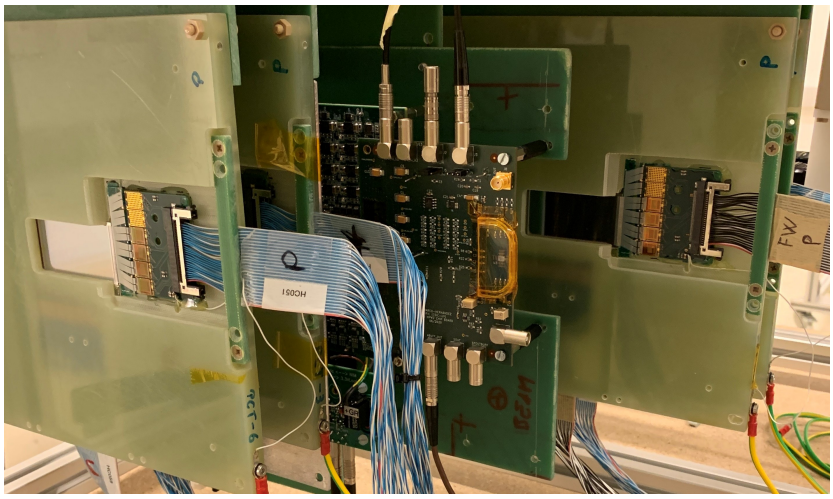

Figure 3: Picture of the setup for tracking studies where RD50-MPW2 is mounted in the middle of 4 telescope planes.

using hits in the DSSD telescope only. Those tracks are then extrapolated to positions on the RD50-MPW2 pixel matrix. Thereafter, for every pixel, a region of interest (ROI) is defined around the pixel, which covers the pixel and half of the neighboring pixels. Only if the extrapolated hit is within the ROI, it is counted in figure 4. In this figure, the ROI for pixel 3/5 is shown as an example (blue square), to illustrate this analysis. The last step is repeated for each pixel. The result of this analysis shows a convolution of multiple effects: Pixels near the active pixel have a higher count of tracks in the ROI due to charge sharing and overlapping ROI with the active pixel. Pixels further away from the measured pixel show no hits which proves that real hits are resulting from particles instead of noise and the reconstruction is working. The results have to be taken with care due to the error of the reconstructed tracks and the very low statistics. Details on this study can be found in [7].

A full data acquisition and reconstruction flow has been demonstrated with the RD50-MPW2 chip. This implementation of the digital readout was used as baseline for designing the digital readout of RD50-MPW3 as described in the next two sections.

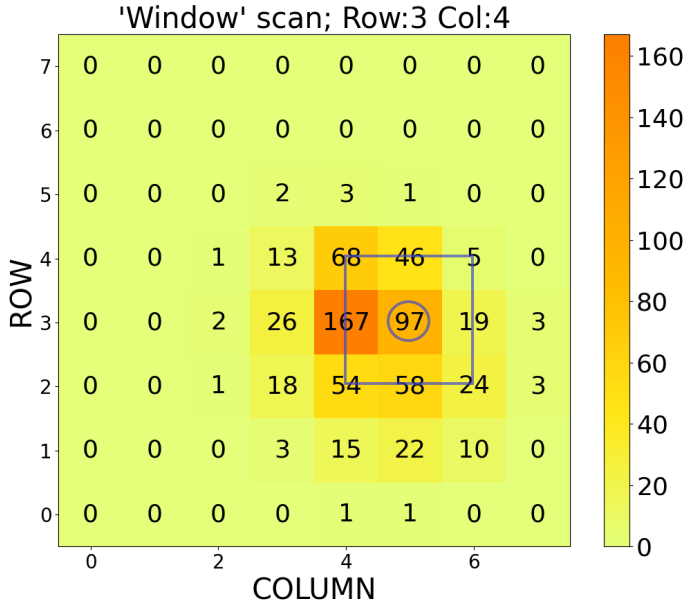

Figure 4: Window-Scan with active pixel row 3, column 4. As an example, the region of interest for pixel row 3 column 5 is shown.

3. Overview of RD50-MPW3 Design

3.1. Pixel Matrix

RD50-MPW3 consists of a pixel matrix of 64 x 64 pixels arranged in 32 double columns (DCOLs) with 128 pixels each. All pixels of the DCOL share the same digital busses to minimize routing congestion. Via these busses, each pixel receives a global 8-bit time-stamp and returns 8-bit leading edge and 8-bit trailing edge as well as 8-bit pixel address. For configuration of the in-pixel registers, all pixels are connected to form a single bit shift register. To determine which of the eight pixel-internal registers is written, another eight shared digital data lines are implemented. Together with 8 control and monitoring signal lines, there are 48 signals in each DCOL, not counting power lines. Details about the pixel electronics as well as an overview of the whole chip can be found in [1].

3.2. Digital Periphery

The focus of this section is the digital periphery, as this part determines how the chip is read out. A schematic overview can be seen in figure 5. It includes a so-called end of column (EOC) circuit per DCOL which is responsible for reading out the pixel matrix and puts data into a 32 words deep buffer. The control unit (CU) reads out these EOC buffers and pushes data into a 128 words deep transmission FIFO. The FIFO is attached to the transmission unit (TX Unit) which adds start of frame and end of frame words, performs 8bit/10bit encoding, serializes data and sends it over a single differential pair to the off-chip electronics. Furthermore, the digital periphery includes a gray-encoded time-stamp counter (TS) which provides an 8-bit time-stamp to each DCOL. A clock and reset unit implements a clock divider, which divides a fast external clock of 640 MHz (CLK640) to a slow clock of 40 MHz (CLK40) which drives most of the digital electronics in the periphery. An I2C to wishbone module is used to convert external I2C control signals to internal used wishbone control signals.

3.3. Transmission Unit and Serializer

As an example for the digital design implementation, the main functionality of the TX Unit and the serializer are discussed in this section. As shown in figure 6, it receives data from three different type of registers with 32-bit each. These bits are encoded using 8bit/10bit encoding which results in 40-bit wide data. In order to reach a 640 MHz data stream at the output, data needs to be provided every 40 clock cycles which corresponds to 16 MHz. However, such a clock frequency is not available and the chip does not have a phase locked loop (PLL) which is normally used in order to generate arbitrary frequencies. Hence, registers are driven by the 40 MHz clock, which leads to a clock domain crossing (CDC) in the transmission unit. A special enable signal (EN) is generated from the fast 640 MHz clock and used to enable all the registers in the TX Unit. As illustrated in figure 7, it is chosen such, that exactly one rising edge of the 40 MHz clock is within one serialization period. Due to the periodicity of the

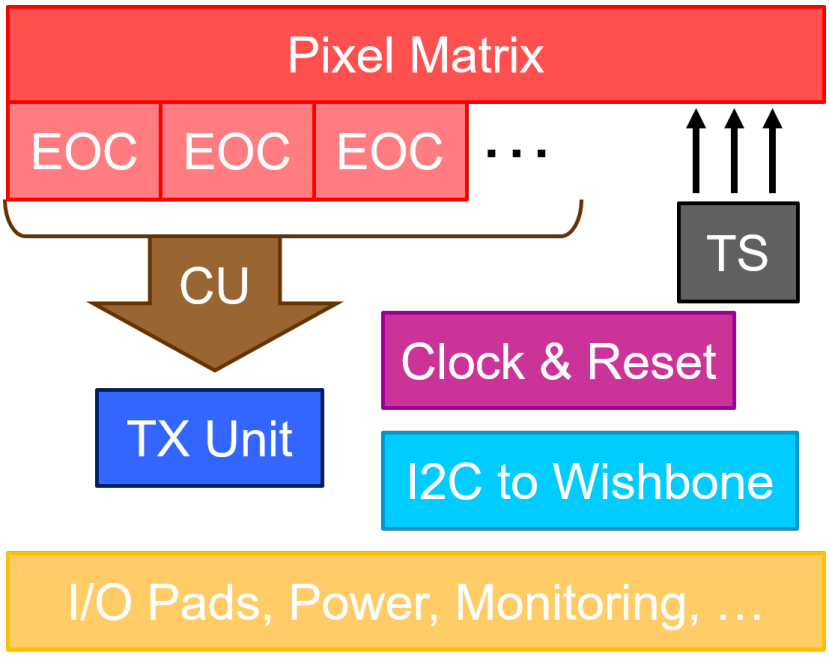

Figure 5: Schematic of the digital periphery of RD50-MPW3

signals, there are only two different patterns in this particular case. Nevertheless, special attention must be given to the timing and phase shift between the two clocks during clock tree design, so there is enough time to encode the data. Thus, at least 3 clock cycles of CLK640 are needed between the relevant rising edge of CLK40 and the falling edge of the EN signal.

4. RD50-MPW3 Readout

The design of the data acquisition (DAQ) focuses on the usage of the chip during test beams. It is based on the Caribou DAQ system [8] which has already been used for RD50-MPW2. Caribou consists of a commercial SoC board (Xilinx Zynq ZC706), the control and readout (CaR) board and a custom carrier board for the sensor. Synchronization with other detectors already played a role during the on-chip design of the digital periphery, where some additional signals (such as a time-stamp overflow output) were implemented. The data

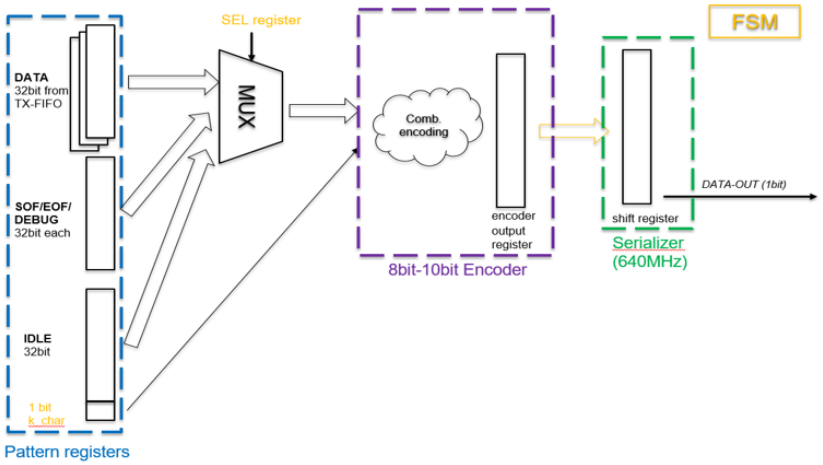

Figure 6: Schematic showing the register structure of the transmission unit. All registers are driven by CLK40 and enabled with signal EN, which are given in figure7

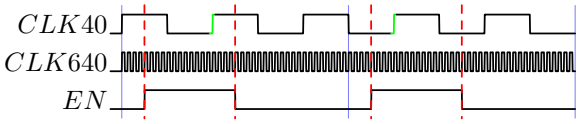

Figure 7: Timing diagram to illustrate the enable signal EN. Blue vertical lines represent one serialization period (40 bits at 640 MHz), CLK40 is driving all registers before the serializer and EN is the signal which enables those. At the green edges of CLK40, data is stored at the output registers of the encoder. CLK640 is the fast clock, which pushes out data from the serializer.

acquisition firmware and readout software continue this principle and focus on test beams as well. As depicted in figure 8, data flows on a single differential line directly into the FPGA where it is buffered and forwarded to two data paths. One of them is a fast data path which gets all the data and is used for storing data at high speed. The second is a slow data path which receives only a configurable percentage of data which is sent over a different interface for monitoring purposes.

The main goal of the fast path is to transmit and store data as fast as possible. Thus, the user datagram protocol (UDP) is implemented in the FPGA firmware, which sends the data over a dedicated, direct UDP link to the receiving

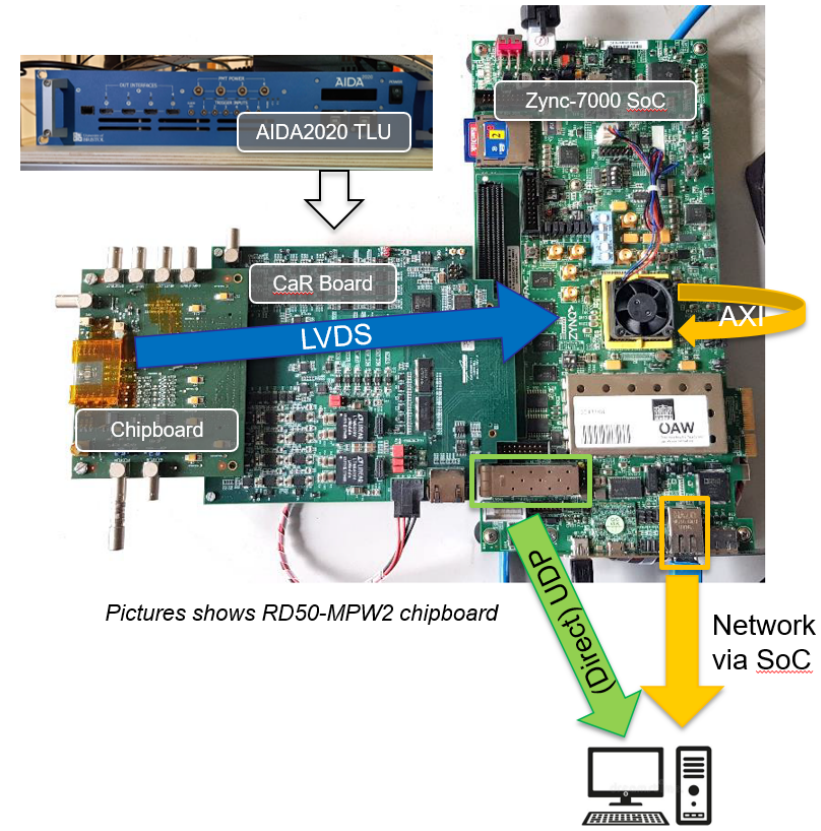

Figure 8: RD50-MPW3 readout electronics consisting of the Caribou system and the AIDA2020 TLU[6]. Since the RD50-MPW3 carrier board is currently under development, the depicted board is still from RD50-MPW2.

PC, which unpacks and stores the data to disk. Therefore the small form-factor pluggable (SFP) interface of the Xilinx Zynq board in combination with a gigabit LAN-transceiver is used, which later can be replaced by optical SFP or SFP+ transceiver to further increase the data transmission rate. With the current setup, around 800 Mb/s can be transmitted. Data acquisition is implemented within the EUDAQ2 framework[9] for synchronization with other detectors and easy integration into the tracking framework corryvreckan [10].

A configurable percentage of the data is sent over the AXI Bus of the SoC to the CPU. It is transmitted over TCP to the receiving PC on a separate

connection. As this is using the single core CPU from the SoC system, this path is rather slow and is used for control and data monitoring purposes only. An EUDAQ2 monitor is implemented to view live data.

5. Conclusion and Outlook

RD50-MPW2 was an intermediate step from which many lessons where learned for the design of its successor, the RD50-MPW3. This new chip comprises the well working analog part from RD50-MPW2 and a completely new digital readout, capable of integration into bigger detector systems. DAQ development including hardware, firmware and software already started in order to be ready to start testing the chip as soon as it is delivered. The submission of RD50-MPW3 was in December 2021 and delivery is expected around May 2022. As a first step, the concepts presented in this paper will be used in order to integrate the chip as DUT in a telescope and measure the typical parameters for tracking performance. As a second step, we are aiming to build a telescope demonstrator with RD50-MPW3. As the design of RD50-MPW3 focuses on high data rate, we expect a readout rate in the order of 10 MHz for single tracks, not counting losses due to cuts during reconstruction (which cannot be determined yet).

Acknowledgements

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URL https://doi.org/10.1088/1748-0221/16/03/p03008

Answer letter:

Thanks you for the feedback, please find the answers to the raised questions below:

Figure 1: What does the broken line in the figure represent?
You claim the pulse width being independent from the deposited charge. Obviously, from the figure there is a lower limit. You should comment on this limit (even if irrelevant for final operation)
Answer: The broken line represent the discriminator threshold, as the analog signal is not measured directly, but after discrimination. The caption of the figure has been updated, to makes this clear.
Regarding your question about the lower limit, we assume you mean the wider pulse for very low signals.
This is because for signals below the discriminator threshold the switched feedback of the integrating amplifier is not activated and thus the pulse is not shortened and has its natural length. We added a note to the caption.

There is no reference to Figure 3 in the text. Please add one.
Answer: A reference including a short description has been added to section 2.2

Typos:
line 30: an ADC
line 61: and the reconstruction is working
line 100: add "/" to 8bit/10 bit encoding - to be consistent with line 87
Caption figure 6: enabled
Line 136: increase the data transmission
Answer: All corrected :)

Very last sentence, line 157: what does (pre-track fit losses) means here?
Answer: The readout rate of tracks is hard to predict as it depends on the clustersize, which we cannot measure with RD50-MPW2 (by design). The 10MHz correspond to a clustersize of 3 pixels, thus this is the rate of actual hits which should be handled by the DAQ. As the analysis framework has the usual cuts (Chi2, track out of region of interested, ...) the number can be only quoted before these rate losses. The wording has been changed, in order make this clear.