Simple Symmetric Switched Inductor High Step-Down Converter

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Abstract

The voltage gain of a traditional buck converter is finite due to the high voltage across the semiconductor and reduced efficiency. A non-isolated high step-down DC-DC converter based on symmetric switched inductors is proposed in this paper. The connection of inductors in series or in parallel is controlled by switches to improve the conversion ratio. The converter has many beneficial characteristics such as high step-down, reduced voltage stresses, and high efficiency. Moreover, it can realize voltage balance on the switches. The voltage on the switch does not oscillate and the loss of the switches is reduced. Therefore, the efficiency of the whole topology is improved. This paper discusses the operation principle, modes analysis, voltage gain analysis, voltage stress analysis, output ripple analysis, loss analysis, comparative analysis and design considerations. The correctness of the theoretical analysis of the proposed converter is verified by a laboratory prototype, and its peak efficiency reaches 96.5%.

Keywords: High efficiency, High step-down converter, Low voltage stress, Symmetrical switched inductor

1 Introduction

In recent years, low power step down DC-DC converters have become more and more widely used i n a wide variety of applications including battery chargers, LED drivers, and communication system [1-3]. The conventional buck circuit is simple in structure and mature in technology. Ideally, the traditional Buck converter can achieve a high step-down conversion by decreasing the duty cycle. However, due to the non-ideality of Buck converters and their inherent resistance, their switching and conduction power losses are high while the duty cycle is very small, which affects the conversion ratio. In addition, the stress of the power devices increase. Therefore, the conventional Buck converter is not applicable for high step-down occasions. A great many researchers have studied and optimized the high step-down converter topology to improve its voltage gain [4-23].

These converters mainly include isolated converters and non-isolated converter. Isolated converters such as forward [4], flyback [5], and full bridge [6] can easily achieve a high step-down ratio. However, for low power applications, isolated topologies suffer from high switching loss, large volume, and increased cost due to the existence of a transformer.

Non-isolated high step-down converters can be divided into a number of different types, including cascading, coupled inductors, gain multiplication cell, switched capacitor, series capacitor, interleaving, switched inductor, and so on. Cascade converters [7-9] accomplish a high step-down by cascading multiple converters. However, the cascade step-down converter topology is excessively complex, which increases both the cost and the power loss. In addition, it experiences high voltage stress across the semiconductor devices. The coupled inductor converter [10,11] is a common high step-down converter. This converter can achieve a high step down by increasing the number of windings turns of the coupled inductor. However, the leakage inductor of the converter leads to a pulsating current and voltage spikes on the semiconductor device. In [12,13], a clamping circuit is added to the converter to assimilate the energy in the leakage inductor. However, it limits the duty cycle extension, and the problem of pulsating output current remains unsolved. A series of voltage multiplier cells [14-16] were designed to achieve a high step-down. However, they need more circuit components and have high voltage stress on devices. Converters based on the switched capacitor [17-19] have been proposed. These converters can realize a

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high step-down. However, they have more components and higher voltage stress. The interleaved technique [20,21] can diminish current ripple and provide current sharing between various components. However, despite increasing the number of elements in the converter, the high voltage stress and voltage gain do not change. Switched inductor high step-down converters [22,23], which have simple structure, can provide a high step-down. However, in actual situations they have high voltage stress across the switches. It is easy to resonate between the switch junction capacitor and the inductor, which may cause voltage oscillations on the diodes. The symmetrical structure can reduce the voltage stress on the switch, suppress the resonance, and balance the voltage stress across the switches.

In this paper, a non-isolated high step-down DC-DC converter based on the symmetrical switched inductor is proposed. By controlling the on-off of the switches and changing the types of connection of the inductor (charging in series and discharging in parallel), high step-down conversion can be achieved. The characteristics of the converter are as follows.

1) It has a simpler circuit topology, fewer components, and is more suitable for low power applications.

2) It is a high step-down converter with low voltage stress. The voltage stress on the switches and diodes are low and are approximately equal to half the input voltage.

3) Its symmetrical structure and can realize the voltage balance of the switches. In addition, owing to the equal voltage distribution of the input and output capacitors, capacitors with a lower withstand voltage value can be selected.

The remainder of this paper is arranged as follows. In Section 2, the operation principle and mode analysis of the converter are introduced. Section 3 exhibits an analysis of the performance and a comparison with some other converters in the literature. Design considerations are given in Section 4. In Section 5, experimental verifications of the converter are carried out. Finally, a conclusion is given in Section 6.

2 Operation Principle

A schematic of the symmetric switched inductor high step-down converter proposed in this paper is shown in Fig. 1. It can realize a high step-down by changing the connection mode of two inductors. The proposed converter is made up of two inductors (L_1, L_2), two pairs of capacitors (input capacitors C_{in1}, C_{in2}, and output capacitors C_{o1}, C_{o2}), two active switches (S_1, S_2), and two diodes (D_1, D_2). As for the converter, the switches are driven by two PWM signals with the same frequency, duty cycle, and phase. The circuit topology is symmetric, which can decrease the voltage stresses of the switches and diodes. Depending on the actual situation, the following analysis is divided into the continuous conduction mode (CCM), the discontinuous conduction mode (DCM), and the boundary conduction mode (BCM).

To simplify the analysis, the following assumptions are considered in this circuit.

1) All of the semiconductor devices are considered ideal.

2) In the steady state performance analysis, it can be assumed that all of the capacitors (C_{in1}, C_{in2}, C_{o1}, C_{o2}) are supposed to be sufficiently large and that the voltages are constant.

3) L_1=L_2=L, C_{in1}=C_{in2}, C_{o1}=C_{o2}.

4) The frequency of the switches is constant.

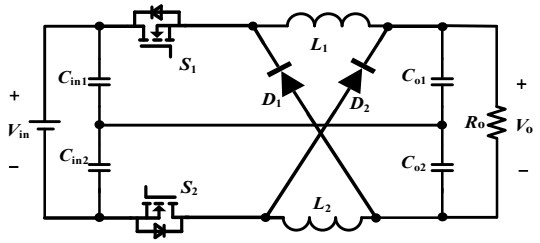


Fig. 1 Schematic diagram of the symmetric switched inductor high step-down converter

2.1 CCM Mode Analysis

Theoretical voltage and current waveforms in the CCM mode are shown in Fig. 2. There are two modes in every switch period. An equivalent circuit diagram of the two operating modes is illustrated in Fig. 3.

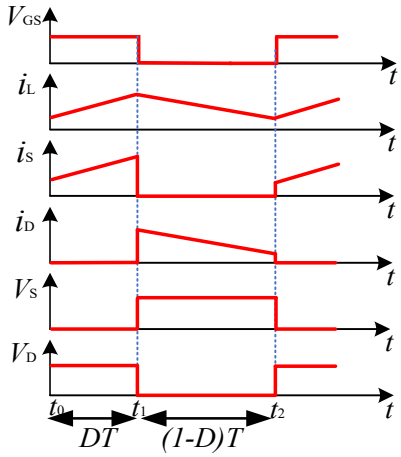


Fig. 2 Voltage and current waveforms in the CCM mode

Mode 1 (t_0~t_1): Fig. 3a shows the equivalent circuit of mode 1. The power switches S_1 and S_2 are simultaneously in the on state. D_1 and D_2 are cut off in reverse, and are in the off state. The inductors L_1, L_2, and the load are charged in series by the power supply through the switches. The voltage of the inductor is constant. According to the formula $V_L = L \cdot di_L / dt$, the current flowing through the inductor increases linearly. In addition, the input is a

constant DC voltage. Thus:

$$i_{\mathrm{Cin1}} = i_{\mathrm{Cin2}} = 0 \tag{1}$$

According to the symmetry of the circuit topology, it can be seen that:

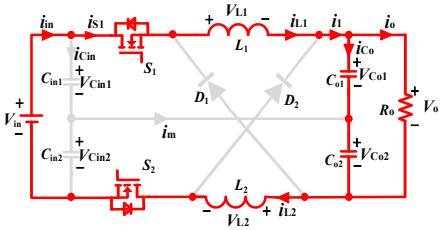
$$\begin{aligned} &i_{\mathrm{m}} = 0 \\ &V_{\mathrm{Cin1}} = V_{\mathrm{Cin2}} = 0.5V_{\mathrm{in}} \\ &V_{\mathrm{Co1}} = V_{\mathrm{Co2}} = 0.5V_{\mathrm{o}} \\ &V_{\mathrm{L1}} = V_{\mathrm{L2}} = V_{\mathrm{L}} = L\frac{di_{\mathrm{L}}}{dt} \end{aligned} \tag{2}$$

Therefore, in this mode, the voltage current equation can be summarized as follows:

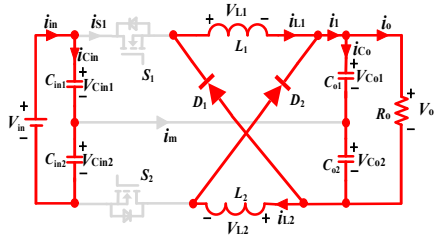
$$\begin{aligned} &V_{\mathrm{in}} = 2V_{\mathrm{L}} + V_{\mathrm{o}} \\ &i_{\mathrm{in}} = i_{\mathrm{S}} = i_{\mathrm{L}} = i_1 \\ &i_1 = i_{\mathrm{o}} + i_{\mathrm{Co}} \end{aligned} \tag{3}$$

Mode 2 (t_1~t_2): Fig. 3b presents the equivalent circuit of this mode. At t_1, S_1 and S_2 are turned off, and D_1 and D_2 are turned on. L_1 and L_2 are discharged in parallel through diodes to provide power for the load. From the equivalent circuit it can be seen that the voltage of the inductor is constant. According to the formula $V_{\mathrm{L}} = L \cdot di_{\mathrm{L}} / dt$, the voltage direction on the inductor is opposite the direction of the inductor current, and the value of inductor is constant. Thus, the inductor current decreases linearly. When combined with (1) and (2), the voltage and current equations can be obtained as follows:

$$\begin{aligned} &V_{\mathrm{L1}} = V_{\mathrm{L2}} = -V_{\mathrm{o}} \\ &i_1 = 2i_{\mathrm{L}} = i_{\mathrm{o}} + i_{\mathrm{Co}} \end{aligned} \tag{4}$$



(a)



(b)

Fig. 3 Equivalent circuit diagrams in the CCM mode: **a** mode 1; **b** mode 2

2.2 DCM Mode Analysis

The inductor is charged when the switches are on, and discharged when the switches are off. In the DCM mode, the inductor releases the stored energy when the switch is off. That is, the inductor current has been reduced to zero before the switch is turned on in the next cycle. In the DCM mode, there are three modes in each period, where the first two modes are the same as those in the CCM mode. The equivalent circuit of mode 3 is shown in Fig. 4. Both the switches and diodes are turned off, and the output capacitors C_{o1} and C_{o2} supply power to the load. The corresponding equations are as follows:

$$\begin{cases} V_{\mathrm{in}} = V_{\mathrm{Cin1}} + V_{\mathrm{Cin2}} \\ V_{\mathrm{o}} = V_{\mathrm{Co1}} + V_{\mathrm{Co2}} \\ i_{\mathrm{L1}} = i_{\mathrm{L2}} = 0 \end{cases} \tag{5}$$

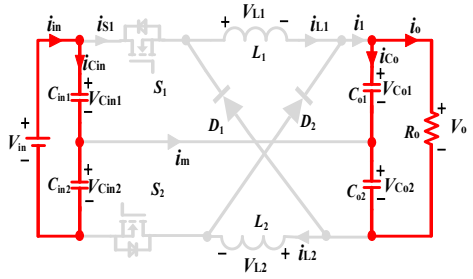


Fig. 4 Equivalent circuit of mode 3 in the DCM mode

3 Performance Analysis

3.1 Voltage Gain

1) Voltage gain in the CCM mode

In the CCM mode, the volt-second balance principle on inductors L_1 and L_2 is as follows:

$$DT \cdot \left(\frac{V_{\mathrm{in}} - V_{\mathrm{o}}}{2}\right) + (1-D)T \cdot (-V_{\mathrm{o}}) = 0 \tag{6}$$

The converter voltage gain in the CCM mode can be obtained by simplifying the above (6):

$$G_{\mathrm{CCM}} = \frac{V_{\mathrm{o}}}{V_{\mathrm{in}}} = \frac{D}{2-D} \tag{7}$$

The voltage gain of the converter under non-ideal conditions depends on the parasitic parameters for each of the elements. Fig. 5 shows the topology of the converter when considering the parasitic parameters of the device.

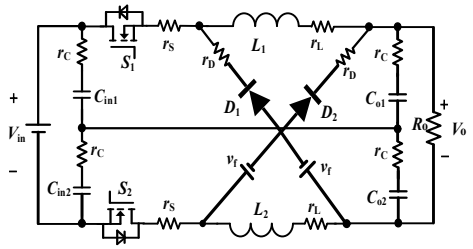


Fig. 5 Proposed converter with its parasitic components

In order to facilitate an analysis and evaluation of the performance of the converter, the parasitic parameters of the device are considered as follows: inductors ($r_{\mathrm{L1}} = r_{\mathrm{L2}} =$

r_L); capacitors ($r_{Cin1} = r_{Cin2} = r_{Co1} = r_{Co2} = r_C$); switches ($r_{S(on)1} = r_{S(on)2} = r_S$); diodes ($r_{D1} = r_{D2} = r_D$); and their forward voltages ($v_{f1} = v_{f2} = v_f$). By considering the parasitic elements, the volt-second balance principle of the inductor can be rewritten as:

$$\begin{aligned}&\frac{V_{in}-V_o-2I_o(r_S+r_L)}{2}\cdot DT\\&-[V_o+v_f+I_o(r_S+r_D)]\cdot(1-D)T=0\end{aligned}\tag{8}$$

The expression of the converter voltage gain in the non-ideal state is as follows:

$$\begin{aligned}G_0&=\frac{V_{in}}{V_o}\\&=\frac{D}{2-D+\frac{2Dr_L}{R_o}+\frac{2r_S}{R_o}+\frac{2r_D}{R_o}-\frac{2Dr_D}{R_o}+\frac{v_f}{V_o}(2-D)}\end{aligned}\tag{9}$$

From the above formula, it can be seen that when considering the parasitic parameters, the voltage gain of the proposed converter changes, and the specific value should be determined in combination with the value of the parasitic parameters.

In addition, when the inductor or capacitor is unbalanced, since the expression of the voltage gain is only related to the switching duty cycle, the voltage gain does not change. However, the neutral line current is no longer zero and the input and output capacitor voltage have large ripples.

2) Voltage gain in the DCM mode

As for the DCM mode, a waveform of the inductor current is shown in Fig. 6. [t_0~t_1], [t_1~t_2], and [t_2~t_3] in the figure correspond to the three modes (mode 1, mode 2, and mode 3) of the converter in the DCM mode. As presented in Fig. 6, the corresponding times of the three modes are DT, D_2T, and (T-DT-D_2T).

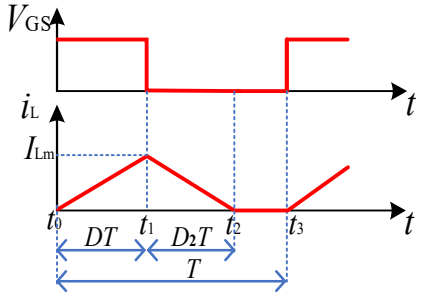


Fig. 6 Inductor current waveforms in the DCM mode

In mode 1, there is:

$$I_{Lm}=\frac{V_L}{L}DT\tag{10}$$

where I_{Lm} is the peak inductor current in the DCM mode.

By substituting (3) into the above formula, it is possible to obtain the following:

$$I_{Lm}=\frac{V_{in}-V_o}{2L}\cdot DT\tag{11}$$

Similarly, in mode 2:

$$I_{Lm}=\frac{V_L}{L}\cdot D_2T=\frac{V_o}{L}\cdot D_2T\tag{12}$$

By combining (11) and (12), the following results can be obtained:

$$D_2=\frac{V_{in}-V_o}{2V_o}D\tag{13}$$

In terms of load resistor R_o, it is possible to obtain the average value of the output current I_o as follows:

$$I_o=\frac{V_o}{R_o}\tag{14}$$

In a cycle, the average current of the output capacitor is zero. Thus, the average value of the output current I_o is equal to I_1 (the average value of i_1) as shown in the equivalent circuit in the DCM mode.

From Fig. 6, it can be seen that:

In mode 1 (t_0~t_1), i_1=i_L;

In mode 2 (t_1~t_2), i_1=2i_L;

In mode 3 (t_2~t_3), i_1=0.

Therefore, the expression of the average value of the output current is:

$$\begin{aligned}I_o&=\frac{1}{T}\int_0^T i_o(t)dt\\&=\frac{1}{T}\left[\int_0^{t_1} i_L(t)dt+\int_{t_1}^{t_2}2i_L(t)dt\right]\\&=\frac{1}{T}\left(\frac{1}{2}DT\cdot I_{Lm}+2\cdot\frac{1}{2}D_2T\cdot I_{Lm}\right)\end{aligned}\tag{15}$$

By substituting (10) and (12) into (14) and (15), the voltage gain of the proposed converter in the DCM mode is expressed as follows:

$$G_{DCM}=\frac{V_o}{V_{in}}=\frac{D\sqrt{D^2+16\tau}-D^2}{8\tau}\tag{16}$$

where $\tau=L/(R_oT)=Lf_s/R_o$ and f_s refers to the switching frequency.

3) BCM conditions

The voltage gain in the CCM mode is made equal to that in the DCM mode. There are:

$$G_{CCM}=G_{DCM}\tag{17}$$

By substituting (7) and (16) into the formula (17), the expression below can be obtained:

$$\tau_{BCM}=\frac{(2-D)(1-D)}{2}\tag{18}$$

The boundary conditions of the proposed converter are presented in Fig. 7.

As can be observed from Fig. 7, when τ is larger than τ_{BCM}, the proposed converter is operated in the CCM mode. When the input and output voltage levels are determined, the resistor load and duty cycle are fixed values. Therefore, when selecting device parameters, it is necessary to select appropriate inductor and switching frequency values to make the converter work in the CCM mode.

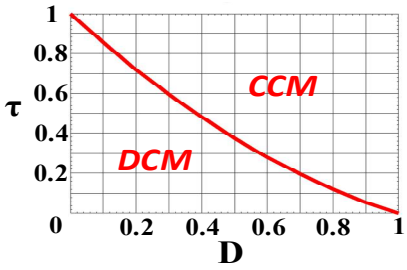


Fig. 7 BCM conditions

3.2 Current and Voltage Stresses of Semiconductor Devices

According to the equivalent circuit and the related voltage current equation in the CCM mode, the following can be obtained:

In mode 1, there are:

$$V_S = 0, V_D = \frac{V_{in} + V_o}{2}, i_S = i_L, i_D = 0 \tag{19}$$

In mode 2, there are:

$$V_S = \frac{V_{in} + V_o}{2}, V_D = 0, i_S = 0, i_D = i_L \tag{20}$$

By combining (19) and (20), the maximum voltage and current stresses of the semiconductor devices can be summarized as follows:

$$V_{Dmax} = V_{Smax} = \frac{V_{in} + V_o}{2} = \frac{V_{in}}{2 - D} \tag{21}$$

$$I_{Smax} = I_{Dmax} = I_p = I_L + \frac{(V_{in} - V_o) D}{4 L f_s} \tag{22}$$

where I_p is the peak of the inductor current. I_L is the average value of the inductor current.

3.3 Voltage Balance Characteristics of the Switches

As for the conventional high step-down converter, since the junction capacitors of the switches and inductor are easy to resonate, the voltage on the switches oscillates. In the proposed converter, due to the existence of a clamp circuit in the topology, the problem of voltage oscillation can be solved. The specific analysis is as follows.

The input capacitor, the output capacitor, and the neutral line in the proposed converter topology together form a clamping circuit. The proposed converter realizes the voltage balance of the switch through this clamping circuit. Voltage balance diagrams on the switch are shown in Fig. 8. The green circuit and blue circuit in the figures represent the voltage circuits across switches S_1 and S_2, respectively.

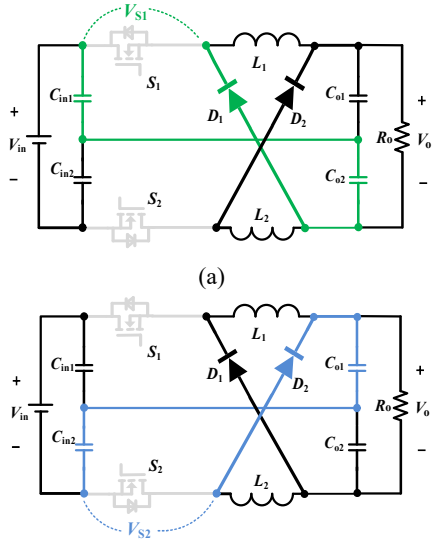


Fig. 8 Voltage balance diagram of the switches: **a** S_1; **b** S_2

From the above figure, it is possible to obtain the expression of the voltage stress on the switches as follows:

$$\begin{cases} V_{S1} = V_{Cin1} + V_{Co2} \\ V_{S2} = V_{Cin2} + V_{Co1} \end{cases} \tag{23}$$

The volt-second balance principle formula of the two inductors can be obtained as follows:

$$\begin{cases} (V_{Cin1} - V_{Co1}) \cdot DT - (V_{Co1} + V_{Co2}) \cdot (1 - D)T = 0 \\ (V_{Cin2} - V_{Co2}) \cdot DT - (V_{Co1} + V_{Co2}) \cdot (1 - D)T = 0 \end{cases} \tag{24}$$

By simplifying the above formula, it is possible to obtain:

$$V_{Cin1} - V_{Co1} = V_{Cin2} - V_{Co2} \tag{25}$$

Then, it is possible to obtain:

$$V_{S1} = V_{S2} \tag{26}$$

Therefore, the function of the clamping circuit is to keep the voltage stress on the switches equal. Thus, the converter can realize the voltage balance of the switches regardless of whether or not the values of capacitors and inductors are symmetric.

3.4 Output Voltage Ripple

According to the above analysis, the output capacitor voltage is always equal to half the output voltage. Voltage and current waveforms of the output capacitor are shown in Fig. 9.

From the above waveforms, the ripple of the output capacitor voltage is:

$$\Delta V_{C_o} = \frac{1}{C_o} \int_{t_0}^{t_1} i_{C_o}(t) dt = \frac{1}{C_o} \int_0^{DT} i_{C_o}(t) dt \tag{27}$$

According to the equivalent circuit of the converter in $[t_0 \sim t_1]$, it can be seen from Fig. 3a that:

$$i_{C_o}(t) = i_L(t) - I_o \tag{28}$$

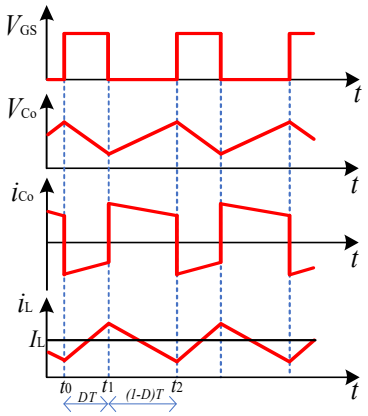


Fig. 9 Voltage current waveforms of the output capacitance

Therefore, the ripple of the output capacitor voltage can be obtained as follows:

$$\Delta V_{C_o} = \frac{1}{C_o}\int_0^{DT}\left[i_L(t) - I_o\right]dt = \frac{I_o(1-D)}{C_o f_s} \quad (29)$$

where I_o is the average value of the output current.

The ripple of the output voltage can be obtained as follows:

$$\Delta V_o = 2\Delta V_{C_o} = \frac{2I_o(1-D)}{C_o f_s} \quad (30)$$

3.5 Loss and Efficiency Analysis

In practice, almost all of the elements including the switches, diodes, capacitors, and inductors are not ideal. The parasitic effects of the internal resistors and inductors increase the losses of the devices, and affect the efficiency of the converter. The specific impacts and effects need to be further discussed by establishing the loss equation model. Generally speaking, the losses of a non-isolated converter mainly include the switch losses, diode losses, inductance losses, and output capacitance losses.

For the convenience of the loss analysis, the expression of the root mean square (RMS) current for each of the devices are shown in Table 1.

Table 1 Current Root Mean Square Equations

Components	Expression
Switching S_1, S_2	$I_{Srms} = \frac{I_o\sqrt{D}}{2-D}$
Diode D_1, D_2	$I_{Drms} = \frac{I_o\sqrt{1-D}}{2-D}$
Inductor L_1, L_2	$I_{Lrms} = \frac{I_o}{2-D}$
Output capacitor C_{o1}, C_{o2}	$I_{Crms} = \frac{I_o\sqrt{D(1-D)}}{2-D}$

1) Switch loss

The conduction losses of the switches are mainly brought by the internal resistance of the switch device:

$$P_{S(on)} = \left(I_{Srms}\right)^2 r_{S(on)} \quad (31)$$

where $r_{S\,(on)}$ is the ON-state resistance of the switch, and I_{Srms} is the RMS value of the current flowing through the switch. Taking the I_{Srms} expression in Table 1 into the above formula, it is possible to obtain:

$$P_{S(on)} = \frac{DI_o^{\,2}}{(2-D)^2}\cdot r_{S(on)} \quad (32)$$

In the switch operation process, there are conduction losses when the switch is in the ON state. In addition, there are also switching losses when the switch is opened and closed. The switching losses depend on the voltage and current of the switch, the part where they overlap, and the working frequency of the switches. For convenience of calculation, a schematic diagram of the on-off transients of the switch are shown in Fig. 10.

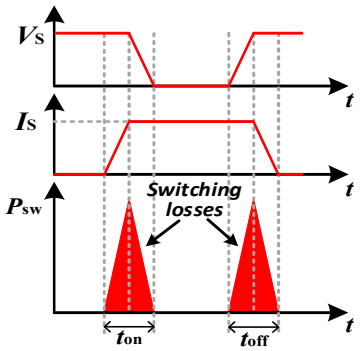


Fig. 10 Transient schematic diagram of switching losses

The switching loss expression of the switch can be written as:

$$P_{sw} = \frac{1}{2}V_S I_S f_s (t_{on} + t_{off}) \quad (33)$$

where V_S and I_S are the maximum voltage and current stresses of the switch, f_s is the operating frequency of the switch, while t_{on} and t_{off} are the on-off times of the switch

By combining (32) and (33), it is possible to see that the switch loss is:

$$\begin{aligned} P_S &= P_{S(on)} + P_{sw} \\ &= \frac{DI_o^{\,2}}{(2-D)^2}\cdot r_{S(on)} + \frac{1}{2}V_S I_S f_s (t_{on} + t_{off}) \end{aligned} \quad (34)$$

2) Diode loss

The loss of a diode is mainly composed of conduction losses and reverse recovery losses.

The expression of conduction loss is:

$$P_{Dc} = v_F I_D \quad (35)$$

where I_D is the average value of the current flowing through the diode. V_D is employed to represent the forward

bias voltage of the diodes. From the above mode analysis of the converter, it is possible to obtain that:

$$I_{\mathrm{D}} = (1-D)I_{\mathrm{L}} = \frac{(1-D)I_{\mathrm{o}}}{2-D} \tag{36}$$

The reverse recovery losses are given by:

$$P_{\mathrm{Dr}} = Q_{\mathrm{r}} v_{\mathrm{r}} f_{\mathrm{s}} \tag{37}$$

where Q_{r} is the reverse stored charge of the diode, v_{r} is the voltage across the diode when it is turned off, and f_{s} is the working frequency of the converter.

Thus, the diode losses can be obtained as follows:

$$P_{\mathrm{D}} = P_{\mathrm{Dc}} + P_{\mathrm{Dr}} = \frac{(1-D)I_{\mathrm{o}} v_{\mathrm{F}}}{2-D} + \frac{Q_{\mathrm{r}} f_{\mathrm{s}} V_{\mathrm{in}}}{2-D} \tag{38}$$

3) Inductor loss

The inductance loss is mainly divided into copper loss and iron loss. The copper loss is mainly related to the DC resistance of the winding wire, and its expression is as follows:

$$P_{\mathrm{Lr}} = \left(I_{\mathrm{Lrms}}\right)^2 r_{\mathrm{L}} \tag{39}$$

where r_{L} is the internal equivalent resistor of the inductor. I_{Lrms} is the RMS value of the inductor current. By taking the I_{Lrms} expression in Table 1 into the above formula, it is possible to obtain:

$$P_{\mathrm{Lr}} = \frac{I_{\mathrm{o}}^{\,2}}{\left(2-D\right)^2} \cdot r_{\mathrm{L}} \tag{40}$$

Meanwhile, the iron loss is mainly related to the magnetic core, and its expression is:

$$P_{\mathrm{Lc}} = (aB_{\mathrm{pk}}{}^{b} f_{\mathrm{s}}{}^{c}) A_{\mathrm{e}} l_{\mathrm{e}} \tag{41}$$

where B_{pk} is the alternating current flux density of the magnetic core; a, b, c are determined to be constant in relation to the magnetic core; l_{e} is the path length of the core; and A_{e} is the cross-sectional area of the magnetic core.

The loss of the inductor can be summarized as follows:

$$P_{\mathrm{L}} = P_{\mathrm{Lr}} + P_{\mathrm{Lc}} = \frac{I_{\mathrm{o}}^{\,2}}{(2-D)^2} r_{\mathrm{L}} + (aB_{pk}{}^{b} f_{\mathrm{s}}{}^{c}) A_{\mathrm{e}} l_{\mathrm{e}} \tag{42}$$

4) Output capacitance loss

Similar to the inductance loss, when combined with the RMS value of the current of output capacitance in Table 1, the expression of the output capacitance loss can be obtained as follows:

$$P_{\mathrm{Co}} = \frac{I_{\mathrm{o}}{}^{2} D(1-D)}{\left(2-D\right)^2} \cdot r_{\mathrm{Co}} \tag{43}$$

where r_{Co} is the internal resistance of the capacitor.

By summing up (31)-(43), the overall loss of the converter is expressed as:

$$P_{\Sigma} = 2P_{\mathrm{S}} + 2P_{\mathrm{D}} + 2P_{\mathrm{L}} + 2P_{\mathrm{Co}} \tag{44}$$

Then the overall efficiency is:

$$\eta = \frac{P_{\mathrm{o}}}{P_{\mathrm{o}} + P_{\Sigma}} \tag{45}$$

where P_{o} is the output power.

Table 2 Comparison of the Proposed Converter With Recent Counterparts

	Interleaved Converter with an Auxiliary Circuit	Valley-Fill Switched Capacitor Converter	Switched-Capacitor Interleaved Bidirectional Converter	Three-Phase Interleaved Converter	Switched-Inductor Converter	Proposed converter
Switches Count	3	5	8	6	1	2
Diodes Count	5	3	0	3	2	2
Capacitor Count	2	3	4	6	1	4
Inductor Count	2	2	3	3	2	2
Voltage gain	$\frac{D}{2}$	$\frac{D}{5}$	$\frac{D}{3}$	$\frac{D}{4}$	$\frac{D}{2-D}$	$\frac{D}{2-D}$
Voltage Stress of switch	V_{in},$2V_{in}$	$0.8V_{in}$	$\frac{V_{in}}{3}$	$\frac{V_{in}}{2}$	$\frac{2V_{in}}{2-D}$	$\frac{V_{in}}{2-D}$
Voltage Stress of diode	V_{in},$2V_{in}$	$0.4V_{in}$	×	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2-D}$	$\frac{V_{in}}{2-D}$
Input Voltage(V)	150	300	400	400	40	400
Output Voltage(V)	12	12	30-100	24	15	48
Output Power(W)	120	100	800	250	60	240
Frequency (Hz)	100k	100k	20k	50k	100k	50k
Peak Efficiency (%)	95	93.4	93.8	94.7	90.7	96.5

3.6 Comparative Analysis

For the sake of evaluating the performance of the converter proposed in this paper, a comparison between the proposed converter and recent counterparts in [3], [18], [20], [21], [23] is presented in Table 2. Their names are "interleaved converter with an auxiliary circuit," "valley-fill switched capacitor converter,"
"switched-capacitor interleaved bidirectional converter," "three-phase interleaved converter," and "switched-inductor converter."

It can be observed from Table 2 that the voltage stresses on the switches and diodes of the proposed converter are lower. The proposed converter has a simpler structure. Moreover, the number of semiconductor elements in the converter is lower, which reduces the losses of the converter in the process of operation. Thus, the proposed converter has improved efficiency. When compared with the other converters, the proposed converter has high step-down ratio, reduced cost, and improved power density.

4 Design Considerations

4.1 Inductor Design

Since the circuit is symmetrical, the two inductance values are equal. In addition, the inductance value should be determined by the inductor current ripple. The expression is as follows:

$$\Delta i_{\mathrm{L}}=\frac{V_{\mathrm{L}}}{L}\cdot DT=\frac{(1-D)DV_{\mathrm{in}}}{(2-D)Lf_{\mathrm{s}}} \tag{46}$$

The expression of L_1 & L_2 inductances can be obtained from the above formula as:

$$L_1=L_2\geq\frac{(1-D)DV_{\mathrm{in}}}{(2-D)f_{\mathrm{s}}\Delta i_{\mathrm{L}}} \tag{47}$$

The above formula shows that the input voltage, switching frequency, duty cycle, and inductor current ripple should be considered when selecting an inductance value.

4.2 Output Capacitor Design

According to the expression of the output capacitance ripple, the expression of the output capacitance can be obtained as follows:

$$C_{\mathrm{o1}}=C_{\mathrm{o2}}\geq\frac{I_{\mathrm{o}}(1-D)}{\Delta V_{\mathrm{C}}f_{\mathrm{s}}} \tag{48}$$

From the above formula it can be seen that the output current, switching frequency, duty cycle, and capacitor voltage ripple should be considered when selecting the output capacitance value.

5 Experimental Results

To further substantiate the correctness of the above theoretical analysis, experiments are carried out. The experimental prototype of the converter is shown in Fig. 11. Considering the practical application of the converter, a voltage level of 400/48V was chosen since it is more widely used in industry. The parameters for each of the devices are calculated as follows:

$$\begin{cases}V_{\mathrm{in}}=400\mathrm{V},V_{\mathrm{o}}=48\mathrm{V},P_{\mathrm{o}}=240\mathrm{W}\\ I_{\mathrm{o}}=5\mathrm{A},R_{\mathrm{o}}=\dfrac{V_{\mathrm{o}}}{I_{\mathrm{o}}}=9.6\Omega,D=\dfrac{2G}{1+G}=0.214\\ V_{\mathrm{Smax}}=V_{\mathrm{Dmax}}=\dfrac{V_{\mathrm{o}}+V_{\mathrm{in}}}{2}=224\mathrm{V}\\ V_{\mathrm{Lmax}}=\dfrac{V_{\mathrm{in}}-V_{\mathrm{o}}}{2}=176\mathrm{V}\\ V_{\mathrm{Cin}}=\dfrac{1}{2}V_{\mathrm{in}}=200\mathrm{V},V_{\mathrm{Co}}=\dfrac{1}{2}V_{\mathrm{o}}=24\mathrm{V}\end{cases} \tag{49}$$

When combined with the design considerations in section 4, it is possible to obtain the experimental conditions and device parameters of the converter as shown in Table 3.

Table 3 Experimental Conditions and Device Parameters of the Proposed Converter

Components	Parameters
Input voltage: V_{in}	400V
Output voltage: V_{o}	48V
Output power: P_{o}	240W
Switching frequency: f_{s}	50kHz
Switching S_1, S_2	BSC600N25NS3 G (R_{on}=60mΩ, t_{on}+t_{off}=50ns)
Diode D_1, D_2	HRM10L300SFCT (V_{F}=840mV)
Inductor L_1, L_2	960μH(220mΩ)
Input capacitors: C_{in1}&C_{in2}	100μF/250V
Output capacitor C_{o1}, C_{o2}	470μF/35V

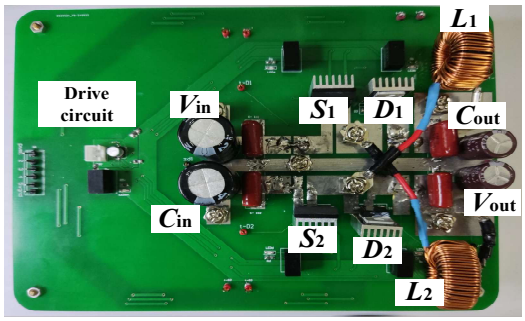


Fig. 11 Experimental topology circuit

Waveforms of the experiments are displayed below. Fig. 12 shows waveforms of the inductor current. From the experimental waveforms it can be seen that that the average value of the inductor current is about 2.8A. When

the switches are on, the inductor current increases linearly, and when the switches are off, the inductor current decreases linearly.

Waveforms of the input voltage and output voltage are displayed in Fig. 13. When the input voltage is 400V, the output voltage is about 48V. The converter has achieved a high step-down conversion. Waveforms of the input capacitor voltage and output capacitor voltage are presented in Fig. 14. From Fig. 13 - Fig. 14, it can be seen that the input capacitor voltage is 200V and the output capacitor voltage is about 24V. Since the converter is symmetrical, the voltages on the input and output capacitors are equivalent to half of the input and output voltages, respectively.

Experimental waveforms of the current through the switches and diodes are shown in Fig. 15. When the switches or diodes are on, the current flowing past them is equivalent to the inductor current. When they are off, the current is zero. Experimental waveforms of the voltage stresses on the switches S_1 and S_2 are presented in Fig. 16. In addition, the waveforms of the voltage stress of the diodes D_1 and D_2 are presented in Fig. 17. From the Fig.16 - Fig. 17, it can be concluded that the maximum value of the voltage stress is equal to half the sum of the input and output voltages. The voltage stresses of the switches and diodes are far less than the input voltage, which is in line with the previous analysis.

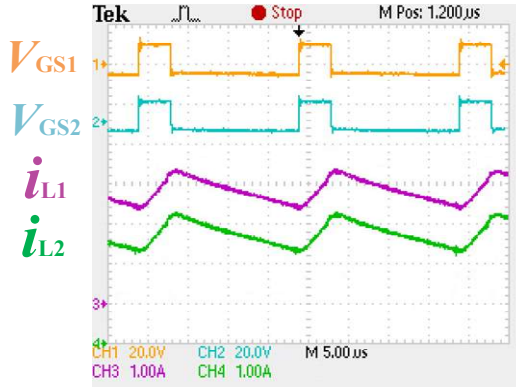


Fig. 12 Gate-source signal (V_{GS}) and inductor current (i_L) waveforms

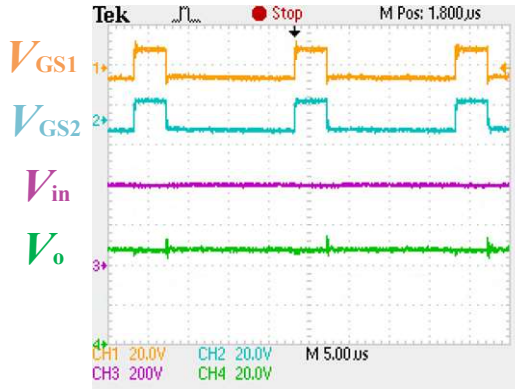


Fig. 13 Gate-source signal (V_{GS}), input voltage (V_{in}), and output voltage (V_o) waveforms

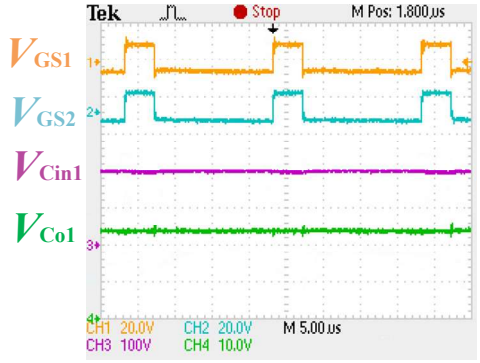


Fig. 14 Gate-source signal (V_{GS}), input capacitor voltage (V_{Cin1}), and output capacitor voltage (V_{Co1}) waveforms

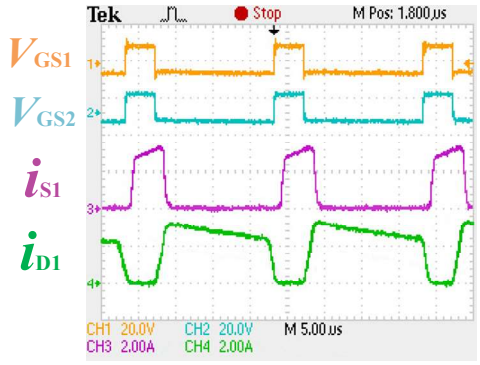


Fig. 15 Gate-source signal (V_{GS}), switch current stress (i_{S1}), and diode current stress (i_{D1}) waveforms

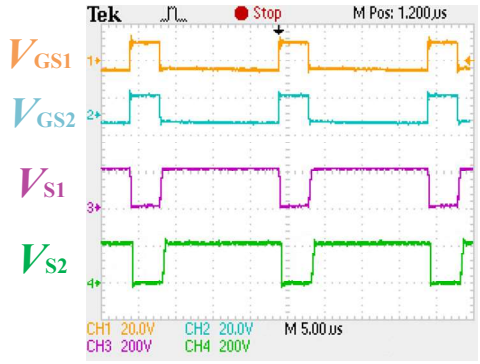


Fig. 16 Gate-source signal (V_{GS}) and drain-source voltage (V_S) waveforms

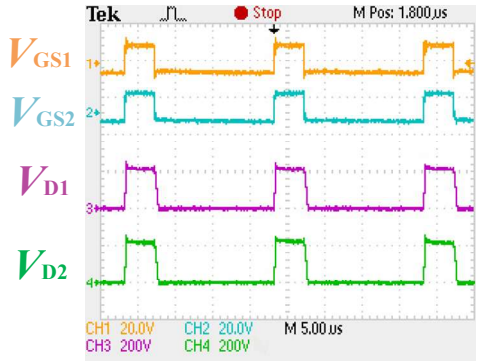


Fig. 17 Gate-source signal (V_{GS}) and diode voltage stress (V_D) waveforms

From Fig. 16, it can be seen that the voltage stress of the switches is equal, and that there is no oscillation due to the symmetrical structure of the circuit. In addition, the

voltage stresses of diodes D_1 and D_2 are the same, as shown in Fig. 17. Obviously, the converter has good voltage balance performance. In addition, as shown in Fig. 13 - Fig. 14, the voltage on the two input capacitors is equal, and the same is true on the output capacitors. This also confirms the voltage balance characteristics of the converter.

To test the analysis of the output current ripple, simulation experiments in PSIM are carried out and the results are shown in Fig. 18. It can be observed that the ripple of the output current is very small, and the ripple rate is as follows:

$$k_{Io} = \frac{\Delta I_o}{I_o} \approx \frac{0.006}{5} = 0.12\% \tag{50}$$

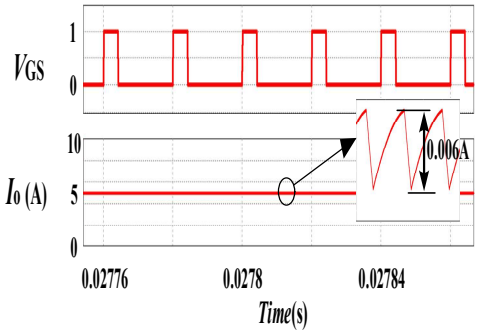


Fig. 18 Gate-source signal (V_{GS}) and output current (I_o) simulation waveforms

In order to evaluate the transient performance of the proposed converter, load transient experiments have been carried out after adding the closed-loop control of the converter. Transient experimental waveforms of the output voltage when the load current changes from 5A to 10A are shown in Fig. 19, and the corresponding waveforms when the load current changes from 10A to 5A are shown in Fig. 20. It can be seen from these waveforms that when the load suddenly changes, the output voltage slightly fluctuates. However, on the whole, it can still be maintained at the rated output voltage. Therefore, it can be senn from the transient experiments that the proposed converter has good transient performance.

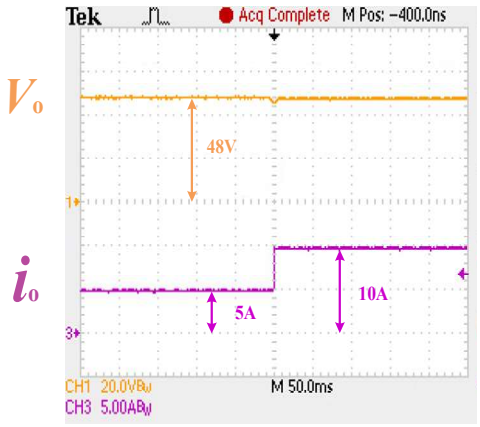


Fig. 19 Transient waveforms of the output voltage when the load current changes from 5A to 10A

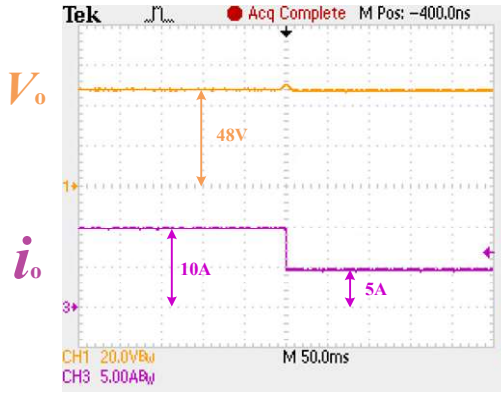


Fig. 20 Transient waveforms of the output voltage when the load current changes from 10A to 5A

When combined with the specific parameters in the experiments and in the above loss analysis, a loss distribution diagram of the converter can be obtained as shown in Fig. 21. From Fig. 21 it can be seen that the losses of the converter mainly include the switches losses and the diodes losses.

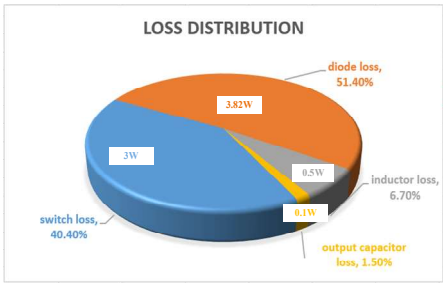


Fig. 21 Loss distribution of the proposed converter

Experimental efficiency curves are shown in Fig. 22. It can be seen that the peak efficiency value of the proposed converter is about 96.5%, while maximum efficiency of the three-phase interleaved converter in [21] is 94.7%. With an increase of the load, the losses increase, and the efficiency decreases accordingly.

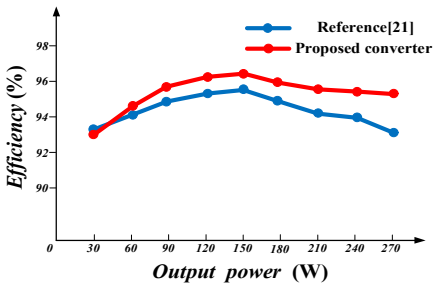


Fig. 22 Efficiency curve

6 Conclusion

In this paper, a symmetrical non isolated high step-down converter based switched inductor topology was proposed. By controlling the on-off of the switch to change the

inductor in series or parallel, the purpose of high step-down capability is realized. The proposed converter was analyzed in detail with a modes analysis in CCM, DCM, and BCM, voltage gain, voltage stress, output ripple analysis, loss analysis, comparison analysis, and design considerations. When compared with other high step-down converters, the proposed converter has a lot of virtues such as a simpler structure, fewer components, lower voltage on the semiconductor devices, voltage balance capability, and lower loss, which improves the efficiency of the proposed converter. Therefore, the converter is more applicable to high step-down occasions. Finally, experimental results on the circuit topology verify the above theoretical analysis.

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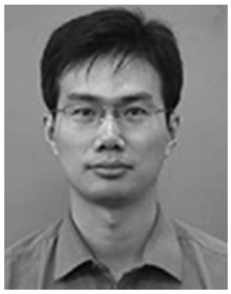

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