Switching Loss Balance and Transient DC-Bias Suppression Strategies in Three-Level DAB Converters Modulated with Five DoFs

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***Abstract*—In the three-level (3L) neutral-point-clamped (NPC) dual-active-bridge (DAB) converter, both sides of the converter can adapt to higher DC bus voltage, and more control degrees of freedom (DoFs) are provided compared to the conventional DAB converter. In the PWM generating technique with 5 DoFs, switching loss imbalance may develop because switch devices turn on and off under varying current stresses, affecting system reliability. In addition, the transient DC-bias issue may also arise in the 3L-NPC-DAB converter modulated with 5 DoFs, leading to the transformer saturation. In this paper, two strategies are proposed to suppress the loss imbalance and the transient DC-bias in the current stress and magnetizing branches. It is also general and applicable for SPS, DPS, and TPS modulations. Furthermore, the switching loss balance strategy and DC-bias suppression strategy are applied in the PWM generation technique simultaneously without additional components. With the proposed solutions, the switching loss imbalance is suppressed and DC-bias in the integral of voltages on both sides of the 3L-NPC-DAB converter is abolished. The effectiveness of the proposed strategies is validated by a series of experiments conducted under varying situations.**

***Index Terms*—Dual-Active-Bridge (DAB), DC-bias, Switching loss balance, Three-Level.**

I. Introduction

Since its introduction in [1], the two-level (2L) Dual-Active-Bridge (DAB) converter has attracted considerable interest because of its ease of operation, simple topology, and high power density. Therefore, in the field of Isolated Bidirectional DC-DC Converter (IBDC), the DAB converter and its variants (three-phase [2], half-bridge [3], etc.) are widely used in power electronic transformers and distributed energy storage systems [4] [5]. The conventional two-level DAB converter consists of a high-frequency transformer and two full bridges located at the primary and secondary sides. For DAB converter modulation techniques, single-phase-shift (SPS) modulation is the most common and simplest control method. In SPS modulation, the diagonal switch devices on each side of the DAB converter are driven by the same pulses, while the switch devices in the same bridge arm are driven by complementary pulses. Square wave voltages with a duty cycle of 50% are generated on the primary and secondary sides of the DAB converter, respectively. The two voltages are phase-shifted to adjust the transmission power's direction and magnitude [6]. Extended-phase-shift (EPS) modulation [7], dual-phase-shift (DPS) modulation [8], and triple-phase-shift (TPS) modulation are proposed to boost the efficiency and zero-voltage-switching operation range by adding additional degrees of freedom (DoFs) [9]. In EPS modulation, the output of one bridge is still the square wave voltage with a duty cycle of 50%, while the other generates a three-level voltage waveform. In DPS modulation, both bridges generate the three-level voltage waveform, and the inner phase shift angles on both sides are the same. TPS modulation, like DPS modulation, causes the two bridges to exhibit voltage waveforms with three levels, but the inner phase shift angles on the two sides may be different.

Introducing a multi-level structure into the classic DAB architecture is another feasible way for improving the operational characteristics of the DAB converter [10]. This provides two benefits. On the one hand, the multi-level topology enables switch devices with better on-off and switching characteristics in high-voltage applications, hence decreasing system losses and costs. In addition, the multi-level structure provides additional DoFs, which makes the DAB converter easier to control and makes it simpler to improve system performance [11].

The high-voltage input is achieved in [12] by putting a three-level (3L) neutral-point-clamped (NPC) bridge arm into the primary side of DAB. During the process of generating multiple voltage levels by simple series connection of capacitors, the problem of capacitor voltage balancing arises, as discussed in [13]. In [14], the high-voltage output is realized by adding a 3L-NPC bridge arm on the secondary side of the DAB converter. In [15], 3L-NPC bridge arms with flying capacitors are introduced to the primary and secondary sides of the DAB converter so that both sides can adjust to a greater DC bus voltage. For the modulation of the 3L-NPC-DAB converter, the vast majority of scholars concentrate on the capacitor voltage balance issue [13][16][17]. In [11], a modulation strategy with 13 DoFs is proposed to enhance the control flexibility, but its implementation is impractical due to its complexity. In [18], a modulation strategy with five DoFs is proposed to achieve a balance between the control degrees and the implementation complexity, the optimization scheme is centered on minimizing the rms value of the inductor current.

In conventional DAB converters, switch devices have different switching losses under TPS modulation, resulting from turning on and off under varying currents [19]. This will result in varying switch device service lives and affect the system's reliability. Similar switching loss imbalance may develop in

the 3L-NPC-DAB converter due to the leading signal and lagging signal introduced by the modulation. In this paper, a switching loss balance technique for modulation with 5 DoFs is proposed by alternating leading and lagging signals every two switching cycles.

DC-bias current is another issue that must be addressed in DAB converters. In general, the volt-second product of the transformer's primary and secondary voltages during one switching cycle is zero. The current going through the transformer will therefore not have a DC bias. However, this premise cannot be satisfied in real applications, particularly for processes that are transient. In actual operation, the transient DC-bias problem may be caused by variances in component parameters, asymmetry in circuit layout, inconsistent voltage drop, inconsistent turn-off duration, and asymmetry of trigger pulse waveforms of both sets of bridge arms [20]. It causes the current waveform of the high-frequency transformer to be asymmetrical, resulting in an unsymmetrical magnetization curve about the origin. Due to the nonlinearity of the magnetization curve, when the bias is severe, the core will inevitably enter deep saturation in one direction, resulting in an increase in loss, an increase in unidirectional magnetizing current, and damage to the switch devices, which has a severe impact on the bidirectional converter's reliability.

The DC-bias current could be categorized as either steady-state or transient-state [21]. The steady-state DC-bias current could be suppressed by passive methods like selecting power devices, adding an air gap or DC-blocking capacitors to the transformer core, and active methods, such as closed loop control using sensors [22]. However, due to the phase-shift nature of the transient DC-bias current, these approaches are inapplicable. The transient DC-bias current is created mostly by the dynamic activities of the DAB converter, such as startup, load change, and power reversal [20]. Many methods have been proposed to address the transient DC-bias, and they could be classified into flux bias suppression method, dynamic optimization method, straightforward transient control, and piece-wise linear transient phase-shift optimization [20]. There are passive and active flux-bias suppression methods. In passive methods, DC-blocking capacitors are placed into the transformer to eliminate the DC-bias current. However, this causes low-frequency oscillations and impacts the power density [23]. Active methods use sensors to regulate the DC component flux of the magnetizing core but at a higher price. The method of dynamic optimization speeds the transient process, which naturally mitigates the impacts of the transient DC-bias current, hence minimizing the settling time [24]. However, multiple switching cycles are required to eliminate the DC bias current entirely. In the piece-wise linear transient phase shift optimization, both accelerating the transient state and eliminating the DC-bias rapidly are objectives. In [21], the methods of transient modulation are centered on SPS modulation. There is a constraint on the ratio of phase shift to guarantee that the currents are within the safe range, which also restricts the speed of dynamic response [25]. In general, the piece-wise linear transient phase shift optimization method controls the gate signals between two steady-state cycles, and does not need extra components or sensors. However, it may be more complicated to control the transient-state with the increase of DoFs. The straightforward transient control is to adjust the inductor current in a linear manner to obtain the maximum current slope and the shortest settling time. In [26], a non-zero voltage is injected at the end of a switching cycle in order to force the current into the new steady state. However, this could be hard to accomplish if changes are made continually across successive switching cycles.

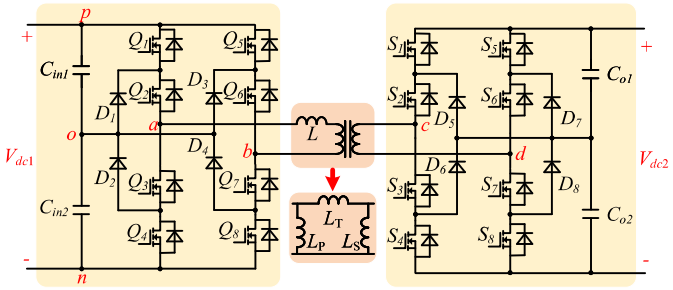

Fig. 1. Circuit configuration of the 3L-NPC-DAB converter.

Since the 3L-NPC-DAB converter modulated with 5 DoFs has similar operating states to the 2L-DAB converter, the DC-bias issue still exists in the transient performance, and no strategy was previously proposed. This paper presents a detailed analysis of the DC-bias in the 3L-NPC-DAB converter with five DoFs modulation and proposes a solution to mitigate the DC-bias problem. The waveform of the current does not need to be piece-wise analyzed, because once the DC-bias in the integral of the primary voltage and the secondary voltage is eliminated, the DC-bias in current stress is also reduced. Moreover, SPS, DPS, and TPS modulation methods are all special situations of modulation with 5 DoFs, hence the proposed DC-bias suppression strategy is applicable to different modulation modes. The steady-state and transient-state of the 3L-NPC-DAB converter can be enhanced by combining the above-mentioned switching loss balance strategy and DC-bias suppression strategy into the PWM generation module. The PWM generation method is discussed in detail. Meanwhile, experiments under diverse conditions are carried out to verify the effectiveness of the proposed strategies.

II. Modulation Strategy With Five Control Degrees of Freedom

The three-level (3L) neutral-point-clamped type (NPC) DAB converter is depicted in Fig. 1. Two 3L-NPC-type full bridges are introduced into the conventional 2L-DAB converter (Q_1 to Q_8 in the primary bridge and S_1 to S_8 in the secondary bridge). The turns ratio of the transformer is n:1, and L consists of both leakage inductance and extra inductance. In addition, the π model equivalent circuit is illustrated, where L_{P} and L_{S} represent the influence of the magnetizing branch on the primary and secondary sides, respectively. The inductance that transfers the power is L_{T}. Voltage gain G is defined as: $G = nV_{dc1}/V_{dc2}$, where V_{dc1} and V_{dc2} are the voltages between the primary side and the secondary side, respectively.

In the 3L-NPC-DAB converter, a modulation strategy with five DoFs (d_1, d_2, d_3, d_4, d_5) is implemented due to the

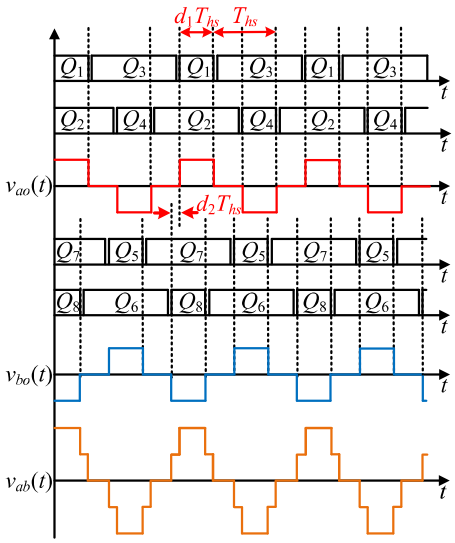

Fig. 2. Modulation strategy of the primary three-level H-bridge.

control degrees and the implementation complexity achieve a balance [18]. As illustrated in Fig. 2, take the primary bridge for example, there are two three-level legs v_{ao} and v_{bo}. They both have three output states: positive state (voltage is V), negative state (voltage is $-V$), and zero state (voltage is 0). In v_{ao}, the duration of the positive and negative states is identical and is modulated as d_1T_{hs}. d_2 is utilized to modulate the shift time between v_{ao} and v_{bo}, which is d_2T_{hs}. Similarly, on the secondary side, d_3T_{hs} and d_4T_{hs} represent the time of positive state (or negative state) and the shift time between v_{co} and v_{do}, respectively. d_5 is the control degree utilized to enable power flow between both sides of the converter, it controls the shift time between v_{ab} and v_{cd}. In this paper, d_5T_{hs} is defined as the time of v_{ab} leads v_{cd}. It should be noted that in order for both sides of the 3L-NPC-DAB converter ($v_{ab}\&v_{cd}$) have the desired five voltage levels, the following constraints must be met: $d_1 > d_2$ and $d_1 + d_2 \leq 1$ for the primary side; $d_3 > d_4$ and $d_3 + d_4 \leq 1$ for the secondary side. In addition, when the inner phase shift degrees ($d_2\&d_4$) are 0, the modulation is the same as the TPS control. Therefore, by adjusting the DoFs, the modulation state can be changed to SPS, DPS, or TPS control, as they are all special cases of the modulation strategy with 5 DoFs.

III. Switching Loss Imbalance Analysis and Strategy

A. Switching Loss Imbalance Analysis

In the modulation strategy applied in the 3L-NPC-DAB converter, as can be seen in Fig. 2, the leading leg and lagging leg are introduced to realize the inner phase shift. For the v_{ab}, the v_{bo} signal is the leading signal and that of v_{ao} is the lagging signal. Similarly, there are leading and lagging legs for the v_{cd} side to accomplish the inner phase shift as well.

For the primary side v_{ab}, which is shown in Fig. 3, the voltage changes from zero to V at t_1, Q_6 turns off and Q_8 turns on at this moment. When v_{ab} changes from V to $2V$ at t_2, Q_1 turns on and Q_3 turns off. Q_8 turns off and Q_6 turns on at t_3 when v_{ab} falls from $2V$ to V, and at t_4 when

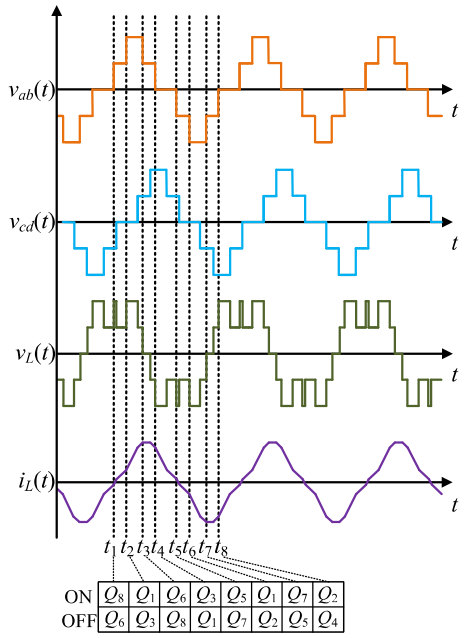

Fig. 3. Waveforms of the 3L-NPC-DAB with conventional modulation.

v_{ab} drops to zero, Q_1 turns off and Q_3 turns on. As can be observed, the magnitude of inductor current at t_1 and t_2 is different, hence the current flowing through the switch devices is not the same, leading to the switching losses of Q_1 and Q_8 are unbalanced. In addition, when Q_5 turns on and turns off at t_5 and t_7, the magnitude of the current flows through the switch devices is the same but the direction is the opposite with that of Q_8. Therefore, there are four pairs $Q_1\&Q_4$, $Q_5\&Q_8$, $Q_2\&Q_3$, and $Q_6\&Q_7$. In each pair, the two switch devices have the same switching loss. However, due to the leading and lagging signals, the switching losses of the pair $Q_5\&Q_8$ are unbalanced with $Q_1\&Q_4$. Similarly, the pairs $Q_2\&Q_3$ and $Q_1\&Q_8$ also have the switching loss imbalance.

By the same analysis, it could be obtained that in the secondary side of the 3L-NPC-DAB converter, the problem of switching loss imbalance also exists. In conclusion, $S_1\&S_4$ and $S_5\&S_8$ have the different switching losses, and $S_2\&S_3$ and $S_6\&S_7$ have the unbalanced switching losses as well. As the 3L-NPC-DAB converter has the characteristic of switching at high frequency, the switching loss imbalance is a problem that cannot be ignored and the losses generated by switch could account for a large proportion.

B. Switching Loss balance Strategy

A modulation strategy is proposed to solve the switching loss imbalance mentioned above in this paper. The leading leg and the lagging leg can alternate once two switching cycles, as shown in Fig. 4. The primary side is taken as the example and the driving signals are given. Q_1, Q_2, Q_3, Q_4 control the output waveform of v_{ao}. $Q_1\&Q_3$ are in a complementary state and the driving signals of $Q_2\&Q_4$ are also complement. $Q_1\&Q_4$ keeps in on-state for d_1T_{hs} to control positive state of v_{ao}. The durations of $Q_3\&Q_2$ alternate between $(2 - d_1 - d_2)T_{hs}$ and $(2 - d_1 + d_2)T_{hs}$ to realize the transition between leading state and lagging state. The

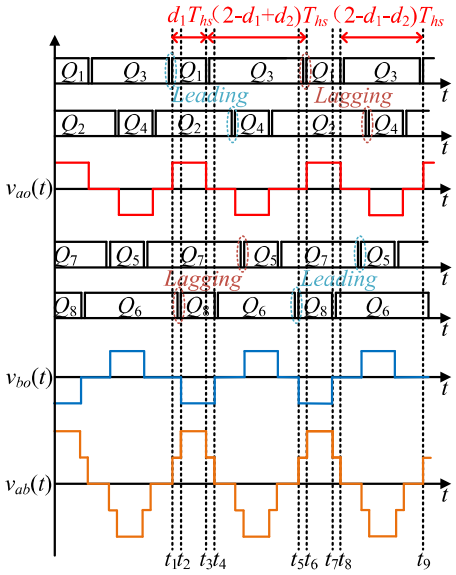

Fig. 4. Waveforms of the 3L-NPC-DAB with switching loss balance strategy.

interval between Q_1 and Q_4 is T_{hs}, which is the same as the conventional strategy.

From the previous analysis, after the v_{ab} dropped from v to 0 at t_4, the sum of current flowing through $Q_1(Q_3)$ and $Q_6(Q_8)$ are different, leading to the loss imbalances between switch devices. By applying the proposed strategy, the switching loss could be balanced. As can be observed, when at the moment Q_8 should have turned on at t_1, Q_1 turned on because the leading leg and the lagging leg have been alternated. As a result, the sum of switching losses is balanced in two switching periods. The strategy could also be applied to the secondary side of 3L-NPC-DAB to tackle the problem of switching loss imbalances. The output voltages v_{ab} and v_{cd} are unaffected when the traditional modulation is replaced with the proposed improved method.

IV. Transient DC-bias Analysis And Suppression Strategy

A. Transient DC-bias Analysis

From the π equivalent circuit in Fig. 1. The current through L_{T}, L_{P}, L_{S} are i_{LT}, i_{LP}, i_{LS}, and can be calculated as:

$$i_{\mathrm{LT}} = \frac{1}{L_{\mathrm{T}}}\int_0^t v_{ab}dt - \frac{n}{L_{\mathrm{T}}}\int_0^t v_{cd}dt \tag{1}$$

$$i_{\mathrm{LP}} = \frac{1}{L_{\mathrm{P}}}\int_0^t v_{ab}dt \tag{2}$$

$$i_{\mathrm{LS}} = \frac{1}{L_{\mathrm{S}}}\int_0^t v_{cd}dt \tag{3}$$

As seen in (1)-(3), the magnetizing current is proportional to the integrals of the voltages on the primary and secondary sides. If the volt-seconds are biased, the DC-bias is formed in the inductor current during the transient state.

Through the above analysis, we can analyze whether the 3L-NPC-DAB converter has the DC-bias issue by observing the integral of voltage on the primary and secondary sides at the transient state. There are two DoFs in each side, therefore

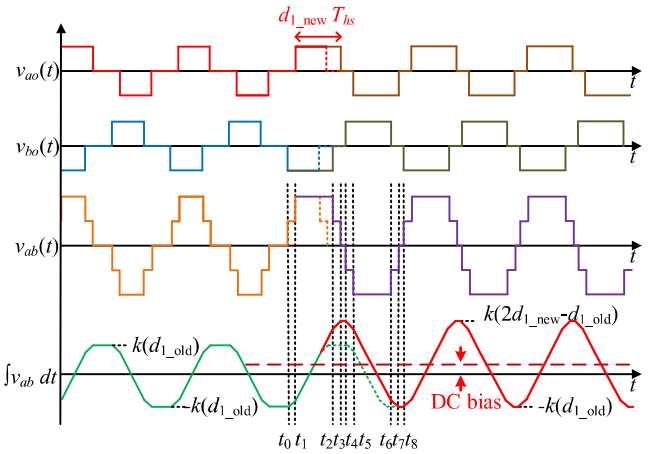

Fig. 5. Waveforms of the primary side without optimization strategy when d_1 changes.

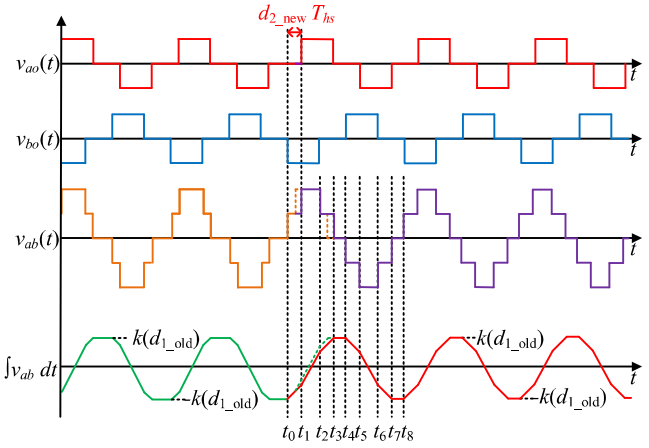

Fig. 6. Waveforms of the primary side without optimization strategy when d_2 changes.

numerous combinations of DoF modifications are possible. Since the analysis of both sides is identical, just the primary side is used as an illustration. When only d_1 has a change in a switching cycle, the waveforms of v_{ao}, v_{bo}, v_{ab} and the integral of v_{ab} are illustrated as Fig. 5 shows. In order to differentiate between the variables in the previous cycle and the current cycle, the subscripts old and new are used for the new and old values, respectively. As can be seen, after t_0, d_1 has a change from d_{1_old} to d_{1_new}, leading to a change of the integral, which changes from the bottom $-k(d_{1\_\mathrm{old}})$ at t_0 to the peak $k(2d_{1\_\mathrm{new}} - d_{1\_\mathrm{old}})$ at t_3, where k is $v/2f_s$. Therefore, a DC-bias of $2k(d_{1\_\mathrm{new}} - d_{1\_\mathrm{old}})$ is added to the volt-second on the primary side v_{ab} at the transient state. The integral of voltage will always have a DC-bias for the subsequent switching cycles unless d_1 changes back to its previous value. According to (1), it is known that the inductor current i_L will have a DC-bias and will continue to increase until it reaches the new set value d_{1_new} during the interval of updating d_1. In addition, although the transformer and switch devices have their own resistance and there is parasitic resistance in the circuit, the decay of the DC-bias still lasts for several switching cycles, increasing the risk of converter damage and limiting the converter's dynamic performance.

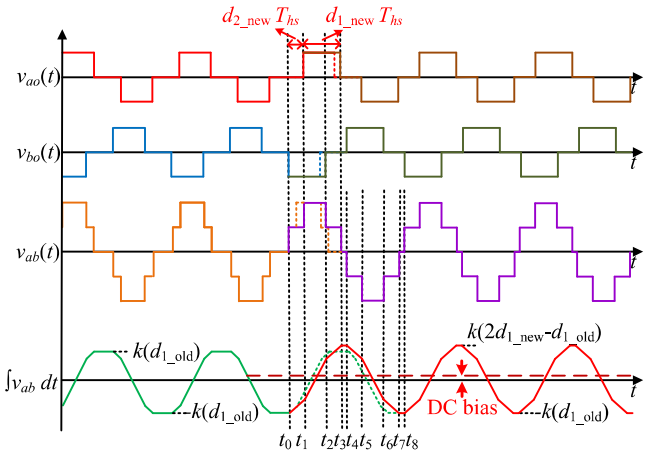

Fig. 7. Waveforms of the primary side without optimization strategy when d_1 and d_2 change.

In the scenario when just d_2 changes, the analysis is depicted in Fig. 6. As can be observed, after d_2 is updated at t_0, there is no DC-bias generated. In one switching cycle, the duration of v_{ab} at $2V$ is $(d_1 - d_2)T_{hs}$, while the duration at V is $2d_2T_{hs}$. Consequently, the increase in the integral of v_{ab} during one switching cycle is $2kd_1$, where k equals $v/2f_s$ and d_2 does not exist. Therefore, the DC-bias doesn't occur when only d_2 changes.

Fig. 7 depicts the waveforms of v_{ao}, v_{bo}, v_{ab} and the integral value of v_{ab} when both d_1 and d_2 change during a switching cycle. Before the values of d_1 and d_2 are updated, there is no DC-bias in the steady state and the integral ranges between $\pm k(d_{1\_\text{old}})$, where k is $v/2f_s$. After the transition at t_0, d_2 is updated from d_{2_old} to d_{2_new}, causing the zero-level duration of v_{ao} to undergo a change of time equal to $(d_{2\_\text{new}} - d_{2\_\text{old}})T_{hs}$. Additionally, the length of the v_{ao} in positive state is updated from $d_{1\_\text{old}}T_{hs}$ to $d_{1\_\text{new}}T_{hs}$. For the waveform of v_{bo}, as seen by the integral of v_{ab}, the value before the transition ranges between $\pm k(d_{1\_\text{old}})$ without any DC-bias. The volt-second then growes from the bottom $-k(d_{1\_\text{old}})$ at t_0 to the peak $k(2d_{1\_\text{new}} - d_{1\_\text{old}})$ at t_3, resulting in a DC-bias of $k(2d_{1\_\text{new}} - 2d_{1\_\text{old}})$ being introduced into the primary side voltage v_{ab}. Therefore, the DC-bias only occur in the primary side when d_1 has a change, and not affected by the change of d_2.

The variable d_5 determines the phase shift angle between v_{ab} and v_{cd}, which can adjust the amount of transmission power. During the transition period, the change in d_5 could be accomplished by extending its zero-state duration. Extending the length of the zero-state of v_{cd} could result in the reduction of d_5. Due to the fact that extending the zero-state duration has no effect on the integral of the voltage v_{ab} or v_{cd}, the update of d_5 will not introduce any DC-bias. According to Fig. 8, d_5 increases from d_{5_old} to d_{5_new} at t_4. Before the transition, the integral of v_{ab} ranges between $\pm k(d_1)$ and the duration of zero-state is $(1 - d_1 - d_2)T_{hs}$. After the transition, the duration of zero-state extends to $(1 - d_1 - d_2 + d_{5\_\text{new}} - d_{5\_\text{old}})T_{hs}$, whereas the integral of v_{ab} remains unchanged. Therefore, the modification of d_5 does not introduce the DC-bias issue.

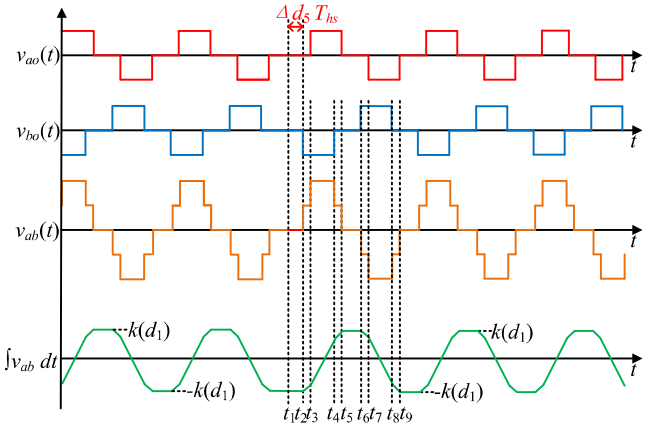

Fig. 8. Waveforms of the primary side without optimization strategy when d_5 changes.

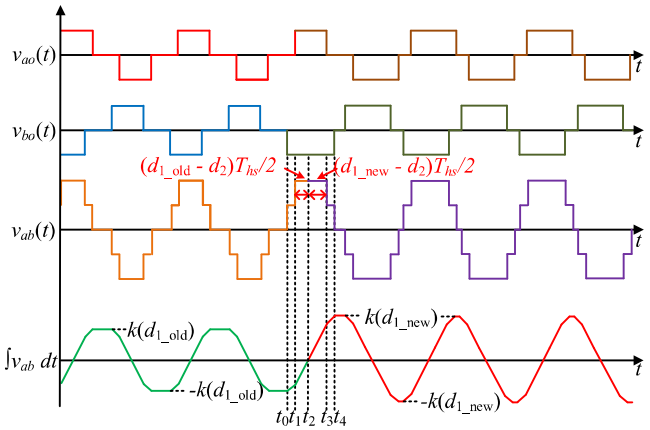

Fig. 9. Waveforms of the primary side with proposed DC-bias suppression strategy when d_1 changes.

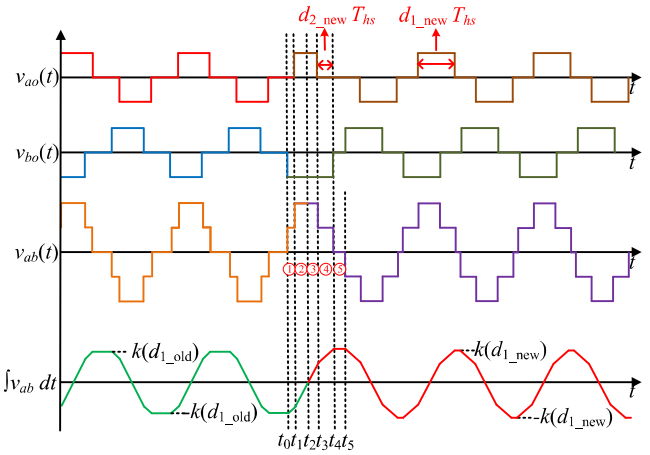

Fig. 10. Waveforms of the primary side with proposed DC-bias suppression strategy when d_1 and d_2 change.

B. Transient DC-bias Suppression Strategy

This subsection describes how to eliminate DC-bias issues during transient processes. The above analysis reveals that the DC-bias arises during the switching cycle when d_1 or d_3 undergo a change. Fig. 9 depicts the suppression strategy of DC-bias when d_1 changes. In the steady state before v_{ab} is updated, the duration of the voltage v_{ab} at V and $-V$ is the

same, and the time at $2V$ and $-2V$ is the same as well, so the integral of voltage is always symmetric about zero and no DC-bias is formed. During the interval of updating d_1, the integral of voltage rises from its minimum value of $-k(d_{1\_\text{old}})$ to its maximum value of $2k(d_{1\_\text{new}} - d_{1\_\text{old}})$, resulting in the DC-bias. In order to eliminate the extra rise time, the rise interval could be divided into two parts. The first part is the period before the integral approaches zero. In this part, d_1 is taken to be d_{1_old}, so the negative integral in this period is symmetrical with the last positive voltage integral. In the second part, when the integral is greater than zero, the value of d_1 is d_{1_new}, then the time required to ascend after the integral is greater than zero is still half of the entire time that should have been required. Thus, there will be no DC-bias, and the absolute value of positive and negative integrals of v_{ab} will remain the same even if d_1 is changed.

The approach to eliminate the DC-bias introduced by adjusting $d_1\&d_2$ is depicted in Fig. 10. In the switching cycle of the transition, the period of time during which the integral climbs from the bottom to the peak can be divided into five parts which are labeled in the figure. Before the integral value reaches to zero, there are two parts, and they are the same with the waveforms before the transition. The duration of the first part is $(d_{2\_\text{old}})T_{hs}$, while the duration of the second part is $(d_{1\_\text{old}} - d_{2\_\text{old}})T_{hs}/2$. After the integral value of v_{ab} reaches zero, there are three parts. Before t_4, the third part's duration is $(d_{1\_\text{new}} - d_{2\_\text{new}})T_{hs}/2$. The time of the part four is $(d_{2\_\text{new}})T_{hs}$. In addition, the fifth part has a time of $(2 - d_{1\_\text{old}} - d_{2\_\text{old}} - d_{1\_\text{new}} - d_{2\_\text{new}})T_{hs}/2$. A special case should be noted that if $(d_{1\_\text{old}} + d_{2\_\text{old}} + d_{1\_\text{new}} + d_{2\_\text{new}})T_{hs}/2$, the sum of the durations of parts 1,2,3 and 4 is greater than $(d_{1\_\text{new}})T_{hs}$. Then, the duration of the voltage v_{bo} should be kept longer than $(d_{1\_\text{new}})T_{hs}$ and be modified to equal the total of the durations of parts 1,2,3 and 4. The leading leg v_{bo} will keep the negative state for the time of $(d_{1\_\text{old}} + d_{2_\text{old}} + d_{1\_\text{new}} + d_{2\_\text{new}})T_{hs}/2$. Consequently, when the proposed strategy is implemented, the integral value reaches zero at t_3, then the value is zero after every switching cycle and without any DC-bias. The integral of the v_{ab} varies between $\pm k(d_{1\_\text{new}})$.

V. PWM Generation Control Technique

In this section, the PWM generation technique will be introduced to suppress the switching loss imbalance and the DC-bias generated by transient state changes in the 3L-NPC-DAB converter.

The simplified control diagram of the proposed switching loss balance & DC-bias suppression strategy is illustrated in Fig. 11. According to the applied optimization objective and reference power, after receiving the input voltage and output voltage, the control module transmits the old-state and new-state values of the five DoFs to the FPGA device.

A straw wave carrier is generated in the FPGA device and its maximum count is $T_s + \delta d_5 T_{hs}$, which corresponds to one switching cycle in the modulation strategy. After obtaining the five control degrees of freedom d_1-d_5, two

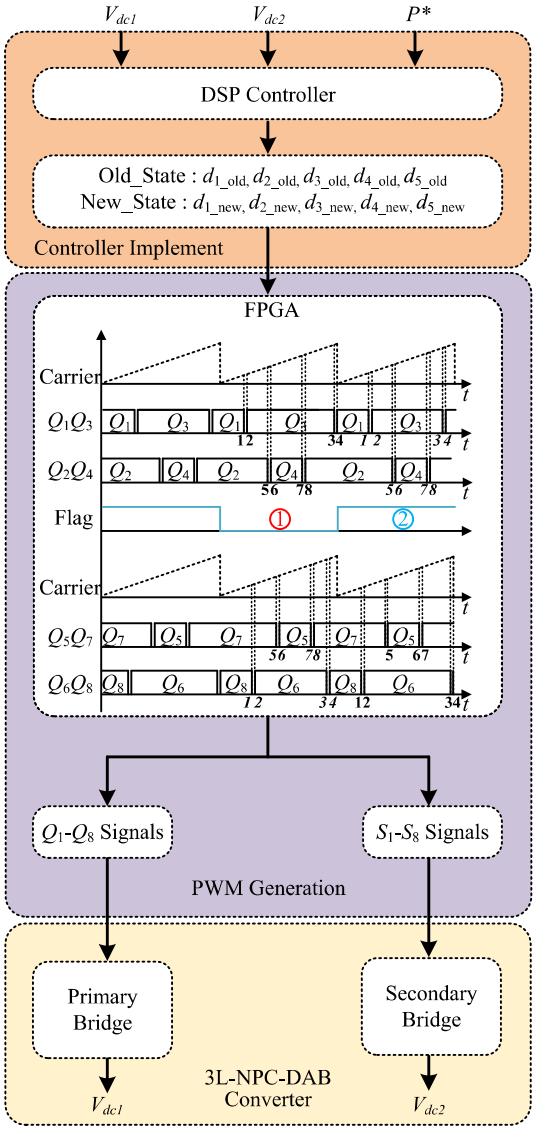

Fig. 11. Control structure of the 3L-NPC-DAB converter.

additional variables δd_5 and d_{2_T} will be calculated. δd_5 may be different between the two bridges. In the primary bridge, if $d_{5\_\text{new}} - d_{5\_\text{old}} > 0$, then $\delta d_5 = d_{5\_\text{new}} - d_{5\_\text{old}}$, otherwise equals 0. In the secondary bridge, if $d_{5\_\text{new}} - d_{5\_\text{old}} < 0$, then $\delta d_5 = d_{5\_\text{old}} - d_{5\_\text{new}}$, otherwise equals to 0. The value of d_{2_T} will be determined by (4).

$$d_{2\_\text{T}} = \begin{cases} d_{2\_\text{new}}, & |d_{1\_\text{new}} - d_{1\_\text{old}}| \neq 0 \\ -d_{2\_\text{new}}, & |d_{1\_\text{new}} - d_{1\_\text{old}}| = 0 \end{cases} \tag{4}$$

There are sixteen comparators calculated from (5)-(6) through the analysis in section IV, the comparators are divided into two sets for the two bridges. The dead time between two switches is defined as DT. A flag is utilized to solve the problem of switching loss imbalance. As shown in Fig. 11, for the primary side, when the flag is 1, CMP*1*-CMP*4* are adopted to generate the signals of $Q_1\&Q_3$, and CMP*5*-CMP*8* are adopted to generate the signals of $Q_2\&Q_4$. Then the waveform of v_{ao} is generated. For the waveform of v_{bo}, CMP1-CMP4 are used for the signals of $Q_5\&Q_7$, and CMP5-CMP8 are used for $Q_6\&Q_8$. On the contrary, when the flag is 2, $Q_1\&Q_3$ utilize CMP*5*-

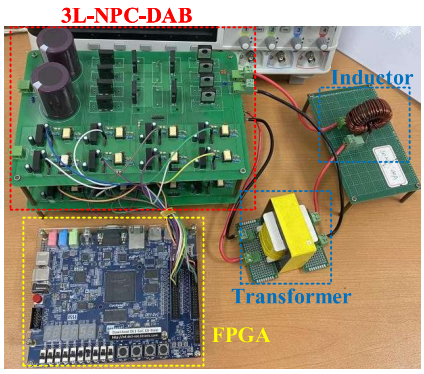

Fig. 12. Prototype of the 3L-NPC-DAB converter.

TABLE I
MAIN PARAMETERS OF THE 3L-NPC-DAB CONVERTER.

Parameter	Symbol	Device or Value
Primary bus voltage	V_{dc1}	80V-100V
Secondary bus voltage	V_{dc2}	64V-80V
Transformer turns ratio n	$n:1$	1
Switching frequency	f_s	20kHz
Inductor	L_s	60μH
Input and output capacitor	$C_{in1}, C_{in2}, C_{o1}, C_{o2}$	470μF
Deadtime	DT	20μs
Switch tube	$Q_1 - Q_8, S_1 - S_8$	APT40GP90B2DQ2G
Diode	$D_1 - D_8$	RURG80100

CMP*8* and Q_2&Q_4 utilize CMP*1*-CMP*4*; Q_5&Q_7 utilize CMP5-CMP8 and Q_6&Q_8 utilize CMP1-CMP4.

$$\begin{cases} \text{CMP}1 = (d_{1\_\text{old}} + d_{1\_\text{new}} - d_{2\_\text{old}} - d_{2\_\text{T}})T_{hs}/2 \\ \text{CMP}2 = (d_{1\_\text{old}} + d_{1\_\text{new}} - d_{2\_\text{old}} - d_{2\_\text{T}})T_{hs}/2 + DT \\ \text{CMP}3 = (2 - d_{2\_\text{new}} + \delta d_5)T_{hs} - DT \\ \text{CMP}4 = (2 - d_{2\_\text{new}} + \delta d_5)T_{hs} \\ \text{CMP}5 = (1 + \delta d_5)T_{hs} - DT \\ \text{CMP}6 = (1 + \delta d_5)T_{hs} \\ \text{CMP}7 = (1 + d_{1\_\text{new}} + \delta d_5)T_{hs} \\ \text{CMP}8 = (1 + d_{1\_\text{new}} + \delta d_5)T_{hs} + DT \end{cases} \tag{5}$$

$$\begin{cases} \text{CMP}1 = (d_{1\_\text{old}} + d_{1\_\text{new}} - d_{2\_\text{old}} + d_{2\_\text{T}})T_{hs}/2 \\ \text{CMP}2 = (d_{1\_\text{old}} + d_{1\_\text{new}} - d_{2\_\text{old}} + d_{2\_\text{T}})T_{hs}/2 + DT \\ \text{CMP}3 = (2 + \delta d_5)T_{hs} - DT \\ \text{CMP}4 = (2 + \delta d_5)T_{hs} \\ \text{CMP}5 = (1 - d_{2\_\text{new}} + \delta d_5)T_{hs} - DT \\ \text{CMP}6 = (1 - d_{2\_\text{new}} + \delta d_5)T_{hs} \\ \text{CMP}7 = (1 + d_{1\_\text{new}} + d_{2\_\text{new}} + \delta d_5)T_{hs} \\ \text{CMP}8 = (1 + d_{1\_\text{new}} + d_{2\_\text{new}} + \delta d_5)T_{hs} + DT \end{cases} \tag{6}$$

VI. Experiment Verification

In this section, the experimental results are shown to verify the effectiveness of the proposed strategies. The 3L-NPC-DAB converter prototype is fabricated with the main parameters listed in TABLE I, and the photograph is shown in Fig. 12.

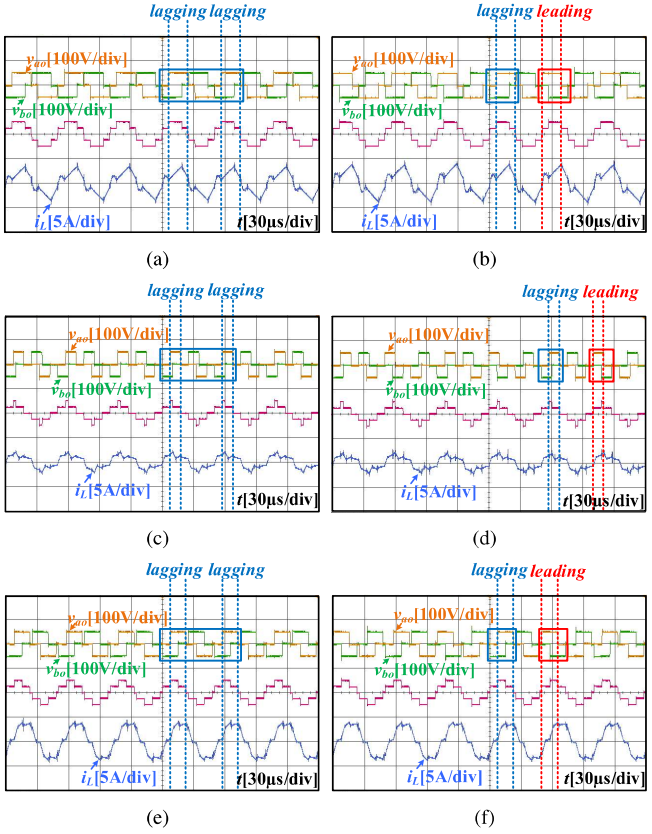

Fig. 13. Experimental results of waveforms under conventional control and switching loss balance control. (a) Case 1 under conventional control. (b) Case 1 under switching loss balance control. (c) Case 2 under conventional control. (d) Case 2 under switching loss balance control. (e) Case 3 under conventional control. (f) Case 3 under switching loss balance control.

A. Verification Of Switching Loss Balance Strategy

This subsection verify the effectiveness of switching loss balance strategy by comparing it with the conventional modulation.

Fig. 13 shows three cases of v_{ao}, v_{bo}, v_{ab}, and i_L under conventional control and switching loss balance control. In case 1, d_1, d_2, d_3, d_4, d_5 are 0.7, 0.2, 0.6, 0.1, 0.08. In cases 2 and 3, the corresponding values are 0.4, 0.3, 0.4, 0.2, 0.06; and 0.6, 0.3, 0.5, 0.3, 0.08. Fig. 13(a) displays waveforms of the primary side under conventional control, v_{ao} is always the lagging one compared with v_{bo}. In every switching cycle, Q_1 turns on and Q_3 turns off under 0.75A. Q_1 turns on and Q_3 turns off under 4.125A; Q_4 turns on and Q_2 turns off under 0.75A. Q_2 turns on and Q_4 turns off under 1A. After applying the switching balance strategy, as shown in Fig. 13(b), v_{ao} and v_{bo} alternate with each other in the leading every switching cycle. Q_1 turns on and Q_3 turns off under 4.125A when v_{ao} is lagging and under 0.75A when v_{ao} is leading, resulting in the switching loss balance. In Fig. 13(c)-Fig. 13(f), switching loss balance are achieved by alternating the leading leg and lagging leg.

The switching loss of one MOSFET could be calculated as

$$P_{sw} = \frac{1}{2} V_{sw} I_{sw} (t_{on} + t_{off}) f_{sw}, \tag{7}$$

where V_{sw} and I_{sw} are transition voltage and current of

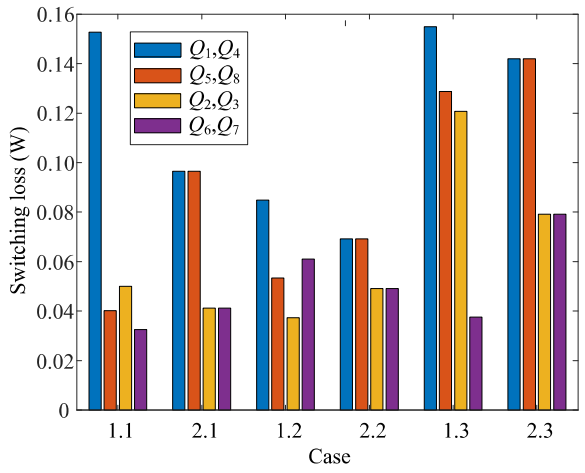

Fig. 14. Switching losses of switch devices in the primary side under different cases. Case1.1: Case 1 under conventional control. Case2.1: Case 1 under switching loss balance control. Case1.2: Case 2 under conventional control. Case2.2: Case 2 under switching loss balance control. Case1.3: Case 3 under conventional control. Case2.3: Case 3 under switching loss balance control.

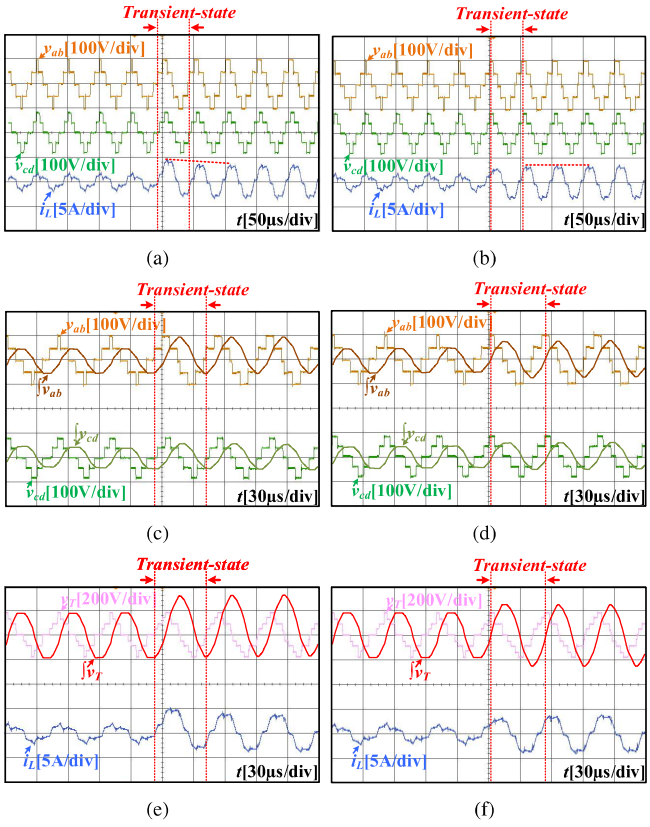

Fig. 15. Experimental results of Case 4 under power increase condition. (a) v_{ab}, v_{cd}, i_L with conventional control. (b) v_{ab}, v_{cd}, i_L with proposed strategy. (c) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with conventional control. (d) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with proposed strategy. (e) v_T, $\int v_T$, i_L with conventional control. (f) v_T, $\int v_T$, i_L with proposed strategy.

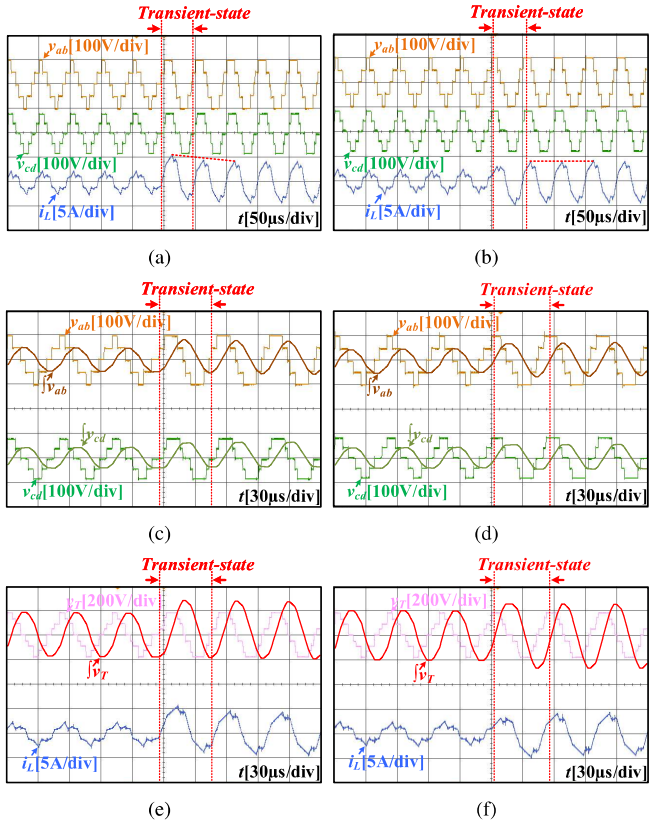

Fig. 16. Experimental results of Case 5 under power increase condition. (a) v_{ab}, v_{cd}, i_L with conventional control. (b) v_{ab}, v_{cd}, i_L with proposed strategy. (c) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with conventional control. (d) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with proposed strategy. (e) v_T, $\int v_T$, i_L with conventional control. (f) v_T, $\int v_T$, i_L with proposed strategy.

MOSFET, respectively; t_{on} and t_{off} are the time during ON and OFF; f_{sw} is the switching frequency.

Through (7), the switching loss of every MOSFET in the primary side of 3L-NPC-DAB converter could be calculated as shown in Fig. 14. As can be observed, in case 1, Q_1 and Q_4 both have large switching loss of 0.152W under conventional control, which is nearly four times as that of Q_5 and Q_8. After applying switching loss balance strategy, Q_1,Q_2,Q_3,Q_4 have the same switching loss of 0.096W, Q_1 and Q_4 no longer bear the major switching losses of the system and enhance the system reliability, solving the problem of different expected service life time of switch devices. Similarly, In case2 and case3, switching loss unbalance is suppressed by introducing the proposed strategy.

B. Verification Of Transient DC-bias Suppression Strategy

In this subsection, the proposed transient DC-bias suppression strategy is verified under various conditions.

Fig. 15 shows the experimental results of case 4 where transmission power has an increase with conventional modulation and the proposed strategy. In this case, v_{ab} is 80V, v_{cd} is 64V. The old-state phase ratios are $d_{1\_\text{old}} = 0.4$, $d_{2\_\text{old}} = 0.3$, $d_{3\_\text{old}} = 0.4$, $d_{4\_\text{old}} = 0.2$, $d_{5\_\text{old}} = 0.06$; the new-state phase ratios are $d_{1\_\text{new}} = 0.6$, $d_{2\_\text{new}} = 0.3$, $d_{3\_\text{new}} = 0.5$, $d_{4\_\text{new}} = 0.3$, $d_{5\_\text{new}} = 0.17$. On the primary side, d_1 has an increase while d_2 has no change. On the

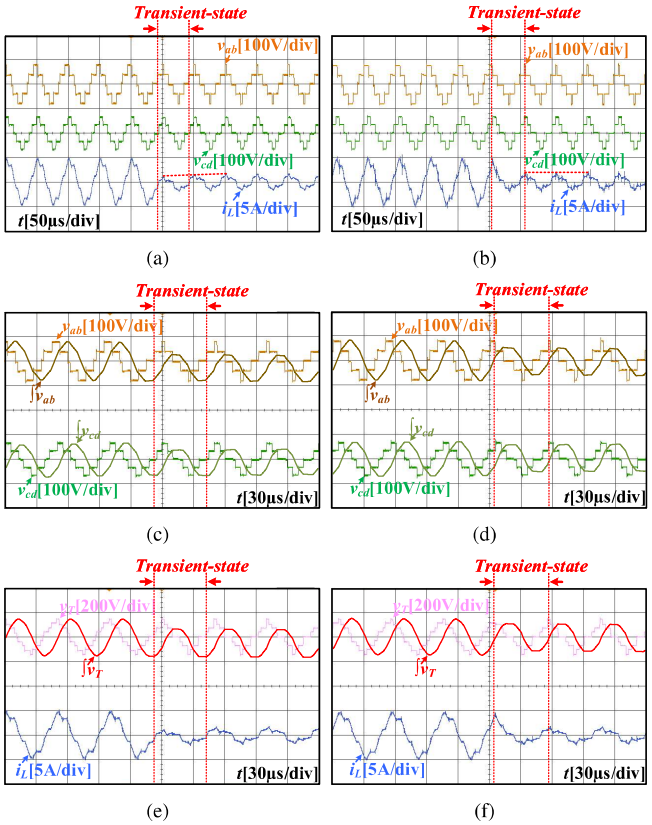

Fig. 17. Experimental results of Case 6 under power decrease condition. (a) v_{ab}, v_{cd}, i_L with conventional control. (b) v_{ab}, v_{cd}, i_L with proposed strategy. (c) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with conventional control. (d) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with proposed strategy. (e) v_T, $\int v_T$, i_L with conventional control. (f) v_T, $\int v_T$, i_L with proposed strategy.

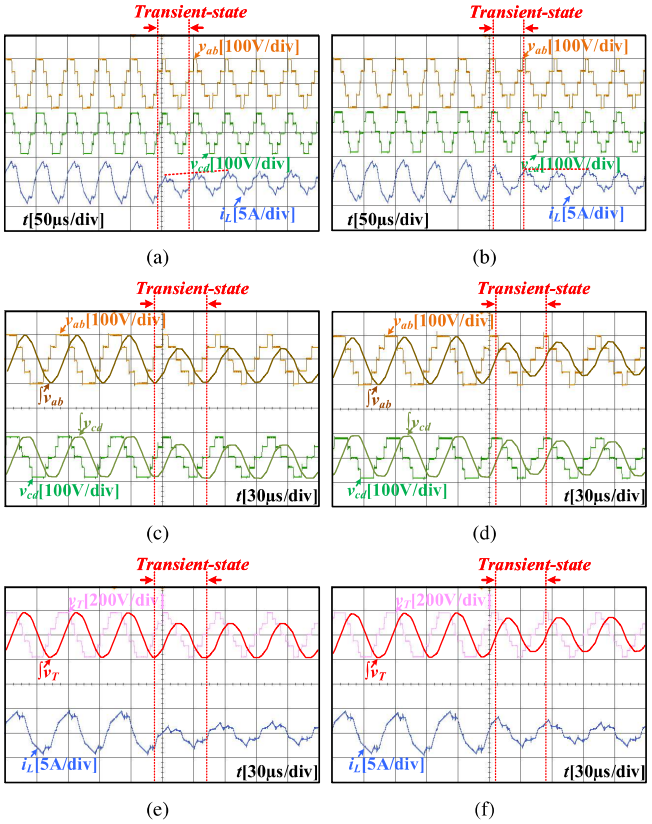

Fig. 18. Experimental results of Case 7 under power decrease condition. (a) v_{ab}, v_{cd}, i_L with conventional control. (b) v_{ab}, v_{cd}, i_L with proposed strategy. (c) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with conventional control. (d) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with proposed strategy. (e) v_T, $\int v_T$, i_L with conventional control. (f) v_T, $\int v_T$, i_L with proposed strategy.

secondary side, both d_3 and d_4 have an increase. Obviously, when employing the conventional modulation, the measured current stress has a DC-bias, as shown by the red dashed line in Fig. 15(a). And it decays after several switching cycles. As can be seen from Fig. 15(b), there is no DC-bias following the transient modulation cycle. In Fig. 15(c). The waveforms of v_{ab}, v_{cd} and their integral values $\int v_{ab}$, $\int v_{cd}$ are given. The integral values are calculated by the data derived from the oscilloscope. As the same with the analysis in the section IV, both the integrals of v_{ab} and v_{cd} have the DC-bias after the direct change without transient optimization. And by using the proposed strategy, the integral values do not have any DC-bias after the transient cycle. Moreover, sometimes the DC-bias of the integral of v_{ab} and v_{cd} may cancel out part or all their influence on the current stress, so that the DC-bias in the current stress is not obvious or disappears. However, DC-bias continues to be a concern in the magnetizing branch [19]. As illustrated in Fig. 15(e), v_T is the voltage between high-voltage ports of the transformer, there is no DC-bias in $\int v_T$ before the transient state, but after the transient state without any transient optimization, there is an obvious DC-bias in $\int v_T$. It could possibly cause transformer damage by saturating the transformer. Fig. 18(f) shows the experiment results of the same power change with the proposed strategy. The integral of v_T has no DC-bias after the transition cycle, and the risk of the damage to the transformer is eliminated.

In case 5, the change of the control variables is the inverse of case 4, and the power has a decrease. In this case, v_{ab} is 80V while v_{cd} is 64V. d_1, d_2, d_3, d_4, d_5 change from 0.6, 0.3, 0.5, 0.3, 0.17 to 0.4, 0.3, 0.4, 0.2, 0.06. As seen in Fig. 16, the DC-bias occurs following the transient state in the current with conventional modulation. Although the DC-bias in the current stress is not as obvious as in case 4, the severe unbalance in the integrals of v_{ab} and v_{cd} leads to an obvious DC-bias in the integral of v_T. By using the proposed strategy, there is no DC-bias in the current after the transient state, and the volt-seconds of v_{ab} and v_{cd} are balanced, resulting in the elimination of DC-bias in the integral of v_T and confirming the effectiveness of the proposed strategy.

Fig. 17 shows the case 6 where transmission power has an increase with conventional modulation and the proposed strategy. In this case, v_{ab} is 100V and v_{cd} is 80V. d_1, d_2, d_3, d_4, d_5 change from 0.5, 0.3, 0.5, 0.2, 0.06 to 0.7, 0.2, 0.6, 0.1, 0.08. For the primary and secondary sides, d_1&d_3 have an increase while d_2&d_4 have a decrease. Observable DC-bias in the current is generated by using the conventional modulation. The volt-seconds of v_{ab} and v_{cd} are unbalanced and there is a positive DC-bias introduced in the integral of v_T after the transient state. Fig. 20(d) shows there is no DC-bias in the current and the integral of v_T is balanced after the transient state. Fig. 18 shows the experimental results of case 7, where the change of control variables is the inverse of case

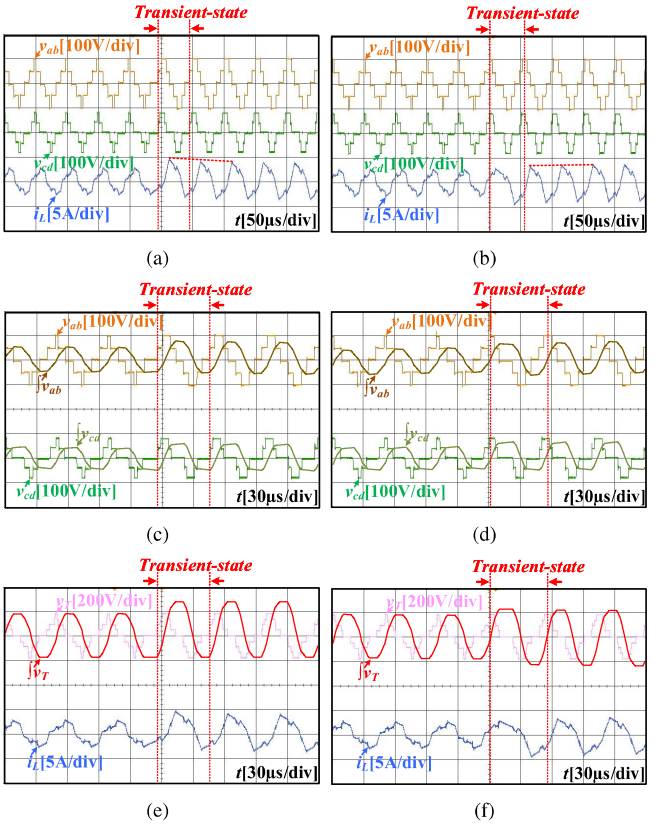

Fig. 19. Experimental results of Case 8 under power reverse condition. (a) v_{ab}, v_{cd}, i_L with conventional control. (b) v_{ab}, v_{cd}, i_L with proposed strategy. (c) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with conventional control. (d) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with proposed strategy. (e) v_T, $\int v_T$, i_L with conventional control. (f) v_T, $\int v_T$, i_L with proposed strategy.

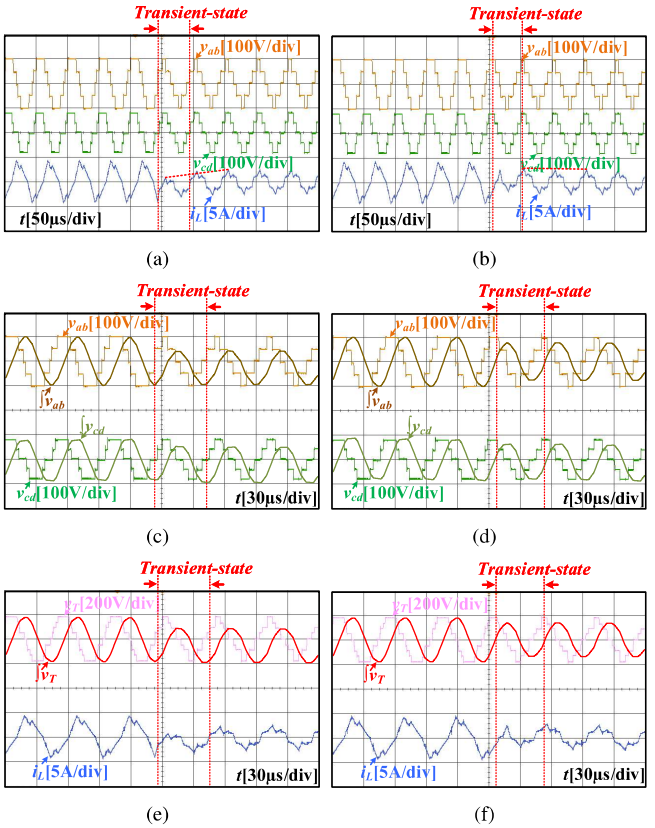

Fig. 20. Experimental results of Case 9 under power reverse condition. (a) v_{ab}, v_{cd}, i_L with conventional control. (b) v_{ab}, v_{cd}, i_L with proposed strategy. (c) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with conventional control. (d) v_{ab}, v_{cd}, $\int v_{ab}$, $\int v_{cd}$ with proposed strategy. (e) v_T, $\int v_T$, i_L with conventional control. (f) v_T, $\int v_T$, i_L with proposed strategy.

6. Similarly, a DC-bias is introduced into the inductor current and the integral of v_T by using the conventional modulation. The DC-bias in the current and the integral of v_T could be mitigated with the proper adjustment.

Fig. 19 shows the experiment results for case 8 under different modulation strategies. In this case, the transmission power changes from forward 40W to reverse 50W, v_{ab} is 100V, and v_{cd} is 80V. The old-state phase ratios are $d_{1\_\text{old}} = 0.4$, $d_{2\_\text{old}} = 0.3$, $d_{3\_\text{old}} = 0.4$, $d_{4\_\text{old}} = 0.2$, $d_{5\_\text{old}} = 0.03$; the new-state phase ratios are $d_{1\_\text{new}} = 0.5$, $d_{2\_\text{new}} = 0.2$, $d_{3\_\text{new}} = 0.4$, $d_{4\_\text{new}} = 0.1$, $d_{5\_\text{new}} = -0.08$. The experiment results for case 9 are illustrated in Fig. 20, the transmission power changes from reverse 81W to forward 72W. The phase ratios d_1, d_2, d_3, d_4 change as the same with the case 7, while d_5 is updated from -0.08 to 0.06. In these two power reverse cases, sever DC-bias is observed in current stress, $\int v_{ab}$, $\int v_{cd}$, and $\int v_T$ when using conventional modulation. Due to a relatively large loop resistance in the experimental prototype, the envelope of the inductor peak current is seen to go down for approximately three cycles until the average inductor current becomes zero. The loop resistance can be lowered by improving the hardware design, resulting in a longer transient settling period. Even in this scenario with a large loop resistance, the proposed strategy still be effective. The settling time is shortened from three cycles to one cycle. The results show the proposed DC-bias suppression strategy is also capable of eliminating DC-bias for reverse power changes with fast response.

VII. Conclusion

In this paper, a switching loss balance strategy and a DC-bias suppression strategy are introduced into the 3L-NPC-DAB converter modulated with 5 DoFs. First, the causes of unbalanced switching loss and transient DC-bias are studied, and then the proposed switching loss balancing strategy and DC-bias suppression strategy are presented. Specifically, switching loss balance is achieved by alternating the leading leg and lagging leg every two switching cycles. DC-bias issues are suppressed by eliminating the DC-bias in the integral of v_{ab} and v_{cd} in one switching cycle, and the problem of DC-bias occurring on magnetizing branches is eliminated as well. In addition, the strategy is general and can be applied in other conventional modulations. A PWM generation technique is introduced in detail to combine the two proposed strategies at the same time without any extra components. Main experiment results on the prototype under different conditions are given to verify the effectiveness of the proposed switching loss balance strategy and DC-bias suppression strategy. Finally, on each side of the 3L-NPC-DAB converter, there is no switch device facing much higher switching loss than other devices. The transient DC-bias could be suppressed in power increase, decrease, and reverse conditions.

VIII. Acknowledgement

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