A Monolithic GaN Driver with A Deadtime Generator (DTG) for High-Temperature (HT) GaN DC-DC Buck Converters

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Abstract: This paper presents a monolithic GaN driver with a deadtime generator (DTG) for half-bridge DC-DC buck converters. The proposed GaN integrated circuits (ICs) were fabricated in a 3 µm enhancement-mode GaN MIS-HEMTs process. The integrated DTG converter can operate at 250 ℃ with a large gate swing of 10 V, and it exhibits a maximum efficiency of 80 % at high temperatures, with V_{IN}=30 V at 100 kHz. The monolithic GaN DTG driver requires one control signal and generates a deadtime of fewer than 0.13 µs at high temperatures up to 250 ℃. The proposed DTG converter is compared to an integrated GaN converter without DTG (w/o) under various conditions. At high temperatures, the optimized GaN DTG converter shows better performance than the GaN converter w/o at high load currents, in terms of smaller voltage overshoots and better efficiency as well. This work demonstrates a simple GaN deadtime method for high temperature (HT) GaN power converters.

1. Introduction

High temperature (HT) power converters are increasingly required in harsh-environments applications such as deep earth, automotive, avionics, aerospace, and industrial measurement [1, 2]. In a high-temperature environment, the external cooling system is required to ensure the safe operation of power converters, but it increases the cost, volume, and weight of the converters. Therefore, power electronics with intrinsic high-temperature tolerance would be preferred. Due to the limited temperature operation (<150 ℃) of Si-based devices, the wide bandgap (WBG) semiconductors (GaN and SiC) are excellent candidates for HT power converters. Most reported HT converters are based on SiC devices but are limited to power modules with discrete components like gate drivers and controllers [3-12]. By contrast, there are seldom studies about HT GaN converters. However, the monolithic integration of GaN power converters stimulates tremendous industry and research interest in the reduced volume as well as the cost of an additional cooling system. Our previous work [13, 14] demonstrated the monolithic integration of GaN converters with gate drivers at high temperatures up to 250 ℃.

In half-bridge power converters, deadtime is essential to avoid simultaneous conduction between the high-side power transistor and the low-side synchronous rectifier. Fixed deadtime control is widely used in many power converters, ascribed to its simplicity of control [15]. Various model-based adaptive deadtime control methods for GaN converters were reported to optimize deadtime and improve the converter efficiency [16-19]. Advanced techniques were developed to optimize deadtime on the gate driver side owing to self-switching techniques. An adaptive deadtime controller in a 0.35 µm CMOS process was implemented for normally-off GaN power converters [20]. An all-digital deadtime correction was designed for E-mode GaN HEMT converters [21]. A gate driver with an integrated deadtime controller was reported based on SiC JFETs and GaN HEMTs converters, and the auto-adaptive management detects reverse conduction by gate-drain capacitance [22]. An adaptive deadtime controller with a 5-bit delay cell was proposed in a 0.18 µm BCD process, and the proposed circuit optimized deadtime in a wide loading range [23]. An adaptive deadtime controller with three-level gate drivers was reported to achieve near-optimal zero-voltage switching in a 0.18 µm BCD process [24]. However, most of these techniques are based on external deadtime management or Si-based integrated circuits. One recent GaN-based driver uses a diode-emulated GaN technique to minimize the deadtime loss at room temperature [25]. The reports about GaN-based deadtime management on an integration level are still lacking, especially for high-temperature operations. For extreme environments where temperature tolerance is over 200 ℃, an all-GaN method is required to manage deadtime in achieving small chip size and self-contained functionality without external heatsink or cooling systems. This work proposes an integrated GaN-based driver with a deadtime generator (DTG) for HT GaN converters.

In this work, an integrated GaN driver with a deadtime generator is experimentally demonstrated, and the integrated GaN DTG converter shows a maximum efficiency of 80 % at 250 ℃ at 100 kHz. Unlike Si CMOS technology, the lack of high-performance p-channel GaN devices has been the major obstacle to implementing GaN-based CMOS integrated circuits (ICs). NMOS logic circuits have the advantage of small chip areas. GaN-based logic circuits with integrated enhancement/depletion n-channel devices were reported on the integration platform [26-31]. The GaN deadtime generation circuit consists of inverters, NAND gates, and NOR gates. This circuit is based on a Si-based deadtime generator [21] using two inverter delay chains to generate two

complementary signals with a small deadtime. The proposed GaN DTG converter is compared with an integrated GaN converter w/o under various load conditions. The two converters show a comparable maximum efficiency of 80 % at high temperatures, indicating good advantages of GaN MIS-HEMT based power ICs for HT power converters. Especially at large load currents, the proposed GaN DTG converter shows better efficiency compared with the GaN converter without DTG. The results in this work provide a simple deadtime-management method with only one control signal for HT power converters, which benefits applications under extreme environments.

2. Fabrication and device characterization

The lateral AlGaN/GaN heterostructure generates two-dimensional electron gas (2DEG) at the interface, featuring a depletion-mode (D-mode) device. Enhancement (E-) mode devices in this work were achieved by etching the barrier to remove the 2DEG channel under the gate electrode, with an MIS (metal-insulator-semiconductor) gate technique to enlarge the gate swing. The GaN integrated circuits were fabricated on a commercial GaN-on-Si substrate. The n-MOS GaN technology was used to monolithically integrate D-mode and E-mode MIS-HEMTs, as shown in Fig. 1. The detailed fabrication process of the GaN ICs was introduced in previous research [14].

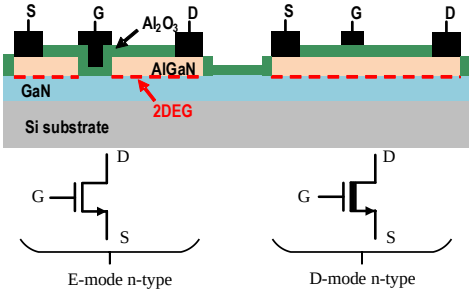

Fig. 1. *Cross-section of monolithic integration of E-mode and D-mode MIS-HEMTs.*

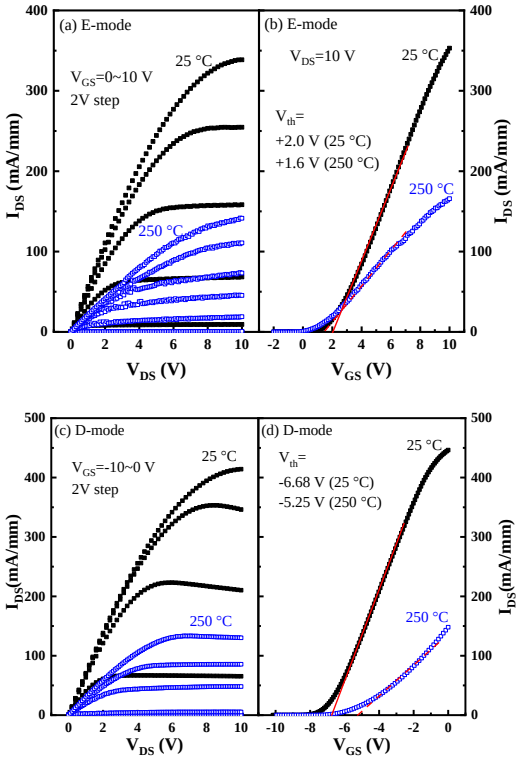

Fig. 2. *Output and transfer characteristics of E-mode MIS-HEMTs (a) and (b), D-mode MIS-HEMTs (c) and (d) at 25 ℃ and 250 ℃, respectively. (Device dimension: L_{GS}/ W_G/ L_G/ L_{GD}=5/50/3/10 μm).*

Fig. 2 shows the DC characteristic of discrete E-mode and D-mode devices, which were fabricated on the same chip with GaN ICs. All devices have the same gate length L_G=3 μm, gate-to-source distance L_{GS}=5 μm, and gate-to-drain distance L_{GD}=10 μm. At 25 °C, the threshold voltage (V_{th}) and the maximum drain current ($I_{DS,max}$) are +2.0 V and 330 mA/mm for E-mode devices, -6.68 V and 420 mA/mm for D-mode devices, respectively. At 250 °C, the V_{th} and $I_{DS,max}$ are +1.6 V and 140 mA/mm for E-mode devices, and -5.25 V and 133 mA/mm for D-mode devices, respectively. The results in Fig. 2 indicate a large gate swing of 10 V for both D-mode and E-mode devices at high temperatures up to 250 °C, owing to the recessed MIS gate technology.

3. GaN deadtime generation circuit for DC-DC buck converters

Fig. 3 shows the block diagram of the proposed GaN synchronous DC-DC buck converter with DTG. It integrates a deadtime generation circuit, gate driver circuits, and a half-bridge power stage. The bootstrap diode D_{BT} and the bootstrap capacitor C_{BT} provide a floating DC power supply when the switching node V_S varies from 0 to V_{IN}. The deadtime generation circuit consists of a two-stage inverter delay chain (direct-coupled FET logic, DCFL inverter), two-input AND gates, and two-input NOR gates. The small deadtimes between the high-side driver and the low-side driver are generated through the inverter delay chain. In addition, further details of the circuit are exhibited in Fig. 4. It is implied that the GaN deadtime generation circuit, the high-side driver, low-side driver, high-side power switch E_{HS}, and low-side rectifier E_{LS} were integrated on one chip.

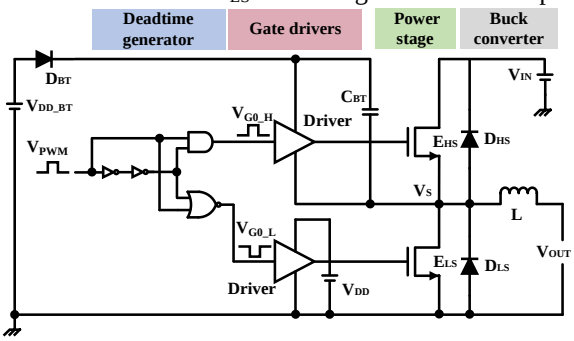

Fig. 3. *Block diagram of the GaN synchronous DC-DC buck converter with a deadtime generator.*

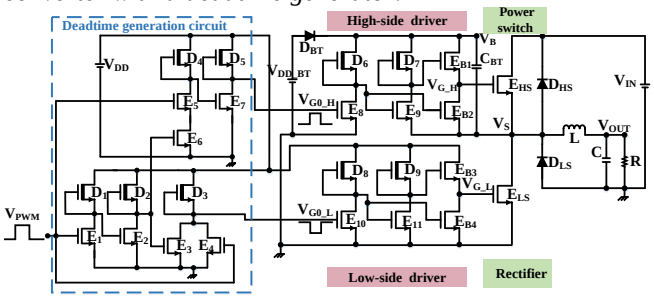

Fig. 4. *The circuit diagram of the proposed GaN DC-DC converter with an integrated deadtime generator (w/ DTG). (Detailed circuit diagram of Fig. 3)*

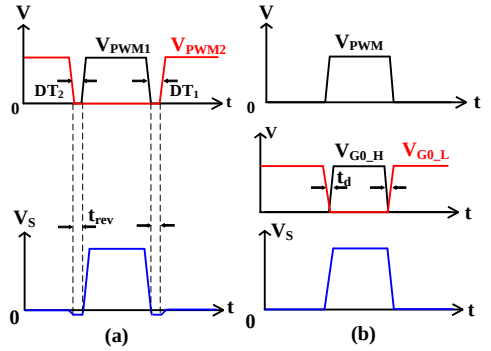

Fig. 5. *Schematic diagrams of dynamic waveforms. (a) Synchronous converter (w/o). (b) Synchronous converter with a deadtime generator (w/ DTG).*

The circuit diagram of a traditional converter [14] in Fig. 5 (a) requires two input PWM control signals (V_{PWM1} and V_{PWM2}) with manually presetting deadtimes (DT_1 and DT_2). Additional deadtimes t_{rev} are required to avoid simultaneous conduction, which leads to extra reverse conduction loss from freewheeling diodes (V_S below zero). The proposed converter with a deadtime generation circuit (w/ DTG) in Fig. 5 (b) uses one control signal V_{PWM}, and it automatically generates two complementary signals V_{G0_H} and V_{G0_L} for the high-side driver and low-side driver, respectively. The complementary signals with a small deadtime reduce reverse conduction deadtimes and avoid unnecessary shoot-through current by false turn-on events or false triggering problems. The small deadtime or delay time between V_{G0_H} and V_{G0_L} is attributed to the propagation delay of the two-stage inverter chain. The propagation delay time (50 % of output-high to 50 % input-high) of two-stage inverters is based on our previous driver circuit [13], and its temperature dependence is shown in Fig. 6. The propagation delay time t_d is less than 0.13 μs at high temperatures approaching 250 °C. Moreover, the monolithic DTG circuit with self-generated deadtimes can operate at various temperatures and provide a simple method of deadtime management for high-temperature power converters.

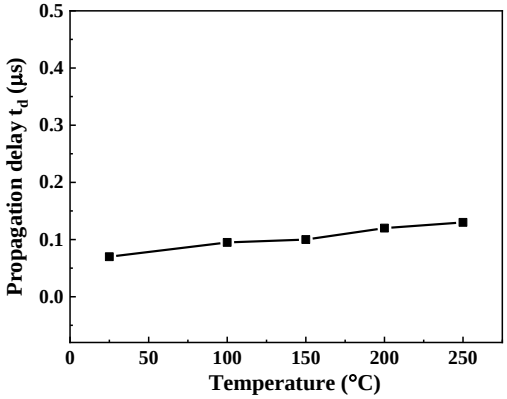

Fig. 6. *Propagation delay time t_d of two-stage inverters (W_D/W_E=50/2000 μm) at various temperatures.*

4. Experimental results and discussions

In this section, the results of GaN-based logic circuits are introduced. Then, a comparison between the proposed GaN DTG converter (w/ DTG) and the GaN converter without DTG (w/o) is discussed at room temperature and high temperatures.

4.1. GaN logic circuits

Two input GaN NAND and NOR gates are basic logic circuits and are widely used in digital circuit design. In this work, we implement GaN nMOS depletion-load logic circuits in GaN DC-DC converters. Fig. 7 shows experimental results of the GaN two-input NAND gates, where a D-mode active load resistor (50 μm) is connected in series with two E-mode transistors (2000 μm). The static voltage transfer characteristics (VTC) are demonstrated in Fig. 7 (a). When V_1=V_2=V_{IN}, the output high voltage (V_{OH}) is 9 V, and the output low voltage (V_{OL}) is 1.12 V. The logic-low noise margin (NM_L) and logic-high noise margin (NM_H) are 1.03 and 3.78 V, respectively. Fig. 7 (b) shows dynamic waveforms of the NAND gates at 100 kHz. As the figure shows, the function of the GaN NAND gates is logically correct, and the output voltage is low only when both E-mode transistors turn on.

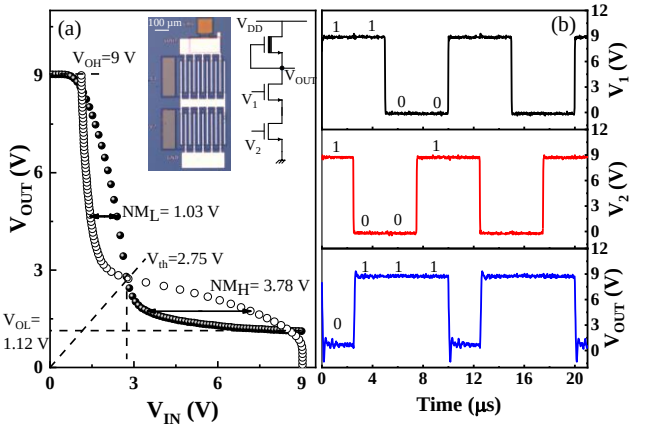

Fig. 7. *(a) Static voltage transfer characteristics (VTC) of GaN NAND gates when V_1=V_2=V_{IN}. (b) Dynamic waveforms at 100 kHz, V_{DD}=9 V.*

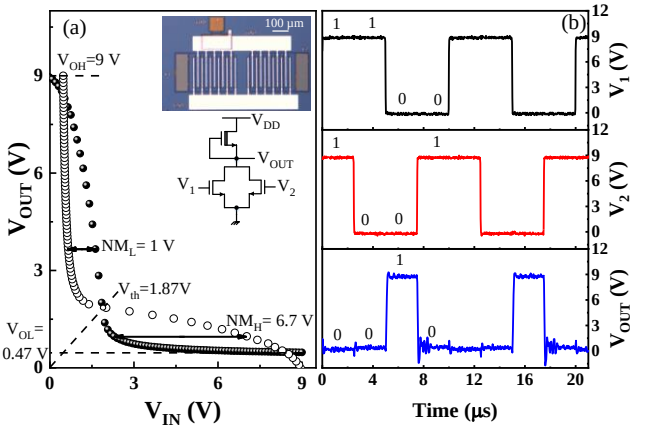

Fig. 8. *(a) Static voltage transfer characteristics (VTC) of GaN NOR gates when V_1=V_2=V_{IN}. (b) Dynamic waveforms at 100 kHz, V_{DD}=9 V.*

Fig. 8 (a) shows the VTC curve of the GaN NOR gates (W_D/W_E=50/2000 μm). When V_1=V_2=V_{IN}, the V_{OH}, and V_{OL} are 9 V and 0.47 V, respectively. Compared with the series connection of NAND gates, the lower V_{OL} of NOR gates is caused by the parallel connection of two E-mode transistors. The NM_L and NM_H are 1 V and 6.7 V, respectively. The

dynamic waveforms of the GaN NOR gates are shown in Fig. 8 (b) at 100 kHz, and the output voltage is high only when two E-mode transistors turn off.

4.2. Converter results comparison at room temperature

Fig. 9 shows the experimental setup of the proposed GaN buck converter (w/ DTG) in Fig. 4. The detailed parameters are shown in Table 1. Two external freewheel diodes D_{HS} and D_{LS}, an inductor L, a load capacitor C, and a load resistor R were integrated on a PCB board. The GaN power ICs were externally connected with a bootstrap diode D_{BT}, a bootstrap C_{BT}, and components of the PCB board using probes. A synchronous GaN converter without DTG (w/o) was also fabricated on the same chip in Fig. 10. The main difference is the absence of the deadtime generation circuit in the GaN converter w/o in Fig. 10, which requires two complementary input signals V_{PWM1} and V_{PWM2} with a presetting deadtime for the high side driver and low side driver, respectively.

Table 1. Summary of device widths of two converters

	D_1, D_2, D_5 (μm)	D_3 (μm)	D_4 (μm)	D_6~D_9 (μm)	E_1~E_7 (μm)	E_8~E_{11} (μm)	E_{B1}~E_{B4} (μm)	E_{HS}, E_{LS} (mm)
w/DTG	50	100	25	50	2000	2000	2000	20
w/o	-	-	-	50	-	2000	2000	10

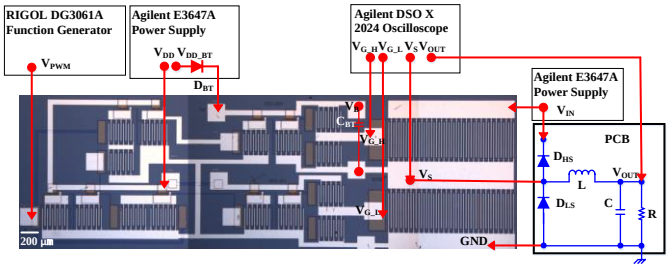

Fig. 9. *Experimental setup of the integrated GaN synchronous converter with a deadtime generator (w/ DTG) in Fig. 4. (The parameters of discrete components involves L=1 mH, C=20 μF, V_{DD} =V_{DD_BT}=9 V, and f=100 kHz. The threshold voltage V_F of the discrete diodes D_{HS}, D_{LS}, and D_{BT} is +0.7 V, C_{BT}= 220 nF.) The effective chip area is 8.6 mm^2.*

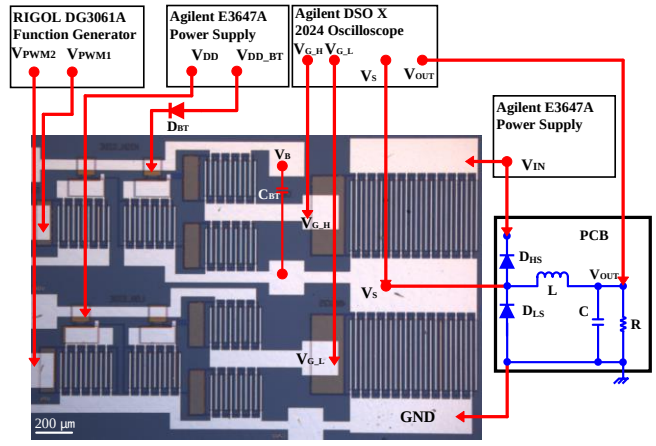

Fig. 10. *Experimental setup of the GaN-based synchronous converter without DTG (w/o) in Table 1. (The parameters of discrete components are the same as Fig. 9)*

Fig. 11 shows dynamic waveforms of the GaN converter w/o in Fig. 10 at a duty cycle of 0.2, 0.5, and 0.7 with a fixed deadtime of 0.5 μs. Obvious gate voltage overshoots were observed, and the overshoots of V_{GS_H} (voltage between V_{G_H} and V_S) are up to 15 V, which might be caused by the large charging and discharging current in the GaN driver. These large overshoots can be detrimental and even damage power devices using p-GaN HEMT technology, which has a gate voltage limitation of 7 V. In this work, the recessed gate with a high-k insulator has a large gate swing of more than 10 V, indicating advantages of strong noise immunity in power converters. The probes and external wires are used to connect the GaN ICs and discrete components, causing extra parasitic in both the gate loop and power loop, leading to large ringings in the testing results. Meanwhile, the deadtime has little impact on the efficiency of the GaN converter w/o due to the negligible contribution of reverse diode conduction loss in this work. Hence we use a deadtime of 0.5 μs in the GaN converters w/o to avoid unnecessary short circuits. The large ringing can increase the switching loss during turn-ON and turn-OFF ringing sub-intervals, which are considered as the energy dissipation contributed by damping the ringing.

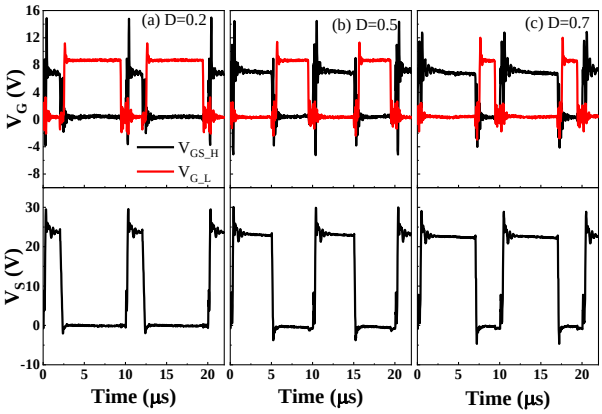

Fig. 11. *Dynamic waveforms of the GaN converter w/o in Fig. 10. V_{GS_H}, V_{G_L}, and switching node V_S with a fixed deadtime of 0.5 μs. f=100 kHz, V_{IN}=25 V, R=100 Ω. (a) D=0.2, (b) D=0.5, (c) D=0.7.*

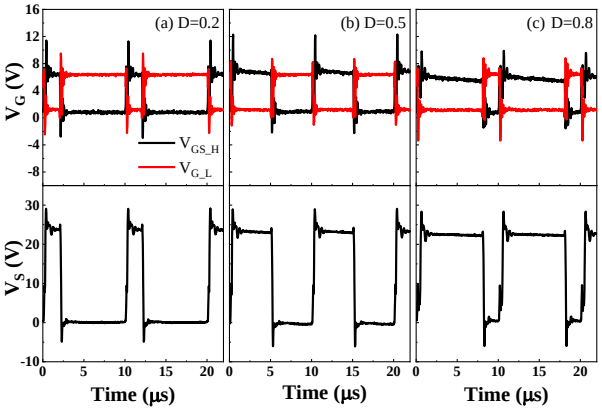

Fig. 12. *Dynamic waveforms of the GaN converter w/ DTG in Fig. 9. V_{GS_H}, V_{G_L}, and switching node V_S. f=100 kHz, V_{IN}=25 V, R=100 Ω. (a) D=0.2, (b) D=0.5, (c) D=0.8.*

Fig. 12 shows the dynamic waveforms of the proposed GaN converter w/ DTG in Fig. 9 with a duty cycle of 0.2, 0.5, and 0.8. The output signals of gate drivers have the maximum overshoot voltage of 12 V lower than 15 V in the GaN converter w/o in Fig. 11. Besides, owing to a smaller ringing, the GaN converter w/ DTG can steadily operate at a high duty cycle of 0.8, while only a duty cycle of 0.7 can be steadily achieved in Fig. 11. This indicates the advantages of the integrated GaN converter with a deadtime generator over the converter with a fixed deadtime, in terms of small voltage overshoot/ringing, and operation capability at high duty cycles.

The efficiency of the power stage was calculated to be the percentage of output power to input power [32]. Fig. 13 and Fig. 14 show the power stage efficiencies of the integrated GaN converter w/o and the GaN converter w/ DTG at various conditions, respectively. Overall efficiencies of 60 %~70 % at large load currents are achieved for both converters. The GaN converter w/o shows a maximum efficiency of 71 % at 5.4 W, and the proposed GaN converter w/ DTG shows a maximum efficiency of 73 % at 8 W. Owing to small voltage ringing in the gate drivers, the GaN converter w/ DTG can operate at a high duty cycle of 0.8 and a larger load power of 11.8 W.

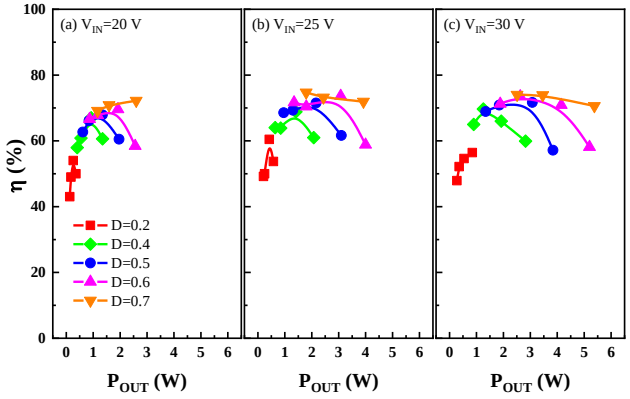

Fig. 13. *Power stage efficiencies of the GaN converter w/o. f=100 kHz, (a) V_{IN}=20 V, (b) V_{IN}=25 V, (c) V_{IN}=30 V.*

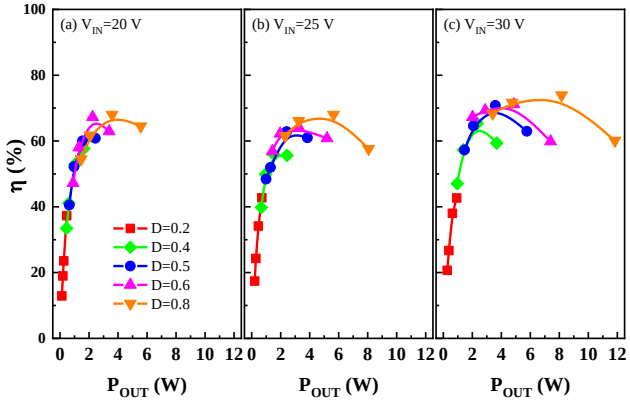

Fig. 14. *Power stage efficiencies of the GaN converter w/ DTG. f=100 kHz, (a) V_{IN}=20 V, (b) V_{IN}=25 V, (c) V_{IN}=30 V.*

The comparable maximum efficiency in both converters with and without DTG is attributed to the main contribution of power transistor conduction loss. The reverse diode conduction losses during deadtimes are small, resulting in a small maximum efficiency difference between the two converters. The large conduction loss is generated from the increased dynamic on-state resistance using the recessed MIS-gate technology in this work. Moreover, the low frequency of 100 kHz might be caused by the 3 μm recessed gate technology. The recessed channel causes decreased mobility and increased R_{ON}, leading to a low switching speed of the integrated GaN converters. From the process point of view, the mainstream p-GaN HEMT would benefit from low on-state resistance for high frequency and high efficiency converters. However, the Schottky gate in p-GaN HEMTs has a large gate leakage current, which highlights the advantage of the recessed MIS-gate technique for high-temperature power converters.

4.3. Converter results at high temperatures

The driver size could have an effect on the switching performance of the drivers and converters. The driver size of the two converters is optimized and reduced by half as shown in Table 2. Compared with Table 1, the main difference is the reduction in the sizes of the drivers and the deadtime generator. The optimized converter w/ DTG and the converter with a fixed deadtime (w/o DTG) have the same width of 20 mm in power transistors.

Table 2. Optimized parameters for two converters

	D_1, D_2, D_5 (μm)	D_3 (μm)	D_4 (μm)	D_6~D_9 (μm)	E_1~E_7 (μm)	E_8~E_{11} (μm)	E_{B1}~E_{B4} (μm)	E_{HS}, E_{LS} (mm)
w/DTG	25	50	12.5	25	1000	1000	2000	20
w/o	-	-	-	25	-	1000	2000	20

The scaled size can reduce the charging and discharging current of the drivers. However, the small driver size causes extra switching delays. Thus, the balance should be made between switching speed and voltage ringings. The optimized converters show improved efficiency due to smaller voltage overshoot and oscillation. Moreover, the depletion-mode devices in GaN ICs can cause extra power loss, and the static driver consumption of four converters is calculated and summarized in Table 3. Compared with GaN converters w/o, the integrated GaN converters w/ DTG have a larger total driver loss, which is ascribed to the extra power loss of deadtime generation circuit P_{DTG}. However, the total driver loss $P_{d,total}$ could be reduced through shrinking drivers. When the size of driver transistors is reduced by half, the driver loss of the proposed GaN converter w/ DTG converter is changed from 0.96 W to 0.48 W.

Table 3. Comparison of estimated driver conduction losses

	I_{D1}, I_{D2}, I_{D5} (mA)	I_{D3} (mA)	I_{D4} (mA)	I_{D6}~ I_{D9} (mA)	P_{DTG} (W)	P_{driver} (W)	$P_{d,total}$ (W)
w/ DTG	22.5	45	11.25	22.5	0.56	0.40	0.96
w/o	-	-	-	22.5	-	0.40	0.4
Optimized w/ DTG	11.25	22.5	5.62	11.25	0.28	0.20	0.48
Optimized w/o	-	-	-	11.25	-	0.20	0.2

The high-temperature measurements were carried out using a Semishare SE-6 probe station, which is equipped with a temperature hot chuck system. A temperature controller is connected to the chuck with a temperature range from 25 ℃ to 300 ℃. During the high-temperature experiments, only the fabricated GaN chip with integrated GaN devices and ICs were heated on the hot chuck, while the PCB board and external components like bootstrapped diode and capacitor were off the hot probe stage for high-temperature measurements. Fig. 15 shows high-temperature results of the optimized GaN converters in Table 2. At 100 kHz, V_{IN}=25 V, the GaN converters show a slight increase of efficiency at high temperatures up to 250 ℃, which might be caused by the reduced current and thus smaller ringing at high temperatures. At high temperatures, both of the optimized GaN converter w/ DTG converter and GaN converter w/o show a comparable maximum efficiency of 80 % at low load currents. The high efficiency of the GaN converters validates the advantages of the recessed MIS gate for HT power converters.

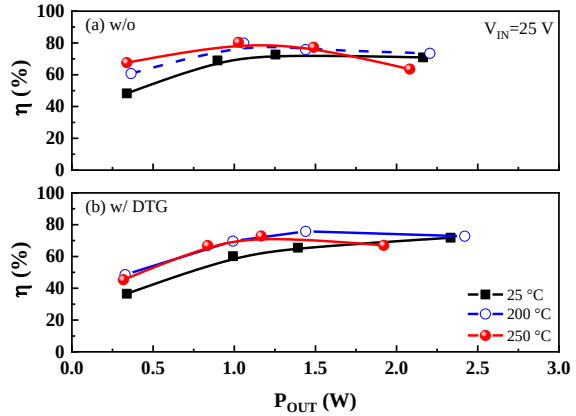

Fig. 15. *Power stage efficiencies of the optimized converter w/o (a) and the optimized converter w/ DTG (b) in Table 2. D=0.5, V_{IN}=25 V, T=25 ℃, 200 ℃, and 250 ℃, f=100 kHz.*

Both converters can operate at high temperatures up to 250 ℃, and here we use 200 ℃ as an example to compare two optimized converters at various load conditions. Fig. 16 and Fig. 17 show gate signals of the optimized driver w/o and the optimized driver w/ DTG at various load conditions, respectively. The optimized GaN converter with a fixed deadtime (w/o) in Fig. 16 shows obvious gate overshoot at the switching-off transient of the high-side transistor, and the increased overshoot with incremental input voltages and load currents. The overshoot might be caused by the delay between the switching node V_S and high-side gate driver signal V_{G_H}, due to the increased R_{ON} at large load currents and high temperatures. The maximum overshoot voltage is up to 20 V, which is detrimental to some Schottky gate GaN devices with a strict gate voltage limitation of 7 V [33]. Owing to the insertion of the high-k insulator Al_2O_3 in this work, the recessed E-mode MIS gate can provide a dynamic gate-to-source voltage tolerance of 20 V at high temperatures. Fortunately, the proposed GaN converter w/ DTG shows a smaller gate overshoot at various load conditions at 200 ℃ in Fig. 17, validating the advantages of the proposed GaN deadtime generation circuit for high-temperature power converters.

Fig. 18 gives a comparison of dynamic V_S waveforms at various load conditions at 200 ℃. At a small load current with a load resistance of 500 Ω, the maximum voltage of stable V_S ($V_{S,Max}$) has no obvious difference between the two converters. However, when the load resistance is increased to 25 Ω, the $V_{S,Max}$ in the proposed converter w/ DTG is higher than that in converter w/o, and the discrepancy increases with increasing input voltages. The large gate overshoot in Fig. 16 can increase R_{ON} at large load currents. The dynamic R_{ON} increases with increasing gate voltage [34], and this can explain the lower $V_{S,Max}$ of the optimized converter w/o at large load currents at 200 ℃ in Fig. 18. The temperature dependence of electrical parameters of GaN power transistors [35] can guide the design of drivers for high-temperature power converters.

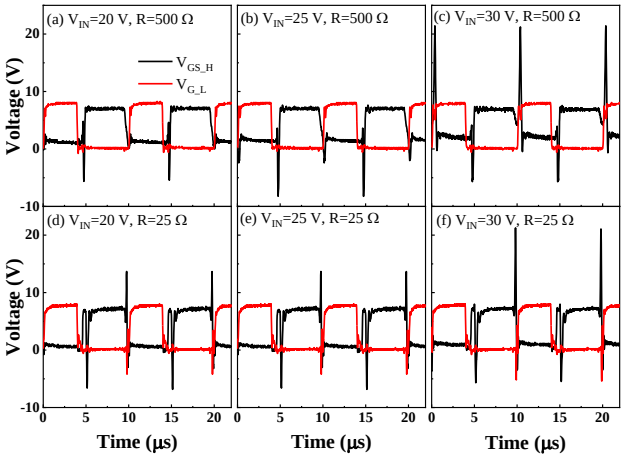

Fig. 16 *Gate driver signals of the optimized GaN converter w/o at various load conditions at 200 ℃. f=100 kHz, D=0.5.*

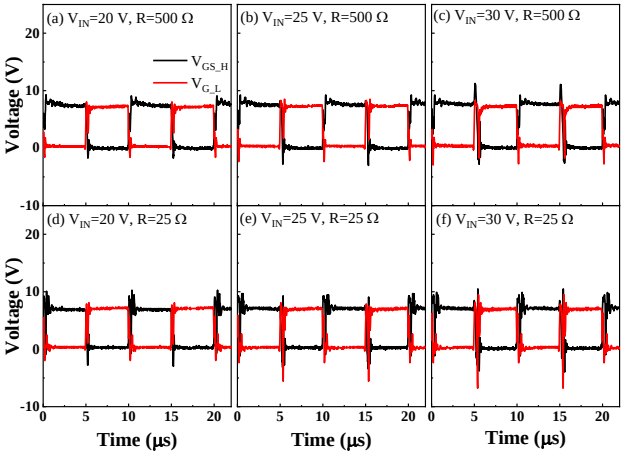

Fig. 17 *Gate driver signals of the optimized GaN converter w/ DTG at various load conditions at 200 ℃. f=100 kHz, D=0.5.*

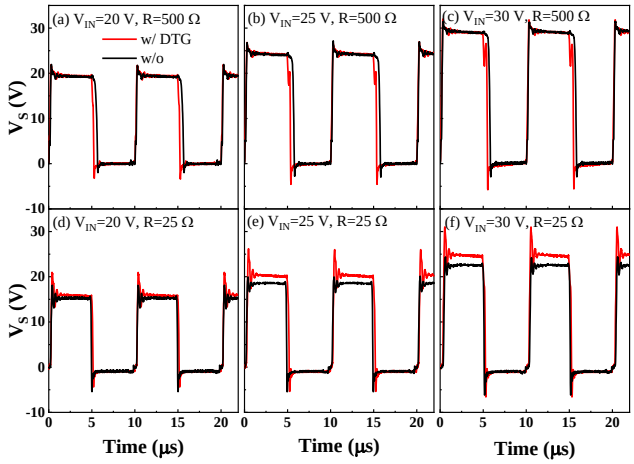

Fig. 18. *Comparison of dynamic V_S waveforms between the optimized converter w/ DTG and converter w/o at various load conditions. D= 0.5, T= 200 ℃.*

Fig. 19 shows the power stage efficiencies of two optimized converters at various load currents at 200 ℃ to investigate temperature-dependent efficiency, since R_{ON} increases at high temperatures due to the degradation of the channel mobility [36]. At low load powers, both converters exhibit a comparable maximum efficiency of 80 % at 200 ℃, benefiting from the recessed GaN MIS-HEMTs for high-temperature converters. The little difference in peak efficiency between the two converters is attributed to the large power conduction loss and small reverse conduction loss during deadtimes as discussed previously. Advanced interface engineering techniques and a larger power transistor width could be helpful to reduce dynamic R_{ON} and improve power efficiency. However, the proposed GaN converter with a deadtime generator shows smaller efficiency degradation with increasing load powers compared with the converter w/o at high temperatures. Moreover, under the same load resistances, the maximum power reaches 5.4 W for the optimized converter w/ DTG in Fig. 19 (b), which is larger than 3.7 W for the optimized converter w/o in Fig. 19 (a), respectively. This can be explained by higher $V_{S,Max}$ of the optimized converter w/ DTG at large load currents in Fig. 18. The high-temperature results indicate a better performance of the proposed GaN converter w/ DTG at high temperatures.

Table 4 Deadtime Techniques for GaN-based DC-DC Converters

Design	**[21]**	**[18]**	**[22]**	**[19]**	**[23]**	**[24]**	**[25]**	**This Work**
Year	2015	2016	2016	2020	2022	2022	2022	2022
Topology	Buck	Boost	Buck	Boost	Buck	Buck/Boost	Buck	Buck
GaN switch	E-mode (discrete EPC2014,2015)	E-mode (discrete EPC2001)	E-mode (discrete EPC2007)	E-mode (discrete GS66508P)	E-mode (discrete EPC2014C)	E-mode (discrete EPC8009)	E-mode (p-GaN HEMT)	E-mode (GaN MIS HEMT)
Deadtime technique	Deadtime corrector (0.35μm CMOS)	Analytical model	Deadtime controller (0.35μm CMOS)	Adaptive model	Deadtime controller (0.18 μm BCD process)	Deadtime controller (0.18 μm BCD process)	Integrated deadtime controller (GaN process)	Integrated deadtime generator (3 μm GaN process)
Gate driver	On-chip (simulated)	Discrete LM5113	On-chip	Discrete SI8271	On-chip	On-chip	Integrated GaN driver	Integrated GaN driver
Frequency	1 MHz	400 kHz	100 kHz	270 kHz	1 MHz	9 MHz	50 MHz	100 kHz
Efficiency	93.6%	95%	95%	98.6%	84.68 %	86.37% (Buck)	95.4%	80%
V_{IN} Range	12V	24 V	45 V	250V	12V	20-40 V	48-400 V	20-30 V
$V_{GS,max}$	6 V	6 V	6 V	7 V	6 V	6 V	N.A.	10 V
Temperature	RT	RT	RT	RT	RT	RT	RT	250 °C
Area	Simulation	N.A.	0.22 mm^2 (CMOS deadtime controller)	N.A.	1.5 mm^2 (Driver only)	9 mm^2 (Driver only)	16.75 mm^2 (GaN driver+GaN switch)	8.6 mm^2 (GaN driver+ GaN switch)

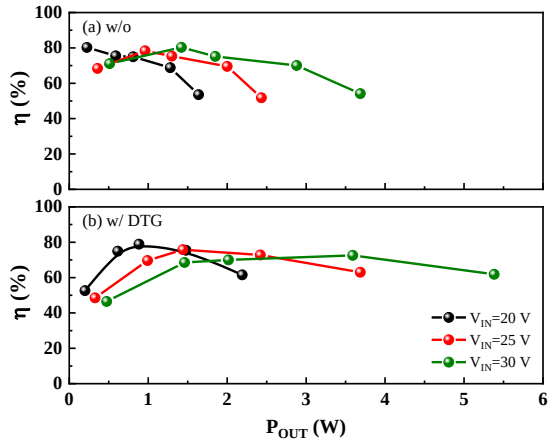

Fig. 19. *Power stage efficiencies of the optimized converter w/o (a) and the optimized converter w/ DTG (b) in Table 2. f=100 kHz, D= 0.5, T= 200 ℃, V_{IN}=20 V, 25 V, and 30 V.*

Table 4 shows a summary of deadtime techniques for GaN-based DC-DC converters. Most of the reported methods are based on external deadtime management or Si-based integration technology. One recent method using GaN technology was reported [25] with high frequency, high efficiency, and a small chip size. However, this technique is based on p-GaN HEMT technology, which is not suitable for high-temperature operation due to its leakage current from the Schottky contact. In this work, the proposed GaN DTG converter with one control signal can operate at 250 ℃ with a large gate swing of 10 V, and it shows a maximum efficiency of 80 % at high temperatures. Due to the limitation of the 3 µm recessed MIS-gate technology, the frequency and efficiency of the proposed converter with a deadtime generator are not high enough. However, this work validates the possibility of the monolithically integrated GaN deadtime method using all-GaN nMOS technology. Results in this work provides the guidance to develop GaN-based advanced deadtime correction circuits or controllers in the future, especially for high-temperature operations.

5. Conclusion

Deadtime management is essential for power converters to avoid short circuit failure and reduce power loss during deadtimes. This work demonstrates a GaN deadtime generation (DTG) circuit and provides a simple deadtime management method for high temperatures power converters. The proposed GaN integrated circuits (ICs) simply use one pulse signal to generate two complementary signals with a small deadtime. The GaN converter w/ DTG is compared to a GaN converter (w/o) with two input signals and a presetting deadtime at various load conditions. The proposed GaN DTG converter provides smaller gate voltage overshoot and ringing than the converter w/o with a compromise of extra driver consumption. Moreover, the two optimized converters show a comparable maximum efficiency of 80 % at high temperatures up to 250 ℃. At high temperatures, the proposed converter w/ DTG shows better efficiency at large load currents than the optimized converter w/o, owing to the small voltage overshoot of driver signals. The results in this work provide a simple deadtime method for high-temperature power converters in applications under extreme environments, where a high temperature above 200 ℃ is required.

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7. Conflict of interest

The authors have no conflict of interest.

8. Data availability statement

Data sharing not applicable.

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