A K-Band MMIC Cross-Coupled Oscillator With High Output Power in 0.25- μ m GaN HEMT

Jiayou Wang[®], *Graduate Student Member, IEEE*, Yi Huang[®], *Fellow, IEEE*, Yin-Cheng Chang[®], *Member, IEEE*, Yeke Liu, Da-Chiang Chang[®], *Member, IEEE*, and Shawn S. H. Hsu[®], *Member, IEEE*

Abstract— In this letter, a monolithic microwave integrated circuit (MMIC) cross-coupled oscillator with high operating frequency and high output power is proposed using 0.25- μ m gallium nitride (GaN) high electron mobility transistor (HEMT) technology. The coupling capacitors in the core circuit are analyzed to obtain high output power with a suitable tank inductor. The π -type matching network is adopted to effectively extract the fundamental output signal. Also, a flip-transistor layout with a shared back via is proposed for reduced interconnect loss and a compact layout. With a chip area of only 0.71 mm², the measured results demonstrate a maximum output power of 16 dBm at 24.3 GHz, and a phase noise (PN) of -137.9 dBc/Hz at a 10-MHz offset.

Index Terms—Gallium nitride (GaN), high electron mobility transistor (HEMT), K-band, monolithic microwave integrated circuit (MMIC), oscillator.

I. INTRODUCTION

G ALLIUM nitride (GaN) high electron mobility transistor (HEMT) has received great attention recently due to its capability of high speed and high power operation [1]. Based on GaN HEMT technology, power amplifiers (PAs) with good performance have been reported [2]. Utilizing GaN HEMTs for high power oscillator design is also of great interest [3]. The oscillator is an essential block in many microwave systems for different applications such as radars, communications, imaging, and sensing. With advanced GaN HEMTs of the gate length down to 0.1 μ m or even 60 nm, oscillators with operating frequencies up to W-band and G-band have been reported [4], [5]. However, most of the reported works are with relatively low frequencies in the range of several gigahertz [6], [7], [8] using the 0.25- μ m GaN technology, which could be attributed to the relatively low $f_{\rm T}$ and $f_{\rm max}$ of

Manuscript received 26 January 2023; revised 28 March 2023; accepted 24 April 2023. This work was supported by the National Science and Technology Council (NSTC) under Contract 110-2222-E-007-003-MY3 and Contract 111-2218-E-110-002. (Corresponding authors: Shawn S. H. Hsu; Yi Huang.)

Jiayou Wang is with the Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan, and also with the Department of Electrical Engineering and Electronics, University of Liverpool, L69 3GJ Liverpool, U.K.

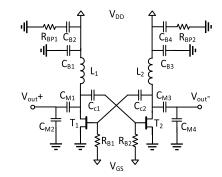
Yi Huang is with the Department of Electrical Engineering and Electronics, University of Liverpool, L69 3GJ Liverpool, U.K.

Yin-Cheng Chang and Da-Chiang Chang are with the Taiwan Semiconductor Research Institute (TSRI), Hsinchu 300091, Taiwan.

Yeke Liu and Shawn S. H. Hsu are with the Department of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan (e-mail: shhsu@ee.nthu.edu.tw).

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWT.2023.3271989.

Digital Object Identifier 10.1109/LMWT.2023.3271989



1

Fig. 1. Circuit topology of the proposed cross-coupled GaN oscillator.

the transistors, design limitations of inductive elements, and restricted circuit topology and layout.

In this letter, we report a *K*-band oscillator monolithically integrated using 0.25- μ m GaN HEMT technology. Analysis and design considerations are described in Section II, and simulated and experimental results are reported in Section III. With a cross-coupled topology, π -type output matching, and flipped-transistor layout, the proposed oscillator achieves the highest operating frequency at the fundamental tone with a high output power compared with prior works using similar technology. The obtained figure of merit (FoM) are also among the best.

II. OSCILLATOR DESIGN

The technology adopted in this design is WIN semiconductor 0.25- μ m GaN-on-SiC HEMTs [9]. The AlGaN/GaN transistor incorporates a T-gate, which utilizes the lift-off process to reduce gate resistance [10]. The Si₃N₄ film is employed as the dielectric material for different metal layers and the capacitor. A thick top metal layer by Au (metal 2) of 4 μ m is available, which can be used to design low-loss transmission lines and spiral inductors. The SiC substrate is thinned down to 100 μ m and with vias connected to the backside metal. More process details can be found in [9]. It is worth mentioning that the process utilizes a source-coupled field plate to provide a breakdown voltage exceeding 120 V required for reliable high drain bias operation. The nominal $f_{\rm T}$ and $f_{\rm max}$ are 25 and 75 GHz, respectively.

Fig. 1 shows the details of the proposed cross-coupled oscillator. The two GaN HEMTs T_1 and T_2 are cross-coupled by C_{c1} and C_{c2} , which also act as dc blocking capacitors. R_{B1} and R_{B2} are used to provide negative bias voltage for the transistors. L_1 and L_2 are the equivalent inductors, combining the resonant tank inductance and also the output-matching

2771-957X © 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

IEEE MICROWAVE AND WIRELESS TECHNOLOGY LETTERS

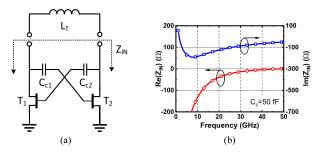


Fig. 2. (a) Simplified oscillator core circuit. (b) Real and imaginary parts of $Z_{\rm IN}$ versus frequency with $C_{\rm c} = 50$ fF.

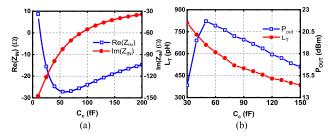


Fig. 3. (a) Simulated Z_{IN} . (b) Tank inductor L_T and output power P_{OUT} versus C_c at 25 GHz.

inductance. The capacitors $C_{\rm M1} - C_{\rm M4}$ construct the equivalent π output matching network together with part of L_1 and L_2 . The *RC* networks including $R_{\rm BP}$ and $C_{\rm B}$ are employed for bypass networks.

A. Design of Cross-Coupled Pair

The transistor periphery used in the design is $2 \times 75 \ \mu m$ considering the trade-off between the output power level and the desired operating frequency according to f_T and f_{max} . Fig. 2(a) shows the simplified oscillator core circuit, including a cross-coupled pair, coupling capacitors, and an equivalent resonant tank inductor L_T . The design of the coupling capacitor C_e is critical to the oscillator characteristic which can be seen from Z_{IN} looking into the cross-coupled pair. Fig. 2(b) shows the simulated real and imaginary parts of Z_{IN} as a function of frequency. The real part Re(Z_{IN}) becomes less negative as frequency increases. Also, the imaginary part Im(Z_{IN}) is mostly negative, which indicates a capacitive impedance of Z_{IN} .

Fig. 3(a) shows the simulated Z_{IN} as a function of C_c at the center frequency of 25 GHz. As can be seen, the negative resistance disappeared if C_c is very small since T_1 and T_2 are no longer cross-coupled. On the other hand, $Re(Z_{IN})$ becomes less negative if C_c increases gradually after a certain point. The value of $C_{\rm c}$ used in the final design is approximately 60 fF for obtaining maximum negative resistance. It should be mentioned that $Im(Z_{IN})$ becomes more negative monotonically with reduced $C_{\rm c}$. This indicates a relatively small equivalent capacitance of Z_{IN} with small C_c . As a result, a larger inductor is allowed for the LC tank of the oscillator even designed at high frequency. This is beneficial for practical design, especially using the adopted GaN technology. Different from using a typical CMOS process, small inductors could be challenging to implement considering the relatively large size of GaN transistors. Increasing the required inductance for the LC tank can ease the design of the circuit layout. Based on the final design, Fig. 3(b) shows how the required equivalent

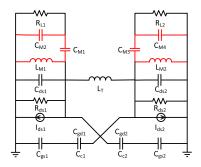


Fig. 4. Simplified small-signal model of the proposed GaN oscillator.

tank inductor $L_{\rm T}$ and output power $P_{\rm OUT}$ change as a function of $C_{\rm c}$. At $C_{\rm c}$ of ~60 fF, $P_{\rm OUT}$ is close to the maximum value, and the corresponding tank inductance is ~600 pH.

B. Design of Output Matching Network

Using the output buffer stage is a typical approach for connecting the output to the 50 Ω load in high-frequency oscillator design, which is usually seen in CMOS-based RFICs with a cross-coupled topology [11]. However, this is unsuitable if using GaN technology considering the large transistor size and the area-consuming through wafer vias (TWV). The buffer stage also requires a considerable amount of extra dc power.

In the proposed design, the π -type matching network is employed for matching the circuit to 50 Ω load. Fig. 4 shows the small-signal equivalent circuit of the oscillator including the matching network $C_{M1}-C_{M4}$ and $L_{M1}-L_{M2}$. The design starts with establishing the small-signal model of the transistor under the chosen biasing conditions. In the small-signal model, the drain-source resistance R_{ds} extracted based on the S-parameters is employed to design outputmatching networks. Once oscillation starts, the reactive part is resonated out, and the matching network is mainly designed by converting R_{ds} to the 50- Ω load. As illustrated in Fig. 4, the π -matching network composed of C_{M1} - C_{M2} (C_{M3} - C_{M4}) and $L_{M1}(L_{M2})$ is designed as wideband matching for maximum power transfer. Note that the circuit is differentially operated at the fundamental frequency, the center of L_T is a virtual ground. Thus, in practical implementation, only one inductor L_1 (L_2) is required (see Fig. 1) on each side which combines $L_{\rm M}$ and $L_{\rm T}/2$, as expressed in (1). Note that L_1 and L_2 also serve as the paths where dc power is fed to the transistors

$$L_1 = \frac{L_{\rm M} L_{\rm T}}{2L_{\rm M} + L_T}.\tag{1}$$

In our final design, L_1 and L_2 are both 270- μ m long and 35- μ m wide. Based on EM simulation, the corresponding inductance and quality factor (*Q*) are 160 pH and 56, respectively, at 25 GHz. Compared with the typical CMOS process on a silicon substrate, a relatively high-quality factor can be obtained for the adopted GaN HEMT technology due to the low-loss SiC substrate and the thick metal layer. We also simulate the phase noise (PN) with varying values of *Q* by adjusting the geometry of L_1 and L_2 while maintaining a constant frequency. The results show that the PN varies from -117.7 dBc/Hz (Q = 26) to -119 dBc/Hz (Q = 70) at a 1 MHz offset. The PN can be improved with increased *Q* as expected. Despite this, the PN is not a strong function of the

Ref.	f _{osc} (GHz)	Topology	Peak P _{OUT} (dBm)	Tuning range (%)	P _{DC} (mW)	Size (mm ²)	PN (dBc/Hz)	FoM ¹ (dBc/Hz)	FoM ² (dBc/Hz)	FoM ³ (dBc/Hz)
[6]	7.9	Single-end	21		1456	0.66	-135@1MHz	-181.3	-213	-202.3
[7]	8.6	Balanced Colpitts	6		600		-102@100KHz	-172.9	-200.7	-178.9
[12]	15.01~15.12	Single-end	-6	0.7	63	2	-133@1MHz	-198	-216.6	-192.5
[13]	7.16~7.31*	Single-end	1.06	2.1*	18.33	2	-122.5@1MHz	-187	-199.7	-188.1
[14]	6.45~7.55	Balanced Colpitts	2	15.7	198	1.82	-132@1MHz	-185.9	-208.9	-187.9
This work	23.9~24.4	Cross- coupled	16	2.1	747	0.71	-109.4@1MHz -137.9@10MHz	-168.3 -176.8	-197.1 -205.6	-184.3 -192.8

TABLE IPerformance Comparison With Prior Works Using 0.25- μ m GaN HEMT Technology

*Estimated from the paper; FoM¹ = PN - $20\log(f_0/\Delta f) + 10\log(P_{DC}/1mW)$; FoM² = PN - $20\log(f_0/\Delta f)$; FoM³ = PN - $20\log(f_0/\Delta f) + 10\log(P_{RF}/P_{DC})$.

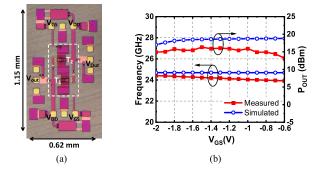


Fig. 5. (a) Chip micrograph of the proposed GaN oscillator. (b) Simulated and measured oscillating frequency and P_{OUT} versus V_{GS} .

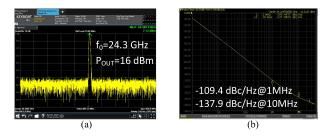


Fig. 6. Measured results of the GaN HEMT oscillator. (a) Output spectrum. (b) PN.

Q of L_1 and L_2 since these inductors are part of the output matching network. The overall quality factor of the matching network has a more significant influence on the oscillator PN.

III. EXPERIMENTAL RESULTS

Fig. 5(a) shows the chip micrograph of the proposed GaN cross-coupled oscillator. The chip size is 0.71 mm² including the testing pads. It should be emphasized that a typical layout of cross-coupled transistors needs relatively long interconnects, which makes it difficult for a practical layout using the adopted GaN technology. As indicated in the dashed-line box in the chip photo, one transistor is flipped by 180° and the cross-coupled route can form a loop to effectively reduce the length of the interconnect. Also, a TWV at the center is shared by two transistors to further reduce the circuit size.

The oscillating frequency and output power of the fabricated design were measured on-wafer using a spectrum analyzer (Keysight N9041B UXA), and the PN was measured using a signal source analyzer (Keysight E5052A). Fig. 5(b) shows the comparison of the simulated and measured results of oscillating frequency and output power which show a good

agreement in general. The relatively small discrepancy could be mainly attributed to the active device model, given that rigorous full electromagnetic (EM) simulations of the entire circuits, including the probing pads and all interconnects, have been performed. Note that one possible reason for the inaccuracy of the transistor model is the thermal effect [15], which is challenging to model precisely under different bias conditions. This also makes it more difficult to predict the P_{out} of the GaN oscillator. The operating frequency can be tuned from 23.9 to 24.4 GHz with V_{GS} varying from -2 to -0.6 V. Fig. 6(a) shows the measured spectrum with the peak output power of 16 dBm at 24.3 GHz after calibration of cable loss. The measured values of PN were -109.4 and -137.9 dBc/Hz at 1 and 10 MHz, respectively, as shown in Fig. 6(b). Table I summarizes and compares the performance of the proposed oscillator with previously reported oscillators using 0.25- μ m GaN HEMT technology. To the best of our knowledge, the proposed design achieves the highest oscillation frequency with a higher or comparable output power level based on a similar GaN HEMT technology. The proposed design also obtains comparable or better FoMs [3], [6], [11] even with a higher operating frequency.

IV. CONCLUSION

In this letter, a *K*-band MMIC cross-coupled oscillator using 0.25- μ m GaN HEMT technology has been demonstrated. The coupling capacitors in the core circuit were analyzed and designed carefully to achieve high output power with a suitable tank inductor at the desired frequency. The π -type output matching network was employed instead of a buffer stage to extract the fundamental signal to 50 Ω load. Also, the flipped transistor with shared TWV of the cross-coupled pair was proposed for reduced interconnect loss and a compact layout. The experimental results showed that the proposed oscillator achieved the highest frequency with a high output power compared with prior works using similar GaN technology. The results indicate the potential of GaN technology for high-power millimeter-wave signal source applications.

ACKNOWLEDGMENT

The authors would like to thank the Taiwan Semiconductor Research Institute (TSRI), Hsinchu, Taiwan, for the chip measurements.

4

REFERENCES

- L. Li et al., "GaN HEMTs on Si with regrown contacts and cutoff/maximum oscillation frequencies of 250/204 GHz," *IEEE Electron Device Lett.*, vol. 41, no. 5, pp. 689–692, May 2020.
- [2] S.-H. Li, S. S. H. Hsu, J. Zhang, and K.-C. Huang, "Design of a compact GaN MMIC Doherty power amplifier and system level analysis with X-parameters for 5G communications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5676–5684, Dec. 2018.
- [3] D. Kim and S. Jeon, "W- and G-band GaN voltage-controlled oscillators with high output power and high efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 8, pp. 3908–3916, Aug. 2021.
- [4] R. Weber, D. Schwantuschke, P. Bruckner, R. Quay, F. van Raay, and O. Ambacher, "A 92 GHz GaN HEMT voltage-controlled oscillator MMIC," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Tampa, FL, USA, Jun. 2014, pp. 1–4.
- [5] T. N. Thi Do, Y. Yan, and D. Kuylenstierna, "A low phase noise W-band MMIC GaN HEMT oscillator," in *Proc. IEEE Asia–Pacific Microw. Conf. (APMC)*, Hong Kong, Dec. 2020, pp. 113–115.
- [6] H. Liu et al., "Design of ultra-low phase noise and high power integrated oscillator in 0.25 μm GaN-on-SiC HEMT technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 2, pp. 120–122, Feb. 2014.
- [7] S. Lai et al., "Accurate phase-noise prediction for a balanced Colpitts GaN HEMT MMIC oscillator," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 11, pp. 3916–3926, Nov. 2013.
- [8] C.-C. Chuang and H.-K. Chiou, "A low phase noise X band class E power VCO in 0.25 μm GaN/SiC technology," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT)*, Taiwan, Aug. 2021, pp. 1–3.

- [9] M.-H. Weng, C.-K. Lin, J.-H. Du, W.-C. Wang, W.-K. Wang, and W. Wohlmuth, "Pure play GaN foundry 0.25 μm HEMT technology for RF applications," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Monterey, CA, USA, Oct. 2013, pp. 1–4.
- [10] C.-W. Tsou, C.-Y. Lin, Y.-W. Lian, and S. S. H. Hsu, "101-GHz InAlN/GaN HEMTs on silicon with high Johnson's figure-ofmerit," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2675–2678, Aug. 2015.
- [11] P.-Y. Wang, G.-Y. Su, Y.-C. Chang, D.-C. Chang, and S. S. H. Hsu, "A transformer-based current-reuse QVCO with an FoM up to -200.5 dBc/Hz," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 6, pp. 749–753, Jun. 2018.
- [12] M. Hörberg and D. Kuylenstierna, "Low phase noise power-efficient MMIC GaN-HEMT oscillator at 15 GHz based on a quasi-lumped onchip resonator," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Phoenix, AZ, USA, May 2015, pp. 1–4.
- [13] S.-L. Jang, Y.-H. Chang, and W.-C. Lai, "A feedback GaN HEMT oscillator," in *Proc. Int. Conf. Microw. Millim. Wave Technol. (ICMMT)*, Chengdu, China, May 2018, pp. 1–3.
- [14] T. N. T. Do, S. Lai, M. Horberg, H. Zirath, and D. Kuylenstierna, "A MMIC GaN HEMT voltage-controlled-oscillator with high tuning linearity and low phase noise," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, New Orleans, LA, USA, Oct. 2015, pp. 1–4.
- [15] M.-J. Liu and S. S. H. Hsu, "A miniature 300-MHz resonant DC–DC converter with GaN and CMOS integrated in IPD technology," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9656–9668, Nov. 2018.