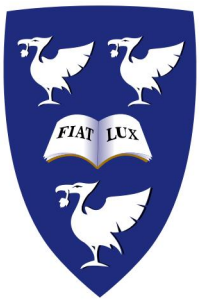

UNIVERSITY OF LIVERPOOL

Application of advanced material in flexible fully solution processed thin film transistors

先进材料在柔性全溶液处理薄膜晶体管中的应用

Thesis submitted in accordance with the requirements of the University of Liverpool for the degree of Doctor in Philosophy in the Department of Electrical Engineering and Electronics

April 2023

By

Qinan Wang

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Abstract

The advanced computing system with a bionic nervous neuromorphic structure to facilitate parallel data updates for artificial neural networks (ANNs) has aroused extensive concern due to the limitations of conventional logic operation rules based on the von Neumann architecture. In order to construct the core units for the ANN system, the artificial synaptic transistors were then proposed for multi-level storage and parallel computing, which has been being intensively investigated to mimic the behavior and function of the biological synapses. At present, the development of both end devices has become increasingly mature, and the latest research is to be able to run basic neural networks and perform complex tasks on millions of scale integrated chips. Thus, the comprehensively deepen innovation of three terminal neural devices must be explored in all related fields, including model algorithm, software, chip, and data. According to the various storage mechanisms and physics, the ferroelectric transistors, floating-gate transistors, electrolyte gate transistors, and electret-based organic transistors have been researched to realize the neurons behaviors. Nevertheless, neuromorphic device , synaptic long-term plasticity and mechanisms of bionic synapse must be further explored to simultaneously enable signal transmission, iterative learning, and timely surveillance. Furthermore, briefly summarize the evolution of neural networks from the first generation to the third generation. The first generation neural network uses mathematical and physical modeling to abstract the human brain neural network and establish a simplified model. ANN mainly uses weight and multiplication to simulate synaptic characteristics, and addition to simulate the interconnection of dendrites. Further algorithm optimization is carried out on the structure of error feedback, and various frameworks and strategies (such as convolution, loops, and residuals) are added to form the second generation neural network. Compared to the first generation, the second generation neural network can perform more complex tasks. Faster speed and higher efficiency. In order

to better fit the working mechanism of the human brain (low power consumption), the third generation neural network has been proposed to achieve higher levels of biological neural simulation. In addition to neuronal and synaptic states, the third generation neural network also incorporates the concept of time into its operations. It can more accurately simulate the dynamics of brain neurons. Then it also can perform complex intelligent tasks at low energy consumption.

In this work, we propose the ion-doped eco-friendly solution-processed indium oxide (InO_x)/aluminum oxide (AlO_x) electrolyte gate transistors (EGTs) with typical and reliable synaptic behavior. The lithium (Li) ions doped into the AlOx solid state layer to facilitate the generation of electrical double layers (EDLs) and doped into InOx to improve the stability of long-term potentiation/depression (LTP/LTD) cyclic update and enhance the synaptic plasticity. For the application, an ANN (first generation) simulator is well designed to electrocardiogram (ECG) signal recognition based on the G_{max}/G_{min} ratio and nonlinearity of weight update curve. According to the results, the device possesses tremendous potential for bio-signal prediction and neural intervention. Moreover, for the first time, the recognition accuracy of the abnormality of the cardiovascular can reach over the 94.8% obtained from the confusion matrix. Consequently, this research article presents a stable and robust neuromorphic device for bio-signal recognition based on solid state EGTs via the synaptic long-term plasticity (**Chapter 2**).

Second, to effectively control the non-volatile conductance, dynamic deep learning is considered to simulate the nonlinear memory process of human brain during the long-term potentiation and long-term depression of weight update process to implement complex tasks. Here, we firstly propose a photoelectrically modulated synaptic transistor based on two-dimensional material (MXenes), which well adjusts the nonlinearity and asymmetry by mixing controllable electric pulses and optical pulses. According to the advantage of the

residual deep learning (second generation) can amplify the difference between labels, the rule of dynamic learning is thus elaborately developed to improve significantly the accuracy of highly similar and homologous database (using a classic Rabbit IgG antigen as the colorimetric enzyme-linked immunosorbent assay (c-ELISA) sensing target at microfluidic paper-based analytical devices (μPAD) from 80.9% to 87.2% and therefore realize the fast convergence. Besides, photoelectric mixed stimulation also remarkablely shortens the iterative update time to 11.6 s during training epochs as a result that the photoelectric effect accelerates the relaxation of ion migration. Then, we even further extend the dynamic learning strategy to Long Short-Term Memory (LSTM) and standerd data sets (Cifar10 and Cifar100) which well proves the strong robustness. This work firstly represents a significant advance and pave the way towards potential synaptic-device-based bionic retina for computer aided detection in immunology about quantitative analysis of immune protein and also lays a foundation for selecting matching neural network and tasks according to the synaptic plasticity of synaptic devices (**Chapter 3**).

Third, deeply explore the functions of neural devices, match neural networks that best match biological characteristics, and build an overall architecture. Spiking neural networks (SNNs) incorporating synaptic plasticity hold great potential because of the temporal correlation and low power consumption. Leaky intergrate-and fired (LIF) model and spike timing dependent plasticity (STDP) are the core and specific components of SNNs. Here, the neural device is first demonstrated by zeolitic imidazolate frameworks (ZIFs) as essential part of synaptic transistor to simulate the neuromorphic computing in SNNs. Significantly, three kinds of typical functions between neurons, the memory function achieved through hippocampus, synaptic weight regulation and membrane potential triggered by ion migration, are effectively described through the short-term memory/long-term memory (STM/LTM), long-term depression/long-term potentiation (LTD/LTP) and LIF, respectively. Further, update rule of

iteration weight in the back propagation based on the time interval between pre-synaptic and post-synaptic pulses is extracted and fitted from the synaptic transistors. Besides, the postsynaptic currents of channel directly connect to the Very Large Scale Integration (VLSI) implementation of the LIF mode that can convert high-frequency information into spare pulses based on the threshold of membrane potential. Leaky integrator block, firing/detector block and frequency adaption block instantaneously release the accumulated voltage to form pulse. Finally, we recode the Steady-State Visual Evoked Potentials (SSVEP) belongs to electroencephalogram (EEG) with filter characteristics of LIF. SNNs deeply fused by synaptic transistors are designed to recognize the 40 different frequencies of EEG and improve accuracy to 95.1 %. This work represents an advanced contribution for brain-like chip and promotes the systematization and diversification of artificial intelligence (**Chapter 4**).

Keywords: synaptic transistors, neural network, neuromorphic computing

摘要

基于 von Neumann 架构的传统逻辑运算规则具有并行运算的局限性，因此，具有仿生神经形态结构的计算系统，由于具备可以模拟人工神经网络（ANN）的架构和可以并行更新数据等特点，引起了类脑计算研究员们的广泛关注。为了构建神经网络系统的核心单元，我们提出了用于多级存储和并行计算的多种突触薄膜晶体管，并对其进行深入研究，用以模拟生物突触的特征行为和功能。现在为止，两端器件的类脑器件的发展已经接近商用，最新的研究进展是能够在百万级的集成芯片上运行完整的神经网络并执行识别任务。因此，三端突触器件需要在模型算法、软件架构、芯片设计，数据匹配和实际应用等相关联领域进行深入全面的挖掘和研究。根据各种机制和实现突触的原理，许多发表的工作已经研究了铁电突触晶体管、浮栅突触晶体管、电解质突触晶体管，驻极体突触晶体管，有机突触晶体管和光突触晶体管来实现神经元的生物行为。但是还须进一步探索神经形态器件的架构、突触的长/短期可塑性和其他生物突触行为，以同时实现信号传输、迭代学习和及时监测的功能。并为三端器件作为核心单元运行完整的神经网络奠定了坚实的基础。此外，简要总结了神经网络从第一代到第三代的发展历程。第一代神经网络使用数学和物理建模来模拟人脑神经网络并建立简化模型。人工神经网络主要利用权重和乘法来模拟突触特性，并利用加法来模拟树突的互连。接着对误差反馈策略进行了进一步的算法优化，并添加了各种框架和策略（如卷积、循环和残差），从而形成了第二代神经网络。与第一代相比，第二代神经网络可以用更快的速度和更高的效率执行更复杂的任务。进一步地，为了更好地匹配人脑的工作机制（低功耗），第三代神经网络被提出以实现更高水平的生物神经模拟。

除了对于神经元和突触状态的建立，第三代神经网络还将时间的概念融入其框架中。它可以更准确地模拟大脑神经元的动力学，并以低能耗执行复杂的智能任务。

在初步的探究中，我们提出了具有典型和可靠突触行为的氧化铟（InO_x）/氧化铝（AlO_x）电解质栅晶体管（EGT)。核心是将锂（Li）离子掺杂到 AlO_x 固态介电层中以促进双电层（EDL）的产生，将离子掺杂到 InO_x 中以提高循环长时程增强/抑制（LTP/LTD）过程的稳定性并巩固突触可塑性。在实际应用方面，我们基于 G_{max}/G_{min} 比值和权重更新曲线（LTP/LTD）的非线度，并通过模拟实际的电导变化设计出了一个用于心电图信号识别的 ANN（第一代神经网络）模拟架构。该架构在生物信号预测和神经干预方面具有巨大的潜力。并且从混淆矩阵中获得的判断心血管异常的准确率首次达到 94.8%以上。本章节提出了一种基于离子迁移机制的神经形态薄膜晶体管，实现了基本的突触可塑性和非易失性，并将该特性应用于基础生物信号的识别任务（**第 2 章**）。

进一步地，在第二章研究工作的基础上。为了能够有效地控制电导的非易失性，我们使用采取了和第二章不同的刺激方式。更重要的是，构建提出了动态学习规则来模拟人脑在记忆和学习过程中的规律，并用以执行更加复杂任务。因此，我们顺势提出了一种基于二维材料（Mxenes)的可光电调制的突触晶体管，该晶体管通过混合电脉冲和光脉冲被有效地调节电导的非线性度和不对称性。根据所使用的残差网络可以放大标签之间的差异的优点，因此，特别地将该网络融合此突触器件特有的动态学习规则，以显著提高高度相似数据类型的识别准确率。针对实现硬件和软件深度结合这一目标，高度同源数据库将使用经典的兔 IgG 抗原作为比色酶联免疫吸附测定（c-ELISA）传感靶点。结合硬件学习规则的神经网络把识别率从 80.9%（基准）提高到 87.2%，同时还可以实现快速收敛。因此，光电混合刺激也显著地将训练周期的迭代更新时间缩短到

了 11.6s，这一优势归因于光电效应加速了离子恢复的弛豫过程。进一步地，为了验证我们提出的动态学习规则的鲁棒性，将硬件中的动态学习策略进一步扩展到 LSTM 神经网络和标准数据集（Cifar10 和 Cifar100）。本章工作探究出了突触更新规则的关键参数，并且为免疫学中免疫蛋白定量分析检测奠定了基础，为根据突触器件中突触可塑性的不同特点定制专属的神经网络和识别任务奠定了基础（**第 3 章**）。

第三，根据前面两章探究的结果和经验，我们下一步深入探索神经器件的潜在功能，匹配最符合生物特征的神经网络，进而构建整体神经网络架构。结合突触可塑性的脉冲神经网络 （SNN)（第三代神经网络), 由于其具备时序相关性和低功耗等特点而具有巨大的超大规模并行计算潜力。其中 LIF 模型和尖峰时间相关塑性（STDP）是 SNN 的核心和特定组成部分。综上，我们构建的神经形态器件首次通过沸石咪唑盐框架（ZIFs）作为突触晶体管的重要组成部分来模拟 SNN 网络。此外我们还挖掘出此器件具备的三种生物功能。神经元之间的三种典型功能，即记忆功能、突触权重调节和膜电位产生，分别通过短期记忆/长期记忆（STM/LTM）、长时程抑制/长时程增强（LTD/LTP）和 LIF 得到有效模拟和展示。进一步地，不同于前两章节，突触晶体管中的 STDP 特性将用于迭代更新权重。该更新规则基于突触前脉冲和突触后脉冲之间的时间间隔(时序相关性）。除了基础的模拟之外，我们还实现了将突触后电流直接连接到 LIF 电路（超大规模集成电路（VLSI））进行模拟。该电路可以基于膜电位的阈值将高频信息转换为稀疏脉冲。搭建的主要三种模块（泄漏积分器块、点火/检测器块和频率自适应块）瞬间释放累积电压以形成脉冲。匹配的相关应用是将稳态视觉诱发电位（SSVEP）重新编码并通过 LIF 滤波形成新的脑电图（EEG）。结合突触晶体管时序特性的 SNN 被设计用于识别 40 种不同频率的新 EEG，并将原有的准确率提高到 95.1%。本章整体实现了三个方面的突破和创新，突触晶体管有了初步的膜电位阈值特

性，SNN 和 STDP，LIF 的兼容性模拟，复杂的高频信息可以通过神经器件得到滤波。此章节工作促进了以三端神经器件为核心的类脑架构的系统化和多样化（**第 4 章**）。

关键词：突触薄膜晶体管，神经网络，神经形态计算

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As time goes by, my doctoral research has come to an end. This is the most unforgettable, exciting, meaningful, and hardworking four years of my life. I would like to take this opportunity to thank everyone who has helped me in my life and studies. Without their continuous support and kind encouragement, my research and life would be very difficult and tortuous. Firstly, I would like to thank my supervisors Prof. Chun Zhao, Prof. Cezhou Zhao, and Prof. Wen Liu for their continuous support and guidance. They gave me the opportunity to acquire academic knowledge, as well as the resilience to overcome difficulties and the courage to persevere. I would also like to extend my sincere gratitude to my co-supervisors Prof. Harm van Zalinge. Especially, I would like to thank Prof. Chun Zhao, during my doctoral research, he often communicated with me and shared his insights on academia and life.

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Qinan Wang

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List of Publications

Journal Papers

Q N Wang, T S Zhao, C Zhao*, W Liu*, L Yang, Y N Liu*, D Sheng, R X Xu, Y T Ge, X Tu, H Gao, C Z Zhao. Solid State Electrolyte Gate Transistor with Ion Doping for Bio-signal Classification of Neuromorphic Computing, 2101260, Advanced Electronic Materials (2022).

Q N Wang, C Zhao*, W Liu*, I Z Mitrovic, H van Zalinge, Y N Liu, C Z Zhao. Synaptic Transistors Based on Transparent Oxide for Neural Image Recognition, 108342, Solid-State Electronics (2022).

Accept: **Q N Wang**, Y Sun, R X Xu, C R Li, C B Wang, W Liu*, J M Gu, L Yang, X Tu, H Gao, C Zhao*, Z Wen*. Synaptic Transistor with Multiple Biological Function Based on Metal-Organic Frameworks Combined with LIF Model of Spiking Neural Network to Recognize Temporal Information. Microsystems & Nanoengineering (2023).

Accept: **Q N Wang**, S X Duan, J H Qin, Y Sun, S H Wei, P F Song*, W Liu*, J M Gu, L Yang, X Tu, H Gao, C Zhao*. Dynamic Residual Deep Learning with Photoelectrically Regulated Neurons for Immunological Classification. Cell Reports Physical Science (2023).

Minor revision: S Y Wang, **Q N Wang**, M Li, Y X Fang, S S Shao, T H Xie, C Zhao*, L J Liang*, J W Zhao*. Roll-to-Roll Printed Large-area Flexible Carbon Nanotube Synaptic Photogating Transistor Arrays for Image Recognitions. Nano Energy (2023).

Accept: T H Xie, **Q N Wang**, M Li, Y X Fang, S S Shao, W B Yu, S Y Wang, W B Gu, C Zhao*, M H Tang*, J W Zhao*. Carbon Nanotube Optoelectronic Synapse Transistor Arrays with Ultralow-Power-Consumption for Stretchable Neuromorphic Vision Systems. Advanced Functional Materials (2023).

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Q N Wang, C Zhao*, W Liu*, H V Zalinge, Y N Liu, L Yang, C Z Zhao. All-Solid-State Ion Doping Synaptic Transistor for Bionic Neural Computing. International Conference on IC Design and Technology (ICICDT), 2021, Dresden, Germany.

D Sheng, R X Xu, **Q N Wang**, C Zhao*. Spiking Neural Networks for digital hand-written number recognition. International SoC Design Conference (ISOCC), 2022, Kangwon-do, Korea.

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List of Abbreviations

Term	Initial components of the term
2D	two-dimensional
2-Me	2-methoxyethanol
AFM	atomic force microscope
Al	aluminum
$Al(NO_3)_3$•9H2O	aluminum nitrate nonahydrate
AlOx	aluminum oxide
D	drain
EPSC	excitatory postsynaptic current
HCl	Hydrochloric acid
IDS	drain current
In	indium
InO	indium oxide
Li	lithium
LTD	Long-term depression
LTM	Long-term memory
LTP	Long-term potentiation
MNIST	Modified National Institute of Standards and Technology
NL	non-linearity
O	oxygen
PPF	Paired-pulse facilitation
RGB	Red,green, and blue7676666776qw21

STM	short-term memory
TFTs	Thin-film transistors
UV	ultraviolet
VDS	drain voltage
VGS	gate voltage
Vth	threshold voltage
XPS	X-ray photoelectron spectroscopy
XRD	x-ray diffraction
ZrOx	zirconium oxide
Δt	time intervals
CMOS	Complementary metal oxide semiconductor
AI	artificial intelligence
GPU	graphics processing unit
ANNs	artificial neural networks
EGTS	electrolyte gate transistors
EDL	electrical double layer
ECG	electrocardiogram
c-ELISA	colorimetric enzyme-linked immunosorbent assay
μPAD	microfluidic paper-based analytical devices
LSTM	long short-term memory
SNNs	spiking neural networks
LIF	leaky intergrate-and-fired
STDP	spike timing dependent plasticity
ZIF	zeolitic imidazolate frameworks

VLSI	Very Large Scale Integration
SSVEP	Steady-State Visual Evoked Potentials
EEG	electroencephalogram
G	conductance
W	synaptic weight
BCI	Brain-computer interfaces
IF	Ingrate-and-fire
H-H	Hodgkin-huxley
MOF	Metal-organic frameworks
STs	Synaptic transistors
RRAMs	resistive random access memories
CIM	Computing in memory
POC	Point of care
CNN	Conventional neural networks
ΔG	Difference in conductance
IPSC	Inhibitory postsynaptic current
PTFE	polytetrafluoroethylene
RMS	Root mean square
$(In(NO_3)_3 \cdot xH_2O$	indium nitrate hydrate
M	mole
rpm	Revolutions per minute
G_{min}	Minimum conductance
G_{max}	Maximum conductance
PSC	postsynaptic current

G_p	potentiation conductance
G_d	depression conductance
P_{max}	maximum number of pulses
SNR	Signal noise ratio
MIT-BIH	Massachusetts Institute of Technology-Beth Israel Hospital
LHb	Lateral Habenula
LiF	lithium fluoride
PTFE	polytetrafluoroethylene
DI	deionized water
MAX	MAX-Ti_3AlC_2
CH_3CH_2OH	ethanol
ResNet	Residual Network
ΔW	weight difference
SEM	scanning electron microscopy
Nseff	effectively utilized conductance number
HIV	human immunodeficiency virus
V_m	membrane potential
C	capacitor
SCR	silicon controlled rectifier
ITR	information transfer rate
POC	point-of-care

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The determination of the doping concentrations in the dielectric and semiconductor layers is based on synaptic plasticity and the stability of the cyclic tests (Figure 2.9). As can be seen from the figure, when 5% lithium ions are doped in the dielectric layer, the exhibited synaptic plasticity is the best. The value of the stabilized conductivity is the highest. When 5% lithium ions are doped in the semiconductor

Chapter 1 Introduction

Section 1.1 Synaptic device and brain-like chip

Section 1.1.1 Synaptic device

There are about 10^{11} neurons and about 10^{15} synaptic connections in human brain. The synaptic structure is the key part of information transmission between neurons and the basic unit of human cognitive behavior. Therefore, the development of synaptic devices is of great significance for neuromorphological engineering. In recent years, brain-like neuromorphic devices are becoming an important branch of artificial intelligence and neuromorphic field, which will inject new vitality into the development of artificial intelligence in the future. The human brain is able to process large amounts of information at ultra-low power consumption, thanks to the plasticity of synapses in the human brain. If we can use nano-sized artificial devices to simulate biological synapses, artificial neural networks and even artificial brains will be realized. In the age of information explosion, the demand for storage capacity is increasing rapidly. The development of small-size multi-value non-volatile memory can be widely used in military and civil fields, which is in line with the major national needs. Tri-terminal memristor materials and devices are the best way to realize small size multi-value non-volatile memory and should be developed vigorously. Reducing energy consumption and improving efficiency is the ultimate development direction of information processing chips. Brain-like chips, with their inherent advantages of low power consumption and high efficiency, will become the final choice of information processing chips in the future and have a huge market prospect. Three-terminal memristor materials and devices are the basis for the construction of brain-like chips. It is of great practical significance to increase the investment in its science and technology. Nano-sized memristor resistors can be continuously adjusted and maintained by electric field, and are considered as the most promising information

electronic devices to simulate biological synapses. High performance memristors need to be based on specially designed nano-memristor materials, controlling electrons or ions to change the resistance of the memristor materials. At present, the function of realizing memristor by controlling ions is developing rapidly. The resistance can be adjusted continuously by controlling oxygen ions or metal ions to form conductive wires in the matrix of memristor materials. It is an international trend to develop CMOS-compatible memristor materials and process memristor devices using standard CMOS technology, which is the only way to obtain low-cost brain-like chips. At present, the following research contents need to focus on: the development of continuously adjustable multi-valued memristor, the construction of artificial neural network; A quantum memristor is developed and multi-value non-volatile memory is constructed to improve the stability of the memristor. Quantified the different defect formation and migration energies of different memristor material systems, and quantified the controllability and stability of conductive channels of memristor devices. To develop memristor devices based on carbohydrate materials, artificial neural network and biological neural network are fully integrated.

Section 1.1.2 Brain-like chip

With the upsurge of artificial intelligence (AI) sweeping all walks of life, the "Al chip", as the core of AI, has become popular. It is an essential core device for all intelligent devices, dedicated to processing Al related computing tasks. The field of Al chips is not only a competitive arena for semiconductor chip companies, but also Internet companies and cloud computing companies have released plans to launch chips. AI chips include two fields of content: one is the field of computer science, which simply refers to software, that is, research on how to design efficient intelligent algorithms; The other is the field of semiconductor chips, which is simply referred to as hardware, which is the study of how to effectively implement these algorithms on silicon wafers and turn them into final products that can be combined

with supporting software. Starting from the Industrial Revolution, machines have gradually replaced human repetitive manual labor and heavy manual labor. Nowadays, part of human mental and intellectual work can gradually be replaced by machines with artificial intelligence. This "intelligent machine" with AI chips has powerful computing and learning capabilities, and can operate independently. Intelligent machines can not only imitate human muscles to perform tasks, but also become replacements for brain functions. This intelligent machine will become increasingly popular and its performance will continue to improve. It will be widely used in face recognition, car driving, artistic creation, new material synthesis, new drug development, medical diagnosis, robotics, and people's daily lives. The emergence of Al's idea and the subsequent development of neural network mathematical models and algorithms have been accompanied by the evolution of semiconductor chips along the way. Although some people were studying human brain function in the 1930s and 1940s and trying to establish a mathematical model, it did not have a significant impact. Until 1957, the invention of the Perceptron, which simulates the human brain, was seen as the first breakthrough in "artificial neural networks.". The sensor was invented by Frank Rosenblatt, who worked at the Cornell Aerospace Laboratory at the time. As the simplest form of forward artificial neural networks, perceptrons have a simple structure, but they have the ability to learn and evolve continuously to solve more complex problems. In 2012, everything changed. A series of influential papers have been published, such as Alex Krizhevsky, Ilye Sutskever, and Hinton's "ImageNet Classification with Deep Convolutional Neural Networks", demonstrating their achievements in the lmageNet Image Recognition Challenge. Many other laboratories are already engaged in similar work. Before the end of the year, deep learning had become the front page of the New York Times and quickly became the most well-known technology in artificial intelligence. After that, the experimental results of deep learning in image recognition and speech recognition have been improved year by year, until they exceed the

recognition rate of humans, causing great attention and once again setting off an Al craze. It can be seen that Al and the development of semiconductor chips are closely linked **(Figure 1.1**). Without the rapid development of semiconductor chips such as GPUs in recent years, Al would not be so hot as it is today [1-5].

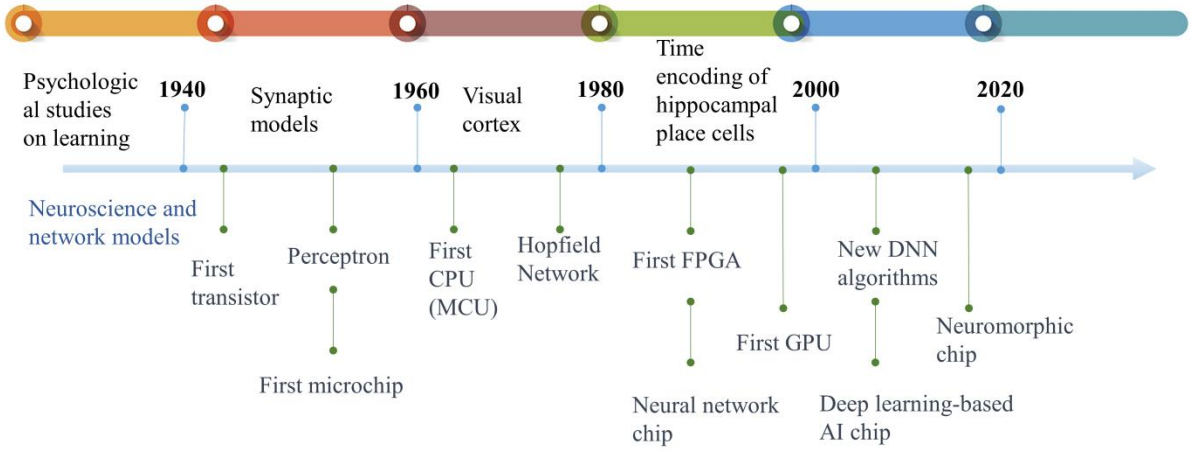

Figure 1.1 Comparison of the evolution of AI and chips.

Section 1.2 Synaptic plasticity in three terminal neural device

Section 1.2.1 Nonvolatile Memory: short-term potentiation and long term potentiation

STP and LTP are important mechanisms for information transfer between neurons. STP is a transient signal enhancement that typically lasts for several hundred milliseconds to a few seconds. STP can be achieved through rapid modulation of neurotransmitter release from presynaptic neurons, changes in postsynaptic membrane potential, and synaptic plasticity. STP is important for rapid information processing and short-term memory [6-9]. LTP is a persistent signal enhancement that can last for several hours to several days. LTP is mainly achieved through changes in postsynaptic membrane potential and synaptic plasticity. LTP is important for learning and memory formation because it can strengthen connections between neurons, thereby enhancing information transfer and storage. STP and LTP are important regulatory mechanisms for information transfer between neurons [6]. They can be regulated through various ways, such as neurotransmitter release, receptor density, presynaptic and postsynaptic neuronal activity, and membrane potential of neurons. Understanding the mechanisms and regulation of STP and LTP is crucial for understanding the fundamental principles of information transfer between neurons.

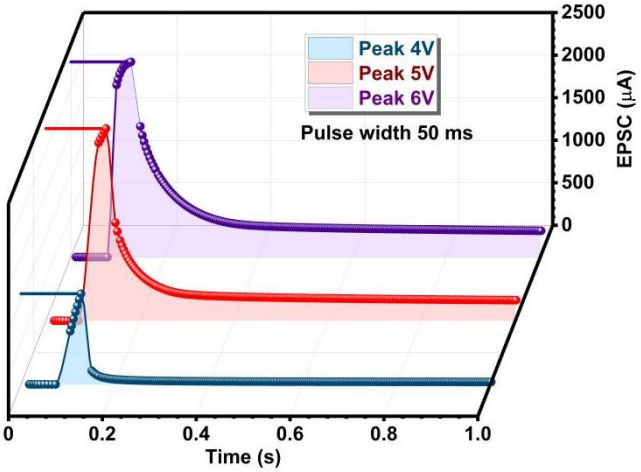

Figure 1.2 EPSC triggered by three pulses with different amplitudes (4, 5, and 6 V) at V_{DS} = 4 V.

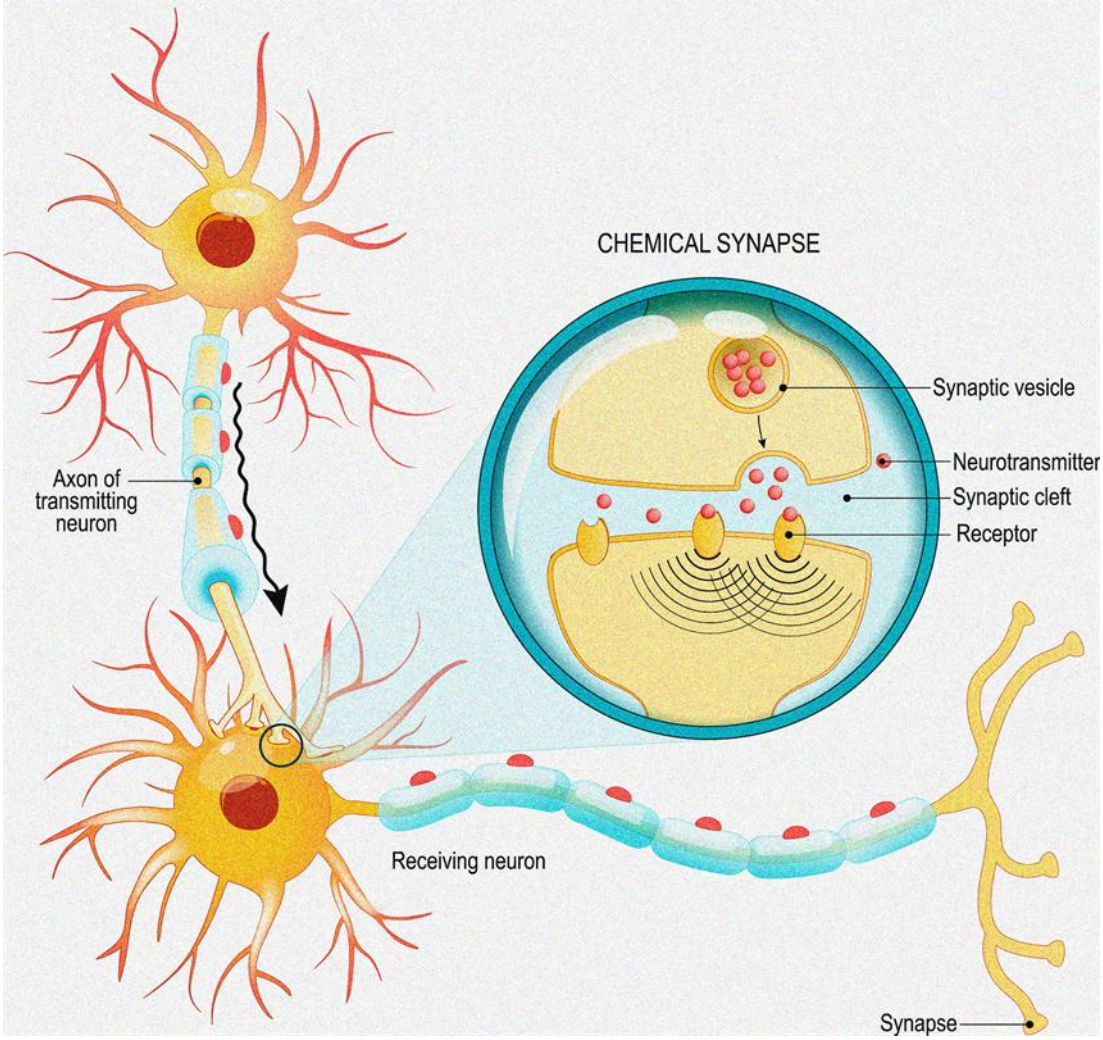

Figure 1.3 Biological synapse behavior similar to electrical synapses.

To simulate the synaptic memory-guided behavior inspired from short-term memory (STM) and long-term memory (LTM) in the human brain, the EGTs are stimulated by the appropriate and complex voltage pulses for STP and LTP [7]. The regular renewal of synaptic weight is the foundation of procedures for learning and memory, and the weight change is correlated with a presynaptic signal from the neurotransmitter. In a synaptic EGT, the channel conductance (G) represents the synaptic weight (W), and the conductance is also directly related to EPSC. To analyze the STP and LTP modes of the EGTs deeply, a series of voltage pulses (4, 5, and 6 V) with a duration of 40ms are applied to the gate terminal (**Figure 1.2**). Similar to biological synapses, electrical synapses are a mechanism for rapid signal transmission between neurons. The conductance of electrical synapses can change the

strength of connections between neurons by rapidly transmitting ion currents, thereby regulating the efficiency of information transfer between neurons (**Figure 1.3**). Thus, the conductance values of electrical synapses can represent the connection strength between neurons, similar to the synaptic transmission efficiency between pre-synaptic and post-synaptic neurons in biological synapses. In artificial neural networks, electrical synapse models can be used to simulate the behavior of biological synapses [8]. Similar to biological synapses, electrical synapse models can simulate the strength of connections between neurons by adjusting the conductance, thereby achieving information transmission and processing. In many applications, electrical synapse models can achieve efficient information processing and learning because they can quickly adjust the connection strength between neurons by regulating the conductance, thereby adapting to different tasks and environments [9].

Section 1.2.2 Synaptic weight array with LTP/LTD

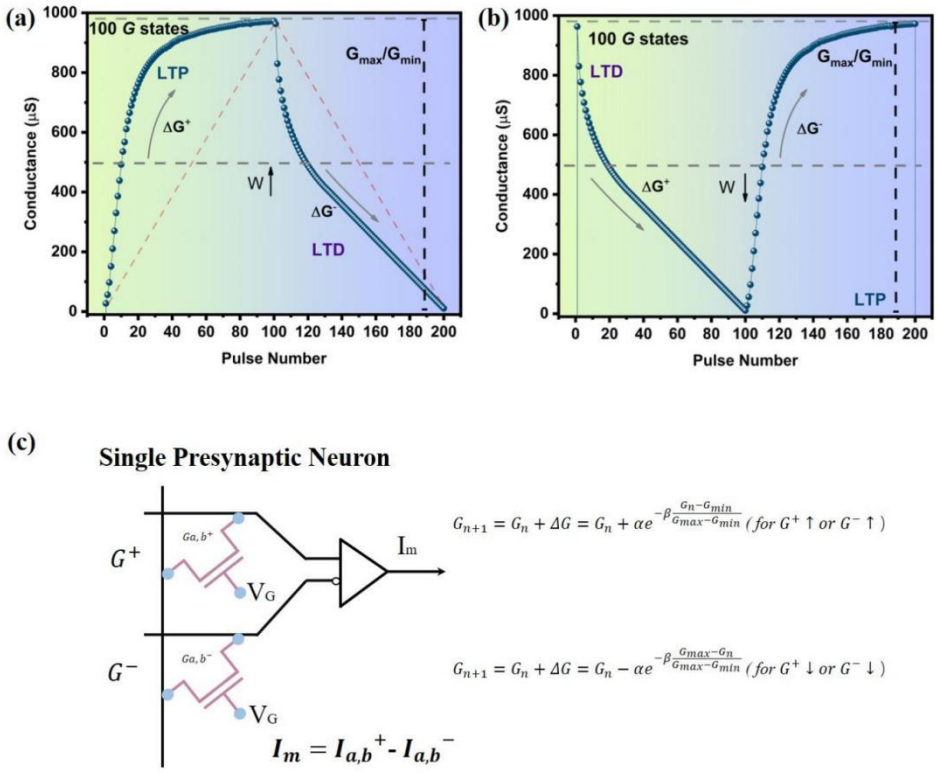

Figure 1.4 The weight update rule (a) The weight increase method based on the LTP/LTD curve of synaptic transistor. (b) The weight decrease method based on the LTP/LTD curve of synaptic EGT. (c) Two synaptic device represents a signle neural unit in neural network.

First, from the most basic ANN to briefly introduce the working principle. In short, the neural network is mainly divided into training and testing. The training part trains the weight value through the labeled data set. The most basic connection method is full connection. The measured conductance states of the synaptic devices had only positive values; however, the synaptic weight should have both positive and negative values for neuromorphic computing in ANNs. Therefore, the synaptic weight ($W = G^+ - G^-$) could be represented by the difference between the values of each conductance state (represented by G^+ and G^-) of two synaptic devices (**Figure 1.4**). In the weight updating process, the output vector (f_{output}) obtained by a sigmoid activation function was determined as mentioned above. Then, W was calculated using the difference between the output values (f_{output}) of the output vector and the label value (f_{expect}) of the input image [10]. To determine whether the synaptic weight was potentiated or

depressed, the sign of ΔW (sgn(ΔW)) should be calculated.

When the synaptic weight is in the potentiation phase (sgn(ΔW) > 0), G^+ should be increased and G^- should be simultaneously decreased (W ↑= G^+ ↑-G^- ↓). On the other hand, in the depression phase (sgn(ΔW) < 0), G^+ should be decreased and G^- should be simultaneously increased (W ↓= G^+ ↓-G^- ↑). The amount of conductance change (ΔG) of G^+ and G^- can be determined according to the following equations.

$$G_{n+1} = G_n + \Delta G = G_n + \alpha e^{-\beta \frac{G_n - G_{min}}{G_{max} - G_{min}}} \quad (1.1)$$

$$G_{n+1} = G_n + \Delta G = G_n - \alpha e^{-\beta \frac{G_{max} - G_n}{G_{max} - G_{min}}} \quad (1.2)$$

G_n and G_{n+1} denote the value of the present conductance state and the value updated using the equation, respectively. Further, parameters α and β denote the step size of the conductance change and the NL value, respectively.

In conclusion, the synaptic weight matrix in the iterative process makes the actual mapping relationship between output (f_{output}) and input consistent with the expected (f_{expect}) mapping relationship. Actual changed value of weight updating depends on the difference between the conductance state of two synaptic EGTs which extracted from the LTP/LTD curve [11].

In addition, the weight matrix that is iteratively updated in neural networks is simulated by an array of synaptic devices (**Figure 1.5**). The updating effect can be verified by changes in the values of each node on the array. Similar to biological synapses, the synaptic devices in the array can adjust their conductance values to simulate the strength of connections between neurons [12]. During training, the weight matrix is updated by adjusting the conductance values of the synaptic devices according to the error between the predicted output and the actual output. The updating effect can be monitored by observing the changes in conductance values of the synaptic devices on the array, allowing for real-time feedback and optimization. This approach has been shown to be effective in achieving high accuracy and efficiency in various neural network applications.

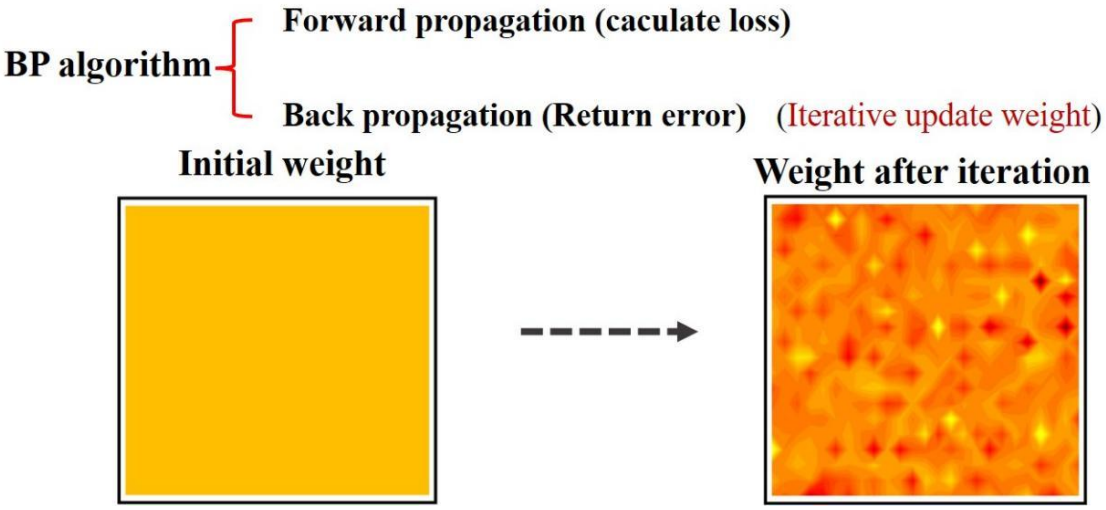

Figure 1.5 Neural network algorithm and weight updating process with synaptic weight array.

Section 1.2.3 Temporal correlation analysis (PPF, STDP, LIF)

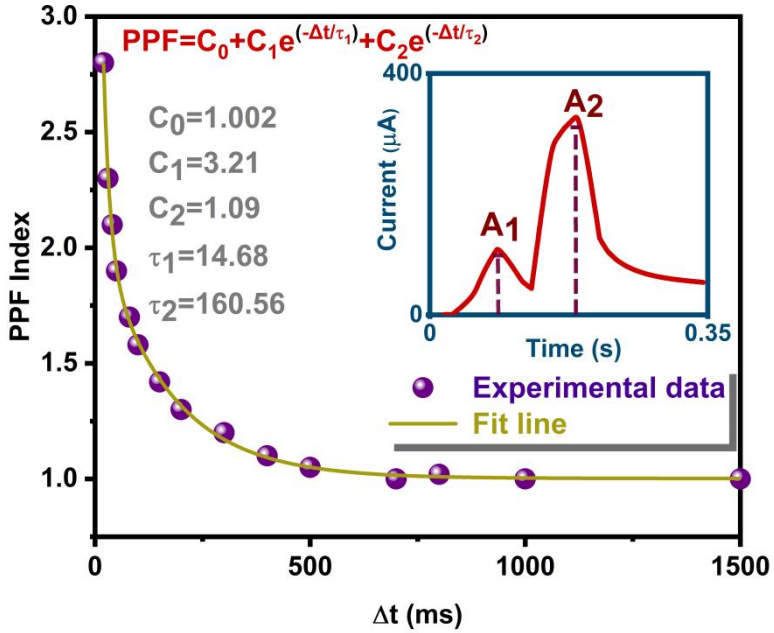

Figure 1.6 PPF index versus interval time Δt between two negative pulses (5 V). Inset: definitions of A_2 and A_1 with two successional 60 ms pulses.

PPF is a method used to study synaptic plasticity. It evaluates the short-term plasticity of synapses by observing signal transmission between two stimuli sent in a short time period. In PPF testing, the first stimulus (P_1) causes a certain degree of neuron excitation, while the second stimulus (P_2) enhances the effect of the first stimulus, resulting in a stronger neuron excitation response. If synaptic plasticity occurs, the effect of P_2 will be more pronounced [10-13]. The biological significance of PPF testing is to explore the physiological mechanisms underlying short-term synaptic plasticity. PPF is usually caused by factors such as an increase in the frequency of presynaptic neurons, changes in the membrane potential of postsynaptic neurons, and calcium ion concentration. An increase in the frequency of presynaptic neurons can promote the release of neurotransmitters, leading to an enhancement of the P_2 effect. Changes in the membrane potential of postsynaptic neurons and an increase in calcium ion concentration can also enhance the P_2 effect, thereby regulating the efficiency of synaptic transmission. PPF testing that can further evaluate the short-term plasticity of synapses [14-16]. In double-pulse testing, synapses receive two consecutive electrical stimuli,

and the time interval between the two stimuli can be adjusted. By adjusting the time interval, the response of synapses to stimulus frequency can be evaluated, thereby gaining a deeper understanding of the biological significance of synaptic plasticity.

Two stationary amplitude and width pulses (5 V, 60 ms) are applied to the presynaptic terminal with the interval of 2 s, and the postsynaptic current is evaluated with source-drain voltage (V_{DS}) of 1 V (**Figure 1.6**). EPSC will continue to decay after the end of the first pulse (A_1) stimulation before the arrival of the second stimulation until the Li^+ ions in the electrolyte return to the equilibrium position. If the second stimulus (A_2) is triggered before the whole remaining Li^+ ions are recovered, the remaining Li^+ ions will be superimposed by the second stimulus, furthermore, increase the amplitude of EPSC. The following expression can be described and evaluated as the PPF index.

$$PPF = \frac{A_2}{A^1} * 100\% \tag{1.3}$$

Under the minimum time interval, the double-pulse facilitation coefficient((A_2/A_1) is the maximum. The following function expresses the relation between PPF and Δt.

$$PPF = C_0 + C_1\, e^{\left(-\frac{\Delta t}{\tau 1}\right)} + C_2\, e^{\left(-\frac{\Delta t}{\tau 2}\right)} \tag{1.4}$$

Initial constants of rapid and slow phases C_0, C_1, and C_2 are 1, 23%, and 45%. The relaxation times are $\tau 1$(20 ms) and $\tau 2$(65 ms).

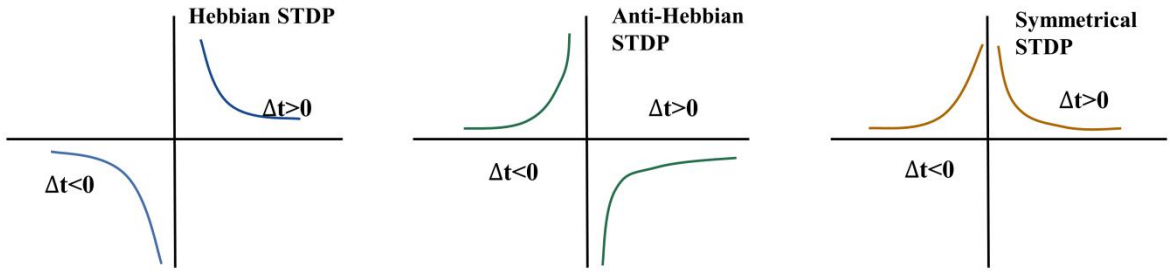

Figure 1.7 Multiple STDP curves (hebbian STDP, anti-hebbian STDP, and symmetrical STDP).

STDP is a synaptic plasticity mechanism that can be used in neuromorphic chips to achieve information transmission and synaptic connection regulation between neurons [1-15]. In

neuromorphic chips, STDP can be implemented by changing the synaptic connection strength to simulate information transmission between neurons. When repeated activation of information transmission between neurons occurs, the STDP mechanism in neuromorphic chips can enhance the synaptic connections between them, promoting the formation of memory and learning. Additionally, STDP can also be used to regulate the plasticity of information transmission and synaptic connections between neurons. The STDP mechanism in neuromorphic chips can regulate the enhancement and weakening of synaptic connection strength by simulating the time difference of action potentials between pre- and post-synaptic neurons, thus achieving the regulation and coordination of information transmission between neurons [16-18]. Therefore, STDP has significant implications in neuromorphic chips, as it can help achieve information processing and learning capabilities similar to those of biological neural networks, promoting the development of artificial intelligence and neuroscience. Hebbian STDP, anti-Hebbian STDP, and symmetrical STDP are three different synaptic plasticity mechanisms that differ in how the synchrony of pre- and post-synaptic neuron activity affects synaptic connection strength (**Figure 1.7**).

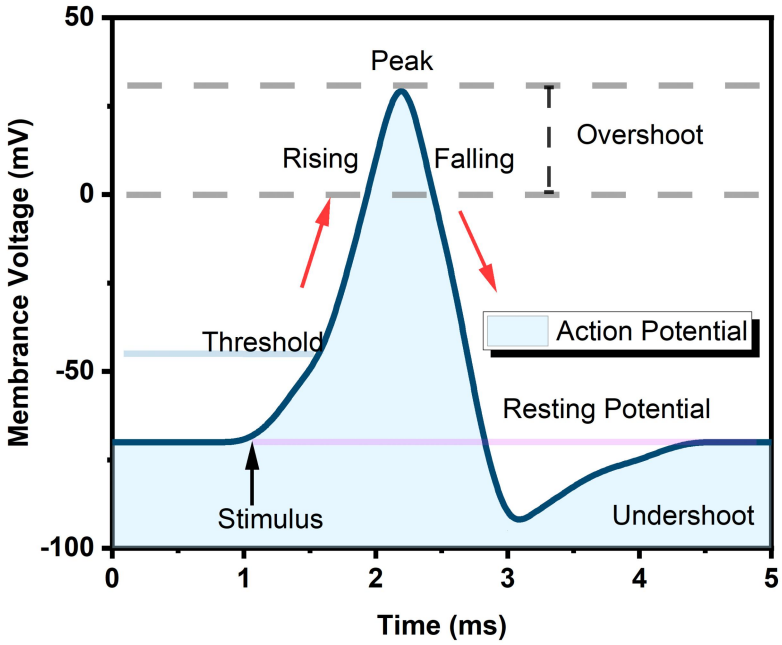

Figure 1.8 Fluctuation area of membrane voltage in biological neurons.

The LIF neuron model is commonly used to simulate the behavior of neurons. The LIF model can simulate how neurons receive and process signals from other neurons and fire a spike when a certain threshold is reached (**Figure 1.8**). Additionally, the leaky integration mechanism in the LIF model can mimic the gradual decrease of membrane potential in biological neurons over time. Membrane potential: The potential difference between the two sides of the cell membrane plays an important role in neuronal communication. When the membrane potential exceeds a threshold, a pulse is fired.

Resting potential: Neurons are in a polarized state and have a constant membrane potential.

Action potential: When a cell receives external stimuli, ions on both sides of the cell membrane move rapidly across the membrane, causing a change in membrane potential.

Leaky refers to the leakage of the membrane potential, meaning that if only one input is received by a neuron, it is not enough to exceed the threshold and the membrane potential will gradually fall back to the resting state due to the continuous exchange of ions inside and outside the cell membrane. Integrate refers to integration, meaning that a neuron receives all the pulses arriving at its axon terminal (from the previous neuron) that are connected to it. Fire refers to the firing of a neuron, meaning that when the membrane potential exceeds the threshold, the neuron will send out a pulse. After sending out the pulse, the neuron enters the hyperpolarization state, followed by the refractory period, during which even if it is stimulated, it will not respond, and the neuron no longer receives stimulation, maintaining the resting potential.

Section 1.3 Synaptic device based neural networks and overall architecture.

Section 1.3.1 Neural network for matching synaptic device.

ANN (Artificial Neural Networks), CNN (Convolutional Neural Networks), and SNN (Spiking Neural Networks) are common neural network models, each with their own characteristics (**Figure 1.9**). ANN is an artificial neural network model based on biological neuron models, and is suitable for various machine learning and data processing tasks. Its advantages include easy implementation and training, applicability to various problems, and high accuracy [10-17]. Its disadvantages are that it usually requires more computing resources and storage space, and has relatively weaker data processing capabilities. CNN is mainly used in image processing and computer vision, and has the following characteristics: local connection, weight sharing, and pooling. This enables CNN to effectively extract local information in images, while reducing the number of network parameters and computational complexity, resulting in fast processing speeds and good robustness. SNN is a neural network model based on spiking neurons, which can be used to simulate behavior in biological neural systems. SNN features include temporal properties, synaptic plasticity mechanisms, and sparse coding [11-18]. These characteristics make SNN suitable for simulating complex neural system behavior, such as vision, hearing, and motor control. In addition, SNN models have low power consumption, high efficiency, and fault tolerance, making them widely applicable in edge computing and biomedical applications. Therefore, these three neural network models have different characteristics and application scenarios. ANN is suitable for various machine learning and data processing tasks, CNN is suitable for image processing and computer vision, while SNN is suitable for simulating behavior in biological neural systems and edge computing applications.

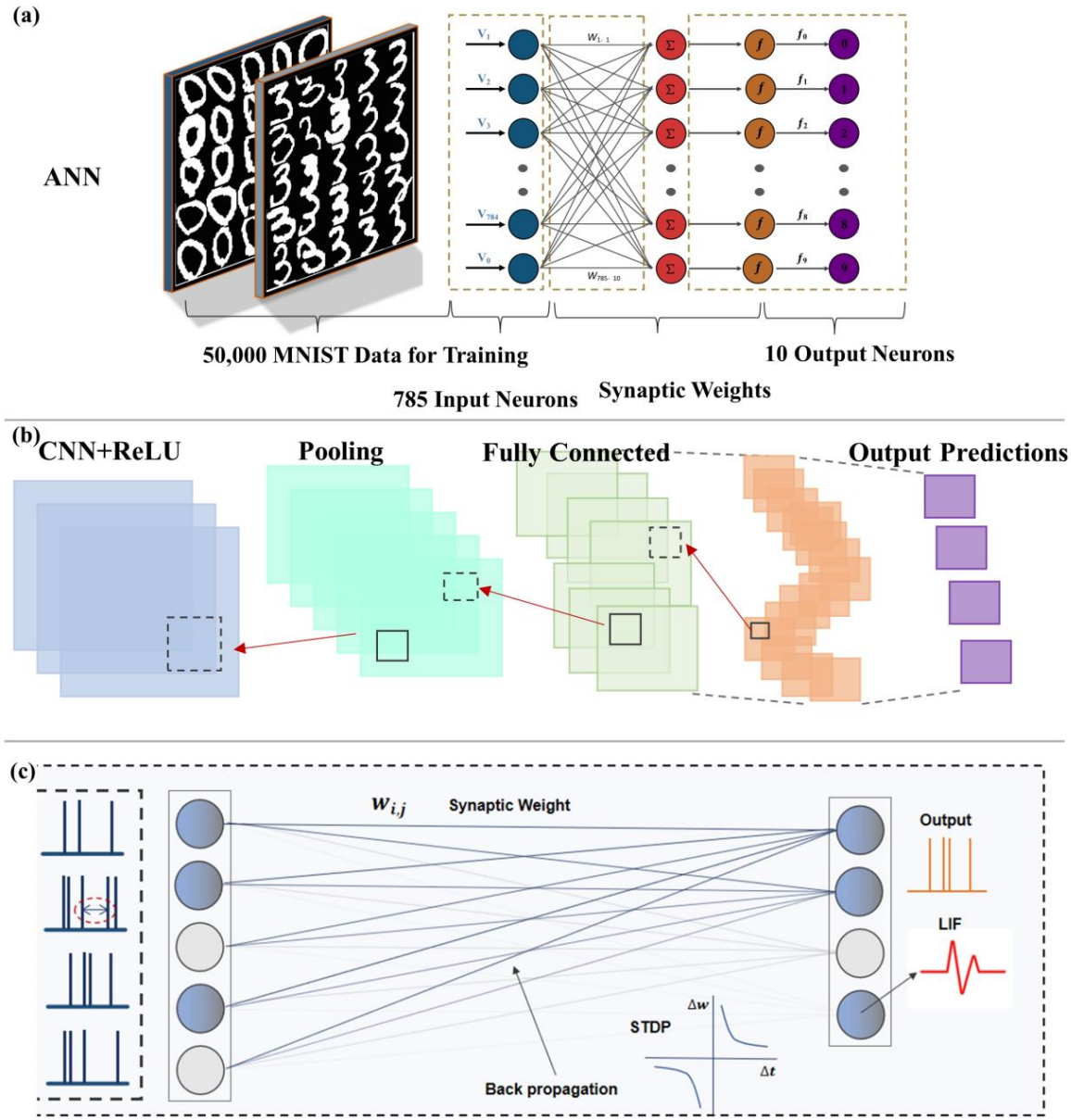

Figure 1.9 Three common neural network architectures. (a) ANN. (b) CNN. (c) SNN.

Section 1.3.2 Integrated architecture for hardware implementation of neural networks.

A neuromorphic chip is an interdisciplinary research based on neuroscience and computer engineering, which aims to simulate the computational principles and behavior of the human brain(**Figure 1.10**). Its typical architecture includes the following parts:

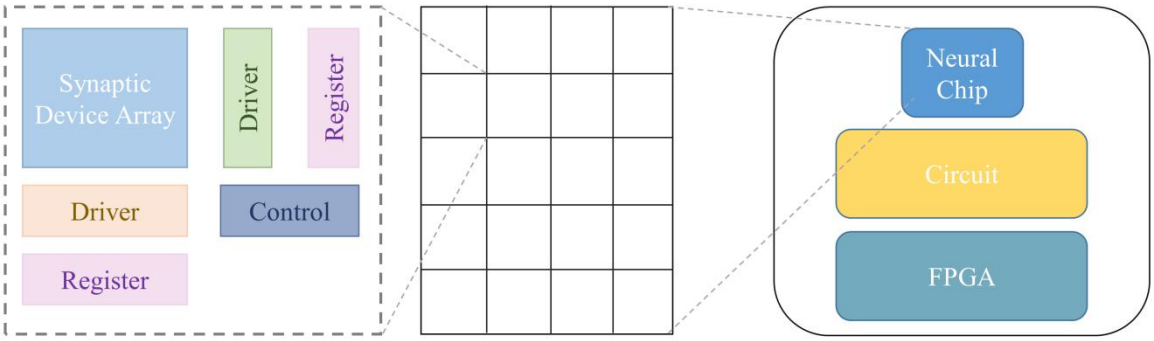

Figure 1.10 Simplified diagram of brain like chip architecture.

Synaptic device array: Synaptic devices array in neuromorphic chips typically use adjustable synaptic weight simulation devices, such as variable resistors and capacitors. These circuits can simulate the synchronicity of pre- and postsynaptic neuron activity and synaptic plasticity mechanisms [13-20].

Neuron circuits: Neuron circuits typically use pulse neuron circuits to simulate the behavior of biological neurons. These circuits can simulate the membrane potential, spike generation, and input and output of synapses.

Chip interconnection network: The chip interconnection network connects synaptic circuits and neuron circuits, as well as different neuron circuits. These networks typically use layered, hierarchical, and grouped structures to achieve efficient information transmission and processing.

Processing units: Processing units are used to implement the computation and control functions of neuromorphic chips. These units can use digital and analog hybrid methods to achieve efficient computing and low-power operation.

In summary, the architecture of neuromorphic chips aims to simulate the computational principles and behavior of the human brain and achieve efficient information processing and

control functions through synaptic circuits, neuron circuits, chip interconnection networks, and processing units.

Section 1.4 Object of the Thesis

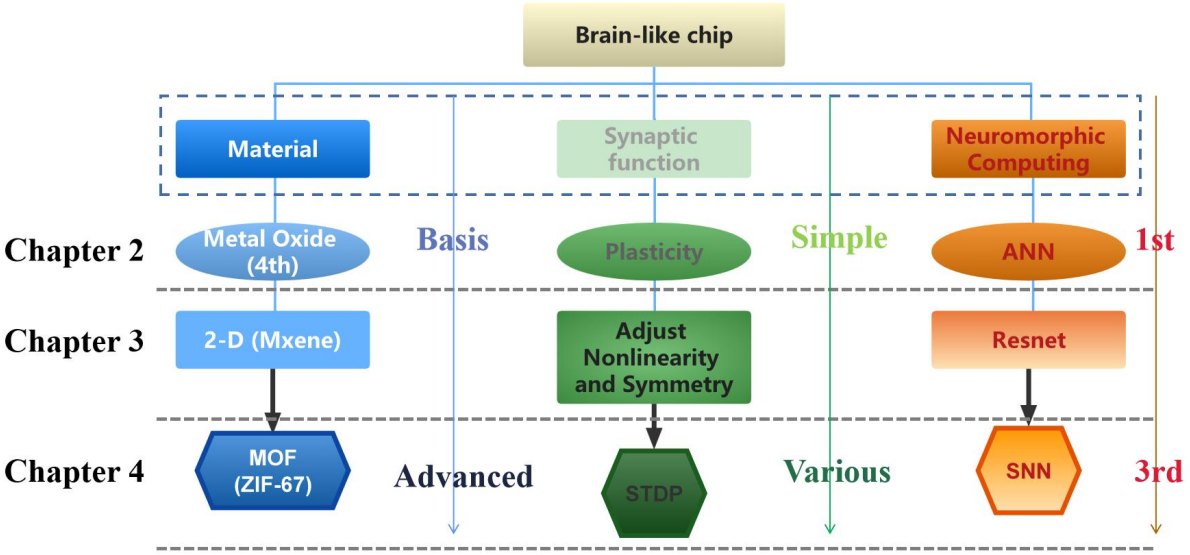

Figure 1.11 The overall article logic consists of three aspects: materials, synaptic functions, and neuromorphic computing.

The article elaborates on brain-like computing and its related applications from three aspects (material, synaptic function, and neuromorphic computing) through three chapters (chapter 2, chapter 3, and chapter 4) (**Figure 1.11**). From the perspective of materials, the logical relationship between metal oxides, 2D materials (Mxene), and MOFs as synaptic devices can be described as follows. Complexity: Metal oxides represent relatively simple materials with well-established properties, while 2D materials like Mxene introduce added complexity with unique features arising from their two-dimensional structure. MOFs are the most complex among these materials, offering highly customizable structures and functionalities. Evolution: The development of synaptic devices can be seen as an evolution from metal oxides to more advanced materials like Mxenes and MOFs. This progression demonstrates an increasing demand for customizable, high-performance, and multifunctional materials in the field of neuromorphic computing. Complementarity: While each material possesses its unique advantages, they can also complement each other when combined or integrated. For example, hybrid structures incorporating metal oxides, Mxenes, and MOFs can lead to novel devices with enhanced properties or additional functionalities, thereby pushing the boundaries of what

is possible with neuromorphic systems. Application-driven: The choice of material for a synaptic device depends on the specific requirements and constraints of a given application. Metal oxides, Mxenes, and MOFs each offer their unique advantages, and their use in synaptic devices may be dictated by factors such as power consumption, scalability, flexibility, or sensitivity [14-22].

For synaptic function, synaptic plasticity, the ability to adjust nonlinearity and symmetry, and the implementation of STDP are all critical aspects of synaptic devices in neuromorphic systems. The logical relationship between these three aspects can be described as follows. Synaptic plasticity serves as the foundation for learning and adaptation in both biological and artificial neural networks. It enables synaptic devices to change their strength and connectivity in response to neural activity, facilitating learning, memory, and adaptability in neuromorphic systems [21-24]. Adjusting nonlinearity and symmetry in synaptic devices is essential for achieving biological fidelity and enhancing computational efficiency. Nonlinear and asymmetric synaptic behavior can improve the implementation of learning algorithms, including STDP, and allow neuromorphic systems to process information more effectively and adapt to various tasks and inputs. STDP is a specific form of synaptic plasticity that is biologically relevant and crucial for unsupervised learning and temporal information processing in neuromorphic systems. The implementation of STDP relies on the interplay between pre- and post-synaptic neural activity and can be affected by the nonlinearity and symmetry of the synaptic devices.

For neuromorphic computing, artificial Neural Networks (ANNs), residual Networks (ResNet), and Spiking Neural Networks (SNNs) each play a unique role in neural computation. ANNs are computational models inspired by the structure and function of biological neural networks. They consist of interconnected artificial neurons that process and transmit information through weighted connections. ANNs have been widely used in a variety

of applications, such as image recognition, natural language processing, and recommendation systems. The primary role of ANNs in neural computation is to perform complex pattern recognition and classification tasks through supervised or unsupervised learning. ResNet is a specific type of ANN architecture designed to address the vanishing gradient problem that occurs in deep neural networks. ResNet introduces shortcut connections, also known as skip or residual connections, that allow the network to learn residual functions and improve the flow of gradients during backpropagation. These connections help mitigate the degradation of performance and accuracy in deep networks. ResNet has been particularly successful in computer vision tasks, such as image classification and object detection. The main role of ResNet in neural computation is to enable the efficient training of deep neural networks, leading to improved performance and generalization. SNNs are a distinct class of neural networks that more closely emulate the behavior of biological neurons. In SNNs, artificial neurons communicate through discrete spikes or events, rather than continuous values as in traditional ANNs. SNNs can process temporal information more effectively, making them suitable for tasks involving time-varying data, such as speech recognition or sensory processing. Additionally, SNNs can be more energy-efficient, as they only consume power when spikes are generated. The primary role of SNNs in neural computation is to provide a more biologically realistic and energy-effiANNs, ResNet, and SNNs each contribute differently to neural computation. ANNs provide a general framework for pattern recognition and classification, ResNet enhances the training of deep neural networks, and SNNs offer a more biologically plausible and energy-efficient approach to neural processing. These distinct roles enable the development of advanced and versatile neural computing solutions tailored to various tasks and applications.cient alternative to traditional ANNs for various learning and processing tasks.

Section 1.4.1 Achieving basic synaptic plasticity and simple neural networks

The chapter 2 demonstrates the practicability of the solution-processed oxide synaptic thin-film transistors. We have proposed an advanced weight update mechanism by voltage spike stimulation that the Li^+ ions accumulate and across between the AlO_x-Li and InO_x-Li layer. EPSC, IPSC, and PPF are basic information flow and the typical manifestation of short-range synaptic plasticity. In this work, we analyze the conductance and nonlinearity that significantly impact the learning accuracy rate based on the LTP/LTD characteristic. Besides simulating the matrix data recognition, the artificial neural network composed of crossbar EGTs array and back-propagation is then developed. Integrated memory and computing synaptic EGTs are utilized as the cardiovascular management system. The Li-doped solution-processed EGTs enriched a variety of synaptic devices alternatives and further evolved in the generation of neural morphological systems as a core component for an intelligent computational machine.

Section 1.4.2 By combining pulses to regulate the plasticity of devices and designing modern networks to match them.

The chapter 3 demonstrates the Al/InOx/MXenes/ZrOx-Li/Si/Al structure of synaptic transistor as bionic retina and proposes dynamic neuromorphic deep residual learning strategy for the recognition of ELISA_IgG in immunology. PPF, STP/LTP and EPSC are basic information flow, also are the typical manifestation of synaptic plasticity. Here, we analyze that the dynamic learning rate, update interval, and learning accuracy rate according to the various LTP/LTD curves which regulated separately by three modulation modes (Type I, Type II, and Type III). The synaptic devices stimulated by Type III have high linearity and symmetry, which is necessary to reduce the number of training epochs in the neural network. At the same time, the fast conductance recovery trend can reduce the interval of each calculation. Moreover, recognizing the Rabbit IgG of ELISA to demonstrate the potential in

immunology for immune protein detection and other neural networks (LSTM) composed of the Cifar10 and Cifar100 database are then developed to verify the robustness and feasibility. The synaptic transistor based on 2D materials and dynamic learning strategy enriches weight update process of neural morphological systems and further developed as bionic retina to successfully complete complex visual perception tasks.

Section 1.4.3 Develop multiple biological functions of devices and implement spiking neural networks

The proposed concepts in chapter 4 open many new avenues for the syanptic devices combined the neuron circuits as the core components of SNNs. From a deep learning perspective, the improved SNN makes it possible to explore the capabilities of more advanced biologically inspired neural models based on the LIF model and to benefit from its low computational complexity as well as its simplicity. From a neuro-scientific perspective, ZIF-67 SNNs system offers a new framework for modelling and understanding the neural dynamics that could benefit from the memory, synaptic plasticity and membrane potential. From a neuromorphic computing perspective, the design of in-memory accelerators combined with SNN-based STDP weight update rule will increase the adoption of spiking neural networks for SSVEP recognition applications (rate=95.1 %) and unlock the benefits of power-efficient neuromorphic hardware implementations. Finally, multi-functional synaptic transistor are integrated into the improved SNNs allows the use of existing or forthcoming network accelerators to be expanded for the whole SNN implementation and deployment.

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Chapter 2 Basic synaptic plasticity and simple neural networks (Solid state electrolyte gate transistor with ion doping for bio-signal classification of neuromorphic computing)

Section 2.1 Experimental Section

Section 2.1.1 Synthesis and fabrication of synaptic EGTs

Synthesis of EGTs: The AlO_x precursor solution was obtained by dissolving 2.5M aluminum nitrate hydrate ($Al(NO_3)_3 \cdot xH_2O$) in 5 ml 2-methoxyethanol (2-Me). AlO_x-Li precursor solution was obtained by mixing 2.5 M aluminum nitrate hydrate ($Al(NO_3)_3 \cdot xH_2O$) and 0.25 M indium nitrate hydrate with 10 ml deionized water. The InO_x precursor solution was obtained by dissolving indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$) into 20 mL deionized water. The InO_x-Li precursor solution was obtained by mixing 0.15 M indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$) and 0.015 M LiOH with 20 ml deionized water. All solutions were vigorously stirred under atmospheric conditions for 5 hours and filtered before spin coating using 0.25 μm polytetrafluoroethylene (PTFE) syringe filters, respectively.

Fabrication of Synaptic EGTs:

First, a heavily doped Si (n^{++}) substrate was cleaned by deionized water and dried under N_2 flow. Afterward, the processed substrate was further treated by Plasma for 15 minutes to allow the film surface hydrophilic treatment. The AlO_x and AlO_x-Li films were spin-cast with precursor solution at 3500 rpm for 20 s and then annealed for 30 mins at 200°C in the air atmosphere. The InO_x and InO_x-Li films were spin-cast with precursor solution at 3500 rpm for 30 s and then annealed for 1h at 200°C for the in the air atmosphere. The 30 nm thick Al source/drain(S/D) electrodes were fabricated by thermal evaporation through the shadow mask.

Section 2.1.2 Characterization and ANN simulation

Characterization:

A semiconductor parameter analyzer (Agilent B1500) with transistor characterization software under atmospheric conditions was operated to test the electrical properties of the Li doing InO_x/AlO_x synaptic EGTs. In order to measure the EPSC/ IPSC current flowing between the S/D electrodes, the 0.1 V steady voltage bias was applied to the postsynaptic terminal (V_{post}). Two sets of continuous weight control pulses (Voltage = ±4 V, width = 40ms Δt = 150ms) were added to the weight control terminal to describe each weight state. The surface roughness of the AlO_x, InO_x, AlO_x-Li, and InO_x-Li thin-films were analyzed by atomic force microscopy (AFM). The chemical compositions of dielectric and semiconductor layers were measured by X-ray photoelectric spectroscopy (XPS).

ANNs Simulation:

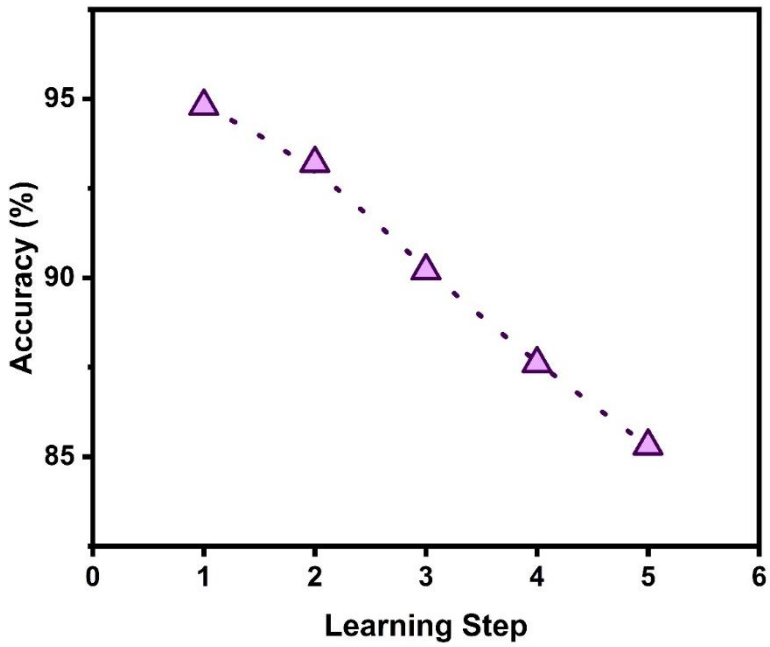

Figure 2.1 The effect the range of learning step on recognition rate.

The calculated conductance of synaptic EGTs in the crossbar array was applied with the positive synaptic weight value. The measurement of the neurocomputing in ANNs includes negative values. Subsequently, the synaptic weight ($W = G^+ - G^-$) was expressed as the

difference between the state of two synaptic devices (expressed as G^+ and G^-) between each conductance value. The 2001 input neurons corresponded to the 2000 sampling points of ECG and 1 bias input, and the 10 output neurons referred to 10 classes of timing signal. The initial weights were set up random fluctuation near 0 and the value between G_{min} and G_{max} normalized to (-1,1). When the random floating value is less than one learning step in random process, the initial weight will not affect the recognition rate (**Figure 2.1**).The synaptic weight matrix in the iterative process makes the actual mapping relationship between output (f_{output}-activation function) and input consistent with the expected (f_{expect}) mapping relationship. Actual changed value of weight updating depends on the difference between the conductance state of two synaptic EGTs (G^+ and G^-) which extracted from the LTP/LTD curve. The synaptic weight defined as the difference of conductance in two synaptic EGT which represent single neuron. When sgn(ΔW) > 0, the formula $W \uparrow = G^+ \uparrow - G^- \downarrow$ will be used. And when sgn(ΔW) < 0, the $W \downarrow = G^+ \downarrow - G^- \uparrow$ will be used.

Section 2.2 Results and discussion

Section 2.2.1 The mechanism and phenomenon of formation of electrical synapses

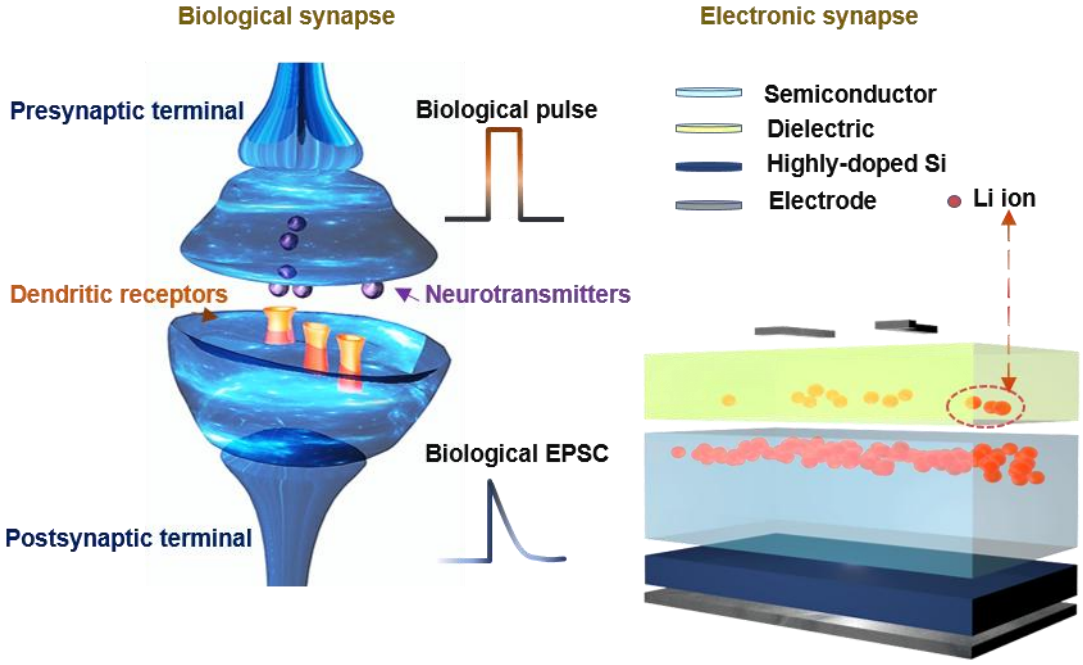

Figure 2.2 Schematics illustration of the biological synapse and the solution-processed synaptic EGTs.

Synapse is a juncture that conveys biological impulses between the presynaptic and postsynaptic terminals (**Figure 2.2, left**). Typically, neurotransmitters in the synaptic vesicle, which carry the biological and chemical information, travel through the synapse to enter the dendritic receptor. This mechanism transforms the chemical signal into an electrical pulse, eventually producing an EPSC [1-7]. Structural and functional resemblances between a biological synapse and a solution-processed artificial synapse are reflected about the gate electrode can be regarded as a presynaptic terminal and the drain electrode as a postsynaptic terminal (**Figure 2.2, right**). In addition to the mechanism of ion migration, the formation of synaptic thin film transistors can also be attributed to band barrier and quantum tunneling (floating gate transistor), polarization effect (ferroelectric transistor), and photogenerated carrier (optical transistor) [1-15].

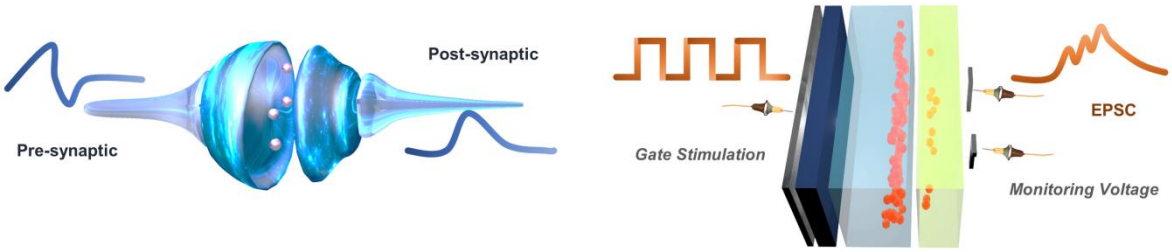

Figure 2.3 Schematic illustration of signal transmission in biological synapse and electrical evaluation for artificial synaptic plasticity.

The information transmission between presynaptic and postsynaptic terminals can be simulated by applying an electrical pulse to the gate and a monitoring voltage to the drain (**Figure 2.3**).

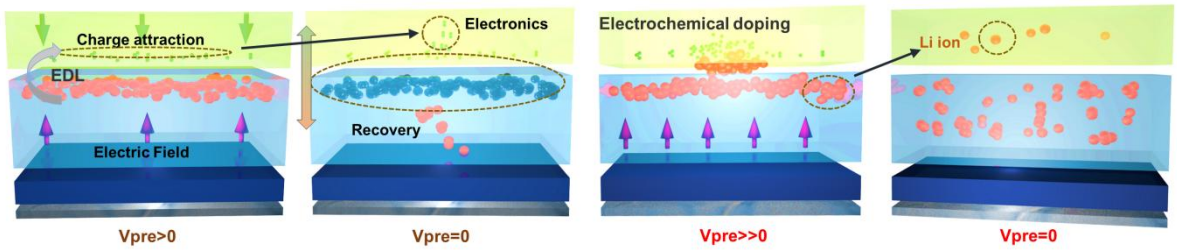

Figure 2.4 Li^+ ion migration in the dielectric layer under weak gate bias stimuli for short-term potentiation and Li^+ ion migration in the dielectric layer under strong gate bias stimuli for long-term potentiation.

In order to explain the phenomenon of conductance change in the dielectric layer due to Li^+ migration in detail, the schematic diagram of the movement of ions by voltage stimulation is proposed (**Figure 2.4**). Via two modules of ion electronic modulation processes, these Li^+ ions accumulate, and electrons are attracted near the dielectric layer/channel interface: electronic double layer modulation (under weak electric field in Figure 2.4 left side) and electrochemical doping (under enhanced electric field in Figure 2.4 right side). When the programmed V-pre is added to the EGTs presynaptic terminal, the limited radius and larger diffusion coefficient Li^+ ions effortlessly drift towards and cross the dielectric layer/channel interface due to the field accelerated ion migration [10-18]. With the weak spike stimulation (0-3 V), Li^+ ions shift under the electric field and accumulate at the interface and attract

electrons, resulting in short-term potential. With the enhanced spike stimulation (4-6 V), Li^+ ions across the AlO_x-Li/InO_x-Li interface, subsequently led to the formation of electrochemical doping. Li^+ ions and electronics gradually diffuse back to the original state of equilibrium with uniform composition when V_{pre} = 0 in both situations (weak and robust stimulation). According to the above mechanism, the hysteresis phenomenon in the transfer characteristic curve of EGT can be explained clearly. When a positive voltage applied to the gate from -2 to 4 V, the Li ions in the electrode migrate to the interface (form the EDL) and then intercalated into the channel with increasing the voltage amplitude (electrochemical doping) [19-21]. Then the positive reduced from the 4 V, the Li^+ ions accumulated in the interface recover into the dielectric layer (electrolyte) due to the concentration gradient of ions (internal field). With the negative voltage decrease to the -2 V, the ions migrate back to the electrode and the conductance restore the initial state.

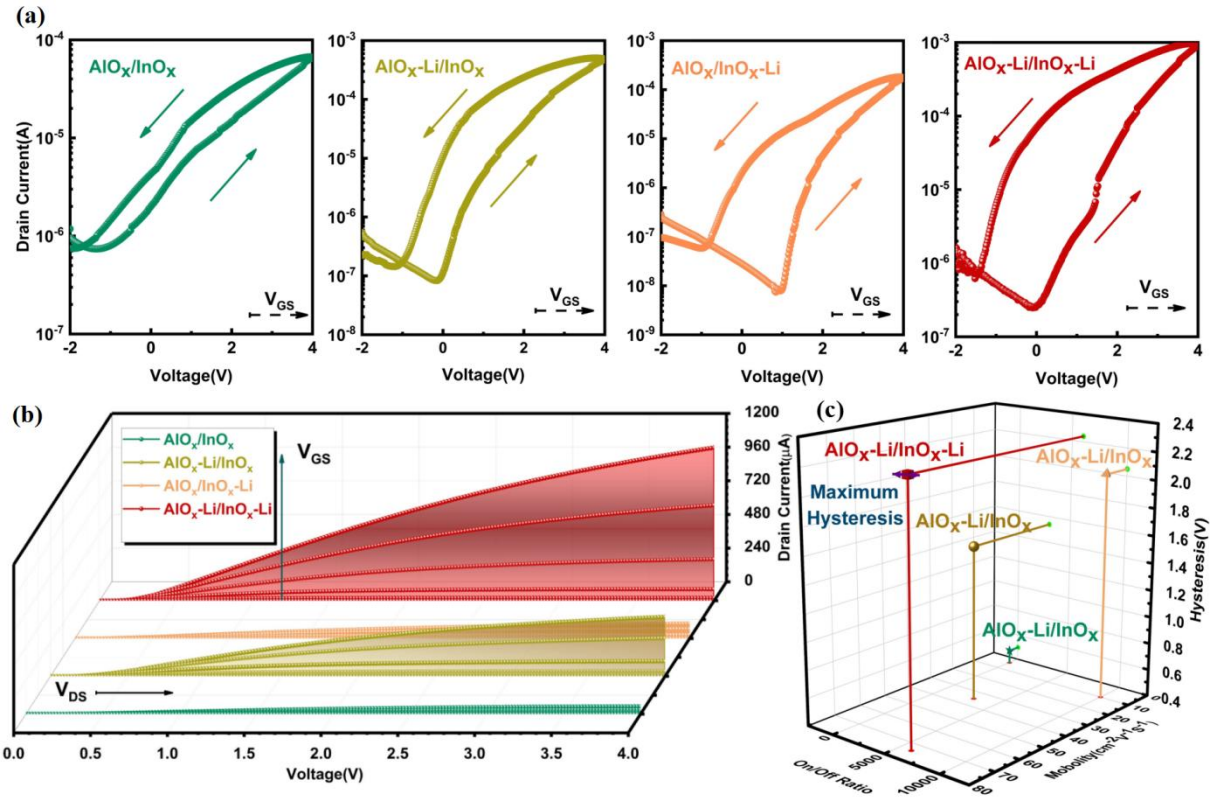

Figure 2.5 Characteristic parameters of synaptic EGTs (a) Transfer characteristics of four different doping EGTs (AlO_x/InO_x AlO_x-Li/InO_x, AlO_x/InO_x-Li, and AlO_x-Li/InO_x-Li). (b)

Output characteristic curves of the four different types EGTs. (c) Parameters (on/off current ratio, mobility, and hysteresis) of EGTs extracted from the transfer characteristics curves.

In order to compare the n-type transistor characteristic parameters of the synaptic EGTs with four doping types, the transfer curves of the system with V_{GS} (gate voltage) sweeping at a rate of 20 mV s^{-1} were evaluated and plotted (**Figure 2.5a**). The AlO_x-Li/InO_x-Li EGT demonstrate a clear counterclockwise hysteresis and a large change ratio of 2630 at V_g=0 due to the Li^+ ions migration. Different Li^+ ions doping concentration in AlO_x thin film would determine the formation strengths of electrostatic and electrochemical modulations. The synaptic plasticity of STP/LTP at different doping concentrations is analyzed and compared by applying incremental electric pulse to the gate [20-24].The electronic solution-processed synaptic transistors generate artificial EPSC and realize diverse synaptic plasticity based on the gate voltage applied to the n^+ Si bottom electrode activates a similar presynaptic pulse signal. The spin coated AlO_x and InO_x layers have the advantage of high k material, stability in the air and less defect states. The thin films were fabricated on heavily doped n^+-Si substrates by alumina (AlO_x), Li^+ ion-doped doped alumina (AlO_x-Li), indium oxide (InO_x), and Li^+ ion-doped doped indium oxide (InO_x-Li) precursor solutions. The AlO_x and AlO_x-Li layers (dielectric) were both annealed at 200°C, the InO_x and InO_x-Li layers (semiconductor) were both annealed at 300°C. The doping concentration in the InO_x layer is based on the stability of the cyclic test. The on/off current ratios are 100, 8000, 10000, and 6000, respectively belonging to AlO_x/InO_x, AlO_x/InO_x-Li, AlO_x/InO_x-Li, and AlO_x-Li/InO_x-Li EGTs. The migration of Li^+ within the AlO_x and InO_x layers contributes to the hysteresis behavior, which can be observed through the transfer characteristic curves of four synaptic EGTs. The large hysteresis indicates channel conductance changes, which is a significant synaptic characteristic in the EGTs for neural network simulation [13-27]. Hysteresis phenomenon is not only because of ion migration and ion pass through the interface between dielectric and

channel but also due to oxygen vacancy from the low-temperature technology. The output curves indicate the apparent pinch-off voltage and saturation current indicating good ohmic contact between Al electrodes and the InO_x or InO_x-Li channel layer (**Figure 2.5b**). Three-dimensional graphic displays the comparison of three parameters (on/off current ratio, mobility, and hysteresis) between four types of synaptic EGTs (**Figure 2.5c)**. It could be clearly observed that all the Li^+ doped EGTs, including AlO_x-Li/InO_x, AlO_x/InO_x-Li, and AlO_x-Li/InO_x-Li, exhibit more symmetrical hysteresis window than the AlO_x/InO_x device, which complies with the principle of ion migration.

Section 2.2.2 Physical characterization and effect of ion doping

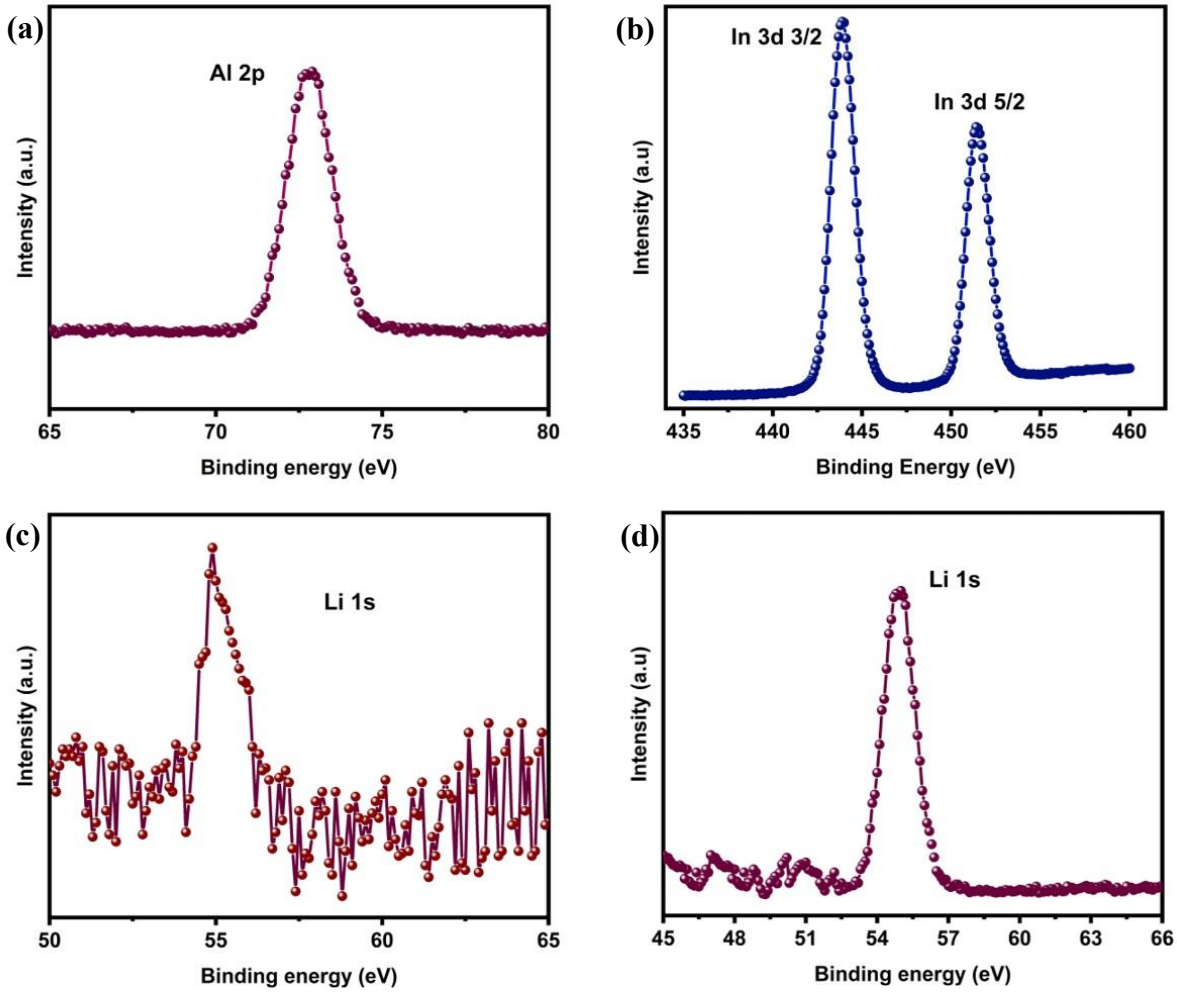

Figure 2.6. Analyze the chemical environment on the surface of the layer (a) XPS Al 2p spectra for dielectric thin-films. (b) XPS Al In 3d spectra for semiconductor thin-films. (c) XPS Li 1s spectra for dielectric thin-films. (d) XPS Li 1s spectra for semiconductor thin-films.

The chemical compositions of Li-ion doping synaptic EGTs are verified by X-ray photoelectron spectroscopy (**Figure 2.6**). The normalized Li 1s spectra of four type EGTs are obtained by standard the C 1s peak. In addition, the relatively smooth film surface can improve the yield and synaptic plasticity of the EGTs. Significantly, the smooth and uniform dielectric (AlO_x and AlO_x-Li) and semiconductor (InO_x and InO_x-Li) thin films are obtained by AFM deflection images (**Figure 2.7**). The root mean square (RMS) roughness of AlO_x, AlO_x-Li, InO_x, and InO_x-Li thin films are 1.552, 2.084, 0.380 and 0.306 nm, respectively. A simulated parallel neural computing system requires high plasticity and stability of the synapt-

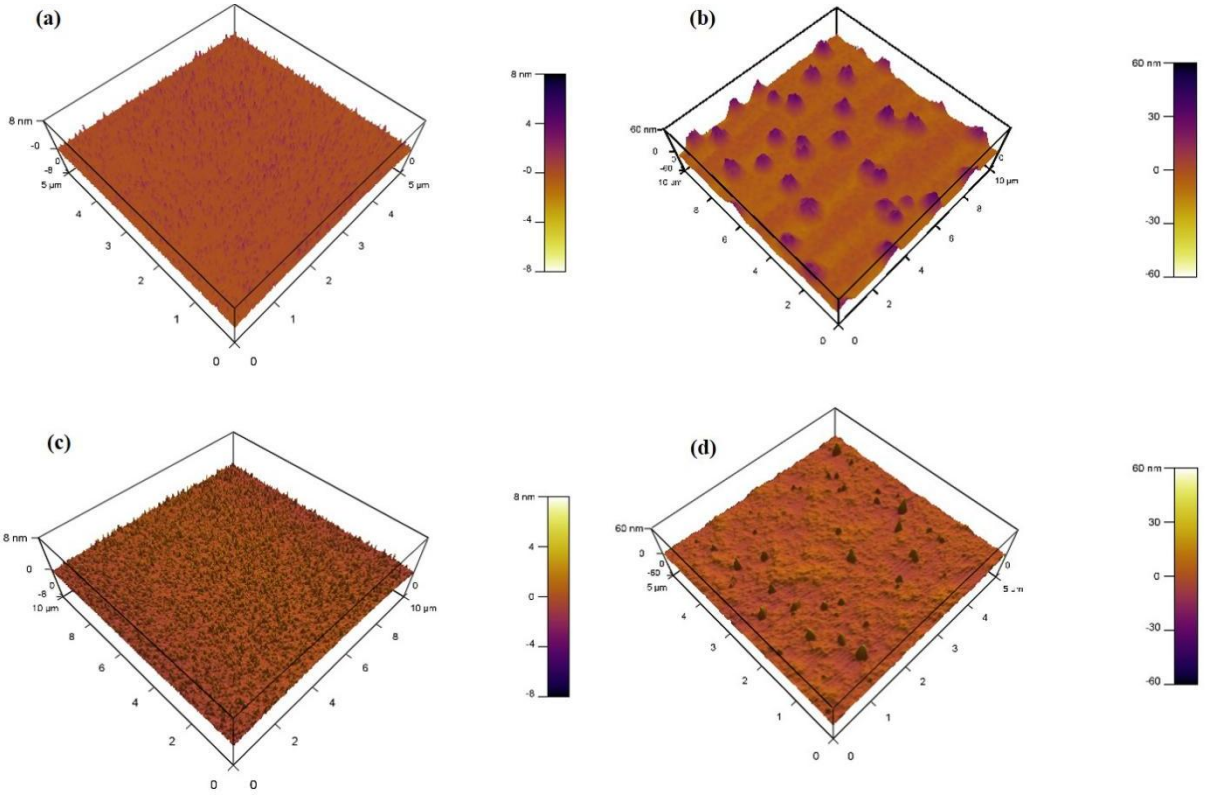

Figure 2.7 AFM images of (a) AlOx thin-films, (b) AlLiO thin-films, (c) InOx thin-films and (d) InLiO thin-films.

-ic EGTs to update synaptic weights accordingly. Similarly, the SEM image clearly demonstrates the synaptic device structure for the AlOx (30 nm)/InOx (15 nm) and the parameters about the channel are W=150 μm and L=10 μm (**Figure 2.8**).

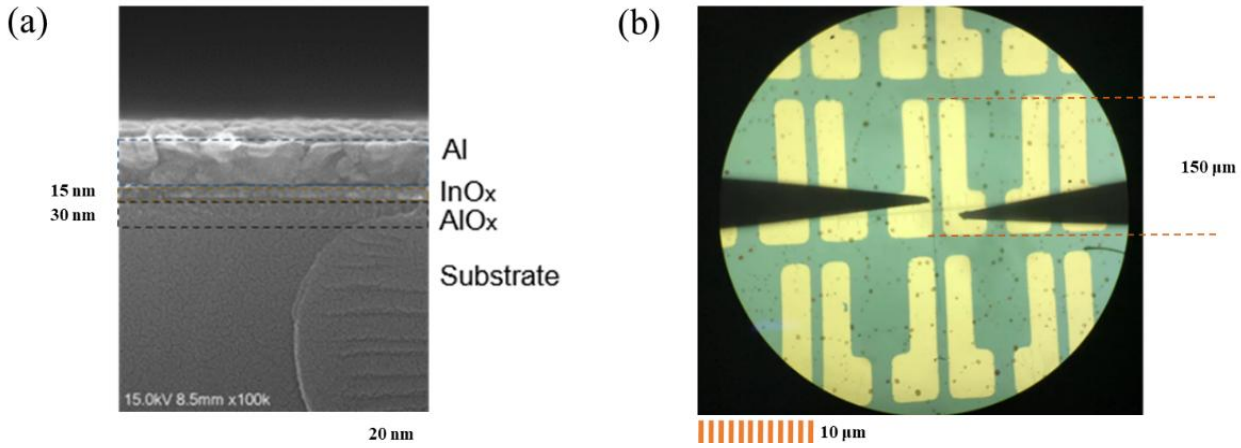

Figure 2.8 Cross sections and top view of synaptic EGTs (a) Scanning electron microscope image for the synaptic electrolyte gate transistor. (b) The actual example of the synaptic device (show the drain and source electrodes).

The determination of the doping concentrations in the dielectric and semiconductor layers is

based on synaptic plasticity and the stability of the cyclic tests (**Figure 2.9**). As can be seen from the figure, when 5% lithium ions are doped in the dielectric layer, the exhibited synaptic plasticity is the best. The value of the stabilized conductivity is the highest. When 5% lithium ions are doped in the semiconductor layer, the conductivity difference in the cyclic tests is the smallest, which is more conducive to large-scale preparation.

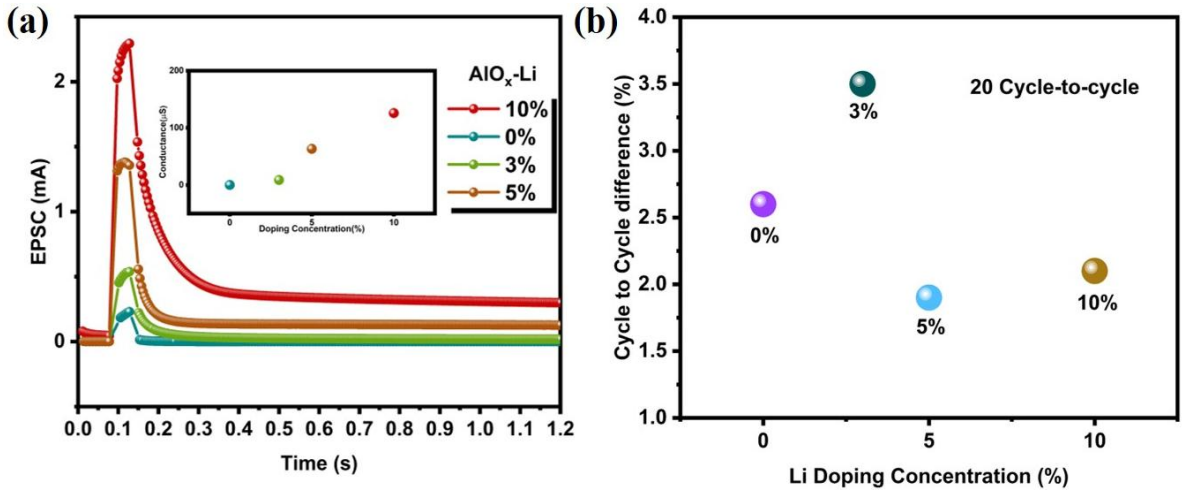

Figure 2.9 Synaptic plasticity and stability of transistor without Li doping (a) EPSC triggered by spike (6 V width = 50ms) for different Li doping concentration (0%, 3%, 5%, and 10%) in AlO_x thin-films. (b) The cycle-to-cycle difference for different Li doping concentration (0%, 3%, 5%, and 10%) in InO_x thin-films.

Section 2.2.3 Synaptic plasticity for solid state electrolyte gate transistor

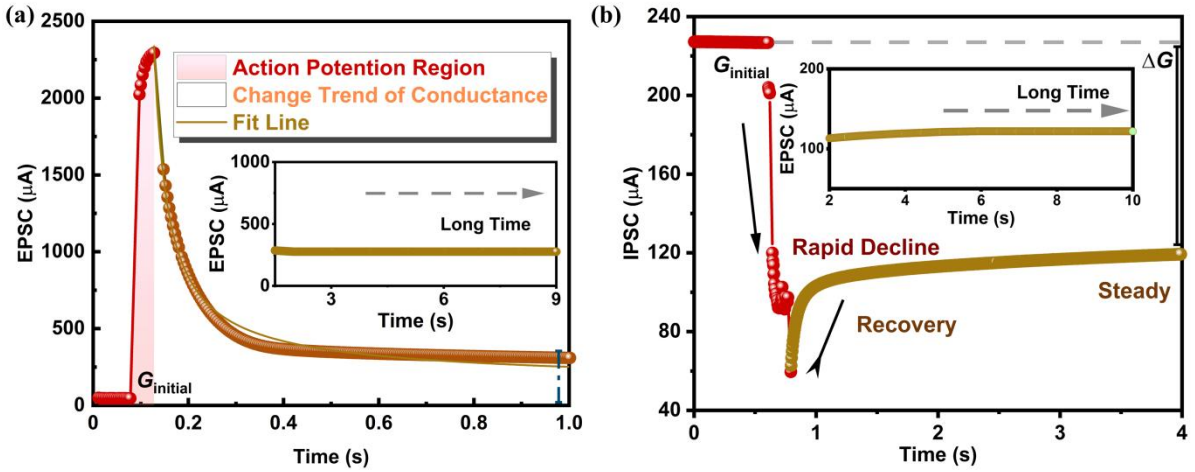

Figure 2.10 Typical EPSC and IPSC (a) EPSC property triggered by pre-synaptic spikes (6 V 50 ms) in 1 s. (b) IPSC property triggered by pre-synaptic pulses (-6 V 50 ms) in 4s.

EPSC and IPSC are the elemental information flow, processing processes, and synaptic plasticity for a neuron to carry out intricate computing and retain synaptic weight. In order to indicate the synaptic behaviors acquired from the typical EPSC and IPSC curves, the two numerical equivalent positive (6 V, 50 ms) and negative (-6 V, 50 ms) voltage spikes were applied to the gate terminal (Figure 2.10). The insert figures of EPSC/IPSC show long-term potentiation for the longer period [26-30]. The EPSC increased rapidly from the initial value to 2.4 mA after electrical stimulation, which is shown in the active region, and then decreased slowly from peak value to 310 μA in 1 s (**Figure 2.10a**). The postsynaptic current (PSC) stays steady as a result of no change in conductance prior to the operation of the pre-terminal voltage pulse. When a voltage pulse is applied to the gate of a synaptic transistor, lithium ions will migrate from AlO_x to the channel, resulting in an improvement in channel current and the formation of EPSC. When the pulse stimulation ends, the ions near the channel electrolyte interface will diffuse away from the interface due to the Li^+ concentration gradient [22-32]. Thereafter, the downward trend in the channel contributes to the inhibition of PSC when the presynaptic impulses are negative, thus generating an IPSC (**Figure 2.10b**). The IPSC includes the rapid decline region, recovery area, and conductance stability section. The

current after negative voltage stimulation changes from initial value 230 μA to steady 118 uA since Li^+ ions are considered to cross from the InO_x layer to the AlO_x layer.

Change of the conductance illustrates that the accelerated concentration of electrons/holes enhancement or suppression in the channel results from broad positive or negative voltage, resulting in a comparatively large (EPSC) and low (IPSC) conductivity than the original ones until the pulse is withdrawn [31-33]. The change of channel conductance is simultaneously triggered by the pulse voltage modulation of the gate. This partly originated by the oxygen vacancy in the dielectric layer. Under the action of the electric field, oxygen vacancies act as traps to attract electrons or holes into the AlO_x or AlO_x-Li layer. Interestingly, presynaptic neurons regulate EPSC/IPSC through neurotransmitter transduction, while gate electrodes control channel conductance through the transfer of the charge carrier.

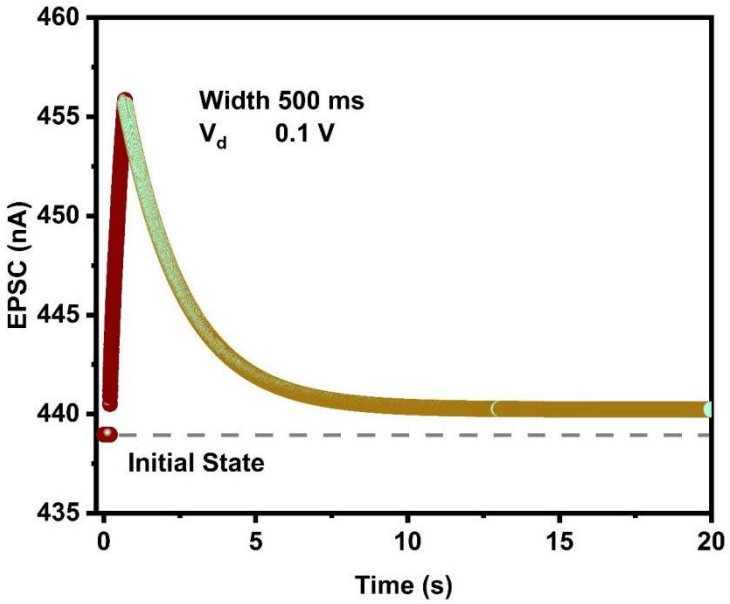

Figure 2.11 The energy consumption per spike of EGT extracted from the EPSC curve which is triggered by presynaptic spike (V_{gs}=3V, V_{ds}=0.1V, Pulse Width=500ms) in 20 s.

Further, to verify the low energy consumption of synaptic EGT, the energy consumption per spike of EGT is calculated by the Equation $E= I_{peak} \times t \times V$ =22.79 nJ (**Figure 2.11**). I_{peak} is the maximum value (455.8 nA) of generated EPSC, t is the spike duration (500 ms), and V is the voltage applied to the drain electrode (0.1 V).

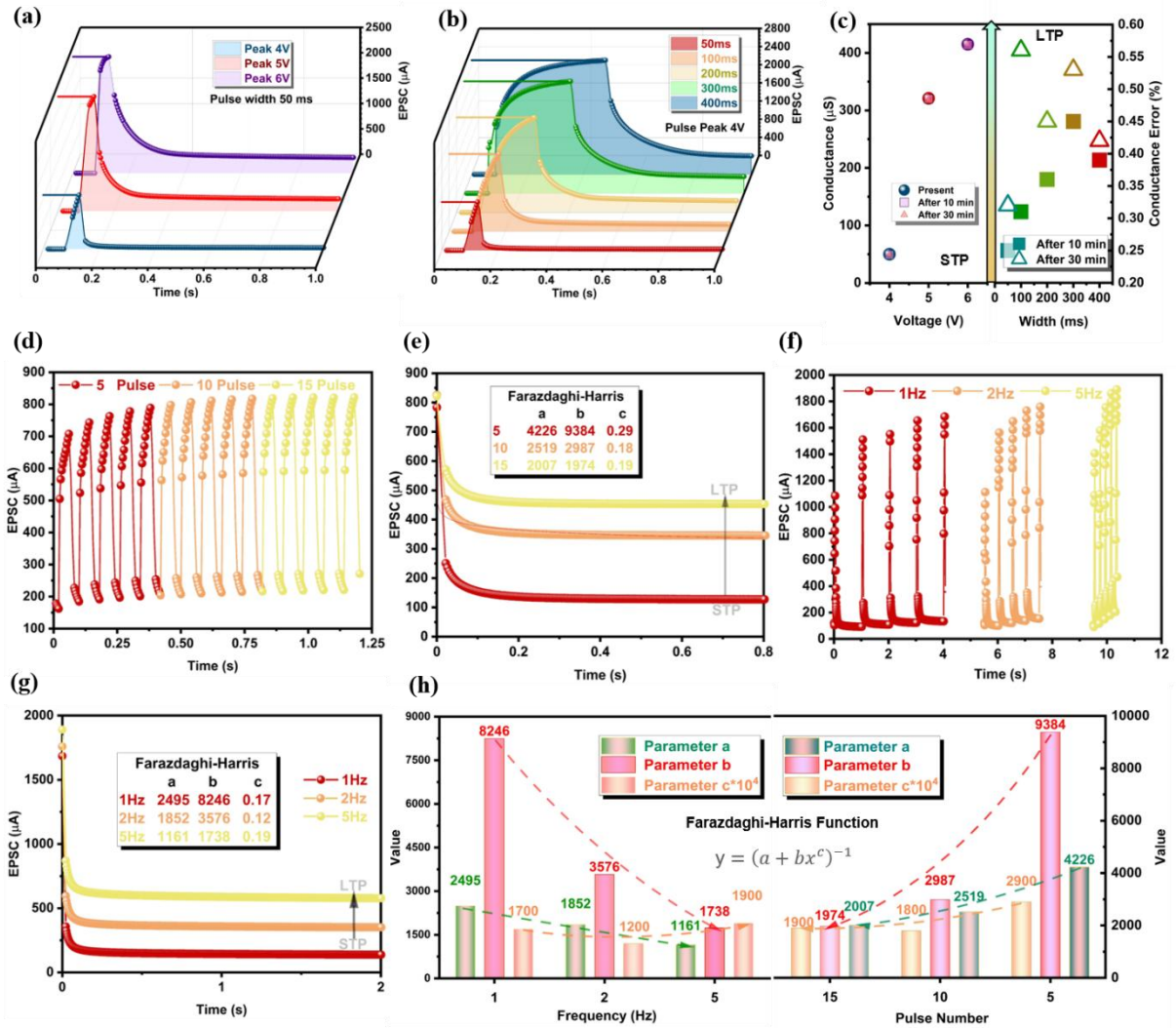

Figure 2.12 Synaptic plasticity under multiple conditional stimuli (a) EPSC triggered by three pulses with different amplitudes (4, 5, and 6 V) at V_{DS} = 4 V. (b) EPSC triggered by five pulses with different durations (50, 100, 200, 300, and 400 ms) at V_{DS}=4 V. (c) Stable conductance multi-level from STP to LTP for different voltages and widths. (d) EPSC stimulated by a sequence of 15 voltage pulses (5, 10, and 15 pulses) with the 50 ms period and 4 V amplitude. (e) STP to LTP conversion process in 0.8 s under 5, 10, and 15 presynaptic pulses. (f) EPSC stimulated by five continuous pulses (4 V, 40 ms) with different frequencies (1, 2, and 5 Hz). (g) Process of STP to LTP conversion in 2 s with different frequencies. (h) Fitting of the attenuation process to the curve of Farazdaghi-Harris function showing a trend of the three parameters (a, b, c).

To simulate the synaptic memory-guided behavior inspired from STM and long-term memory LTM in the human brain, the EGTs are stimulated by the appropriate and complex voltage pulses for STP and LTP [28-32]. The regular renewal of synaptic weight is the foundation of procedures for learning and memory, and the weight change is correlated with a presynaptic signal from the neurotransmitter [30-34]. In a synaptic EGT, the channel conductance (G) represents the synaptic weight (W), and the conductance is also directly related to EPSC. To analyze the STP and LTP modes of the EGTs deeply, a series of voltage pulses (4, 5, and 6 V) with a duration of 40ms are applied to the gate terminal (**Figure 2.12a**). The peaks of EPSCs are observed to escalate maximums (2.3 mA, 2.2 mA, and 1.1 mA), subsequently slowly decay to the stable value (380, 350, and 65 μA), respectively. Large values of EPSC indicate that ion migration has a significant effect on conductance. Considering that continuous spike input deepens synapse plasticity to be facilitated, a standard principle is proposed that maintains a 3-minute interval between every two tests to ensure the accuracy.

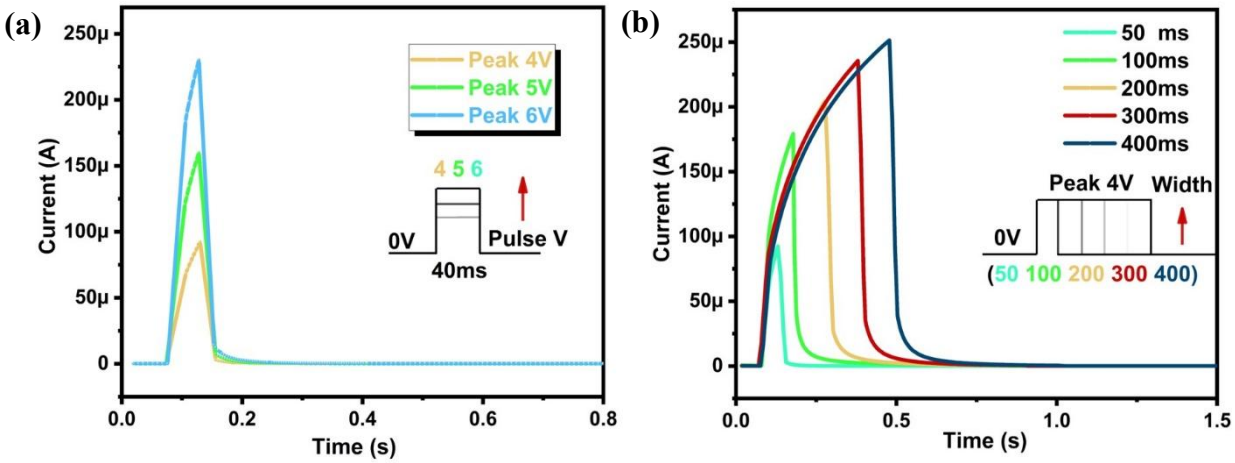

Figure 2.13 Synaptic plasticity of without Li ion doped (a) The EPSC triggered by the same width time (40 ms) pulses with three pulse amplitudes (4, 5, and 6 V) at V_{DS} = 4 V without Li ion doped. (b) The EPSC triggered by positive pulses (4 V) with five pulse durations (50, 100, 200, 300, and 400 ms) at V_{DS}=4 V without Li ion doped.

Meanwhile, the solution EGTs (AlO_x/InO_x) without Li doping has no STP-LTP response (**Figure 2.13**). This phenomenon further proves that Li^+ ion plays an irreplaceable role in

channel conductance update for neuromorphic computing. Therefore, the conversion from STP to LTP is similarly realized by increasing the presynaptic pulse width (**Figure 2.12b**). This figure indicates that the intensity of EPSCs rise linearly from 50 ms to 400 ms. These peak values (2.5, 2.4, 2.05, 1.7, and 1.1 mA) descend gradually to the stable value (481, 475, 302, 254, and 52 μA), which is also attributed to Li ions accumulate at the AlO_x/InO_x interface. Stimulated by different presynaptic pulse amplitudes and pulse widths, EGTs can realize multi-level storage for neural networks (**Figure 2.12c**). The figure also demonstrates the stability of long-term potentiation after 10 minutes and 30 minutes. The characteristic of maintain conductance for a long time further illustrates the excellent synaptic plasticity of EGT [31-36].

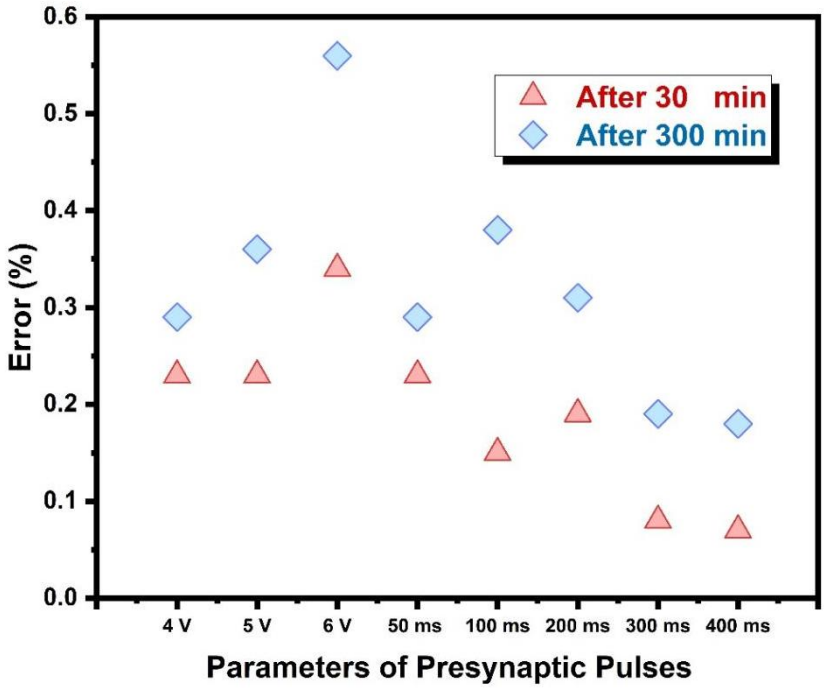

Figure 2.14 The 30 minutes and 300 minutes error after the presynaptic electric pulse stimulation.

Further, the differences between the initial conductance and the maintained conductance (refers to error) after 300 minutes are summarized to show the excellent level of stability due to the substantial part of errors below the 0.5% (**Figure 2.14**).

Conductance is positively correlated with the EPSC curve that has the potential for process controlling and parallel computing. Meanwhile, enough large difference between the maximum and minimum conductance (G_{max}, G_{min}) satisfies the neural calculation requirements. Moreover, the gate terminal is then stimulated by a variety of continuous spikes to achieve complex synaptic plasticity. The nonvolatile portion of conductance gradually increased to the saturation state with increasing the pulse number (5, 10, and 15) to demonstrate the effect of continuous multi-pulse on synaptic weight (**Figure 2.12d, e**). The transition from STP to LTP occurs as pre-terminal pulses increase from 5 to 15 mainly due to electrochemical doping effects. The initial conductance values increased from the 118μA and finally stabilize at 120 μA (5 pulses), 370 μA (10 pulses), and 490 μA (15 pulses) in 0.8 s, respectively. The three parameters of the Farazdaghi Harris function vary with the frequency and number of pulses (**Figure 2.12h**). All fast natural forgetting processes from STP to LTP are accurately fitted by the above function. Moreover, synaptic EGTs exhibit filter characteristics under different series frequencies (1, 2, 5 Hz) of presynaptic pulse signals (**Figure 2.12f, g**). With the series of pulses increases to 5 Hz, the solution-processed synaptic EGTs are applied to verify high-pass filtering characteristics. The potentiation of channel conductance from 180 μA to 620 μA with the frequency increasing from 1 to 5 Hz which can be observed in the case of the initial state value is 100 μA before stimulation. The EGTs with STP/LTP characteristic have limited transmitter release probability which are similar to the biological synapse, and the signal transduction process in neurons is effectively regulated. Consequently, these results can be confirmed that the signal transduction process in EGTs is effectively controlled and the EGTs acquired various electrical stimulation methods to further modify neural communication.

Section 2.2.4 Synaptic weight update process for neural network

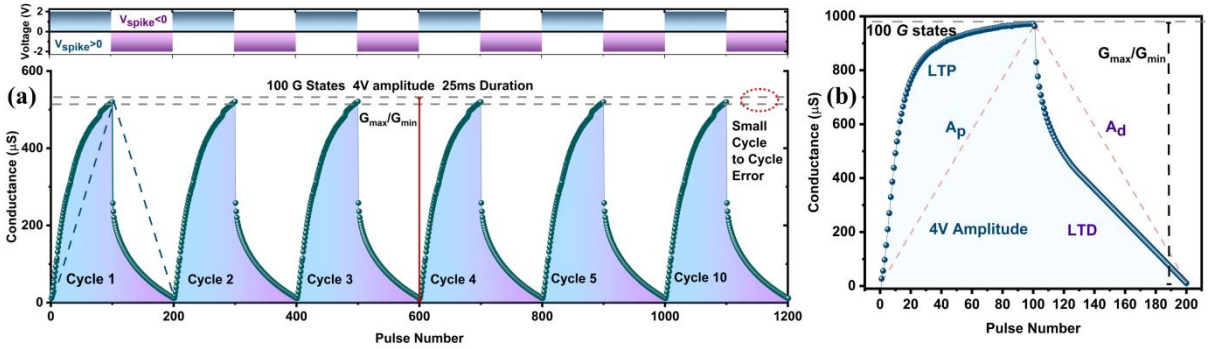

Figure 2.15 Stability testing of LTP/LTD (a) Increasing and decreasing of channel conductance illustrating the long-term potentiation and long-term depression (LTP/LTD) characteristics triggered by 100 positive (5V, 50 ms) and 100 negatives (-4 V, 50 ms) continuous spike signals. (b) Channel conductance modulation of weight update for 10 repeated 100 positive pulses (4 V Δt = 50 ms) and 100 negative pulses (-4 V Δt = 50 ms).

Through the analysis of several cycle-to-cycle curves of LTP/LTD, a cycle-to-cycle error was negligible after 10 cycles, showing the excellent robustness of the proposed EGTs device (**Figure 2.15a**). For weight updating process in neuromorphic computing, the parameters for emulating the learning process in ANN are extracted from long-term potentiation and long-term depression curves under the 100 positive pulses (5 V, width= 50 ms and Δt = 30 ms) and 100 negative pulses (-4 V, width = 50 ms and Δt = 30 ms). With alternate positive and negative voltage pulses, the synaptic EGTs have excellent LTP/LTD properties to contribute weights update in ANN, such as 100 level conductance states, G_{max}/G_{min} = 67, appropriate A_p (3.1), A_d (-2.7) (**Figure 2.15b**). The continuous combination under different conductance states (G) is defined as assessing the nonlinearity of potentiation and depression.

$$G_p = B\left(1 - e^{\left(-\frac{p}{A_p}\right)}\right) + G_{min} \tag{2.1}$$

$$G_d = -B\left(1 - e^{\left(\frac{p - P_{max}}{A_p}\right)}\right) + G_{min} \tag{2.2}$$

$$B = (G_{max} - G_{min})/\left(1 - e^{\left(\frac{-P_{max}}{A_{p,d}}\right)}\right) \tag{2.3}$$

G_p is the potentiation conductance, G_d is the depression conductance, P_{max} is the maximum number of pulses, and A is the parameter describing the potential and depression nonlinearity [35-39].

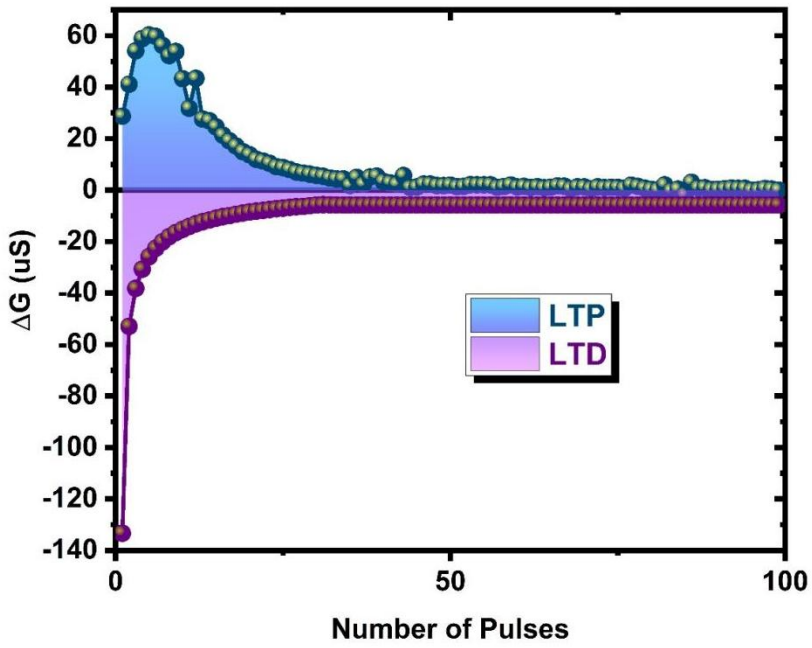

Figure 2.16 ΔG in the potentiation and depression process.

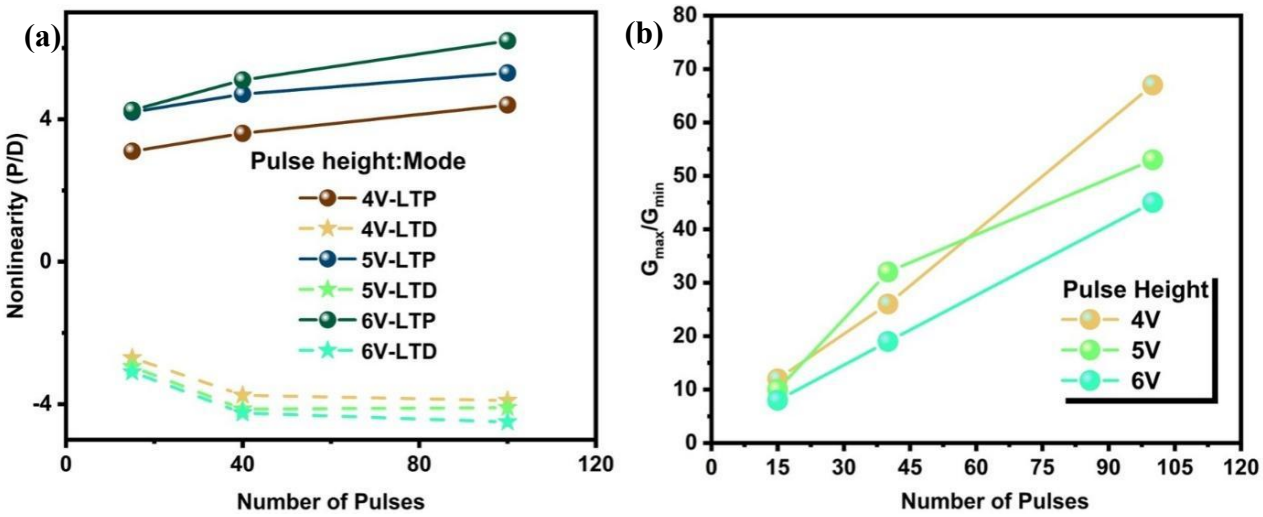

Figure 2.17 Update parameters under different LTP/LTD curves (a) The nonlinearity (NL) change characterized by the LTP/LTD curves with different voltage stimulation (4, 5, and 6 V). (b) G_{max}/G_{min} as functions of (15, 40, and 65) pulses at different pulse heights (4, 5, and 6 V).

Besides, two curves about ΔG in the potentiation and depression process, which relate to the number of pulses, are plotted **(Figure 2.16)**. The difference between every two neighboring

average conductance values is ΔG. The conductance (G) analysis aims to measure the Signal Noise Ratio (SNR) for synaptic transistors.

To match higher learning efficiency in the ANN algorithm, the changing trend of G_{max}/G_{min} and nonlinearity with the increase of pulse number under incremental voltage stimulations (4-6 V) are researched (**Figure 2.17**). The larger G_{max}/G_{min} creates the larger storage range for weight update (under 4 V spike stimulation).

Section 2.2.5 The bio-signal classification based on the synaptic transistor and ANN.

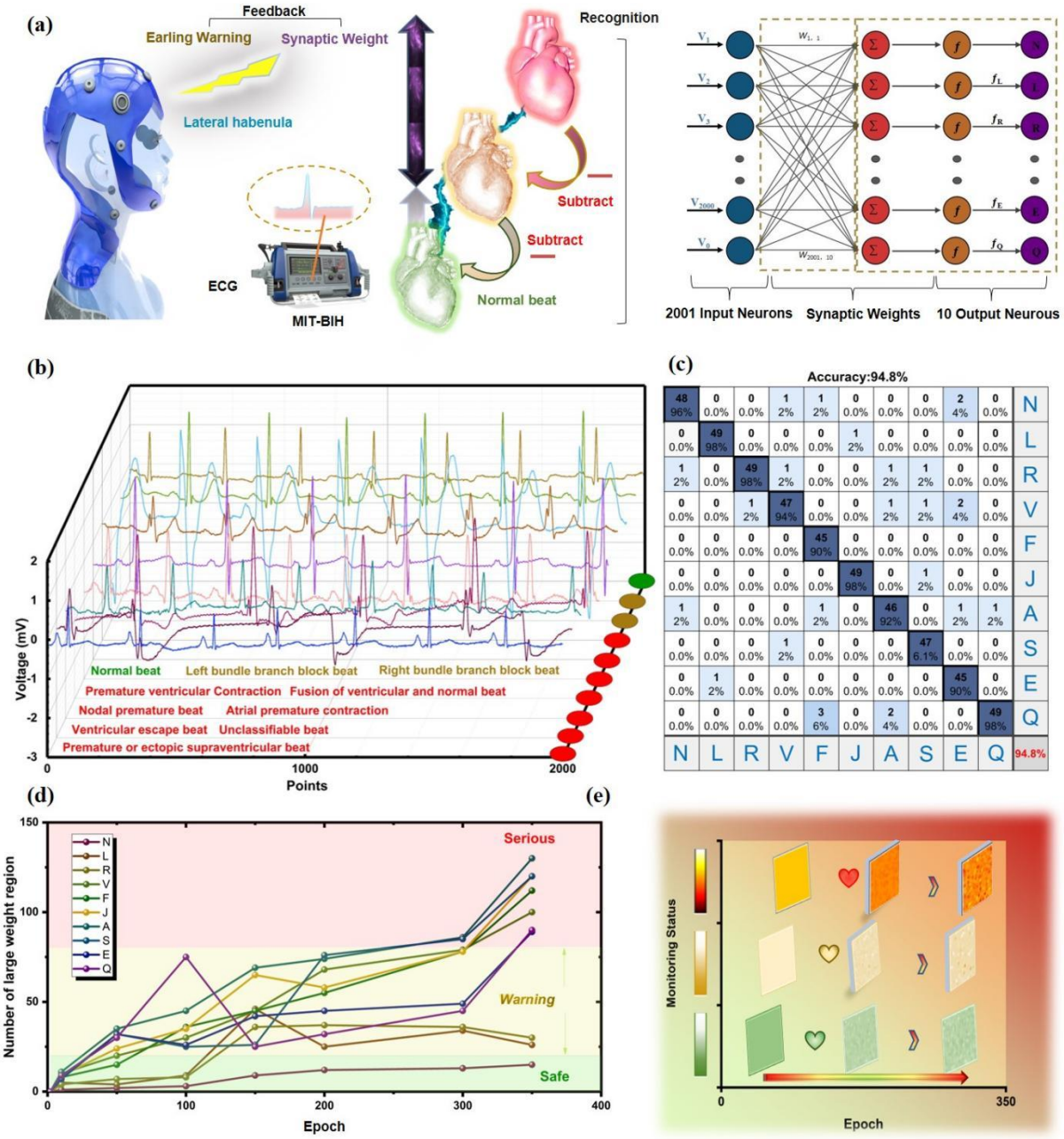

Figure 2.18 Recognition application of synaptic EGTs (a) Schematic diagram of cardiovascular abnormality monitoring and timely intervention system. (b) 10 ECG signals from the MIT-BIH database include one normal beat and 9 arrhythmia beats. (c) Confusion map of 10 heartbeat types labeled as N, L, R, V, F, J, A, S, E, Q. (d) Trend of the number of synaptic weight extreme regions in the three states (safe, warning, and serious) with the

stimulation time. (e) Synaptic weight map in three monitoring statues with the increase of training epochs.

To further investigate the efficiency and application of the ANN in the field of cardiovascular recognition, we utilized the simulator for training and recognizing ECG signals from the Massachusetts Institute of Technology-Beth Israel Hospital (MIT-BIH) database and extracted the synaptic weight with multi-level memory for the timely intervention of abnormal heartbeat (**Figure 2.18a**). One significance of ECG recognition is related to health care since the abnormal beating of the cardiovascular system cannot be consciously sensed by the brain nerve in time. Recent researches have proven that the specific parts of the brain (Lateral Habenula, LHb) could regulate the cardiovascular system [27-29]. Therefore, it is possible to intervene and stimulate the LHb to adjust the abnormal heartbeat when a serious heartbeat is recognized. This intervening also due to the number of extreme weight regions exceed a safe and warning threshold. Further, we simulate a single-layer-perception (SLP)-based ANN with the back-propagation algorithm and Manhattan update rules in MATLAB. The training datasets are collected from the MIT-BIH. The inputs of SLP-based ANN consist of 2001 presynaptic electrical signals, which include 1 bias signal and 2000 input signals. The 2000 input neurons based on time-domain signals of ECG, and 10 output neurons recognize 10 kinds of ECG. In the ANN simulator, the EGTs array is served as a weight unit of iterative operation and is updated due to the error gradient between the weighted sum and expected output. The 10 kinds of ECG signals from the MIT-BIH database include one normal beat and 9 arrhythmia beats, which could be labeled as N, L, R, V, F, J, A, S, E, Q (**Figure 2.18b**). According to the extent of the irregularity, these time-domain signals could be divided into three types (safe, warning, and serious) and converted to the input (within 2000 points) of the neural network. The confusion map shows that the 500 ECG matrixes are utilized for the testing section, and the recognition rate achieved 94.8% after 350 epochs (**Figure 2.18c**). The

more stable and equilibrium recognition rate illustrates that the ECG signal is more suitable for neural networks than MNIST. When the data cannot pass through the neural network at one time, it is necessary to divide the data set into several batches.

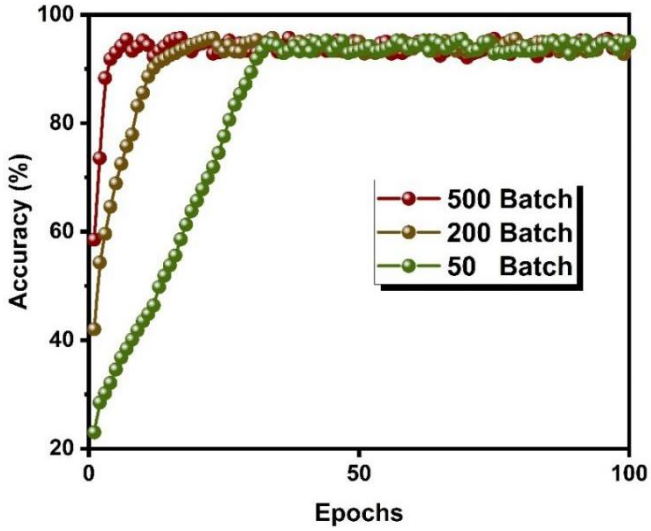

Figure 2.19. The recognition rate with different batch (500, 200 and 50 batch) for quick speed.

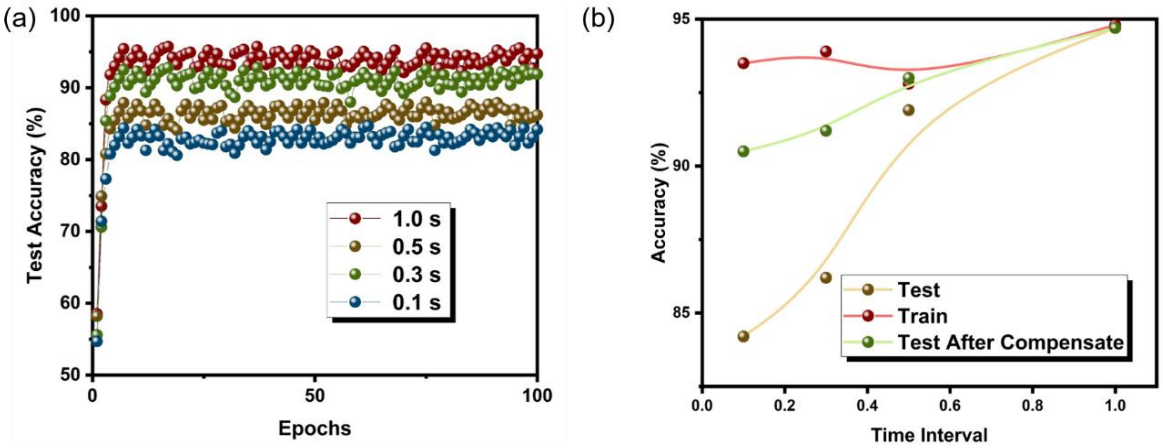

Figure 2.20. Accuracy of electrical signal (a) The recognition rate for different weightd updates time. (b) The comparison between the different situations (test, train and test after compensate) for recognition rates.

The **Figure 2.19** demonstrate the fast operation speed when the more batches (50, 200, 500) added in to the train process of ANN. Besides neural computing, the synaptic weight matrixes based on EGTs as a full connection for error back-propagation also have memory capacity. Moreover**,** The algorithm in ANN need a tradeoff between computing speed and accuracy

because One of the drawbacks of electrolyte gate transistor (memory) is conductance decay. To decrease the error caused by the large decay, we adjust update method in algorithm to compensate for the decay during the computing. We reconstruct a weight update rule with compensation measures in algorithm according to the recognition rate for different weigh updates frequency (0.1 s, 0.3 s, 0.5 s and 1.0 s) **(Figure 2.20**). When the computing speed is 0.1 s, the accuracy difference between the test and train process is the 9.5%.

The stored weight values of the matrix were extracted from the training process, showing that the more abnormal beats, the more extreme weight regions (**Figure 2.18d, e**). As the number of training epochs is increased to 350, the three areas of safe, warning, and serious were clearly separated. This clearly distinguished result indicates that the network can be designed for Computer-aided Diagnosis and timely intervention systems. This can be expected that in special risk situations without first aid measures, the health management system based on synaptic EGTs can stimulate LHb to enhance heart function when the extreme weight regions beyond the safe threshold.

Section 2.3 Conclusion

In the chapter 2, solid state electrolyte gate transistor with Li^+ ions doping has been proposed for neuromorphic computing. The Li^+ ions doping into AlO_x (dielectric layer) to enhance the synaptic long-term plasticity and charge storage ability. Purpose of Li^+ doping into the InO_x (semiconductor) layer for improving the stability apparently due to the cyclic update (cycle-to-cycle error). The doping concentration in the AlO_x and InO_x layers have been well discussed systematically. The typical synaptic behaviors, including IPSC/EPSC, LTP/LTD, STP, and PPF, have been successfully illuminated through the voltage spikes applied to the presynaptic terminal. It is worth noting that both the EPSC and IPSC are induced by the increase and decrease of channel conductance, respectively, which could be regarded as the change of synaptic weight. According to the G_{max}/G_{min} ratio and nonlinearity trend curves of LTP/LTD curve, the iterative update of synaptic weight matrix is demonstrated with the increase of epoch and the recognition accuracy of the bio-signal (ECG) can reach over the 94.8%. Moreover, the neural network can predict the abnormal beats of the cardiovascular due to extreme weight regions. We believe that this systematic research of Li^+ ion-doped solid state EGTs would pave the way for future neuromorphic computing networks.

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Chapter 3 Adjust the non-linearity and symmetry for matching improved neural network (Dynamic Residual Deep Learning with Photoelectrically Regulated Neurons for Immunological Classification)

Section 3.1 Experimental Section

Section 3.1.1 Synthesis and fabrication of 2D synaptic transistor

The ZrO_x precursor solution was obtained by dissolving 1.5M aluminum nitrate hydrate ($Zr(NO_3)_2 \cdot xH_2O$) in 20 mL 2-methoxy ethanol (2-Me). ZrO_x-Li precursor solution was obtained by mixing 1.5 M aluminum nitrate hydrate ($Zr(NO_3)_2 \cdot xH_2O$) and 0.15 M indium nitrate hydrate with 20 mL deionized water. The InO_x precursor solution was obtained by dissolving $In(NO_3)_3 \cdot xH_2O$ into 20 mL deionized water. All solutions were vigorously stirred under atmospheric conditions for 5 hours and filtered before spin coating using 0.25 μm polytetrafluoroethylene (PTFE) syringe filters, respectively.To prepare MXenes, first, 2 grams of lithium fluoride (LiF) with 99.99% metals basis from Aladdin and 40 mL of hydrochloric acid (HCl) with a concentration of 36.0-38.0% from Sinopharm Chemical Reagent Co., Ltd. were mixed and stirred in a polytetrafluoroethylene (PTFE) beaker for 30 minutes. Next, 2 grams of titanium aluminium carbide MAX (MAX-Ti_3AlC_2) with a purity of 98% from 11 technology Co., Ltd. was gradually added to the beaker under continuous stirring, and the reaction temperature was maintained at 35°C for 24 hours in a fume hood. After the reaction was completed, the resulting solution was centrifuged for 10 minutes at 3500 rpm, and the supernatant was discarded. Then, 40 mL of deionized water (DI) was added to the sediment in the centrifuge tubes, and the tubes were manually shaken to mix the sediment with DI water. The mixture was further ultrasonicated for 15 minutes using a high-power ultrasonic machine with 750 W output. These centrifugation and ultrasonication steps were repeated until the pH

of the supernatant reached 5. Subsequently, 40 mL of ethanol (CH_3CH_2OH) with a purity of 99.7% from Sinopharm Chemical Reagent Co., Ltd. was added to the centrifuge tubes, and the mixture was ultrasonicated for 1.5 hours using an intercalator function. Then, the mixture was centrifuged at 10,000 rpm for 10 minutes, and 20 mL of DI water was added to the sediment. The mixture was further ultrasonicated for 20 minutes and then centrifuged again at 3500 rpm for 3 minutes to obtain a black-brown few-layer dispersion with a concentration of approximately 5 mg mL^{-1}. Finally, the MXenes dispersion was stored in an argon atmosphere and the storage time was limited to 14 days.

First, a heavily doped Si (n^{++}) substrate was cleaned by deionized water and dried under N_2 flow. Afterward, the processed substrate was further treated by Plasma for 15 minutes to allow the film surface hydrophilic treatment. The ZrO_x and ZrO_x-Li films were spin-cast with precursor solution at 4500 rpm for 30 s and then annealed for 80 mins at 250°C in the air atmosphere.Then, the MXenes solution was then diluted to 1 mg/mL and spin-coated at 3000 rpm for 20 s on the surfaces of ZrO_x and ZrO_x-Li films. Substrates with solution film were then oxidized at 80°C for 1 min on a hotplate in air condition. The InO_x film was spin-cast with precursor solution at 3500 rpm for 30 s and then annealed for 1h at 200°C for the in the air atmosphere. The 30 nm thick Al S/D electrodes were fabricated by thermal evaporation through the shadow mask.

Section 3.1.2 ELISA Detection

Rabbit IgG is the most common model sensing target in c-ELISA assays, and a schematic of the direct c-ELISA protocol for Rabbit IgG on our multi-well uPAD is shown in Figure 1b. Typically, direct c-ELISA is carried out in six steps: (1) biofunctionalization of the test zone using periodate potassium, (2) immobilization of the rabbit IgG antigen on test zone, (3) blocking the test zone to prevent non-specific adsorption of rabbit IgG proteins, (4) labeling the immobilized rabbit IgG antigen with ALP-conjugated anti-rabbit IgG antibody, (5)

washing away the unbound antibody using PBS buffer, (6) adding the BCIP/NBT substrate [1-8].

Section 3.1.3 Characterization

A semiconductor parameter analyzer (Agilent B1500) with transistor characterization software under atmospheric conditions was operated to test the electrical properties of the Al/InO_x/MXenes/ZrO_x-Li/Si/Al synaptic transistor. In order to measure the EPSC and LTD/LTP current flowing between the S/D electrodes, the 0.1 V steady voltage bias was applied to the postsynaptic terminal (V_{post}) [9-13]. The chemical compositions of dielectric and semiconductor layers were measured by XPS. The crystallization and structural information of the thin films were displayed using XRD- BRUKER D8 ADVANCE with Cu Kα radiation (λ = 1.542 Å).

Section 3.1.4 ResNet simulation

We use a Resnet as the base model, which is a compact and efficient neural network. After we convert the image data into RGB three-channel matrix data, we could directly pass it into the residual block. The residual block is the main component of Resnet. Compared with the ordinary neural network structure, the residual block could not only perform weighted operations through the convolution layer and activation function mechanism to extract features, and also retain the initial information of the input data and fuse it with the obtained feature information. Two residual blocks and one linear layer are used in our model. The input image data is passed through two residual blocks to complete the feature extraction, and then passed to the linear layer to complete the final classification task [10-15]. Usually, this is a complete ResNet workflow, and we use a dynamic learning rate in the training step. After each training of the network, different learning steps are used to update the network parameters according to the change direction of the loss.

The calculated conductance of synaptic transistors in the crossbar array was applied with the positive synaptic weight value. The measurement of the neurocomputing in ResNet includes negative values. Subsequently, the synaptic weight ($W = G^+ – G^-$) was expressed as the difference between the state of two synaptic devices (expressed as G^+ and G^-) between each conductance value. The initial weights were set up random fluctuation near 0 and the value between G_{min} and G_{max} normalized to (-1,1). Actual changed value of weight updating depends on the difference between the conductance state of two synaptic devices (G^+ and G^-) which extracted from the LTP/LTD curve [13-18]. The synaptic weight defined as the difference of conductance in two synaptic transistors which represent single neuron. When $sgn(\Delta W) > 0$, the formula $W \uparrow = G^+ \uparrow - G^- \downarrow$ will be used. And when $sgn(\Delta W) < 0$, the $W \downarrow = G^+ \downarrow - G^- \uparrow$ will be used.

In order to make the model converge earlier, we use two functions to adjust the learning rate dynamically. After each round of training, we conducted a round of tests to test the model's performance. If the classification error of the current round is smaller than that of the previous round, we use the function [e* (e+1)] ^(1/2) to appropriately increase the learning rate, where e is the number of training rounds to adjust the value of the learning rate. If the classification error of the current round is more significant than that of the previous round, we use the function e/(e+1) to reduce the learning rate appropriately.

Section 3.2 Results and Discussion

Section 3.2.1 The structure and mechanism of synaptic device

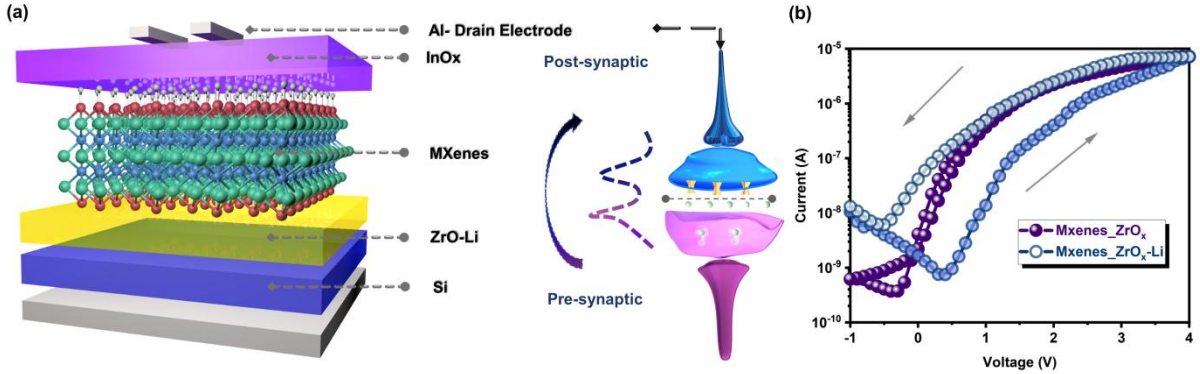

Figure 3.1 2-D synaptic transistor (a) Schematics illustrate the biological synapse and the Al/InO_x/MXenes/ZrO_x-Li/Si/Al synaptic transistor. (b) Transfer characteristics of with and without Li^+ ion doping transistors.

To achieve the application of computer aided detection in immunology of the concentration of immune protein, the Al/InO_x/MXenes/ZrO_x-Li/Si/Al structure is designed to achieve synaptic plasticity by simulating the internal linkage between the learning speed and visual receptors through the virtual neuron light-operated and electric pulse controlled **(Figure 3.1a**). In comparison to the bionic neural network created using the von Neumann architecture and CMOS process currently available, synaptic devices offer more efficient parallel processing speeds and lower energy consumption when dealing with complex tasks. The two-dimensional material depends on the short ion transport distance, excellent electron transport dynamics, and photoelectric response to compose the part of synaptic transistors [19-21]. Compared with the organic materials and metal oxide materials as the partial structure of synaptic transistors, the 2Dimensional materials have the advantage of simple technology, high product yield, fast electronic transmission speed, and stability in environmental change. The clear layered structure is observed by SEM (**Figure 3.2**).The X-ray diffraction spectrum for $Ti_3C_2T_x$ MXenes presents a small peak of 6.4° typical of MXenes (**Figure 3.3**)

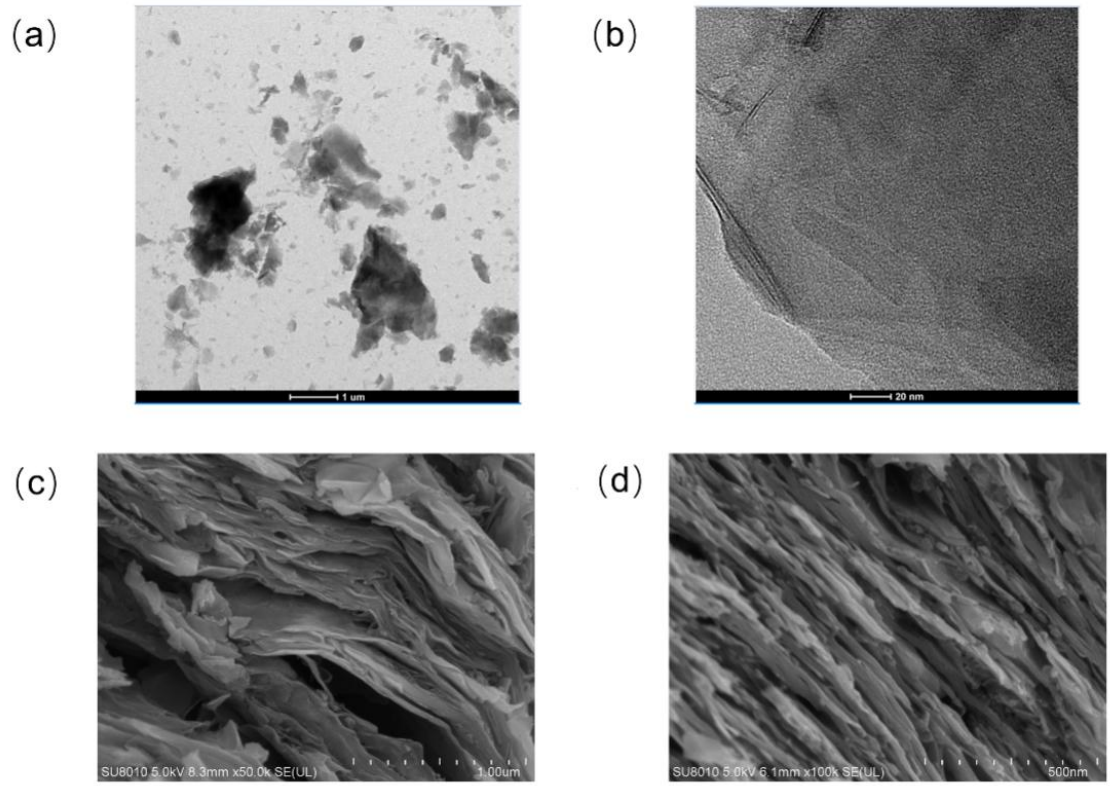

Figure 3.2 Layered structure of MXenes (a) The SEM of MXenes with 1 μm from vertical view. (b) The SEM of MXenes with 20 nm from vertical view. (c) The SEM of MXenes with 1 μm from section view. (d) The SEM of MXenes with 500 nm from section view.

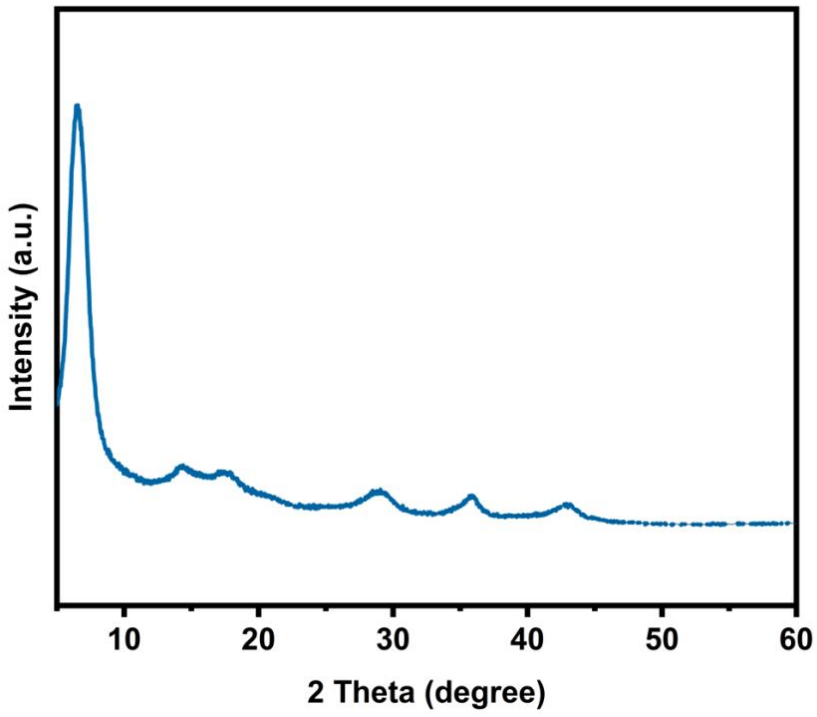

Figure 3.3 The X-ray diffraction spectrum for $Ti_3C_2T_x$ MXenes.

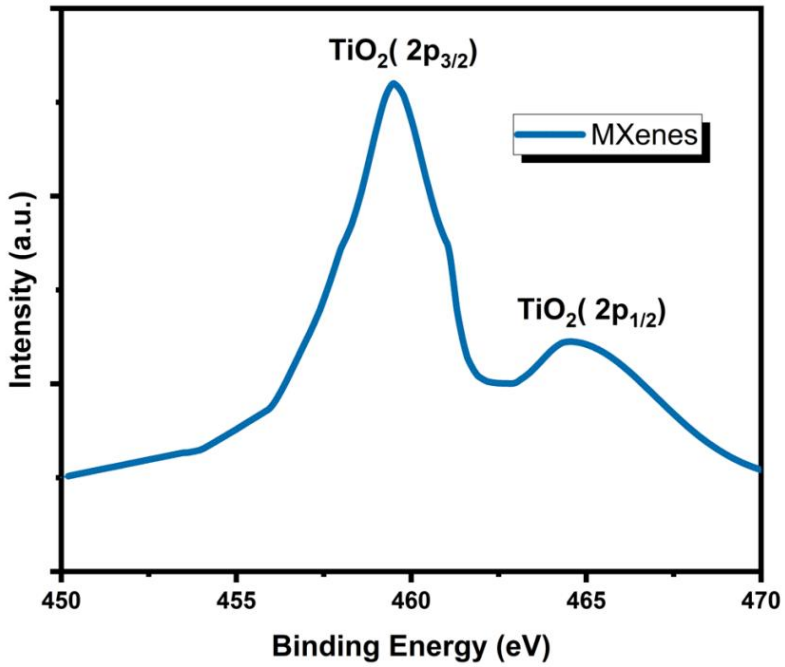

Figure 3.4 The Ti 2p X-ray photoelectron spectroscopy spectra of MXene.

The Ti 2p X-ray photoelectron spectroscopy spectra of MXene demonstrate the apparent peaks of TiO_2 ($2p_{3/2}$) and TiO_2 ($2p_{1/2}$) due to the oxidation during the InO_x fabrication process (**Figure 3.4**).

In the previous studies, optoelectronic synaptic transistors have the advantages of large bandwidth, low energy consumption, and ultrafast signal transmission for artificial neural networks and retina. In the weight update process that has been widely employed in previous works, neural computing adopts one of the LTP/LTD curves from light stimulated or electrically stimulated nonvolatile. To tackle the limitations of the nonlinearity extracted from conductance and the single update rule adopted, the double dynamic update rule is developed according to the conductance change when the preterminal is stimulated by electric pulse and mixed pulse. The schematic diagram of synaptic transistor and synapse demonstrates that the gate electrode as the pre-synaptic terminal and the drain electrode as the post-synaptic terminal. The transmission of information in the synapse is that the chemical signals are converted into electrical signals when the synaptic vesicles release neurotransmitters [22-25]. To verify the synaptic plasticity, the transfer characteristics curves with Li^+ doped into the

ZrO_x layer (5% doping concentration) demonstrate the large hysteresis of typical synaptic characteristics (**Figure 3.1b**). And this phenomenon benefits achieving multilevel storage. Furthermore, the transfer characteristics of an undoped transistor have no evident hysteresis clarifying that Li^+ ion migration changes the channel conductance [18-20]. To briefly expound the transformation from STP to LTP and the dynamic update decision, the schematic diagram shows the mechanism when electric pulse and optical pulse are applied to the gate and channel, respectively. When a positive voltage is applied to the pre-synaptic terminal, Li^+ ions with a large diffusion coefficient and small atomic radius will migrate from the ZrO_x layer to the MXenes and semiconductor layer with the increase of voltage amplitude [21-24]. For applying the optical pulse at the channel (photon radiation: $V_O + h\nu \rightarrow V_O^{2+} + 2e^-$), the oxygen vacancies in the metal oxide network generate the electron-hole pairs (**Figure 3.5**). The competitive advantage of this work is the update interval and the symmetry of long-term potentiation and long-term depression.

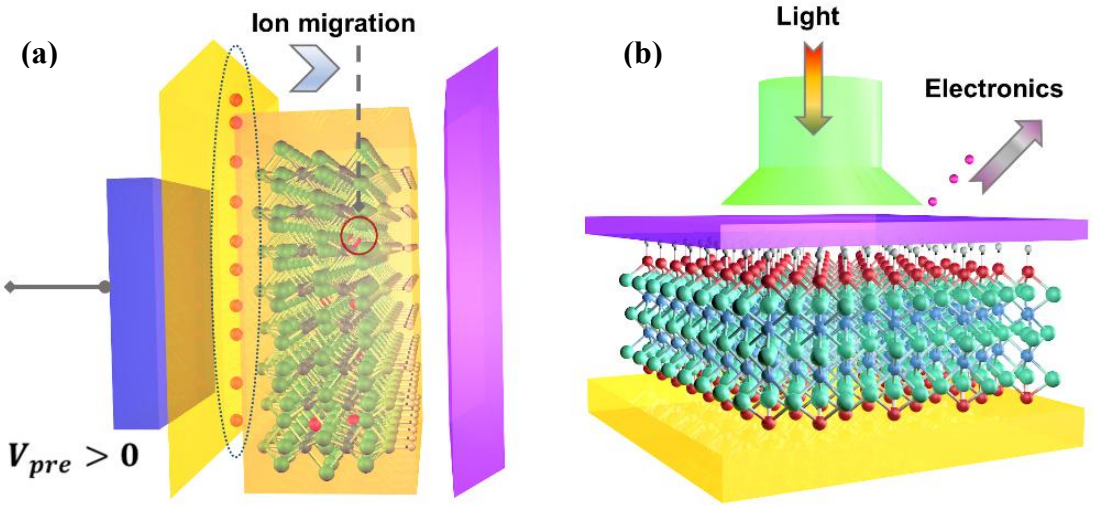

Figure 3.5 Basic mechanism of neural devices (a) Schematic diagram of mechanism for Li^+ ion migration under the stimulation of electric pulse. (b) Schematic diagram of mechanism for photon radiation under the stimulation of optical pulse.

Section 3.2.2 The synaptic plasticity of Mxenes synaptic transistor

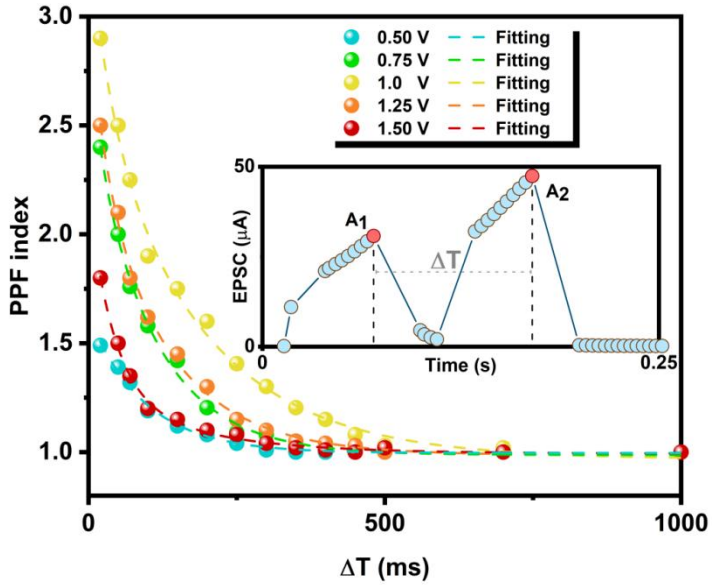

Figure 3.6 PPF index versus interval time Δt under various voltage amplitude (0.50 V, 0.75 V, 1.0 V, 1.25 V, and 1.50 V). Inset: definitions of A_2 and A_1 with two successional 50 ms pulses.

To verify the synaptic plasticity of the transistor, the nonvolatile conductance is recorded when optical and electrical pulses are applied to the channel and pre-synaptic terminal, respectively [20-27]. PPF preliminarily shows the short-term synaptic plasticity, which is the basic function of biological synapse for processing temporal information (**Figure 3.6**). The interval (Δt) between pulses from 20 ms to 1000 ms and the amplitude of electric pulses from 0.5 V to 1.5 V with each increase of 0.25 V.

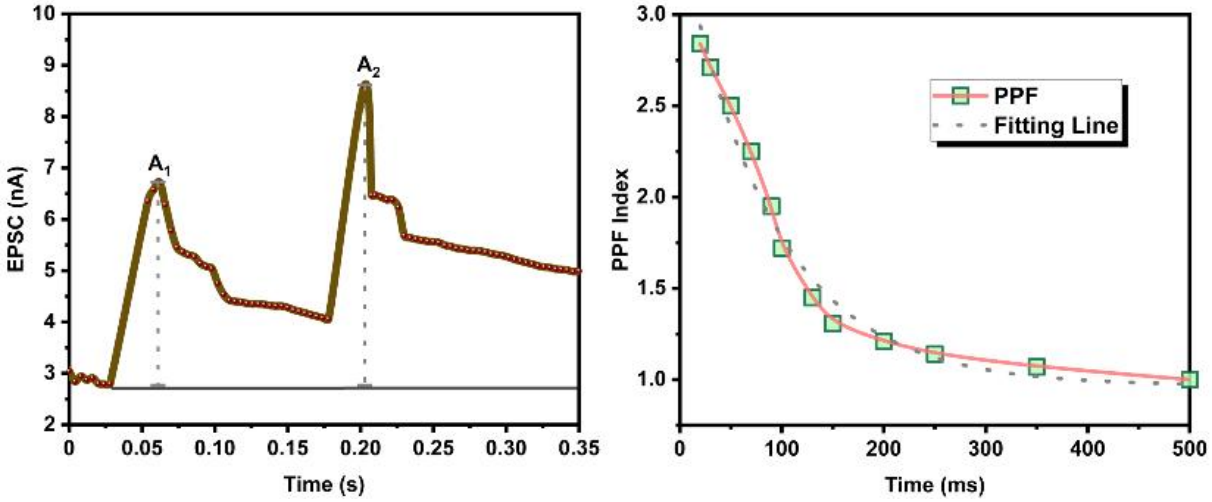

Figure 3.7 The PPF index versus interval time Δt with two successional optical pulses.

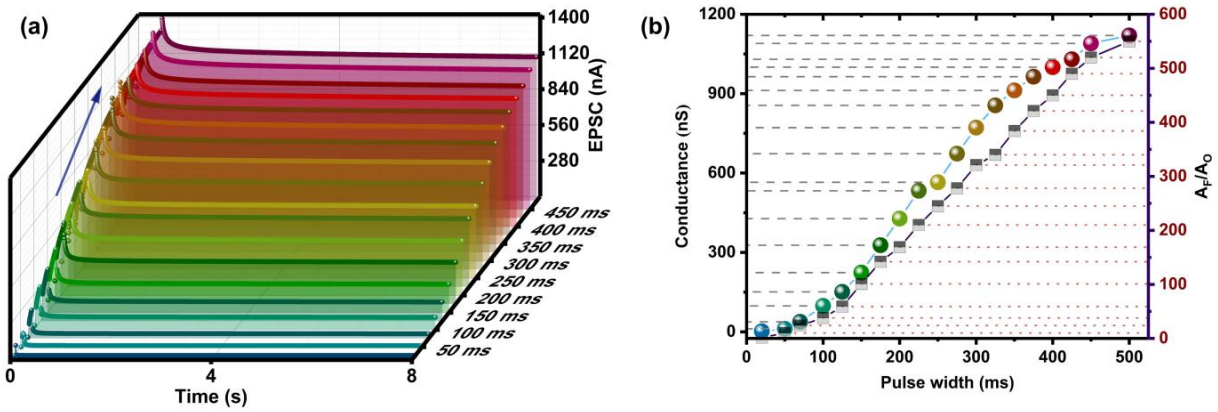

Figure 3.8 Linearly increasing synaptic plasticity (a) EPSC triggered by 19 single pulses with different durations (20, 50, 75, 100, 125, 150, 175, 200, 225, 250, 275, 300, 325, 350, 375, 400, 425, 450, 475, and 500 ms) at V_{DS} = 0.5 V. (b) Extracted stable conductance for various pulses width and the ratio of stimulated conductance over initial conductance (A_F/A_O).

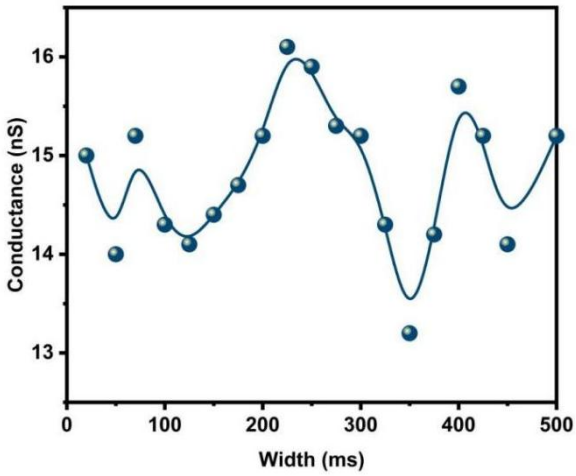

Figure 3.9 The initial conductance level to determine the retention of the memory.

The expression of the PPF index depends on the ratio of the first and second peak value (A_2/A_1) of EPSC [22-28]. The PPF fitting curves include the initial constants of rapid (C_0, C_1, and C_2) and the relaxation times ($\tau 1$ and $\tau 2$) that describe the convergence rate and downward trend. The highest PPF index of Δt =20 ms is attained by the appropriate voltage stimulation (1 V), and the parameters of the fitting curve about C_0=1, C_1=35%, C_2=48%, τ_1=35 ms, and τ_2=35 ms. Similarly, the PPF index curve (C_0=1, C_1=28%, C_2=36%, τ_1=22 ms, and τ_2=56 ms) stimulated by blue light also shows the synaptic plasticity when the photoelectric effect occurs in the channel (**Figure 3.7**). Further, the conversion from short-term to long-term synaptic

plasticity is obtained by increasing the electric pulse width to 500 ms (**Figure 3.8a**). The 19 initial conductance values increased from the 14.9 nA (**Figure 3.9**). The phenomenon is attributed to the Li^+ ion migration in the ZrO_x and MXene layers, leading to multiple conductance states [26-30]. With the width increasing linearly, the changing trend of 19 levels tends to be linear, proving the conductance is precisely programmed by electrical pulse width (**Figure 3.8b**).

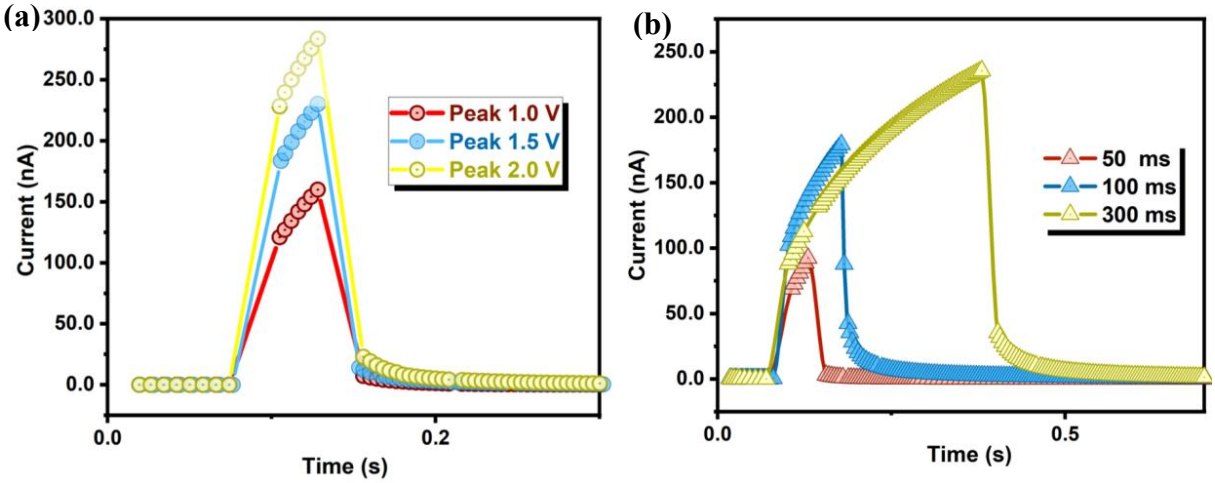

Figure 3.10 Synaptic plasticity of synaptic transistor without Li doping (a) Common: the EPSC triggered by the same width time (40 ms) pulses with three pulse amplitudes (1.0, 1.5, and 2.0 V) at V_{DS} = 1 V without Li ion doped. (b) The EPSC triggered by positive pulses (1 V) with three pulse durations (50, 100, and 300 ms) at V_{DS}=1 V without Li ion doped.

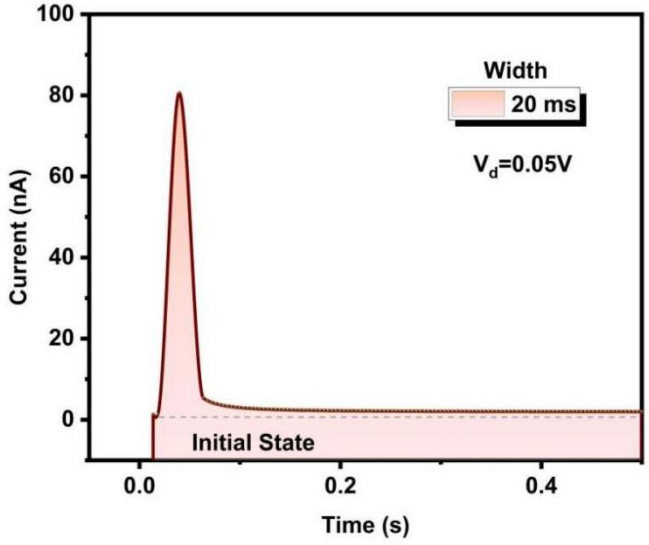

Figure 3.11 EPSC property triggered by presynaptic spike (V_{gs}=1.5 V, V_{ds}=0.1 V, Pulse Width=20 ms) in 0.5 s.

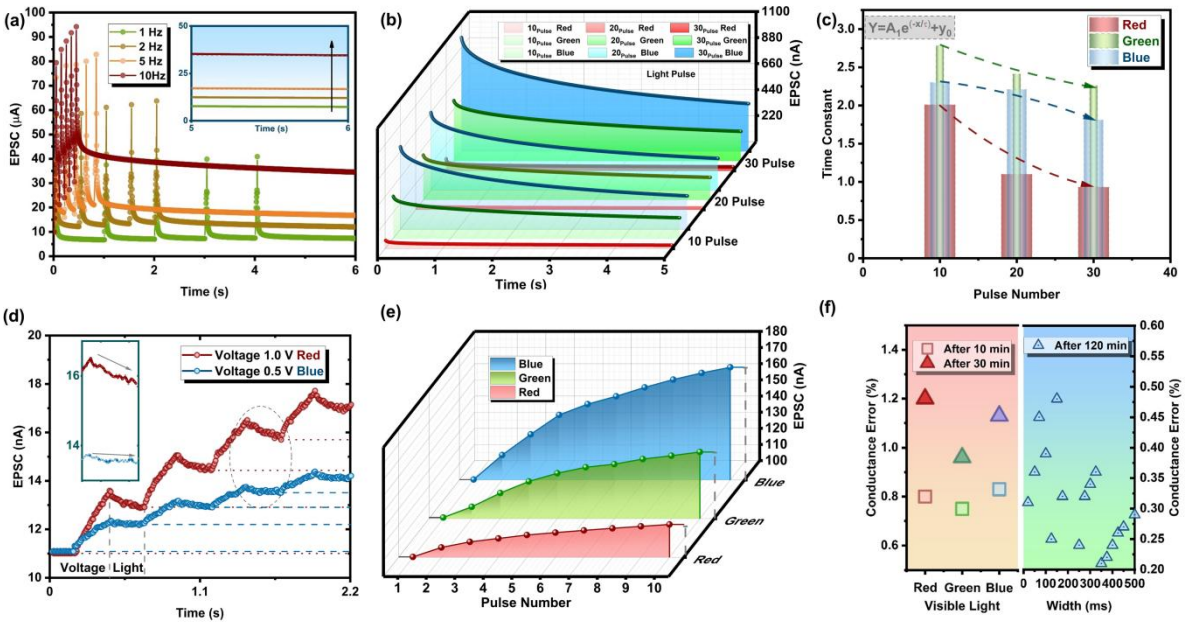

Figure 3.12 Synaptic plasticity under electrical and light stimulation (a) EPSC stimulated by five continuous electric pulses (1 V, 40 ms) with different frequencies (1, 2, 5, and 10 Hz). (b) Relaxation process of EPSC stimulated by the different number of red, green, and blue pulses (10, 20, and 30). (c) Time constant extracted from the natural forgetting process. (d) EPSC triggered by two mixed pulses (0.5 V + blue and 1.0 V + red), which means the electric pulse combined with the optical pulse. (e) Long-term potentiation stimulated by ten groups of combined pulses that red, green, and blue optical pulses involved, respectively. (f) Conductance errors of 30 minutes and 300 minutes later under electric and combined pulses modulated.

The (ZrO_x/Mxenes) without Li doping has no STP-LTP response. This phenomenon further proves that Li^+ ion plays an irreplaceable role in channel conductance update for neuromorphic computing, and the common ZrO_x gate dielectrics are not adequate for a large retention range (**Figure 3.10**). Further, to verify the low energy consumption of synaptic device, the energy consumption per spike of TFTs is calculated by the Equation $E= I_{peak} \times t \times V$ =80.19 pJ (**Figure 3.11**). I_{peak} is the maximum value (80.19 nA) of generated EPSC curve, t is the spike duration (20 ms), and V is the voltage applied to the drain electrode (0.05 V). Similarly, pulse frequency (1, 2, 5, and 10 Hz) also affects the conductance observed from the

EPSC curves. Five consecutive pulses stimulated these curves with the same parameters (1 V and 40 ms) except frequency (**Figure 3.12a**). The inset figure can analyze the obvious multi-conductance and stable nonvolatile within 6 s. On the other hand, to research the optically controlled synaptic plasticity, three wavelengths of light (red, green, and blue) are applied to the InO_x and MXene layers [29-33]. Compared with electrical plasticity, the photocurrent can also be accumulated through the superposition of the number of pulses. The main photoelectric response of MXene under the light with three wavelengths (Red=680 nm, Green=540 nm, and Blue=490 nm) causes a long relaxation time (**Figure 3.12b**). Light with a small wavelength carries strong photon energy, which excites a high photocurrent. Analysis of the relaxation process based on the time constant ($\tau_{10} = 1.91,\ \tau_{20} = 1.08,\ \tau_{30} = 1.08$) illustrates that the fastest decay rate. belongs to red light (**Figure 3.12c**). This phenomenon provides potential feasibility for combined pulse stimulation, which means optical pulse and electric pulse are used alternately during conductance updates [34-38]. According to the previous research, one of the drawbacks of the synaptic transistor (memory) is conductance decay. It is always a trade-off between computing speed and accuracy. In short, if the computing speed is fast, the extensive decay will significantly increase the error. The combined pulses are adopted to shorten the decay process and maintain the conductance state to solve this bottleneck. The first step is to apply an electrical pulse (0.5 V) to the pre-synaptic terminal, and then an optical pulse (blue) is applied to the channel (**Figure 3.12d**). Maintaining the peak conductance value can be observed from the EPSC trend compared with the red pulse. The benefit is to accelerate the conductance update speed greatly [38-40]. Afterward, the same pulse combination rule is extended to red, green, and blue pulses, with the electric pulse amplitude being 0.5 V (**Figure 3.12e**). After ten cycles of combined pulses, the conductance values of three conditions for adding red, green, and blue pulses are 11.5 ns, 13.2 ns, and 16.3 ns, respectively. In addition, as a synaptic device for neuromorphic

computing, nonvolatile conductance is also a necessary factor. To demonstrate all aspects of stability, the conductance errors are counted in three states (10 minutes later, 30 minutes later, and 120 minutes later) after stimulation by ten combined pulses (**Figure 3.12f**). The error range for combined pulses is floating between 0.7 and 1.2, satisfying the storage and computing requirements for the neural network. Similarly, the conductance controlled by the gate can hold relatively stable after 10, 30, and 120 minutes as a result of a 0.25%-0.60% error range. To demonstrate the high level of stability, the variances between the initial conductance and the conductance maintained after 300 and 600 minutes are compared, and the results indicate that the majority of errors are below 0.5% (**Figure 3.13**).

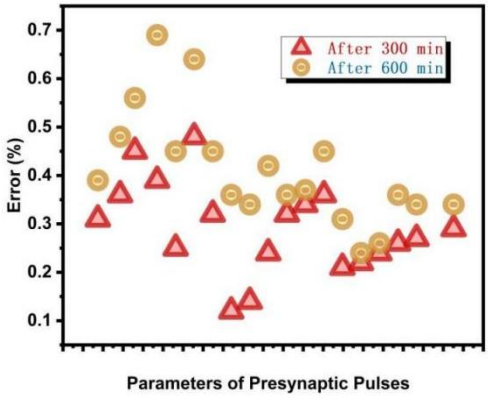

Figure 3.13 The 300 minutes and 600 minutes error after the presynaptic electric pulse stimulation.

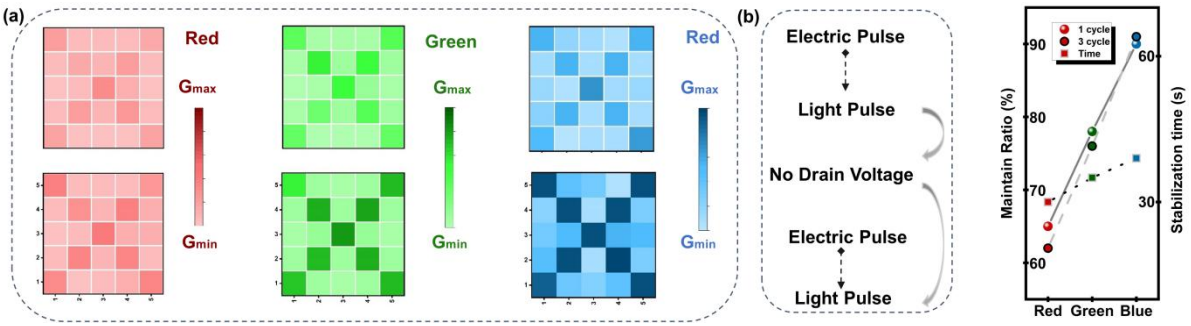

Figure 3.14 Arrayed memory and erasure (a) Three 5×5 matrices for demonstrating the change of conductance of the cycle of 1 and 3 combined pulses. (b) Maintain ratio and stabilization time for 1 and 3 cycles.

Above all show, the Al/InO_x/MXenes/ZrO_x-Li/Si/Al synaptic transistor has a variety of stable modulation modes. To further verify the feasibility of large-scale integration, the combined

pulse update rule applied in a single device is extended to the 5×5 matrix (**Figure 3.14a**). The electric pulse amplitude in all combined pulses is 0.5 V, and the pulse width is 50 ms. When combined pulses are electric pulse and blue light, the ratio of peak value over stable value attains 91% showing that the relaxation time is shorter (**Figure 3.14b**). The short relaxation time enormously curtails the interval between each weight update for the neural network. Every two 5×5 matrices demonstrate the conductance distribution in two states (after one cycle and three cycles), and one cycle represents the complete stimulus of combined pulses. In addition, the conductance value after receiving circulatory stimulation can still maintain 99% of the stable value within 30 s. Therefore, the above results provide novel and efficient rules for simulating the weight updating process in the neural network [41-44].

Section 3.2.3 Adjust the long-term potentiation and long-term depression (nonlinearity and symmetry)

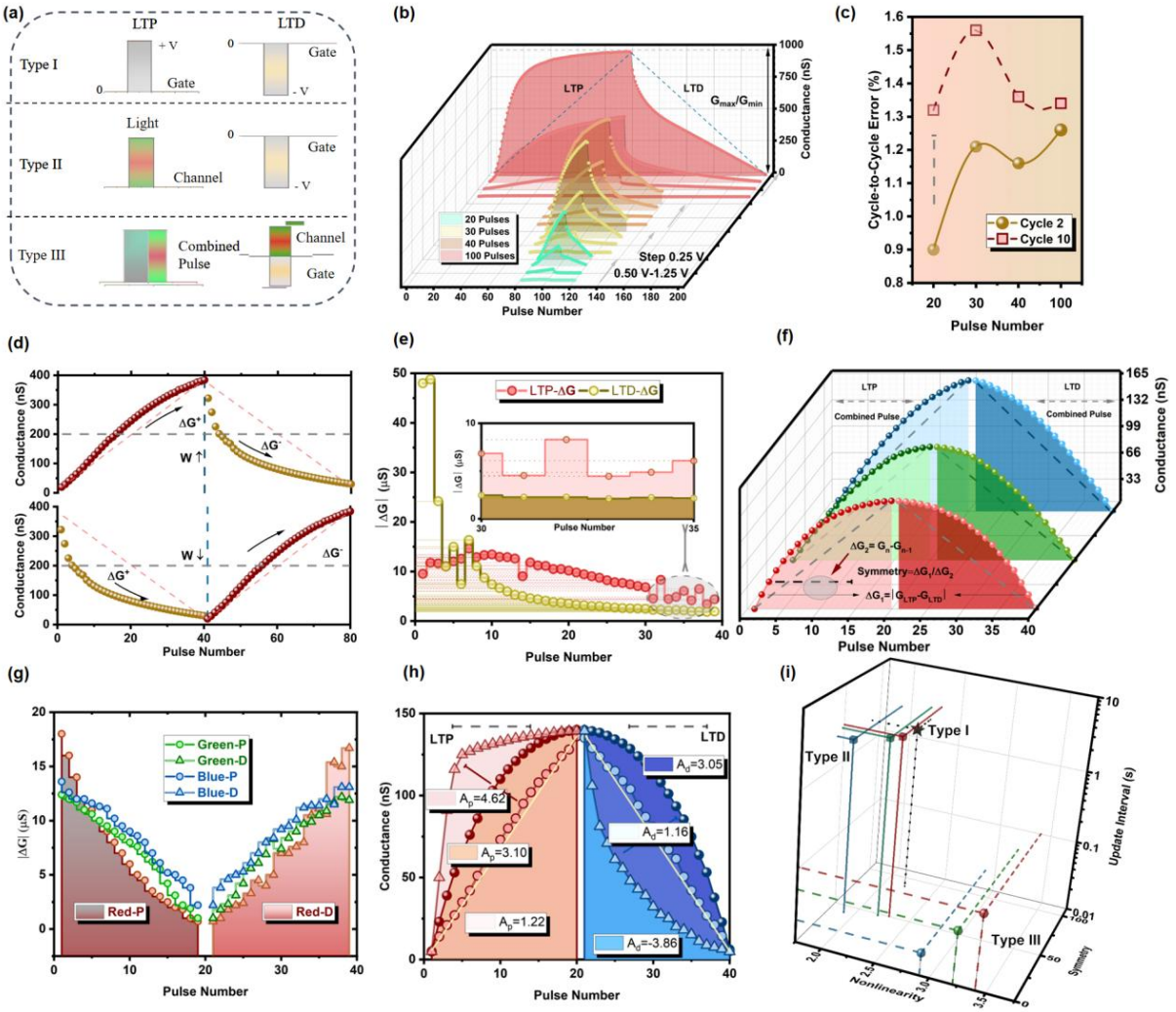

Figure 3.15 Three testing schemes and results (a) Illustration of three types (Type I, Type II, and Type III) are positive pulse/negative pulse, optical pulse/negative pulse, and combined pulse/combined pulse. (b) LTP/LTD curves for various electric pulse numbers under the incremental pulse amplitude from 0.50 V to 1.25 V. (c) Conductance error of cycle-to-cycle for different pulse numbers. (d) Synaptic weight update rule of two synaptic transistors (G^+ and G^-) for the above three types. (e) Change trend of ΔG in LTP and LTD stages under electrical stimulation. (f) Type III: the LTD/LTD stimulated by combined pulses. (g) Change trend of ΔG in LTP/LTD stages of Type III. (h) Combined pulse stimulation can regulate the

nonlinearity and symmetry of LTP/LTD. (i) Nonlinearity, symmetry, and update intervals for the Type I, Type II, and Type III.

Replacing the weight matrix in a neural network with a synaptic device matrix is indispensable for developing neural morphological electronics [40-45]. The update rules of the simulated weight matrix according to the periodic trend of LTP/LTD in the synaptic transistor. The mode of pulses applied for three types (Type I, Type II, and Type III) are positive pulse/negative pulse, optical pulse/negative pulse, and combined pulse/combined pulse, respectively (**Figure 3.15a**). The parameters extracted by LTP/LTD curves and applied to the neural calculation are G_{max}/G_{min}, nonlinearity, cycle-to-cycle error, and symmetry. Then, the modification of G_{max}/G_{min} and nonlinearity by electric pulse amplitude and pulse number in Type I is researched. When the number of pulses is 100, the number of conductance updates increases, resulting in a larger ratio of G_{max}/G_{min}. Further, when the voltage amplitude increases from 0.5 V to 1.25 V in a step of 0.25 V, the number of pulses required becomes small and makes the conductance reach relative saturation, resulting in the curve fitting into a convex function gradually (**Figure 3.15b**). The range and resolution of the weight update depend on the G_{max}/G_{min}, the learning step of each epoch depends on the nonlinearity, symmetry, and the stability of training and testing depends on the error of cycle-to-cycle [46-48]. Above, all factors together affect the final classification accuracy. The cyclic stability of LTP/LTD is verified by alternately applying the positive (0.5 V, 40 ms) and negative (-0.5 V, 40 ms) electric pulses to the pre-synaptic terminal. With the increase in the number of pulses (20, 30, 40, and 100), the error of cycle-to-cycle rise to 1.31%, 1.56%, 1.36%, and 1.33% after ten cycles, respectively **(Figure 3.15c**). The errors floating within a specific limit show the robust stability of LTP/LTD that benefits the training and test process. During the update process, three update modes are proposed to demonstrate the influence of electric pulse and optical pulse on parameters extracted from the LTP/LTD curve [49-50]. Then, the

modification of G_{max}/G_{min} and nonlinearity by electric pulse amplitude and pulse number in Type I is researched. When the number of pulses is 100, the number of conductance updates increases, resulting in a larger ratio of G_{max}/G_{min}. Moreover, the conductance difference (ΔG) between the two synaptic transistors (G^+ and G^-) is used to represent the weight range (-1 to 1) in the algorithm (**Figure 3.15d**). Notably, the left and right parts of the curve need to match the symmetry because the rising and decline stages of conductance should have one-to-one correspondence [50-53]. To explore the regulation of optical pulse on nonlinearity and symmetry, type II and type III are developed. The curvature of the fitting curve determines the sign and magnitude of the nonlinearity. The nonlinearity and ΔG affect the learning step of each training, which is also called the learning rate (**Figure 3.15e)** [51-55]. The convex function (positive nonlinearity) causes the dynamic change of learning step to weaken gradually. On the contrary, the concave function (negative nonlinearity) gradually enhances the learning step size. However, in the standard case, the learning step of the primary function (nonlinearity=1) is a fixed value.

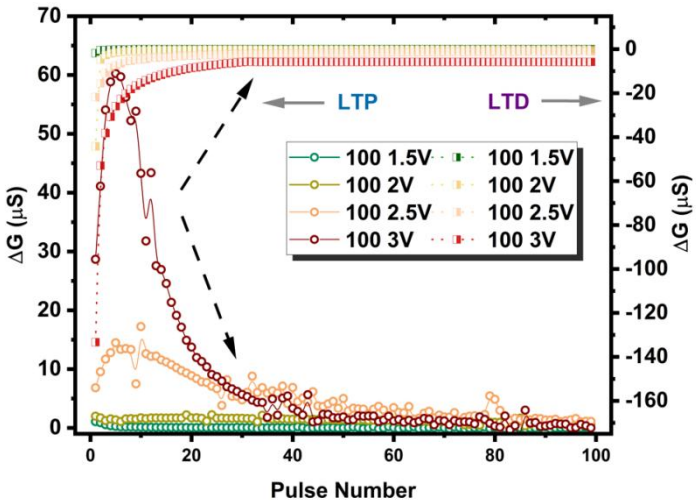

Figure 3.16 ΔG in the 100 potentiation and 100 depression stages for under various voltage stimulation.

Besides, the ΔG in the potentiation and depression process is analyzed to measure the SNR and learning step size for synaptic transistors (**Figure 3.16**).

To explore the regulation of optical pulse on nonlinearity and symmetry, type II and type III are developed. As depicted in **Figure 3.15f**, the 20 optical pulses (red, green, and blue) are adopted in the potentiation stage, and the 20 negative electric pulses (-0.5 V) are adopted in the depression stage. Compared with Type I, the symmetry defined as the ratio of $\Delta G_1/\Delta G_2$ is greatly improved in Type II. ΔG_1 is the difference between the potentiation and depression stages (G^n_{LTP} and G^n_{LTD}) at the same level, and ΔG_2 is the difference between the two adjacent levels (G_n and G_{n-1}) of conductance. Furthermore, Type III fundamentally solves the problem of insufficient symmetry based on the advantage of shortening the relaxation time.[44] Therefore, three Type III composed of three optical pulses (red, green, and blue) and the same electrical pulse (0.5 V for LTP and -0.5 V for LTD) has excellent symmetry as the result of the ratio of $\Delta G_1/\Delta G_2$ floats within 2.1% (**Figure 3.15g**). To match higher learning efficiency in the ResNet algorithm, the number of conductance that can be effectively utilized (Nseff) and nonlinearity from 16 LTP/LTD curves are researched. Moreover, the conductance difference (ΔG) between the two synaptic transistors (G^+ and G^-) is used to represent the weight range (-1 to 1) in the algorithm. Notably, the left and right parts of the curve need to match the symmetry because the rising and decline stages of conductance should have one-to-one correspondence [56]. To explore the regulation of optical pulse on nonlinearity and symmetry, type II and type III are developed (**Figure 3.15h)**. To clearly show the modulation of three modes for updating rules, the parameters, including the nonlinearity, symmetry, and update interval, are analyzed to highlight the prominent advantage of applying Type III (**Figure 3.15i**). Consequently, the RegNet of neural network based on the dynamic learning rate according to the nonlinearity, symmetry, and update interval of the update rule is proposed for the classification task. To match higher learning efficiency in the ResNet algorithm, the number of conductance that can be effectively utilized (N_{seff}) and nonlinearity from 16 LTP/LTD curves are researched (**Figure 3.17**).

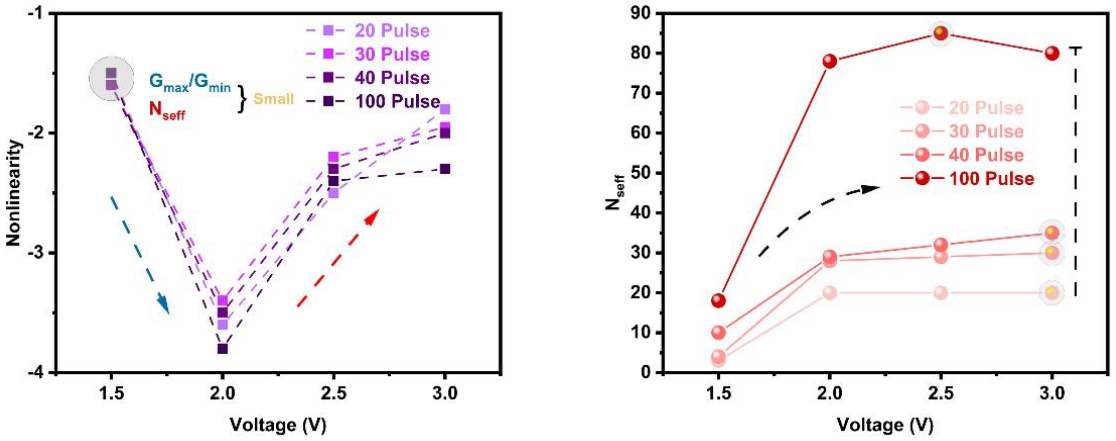

Figure 3.17 Specific update rule parameters (a) The Nonlinearity extracted from the 16 LTP/LTD curves. (b) The effective conductance number for the 16 LTP/LTD curves.

Section 3.2.4 The immunological classification based on dynamic update process (ResNet matching ELISA)

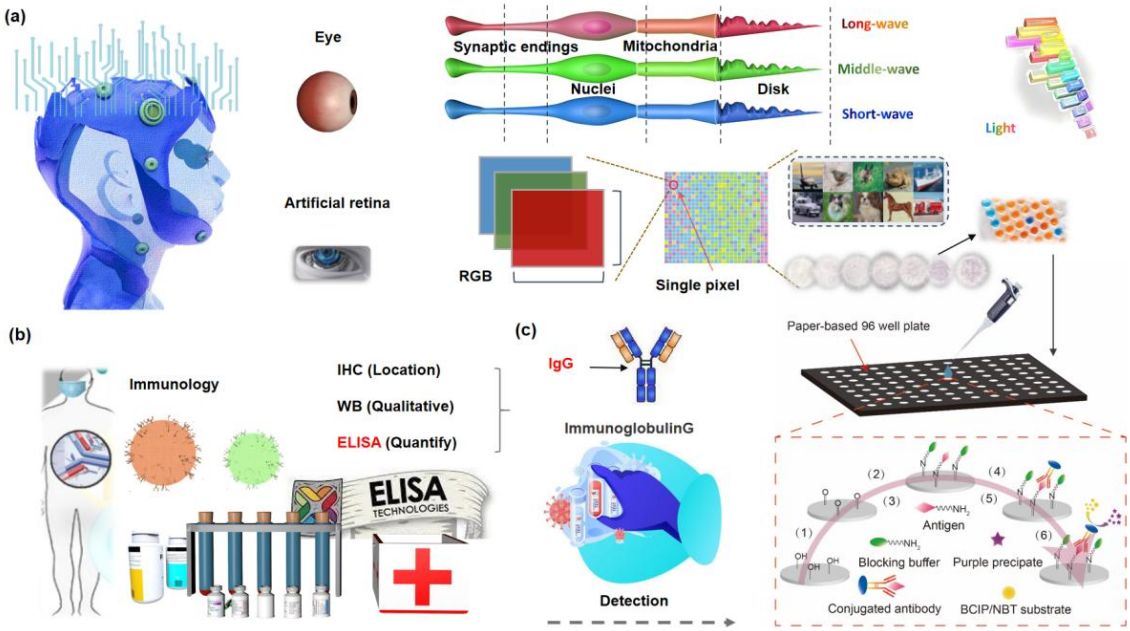

Figure 3.18 Immunological application of MOF transistor (a) Schematic diagram of the visual receptor accepts light stimulation of short, middle, and long wavelengths through three kinds of cone cells. (b) Significance of c-ELISA in immunology and its detection methods. (c) Schematic diagram of a direct c-ELISA performed in a μPAD and the image results of seven Rabbit IgG concentrations (0, 6.7 pM, 67 pM, 670 pM, 6.7 nM, 67 nM and 670 nM).

The human brain processes the external information mainly through various senses and perceptions-most behaviors and decisions from neurons and synapses are based on the visual receptor. Pyramidal cells and optic nerve are connected one-to-one, distinguishing the short-wave, middle-wave, and long-wave light (**Figure 3.18a**). Artificial retina based on the synaptic devices identify RGB values from a single pixel [50-57]. The c-ELISA is the gold standard in immunoassays for the quantitative detection of antibodies, antigens, proteins, hormones, etc. (**Figure 3.18b**). Also, c-ELISA can be widely used for rapid antibody screening tests for viruses (human immunodeficiency virus (HIV), Covid-19 virus, etc.), autoimmune diseases, progesterone HCG, laboratory and clinical studies, and other

diagnostics. **Figure 3.18c** shows the schematic diagram of a direct c-ELISA performed in a μPAD and the image results of seven Rabbit IgG concentrations (0, 6.7 pM, 67 pM, 670 pM, 6.7 nM, 67 nM and 670 nM). The specific experimental steps will be described in the experimental section.

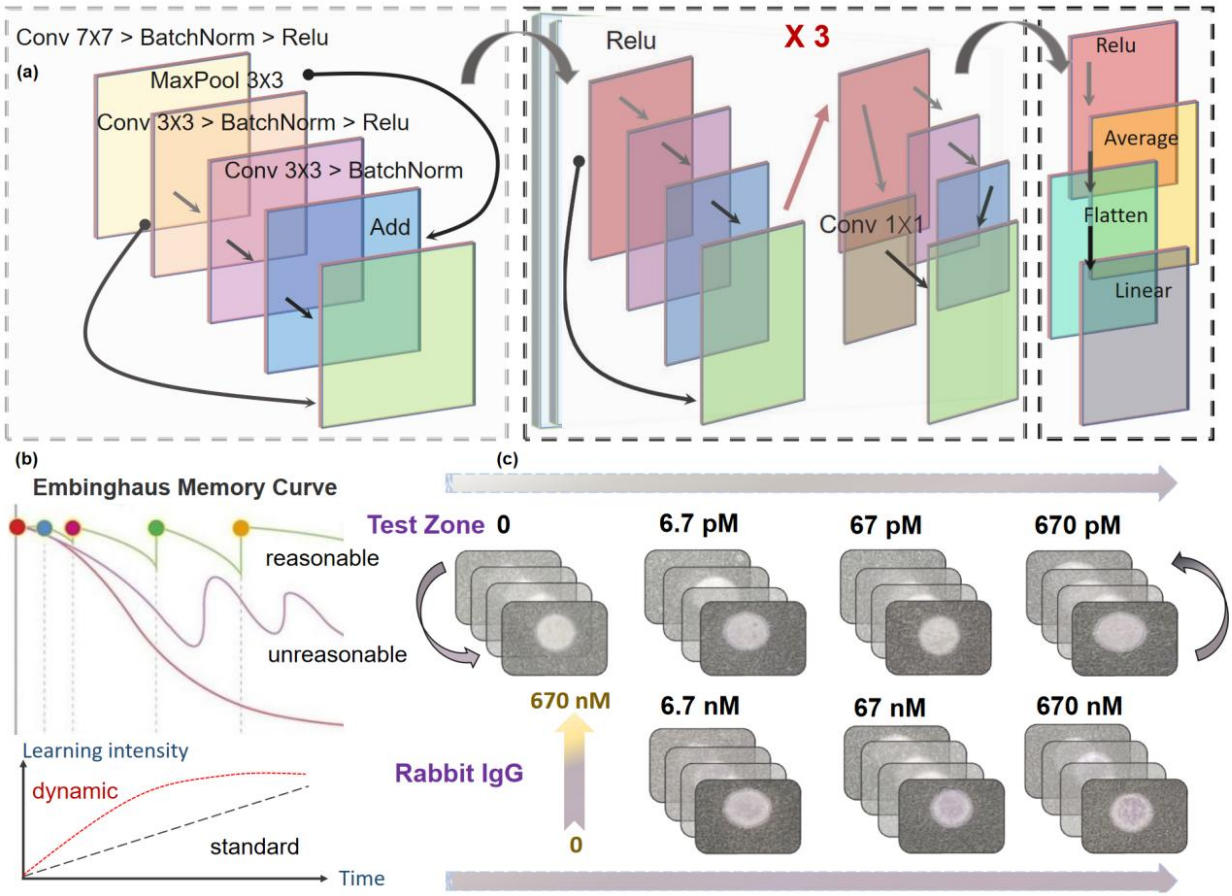

Figure 3.19 Algorithm framework and matching data-set (a) Block diagram of feedforward for the dynamic neuromorphic deep residual learning. (b) Standard and dynamic learning rule based on the Embinghaus memory. (c) Image database of ELISA of seven Rabbit IgG concentrations (0, 6.7 pM, 67 pM, 670 pM, 6.7 nM, 67 nM and 670 nM).

To track the problem of deeper neural networks being more difficult to train, the ResNet with a residual learning framework is proposed to simplify the training of networks and gain accuracy from considerably increased depth [57]. The degradation in the convergence process indicates that not all systems are similarly easy to optimize and can be solved by a deep residual learning framework (**Figure 3.19a**). The building block demonstrates that

feedforward neural networks with shortcut connections can realize the formulation. Moreover, a backward neural network updates the synaptic weight layers with a dynamic learning rate according to the parameters extracted from the LTP/LTD curves. Inspired by the Embinghaus memory map, dynamic learning rules are more in line with the memory behavior of biological synapses (**Figure 3.19b**). The ResNet contains the dynamic algorithm adopted to execute the classification task of ELISA for rabbit IgG. The collected data includes the 0, 6.7 pM, 67 pM, 670 pM, 6.7 nM, 67 nM and 670 nM seven concentrations (**Figure 3.19c**).

The error feedback part in the algorithm is based on the update rules measured by type III (electric pulse combines blue light pulse). Compared with the standard case (lr=0.1), the classification accuracy for seven rabbit IgG is improved from 80.9% to 87.2% after 100 weight iterations. The influence of different colors of light in Type III on the dynamic learning step shows the regulation ability of light (**Figure 3.20a**). Inspired by the first impression of human brain cognition, the dynamic learning rate makes the update step in the initial epoch larger than in the later epoch of the training process because the LTP/LTD curve trend is a convex function [58-60]. Each output in the last layer is connected to 128 neurons, so **Figure 3.20b** shows the iterative updated 7×128 weight matrix. The complex disordered weight matrix proves that the weight value gradually differentiates into two extreme values (G_{max} and G_{min}) by relying on the Manhattan rule.

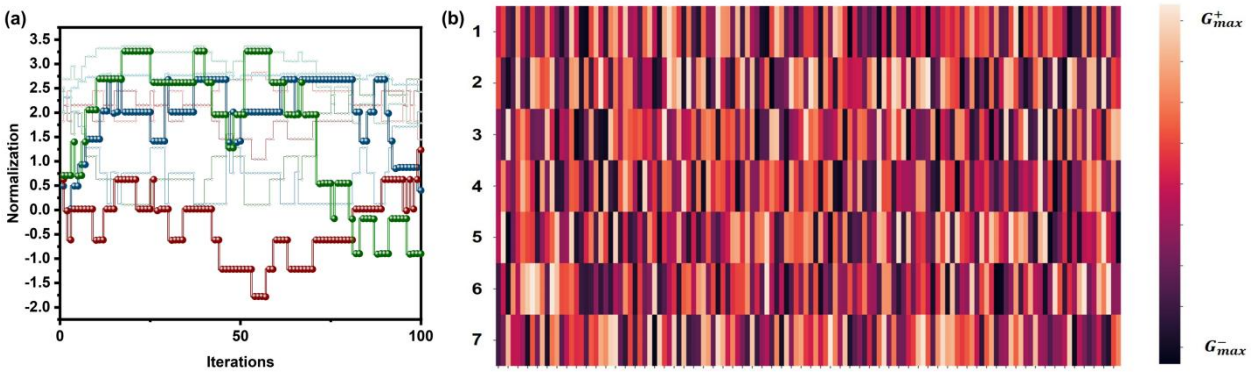

Figure 3.20 Iterative changes in conductance (a) Trend of normalized dynamic learning step with the number of iterations. (b) 7×128 weight matrix connects the last output layers.

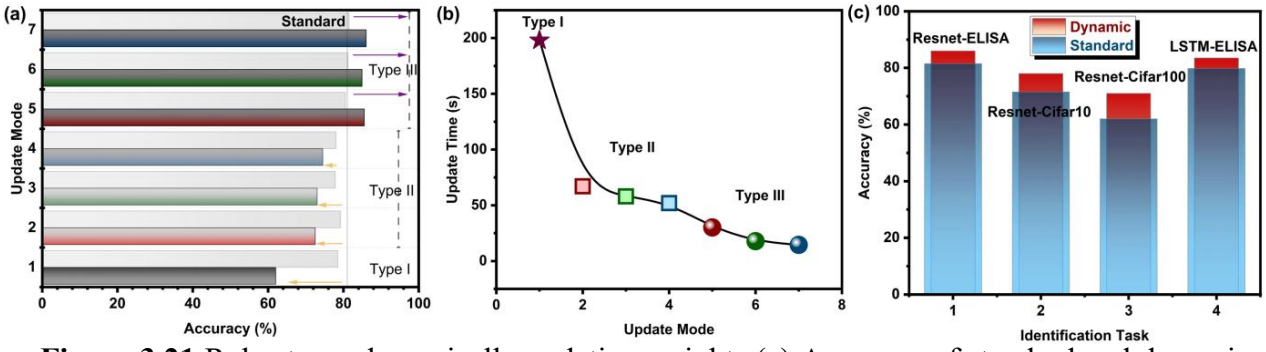

Figure 3.21 Robustness dynamically updating weights (a) Accuracy of standard and dynamic conditions for three modulation modes. (b) Update time during the ResNet neural network training process for Type I, Type II, and Type III. (c) Verify the robustness of dynamic learning rules which extend to the ResNet-ELISA, ResNet-Cifar10, ResNet-Cifar100, and LSTM-ELISA tasks.

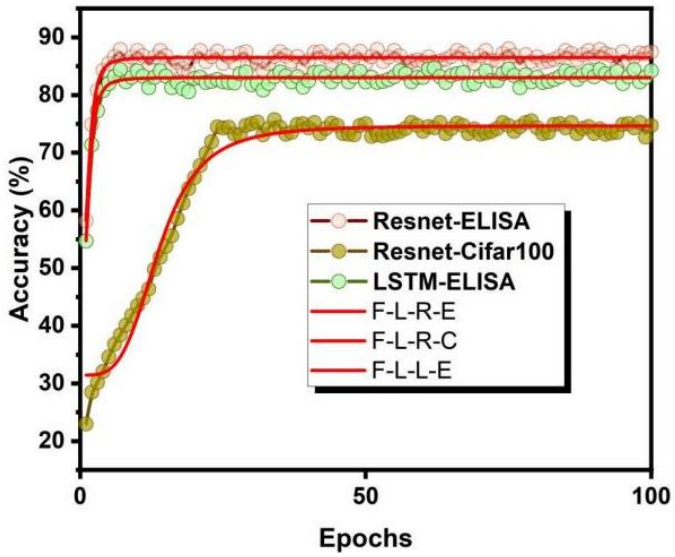

Figure 3.22 The detailed training process of Resnet-ELISA, Resnet-Cifar100, and the LSTM-ELISA.

To analyze the modulation effects of the three modes, the standard accuracy and dynamic accuracy under seven conditions (Type I, Type II_Red, Type II_Green, Type II_Blue, Type III_Red, Type_Green, Type III_Blue are displayed (**Figure 3.21a**). On the one hand, the dynamic accuracy is higher than the standard accuracy in Type III modulation due to the nonlinearity and excellent symmetry. On the other hand, the small update interval in Type III shortens the whole iteration update time for the training process. As shown in **Figure 3.21b**,

the update times for red, green, and blue modes of Type III are 11.6 s, 18.4 s, and 27.4 s, respectively. Consequently, the ResNet combined with characteristics can improve the classification compared with the standard situation and reduce the update time when the modulation mode Type III is adopted.

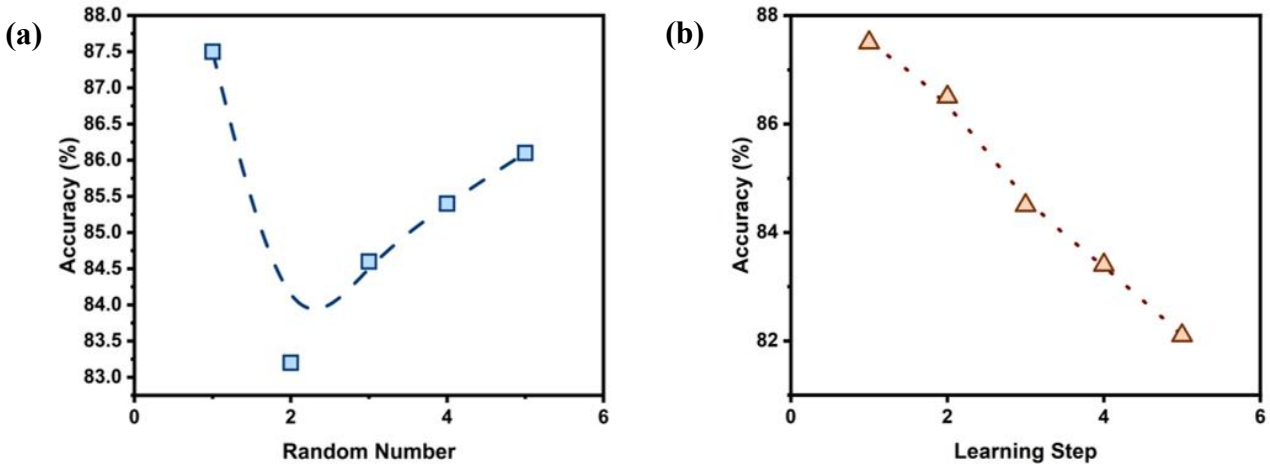

Figure 3.23 Impact of initial setting on accuracy (a) The effect of random number on recognition rate. (b) The effect the range of learning 87step on recognition rate.

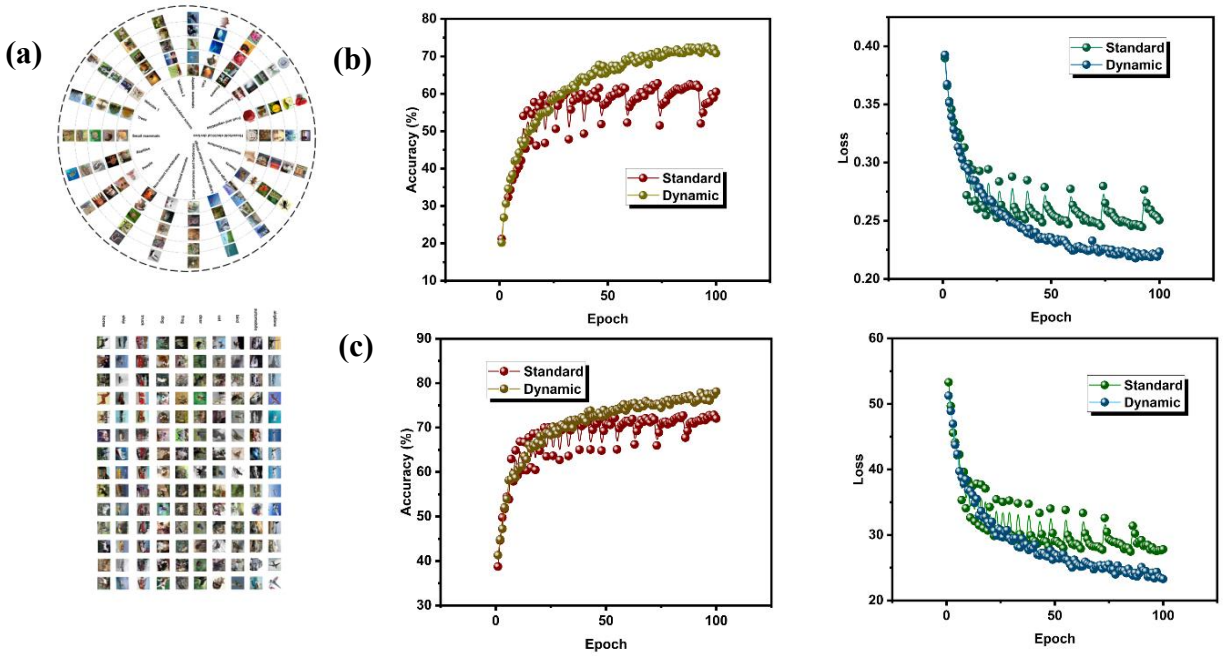

Figure 3.24 Validation of robustness using other standard datasets (a) The database of Cifar10 and Cifar100. (b) The accuracy and loss for Cifar100. (c) The accuracy and loss for Cifar10.

Furthermore, to verify the robustness of the dynamic learning rules in a similar deep neural network, the accuracy of different algorithm structures in identifying different classification tasks is compared (**Figure 3.21ec**). The four neural networks and corresponding tasks are ResNet-ELISA, ResNet-Cifar10, ResNet-Cifar100, and LSTM-ELISA. The **Figure 3.22** demonstrate operation speed of Resnet-ELISA, Resnet-Cifar100, and the LSTM-ELISA through the detailed training epochs. The recognition rate is not significantly affected by the initial weight when the random floating value is smaller than the learning step in a random process(**Figuer 3.23**). The database of Cifar10 and Cifar100 and the results of verifying robustness explicitly demonstrate the feasibility of a dynamic learning rate (**Figure 3.24**). The obvious result is that above neural networks with dynamic learning rate strength, the classification ability resulting from the average improved accuracy is 6.8%.

Section 3.3 Conclusion

Applying stimulation (electric pulse, optical pulse, or stress) to the pre-synaptic terminal simulates the realization of synaptic plasticity for the bionic nerve. The stability and controllability of the storage process has to be strengthened, despite the results of optoelectronic hybrid mode's significant in low power consumption. Moreover, the dimension of materials influences the transmission efficiency and data processing when the synaptic devices are integrated for parallel computing. A comprehensive modulation of mixed photoelectric pulses for LTD and LTP has been lacking in recent years. Furthermore, the influence of the fundamental symmetry and linearity of conductance in the rising and falling stages during the algorithm of error feedback is also not properly considered, and the weight updating process is merely simulated in accordance with the fitted LTP/LTD curves. In previous research, the standard case (LTP/LTD) are two straight lines) generally adopted is that the learning step in each epoch is the fixed value. Afterward, inspired by the first impression of human cognition, the relationship between learning efficiency and temporal memory is nonlinear. In other words, a great of accurate information can be retained and learning is generally particularly efficient in the early stages. The ΔG between two synaptic transistors is normalized to represent the synaptic weight connection strength of two neural units due to the weight range in the neural algorithm containing the negative value. Consequently, the convex function composed of LTP/LTD curves can provide a tight connection strength at the initial epoch of training, and the strength gradually decreases with the increase of the number of iterations. According to each non-fixed stage on the curve, the proposed dynamic learning rule provides the mapping relationship between the dynamic learning step and epochs. The one-to-one symmetry of conductance in the potentiation and depression stages, in addition to nonlinearity, provides assist dynamic response of neuromorphic computing. The iteration direction of synaptic weight is based on the

Manhattan rule in the error backpropagation. Therefore, the updated trend of non-monotonicity requires strong symmetry of LTD/LTP. The strength of symmetry is then suggested to be measured by the ratio of $\Delta G_1 / \Delta G_2$. Previous research has shown that conventional neural networks (such as ANN and CNN) are unable to accomplish indistinguishable categorization tasks due to degradation presents both challenges on by the depth of network layers. The residual learning framework is proposed to simplify the training of networks that are substantially deeper than those previously used. The layer as the learning residual function is explicitly redefined by the reference layer, instead of the learning the unreferenced function. Besides, the differences between various tags are amplified as network layers increase, making it easier to distinguish between tags with a high level of similarity.

In conclusion, this **Chapter 3** demonstrates the Al/InOx/MXenes/ZrOx-Li/Si/Al structure of synaptic transistor as bionic retina and proposes dynamic neuromorphic deep residual learning strategy for the recognition of ELISA_IgG in immunology. PPF, STP/LTP and EPSC are basic information flow, also are the typical manifestation of synaptic plasticity. Here, we analyze that the dynamic learning rate, update interval, and learning accuracy rate according to the various LTP/LTD curves which regulated separately by three modulation modes (Type I, Type II, and Type III). The synaptic devices stimulated by Type III have high linearity and symmetry, which is necessary to reduce the number of training epochs in the neural network. At the same time, the fast conductance recovery trend can reduce the interval of each calculation. Moreover, recognizing the Rabbit IgG of ELISA to demonstrate the potential in immunology for immune protein detection and other neural networks (LSTM) composed of the Cifar10 and Cifar100 database are then developed to verify the robustness and feasibility. The synaptic transistor based on 2D materials and dynamic learning strategy enriches weight update process of neural morphological systems and further developed as bionic retina to successfully complete complex visual perception task.

Section 3.4 References

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Chapter 4 Exploration of complex biological characteristics, neural networks similar to the human brain, and systematic architecture (Synaptic Transistor with Multiple Biological Function Based on Metal-Organic Frameworks Combined with LIF Model of Spiking Neural Network to Recognize Temporal Information)

Section 4.1 Experimental Section

The preparation processes of the InO_x and ZrO_x precursor solutions are introduced in Chapter 2.1 and Chapter 3.1, respectively. The characterization of synaptic plasticity and SNN simulation are also introduced in Chapter 2.1 and Chapter 3.1.

Section 4.1.1 Synthesis and fabrication of synaptic transistors

All solutions were vigorously stirred under atmospheric conditions for 5 hours and filtered before spin coating using 0.25 μm PTFE syringe filters, respectively. Typically.1.0 mmol of cobalt nitrate hexahydrate and 4.0 mmol of 2-methylimidazole are dissolved in 15,0mL methanol,respectively. Then, the 2-methylimidazole solution is slowly poured into the soution of cobalt nitrate hexahydrate under stirring for 6h, After aging at room temperature for 16 h, a purple precipitate is collected by centrifugation, washed with methanol, and dried at 70 ºC 12h. Then, ZIF-76 (the purple powder) is obtained characterized by XRD. Finally, the obtained mixture was centrifuged again at 3500 rpm for 3 min to obtain a black-brown few-layer dispersion of about 5 mg mL^{-1}. The dispersion is stored in an argon atmosphere, and the storage time does not exceed 14 days.

First, a heavily doped Si (n^{++}) substrate was cleaned by deionized water and dried under N_2 flow. Afterward, the processed substrate was further treated by Plasma for 15 minutes to

allow the film surface hydrophilic treatment. The ZrO_x and ZrO_x-Li films were spin-cast with precursor solution at 4500 rpm for 30 s and then annealed for 80 mins at 250°C in the air atmosphere.Then, the ZIF-67 solution was then diluted to 1 mg/mL and spin-coated at 3000 rpm for 20 s on the surfaces of ZrO_x and ZrO_x-Li films. Substrates with solution film were then oxidized at 80°C for 1 min on a hotplate in air condition. The InO_x film was spin-cast with precursor solution at 3500 rpm for 30 s and then annealed for 1h at 200°C for the in the air atmosphere. The 30 nm thick Al S/D electrodes were fabricated by thermal evaporation through the shadow mask.

Section 4.1.2 SNN simulation

We use a SNNs as the base model, which is a compact and efficient neural network. After we convert the SSVEP data into two-dimensional matrix data, we could directly pass it into the block. The LIF block is the main component of SNNs. Compared with the ordinary neural network structure, the LIF and STDP block could not only perform weighted operations through the convolution layer and activation function mechanism to extract features, and also retain the initial information of the input data and fuse it with the obtained feature information. Two blocks and one linear layer are used in our model. The input image data is passed through two residual blocks to complete the feature extraction, and then passed to the linear layer to complete the final classification task. Usually, this is a complete SNNs workflow, and we use a standard learning rate in the training step. After each training of the network, different learning steps are used to update the network parameters according to the change direction of the loss.

Section 4.2 Results and Discussion

Section 4.2.1 Basic transistor characteristics, device structure, and characterization

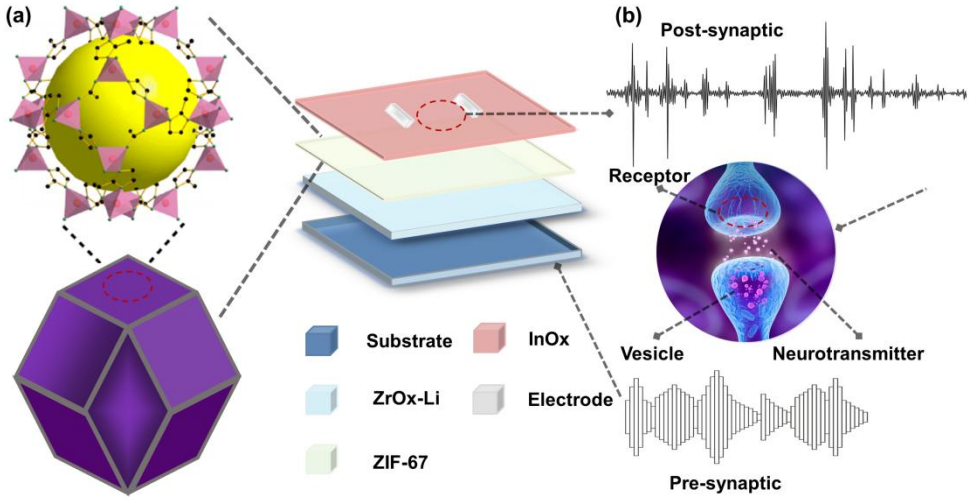

Figure 4.1 MOF synaptic transistor (a) Structure diagram of the synaptic transistor and basic crystal of ZIF-67. (b) Biological chemical synapse is illustrated schematically, comprising a pre-synaptic terminal, receptor, and a post-synaptic terminal.

To promote the systematization of three-terminal neuromorphic devices, we have constructed a modifiable synaptic device with MOFs as the main functional layer (**Figure 4.1a**) [1]. The device is composed of the following layers, from top to bottom: source/drain, InO_x, ZIF-67, ZrO_x, substrate, and gate. The ZIF-67 layer, acting as the trapping layer, can capture and release carriers to change the conductance in the channel when a positive/negative voltage is applied to the gate [2, 3]. In order to provide a vivid explanation of the relationship between biological synapses and electronic synapses, we liken the process of converting chemical signals into electrical signals from the pre-synaptic terminal to the post-synaptic terminal (neurotransmitters released by synaptic vesicles are accepted by receptors on the membrane) to applying a pulse to the gate of the device and receiving a corresponding pulse between the source/drain (EPSC) (**Figure 4.1b**).

To clearly display the MOF structure of ZIF-67, we analyzed SEM images at four different resolutions (**Figure 4.2a**). These results provide valuable insights into the design of neuromorphic computing devices and the potential for energy-efficient processing.

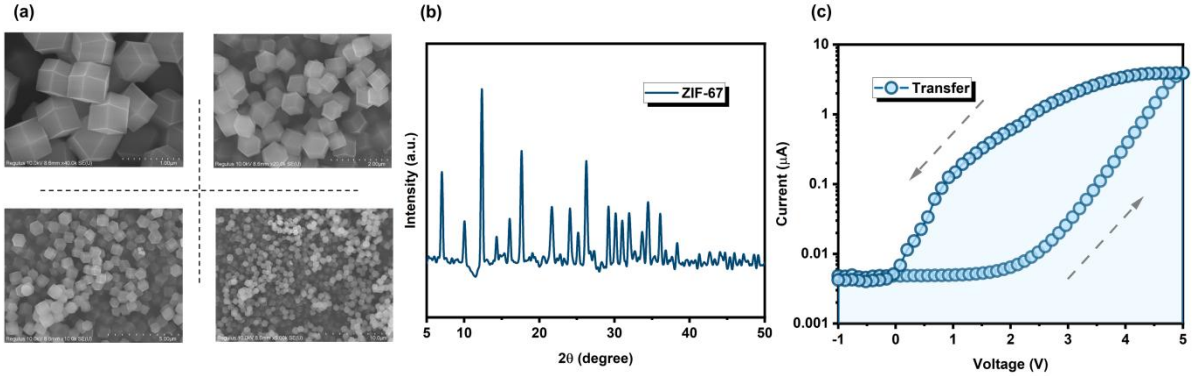

Figure 4.2 Exploring the properties of MOF (a) SEM images of the ZIF-67. (b) XRD patterns of the ZIF-67. (c) Channel current dependence of the gate voltage analyzed at V_{post} of 0.5 V.

The SEM images of the as-prepared ZIF-67 sample reveal that it exhibits a uniform size distribution with well-defined cubic morphology, demonstrating excellent dispersion and a solid interior. These observations provide valuable insights into the structural characteristics of the MOF material and its potential for use in neural applications, including neuromorphic computing devices. The uniform size and cubic morphology of the ZIF-67 particles suggest that they could offer excellent stability and reproducibility in device fabrication processes. Additionally, the well-defined morphology and solid interior of the particles suggest that they could provide a high surface area-to-volume ratio, potentially enhancing their performance in various applications. Overall, the SEM images provide important information about the structural properties of ZIF-67 and its potential for use in a wide range of AI and neuromorphic applications. The crystalline structure of the ZIF-67 sample was analyzed using XRD, which revealed that the main characteristic peaks of the bare ZIF-67 matched well with those reported in the literature (**Figure 4.2b**). These results indicated the successful synthesis of the MOF material on the ZrO_x substrate [1-5]. The XRD analysis was further supported by the SEM characterization, which demonstrated that the ZIF-67 particles exhibited a uniform size and cubic morphology with good dispersion and a solid interior. The successful synthesis

of ZIF-67 on the ZrO_x substrate has been confirmed by both SEM and XRD characterizations. The transfer characteristics of the device are presented in **Figure 4.2c**, where the channel current increases as the applied voltage from -1 V to 5 V, exhibiting a typical n-type transfer behavior [6-8]. The application of a higher positive gate voltage results in the migration of more cations from the electrolyte into the porous MOF channel, leading to n-type doping of the MOF channel and an increase in its conductivity [9-12]. The porous nature of MOFs allows for easy penetration of cations into the channel under low gate voltage, thereby enabling the ZIF-67 synaptic device to operate as a low-voltage transistor with low power consumption.

Section 4.2.2 Three biological function and correspond synaptic characteristics.

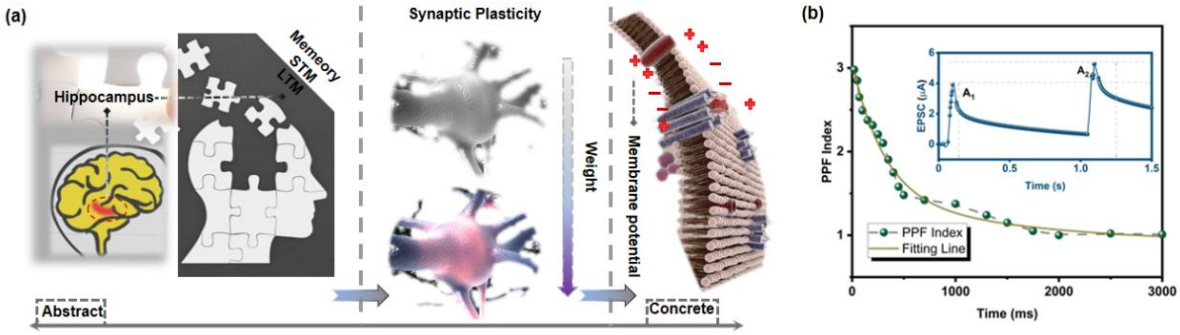

Figure 4.3 Special biological functions of MOF (a) Device simulates three typical functions of synapse: forming memory, synaptic plasticity, and stimulating membrane potential. (b) PPF index is a measure of synaptic facilitation defined as the ratio of the amplitudes of the first (A_1) and second (A_2) EPSCs, plotted against the pulse interval (Δt).

In order to demonstrate the three typical neuronal functions of the proposed synaptic transistor, standard electrical tests are performed for validation (**Figure 4.3a**). Firstly, the memory function (STM/LTM) of the human brain primarily originates from the hippocampus, which is the foundation of memory and the basis of all intelligent life [10-14]. The hippocampus also promote frequent association of events and forgetting unimportant information. Secondly, synaptic weight and plasticity refers to the strength or amplitude of the connection between two nodes, which in biology corresponds to the amount of influence that one neuron has on another node through its discharge [15-17]. Thirdly, biological neurons only transmit stimuli to other neurons they are connected to when they receive external stimuli that exceed a certain threshold, thereby facilitating information exchange through membrane potential. The occurrence of PPF is associated with the release of neurotransmitters by pre-synaptic neurons and is typically believed to be regulated by calcium. The synaptic plasticity characteristics of the ionotronic synaptic transistor were investigated by analyzing the PPF index, which is crucial for recognizing visual signal information in biological neural systems. Paired input spikes with various time intervals (Δt) are used to trigger the PPF index (A_2/A_1), and the resulting secondary EPSC peak (A_2) is compared to the first one (A_1) to

determine the presence of facilitation behavior. In **Figure 4.3b**, the generated A_2 is 301% higher than A_1 when the time interval is 20 ms. The PPF index reflects the extent of synaptic connection enhancement between neurons and can be simulated using the double-exponential function. Initial constants of rapid and slow phases C_0, C_1, and C_2 are 1, 15%, and 33%. The relaxation times are τ_1 (15 ms) and τ_2 (20 ms).

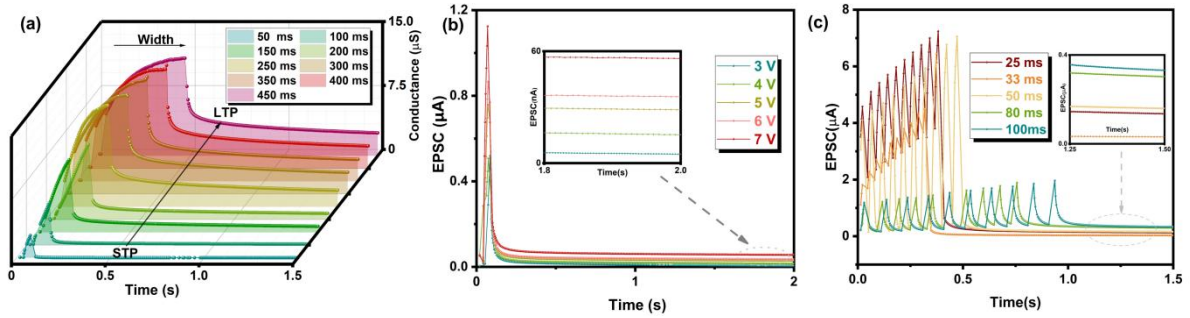

Figure 4.4 Temporal Synaptic plasticity (a) EPSC behaviours activated and modified by electric pulses with 9 different widths (50 ms, 100 ms, 150 ms, 200 ms, 250 ms, 300 ms, 350 ms, 400 ms, and 450 ms) at V_{DS}=0.5 V. (b) EPSC triggered by 5 single electric pulse with different amplitude (3 V, 4 V, 5V, 6 V, and 7 V). (c) Low-pass filtering characteristics are shown by 10 continuous pulses of different frequencies (10 Hz, 12.5 Hz, 20 Hz, 30 Hz, and 40 Hz) applied to the pre-synaptic terminal.

To accurately assess the impact of a single pulse on synaptic plasticity, we analyze the effects of electric pulses with different widths and amplitudes on EPSC excitation. We measure the dynamic current behaviors responsive to gate voltage pulses with different width (50 ms to 450 ms) and the same amplitude of 1.5 V (**Figure 4.4a**). After reaching a peak value, the EPSC returns to its original current state, indicating that the peak values are proportional to the amplitude of the voltage pulses. Nevertheless, it has been observed that pulses with a width greater than 50 ms do not fully return to their original state, indicating significant nonvolatile properties. This behavior is similar to that seen in biological excitatory synapses. Additionally, low power consumption is crucial for developing an energy-efficient neuromorphic chip. By multiplying the peak value of the EPSC, the drain voltage, and the

pulse duration, it is estimated that the power of a single spike generated by the gate voltage of −1 V is 1.8 nJ [18-21]. In order to further discuss the effect of temporal properties on synaptic plasticity, we demonstrate the EPSCs responsive to the gate voltage pulses with different amplitudes (3 to 7 V) and the same duration times of 50 ms (**Figure 4.4b**). Ion doping into the ZrO_x layer plays an important role in lowering the range of width. Curiously, ZIF-67 synaptic transistor has the characteristic of filtering high-frequency information which is similar to the LIF neuron (**Figure 4.4c**). High frequency pulses actually result in lower conductance increments than low frequency pulses.

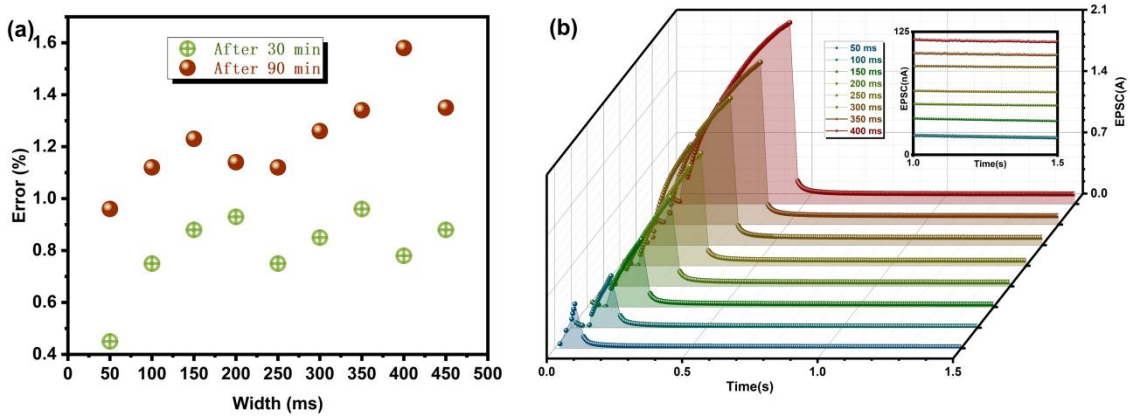

Figure 4.5 The long-term retention of synaptic plasticity after 30 minutes and 60 minutes. (b) Typical EPSC when Li ion doping concentration is 5 %.

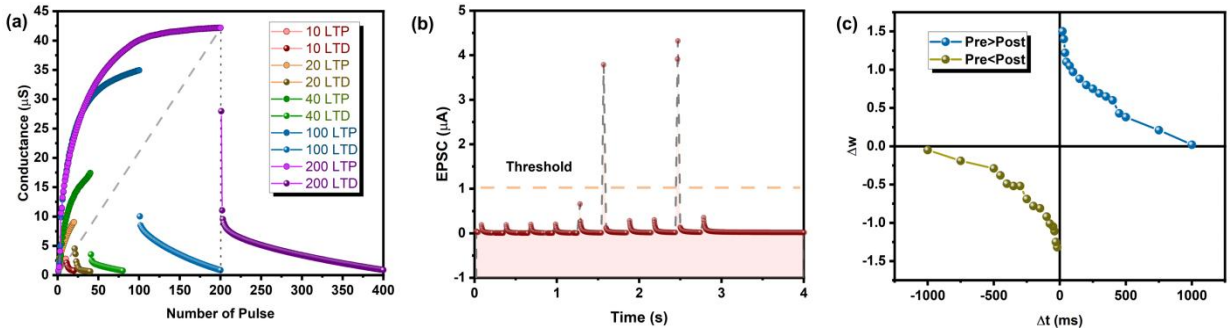

Figure 4.6 Hardware parameters required for simulating SNN (a) LTP/LTD characteristic demonstrates the controllable range and level of conductance. (b) Threshold effect of synaptic device as biological neurons. (c) Trend of STDP curve as weight update rule transform the temporal information.

To demonstrate the conductance retention characteristics of the synaptic device, **Figure 4.5a** shows the fluctuation of the currents within 30 minutes and 90 minutes, respectively. In order to further verify the effect of ion migration on synaptic plasticity, **Figure 4.5b** shows the EPSC when the doping concentration is 5%.

Detailed investigations have been carried out on the characteristics of LTP/D, which are essential features for synaptic operation in neuromorphic computing. The various conductance states of synaptic devices were demonstrated in **Figure 4.6a**, where a sequence of excitatory spikes (V_{DS} = +1 V, t_d = 50 ms, Δt = 100 ms) and inhibitory spikes (V_{DS} = -1 V, t_d = 50 ms, Δt = 100 ms) were applied. The peak current increased gradually from 8.9 μA to 42.5 μA as the quantity of pulses rises from 20 to 100 and recovered to the initial level under application of the excitatory and inhibitory spikes, respectively [22-25].The LTP/LTD curves show the conductance margins (G_{max}/G_{min}) between the maximum and minimum conductance values as a function of the number of spike pulses. In neuromorphic computing, the iterative update rule between neurons is constrained by weights represented by conductance of synaptic device [22-24]. To further verify the membrane potential threshold of synaptic transistors, we applied continuous pulses (V_{DS} = +0.5 V, t_d = 50 ms, Δt = 200 ms) that avoid the potentiation of conductance (**Figure 4.6b**). As observed from the red line, the transient accumulation of ion migration in MOFs can result in the release of an instantaneous pulse exceeding the threshold (1 μA). The measured alteration of synaptic weight following each neuron spiking event is depicted in **Figure 4.6c** using the synaptic device structure. An increase (decrease) in synaptic weight occurs when the pre-neuron spikes before (after) the post-neuron [25-29]. Moreover, the synaptic weight change with respect to the spike timing difference (Δt) can be accurately described by exponential decay functions, confirming that the STDP properties are similar to those observed in biological synaptic systems. It is apparent that upon approaching $\Delta t = 0$ from $\Delta t = 0.1$ s, the synaptic weight is potentiated. While for $\Delta t < 0$, the synaptic weight is

depressed. This behavior is known as the asymmetric Hebbian learning rule. Different ratios (3.809, 14.481, 22.905, 52.620, and 53.36) indicate the resolution between synaptic weight updates and the corresponding learning step size (**Figure 4.7a**). Furthermore, we measured the extreme conditions that trigger STDP to ensure that the neural device can be efficiently and continuously updated (**Figure 4.7b**).

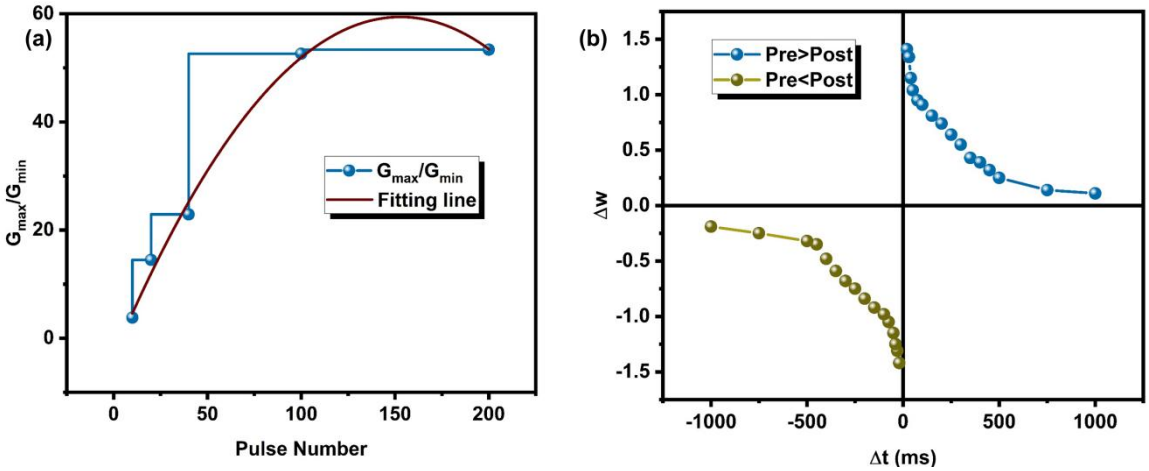

Figure 4.7 Timing rules required for pulse weight update (a) The G_{max}/G_{min} ratio of 10, 20, 40 100, and 200 LTP/LTD curves. (b) The minimum voltage that can trigger the STDP.

Section 4.2.3 Systematic architecture includes the LIF model combine with synaptic device and SNN.

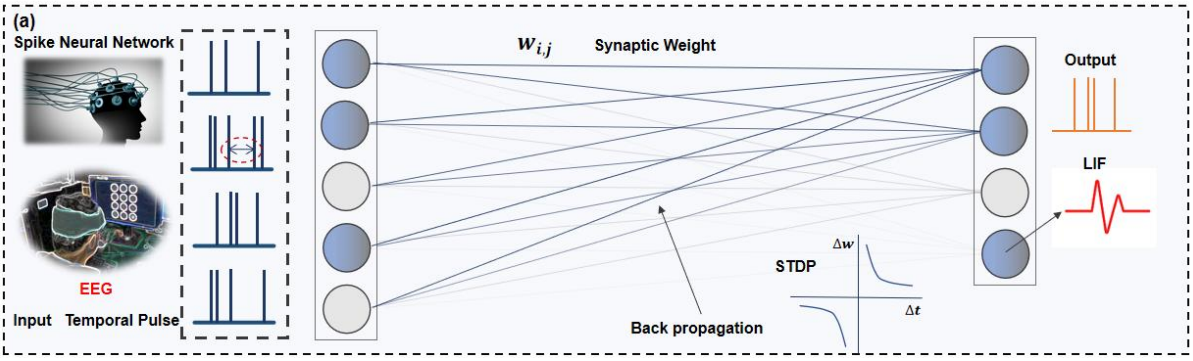

Figure 4.8 Block diagram of feedforward and back propagation for spiking neural network based on the LIF neuron model and STDP weight update rule.

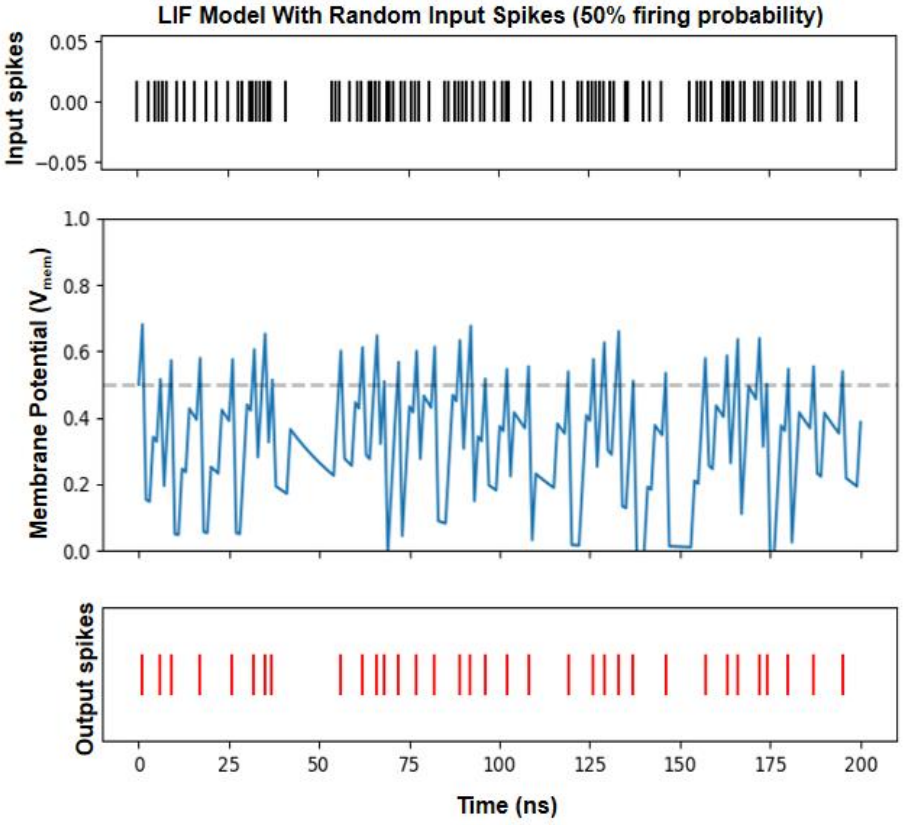

Figure 4.9 LIF model with random input spikes (50% firing probability).

The desire to replicate the remarkable energy efficiency of biological systems has been a significant driving force behind the advancement of SNNs (**Figure 4.8**).One main theory for the superior energy efficiency of SNNs is their significantly higher information capacity when compared to other neural network models, like the multi-layer perceptron, which is based on

firing rates. In contrast to SNNs, training firing-rate networks often involves the use of backpropagation algorithms, which can be challenging to implement efficiently due to the centralized method for computing weight updates and the need for large amounts of high-precision memory [30-32]. In SNNs, the LIF neuron model is commonly used to simulate the behavior of neurons. The LIF model can simulate how neurons receive and process signals from other neurons and fire a spike when a certain threshold is reached. Additionally, the leaky integration mechanism in the LIF model can mimic the gradual decrease of membrane potential in biological neurons over time. STDP is a key mechanism in SNNs that describes how the strength of synapses between neurons changes over time based on the timing of their spike activities.

Figure 4.9 shows the LIF model of standard SNNs with random input spikes (50% firing probability). Synaptic weights are updated through the STDP mechanism to simulate learning and adaptation between neurons. Together, the LIF neuron model and STDP mechanism play crucial roles in SNNs, enabling the simulation of neuronal activity and plasticity.

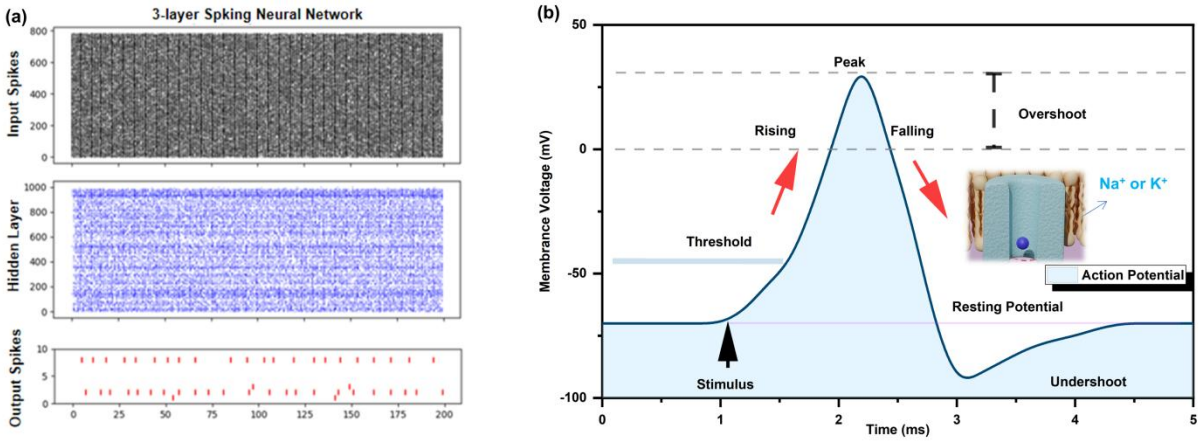

Figure 4.10 The core unit of SNN (a) 3-layer of improved Spiking Neural network based on the STDP of synaptic transistor. (b) Fluctuation area of membrane voltage in biological neurons.

Figure 4.10a demonstrate the 3-layer of improved spiking neural network based on the STDP of synaptic transistor. The LIF neuron model simulates the changes in membrane potential

(V_m) of a neuron over time (**Figure 4.10b**). The V_m changes are determined by the flow of ions through various channels in the neuron's membrane [33-34]. Initially, the neuron is at rest with a resting membrane potential. When a presynaptic neuron sends a signal to the postsynaptic neuron, it causes a small increase in V_m, known as the postsynaptic potential (PSP). If enough PSPs are received, V_m reaches a threshold voltage, at which point an action potential or spike is generated and sent down the axon of the neuron. After a spike is generated, the neuron enters a refractory period where it cannot generate another spike, known as the absolute refractory period [34-36]. The reason for the lack of spike generation is the deactivation of ion channels.

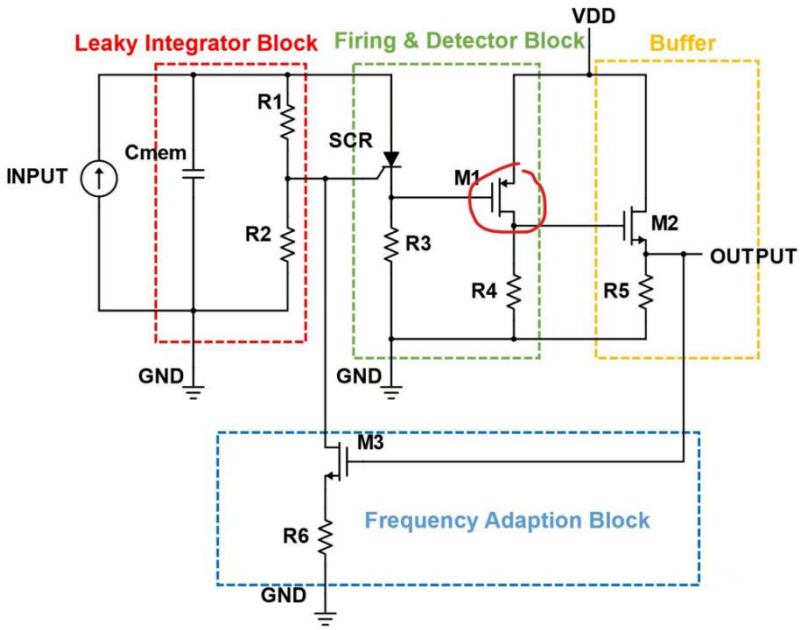

Figure 4.11 Leaky integrator block, fire & detector block, buffer block, and frequency adaption block combine with output of ZIT-67 synaptic devices to form the complete LIF system.

To address this issue, a highly compact electronic circuit has been developed that can implement the leaky integrate-and-fire model of artificial neurons (**Fig. 4.11**). The leaky and integrate characteristics of the model are implemented through the use of an RC pair. The capacitor (C) integrates the incoming current spikes, while the resistor ($R=R_1+R_2$) allows the charge to leak out during the time intervals between spikes. The crucial firing feature of the

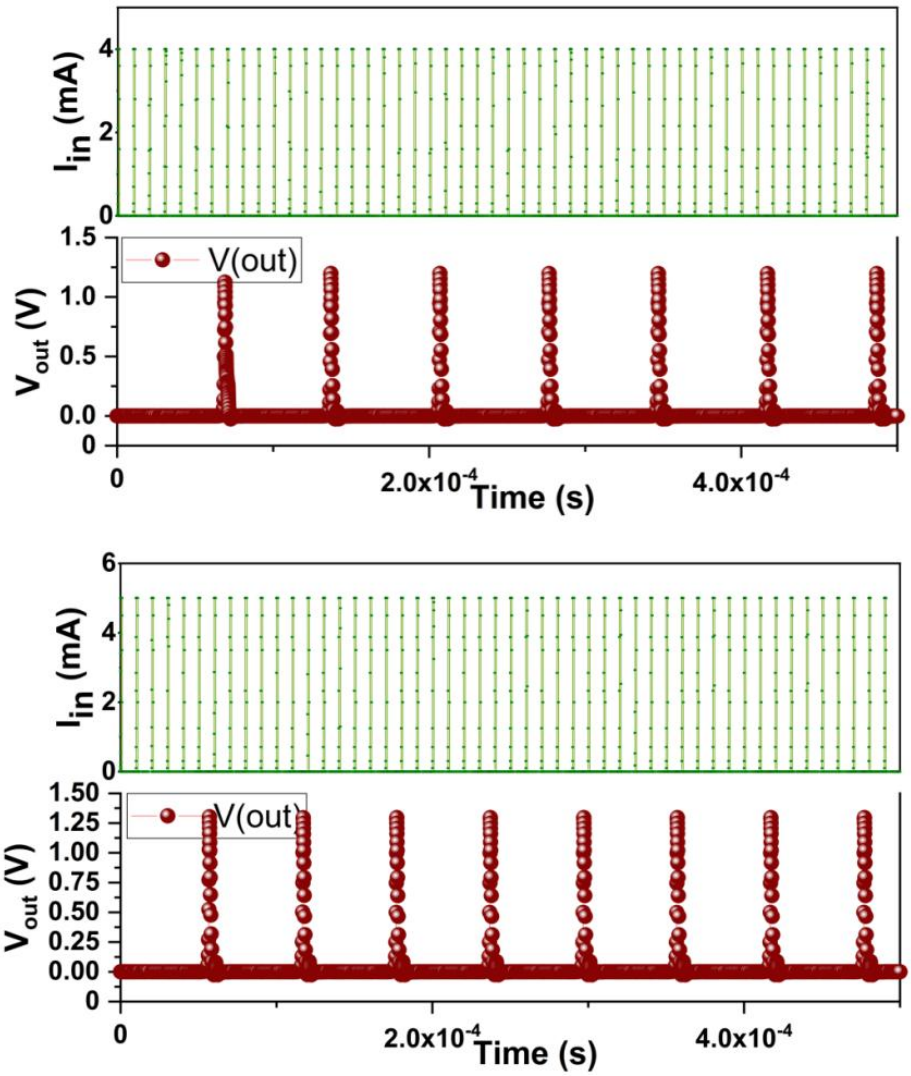

Figure 4.12 Change of membrane potential under different input pulses.

model is achieved by setting the voltage threshold of the silicon controlled rectifier (SCR) through its anode-cathode tension, which is adjusted by the gate via resistors R_1 and R_2. Once the voltage threshold is reached, the SCR switches to the on-state, and the capacitor discharges rapidly through the small R_3, producing a spike of current. The SCR remains in the on-state until the current decreases to the value of I_{hold}, which occurs when the capacitor is nearly fully discharged [37-40]. The observed process can be correlated with the relaxation or refractory period of the artificial neuron. In order to ensure that the spike can activate a downstream neuron, the strength of the signal must be enhanced. Therefore, we propose a design for an ultra-compact (UC) neuron that uses only one SCR and two transistors, in

addition to a "membrane" capacitor and several resistors. This construction has a minimal number of components. Specifically, we have assigned each of the three features of the LIF model to three respective devices: a resistor, a capacitor, and an SCR. These components enable the non-linear process of threshold spike generation in the "soma" of the artificial neuron. Change of membrane potential under limiting input pulse is given in the **Figure 4.12**.

Figure 4.13 illustrates the simulation outcomes of the VLSI circuit when subjected to different types of excitatory inputs, namely a train of synaptic transistor pulses.36 Consistent with a LIF neuron's behavior, increasing the pulse amplitude results in a decrease in the number of required pulses to trigger a response. The three curves (red, green, and blue) demonstrate that the circuit necessitates 10 pulses of 1 μA and 8 pulses of 1.25 μA to reach the threshold.

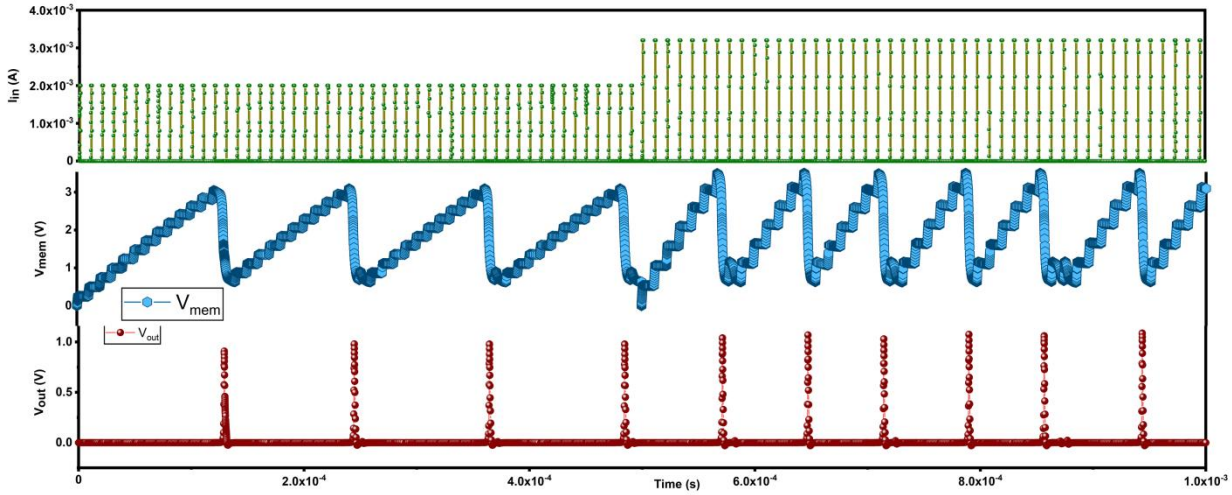

Figure 4.13 Operation of the VLSI circuit with input pulses of synaptic device (t_{on} = 100 ns, t_{rise} = t_{fall} = 1 ns, period = 2μs, I_{in} = 2.0 mA and 3.3 mA).

Section 4.2.4 SSVEP identification task is based on the modified SNN.

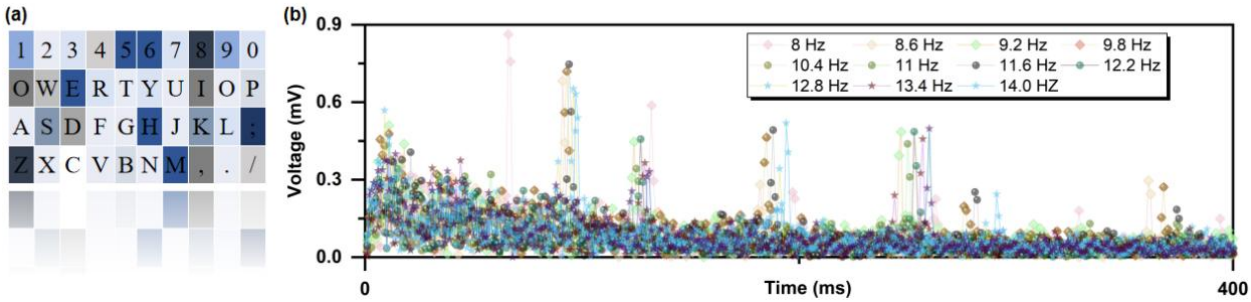

Figure 4.14 BCI data-set (a) SSVEP is a favored signal in brain-computer interface (BCI) systems due to its high information transfer rate (ITR). (b) Eight types of EEG waveforms from 40 different frequencies in the same channel.

SSVEP (steady-state visual evoked potential) is a type of brain activity that occurs in response to repetitive visual stimuli with a fixed frequency (**Figure 4.14a**). One of the main advantages of SSVEP-based brain-computer interface (BCI) is their high information transfer rate (ITR), which refers to the amount of information that can be transmitted per unit of time. In terms of data characteristics, SSVEP signals are typically characterized by a strong response at the stimulus frequency and its harmonics, which can be easily detected and separated from background EEG activity. SSVEP signals are also highly reproducible across trials and participants, which allows for reliable classification and decoding [32-40]. Further, SNNs are biologically inspired models that mimic the behavior of neurons in the brain, and have been shown to be particularly well-suited for processing spatio-temporal data such as EEG signals. **Figure 4.14b** directly demonstrates the 11 EEG curves within 400 ms under different stroboscopic stimuli (8 Hz- 14.0 Hz). Further analysis of different samples reveals that SSVEP, possesses the following advantages for neural computation: wide frequency selectivity range, high amplitude response, sensitivity to stimulus brightness and contrast factors, high stability across different experimental repetitions, and modulation by various

cognitive tasks. These above characteristics make SSVEP a valuable tool for applications in human-computer interaction, brain-machine interfaces, and biofeedback.

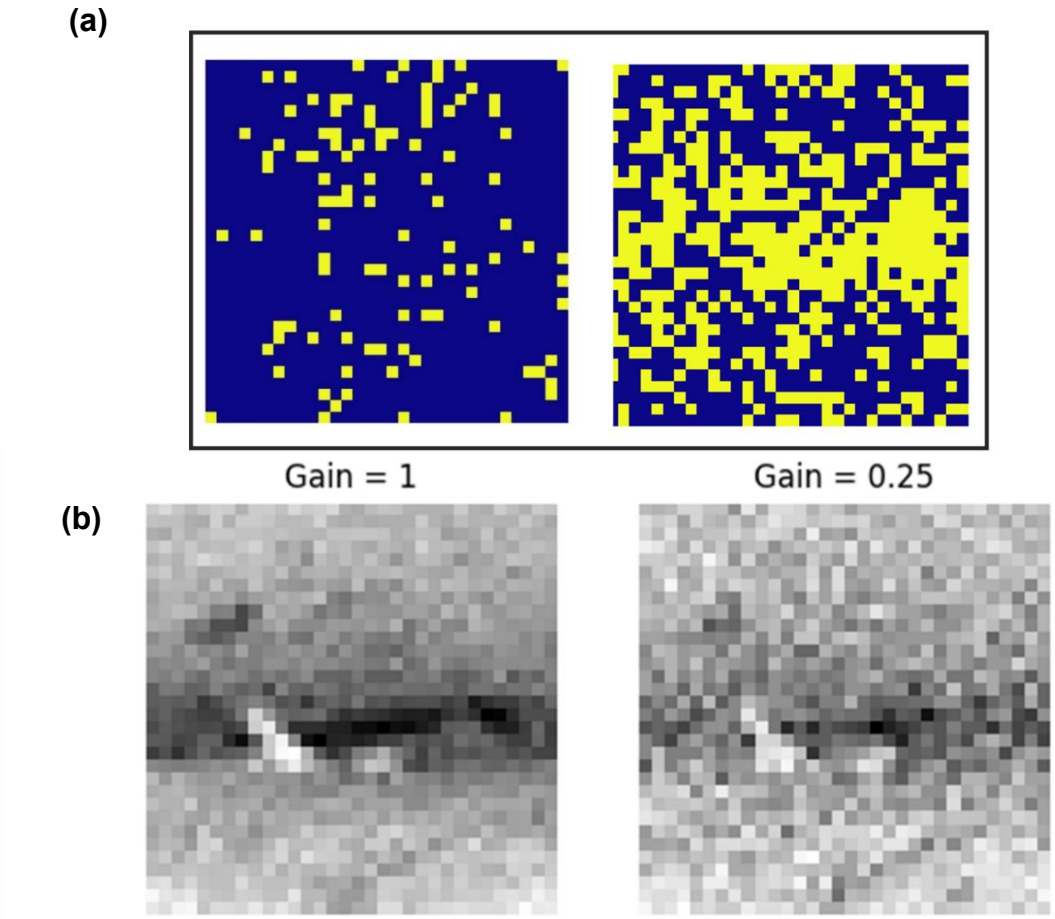

Figure 4.15 Process temporal information (a) SSVEP is processed into a visualized two-dimensional matrix through temporary coding.(b) The Temporal coding for SSVEP with different gain (0.25 and 1).

Besides, temporal coding is a neural coding scheme that encodes information through the precise timing and pattern of action potentials, or spikes, in individual neurons or groups of neurons (**Figure 4.15a**). SSVEP is processed into a visualized two-dimensional matrix through temporary coding. The temporal coding for SSVEP with different gain (0.25 and 1) and the distribution of neurons in the input layer combined with synaptic characteristics are analyzed in **Figure 4.15b**. Temporal coding plays a significant role in neural information processing and is thought to be particularly important for encoding information such as sound, visual stimuli, and motor commands. One adopted way is rate coding, where the frequency of

spikes within a given time window is used to convey information about the intensity or duration of a stimulus. Another improved method is phase coding, where the timing of spikes relative to a particular phase of a periodic stimulus is used to encode information. we conducted an experimental demonstration of the hardware-in-the-loop training using a prototype synaptic device-based simulation environment. This environment includes a tested array of ZIF-67 synaptic transistor with a conductance response. The purpose of our experiment was to verify the efficacy of our proposed training approach. The results of our study provide evidence of the successful implementation of our hardware-in-the-loop training method, which can be a promising approach for developing more efficient and effective neuromorphic computing systems.

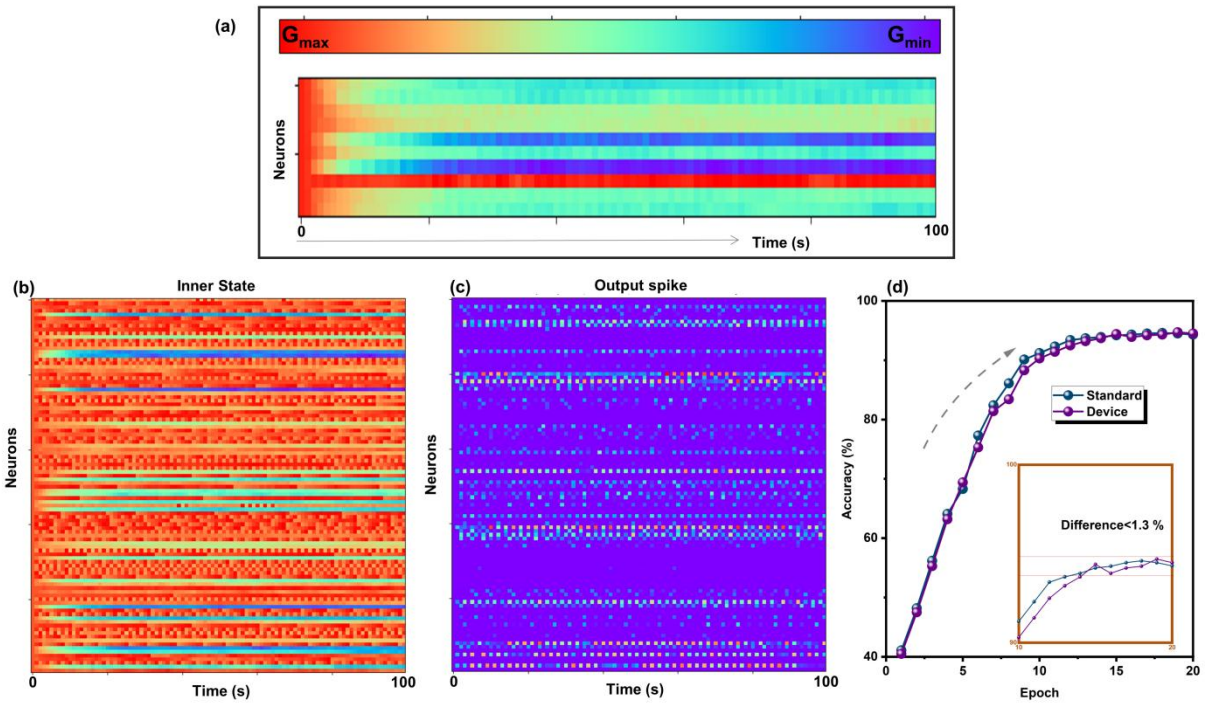

Figure 4.16 Weight changes in the different layers (a) Synaptic efficacy (Conductance of channel), defined as the strength of the communication between neurons, undergoes temporal modulation characterized by both facilitatory and inhibitory changes. (b) Inner state of neurons based on STDP in SNNs. (c) Output spike of neurons in SNNs. (d) Test accuracy of recognition task for SSVEP in improved network.

The conductances of the synaptic devices are iteratively adjusted during training by the framework through STDP update rules, with communication established between the LIF neurons (**Figure 4.16a**). The synaptic weights of the SNNs are implemented using a double differential configuration with two devices, where G^+ and G^- represent the synaptic weight in proportion to the difference of their conductances ($w=G^+-G^-$).

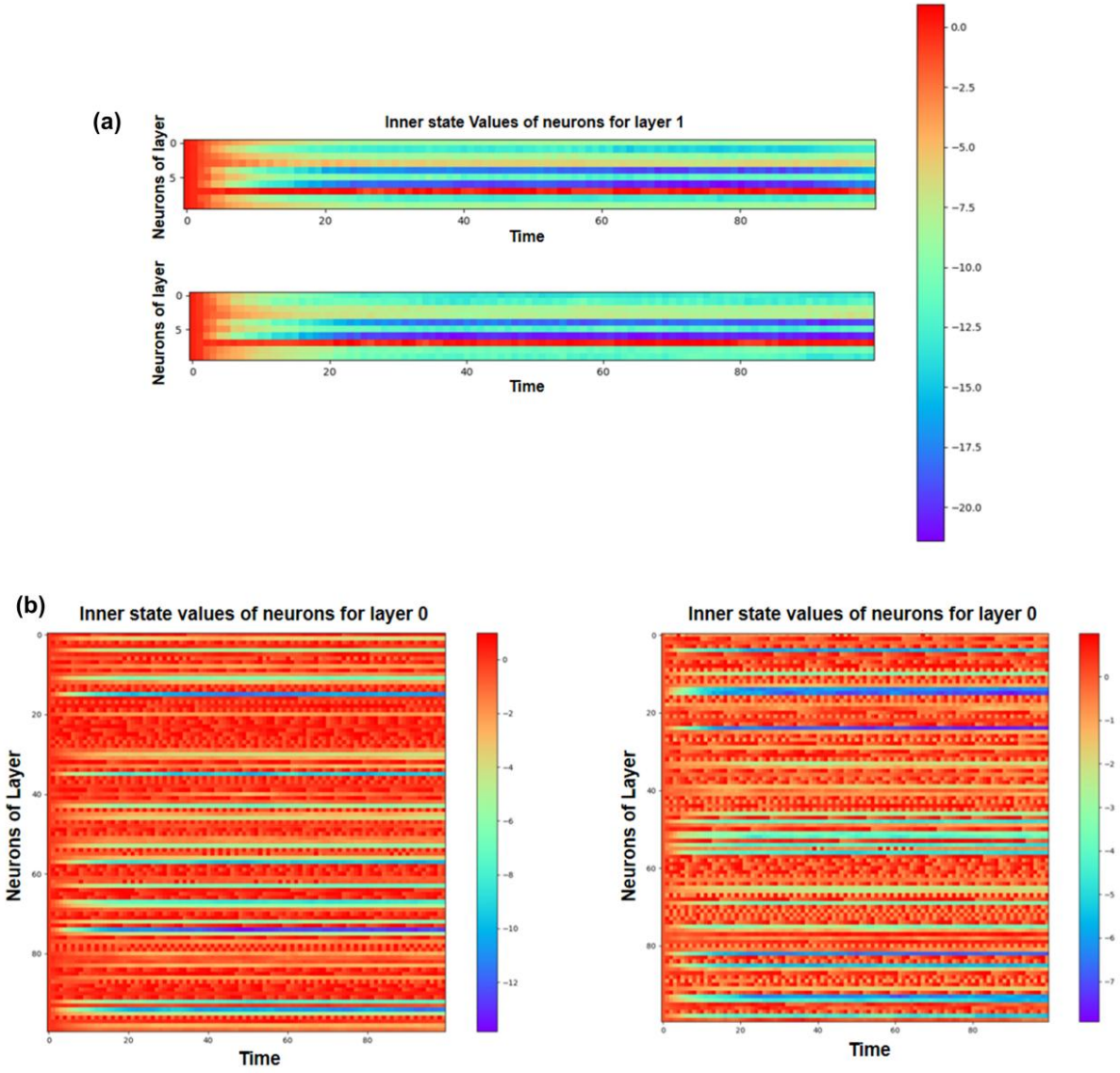

Figure 4.17 Inner state value for different neurons (a) Inner state value of neurons for layer 1 with different LTP/LTD. (b) Inner state value of neurons for layer 0 with different STDP.

To increase the weight w, the conductance of G^+ is increased, while to decrease the weight w, the conductance of G^- is increased. The conductance of the device increases gradually through ion migration in the ZrO_x layer by applying low-power pulses, which allows for gradual

weight updates (Δw) during training. The pre-processed sample is subsequently transmitted to the network, causing the input neurons to spike, as illustrated in **Figure 4.16b**. The resulting spike rasters for the output layer neurons during the speech recognition procedure are displayed in **Figure 4.16c**. Inner state value of neurons for layer 1 with different LTP/LTD and inner state value of neurons for layer 0 with different STDP are both demonstrate in the **Figure 4.17a** and **Figure 4.17b**. In order to evaluate the feasibility of the proposed network, it is reflected by comparing the difference between the recognition rate of the standard network and the enhanced network (**Figure 4.16d**). The ultimate arrangements of synapses proved to be effective and showed that the method can be utilized for creating an analog core that serves as a very efficient in-memory inference engine, without relying on the von Neumann architecture.

Section 4.3 Conclusion

The novel concepts put forward have opened up numerous opportunities for combining synaptic devices with neuron circuits to serve as the core components of SNNs. This improved SNN, based on the LIF model, offers advanced biologically-inspired neural models with low computational complexity and simplicity, enabling exploration of their capabilities from a deep learning perspective. Furthermore, the ZIF-67 SNN system provides a new framework for modeling and understanding neural dynamics, which can benefit from memory, synaptic plasticity, and membrane potential, from a neuroscientific perspective. The in-memory accelerators, combined with SNN-based STDP weight update rule, offer the potential for high adoption rates of spiking neural networks for SSVEP recognition applications (with a rate of 95.1%), and enable power-efficient neuromorphic hardware implementations from a neuromorphic computing perspective. Finally, the integration of multi-functional synaptic transistors into the improved SNNs expands the use of existing or forthcoming network accelerators for the entire SNN implementation and deployment.

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Chapter 5 Conclusion

The synaptic EGTs with transparent metal oxide as the dielectric layers and semiconductor layers possess the potential to obtain multi-level storage and cyclic update. The gate dielectrics manufactured by general mechanism are not considered to be adequate for the requirements of a large retention range for memory and learning due to the lack of large hysteresis observed from the transfer characteristics curve. Inspired by the biological nerve, ion doping can effectively solve this bottleneck which is also the mechanism of EGT. Compared with the bionic neural network produced by current CMOS process based on the von Neumann architecture, the synaptic devices have efficient parallel processing speed and low energy consumption for complex tasks. The EGT makes it possible to achieve synaptic plasticity, weight updating and bionic neural networks with small-scale and lower energy consumption per spike. The ions in the electrolyte layer of EGTs are regulated to migrate under the electric field effect and adjust the channel conductance. According to the migration extent of ions in the electrolyte layer, the working modes of adjusting the conductance could be divided into electrostatics modulation mode and electrochemical modulation mode. According to previous studies, the Li^+ ion has been proved to facilitate the formation of EDL easily belongs to electrostatics mode due to the small ion radius and high diffusion coefficient. In addition, Li^+ ion doping in the semiconductor could effectively reduce the oxygen vacancy, which significantly benefits the stability of the device. Compare with the organic materials and 2Dimensional material as the partial structure of synaptic transistors, the solution-processed metal oxide materials have the advantage of large-scale preparation, simple fabrication and stability in environmental change. However, recently, few studies have focused on the influence of Li^+ doping in the dielectric and semiconductor layers of EGTs for neural computation.

For the **Chapter 2**, solid state electrolyte gate transistor with Li^+ ions doping has been proposed for neuromorphic computing. The Li^+ ions doping into AlO_x (dielectric layer) to enhance the synaptic long-term plasticity and charge storage ability. Purpose of Li^+ doping into the InO_x (semiconductor) layer for improving the stability apparently due to the cyclic update (cycle-to-cycle error). The doping concentration in the AlO_x and InO_x layers have been well discussed systematically. The typical synaptic behaviors, including inhibitory/excitatory postsynaptic current IPSC/EPSC, LTP/LTD, STP, and PPF, have been successfully illuminated through the voltage spikes applied to the presynaptic terminal. It is worth noting that both the EPSC and IPSC are induced by the increase and decrease of channel conductance, respectively, which could be regarded as the change of synaptic weight. According to the G_{max}/G_{min} ratio and nonlinearity trend curves of LTP/LTD curve, the iterative update of synaptic weight matrix is demonstrated with the increase of epoch and the recognition accuracy of the bio-signal (ECG) can reach over the 94.8%. Moreover, the neural network can predict the abnormal beats of the cardiovascular due to extreme weight regions. We believe that this systematic research of Li^+ ion-doped solid state EGTs would pave the way for future neuromorphic computing networks.

For the **Chapter 3**, applying stimulation (electric pulse, optical pulse, or stress) to the pre-synaptic terminal simulates the realization of synaptic plasticity for the bionic nerve. The stability and controllability of the storage process has to be strengthened, despite the results of optoelectronic hybrid mode's significant in low power consumption. Moreover, the dimension of materials influences the transmission efficiency and data processing when the synaptic devices are integrated for parallel computing. A comprehensive modulation of mixed photoelectric pulses for LTD and LTP has been lacking in recent years. Furthermore, the influence of the fundamental symmetry and linearity of conductance in the rising and falling stages during the algorithm of error feedback is also not properly considered, and the weight

updating process is merely simulated in accordance with the fitted LTP/LTD curves. In previous research, the standard case (LTP/LTD) are two straight lines) generally adopted is that the learning step in each epoch is the fixed value. Afterward, inspired by the first impression of human cognition, the relationship between learning efficiency and temporal memory is nonlinear. In other words, a great of accurate information can be retained and learning is generally particularly efficient in the early stages. The ΔG between two synaptic transistors is normalized to represent the synaptic weight connection strength of two neural units due to the weight range in the neural algorithm containing the negative value.[7] Consequently, the convex function composed of LTP/LTD curves can provide a tight connection strength at the initial epoch of training, and the strength gradually decreases with the increase of the number of iterations. According to each non-fixed stage on the curve, the proposed dynamic learning rule provides the mapping relationship between the dynamic learning step and epochs. The one-to-one symmetry of conductance in the potentiation and depression stages, in addition to nonlinearity, provides assist dynamic response of neuromorphic computing. The iteration direction of synaptic weight is based on the Manhattan rule in the error backpropagation. Therefore, the updated trend of non-monotonicity requires strong symmetry of LTD/LTP. The strength of symmetry is then suggested to be measured by the ratio of $\Delta G_1 / \Delta G_2$. Previous research has shown that conventional neural networks (such as ANN and CNN) are unable to accomplish indistinguishable categorization tasks due to degradation presents both challenges on by the depth of network layers. The residual learning framework is proposed to simplify the training of networks that are substantially deeper than those previously used. The layer as the learning residual function is explicitly redefined by the reference layer, instead of the learning the unreferenced function. Besides, the differences between various tags are amplified as network layers increase, making it easier to distinguish between tags with a high level of similarity.

Further, the immunology c-ELISA image data format fully complies with the requirements of high similarity. As the most widely used technique in immunoassays, c-ELISA based on the microfluidic μPADs is the gold standard for detecting protein biomarkers in disease-related clinical samples and can be applied to detect diseases such as HIV, COVID-19, and Lyme disease etc. Then in recent years, μPADs of one kind of point-of-care (POC) diagnostics have received a lot of attention for their ability to perform real-time, rapid on-site testing in non-laboratory settings and provide accurate diagnostic results. Especially, the c-ELISA produces color signals that are correlated with the specific binding of the enzyme-labeled antibody to the sensing target molecule, with high color signals, representing high concentrations of sensing target molecules. These color signals can be easily picked up by the naked eye or by smartphones without the need for more sophisticated equipment. However, the differences in color signals displayed by different concentrations of sensing target molecules are not obvious, especially at low concentrations. Therefore, the ability to effectively distinguish color signal differences of sensing target molecules remains an urgent requirement to improve the performance of colorimetric μPADs analysis. Consequently, this problem can be well solved by using 2D (MXenes) synaptic transistor combined with dynamic learning strategies in residual neural networks.

In the **Chapter 3**, we for the first time report the deep residual learning strategy based on dynamic rules and Al/InO_x/MXenes/ZrO_x-Li/Si/Al structure. The nonlinearity and symmetry of LTP/LTD trends are successfully modulated by adopting the proposed three applied pulse modes (Type I (Electrical stimulation), Type II (Light stimulation), and Type III (Combined stimulation). Further, we constructed dataset by using a classic Rabbit IgG antigen as the c-ELISA sensing target at μPAD. The feasibility of combining a dynamic deep neural strategy with synaptic transistors is explored by analyzing image results of seven different concentrations of c-ELISA for Rabbit IgG. The combined stimulation can obviously improve

the standard accuracy (fixed learning rate) and shorten the update time in neuromorphic computing. The robustness of dynamic tracking rules under different training structures (ResNet and LSTM) and different classification tasks (ELISA, Cifar10, and Cifar100) are further analyzed to verify the advantages of combined stimulation. Finally, bionic retina combined with the dynamic neuromorphic residual deep learning strategy is successfully implemented by adopting the highly homologous database of immunology. This mainly depends on the high nonlinearity and symmetry after photoelectric hybrid control, which effectively shortens the number of neural network training epochs. Meanwhile, the high homology of c-ELISA also further highlights the advantages of residual deep learning, which well matches the synaptic plasticity of device to practical applications.

The low energy consumption and high-speed parallel operation of non-volatile neural devices are the competitive advantages compared with the separated chip. CIM has the same protocols and standards for storage and memory, which is the top research to eliminate boundaries. In recent years, RRAMs as memristors are integrated with microprocessors and peripheral circuits to realize the AI)functionalities of neural networks. The NeuRRAM-a chip is an advanced RRAM-based CIM chip that offers comparable inference accuracy to software models with four-bit weights for various AI tasks. It also boasts energy efficiency that is twice as good as previous state-of-the-art RRAM-CIM chips across different computational bit-precisions. Additionally, the NeuRRAM-a chip allows for flexible reconfiguration of CIM cores to accommodate diverse model architectures. From the perspective of energy consumption, three-terminal neural devices have more potential to approach the power of human brain (25W) in large-scale computing. However, due to the limitations and deficiencies of array fabrication technology for three-terminal neural devices, synaptic transistors as cross-bar weight combined with functional circuits are rarely explored to completely simulate the neural network. And a great quantity of research focuses on the

synaptic plasticity of a single device and the non-volatile regulation mechanism.[3,8] Consequently, the bionic performance of the synaptic transistor is utilized to expand the fusion circuit and match the high-performance network, which has a great contribution to accelerating the improvement of the system of brain-like computing.

For the **Chapter 4**, the essence of brain-like computing is learning from the information processing method or structure of biological neural systems and then developing the matching computer theory, chip architecture, and application models and algorithms. Brain-like computing is considered a significant research avenue in the post-Moore era, which has the potential to break through a technological bottleneck in future intelligent computing. At present, spiking neural networks, which closely replicate biological nervous systems, are a promising technology due to their low-overhead online learning and energy-efficient information encoding, stemming from their intrinsic local training principles. Thus, the comprehensively deepening innovation of SNNs must be explored in all related fields, including model algorithms, software, chip, and data. Several multiterminal synaptic devices, including floating-gate synaptic transistors (STs), ferroelectric-gate STs, electrolyte-gate STs, and optoelectronic STs, have been developed for producing synaptic plasticity. This plasticity is classified based on factors such as the retention time and the number of pulses. These devices effectively provide the ability to manipulate synaptic strength. Respectively, the working principles of the above STs, including the thermal emission or quantum tunneling, promote electrons into the floating gate, the interaction between the carriers in the channel and the polarization of the ferroelectric insulator is known as the coulomb interaction, electrostatic modulation and electrochemical doping and interfacial charge trapping through photogenerated electron pairs. Moreover, the functional layer, comprising a variety of materials (metal oxide, organic material, two-dimensional, quantum dot and perovskite), can

enhance or expand the synaptic properties of a system with regard to energy consumption, computing speed, and compatibility. However, up to now, the Al applications of MOFs in non-volatile neural devices have been rarely reported. MOFs are a type of crystalline porous material that are created by combining polytopic organic ligands with metal centers. These MOFs possess several advantageous characteristics, such as highly ordered pores, a substantial surface area, and a modifiable structure., which conveniently makes designing controlled and multifunctional biological spiking neural devices uncomplicated. Further, deeply introducing the core unit of SNN, SNNs commonly adopt LIF neurons as the fundamental building blocks for constructing neural networks. The LIF neuron model is a well-known type of neuron that offers a combination of the user-friendliness and simplicity of IF model, along with the capability to simulate various physiological properties of biological neurons, similar to the H-H neuron model. For synaptic devices, the LIF model is computationally efficient due to its simplicity, making it suitable for large-scale simulations. Then, the LIF model is biologically plausible and can simulate a wide range of physiological properties of biological neurons, such as action potential generation, synaptic integration, and adaptation. For the Al application, the LIF model is compatible with a range of learning rules (LTP/LTD and STDP) and can be used to train SNNs for various tasks, such as classification, pattern recognition, and control. Especially, the researches on constructing LIF neuron circuits and composing forward propagation process of SNNs with output signal from synaptic weight cross-bar are rarely reported. Therefore, the barrier from the extraction of single device characteristics to the building of an integral neural network system needs more resources to excavate. In terms of operation speed, the appropriate data type is conducive to improving the working efficiency of the neural network. In addition, the advantage of SNNs is to process complex temporal information which has obvious differences in the frequency domain. SSVEP is a neural reaction that occurs in response to visual stimuli. When the eyes receive

periodic flashes of light, the brain generates a stable electrical signal that oscillates at the same frequency as the stimulus. This response can be recorded via EEG and is typically observed as a periodic waveform at a specific frequency. SSVEP is widely used in the development of BCIs, which enable individuals to control external devices by monitoring their brain activity. For instance, in an SSVEP-based BCI system, users can select different commands or controllers by fixating on visual stimuli that flash at distinct frequencies on a computer screen. The system identifies the choice of the user by analyzing their EEG and executes the corresponding operation. SSVEP-based BCIs have diverse applications in fields such as virtual reality, game control, and medical diagnosis.

In the **Chapter 4**, we have proposed the new-type spiking neural network that utilizes ZIF-67 synaptic transistor, LIF neuron circuits, and SSVEP to achieve efficient and accurate neural computations. Forward propagation in our network relies on time sequence coding, accumulation of postsynaptic current, and the membrane potential threshold voltage of LIF neurons. Backpropagation in the proposed SNNs involves determining the iteration update rules and integrating the STDP curve to adjust the synaptic weights between neurons. The functional diversity of the prepared artificial neurons can be clearly observed through the results of STM/LTM, PPF, STDP, and LTP/LTD. More importantly, a LIF circuit capable of producing a matching array output has been simulated, allowing the SNNs to efficiently convert high-frequency information into sparse signals using the four blocks. Ultimately, the task of recognizing EEG signals was achieved using the modified SNN, with the final recognition rate stabilized at 95.2%.

In summary, At the beginning, we used basic metal oxide materials to make electrically controlled synaptic thin film transistors, explore the basic synaptic plasticity and apply it to identify electrical signals in combination with ANN. Furthermore, in order to control the linearity and symmetry of the weight change process, we add Mxenes to make the ions

orderly during migration. Then it deeply combines the characteristics of conductivity changes under electrical and light stimuli, proposes dynamic learning rules and applies them to immunological recognition. Finally, based on the previous two parts of the research, we further explore neural devices based on MOF materials, which have particularly high frequency screening characteristics. This feature can perfectly integrate SNN and embed its three biological functions into the third generation neural network, thereby achieving filtering and recognition of high-frequency information.

Section 5.1 Future work

For many years, despite the rapid development of computer technology, scientists still struggle to build efficient and exquisite brain biomimetic computers. Although we have constructed several artificial synapses, these synapses have improved the efficiency of computer simulation of the human brain and effectively promoted the development of this field. But the human brain is an extremely complex structure. To process complex parallel events with power close to the human brain, it is first necessary to conduct in-depth exploration of brain science. And find suitable hardware to replace and imitate. Just exploring plasticity has already invested a lot of effort and funds. Therefore, the next step is to delve deeper into the connection between brain science and materials and devices.

On the other hand, parallel computing requires a large number of neural nodes, so the scale of neural devices is also one of the factors determining the development of brain like computing. The next step is to build on the previous work and further reduce the size of synaptic devices to achieve large-scale manufacturing. Due to its excellent characteristics such as high integration density, fast read and write, low power consumption, and perfect compatibility with CMOS technology. However, the special application of "integration of memory and computing" puts forward higher requirements for the device characteristics of memristor. The existing device characteristics such as linearity, durability and discreteness are still not ideal. Therefore, it is necessary to explore ways to improve the device performance, increase the effective number of bits available for calculation, improve the accuracy of different resistance state regulation, shorten the pulse time required for conductance regulation, and suppress the conductance drift effect, reduce device fluctuations and fluctuations.