Ultra-Fast Langmuir Probe Diagnostic for Magnetised Plasma

by

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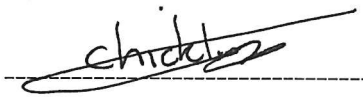
Declaration

I hereby declare that this thesis is my own work and no further sources of information have been used other than the references cited. Neither this thesis nor any part of it have been submitted to any other university or institution for the application of another degree or qualification.

Signed:  (Christopher Hickling)

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Abstract

In order to better understand the processes behind nuclear fusion, high precision and reliable diagnostics are required. Traditionally, analogue diagnostics have been used, mostly due to cost and availability. Analogue electronics take up a large volume and often have to be completely redesigned when moving to different systems or making changes to their function. In recent decades, huge advancements in digital technology has made the use of digital systems more affordable and more robust. The Field Programmable Gate Array (FPGA) can provide a low-cost and modular solution to the analogue problem.

This thesis will describe the designing, implementation and testing of a new diagnostic for future installation onto Mega Amp Spherical Tokamak - Upgrade (MAST-U), the Ultra Fast Langmuir Probe (UFLP). The UFLP aims to solve the Langmuir equation in real time utilising only a single Langmuir probe configuration to return the electron temperature, ion saturation current and plasma floating potential. It achieves this via fast biasing and dynamic adjustment of the bias range to ensure samples are taken within the transition region. The design of such a system both in terms of FPGA design and electrical hardware will be described. To ensure properly functionality, real-world testing results in low temperature magnetron systems will be presented.

Conferences

The work contained in this thesis has been presented at various conferences listed below.

- *C. J. Hickling*, *S. Hall*, *R. Seath*, *J. R. Harrison*, *R. Sharples*, *J. W. Bradley.* **First results of the Ultra-Fast Biasing Langmuir Probe in a pulsed low temperature magnetron plasma**, Proceedings 48th European Conference on Plasma Physics (2022).

- *C. J. Hickling*, *S. Hall*, *R. Seath*, *J. R. Harrison*, *R. Sharples*, *J. W. Bradley.* **Ultra-Fast Langmuir Probe in Magnetised Plasma**, 48th European Conference on Plasma Physics (2022) Online. [Oral]

- *C. J. Hickling*, *S. Hall*, *R. Seath*, *J. R. Harrison*, *R. Sharples*, *J. W. Bradley.* **Ultra-Fast Langmuir Probe in Magnetised Plasma**, High Temperature Plasma Diagnostics, 2022, Rochester, NY. [Poster]

- *C. J. Hickling*, *S. Hall*, *R. Seath*, *J. R. Harrison*, *R. Sharples*, *J. W. Bradley.* **Ultra-Fast Langmuir Probe in Magnetised Plasma**, 49th International Conference on Plasma Science, 2022, Seattle, Wa. [Poster]

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It is no secret that I did not have an extensive knowledge of electronics when I started this project. Robert Seath and Mark Burnley have been invaluable in helping me learn and understand the electronics that were needed to achieve this project. Thank you both.

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Acronyms

ADC Analogue to Digital Converter

ASIC Application Specific Integrated Circuit

CLB Configurable Logic Block

CPU Central Processing Unit

DAC Digital to Analogue Converter

DIONISOS Dynamics of ION Implantation and Sputtering Of Surfaces

FPGA Field Programmable Gate Array

FSM Finite State Machine

HDL hardware description language

HiPIMS High Power Impulse Magnetron Sputtering

IOB Input/Output/Buffer

IP Intellectual Property

ITER International Thermonuclear Experimental Reactor

LED Light Emitting Diode

LTP Low Temperature Plasma

LUT Look-up Table

MAST Mega Amp Spherical Tokamak

MAST-U Mega Amp Spherical Tokamak - Upgrade

MIT Massachusetts Institute of Technology

MLP Mirror Langmuir Probe

ROM Read-Only Memory

SDK Software Development Kit

SoC System on Chip

SOL scrape off layer

UFLP Ultra Fast Langmuir Probe

VHDL (VHSIC-HDL) Very High Speed Integrated Circuit Hardware Description Language

Chapter 1

Review of Background

Worldwide, the demand for energy is increasing [1]. As the population of any country grows or develops, so does it's energy needs. Historically, developing nations would burn fossil fuels to meet their energy production [2]. With the added challenge of the climate crisis, this will have to not be the case in the future so as to not exacerbate the problem. Given that nuclear fusion is not yet an established technique, nuclear fission is one of the better options to meet bulk energy demand paired with renewable sources [3], although long lived radioactive waste and safe energy generation continues to be an issue [4]. The development of nuclear fusion as an energy source could help to phase out conventional nuclear fission power to address both climate goals and radioactivity reduction.

1.1 Introduction to Nuclear Fusion

1.1.1 Physical Process

In 1920 Arthur Eddington first proposed that the stars, including the sun, were not celestial balls of gas aflame; but instead powered by the nuclear fusion of hydrogen atoms [5].

Nuclear fusion is the process by which two small nuclei (up to the atomic mass of iron) can fuse together. It is difficult to achieve as the nucleus of the atom is positively

charged. The presence of this charge causes other positively charged atoms to feel an electrostatic repulsion force governed by Coulombs law:

$$F = k_b \frac{q_1 q_2}{r^2} \tag{1.1.1}$$

where k_b is the Boltzmann constant, $q_{1,2}$ are the charges on particles 1 and 2 respectively and r is the distance between the two particles. As seen in Equation 1.1.1 the force felt between two same charge particles is inversely proportional to the distance between them, squared. Hence, the amount of repulsion such particles will exert upon each other increases exponentially as they get closer. To overcome this Coulomb barrier via kinetic energy alone, two hydrogen atoms would require to each to contain 0.25 MeV of energy. This translates to an average gas temperature of around 1.9 Billion degrees kelvin - around 70 times hotter than the centre of the sun. Fusion is instead facilitated by the presence of quantum tunnelling. If a particle has sufficient energy and the distance to a neighbouring particle is sufficiently close, there is a probability for that particle to tunnel across any potential barriers that may be separating them.

The total mass of the alpha particle (helium nucleus) is less than that of its constituent parts, 2 protons and 2 neutrons. This was found in 1920 by F. W. Aston [6] and named the “mass deficit” or “binding energy”, and for stable nuclei it is always positive.

$$E = mc^2 \tag{1.1.2}$$

Already established at the time, Einstein’s famous equation [7], shown in Equation 1.1.2, explains that mass and energy are interchangeable. For two atoms to fuse together and have a lesser total mass, energy must be released.

$$\Delta E = \Delta m c^2 \tag{1.1.3}$$

For hydrogen nuclei , each with mass $1.00727647u$ and an alpha particle with mass $4.002603254u$ where $u = 1.660\,54 \times 10^{-27}$ kg

$$\Delta E = (4 \cdot 1.00727647u - 4.002603254u) \cdot 3 \times 10^{8^2} = 3.96 \times 10^{-12}\, J = 24.7\, MeV \tag{1.1.4}$$

Equation 1.1.4 proves that by combining 4 hydrogen atoms into a helium atom there will be a large release of energy due to the product having less mass than the constituent parts.

As shown in Figure 1.1, lighter elements have more binding energy per nucleon than heavier elements. This means that, for example, combining two Hydrogen[1] atoms together will result in a Hydrogen[2] atom, plus an amount of energy that is released.

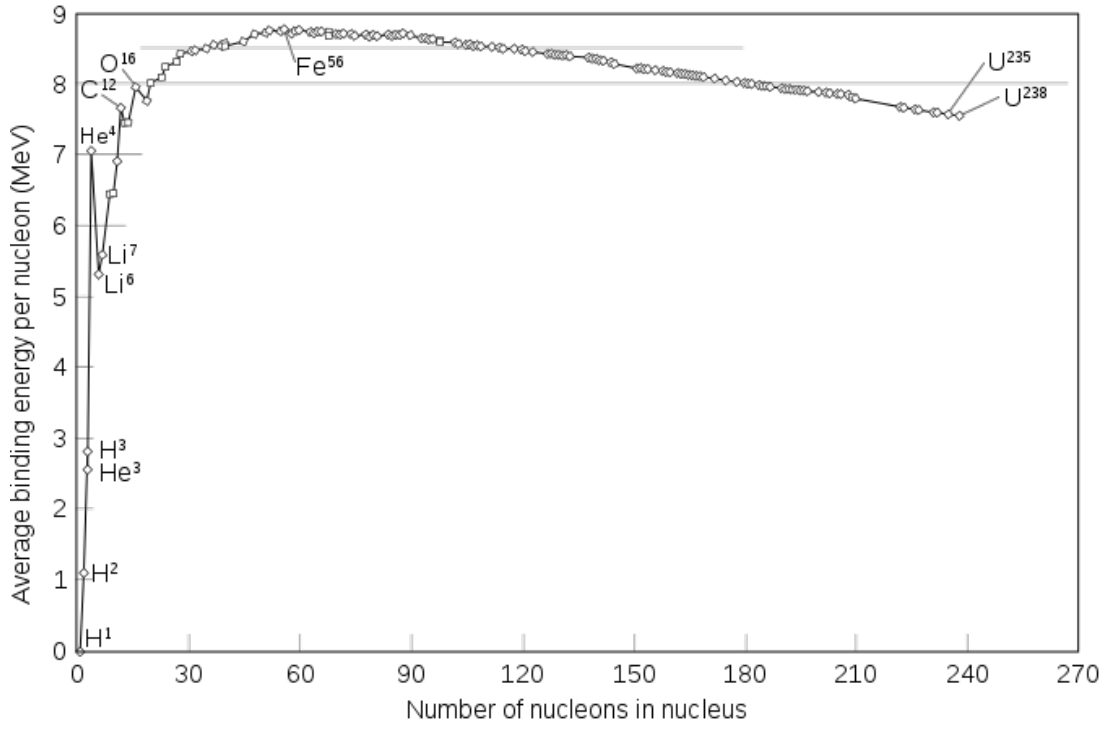


Figure 1.1: The average binding energy of nucleons against the number of nucleons. This shows that a transition from one light element to another results in a large energy deficit, this is released as energy in a fusion reaction [8].

Equation 1.1.5 is known as a "hydrogen-hydrogen" or H-H reaction. The combination of two atoms with increasing mass continues up to iron, but with exponentially decreasing energy released. Iron is the heaviest element that can be achieved via fusion while still having a positive net energy output.

$$ {}^{1}H + {}^{1}H \rightarrow {}^{2}_{1}H + {}^{1}_{0}e + \nu^{-} + 0.42\,MeV \tag{1.1.5} $$

In order to have a functional and efficient nuclear fusion reactor, the energy output must be greater than the energy input. It has already been explained that the energy requirement of inducing fusion reactions is large and the probability of a reaction occurring is small. Figure 1.2 shows some of these probabilities of a reaction occurring as a function of particle energy. It shows that the deuterium-tritium (D-T) reaction has

both the highest probability of occurring and also the lowest energy required to reach this probability.

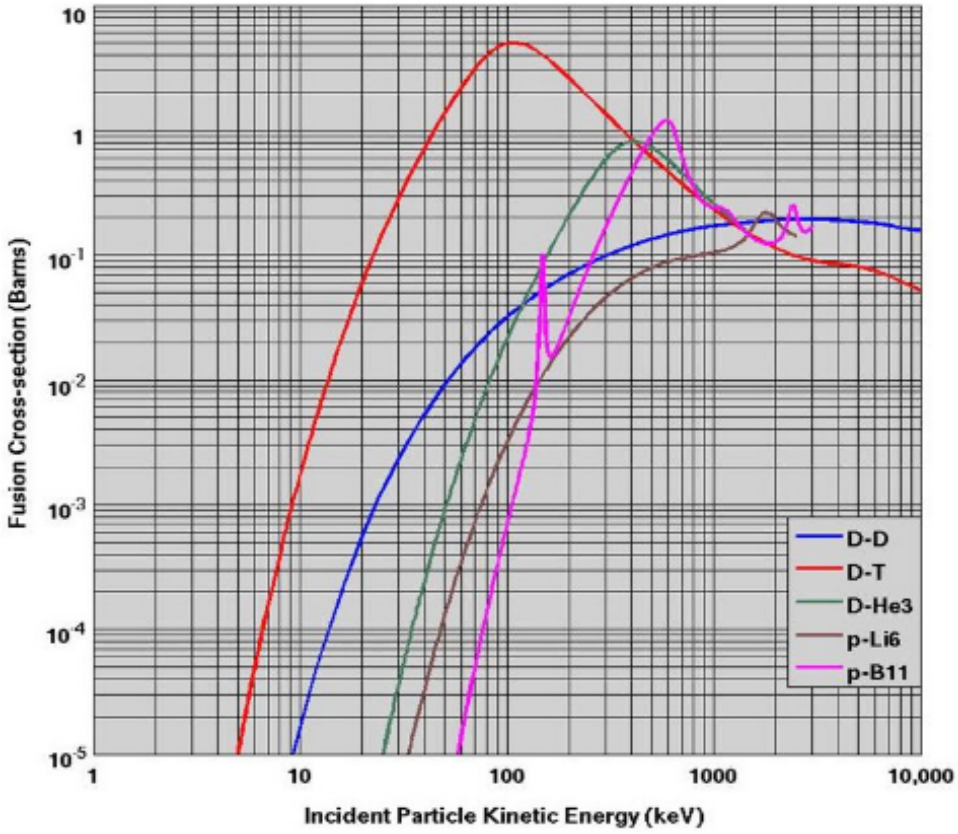


Figure 1.2: Fusion cross-sections of various fusion reactions as a function of kinetic energy of an incident D or p on a stationary target. The data for the D-D, D-T, D-He 3 and p-6Li curves are taken from the ENDF B-VII database [9] for incident deuterium/proton, while that for p-11 B is taken from W Nevins, 2000 [10]. The curve for D-D represents a sum over the cross-sections of the reaction branches. Figure from [11, p. 22]

In order to have a self sustaining fusion reaction, termed as 'ignition', a high density, high temperature plasma must be confined for an adequate length of time. This can be described by the Lawson criterion inequality as shown by the following equation.

$$n_i T_i \tau_E > 5 \times 10^{21}\, m^{-3}\, keV\, s \tag{1.1.6}$$

The product of these 3 parameters is known as the fusion triple product, $n_i T_i \tau_E$. Where n_i and T_i are the ion density and ion temperature of the plasma and τ_E is the energy confinement time. τ_E is described as the timescale that energy is lost from the plasma. From this triple product comes the Lawson ignition criterion. The Lawson ignition cri-

terion [12], an inequality described by Equation 1.1.6 for a D-T reaction and shown in Figure 1.3, defines that if the inequality is met then the plasma will be self sustaining. It is also noted that from Figure 1.3, the triple product required varies depending on which particles are to be fused.

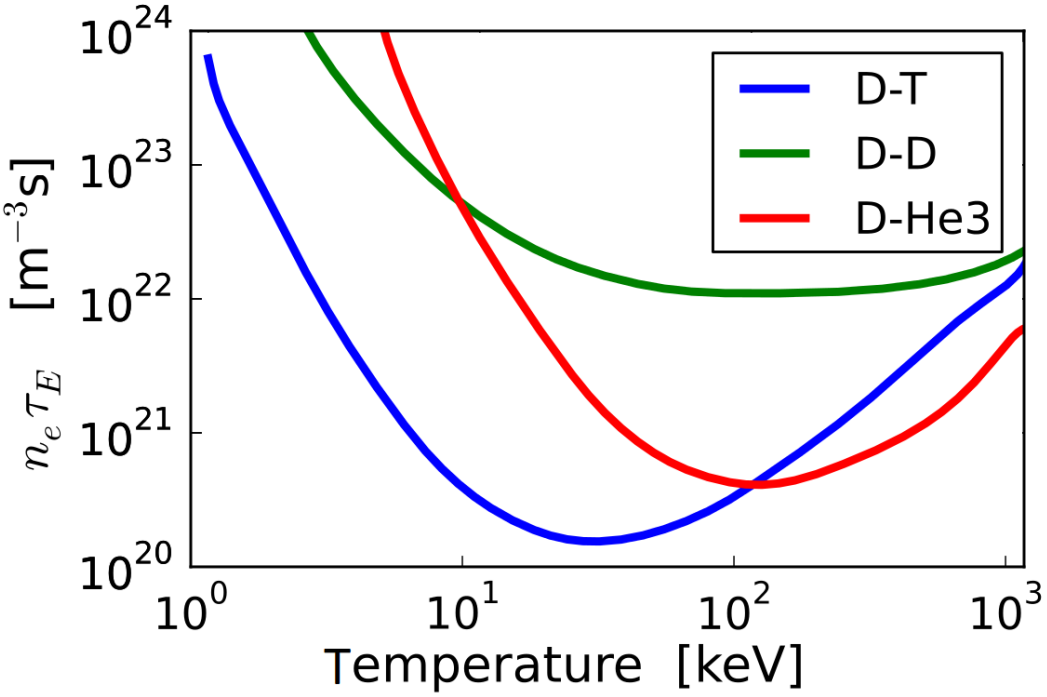


Figure 1.3: The self-heating condition on (electron density $\times$ energy confinement time) for three nuclear fusion reactions. A plasma must exceed the plotted curves for fusion self-heating to overcome energy loss. The 3 curves labelled D-T, D-D and D-He3 represent Deuterium-Tritium, Deuterium-Deuterium and Deuterium-Helium^3. [Adapted from [13]]

The largest amount of energy from a single reaction can be achieved by fusing two atoms and gaining the largest mass deficit possible. The largest of these being a Deuterium-Tritium (D-T) reaction [14, p. 430]:

$$ {}^{2}_{1}H + {}^{3}_{1}H \rightarrow {}^{4}_{2}He + {}^{1}_{0}n + 17.6\,MeV \tag{1.1.7} $$

In this reaction described in Equation 1.1.7, the energy is divided between the neutron and alpha particle (helium ion) by mass. This results in the neutron receiving 80% of the energy due to conservation of momentum. With the alpha particle receiving the remaining 20% of the energy. The D-T reaction also has a higher probability of the

reaction occurring than than both H-H and D-D fusion, shown in Figure 1.2. This was also shown in a paper by Lawson [15] to be an inequality to represent the combination between temperature and reaction time. Very few reactors worldwide have capability of achieving a D-T reaction due to the radioactivity of tritium and issues with tritium retention within the reactor walls. Those that have, namely JET [16, 17] and DIII-D [18], have suffered damage from the high energy particles released.

1.1.2 The Tokamak

The first data obtained from a tokamak was published in 1969 by Sakharov and Tamm [19]. The team managed to produce plasmas of a much higher stability than previously seen, at temperatures up to 10 times higher than previously achieved. Since then, tokamak development has been progressing at a steady pace while encountering a large number of challenges in the fields of engineering, materials research and plasma physics [20].

As shown in Figure 1.4, a tokamak uses toroidal and poloidal magnets to generate a helical magnetic field. This is a path for charges particles to travel on. The inner poloidal field coils (sometimes referred to as the central solenoid) acts as the primary winding on a transformer.

The free electrons present in the gas are accelerated and collide with neutral atoms forming free ions and electrons, a process known as breakdown [21]. These new particles cause a chain reaction of further collisions in a process known as the avalanche. The fast moving sea of ions and electrons is now defined as a plasma and forms the secondary winding of the transformer to inject further energy. This rotating mass of moving charge generates its own electric and magnetic field which causes the plasma to twist into a helix shape, pulling the plasma away from the edges of the device and improving confinement [22].

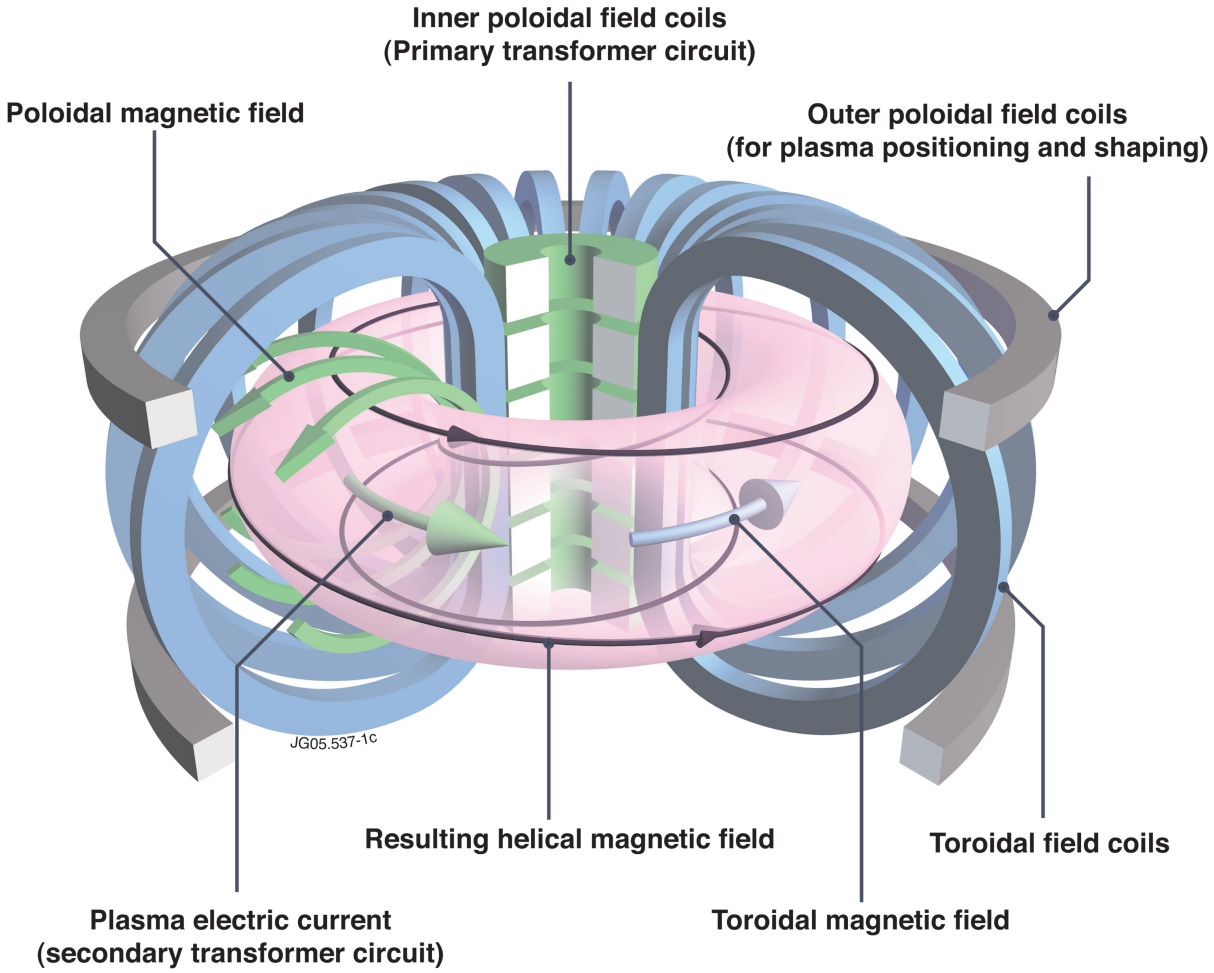


Figure 1.4: A schematic generalised tokamak showing key features to its operation and function [23].

The longer that a fusion plasma can be confined (under fusion conditions), the more probability of fusion reactions taking place. There are two main ways to increase confinement time; an increase of radius of a reactor or an increase in magnetic pressure [24]. Magnetic strength can be increased via the use of superconducting magnets, which will need to be developed to build an efficient fusion reactor [25, 26]. The International Thermonuclear Experimental Reactor (ITER) [27] is the next step to both an increase radius and magnetic pressure.

Mega Amp Spherical Tokamak (MAST)

For the purposes of analysing plasma phenomena and performing research, MAST is well suited due to its large amount diagnostics [28]. MAST has recently completed its upgrade

into MAST-U, where it has many improved features including a new divertor configuration that allows for more complex plasma scenarios and longer path length. This allows the plasma to slow down (and cool down) before striking the divertor plate as shown in Figure 1.5 [29]. This also gives an opportunity for the study of detachment [30]; the process of injecting a neutral gas into the divertor region to further cool down the plasma to prevent serious damage to the target plates.

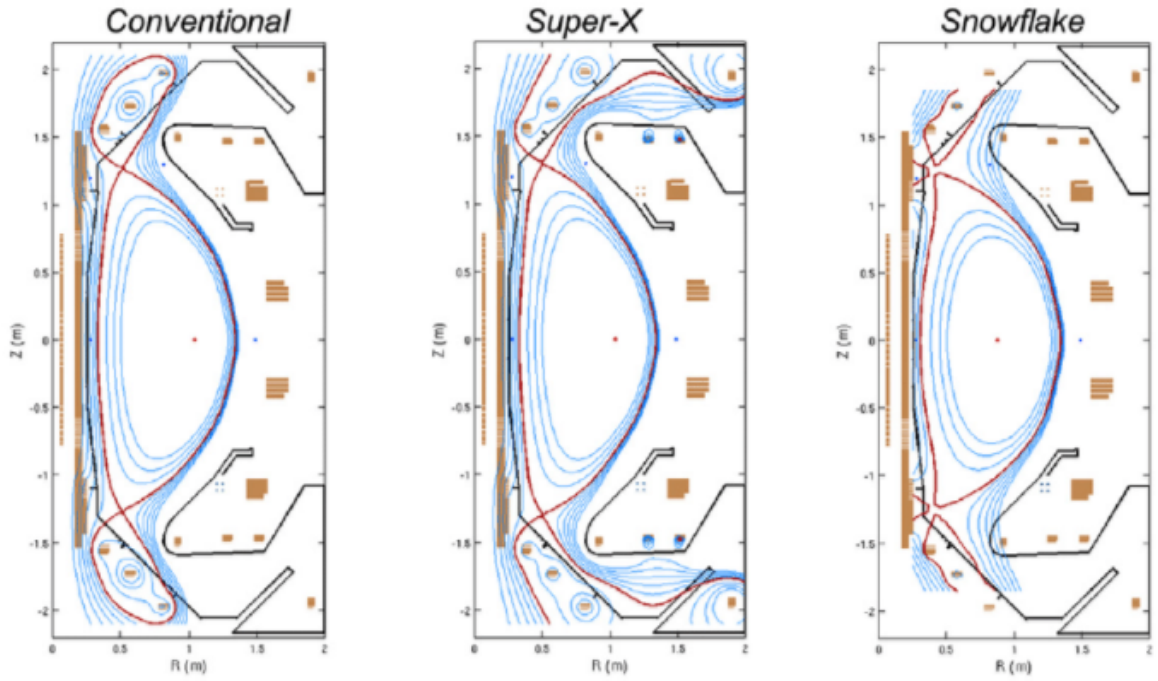


Figure 1.5: MAST-U divertor regions derived by free vacuum boundary calculations. Shows 3 possible new configurations of the magnetic field and ion path passing through the divertor [31].

MAST-U

MAST-U is a low aspect ratio device (R/a = 0.85/0.65 $\approx$ 1.3, Ip = 2 MA, Bθ(R=0.7) = 0.92 T) with a high pulse length of 5s [32]. It has also included the installation of 17 new poloidal field coils which grants a large increase in plasma control. Its main benefit to the field is the contribution of the Super-X divertor [31], which is used to elongate the outermost flux surface far away from the core plasma.

MAST-U has also had a number of control and safety upgrades including the plasma control system [33] and the real time protection system [34], both of which are

driven by FPGA's. The plasma control system gives the operator the ability to control the vertical and horizontal position of the plasma. The real time protection system is designed to take real-time data from diagnostics and provide a signal to the power supplies to perform a safe shutdown if the current state of operation could cause damage to the reactor.

1.1.3 Operating Modes

MAST-U has the ability to control its plasma temperature, density and position through the use of neutral beam injection, startup current and adjusting the power to the poloidal magnets. For a fusion device for energy production, plasma has to be well confined away from the walls to prevent any losses or damage [35]. The two main modes of consideration are High-Confinement Mode (H-Mode) and Low-Confinement Mode (L-Mode). The density profiles of each can be seen in Figure 1.6.

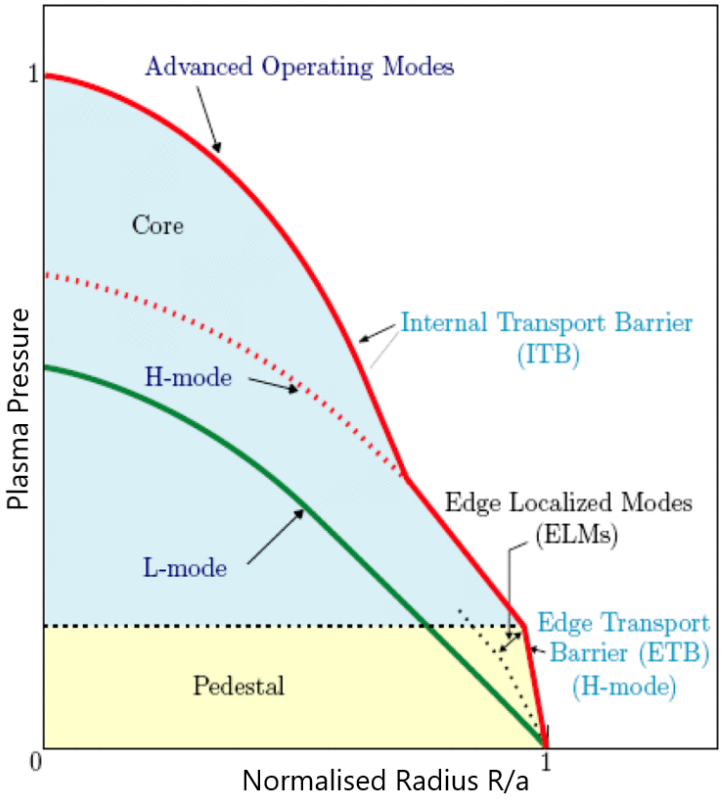


Figure 1.6: Graph highlighting the difference between H-Mode and L-Mode and the disruptions that exist in both. Modified from [36].

H-Mode, as shown in Figure 1.6, is a mode that is enabled by achieving a high density and temperature in the core plasma. This enables a transport barrier to form in the outer edge of the plasma. This transport barrier prevents particles from moving towards the wall, increasing the core density and electron temperature and causing a steep gradient in plasma pressure near the edge. This effect is creates a region known as the pedestal.

1.1.4 Scrape of Layer Turbulence and Filaments

Turbulence is a prevalent form of plasma transport that exists in both MAST-U [28, 37, 38] and Low Temperature Devices at the University of Liverpool [39, 40]. In tokamaks, plasma turbulence gives rise to edge perturbations in the plasma, which has been referred to in literature as filaments [41].

Filaments, sometimes known as "blobs" in literature, can be defined as areas of increased density compared to that of the root-mean-square (R.M.S) background. Filaments are also generally elongated in the direction of the magnetic field and have very small diameters perpendicular to it. Filaments are found in all forms of plasma confinement devices [42]. The filament becomes polarised and an electric field is generated due to the charge imbalance. This electric field induces an $E \times B$ drift that moves the filaments towards the walls of the confinement device. The existence of these filaments in the scrape off layer (SOL) causes much larger particle fluxes towards the wall than previously expected. This can cause an increase in the tritium retention rate [43, 44] due to the increase particle density close to the vessel wall. Propagation of heating methods or diagnostics through the SOL could be disrupted due to filaments possessing different plasma properties to that of the background plasma. Filaments can be seen with fast cameras in tokamaks, as seen in Figure 1.7. In the scope of this thesis, we will also consider "spokes" in low temperature devices, which are fast moving structures of around 1 km/s radial velocity [37]. While these low temperature structures do not move radially to the wall as filaments do, they also exhibit a density profile higher than that of the background and rotate at comparable speeds. This makes them a prime test bench for testing diagnostics for the diagnosis of filaments in tokamaks.

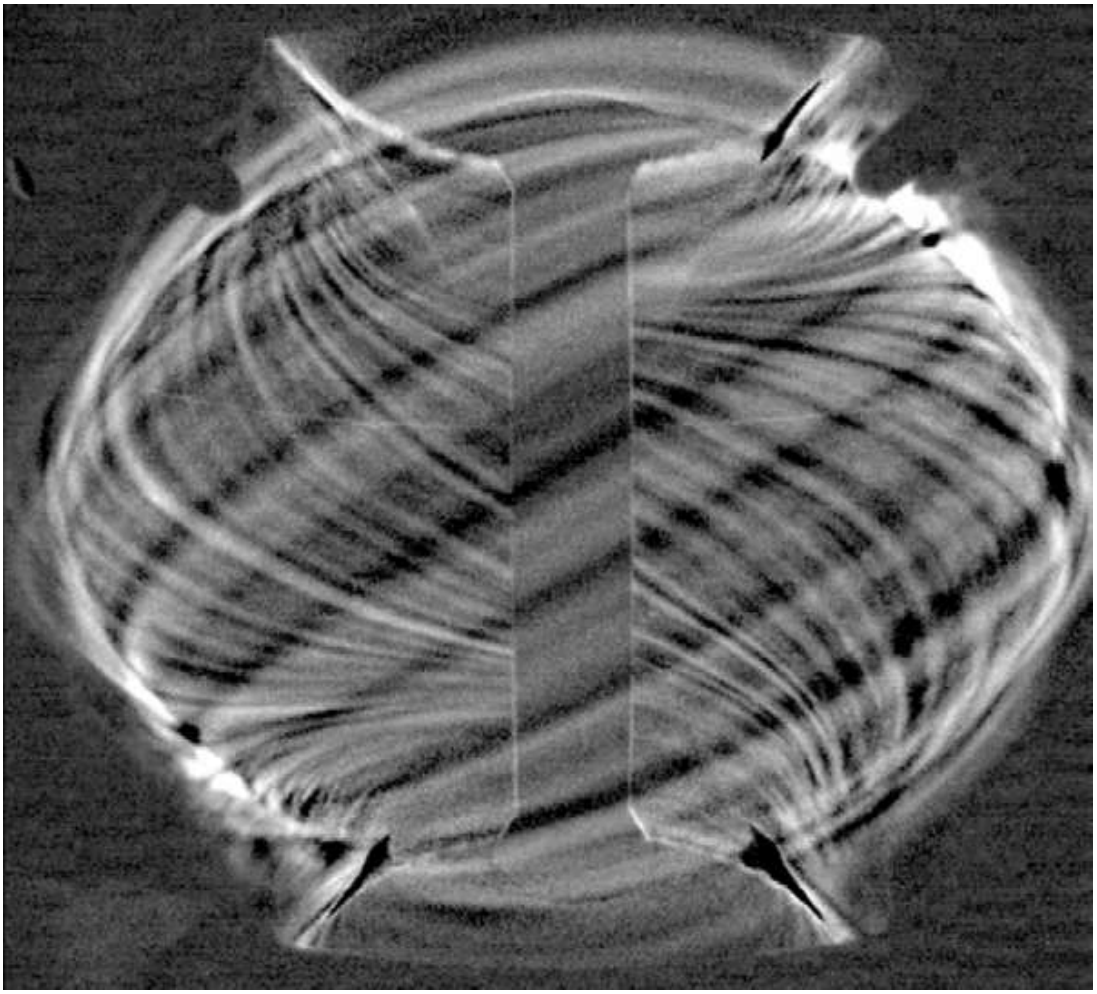


Figure 1.7: Visible light image of filaments in ohmic L-mode on MAST. The fast varying component of light has been digitally enhanced. [45]

1.2 Low Temperature, Low Pressure Plasma's

Low temperature plasma's (LTP) are generally only a few electron volts up to 10 eV in temperature and have a low ionisation degree [46]. If a plasma is also low pressure then it also generally is not very collisional, which generally results in higher electron temperature than ion temperatures, $T_e > T_i$. LTPs have a wide range of applications from manufacture of silicon wafers to biomedical applications [46, 47]. LTPs also have a large range of discharges that can be accessed at different electrical supply currents as can be seen in Figure 1.8. For the purposes of explanation in this thesis, plasmas generated at the university of Liverpool will be considered in the "abnormal glow" region of Glow

Discharges, while tokamak plasmas will be beyond the Arc Discharge region.

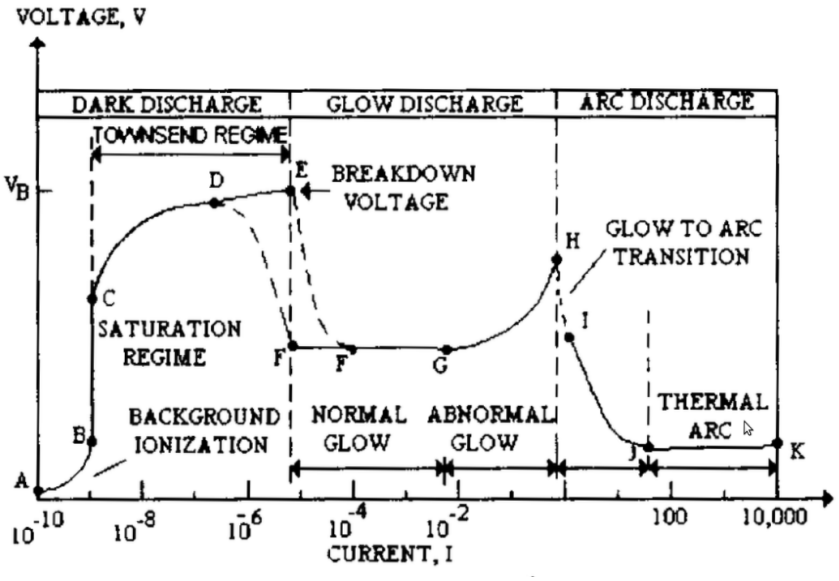


Figure 1.8: The different plasma discharges and their associative currents in a low-pressure electrical discharge tube. Figure from [48]

A simple low temperature plasma system can be made through the method of applying direct current to a pair of parallel plates immersed in a low pressure gas as seen in Figure 1.9. The charging of the plates generates a strong electric field between them which accelerates any free electrons in the gas or on the surface of the plates. These electrons collide with atoms either causing excitation or ionisation. Ionisation results in further events as the newly free electrons are accelerated by the field; in an effect known as the Townsend Avalanche [49].

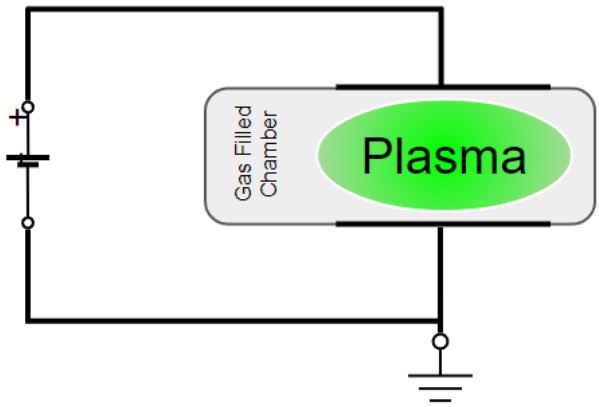


Figure 1.9: A power source being used to generate a simple glow discharge plasma via parallel plate discharge in a gas filled chamber

1.2.1 Planar Magnetron Sputtering Source

Since an electric field has now been established to generate a plasma via the acceleration of electrons, the ions are now accelerated towards the cathode. The addition of a magnetic field emanating from the target plate, as illustrated in Figure 1.10, generates an $E \times B$ drift which traps the electrons in a ring parallel to the target plate.

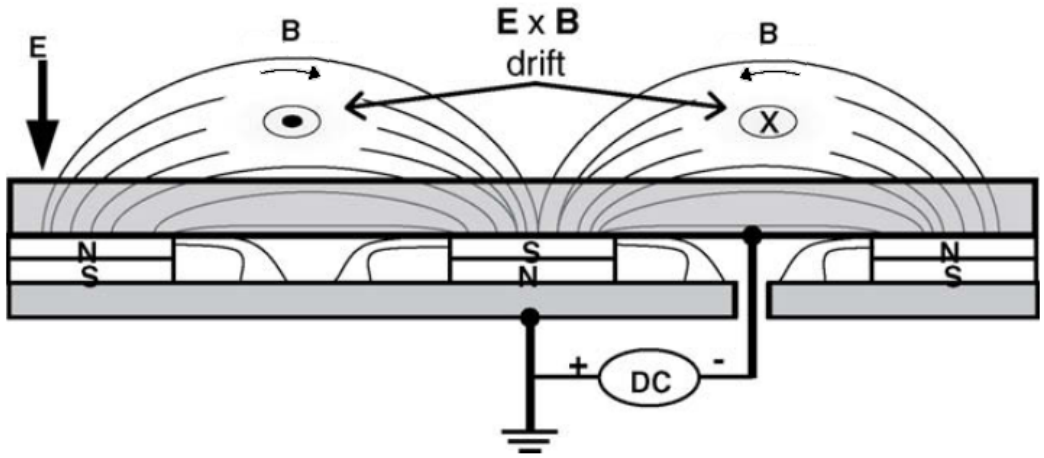


Figure 1.10: A planar magnetron sputtering source illustrating the position of the magnets and existence of the $E \times B$ drift that leads to the confinement of electrons [From [50]]

The confinement of these electrons leads to large ionisation rates which results in higher current densities, typically to the order of 100 $mAcm^{-3}$. Electrons can only escape this confinement through plasma oscillations (transport) or via collisional processes. The positive gas ions produced, bombard the target that causes a liberation of groups of atoms; a process known as "sputtering". Sputtering generally occurs when the collision atoms have energies of the order of 10 eV [51]. In order to maximise efficiency often an inert gas is used, such as argon, Ar. This is so the sputtering gas does not chemically interact with the target or the substrate. More efficient sputtering is achieved when the sputtering gas is close to the atomic mass of the sputtering target. The liberated atoms eventually reach the substrate, depositing a thin layer of the target atoms on the substrate; a process known as "physical vapour deposition"[52]. This is the main use of magnetron glow discharges to generate thin films, which are of interest for a variety of research and development fields [53–55].

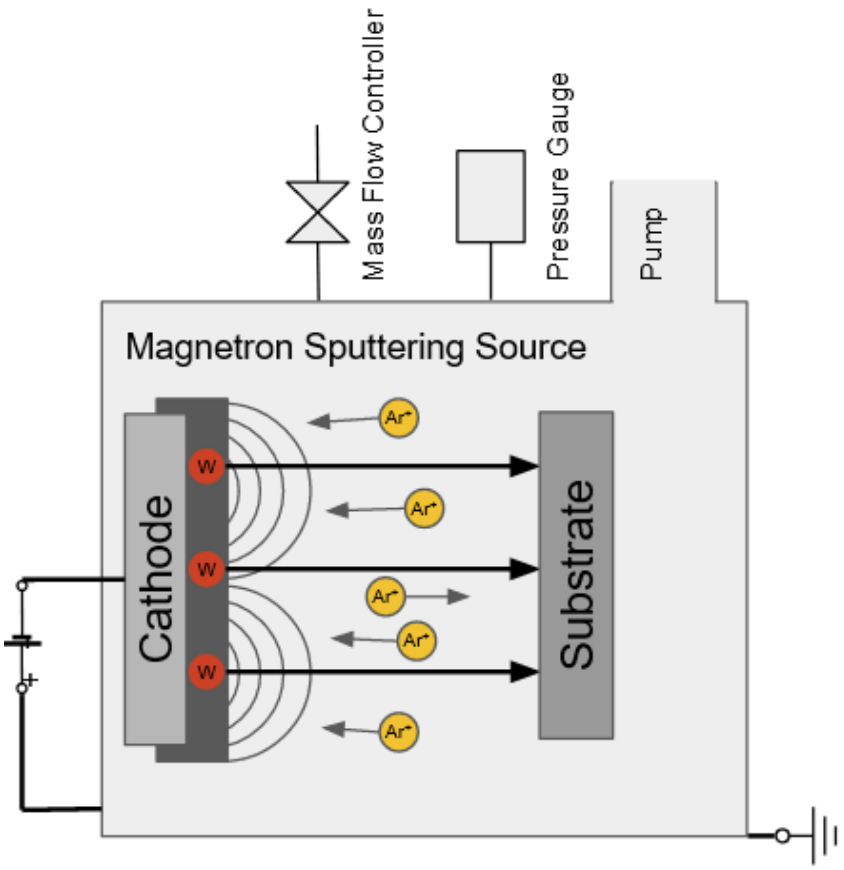


Figure 1.11: Figure showing the sputtering gas ions (argon, Ar^+) accelerating to the cathode and liberating tungsten atoms (W) from the target which get sputtered onto the substrate. Some gas atoms also move towards the substrate.

1.2.2 High Power Impulse Magnetron Sputtering (HiPIMS) Operation

In general, deposition rate to the target is proportional to the density of the plasma. Density of the plasma is also proportional to the power to the cathode. However, by substantially increasing the power to the cathode, this increases the heating of the magnetron, which could potentially lead to damage. The solution is to power the magnetron for short high power pulses, which results in a sufficiently low duty cycle, that allows sufficient time for heat to dissipate, usually with the aid of water cooling. This duty cycle is usually of the order of less than 10% with a period of the order of milliseconds. This results in a higher power but low energy per pulse. In the case of Figure 1.12 the pulse power is 2.3 kW and the energy per pulse is only $E_p = 0.58$ J

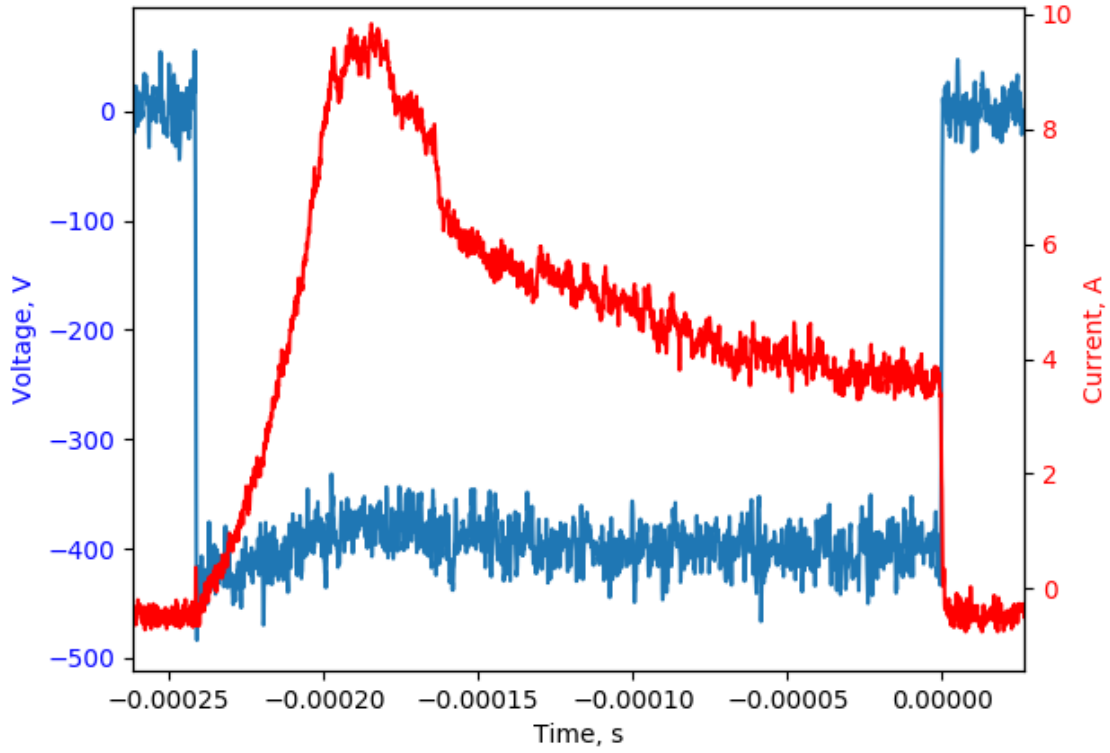


Figure 1.12: The current and voltage profiles of a 250 μs HiPIMS pulse supplied to a target magnetron sputtering source with E_p = 0.58 J

This configuration allows for very high density, high temperature plasmas to be produced locally to the target[56, 57]. These plasmas are comparable to the densities and temperatures seen in the divertor of MAST-U (approx. 10^{19} m^{-3} and a few eV) [58]. As mentioned in subsection 1.1.4 low temperature devices driven by a HiPIMS power supply induce moving regions of dense plasma around the target plate, known as spokes [40].

1.3 Tokamak Diagnostics for Edge Turbulence

Plasma diagnostics are an integral part to the study and understanding of plasmas, both for a fusion and industrial setting. Both low and high temperature plasmas have a number of transport and turbulence effects [37, 40] that are not well understood experimentally or theoretically. In this section we will consider the viability of a small number of diagnostics for the sole purpose of retrieving information in the scrape off layer (SOL) of a tokamak.

1.3.1 Optical Diagnostics

There are a number of optical diagnostics that can be used to return information about tokamak edge turbulence [59, 60]. This is possible via two main optical methods:

- Passing light through the plasma and measuring the collected light for differences in phase, wavelength, intensity, polarisation or spectra.
- Collisions occurring within the plasma cause cooling and recombination and the emission of light, which can be collected.

The first example of optical diagnostics includes two diagnostics capable of measuring electron temperature or density of filaments with some of the required limitations on resolution: Thomson Scattering [61] and Interferometery [62].

Thomson scattering is a process by which a high energy laser is injected into the plasma and the laser photons scatter off of free electrons in the plasma. This scattered light can be collected to analyse the wavelength shift to return the electron temperature. The number of collected photons is also proportional to the electron density. Typical laser frequencies are of the order of 30 Hz - 100 Hz. By using additional lasers and triggering each with a delay, a time spacing of as little as 5 μs can be achieved [63]. However, this does not alter the average time resolution. Thomson scattering remains one of the most reliable diagnostics due to its high spatial resolution and reliability of the data it returns. For this reason it will be one of the keystone diagnostics implemented onto ITER [64].

The most common form of plasma interferometery [65] is a Mach-Zehnder [66, 67] type. This involves passing two lasers of different wavelengths through the plasma across a known path and collecting the superposition of the mixed light. Since the plasmas refractive index is both wavelength dependant and density dependant, the density of the plasma can be calculated by tracking the phase difference between the two lasers. This can operate at very high time resolutions, typically of order 10 MHz [68]. However, this is a line integrated average across the length of the beam, which in the case of the tokamak mixes edge and core plasma.

On the second example, a popular way to observe turbulence and filaments is

through the use of fast cameras, seen in Figure 1.7. This is possible because the edge neutral density in MAST is sufficiently high that one can visibly see plasma effects in the scrape off layer. This is an incredibly powerful diagnostic as it has a field of view that can encompass the entire plasma region, with small fractions of the field of view blocked by the centre column and some wall mounted devices. Such cameras can also operate in excess of 100 kHz which is more than sufficient for the viewing of edge structures in a tokamak plasma. However, it has no capability to return any quantifiable information about the electron temperature, density or current in the plasma. This method is explained in great detail in by Farley [69], where a tomographic inversion technique is implemented to automate the identification of filaments.

1.3.2 Langmuir Probes

The term Langmuir probe, first coined by H. M. Mott-Smith and Irving Langmuir in 1926 [70], refers to a conductive object placed into a plasma with the aim of conducting a current directly from the plasma as a function of applied bias voltage. Fundamentally Langmuir probes are very simple to make and very difficult to analyse. While the act of inserting a probe into a plasma physically disturbs the system, the characteristics in the absence of a probe can be approximated through the use of post processing collected data. In order to correctly understand the way in which a Langmuir probe works, a region called the plasma sheath must be introduced in the space between the plasma and the probe.

Plasma Sheath

At the interface between the plasma and the wall of the vessel that is containing it, a Debye sheath develops spontaneously. This sheath controls the flow of particles to the wall and thus out of the plasma. It arises because the electrons, being many orders of magnitude smaller in mass than the ions, are moving much faster than the ions. This results in a net negative charge at the surface of the walls as it undergoes more collisions with electrons than ions. This net negative charge has a potential difference to that of the plasma, so an electric field is formed. This electric field retards the speed of electrons

to the wall while accelerating ions, causing the wall to float at some negative potential, V_{sf}.

To calculate this surface floating (sf) potential difference, V_{sf}, we first assume that the ion (i) and electron (e) fluxes (Γ) are equal in a single species hydrogen plasma at the sheath edge (se):

$$\Gamma^e_{se} = \Gamma^i_{se} \tag{1.3.1}$$

All ions that cross this sheath edge boundary reach the wall as they are accelerated by the positive potential. The ion flux density arriving at the wall, (w), is therefore:

$$\Gamma^i_w = \Gamma^i_{se} = n^i_{se} c^i_s \tag{1.3.2}$$

where n^i_{se} is the density of the ions in the sheath edge and c^i_s is the mean ion velocity defined by the plasma sound speed:

$$c^i_s \approx [k(T_e + T_i)/m_i]^{1/2} \tag{1.3.3}$$

where T_e and T_i are the electron and ion temperatures respectively and m_i is the mass of the ions. The density of electrons in the sheath falls off according to a Boltzmann factor

$$n_e(x) = n_{se} \exp\left(\frac{e(V_w - V_{se})}{kT_e}\right) \tag{1.3.4}$$

where V_w and V_{se} are the potentials at the wall and sheath edge respectively. The electrons are assumed to follow a Maxwellian distribution so the average thermal speed, $\langle v \rangle$, or average particle speed, $\bar{c}$, can be defined by:

$$\langle v \rangle \ = \int_0^\infty v f^{Max}(v) dv/n = \bar{c} = \left(\frac{8kT_e}{\pi m_i}\right)^{0.5} \tag{1.3.5}$$

where $f^{Max}(v)$ is the Maxwellian velocity distribution. In order to find the one way particle flux density towards the sheath (x-direction) there must be a relationship between the velocity and relative density within the sheath:

$$\delta n = f(v) dv_x dv_y dv_z \tag{1.3.6}$$

Hence it can be defined that by only considering the particle flux in the x-direction yields:

$$\delta \Gamma_x = v_x \delta n = v_x f(v) dv_x dv_y dv_z \tag{1.3.7}$$

Integrating over the limits gives the flux distribution:

$$\Gamma_x = \int_{v_x=0}^{+\infty} f^{Max}(v) v_x dv_x \int_{v_y=-\infty}^{+\infty} dv_y \int_{v_z=-\infty}^{+\infty} dv_z \tag{1.3.8}$$

$$\Gamma_x = \frac{1}{4} n \bar{c} \tag{1.3.9}$$

In the consideration for electrons reaching the wall, the Boltzmann factor is re-introduced from Equation 1.3.4, where their velocity is defined by $\bar{c}_e$:

$$\Gamma_w^e = \frac{1}{4} n_w \bar{c}_e = \frac{1}{4} n_{se} \exp[e(V_w - V_{se})/kT_e] \bar{c}_e \tag{1.3.10}$$

Assuming the same flux of ions and electrons touch the wall such that $\Gamma_w^e = \Gamma_w^i$, Equation 1.3.2 and Equation 1.3.10 are set equal. Assuming that $V_{se} = 0$ states there is no additional potentials outside of the sheath such that $V_w - V_{se} = V_{sf}$.

$$n_{se} c_s = \frac{1}{4} n_{se} \exp[eV_{sf}/kT_e] \bar{c}_e \tag{1.3.11}$$

This results in a relationship between the mass and temperature of both the electrons and ions and the surface floating potential, V_{sf}.

$$\frac{1}{2} ln\left(2\pi \frac{m_e}{m_i}\left(1 + \frac{T_i}{T_e}\right)\right) = \frac{eV_{sf}}{kT_e} \tag{1.3.12}$$

Now consider a case where the ion and electron fluxes are no longer equal because of an externally applied bias. If the left wall surface is biased to $-kT_e/e$ relative to the right wall surface. Let the left and right biases be V_l and V_r respectively. The electron flux reaching the right wall, rw, will be:

$$\Gamma_{rw}^e = \frac{1}{4} n_{se} \bar{c}_e \exp[eV_r/kT_e] \tag{1.3.13}$$

and the ion flux will be

$$\Gamma_{rw}^i = n_{se} c_s = \frac{1}{4} n_{se} \bar{c}_e \exp[eV_{sf}/kT_e] \tag{1.3.14}$$

for the left wall, lw, the electron flux will be

$$\Gamma_{lw}^e = \frac{1}{4} n_{se} \bar{c}_e \exp[eV_{lw}/kT_e] \tag{1.3.15}$$

and the ion flux will be

$$\Gamma_{lw}^i = n_{se} c_s = \frac{1}{4} n_{se} \bar{c}_e \exp[eV_{sf}/kT_e] \tag{1.3.16}$$

Noting that $\Gamma^i_{lw} = \Gamma^i_{rw}$ and invoking charge conservation:

$$\Gamma^e_{lw} + \Gamma^e_{rw} = 2\Gamma^i = 2\, n_{se}\, c_s \tag{1.3.17}$$

Such that the potential between the two walls must be

$$V_r - V_l = V_{applied} \tag{1.3.18}$$

Resulting in

$$\frac{eV_l}{kT_e} = ln\left(\frac{2\exp[eV_{sf}/kT_e]}{1 + \frac{e^{[eV_{applied}]}}{kT_e}}\right) \tag{1.3.19}$$

Since Γ^i_{rw} and Γ^e_{rw} are no longer in balance, there is a net current density to the surface, j:

$$j_r = e(\Gamma^i_{rw} - \Gamma^e_{rw}) = -j_l \tag{1.3.20}$$

$$j_r = en_{se}c_s\left[1 - \exp\left(\frac{e(V_r - V_{sf})}{kT_e}\right)\right] \tag{1.3.21}$$

If $V_{applied} \to -\infty$ then right surface can be considered to be repelling all electrons and only having interactions with ions, a current defined as the ion saturation current as a function of the total density $n_0 = n^i_{se} + n^e_{se} = 2n_{se}$ in an isothermal and quasineutral case:

$$j_r \to en_{se}c_s = j^i_{sat} \approx \frac{1}{2}en_0c_s \tag{1.3.22}$$

Taking this into consideration, the plasma parameters of electron temperature, T_e, ion saturation current, I^+_{sat}, and floating potential can be derived from knowledge about an applied bias to a plasma from the sheathed surface, V_r, and a measured current on the sheathed surface, j_r. This can be extrapolated to a measurement device known as a Langmuir probe by assuming the probe is the sheathed surface such that $V_r = V_{LP}$ and $j_r = I_{LP}$:

$$I_{LP} = I^+_{sat}\left[1 - \exp\left(\frac{e(V_{LP} - V_f)}{kT_e}\right)\right] \tag{1.3.23}$$

From this point forwards in the thesis, the electron temperature T_e will be in units of eV such that $T_e[eV] = k_bT_e[K]/e$ which simplifies Equation 1.3.23 to:

$$I_{LP} = I^+_{sat}\left[1 - \exp\left(\frac{V_{LP} - V_f}{T_e}\right)\right] \tag{1.3.24}$$

Probe Characteristics

Now that subsection 1.3.2 has defined that the probe is drawing a current, the main assumptions are as follows [71]:

1. Electron and ion concentrations are equal (quasineutrality).
2. Electron and ion free paths are much larger than the probe radius.
3. There is a Maxwellian distribution of electron and positive ion velocities.
4. Biasing the probe does not result in expansion of the sheath volume

As is explained in subsection 1.3.2, with the derivation of Equation 1.3.23, important information can be extrapolated from a Langmuir probe by manipulating the flow of particles in the sheath.

It is also explained through the use of Equation 1.3.22 the density can be inferred if one has information about the ion and electron temperature.

$$I_{sat}^{+} \approx \frac{1}{2} A e n_0 \left(\frac{k(T_e + T_i)}{m_i} \right)^{1/2} \tag{1.3.25}$$

where A is the surface area of the probe that is drawing current. For an approximation in some low temperature plasma systems these can be assumed to be equal such that $T_i = T_e$. This allows the density to be approximated from:

$$I_{sat}^{+} \approx \frac{1}{2} A_{LP} e n_0 \left(\frac{2kT_e}{m_i} \right)^{1/2} \tag{1.3.26}$$

In cases where $T_i = T_e$ is not true it can still be used as a close approximation of the density as the correction factor is small.

Figure 1.13 shows some key points on the I-V curve, namely the floating potential, V_f and the plasma potential (sometimes known as the space potential), V_s. The plasma potential is the point at which the electrons within the plasma are no longer exposed to a retarding potential but instead are being accelerated towards the probe. This is seen very clearly as a break in the characteristic and is the reason behind the formation of the “knee”. V_f is always less than V_s because the electron and ion diffusion rates differ

so greatly, with the former always being larger. This means that these two quantities will only ever be equal if there is some retarding field that slows down the electrons.

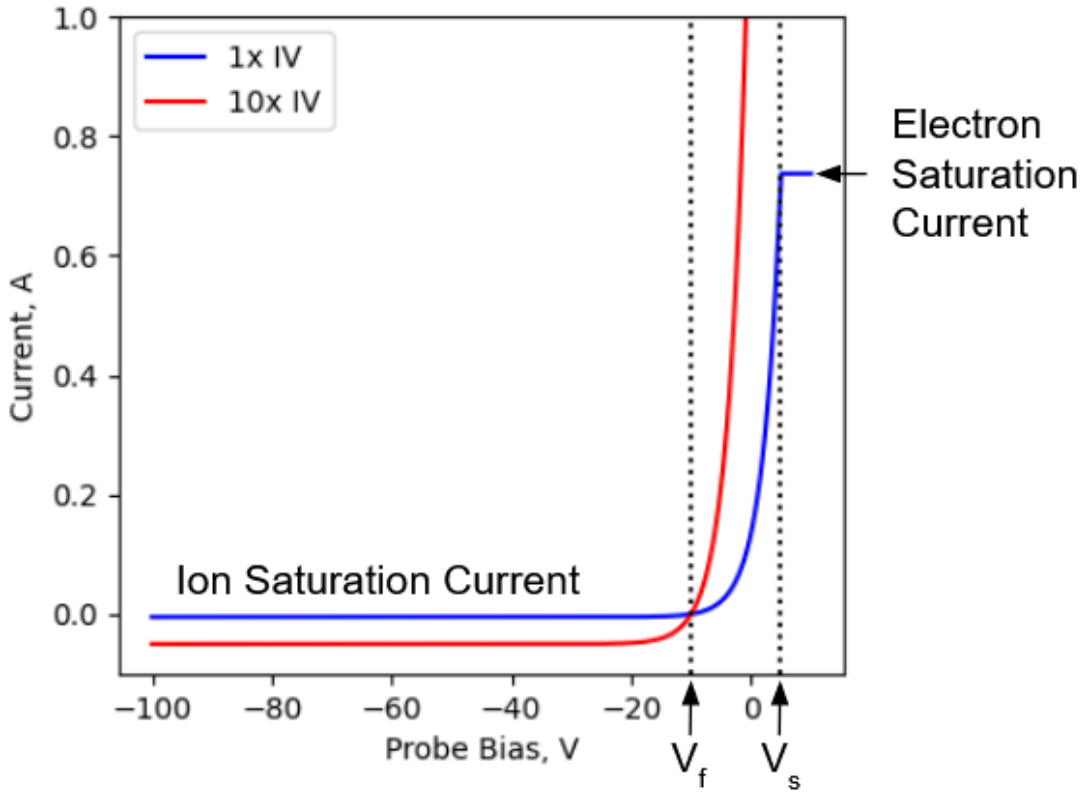


Figure 1.13: A plot showing an idealised probe characteristic (shown in blue) where V_f is floating potential and V_s is the plasma potential. The red curve's current has been multiplied by 10 to show the ion current. Adapted from Chen [72].

A combination of Equation 1.3.23 and Equation 1.3.26 shows that all important plasma parameters can be derived from the information contained within Figure 1.13. The electron current can be derived from I by extrapolating and subtracting the ion current, leaving only the electron current. It is difficult to draw conclusions from the electron region as often the current that is drawn causes a disturbance in the plasma.

Due to the effectiveness of Langmuir probes as a diagnostic, 840 of them are installed in MAST-U. These are positioned mostly around the divertor and nose region of the tokamak, with a single probe being located in the midplane which is mounted on a reciprocating probe stem. These probe positions are shown in Figure 1.14.

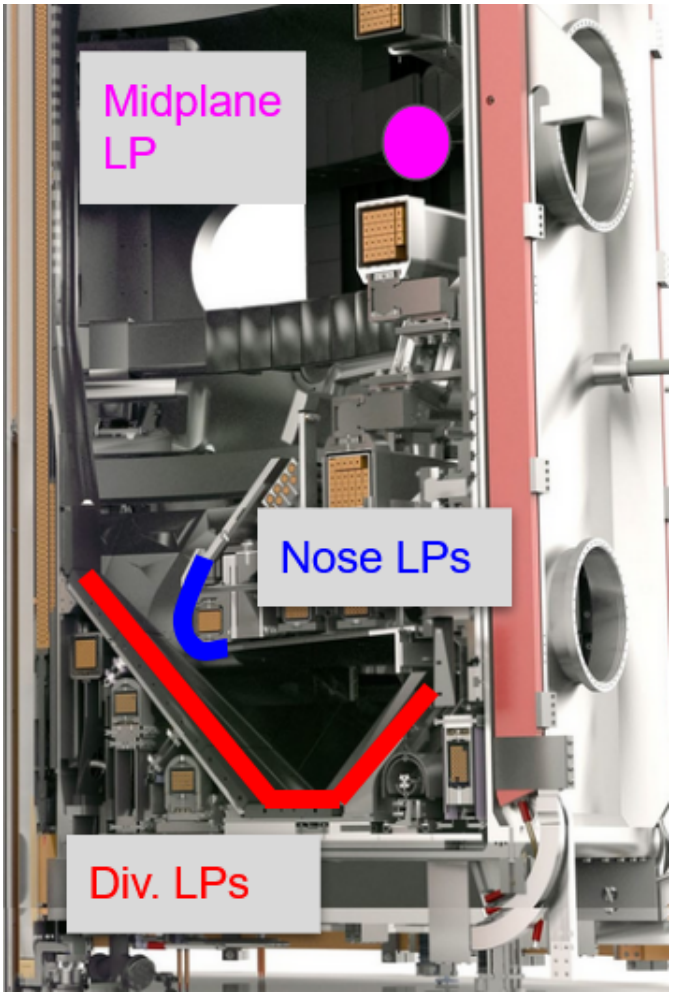


Figure 1.14: MAST Upgrade with the positions of the midplane, nose and divertor Langmuir probes indicated.

1.4 Field-Programmable Gate Arrays

Fusion diagnostics require capabilities for large volumes of data at high time resolutions and some require real time data processing, such as Thompson scattering [73] and laser interferometery [74]. This has usually been fulfilled by analogue electronics, which has induced a large space, power and financial cost. FPGA's bring the advantage that they can be purchased off the shelf and they can be customised to perform digital operations.

1.4.1 The Principle of FPGAs

The Field Programmable Gate Array (FPGA) [75, 76] is fundamentally a piece of hardware that can be used to carry out logic operations. Much like a Central Processing Unit (CPU), it consists of a large network of interconnected transistors arranged into Configurable Logic Block (CLB) on the chip. Unlike a CPU however, it is completely configurable by the end user to perform different logic tasks. A simplification of a CLB can be seen in Figure 1.15. This shows that every individual CLB on an FPGA is capable of storing values or outputting the results of a 4-input LUT forming the basis of logic gate operations. An explanation of the Look-up Table (LUT), clock, multiplexer and flip-flop will be detailed later in this section.

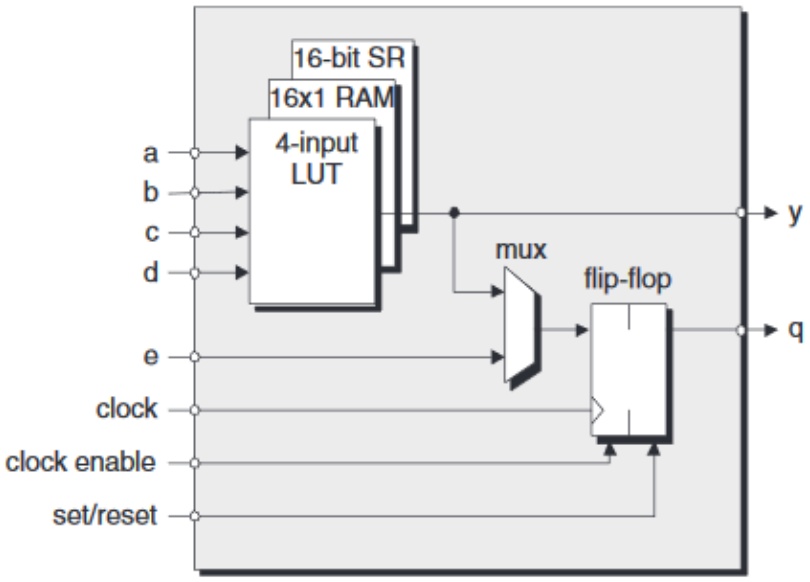


Figure 1.15: A block diagram of a Xilinx Configurable Logic Block (CLB). From [76]

Like the name suggests (**field** programmable gate array), this can be done in the field with very little specialised hardware. The FPGA itself consists of a series of individual CLBs which are all connected together in a interconnect matrix, as seen in Figure 1.16. The inputs and outputs to these CLBs can be connected to Input/Output/Buffer (IOB) to interface to signals external to the FPGA.

This architecture allows the programmer two main areas of development; changing the behaviour of the logic blocks or changing the routing between blocks. The number

of logic blocks on the chip is usually proportional to size and cost, but due to the configurable nature once a design has been shipped, it can be changed in the field by the user.

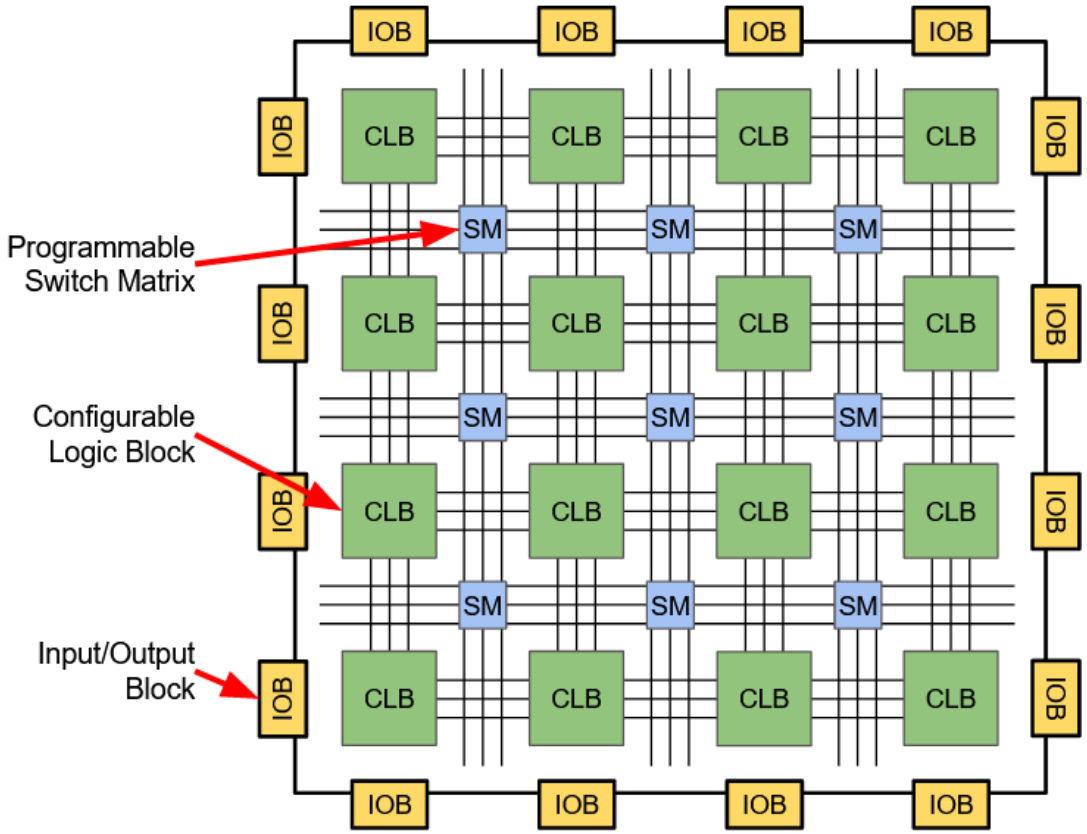


Figure 1.16: Schematic of FPGA architecture showing the relationship between; Input/Output/Buffer, Configurable Logic Block (CLB) and a Switch Matrix.

The FPGA is used in place of an Application Specific Integrated Circuit (ASIC), which as the name suggests is designed to only perform a single task. This results in any modification, no matter the size, requiring a new circuit being created - which can often take considerable time. In contrast to this the FPGA can be reprogrammed by an FPGA developer in the field, perhaps with the FPGA still in-situ, provided that the FPGA has sufficient resources to accommodate any required change. Programming an FPGA is done by using a hardware description language (HDL). The two main HDLs are; (VHSIC-HDL) Very High Speed Integrated Circuit Hardware Description Language (VHDL) [77] and Verilog [78]. These HDLs allow the user to describe the function of the FPGA at a high level where the complexity of the underlying logic circuits is abstracted away. The design can then be synthesised which translates the HDL into the needed logic blocks

and interconnects. Vendor software such as Xilinx Vivado can then map this synthesis to available resources on the desired FPGA. This is known as implementation. From this implementation, a bitstream can be produced, which is a series of instructions including the desired logic, routing and initial configuration for the chip. This loaded onto the device and is used to configure the FPGA at power-up.

1.4.2 FPGA Core Concepts

The implementation of an FPGA requires the precise circuitry of a series of transistors which involves breaking down tasks to suit the resources available on the FPGA. Simple concepts such as the mathematical division of two numbers, require multiple step algorithms and are computationally expensive. However, breaking down a particular task into its smallest possible components also makes the best use the FPGA's capability for parallelisation. In order to describe the design of FPGA architecture, some important digital concepts will have to be introduced in this section. While some operations are standardised, others require custom user-built algorithms to achieve the desired output.

Clock Cycles

A clock, in digital processing terms, is often a 50% duty cycle square wave with a high frequency periodicity that determines how fast a flip-flop operates. A higher frequency clock will result in a larger bandwidth input or output to a flip-flop. This clock signal is distributed across the whole FPGA with careful routing to ensure that the signal reaches each flip-flop with the same delay. The use of external devices may require the use of multiple clocks but this adds an additional level of complexity to the design. If possible it is best practice to build a system that minimises the number clock domains. The capable speed of a clock on an FPGA is one of the main considerations when choosing a suitable FPGA for a given design.

Registers

Another core component of digital processing is the concept of a register, often referred to as a "flip-flop". A register can simply be thought of as memory, with each register storing a single bit of information. This storage is achieved through the use of logic gates connected to a clock, as described by the edge-triggered type-D flip-flop shown in Figure 1.17. Every rising edge of the clock cycle takes in the value of D on that clock event and stores it, ready to be called as the value Q.

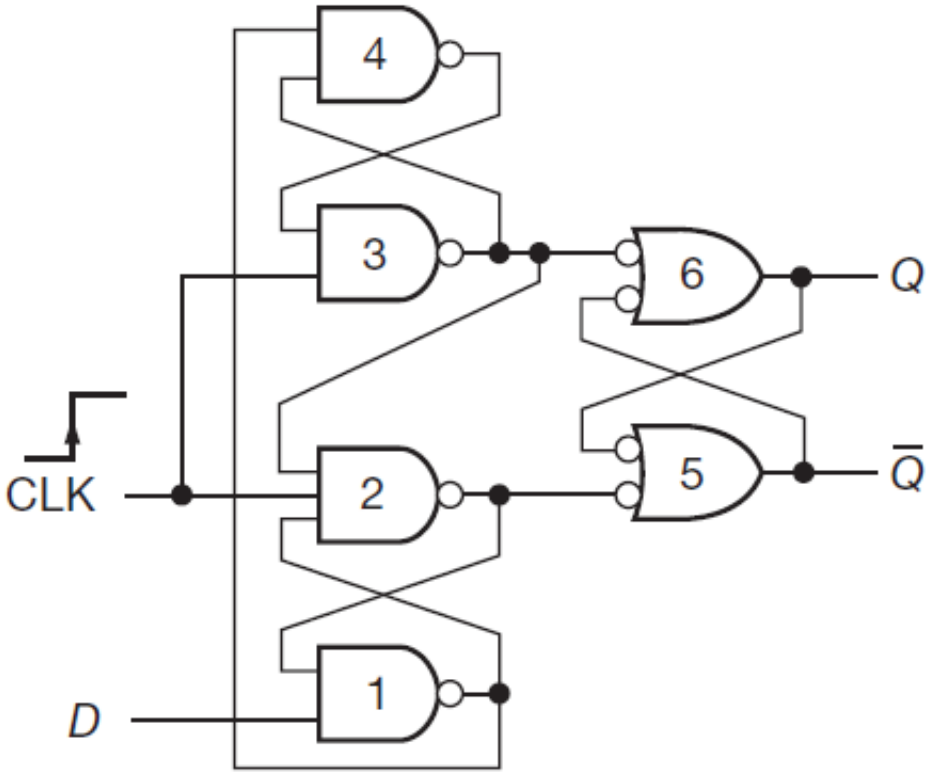


Figure 1.17: Schematic of an edge-triggered type-D register (flip-flop), commonly seen in FPGA architecture where D is the state to be stored and the process is driven by a clock. From [79]

Look-up Table

A Look-up Table (LUT) is a section of Read-Only Memory (ROM) that can relate to some form of truth table where a particular sequence of inputs relates to a specific output. In the given case of Figure 1.18, any of 16 possible states can represent any boolean function. Look-up Tables can also be used to speed up mathematical processes by storing the result

of some value multiplied by a constant. This way the user can input the value and the result will be returned within a single clock cycle, as this is a storage operation rather than a mathematical operation.

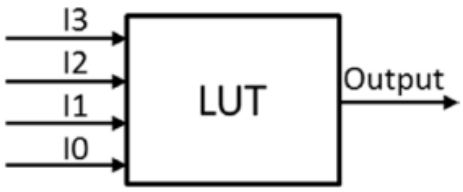


Figure 1.18: Simple 4-input Look-up Table (LUT) logic block. From [80]

Finite State Machines

An important concept in the design of successful and efficient FPGA instruments is the effective use of the Finite State Machine (FSM). A FSM is a mathematical model for breaking down any individual task into a number of states, where only 1 state can be active at a time, with a action to transition between states. A simple FSM that switches between states is illustrated in Figure 1.19. The benefits of designing an FPGA in this way leaves it open to expansion if the user wants to add more states at a later stage of the design. This is utilising one of the main benefits of the FPGA in digital design, the ability to edit the design without having to reprint a whole electronic design.

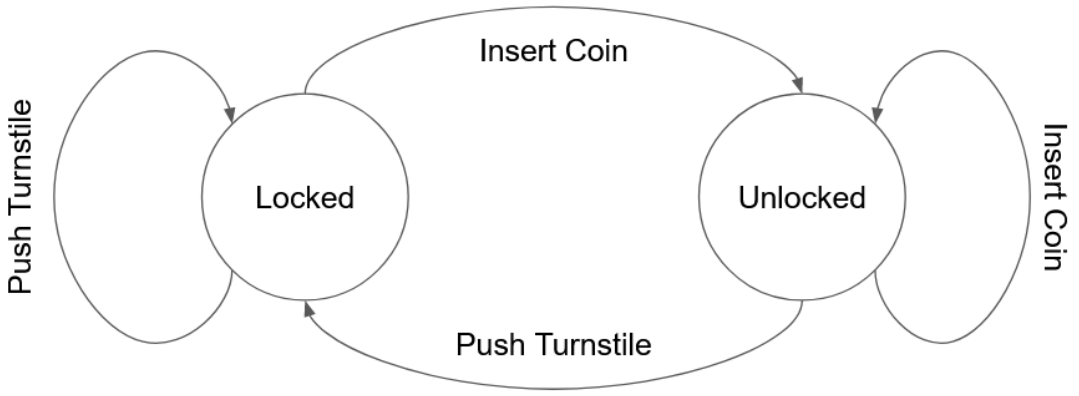


Figure 1.19: Simple finite state machine diagram depicting the operation of a coin operated turnstile. Modified from [81].

Parralisation

Parralisation is an integral part of FPGA design, as each operation is stored to a register per clock cycle. This is suitable for simple calculation such as $A + B = C$, as the whole operation can be completed in a single clock cycle. However $A \times B \times C + D = E$ would take multiple clock cycles because the calculation inherently requires results to be stored on intermediate steps. The given equation, illustrated in Figure 1.20, would first need to store the result of $A \times B$, then the result of this multiplied by C, then the result added to D. Given an operation can only be performed per clock cycle, the value of D may have changed prior to being used. This operation is illustrated in Figure 1.20.

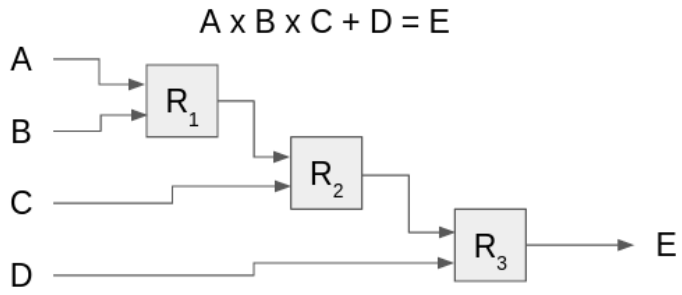


Figure 1.20: Diagram showing an un-pipelined method of performing a calculation, where R_1, R_2 and R_3 are registers and ABCD are inputs with output, E

This however can be addressed by the inclusion of additional registers to store the value of a variable until it needs to be used, as seen in Figure 1.21. This not only has the benefit of allowing the result of the calculation to be correct regardless of the changing of the value between clock cycles. But it also allows all of the values to change once per clock cycle, so while R_4 and R_5 have been calculated using the original $ABCD$; R_1, R_2 and R_3 can be re-calculated using the next set of values. To put this in perspective, if each register requires 1 clock cycle, Figure 1.20 would require 3 clock cycles to complete the first calculation, and a further 3 clock cycles to complete the second calculation. In contrast, Figure 1.21 would also require 3 clock cycles to complete the first calculation, but only 1 further clock cycle to complete the second calculation so on so forth.

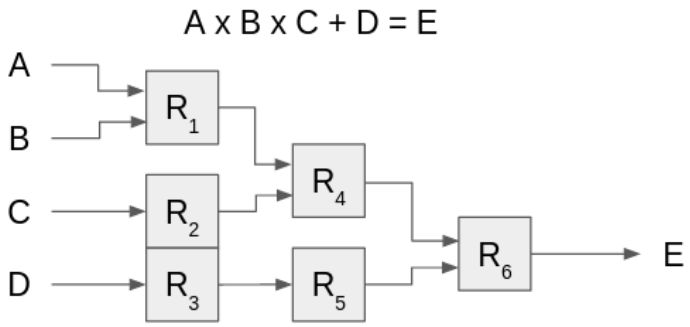


Figure 1.21: Diagram showing a pipelined method of performing the same calculation as seen in Figure 1.20, where R_1, R_2, R_3, R_4, R_5 and R_6 are registers and ABCD are inputs with output, E

1.4.3 Koheron Software Development Kit

The Koheron Software Development Kit (SDK) [82] is an off the shelf open source environment that can be used to distribute standardised IP to Zynq based System on Chip (SoC) devices. The SDK comes with a number of pre-built examples from an Light Emitting Diode (LED) blinker to a custom laser controller design.
By utilising some of the standardised Intellectual Property (IP) developed by Koheron, tasks such as development of an operating system and associated software can be bypassed. This saves a large amount of development time and makes the device easier to modify by future developers. This same framework has been used for a number of diagnostics [83] on MAST-U enabling the workflow to be significantly sped up.

Koheron allows the development of instruments to be streamlined because the architecture for things such as the Analogue to Digital Converter (ADC) and the Digital to Analogue Converter (DAC) are already designed and ready to use in a Vivado block diagram, an example can be seen in Figure B.1. This allows the user to focus on developing a instrument that does what is required and interfacing it with the FPGA (in this case, Red Pitaya) is simplified. Also included in the make file is the ability to write python and C++ drivers that allow the user to pass information to and from the FPGA during runtime, either using a python API or a web interface. Both of which come with detailed examples and guides which can be found on the website and github [82, 84] and the dataflow can be seen in Figure 1.22.

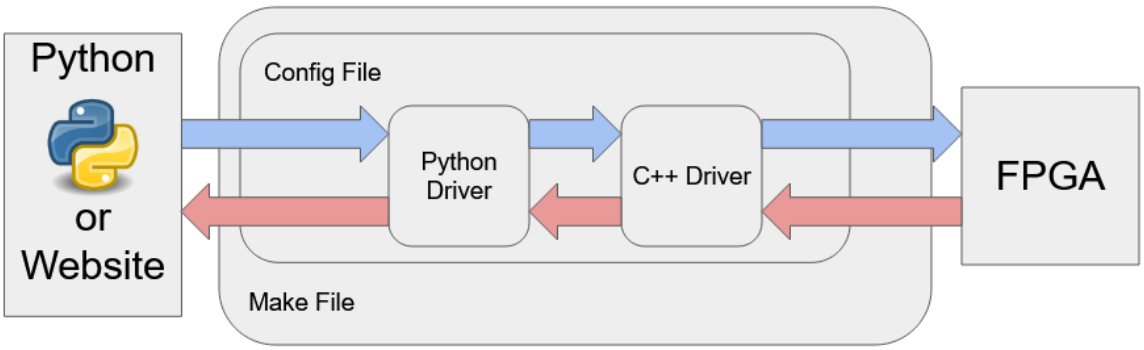


Figure 1.22: Koheron data flow diagram showing how the use of drivers and a config and make file can allow communication between a python or web interface and with the FPGA directly.

1.5 Mirror Langmuir Probe

The Mirror Langmuir Probe (MLP) was developed at Massachusetts Institute of Technology (MIT) by B.LaBombard and L.Lyons for the purpose of fast collection of Ion Saturation current, floating potential and electron temperature [85]. Conventional Langmuir probes have many shortcomings in terms of a trade-off between temporal or spatial resolution. This concept bypasses some of those problems through the use of sophisticated electronics. The basic concept of operation of an MLP is described in Figure 1.23 [85].

The original MLP concept was a Langmuir probe that was capacitively decoupled from the driving power supply. The MLP consists of a pair of NPN transistors that act as a mirror to the I-V response of a magnetised plasma-electrode sheath [86]. This allowed the probe to respond to and record plasma fluctuations on the order of 1 MHz, a few orders of magnitude greater than that of conventional Langmuir probes. This is achieved by a fast switching bias waveform that remains stable within 3 bias regions for a period of time.

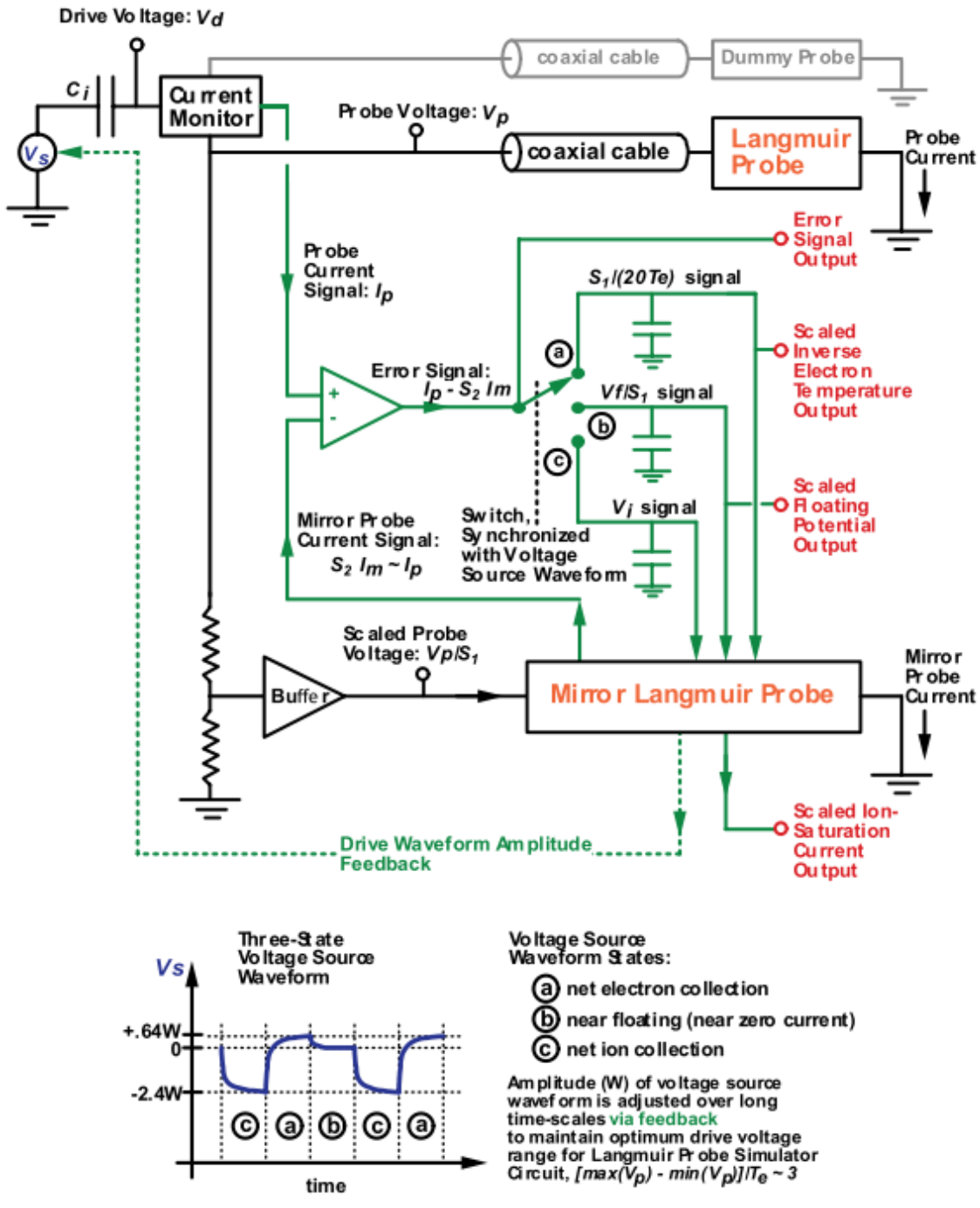


Figure 1.23: MLP System concept as described by L.Lyons [85]

1.5.1 Digital Mirror Langmuir Probe

The digital mirror Langmuir probe is a recent development that has first been through proof of principle [87] and also implementation [88] on the low temperature linear helicon device Dynamics of ION Implantation and Sputtering Of Surfaces (DIONISOS) [89–91].

The combination of this testing has both proven the efficacy of a digital mirror Langmuir probe and also its real world application. However testing by McCarthy et al.[88] only proved the tracking of a 10 Hz fluctuation in magnetic field at a temporal resolution of data output of 140 kHz using some of the data acquisition electronics of the original MLP[85, 86]. The implemented algorithm was also shown to converge on real values on the order of 100 μs, which will not be suitable for some low temperature applications using HiPIMS, as the pulse will be over before the algorithm has converged.

The device developed by Vincent and McCarthy [87, 88] bypassed the use of the pair of NPN transistors that were utilised within the original digital Langmuir probe. This was done by solving the planar in 3 distinct regions of the IV curve and allowing the results to converge until the fit is accurate. The work in this thesis can be considered both an adaptation and a continuation of this work done previously. This revised design has reduced complexity due to the removal of the NPN transistor pair and the a large amount of analogue electronics. This overall dramatically reduces the size of the diagnostic from a large electrical box that has several electrical planes to a single 1u 19" rack.

In addition to this since a large amount of the electrical components are no longer required there is no longer a cost associated with them. The total cost of this design, minus a power supply / amplifier which can be brought off the shelf, is not in excess of four hundred pounds sterling at the time of writing.

Lastly the introduction of using an FPGA for the digital processing means that the design as a whole is more modular and robust. It will be relatively easy, compared to an analogue system, for a new developer to make changes to the existing design to accommodate things such as:

- Larger capacitor range
- Changing of dynamic bias range (from $4 \cdot T_e$)
- The addition of additional data points to increase the accuracy of the fit

Another issue that was found with the previous MLP system is that it was only correctly calibrated for the particular configuration it was designed for use on Alcator C-

Mod [92]. The prospect of moving it to a different device would have been inconceivable due to impedance matching, different voltage and current ranges or changes in capacitance needed. This new design using an FPGA is built in mind of it being a modular system that fundamentally only measures current and voltage at a high bandwidth. Provided that these measurements are impedance matched and the capacitor values are appropriate, this device is fully transferable between a range of different plasma applications.

1.6 Scope of Thesis

The aim of this thesis is to present the design, testing and implementation of a high-speed Langmuir probe FPGA that is capable of measuring the electron temperature and density profiles of fast moving filaments in tokamaks. In order to achieve this, the basic objectives of the device can be outlined:

- Time resolutions exceeding 200 kHz must be achieved, the value for which is explained in chapter 2
- Device is designed for use in MAST-U, but testing in a low temperature - low pressure HiPIMS plasma with a hope to observe spokes will be a good benchmark
- Mitigate / eliminate the effects of the order of 100 μs delay discussed in subsection 1.5.1
- Design and implement low cost electronics for interface between plasma and FPGA including capacitor switching circuit, detailed in section 2.1

In chapter 2 an overview of simulation based work is discussed. This involves defining the initial system requirements and objective including Python simulations as a proof of concept for algorithms. Also discussed is key principles in the FPGA design process including test benching and simulations of an initial prototype.

The scope of this project since its inception has changed dramatically to involve much more electrical design and consideration than originally planned. Chapter 3 considers the system requirements, design and theoretical basis for electrical components and

systems that are required for the FPGA to interface with a physical electrical probe and power supply.

Chapter 4 concerns the experimental setup used for initial testing performed at the University of Liverpool on low temperature magnetron plasma systems. Although this device is designed with the intent of installation onto high-temperature tokamaks for filamentary studies, the ease of access to such devices at Liverpool drastically decreases the length of time in the testing phase.

Chapter 5 discusses the results obtained from installation on a real plasma device, some of the problems that were found and what kind of improvements have been made since the initial design process.

Chapter 6 draws conclusions which summarises the main achievements made from previous chapters and draws comparisons to similar fast probe systems. Considerations are made for the future development of the projects installation onto MAST-U.

Chapter 2

Ultra-Fast Langmuir Probe (UFLP) Design

2.1 System Requirements

As discussed in subsection 1.1.4, "filaments" can be modelled as cylindrical tubes as small in diameter as 1 cm. These move at radial velocities of up to 1 km/s. If a wire Langmuir probe is 1mm in diameter then the time taken for such a filament to pass the probe can be defined as:

$$\frac{0.01[m]}{1000[m/s]} = 10^{-5}[s] \tag{2.1.1}$$

In order to characterise this filament a time resolution of above 200 kHz will be required to fulfil the Nyquist frequency requirement [93, p. 119] to resolve the object. Achieving a higher frequency of 1 MHz would be more desirable, which would result in 10 data points within a single filament.

In addition to the observation of MAST filaments, this probe would be desirable if it was able to observe low temperature "spokes" as also described in subsection 1.1.4. These, conveniently are also shown to cross the probe diameter (smaller in low temperature, 0.25 mm) but would transit the probe faster in times of 3 to 6 μs [40, p. 23]. This would require higher time resolutions of a minimum 333 kHz to 666 kHz. However the main difference being that the temperatures and densities of the plasma tend to be

much smaller. Hence, such a device will have to work in two distinct regimes; high and low current and voltage modes.

2.2 The MLP Algorithm

The original MLP used a pair of NPN transistors to take an input current and solve the fit to a Langmuir curve in a way that gave direct outputs of the desired parameters. This is possible because the NPN transistor pair has a very similar resistive response to the plasma. A full mathematical derivation for this process can be found in [86]. However, the same principle can be achieved simply by analysing 3 data points to produce a rough fit to planar probe equation (Equation 1.3.23) by re-arranging it into 3 forms:

$$I_{sat}^{+} = \frac{I_{V_p}}{e^{\frac{V_p - V_f}{T_e}} - 1} \tag{2.2.1}$$

$$T_e = \frac{V_p - V_f}{\ln(\frac{I_{V_p}}{I_{sat}^{+}} + 1)} \tag{2.2.2}$$

$$V_f = V_p + T_e \cdot \ln\left(\frac{I_{V_p}}{I_{sat}^{+}} + 1\right) \tag{2.2.3}$$

There are some important inferences that can be made from these equations that will give an insight into some of the parameter ranges. Firstly, using Equation 2.2.1, if $V_p << 0$ then the equation converges towards:

$$I_{sat}^{+} = -I_{V_p} \tag{2.2.4}$$

This means that Equation 2.2.1 becomes a small correction to the measured current if a large negative bias is applied.

Secondly, using Equation 2.2.3 if the measured current at the applied voltage is 0, the floating potential, V_f, must equal the voltage at the probe, V_p. This scenario can be forced by floating the probe or decoupling the circuit with a capacitor, which will be discussed in detail in section 3.1. This means that there is another equation that is a

small correction to a measured value. This also forms the basis of the voltage range that is optimal to apply if only 3 voltages can be selected.

There is also something to be said about the chosen ranges for both the bias and current measurements in such a Langmuir system. In order to ensure that the circuit is floating at the plasma's floating potential, the net current passing through a capacitor must be 0. This can be achieved by drawing a negative, positive and zero current sequentially, such that the time-averaged signal is 0. In order to ensure the measurement of 3 such current states, measurements must be taken relative to the floating potential. This defines that 3 voltage levels must be applied that will draw zero current and equal in magnitude positive and negative currents, which can be illustrated by Figure 2.1.

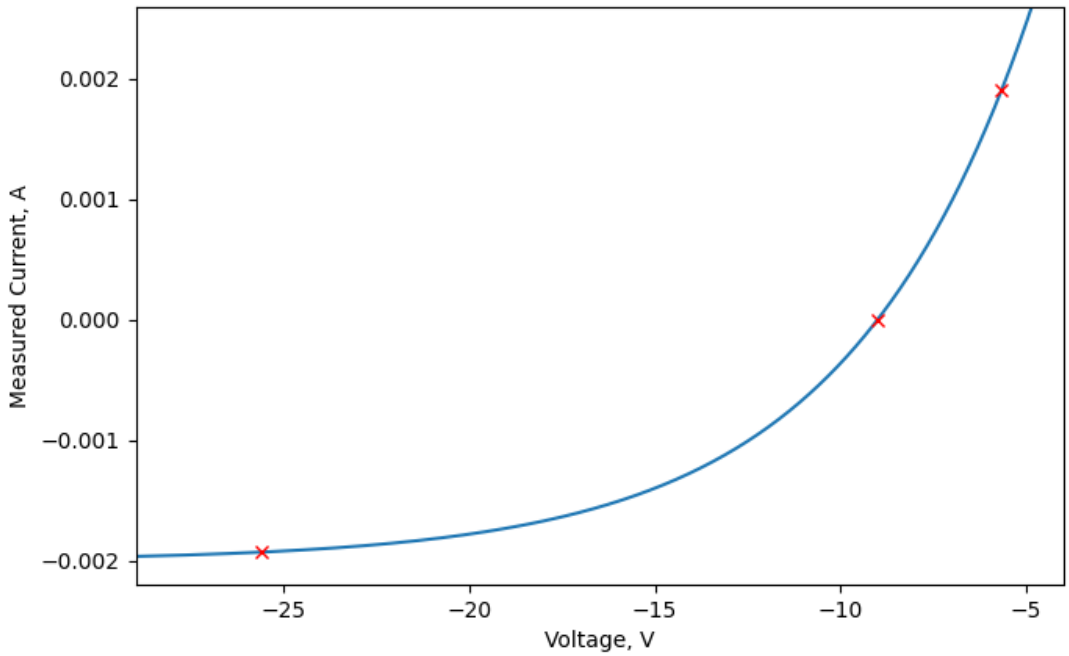


Figure 2.1: The optimal voltages to return equal magnitude currents for a $V_f = -9\,V$ and $T_e = 2.7\,eV$ idealised plasma

From Equation 1.3.23 it can be seen that while the floating potential V_f causes small linear shifts in the position of the IV curve relative to 0 V, the electron temperature scales it. A higher temperature results in needing more applied bias to draw the same current from the plasma. If the goal is to have unity of both positive and negative current, then the applied bias must be offset by the floating potential and be scaled by temperature to ensure the magnitude of the current is the same in both directions. Such

that any applied bias must be:

$$V_p = V_{+,-,0} \cdot T_e + V_f \tag{2.2.5}$$

The bias range can be optimised also by defining that there must be at least a voltage range of either $V_p = 3 \cdot k_b T_e$ as determined by Labombard and Lyons[86] or $V_p = 4 \cdot k_b T_e$ as determined by Vincent et al.[87]. Larger separations can be used which fundamentally will increase the magnitude of the current measurement. This may need to be applied for measuring low density plasma in industrial systems or in a Tokamak divertor. Two such ranges are illustrated in Figure 2.2.

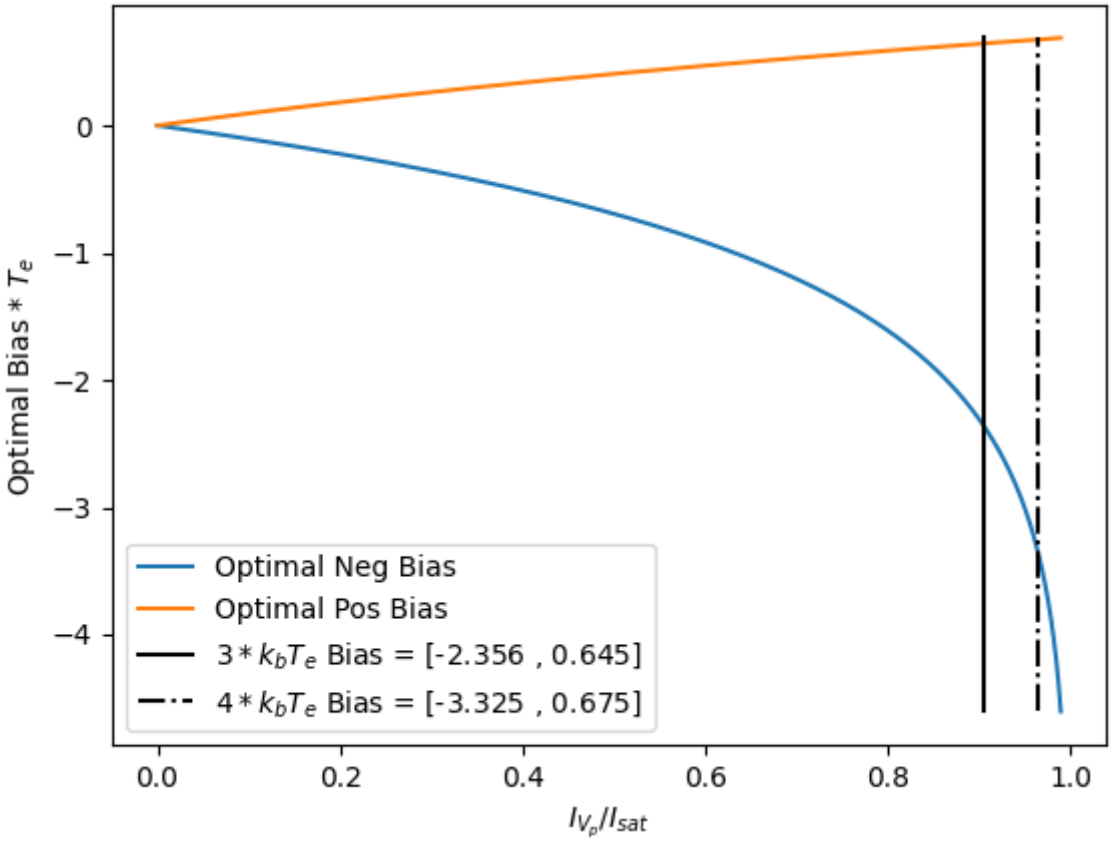


Figure 2.2: The optimal bias values to draw equal magnitude current given a minimum bias range of either $3k_bT_e$ or $4k_bT_e$

Figure 2.2 shows that the choice of these two bias ranges returns different optimal voltages, such that if $V_p = 3 \cdot k_b T_e$:

$$V_{+,-} = [-2.356, 0.645] \tag{2.2.6}$$

Which substituting these values into Equation 1.3.23 returns $I = 0.905 I_{sat}^{+}$ in agreement with Labombard and Lyons[86]. Equally using $V_p = 4 \cdot k_b T_e$ returns:

$$V_{+,-} = [-3.325, 0.675] \tag{2.2.7}$$

Which returns $I = 0.964 I_{sat}^{+}$, in agreement with McCarthy et al.[88]. In a $k_b T_e = 1$ eV plasma with a V_f = -2.4 V, the ideal bias voltage waveform would be as seen in Figure 2.3. The important distinction here is that the voltage applied is different from the voltage that is measured at the probe. This is because if the net current through the capacitor is zero, the requirement for measuring the floating potential is met and all applied voltages will be floating on top of the floating potential.

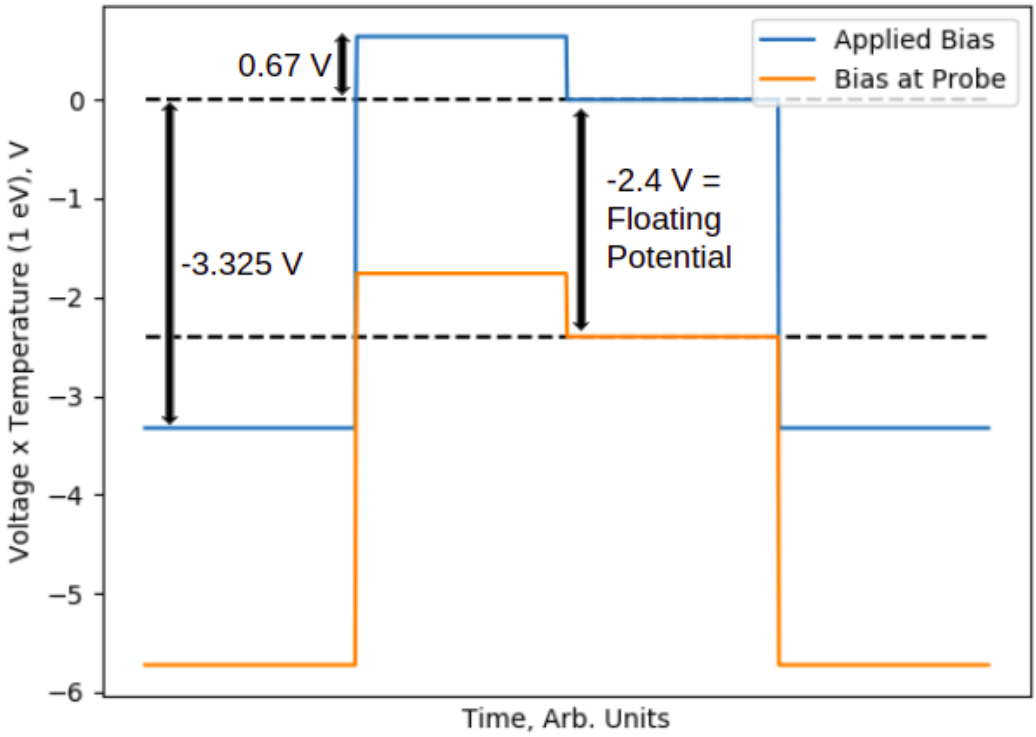


Figure 2.3: A plot of the typical voltage bias waveform highlighting the difference between the applied bias and the voltage measured at the probe for a floating potential of -2.4 V

This means that all voltages that are applied to the probe have the addition of the value of the floating potential added to them through the use of external (to the FPGA) electronics. Such that the applied bias measured at the probe tip can be shown as:

$$V_p = V_{[+,-,0]} + V_c \tag{2.2.8}$$

Where $V_{(+,-,0)}$ is the product of the measured electron temperature of the plasma and the values laid out by Equation 2.2.6 and Equation 2.2.7 that is formulated to return equal magnitude positive and negative currents. V_c is the true floating potential if the net current through the capacitor is zero such that $V_c = V_f$.

2.3 Python Simulations

Now that the framework of the algorithm is laid out, a python simulation can be developed that attempts to replicate the function of the algorithm across a range of data variation. It is important for this purpose that 3 main things be considered in such a simulation:

- The equations must be solved sequentially with each new value contributing to the proceeding calculation.
- The Red Pitaya's ADC and DAC operate with a 14-bit precision. Hence, all calculations using inputs can be simplified to 14 bits. A comprehensive Python simulation should also take into account bit limits to prevent issues with overflows or rounding errors. This will naturally induce maximum values for every used parameter.
- Given that the bias range is dictated by a calculated temperature, the system must be protected from the temperature shrinking to a small value. As this will approach the noise floor where there may be very little difference between the value of currents in all 3 states. This will prevent the device from being able to function effectively.

By utilising the information discussed in section 2.2, and by labelling each iteration as an index, k, the solving of the equations can be defined as:

$$I^+_{sat}[k+1] = \frac{I_{V_-}}{e^{\frac{-3.325 \cdot T_e[k] + V_f - V_f[k]}{T_e[k]}} - 1} \tag{2.3.1}$$

$$T_e[k+1] = \frac{0.675 \cdot T_e[k] + V_f - V_f[k]}{\ln\left(\frac{I_{V_+}}{I^+_{sat}[k+1]} + 1\right)} \tag{2.3.2}$$

$$V_f[k+1] = 0 \cdot T_e[k] + V_f - T_e[k+1] \cdot \ln\left(\frac{I_{V_0}}{I^+_{sat}[k+1]} + 1\right) \tag{2.3.3}$$

In order to solve the exponential in Equation 2.3.1 and the natural logs in Equation 2.3.2 and Equation 2.3.3, a Look-up Table (LUT) in implemented. This is the quickest way to solve a complex mathematical operation in an FPGA. By computing the equation with small steps and saving the results to a form of ROM on the FPGA, the results can be "looked up" by passing the table the variable that is changing like a co-ordinate. This can then be read out back to the FPGA without actually performing the calculation in real time.

An example of a look up table (LUT) can be seen in the perspective of the ion saturation current. A look-up table would need to be used to solve e^x regardless, so by combining it in the completed form one can simply treat the equation as a co-ordinate system.

Given that all values must be unsigned, it is pre-programmed through the use of ROM that if a value is passed to this LUT, it will return the result of the equation. To maximise resolution, since naturally with exponential many values will either be very high or very low, scale factors by some power of two can also be applied to set regions. This allows the FPGA to know for example, if it sends an x value of between 7 and 9, the result is 2^8 times larger than the true result.

This applies for the other regions by the values specified in Figure 2.4. The same process applies to also the temperature and the floating potential to return the value of the natural log in both cases. This is implemented to save processing time.

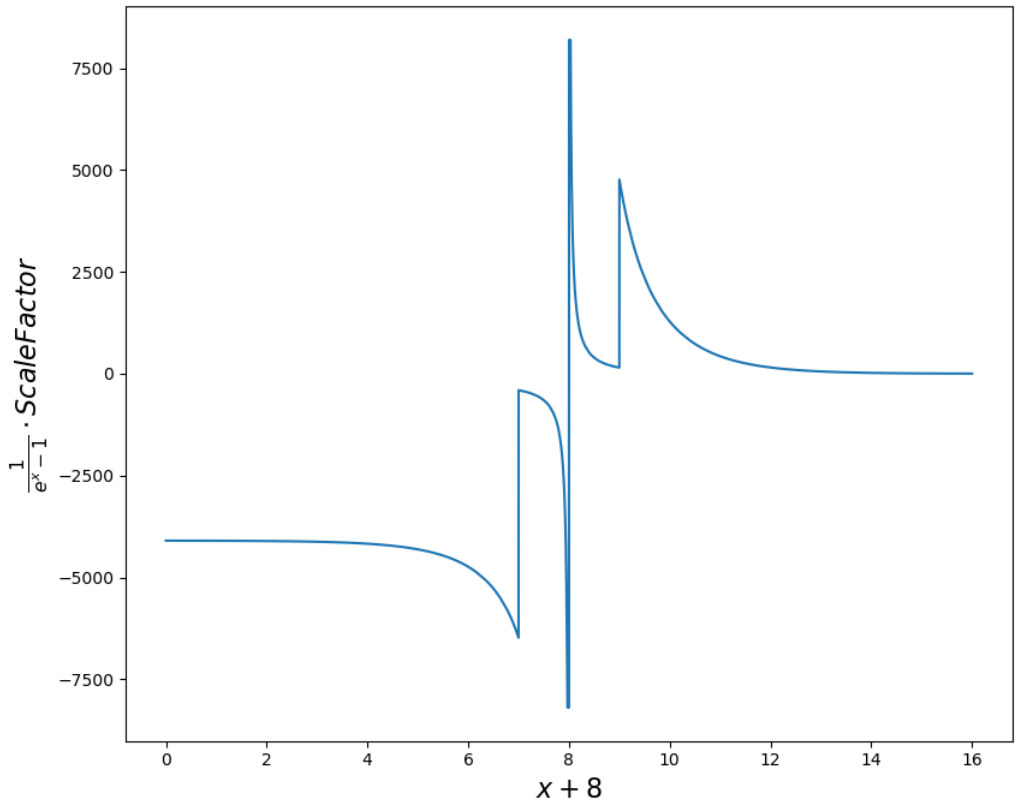


Figure 2.4: A python generated look-up table that solves a 1 over exponential function. By requesting a data point in the x-axis returns the result of the equation in the y-axis. Different regions have different scale factors to increase the resolution. Scale factors are as follows: $\lim_{7\to 9} f(x) \cdot 2^8$; $\lim_{0\to 7} f(x) \cdot 2^{12}$; $\lim_{9\to 16} f(x) \cdot 2^{13}$

The Red Pitaya uses a 14-bit Analogue to Digital Converter (ADC) and Digital to Analogue Converter (DAC) which limits the precision of all digital mathematics that takes place using data input into the device. Hence it seems sensible to limit all values that use inputs to the device are limited to 14-bit numbers. This is important to define the original parameter range for the whole system.

In Table 2.1 the parameter ranges of both a low temperature and high temperature system have been defined, along with the closest encompassing bit values that could be represented in a binary number.

Table 2.1: The required parameter ranges in two distinct plasma regimes and the corresponding bit shift that is required to cover that range in the highest precision

Plasma Type	Ion Saturation Current	Electron Temperature	Floating Potential
Low Temperature Magnetron	20 mA $2^{-17} = \pm 62.5mA$	5 eV $2^{-9} = \pm 16eV$	-20 V $2^{-7} = \pm 64V$
MAST-U	2 A $2^{-12} = \pm 2A$	50 eV $2^{-7} = \pm 64eV$	-150 V $2^{-5} = \pm 256V$

Another key aspect of a comprehensive simulation will be to take into account capacitive effects. Which can be done by splitting each bias state into smaller sections and calculating the resulting potential across the capacitor according to either the charging capacitor equation (for the zero to negative and negative to positive bias states):

$$V = V_0 e^{-\frac{\tau}{RC}} \tag{2.3.4}$$

With V_0 being the desired potential, τ as the time the capacitor has been exposed to V_0, and RC being the series resistance and capacitor respectively. During the transition between the positive and zero states, the capacitor is not charging, it is discharging, so a variation of the equation must be used:

$$V = V_0(1 - e^{-\frac{\tau}{RC}}) \tag{2.3.5}$$

The affect of different value capacitors can be seen in Figure 2.5. It clearly shows that capacitors effectively act like frequency filters to signals. It can be seen that having a low value capacitor allows the signal to pass through the capacitor with the capacitor effectively acting like a wire. However, too large of a capacitor causes the signal to get attenuated as the capacitor does not have long enough to charge so the desired voltage is the potential difference across the capacitor plates.

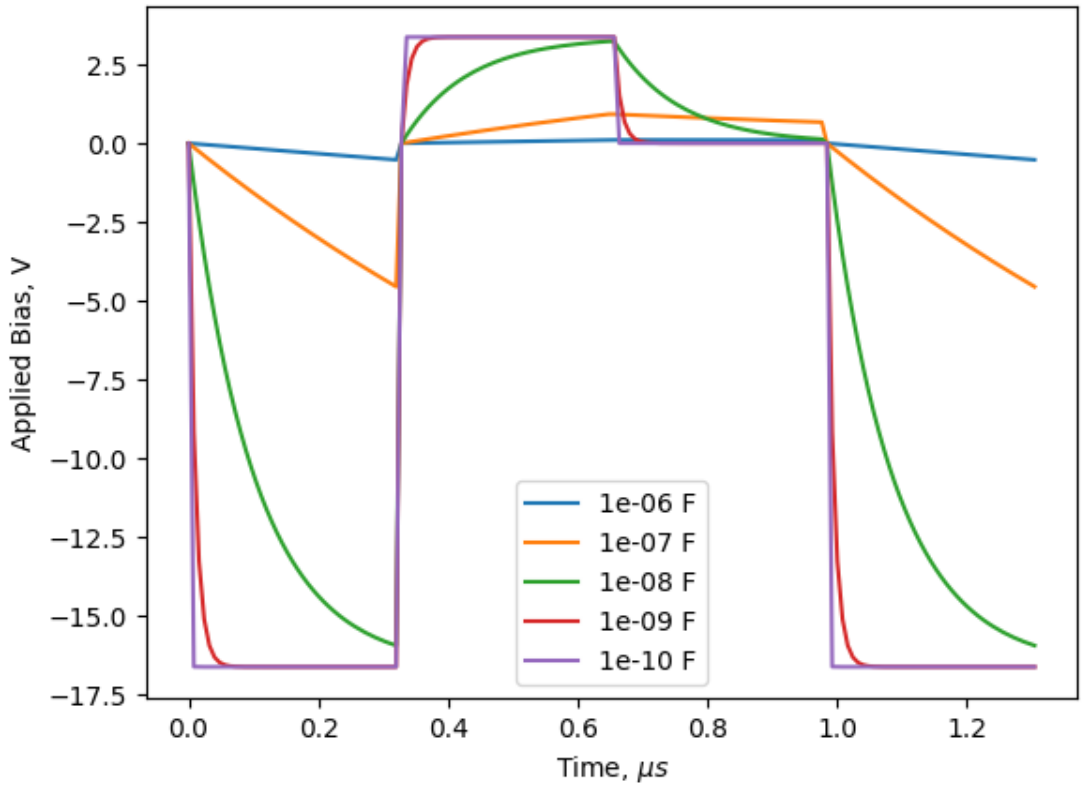


Figure 2.5: A 3 state switching bias waveform with the associated capacitive effects of a range of capacitor values.

From an electronics perspective, this frequency filtering can be considered a low-pass filter that has a cutoff frequency that can be defined by:

$$f_c = \frac{1}{2\pi X_c C} \tag{2.3.6}$$

Where X_c is the capacitive reactance, which is the frequency dependant resistance of the capacitor and C, the capacitance. Solving Equation 2.3.1, Equation 2.3.2 and Equation 2.3.3 as described causes each result to converge closer to the best fit. By programming a current response function that returns the current of a given voltage with pre-determined jSat, T_e and V_f this can act as a simulation for a plasma. A true test of this algorithm will be to induce some perturbation to each parameter and check that the algorithm successfully follows the input. This can be seen clearly in Figure 2.6 with each of the 3 parameters given a different frequency perturbation. To which each is successfully tracked by the algorithm.

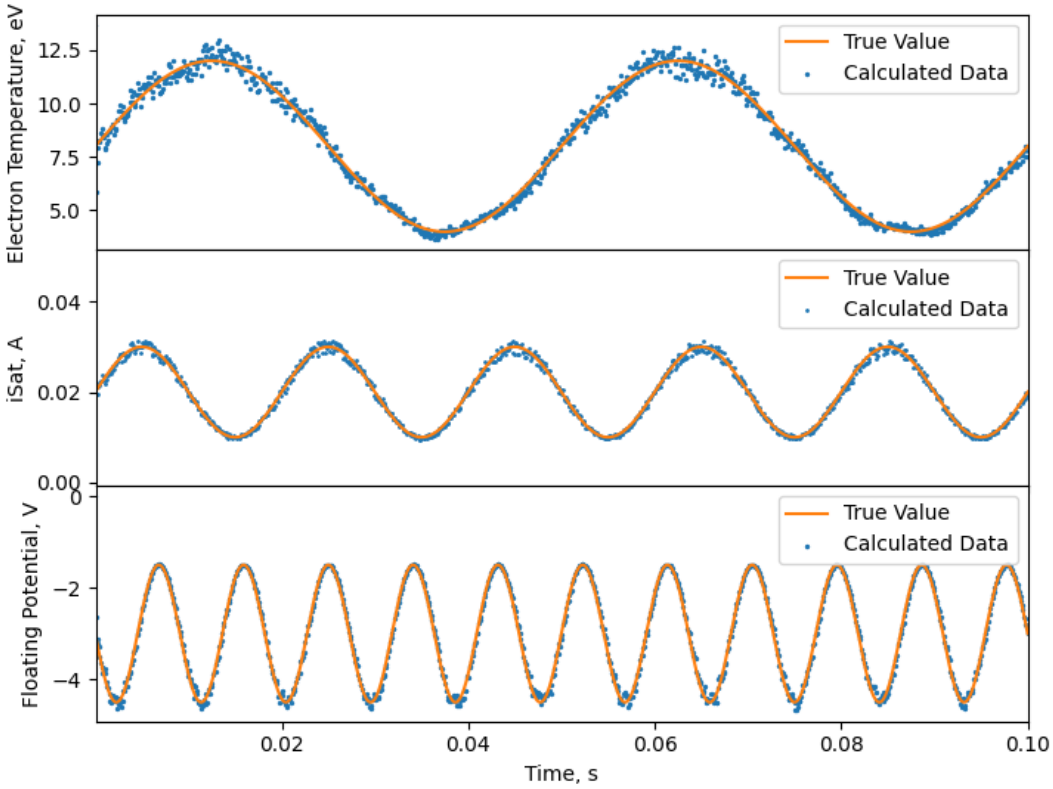


Figure 2.6: Figure showing a sinusoidal variation in the 3 main parameters and how the simulation is able to keep track with no prior knowledge of the true values.

2.4 Digital Hardware

As briefly discussed in section 1.4, FPGA's are the perfect device for this particular application due to their high capacity for pipelined and digital processing. In particular the STEMlab 125-14 Red Pitaya [94] is a powerful and off-the-shelf available instrument that contains a Xilinx Zynq 7010 FPGA chip along with a Dual-Core ARM Cortex-A9 MPCore processor and 512MB of onboard RAM. It also is capable of ethernet connectivity and duel 14-bit RF input and outputs at clock speeds of 125 MHz. It also has extension connectors to facilitate digital control via the use of GPIO pins.

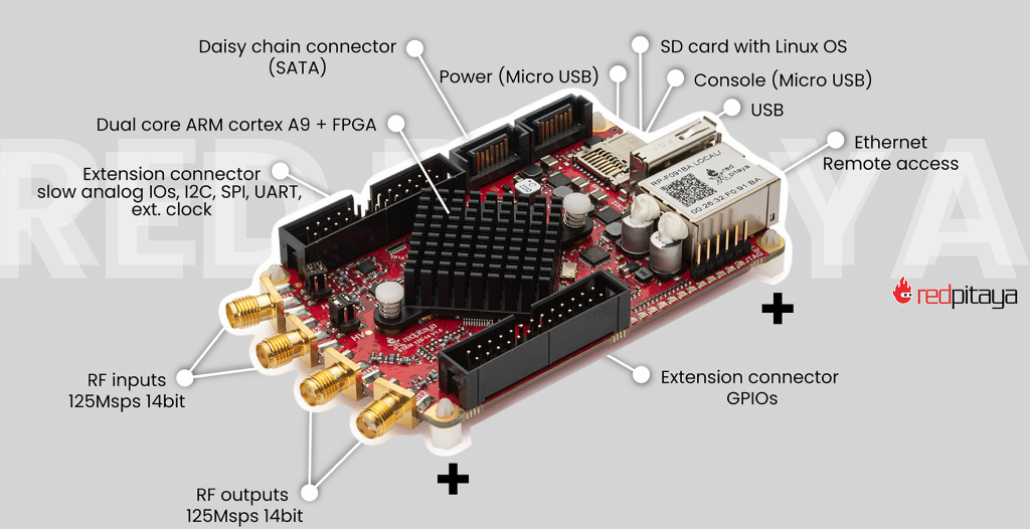


Figure 2.7: A Red Pitaya from STEM-Labs, equipped with a Zynq-7000 FPGA chip [94]. Image from [95].

A main benefit of the use of a Red Pitaya is that it comes supporting the Koherson framework. As briefly discussed in subsection 1.4.3, Koheron SDK is a powerful framework for developing instruments. Through the use of standardisation the package consists of a number of a configuration files, drivers and unique FPGA IP.

2.5 FPGA Design

In this section some of the specifics about the FPGA design will be discussed, with specifics such as the individual function of each FPGA core and the data flow through the system.

The data flow of the FPGA design can be seen in Figure 2.8. There are some cores that oversee all other processes in the design, which can be seen at the bottom of Figure 2.8. The Rst as described in Table 2.2, handles the reset signal for the whole device. If reset is active, the device is in idle mode and all variables are initialised. The FET Drive over arches the whole system dictating what bias state it currently sits in. It is also always active, switching between bias states in the predefined order of; negative, positive and zero. If in a negative state, a negative bias multiplier will be applied to the temperature and the iSat core will be allowed to calculate. The same can be said for the positive state and the Temp core and the zero state and the vFloat core. This can be

broken down into a series of events as follows:

1. The UFLP generates a bias based on its currently calculated temperature paired with the bias state given by FET Driver. For the first cycle this is a guess of a large temperature. This is to ensure a large bias range is collected on the first cycle.

2. The signal, now of the form shown in Figure 2.3, gets amplified. This is because the voltage and current supplied by the Red Pitaya are not sufficient to drive the probe.

3. The signal passes through the capacitor bank, which will only have certain capacitors active. Capacitors are carefully selected so the signal passes with very little resistance. The starting state is to have all capacitor channels open to ensure no signal attenuation.

4. The signal reaches the probe and the probe draws a current roughly approximated by Equation 1.3.23.

5. The current and voltage at the probe tip are measured. If the temperature guess is accurate the magnitude of current in both positive and negative should be equivalent. The voltage measured here should be the applied voltage plus the floating potential.

6. Measured current and voltage are passed into the Data Acquire core where they are calibrated in offset and scale.

7. Depending on the state of FET Drive, one of the 3 calculations will take place.

    - The output of the temperature core is provided to the Bias Set core to apply the next set of biases to the amplifier
    - The output of the iSat core is provided to the Cap Switch core to ensure the correct capacitor is selected

8. The output of each 3 calculation cores is sent to the FIFO and can be collected by the Python API, which will be further discussed in section 2.6.

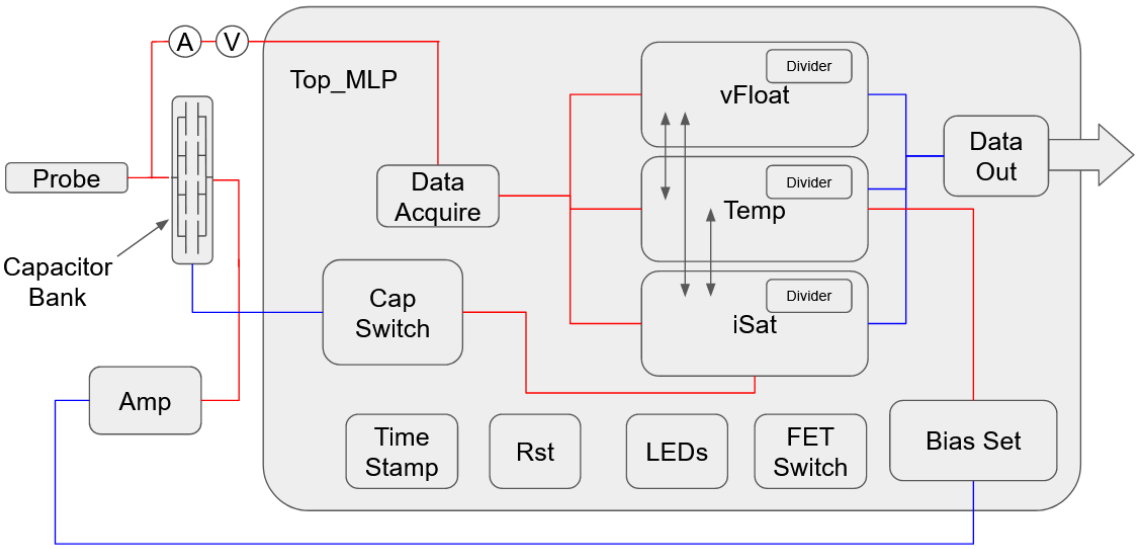


Figure 2.8: Top level FPGA design for the UFLP with blue lines representing UFLP outputs and red lines representing inputs or internal signals in the FPGA.

Table 2.2: The inputs, outputs and function of each individual core that builds up the FPGA architecture for the UFLP

Core	Function
Reset	Generates the reset pulse for all cores. If reset button is activated a reset is pulsed for a given amount of time. Reset Hang holds the reset state so it can be sent to an external LED.
Time Stamp	Generates a timestamp for the data set
Data Acquire	Handles direct data acquisition from the ADC. Scales the values received by appropriate calibration values before forwarding it to other cores.
Data Out	Calibrates final data outputs before they leave the DAC. Available for transmission to other systems via coaxial output if required (e.g. control systems or trigger for other device)
FET Switch	Generates the positive, negative and zero bias states for the given number of clock cycles and passes the states to all cores that require them.

Cap Switch	Uses calculated Ion Saturation Current to change the capacitors to optimise floating potential and current balance.
Core	Function
iSat	Solves for ion saturation current using current measured in a negative bias state using previously calculated electron temperature and floating potential
Temp	Solves for electron temperature using current measured in a positive bias state using previously calculated saturation current and floating potential. Outputs the temperature to the bias_set core to set the dynamic bias range for the following iteration.
vFloat	Solves for floating potential using current measured in a zero bias state using previously calculated saturation current and temperature. Measures the average current in this state and outputs to data_acquire, this is subtracted as an offset to ensure a 0 current state in the following iteration.
Bias Set	Sets the output bias based on the calculated temperature depending which bias state the device is in. If dynamic is enabled, device will use calculated temperature, if not it will use a static Python input using input triple probe temperature. A single temperature is used for a completed 3 bias state, triggered by the signal change bias out.
Data Collect	Sends the data to the RAM on the red pitaya. Collects 1 data point per completed cycle, a single binary number containing all information of the desired output mode. Operation has 4 modes, Voltage/Current, iSat/Temp/vFloat, Current/AvrCurrent and iSat/CapacitorValue. These modes are 0-3 respectively.
Divider	Performs a goldschmidt division algorithm using numerator an denominator inputs for a fixed number of clock cycles. Full algorithm detailed in subsection 2.5.1.

2.5.1 The Goldschmidt Division Algorithm

Division in fixed point operations in an FPGA is incredibly computationally expensive and often takes many clock cycles to complete unless it is by a power of 2. Given Equation 1.3.23 the use of a division is also a necessity. Often in digital systems the best way to compute a division is through the use of a Look-up Table (LUT). A lookup table allows pre-programmed results to be looked up by treating the denominator and numerator as co-ordinates. An example of this can be seen in Figure 2.4, where the ROM can return of an equation by inputting the variable that has been changed. This works very well for a fixed value division (e.g. $\frac{1}{x}$ or $\frac{x}{3}$) but if both values are variable this can use a large amount of storage resources. It is also possible to multiply by a fraction by ensuring the denominator is a power of 2 number, for example to divide by 5 one could first multiply the value by 205, then perform a bit shift operation by divide by 2^{10}:

$$\frac{205}{2^{10}} = 0.2002 \tag{2.5.1}$$

This is as computationally cheap as a simple multiplication, as a division by a power of 2 is just a bit shift which only takes a single clock cycle. The difficulty of a digital division can be explained algebraically by imagining two 14-bit numbers, A and B. Adding them would result in a 15-bit number such that

$$A[14bit] + B[14bit] = X[15bit] \tag{2.5.2}$$

If one was to multiply A and B it would result in a 28-bit number such that

$$A[14bit] \cdot B[14bit] = X[28bit] \tag{2.5.3}$$

But conventionally the way to divide A by B is to multiply A by one over B such that

$$A[14bit] \cdot \frac{1}{B[14bit]} = X[Ybit] \tag{2.5.4}$$

Where Y can be technically infinite depending on if $\frac{1}{B}$ returns a rational number. The issue is that $\frac{1}{B}$ requires a division by necessity unless B is a fixed value constant, as described above, hence a division algorithm will have to be used. While vendors such as Xilinx have lots of custom IP to perform divisions, these often take a fixed number of clock cycles. The default Xilinx IP takes over 40 clock cycles to perform the division.

More clock cycles results in a more precise answer as division algorithms are convergance algorithms. However, in many cases the results could be to a high accuracy long before algorithm returns a valid signal. By building my own division algorithm I can customise the number of clock cycles it requires in an attempt to increase the output time resolution at the cost of overall accuracy.

The Goldschmidt Algorithm [96] is an iterative algorithm that is used that multiplies both the numerator and the denominator by a common factor, F. This causes the denominator to converge to 1 and the numerator converges to the result of the division. This is only possible if the common factor is sufficiently small, often less than 1. This can be achieved by expanding the bit lengths of the numerator and denominator (e.g. multiply both by 2^{14}) and the common factor can be divided by a large factor of 2. This will slightly alter the algorithm as the denominator will converge to the new multiple factor and the result will be 2^{14} times larger than it should be. The algorithm can be described by

$$F_0 = \frac{D_0}{2^{10}} \tag{2.5.5}$$

$$N_0 \cdot F_0 = N_1 \tag{2.5.6}$$

$$D_0 \cdot F_0 = D_1 \tag{2.5.7}$$

$$F_1 = 2 - D_1 \tag{2.5.8}$$

Where Equation 2.5.6 and Equation 2.5.7 can be computed in a single clock cycle and Equation 2.5.5 takes a further clock cycle. Each iteration simply increases the index by 1 such that the next iteration would be:

$$N_1 \cdot F_1 = N_2 \tag{2.5.9}$$

$$D_1 \cdot F_1 = D_2 \tag{2.5.10}$$

$$F_2 = 2 - D_2 \tag{2.5.11}$$

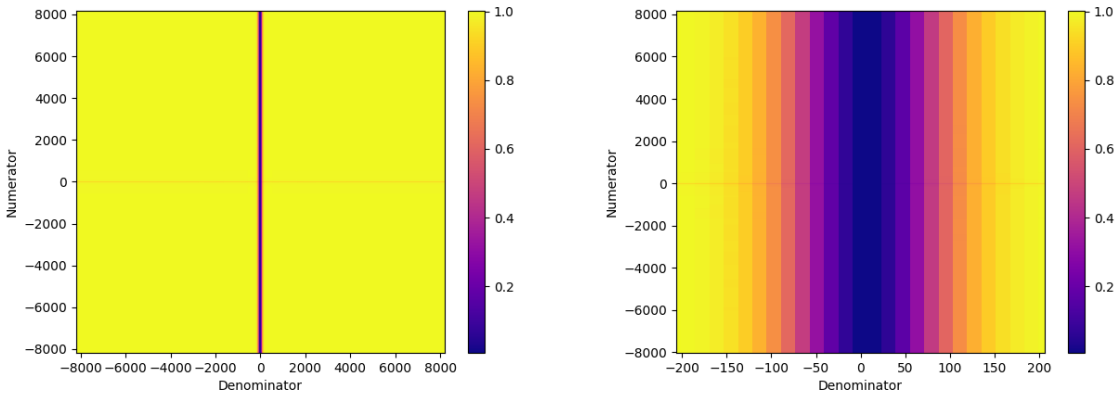
The algorithm causes the value of F_i to converge towards the result of the division as D_n and F_n converge towards unity. In Table 2.3, an example of the algorithm is shown for $\frac{12}{35}$ where $F_0 = D \cdot 2^{-10}$.

Table 2.3: The process of the Goldschmidt division algorithm for the sum of $\frac{12}{35}$ as it converges towards a solution

Index	N	D	F	Deviation from result (%)
0	12	35	0.0341796875	N/A
1	0.41015625	1.196289063	0.8037109375	16.40816327
2	0.3296470642	0.9614706039	1.038529396	-4.007339996
3	0.3423481665	0.9985154856	1.001484514	-0.148672142
4	0.3428563873	0.9999977962	1.000002204	-0.0002203787743
5	0.3428571429	1	1	-0.0000000004856559599
6	0.3428571429	1	1	0

As can be seen the algorithm does fully converge but the deviation is almost immediately very low leaving the result close to the true value. This could be of great benefit for trying to push to device to its limits, as the number of iterations could be limited to trade accuracy for temporal resolution.

The accuracy of the algorithm for a division between two 14-bit numbers can be seen in Figure 2.9. As the value of the denominator approaches zero, the accuracy rapidly diminishes. This occurs for two reasons; firstly the number of iterations is not large enough to reach the results. Secondly, as the denominator tends to zero, the result approaches infinity.



(a) (b)

Figure 2.9: Visualisation of the accuracy of a 14-bit Goldschmidt division algorithm when varying the denominator and numerator values. (a) is the full 14-bit range for both values (b) shows a reduced range in the denominator to show the algorithm fails when trying to calculate large numbers

Since the result is limited to 14-bits this means the difference between the result and the value the algorithm calculates will have a large deviation at very small denominators. This will have to be carefully considered in the design. The two main uses of division is to solve the following in Equation 2.2.1 and

$$\frac{V_p + V_f}{T_e} \tag{2.5.12}$$

and the following in Equation 2.2.2 and Equation 2.2.3

$$\frac{I_p}{I_{sat}} \tag{2.5.13}$$

With respect to Equation 2.5.13, this case should be avoided because I_p and I_{sat} should always be close in magnitude due to the effects discussed in section 2.2. Equation 2.5.12 creates a more complicated scenario as small temperatures could possibly be calculated. However, in order to prevent the MLP algorithm getting stuck in a loop, if a temperature is calculated to be below a bit value of 50 then the initial guess of the system is used. This is to ensure that if a small temperature is calculated, a small bias is not applied, as this could result in measured currents and biases within the noise floor.

2.6 Data Extraction and FPGA Control

A simple method of data extraction exists within the Koheron framework utilising Xilinx IP cores. This can be seen in the block design IP shown in Figure 2.10. By providing a 32-bit signal to s_axis_tdata, each bit value will get saved when s_axis_tvalid is in an on state, which can then be accessed from RAM on the device.

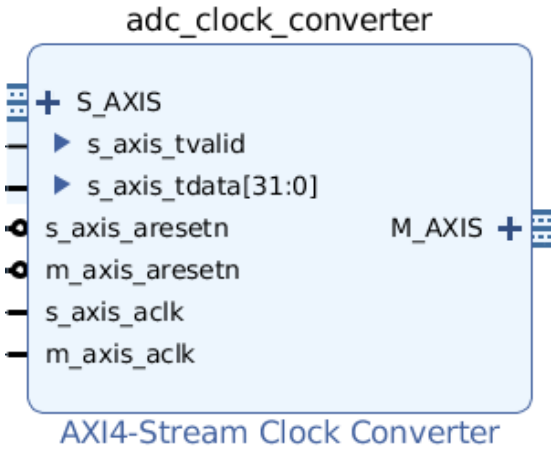


Figure 2.10: Top Level diagram of the AXI4-Stream Clock Converter IP Core available from Xilinx capable of acting as an AXI4 Stream data storage method

In order to fit into the constraints of the 32-bit value, the 3 14-bit values that are stored on the device will have to be sliced and concatenated. This will leave fixed bit values of the output signal corresponding to specific bit values of the requested parameter. Only the most significant bits will be transmitted including the sign bit, to maximise accuracy at the cost of precision. This is shown in Figure 2.11, where both ion saturation current and electron temperature are transmitted with 11-bits and floating potential is using 9-bits.

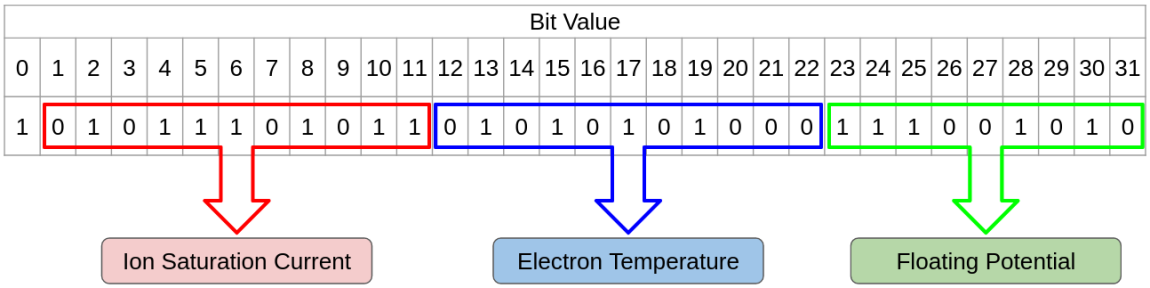


Figure 2.11: How the 32-bit number is divided to contain information about the 3 parameters of interest to be streamed off the device

Note that the full precision values are still being calculated, even if the output result is truncated. This makes the design more adaptable to different FPGA architectures that allow for larger than 32-bit outputs. It is also possible to output a variety of information that is present on the FPGA by replacing the information that is contained within the 32-bit output string. The device is also capable of outputting measured voltage and current into the device, or the current value of the capacitor switching circuit discussed in section 3.1.

As is discussed in subsection 1.4.3, the standardisation of certain generic FPGA architectures can extensively decrease development time. The ADC and DAC core shown in Figure 2.12 is a great example of this.

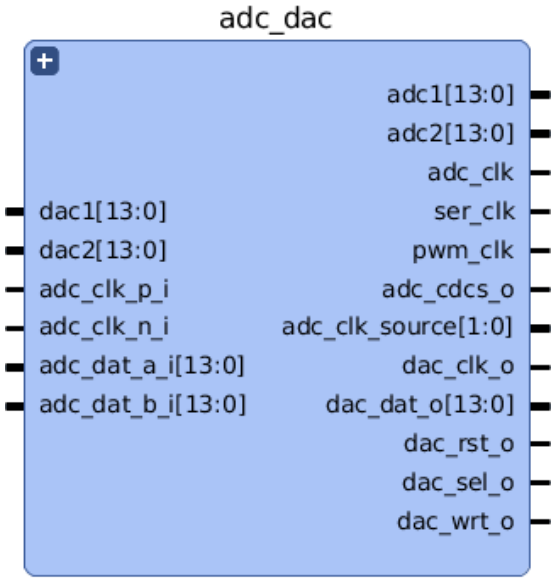


Figure 2.12: Top level diagram from the ADC and DAC block designed by Koheron as part of the Koheron SDK to interface with the ADC and DAC available on the Red Pitaya development board

The standardisation means that the developer does not have to design the data transfer function of the IP and can just use it as a packages solution. The conversion of voltages to bit-values is a very common practice in FPGA design. In addition to the ability to receive and transmit information from the FPGA, its is important to be able to change certain parameters without having to re-compile the device. Another standardised package that is part of the Koheron SDK, is the control register. A top level diagram can be seen for this in Figure 2.13.

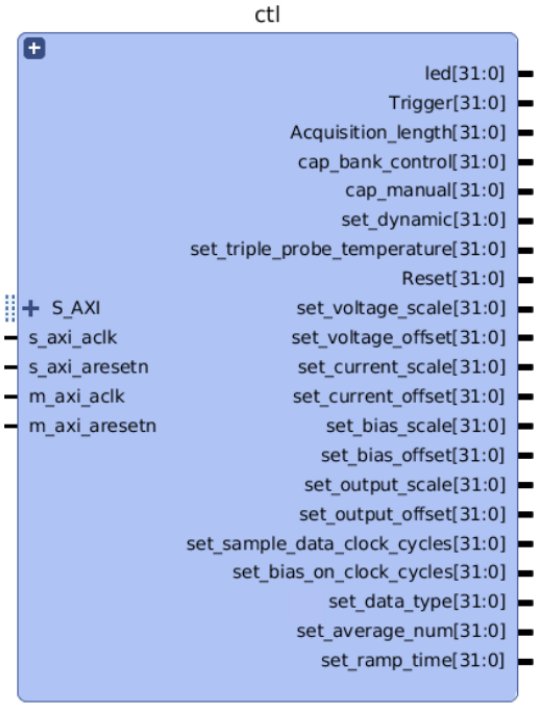


Figure 2.13: Top level diagram of the Control block designed by Koheron to allow the user to control variable to the FPGA pins during operation through the use of C++ drivers and the Python API

This allows the user to define external inputs directly into the FPGA which can be changed in the field via the use of the Python API or web API. This allows a simple implementation of things such as:

- Fully customisable acquisition time and operating frequency
- Simple function to change between triple probe and dynamic voltage modes
- Changing the output values in the AXI4 data stream (Figure 2.10 to allow for plasma parameters, voltage/current or current/capacitor.

- Adjustable ramp time of the voltage waveform to minimise the current spikes due to the shock due to a changing voltage through a capacitor
- Input and output calibration in both scale and offset so a manual calibration can be performed with the use of a fixed signal and an oscilloscope
- External signals for triggering and reset

The existence of such control modules allow for changes to be applied to critical parts of the FPGA architecture with a single line of Python code. This also has room for development to add in new control signals for potential improvements such as increased number of data points or larger dynamic bias range.

Alongside the control register there is also a status register that can be built to have the same functionality but monitor certain variables within the FPGA architecture. This can be useful for monitoring steady state variables without calling the whole data stream.

2.7 System Testing

In order to test the FPGA design effectively before implementation onto a device it is important to generate a test signal of a known parameters and test the efficacy the FPGA. A simple and effective way to do this is to design a second FPGA that simulates the function of a plasma. It simply has a known ion saturation current, electron temperature and floating potential and outputs a current based on an applied voltage.

As can be seen in Figure 2.14, two Red Pitayas can be connected together to allow a transfer of data. One Red Pitaya, the Ultra Fast Langmuir Probe (UFLP), solves the planar probe equation as described in section 2.2. It also generates a bias range based on its calculated electron temperature value. The other Red Pitaya, the current response, effectively simulates a plasma by solving the original form of the planar probe equation to output a current.

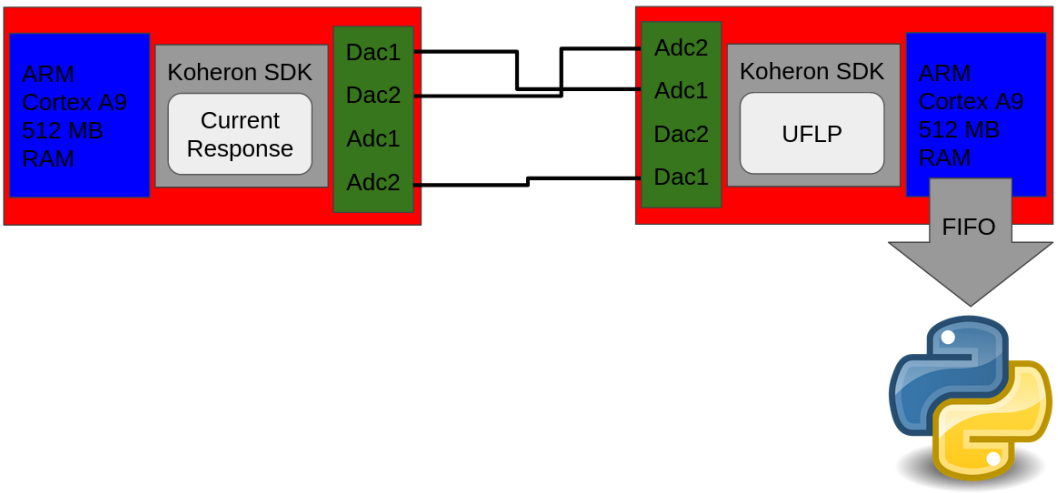


Figure 2.14: Two Red Pitayas communicating via connection of ADC and DAC ports. This allows the two systems to remain isolated for effective simulation of a real world plasma system.

It also outputs the original input bias from the UFLP plus the floating potential. This effectively simulates the effect of a fully decoupled capacitor system, where the signal from the UFLP passes freely to the probe, but the floating potential of the probe transmits zero current back to the UFLP. This effect is illustrated in Figure 2.3.

This mode of testing has 3 significant drawbacks in comparison to a physical system;

- The value of the floating potential added to the bias voltage is an example of a perfectly decoupled system. This may not be true in every plasma scenario, as rapid changes in the floating potential that may cause stray current to pass the capacitor affecting the data output.
- Given the current response unit has to also solve a division, as described in subsection 2.5.1, it will take a significant amount of time to return a current for an associated voltage. This is something that will usually be considered instantaneous in a real plasma, but effectively halves the maximum frequency output in this simulation.
- It is impossible to synthesise truly random numbers (and hence, data noise) in an FPGA system. While a low level (approx 5%) has been implemented in the following simulations, this is from a known seed of random numbers. Hence, there could be

a case where it works for the random seed that has been selected but not for any random seed.

Considering these drawbacks it is still the most effective way of testing the system before exposing it to a laboratory setting. To address the above issues, if the capacitor is not effectively decoupling as it should due to a fast change in floating potential, the algorithm will fail to converge accurately regardless. There are ways to address the second point, such as implementing a look up table, but this makes the system even more so just solving a singular case, as there will be no variation in output.

This would effectively make this physical Red Pitaya simulation fall back into effectively a Python simulation. The third point cannot truly be addressed other than the fact a real world system, by definition, will experience real world noise sources from other electrical objects in its vicinity. This point ultimately will have to be addressed in real world plasma testing.

As can be seen in Figure 2.15, by applying a perturbation to the electron temperature, like in section 2.3, the UFLP is shown to accurately follow the perturbation. It should be noted that in testing there are issues if any parameter gets too close to the edges of its designated range, this is likely due to an overflowing error where the Goldschmidt algorithm cannot calculate the result to a high enough precision due to a very large numerator or a very small denominator. But ultimately this shows that is the parameter ranges are selected effectively, then the algorithm does converge as it is designed to and gives fast and accurate data output.

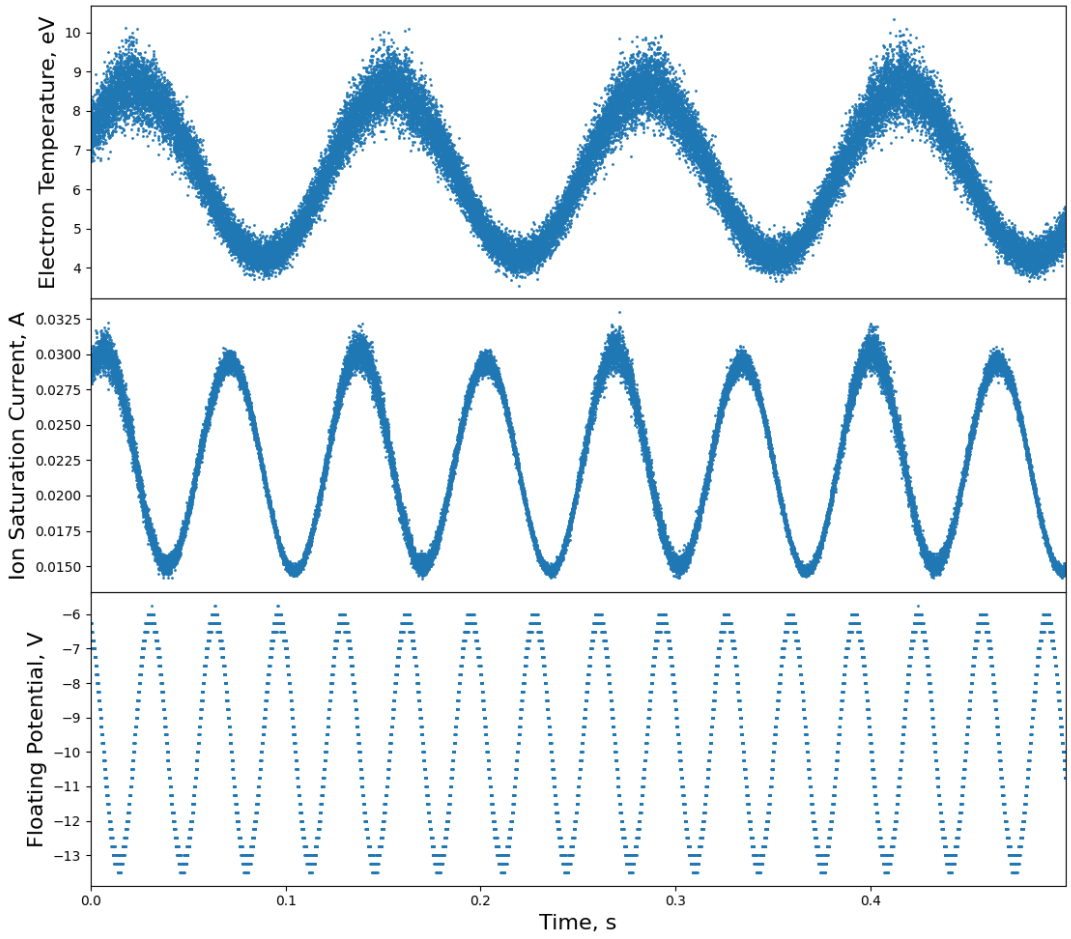


Figure 2.15: Results from running calculation based on PCR input within the UFLP, running at 80 kHz with the same sinusoidal variation used in the Python simulation

The maximum temporal resolution that could be achieved from this method was of the order of 200 kHz, which suggests the UFLP acting alone should be able to operate in excess of 200 kHz. Which would be a sufficient speed to be able to diagnose both filaments, however spokes may still be too fast to be appropriately resolved.

In addition to the given testing, functionality was built to also output the measured ion saturation current and the calculated optimal capacitor combination. The optimal capacitor combination is then sent to activate the relative GPIO pins and the capacitor value is returned. The capacitor value is designed to scale linearly with measured current, such to not attenuate the signal and provide maximum resolution on the floating potential. Since this operates in a binary switching circuit the capacitor values are also quantised. The results can be seen in Figure 2.16.

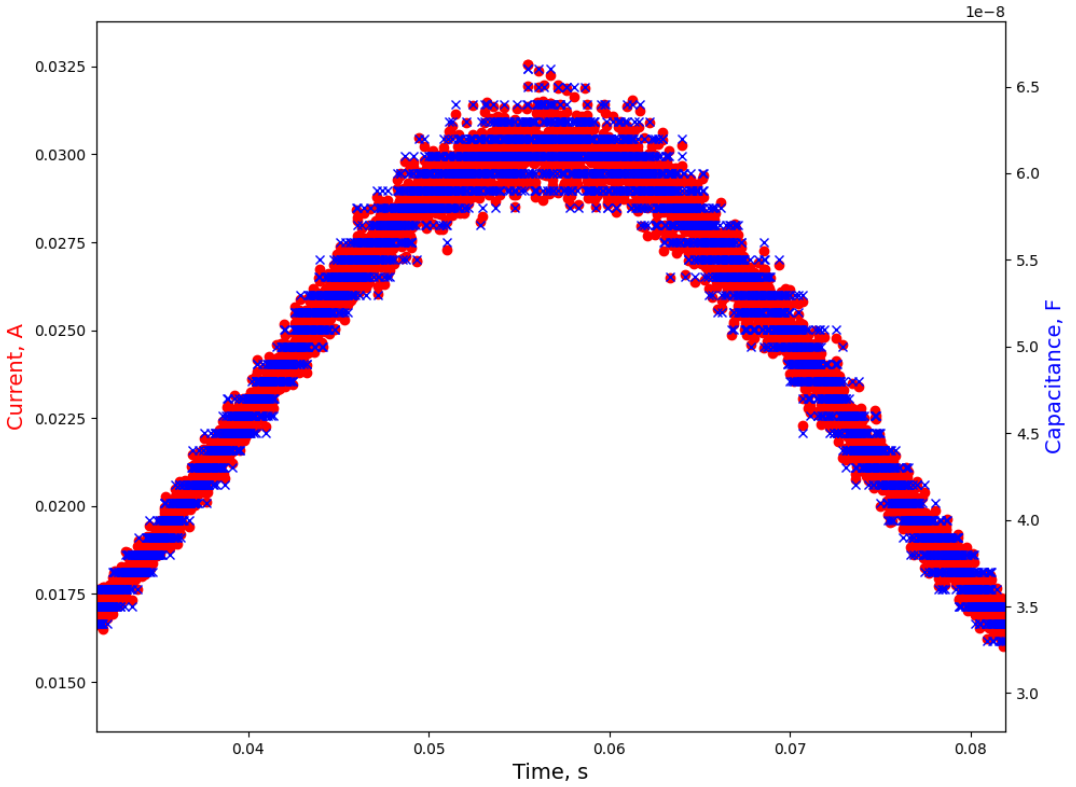


Figure 2.16: Results from returning the output of the current and capacitor value for a small section of the same waveform seen in Figure 2.15. Shows a clear tracking and quantisation of the capacitor values based on the measured current values

In conclusion this form of testing has successfully proven that the algorithm implemented into the FPGA is working as intended. The algorithm correctly converges on an appropriate time scale to track a change in all three desired parameters, purely from a digital perspective. This can give confidence that the FPGA will continue to function as expected as a physical implimentation is developed.

Chapter 3

Electronics for FPGA Interface

While the last chapter mostly focused on the simulation and execution of the MLP algorithm, this chapter will address the real world considerations for such a system to be implemented.

3.1 System Requirements

Different from the system requirements laid out in section 2.1, the system requirements here are imposed on the physical aspects of the system such as the FPGA and electronics. Fundamentally we will break these requirements down into three main areas:

1. The Langmuir probe
2. The electronic components and design
3. The FPGA-electronics interface

The Langmuir Probe

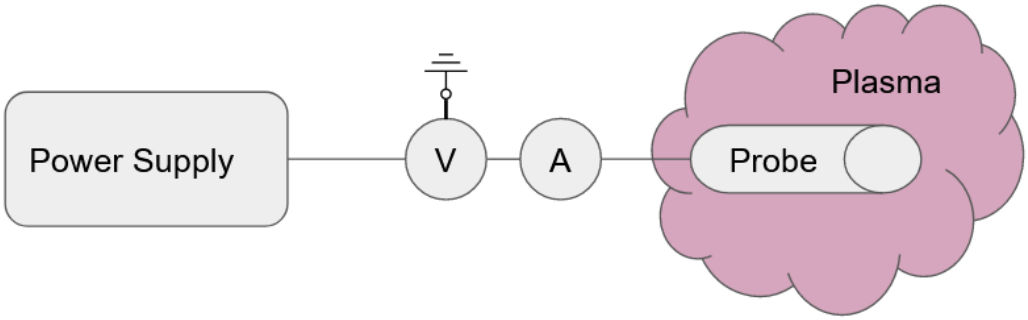


Figure 3.1: A simple probe setup consisting of a power supply, a probe exposed to a plasma and a way to measure both the current and the voltage at the probe tip

Fundamentally this system requires a simple Langmuir probe as shown in Figure 3.1. This can be defined as an electrically conductive object of known area in contact with a plasma that has a range of known biases applied to it. The current at each bias is recorded to form an IV response described in subsection 1.3.2. There are two substantial differences that have profound effects on the design of this probe system:

- The introduction of a capacitor between the power supply and measurement of current and voltage
- The application of a high frequency voltage to the probe

Firstly, capacitance must be considered. Previously the cut off frequency related to a given capacitor has been defined by Equation 2.3.6. Knowing that capacitors have a frequency dependant resistance, the total resistance can be defined by the equation:

$$R_{tot} = \sqrt{R_{shunt}^2 + X_c^2} \tag{3.1.1}$$

Where R_{shunt} is the resistor in series with the capacitor and X_c is the capacitive reactance, which can be defined by re-arranging the original cutoff frequency equation as:

$$X_c = \frac{1}{2\pi f C} \tag{3.1.2}$$

Where f is the applied frequency and C is the capacitor. This equation explains that the resistance of a capacitor is inversely proportional to the frequency of the signal applied. By utilising Equation 3.1.1 and Equation 3.1.2 and substituting them into Ohms law, $V = IR$:

$$I = \frac{V}{\sqrt{R_{shunt}^2 + X_c^2}} \tag{3.1.3}$$

It can be seen that as capacitive reactance increases, the current flowing through the capacitor decreases. This can be thought of as a current limiter that is putting a cap on the maximum amount of current that can flow through the capacitor. Hence, the value of the capacitor must be chosen with respect to the amount of current that the probe may be subjected to, to ensure that there will be no attenuation of the current in the system. In an ideal world the capacitor will be arbitrarily large so as to never attenuate the current.

Alternatively, Equation 3.1.2 also describes the relationship between the plasma and the capacitor. If there are only small frequency variations in the value of the floating potential, the total reactance will be sufficiently high forcing zero current according to ohms law, effectively blocking the signal. For there to be zero current, the capacitor must be charged to the floating potential in this state. However, if there are variations in the floating potential on the timescale of approximately $2\pi RC$, current will pass the capacitor and the current measured at the probe will not be truly described by Equation 1.3.23. This can be mitigated by having the smallest value capacitor possible so that the charge time of the capacitor is very low, $t = RC$.

Given the two conflicting ideas addressed, the current attenuation dictates as large a capacitor as possible. But, tracking the floating potential requires a small capacitor. The ideal scenario is then to measure the magnitude of the current and ensure a capacitor that can only just allow that current to pass is selected. This will maximise the frequency response of the floating potential.

This however does highlight an issue, that there are scenarios where the floating potential is moving with a high enough frequency and the plasma is so dense that too much current is being drawn. Figure 3.2 helps to explain this issue in that there are two different scales. If the current required by the plasma is higher than the current line,

the measured current will be attenuated. If the variation in floating potential is faster than the cut off frequency, it will not be blocked and will transmit a current across the capacitor according to Equation 3.1.5.

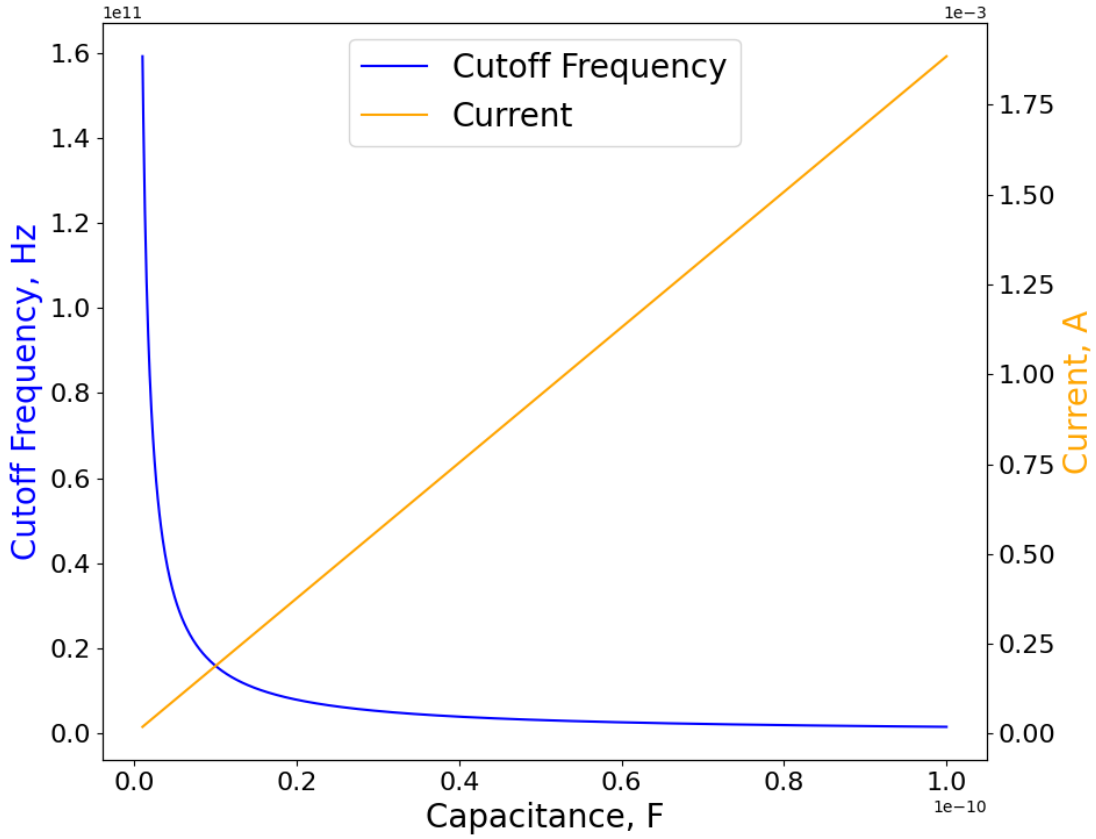


Figure 3.2: The variation of maximum current that can pass a capacitor against the cutoff frequency of the capacitor

The second issue that must be addressed concerns applying a high frequency signal to a long cable. This effect is called cable capacitance and it is also described via Equation 3.1.2. Given that a coaxial cable is a live core surrounded by a grounded sheath, this forms the basis for an electrical field to form between the two due to a difference in potentials. This field can be minimised by increasing the diameter of the cable (distance between the core and the sheath) or by the ground taking a completely different return path. Both of these cause large issues to do with cable impedance which will have more of a negative effect than that of the capacitance, so they will be ignored as solutions. The existence of this electric field effectively means that there is a small capacitor bridging the live core to the ground sheath. This is described by the circuit diagram in Figure 3.3.

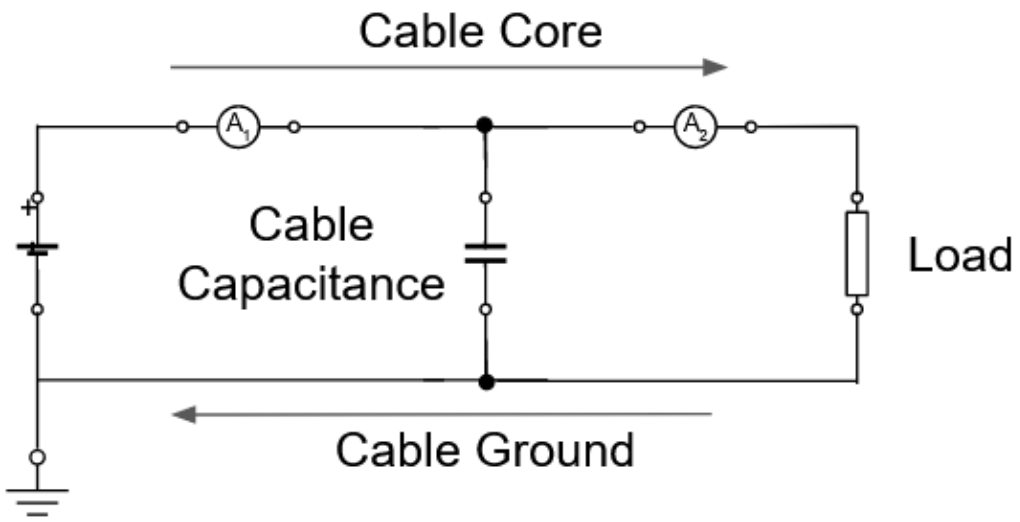


Figure 3.3: Simple circuit diagram illustrating the effect of cable capacitance in a coaxial cable showing current monitors in positions A_1 and A_2

Cable capacitance is generally of order of 10's of picofarads per meter (pFm^{-1}), which are very small values of capacitance. From Equation 3.1.2, it can be seen that small values of capacitance will result in a very large capacitive reactance. So at a fixed frequency of 3 MHz with 1 meter of 10 pFm^{-1} cable the reactance across the capacitor will be:

$$X_c = \frac{1}{2\pi \cdot (3 \cdot 10^6) \cdot (10 \cdot 10^{-12})} = 5305\Omega \tag{3.1.4}$$

A termination load of a coaxial cable of infinite length is generally 50 Ω, hence 99% of the current will flow through the load. It is easy to see how this quickly becomes a significant value flowing directly to ground via the cable capacitance if the frequency is much higher or if the cable is much longer (the capacitance is much higher). In a low temperature configuration at the University of Liverpool, less than a meter of cable can be achieved so cable capacitance will not be a large issue, but for implementation onto MAST-U, many tens of meters of cable will be required.

This issue can be solved however with the implementation of a dummy probe to counteract the additional current within the circuit. This solution is shown in Figure 3.4.

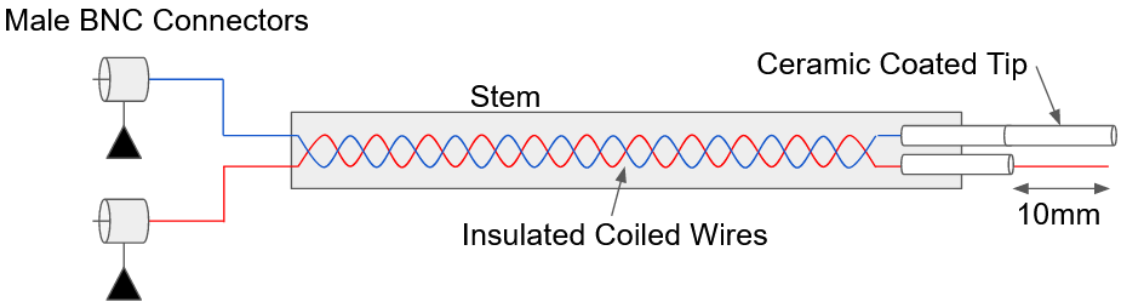


Figure 3.4: Schematic of the design of a Langmuir probe stem that both has a regular Langmuir probe but also a dummy probe that is electrically isolated from the plasma.

By having an identical Langmuir probe that follows the same path through space, that has identical cables both in length and specification, it can be seen that if the same signal is applied to both the cable capacitance reactance must match. The only difference being that the dummy probe is only exposed to the load of the cable, but the real probe has the resistive response of the plasma. From a mathematical perspective when you induce a changing voltage to a capacitor, a current will flow. Such that:

$$\frac{dV}{dt}C = I_{cap} \tag{3.1.5}$$

If Equation 3.1.5 is applied to both the dummy and real probe, the real probe will measure a current of $I_{cap} + I_{plasma}$ but the dummy probe will only measure $Icap$. By subtracting the dummy probe current from the real probe current, the true current as a function of the applied voltage in a plasma can be derived.

Considering all of the effects discussed previously, along with the system requirements considered for a simulation in section 2.1, a comprehensive list of requirements can be formed.

1. Ability to measure currents and voltages with bandwidths exceeding a few MHz and within specified ranges.

2. Capacitor values carefully matched to the range of densities (and size of probe tips) that are expected to be measured and must be able to change mid-operation to ensure no attenuation of current

3. Implementation of a dummy probe system to account for cable capacitance.

4. Ability to change the measurement frequency and acquisition time

3.2 Electronic Components

In order to replicate the simple Langmuir circuit shown in Figure 1.23, all that is required is a power supply, a capacitor and a way to measure current and voltage. To measure current in the first prototype, an instrumentation amplifier, the ADA111 [97] seen in Figure 3.5, is used. This is a simple circuit that subtracts the potential either side of a small sense resistor and increases the output by a desired gain.

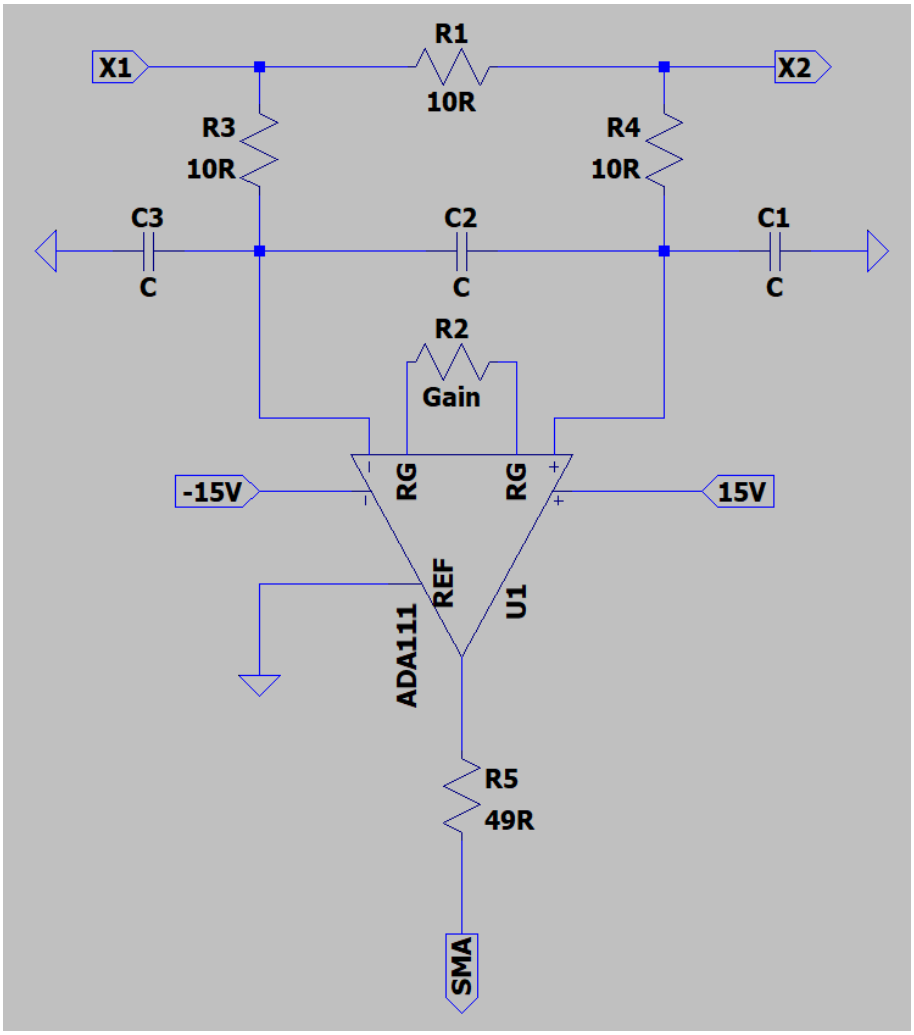


Figure 3.5: Circuit diagram of current sense circuit. Designed for both use in the main current path or measuring in the ground path. ADA111 instrumentation amplifier [97] used to measure current through R1. X1 and X2 are signal from power supply and signal to probe respectively

Measuring voltage, in principle is simple, since the Red Pitaya comes equipped with a $\pm 20\,V$ ADC. With the implementation of a simple potential divider, this can easily be increased and scaled in the internal FPGA logic.

3.2.1 AC Coupling of Capacitor

The main function of the capacitor, as discussed in section 2.2, is to ensure that all applied voltages are relative to the floating potential of the plasma. There are two cases where this assumption does not hold true;

- If the floating potential of the plasma is varying faster than the cutoff frequency of the capacitor system
- If the magnitude of the current in the positive and negative states are not equal and opposite.

The first point has already been addressed in section 2.2, but the second point needs an explanation. In the ideal system where the potential differences have been selected such that the currents in both states are of equal magnitudes, as shown in Figure 2.5. This, by definition, assumes that the electron temperature value used to scale the bias input is correct. This would yield bias states as seen in Figure 3.6. This shows that for the 3 given bias states with the correct electron temperature, the currents in the negative and positive states are equal and opposite with the zero state drawing no current, indicating that the capacitor is offsetting the floating potential correctly.

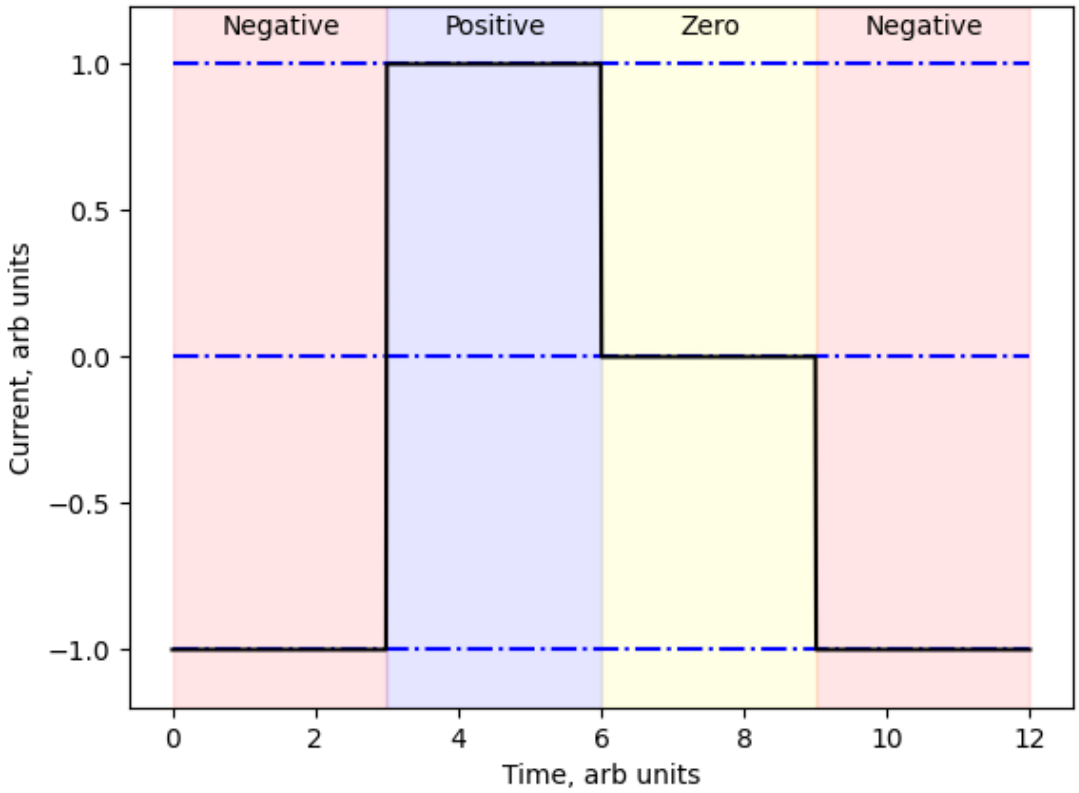


Figure 3.6: The relationship between the measured current in each of the 3 states when a correct temperature is used in the applied bias states

If the electron temperature is overestimated, then the bias states will have a large separation. Since a smaller electron temperature creates a steeper transition region, the positive current could be many times greater than the negative, which remains relatively constant. This can be seen in Figure 3.7. A scenario where the time averaged current through the capacitor is no longer zero is now introduced, which induces a DC current to further charge the capacitor.

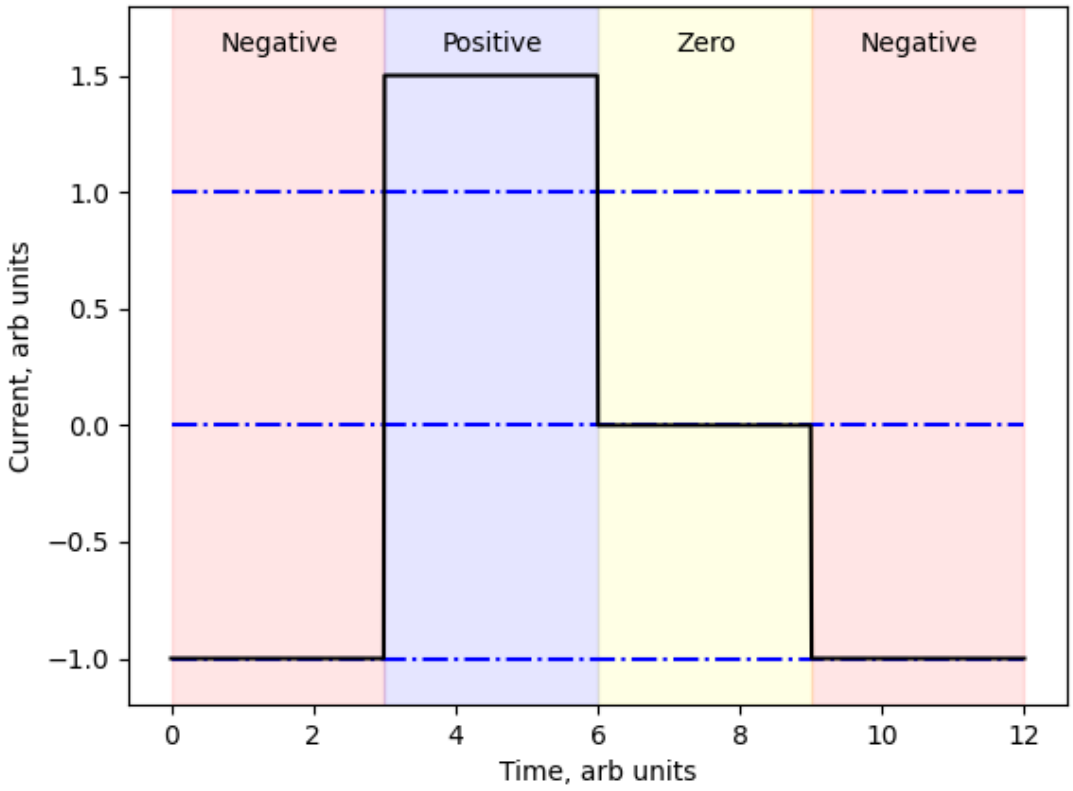


Figure 3.7: The relationship between the measured current in each of the 3 states when an overestimated temperature is used in the applied bias states

This effectively subtracts the time average current from all values and generates an offset, which causes all values to be underestimated. The result of this effect is seen in Figure 3.8. This forces the FPGA to calculate the wrong floating potential, even if the value it was applying was correct. This effect is also possible in the opposite polarity where the temperature is under-estimated.

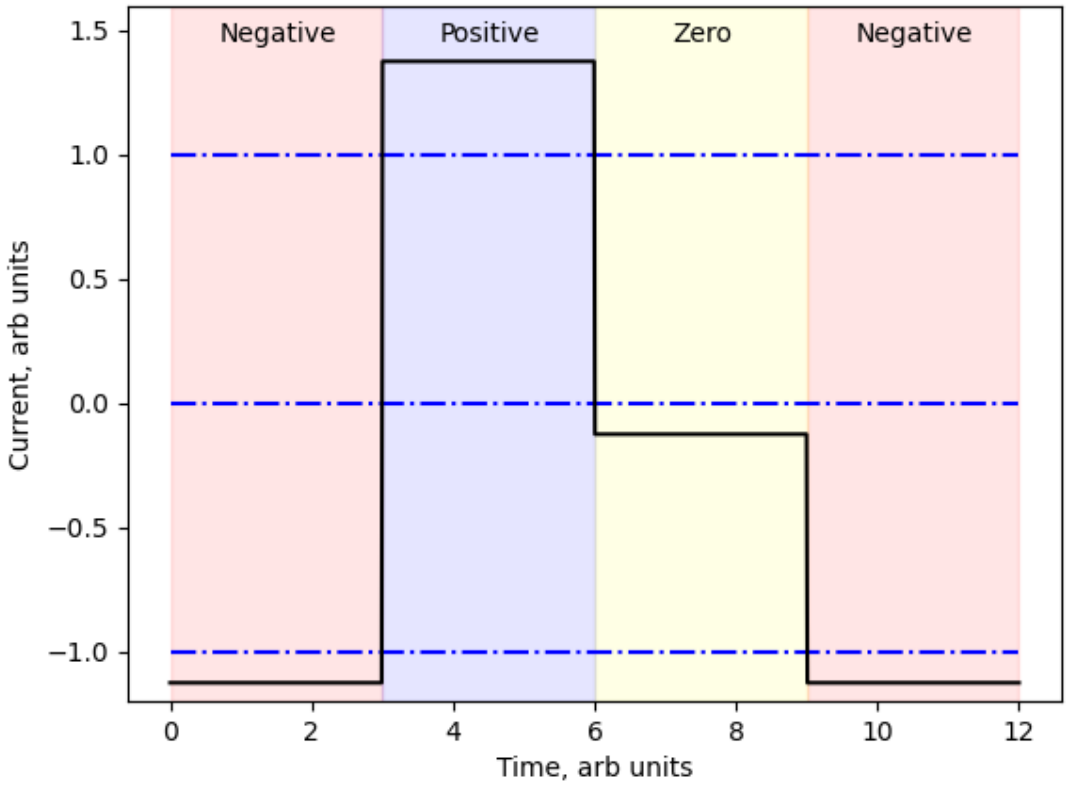


Figure 3.8: The relationship between the measured current in each of the 3 states when an overestimated temperature is used in the applied bias states when the circuit is capacitively coupled to a power supply causing AC coupling

This effect can be addressed with the use of digital processing. Storing the moving average value of the current during the zero state and adding it to the next iteration, forces zero current. Under conventional probe analysis this is a poor assumption to make, but if the capacitor is not correctly decoupling the probe from the power supply then the system breaks down. This is further relying on this assumption that there must be net-zero current passing through the capacitor. This effect, at least in this Python simulation, has not been shown to make the algorithm incapable of converging. However, it does induce a significant delay in achieving the correct value. This could be a major factor why McCarthy 2021 [88] noted around the order of 100 μs for the algorithm to accurate converge to the known plasma parameters.

3.2.2 Isolation Transformer

One important factor in the measurement of the current is the limitations of any operational amplifier used to find the difference between the two potentials either side of the resistor. Two main complications arise:

- The entire path that the current is being measured on is floating on the top of the floating potential. Particularly in HiPIMS plasmas this can be a large value, typically order of -20 V.
- In addition to all values floating at the floating potential, the raw applied voltage has to be able to be measured. In the case of using an AD111 instrumentation amplifier, which only has $\pm 15\,V$ rails, this causes a complication. As the temperature at the beginning of the pulse can rise in excess of 10 eV, this would result in up to -50 V needing to be applied to the probe tip.

One way to address both of these issues is through the implementation of potential dividers. However, by making either of these paths into the instrumentation amplifier a potential divider, a current divider is also created. This would sap current from the main path and prohibit an accurate measurement. It is however possible to isolate the main path from the instrumentation amplifier through the use of an high bandwidth isolation transformer. This will allow the signal to pass unimpeded while also maintaining a very high impedance to not draw a large amount of current. By separating the path and the instrumentation amplifier by this transformer ensures there are no additional paths to ground that would usually be required with a potential divider. This circuit can be seen in Figure 3.9.

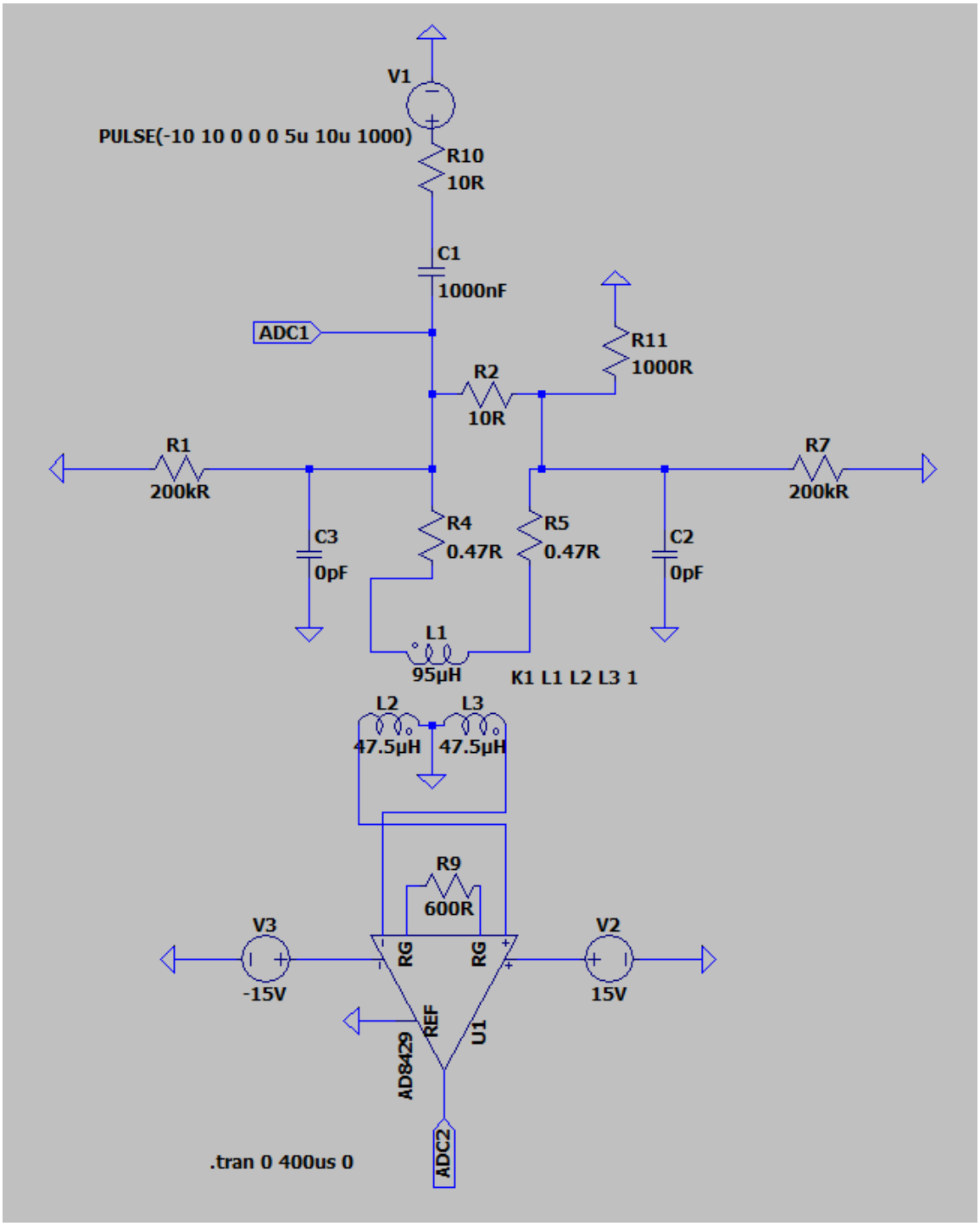


Figure 3.9: Circuit Diagram made in LTSpice showing a basic implementation of how current measurement using an isolation transformer works

However, the addition of this component can cause further complications if the resistors labelled in Figure 3.9 R4 and R5 are of too high value. If this is the case then the RC response of the isolation transformer dominates and the instrumentation amplifier is actually measuring the current across the transformer, rather than the resistor. The

effects of such a scenario can be seen in Figure 3.10.

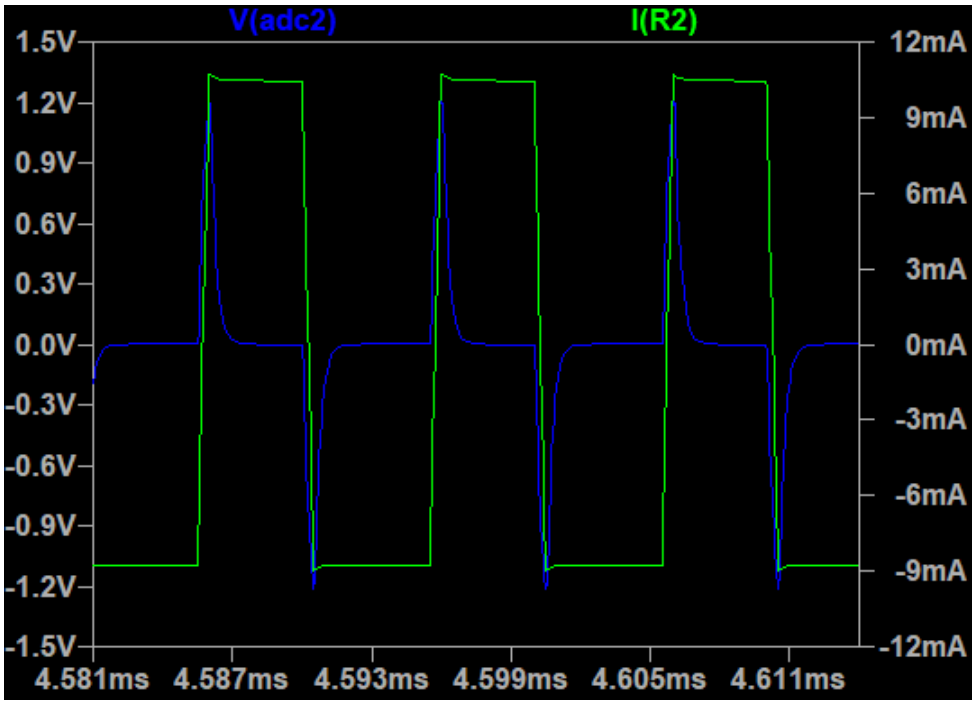


Figure 3.10: Graph from LTSpice showing the voltage measured at point ADC2 (output from the instrumentation amplifier) and the current through R2, the current sense resistor. Resistors R4 and R5 are fitted with 200R resistors, causing the RC response of the isolation transformer to dominate

By reducing the values of the resistors, more current is allowed to flow through the transformer and the signal is successfully passed to the amplifier. The value of these resistors has to be carefully selected based on the current that is expected to be measured. A clean example of this signal can be seen in Figure 3.11, where it is shown that the current in resistor R2 is cleanly converted into a scaled voltage measured at the LTSpice probe point “adc2”. This can be read directly into the Red Pitaya using the ADC ports.

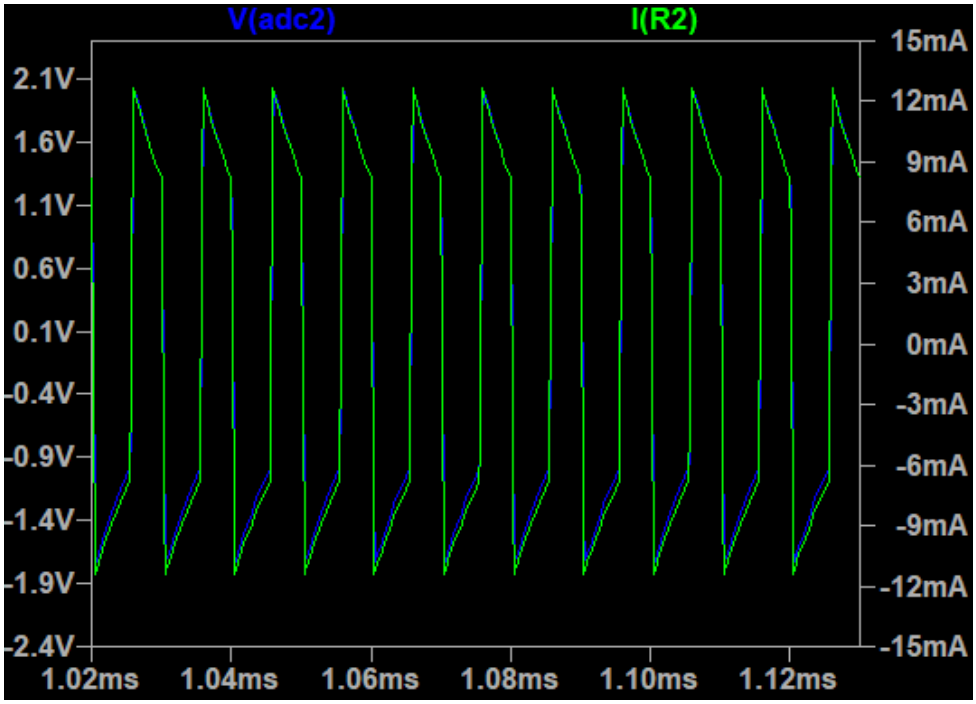


Figure 3.11: Graph from LTSpice showing the voltage measured at point ADC2 (output from the instrumentation amplifier) and the current through R2, the current sense resistor. Resistors R4 and R5 are fitted with 0.47R resistors, allowing enough current to reach the instrumentation amplifier

3.3 Electronics

While the majority of this thesis is concerning the design and implementation of the FPGA, this is not a complete solution as the FPGA receives and sends electrical signals to the probe. This requires physical electronics to perform the measurement of both the current and the voltage. In addition to this, the capacitance requirement, discussed in item 3.1, can be addressed by building a capacitor switching bank, capable of a range of capacitive values. By connecting capacitors up in series and controlling each connection with a switch, values from 68 pF to 6.5 nF in 68 pF steps can be achieved. The switches used in this circuit are W117SIP-1 reed relays [98] which have an operation frequency of approximately 1 kHz. A circuit to achieve this has been designed and implemented as shown in Figure 3.12.

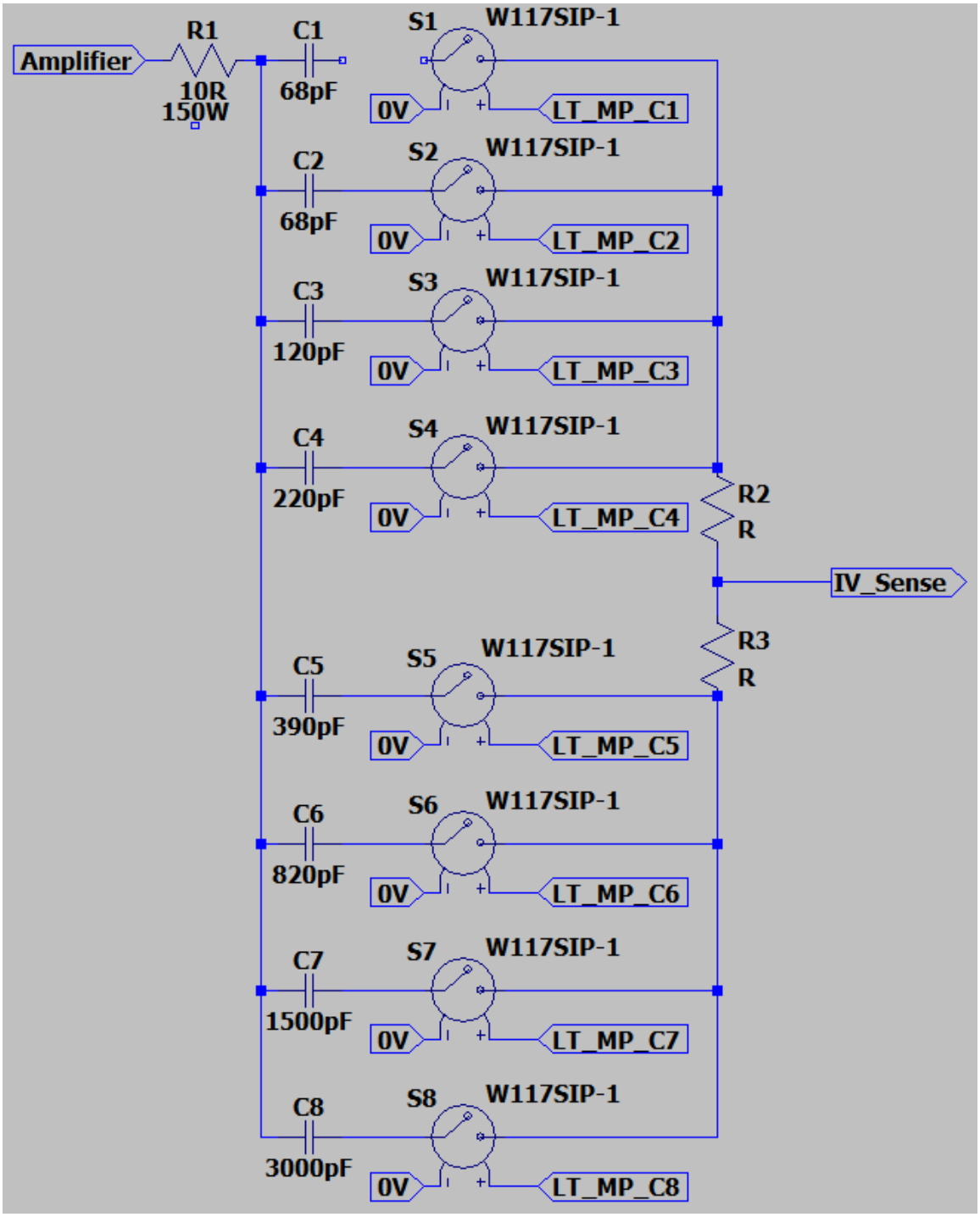


Figure 3.12: Circuit diagram of capacitor switching circuit with each W117SIP-1 reed relays [98] controlled via GPIO pin on the Red Pitaya. C1 is left open circuit due to an in-situ modification.

Firstly a high power, low resistance, resistor is used to couple to the capacitor to form the initial RC circuit. This has to be high power as the fully amplified signal transits the resistor. Each switch is controlled by the Red Pitaya via the GPIO pins on the external connector E2, seen in Figure 3.13. The GPIO pins are controlled by a lookup table which

records the measured current and returns a suitable capacitor value. Since there are 7 capacitor switches, there are 127 unique capacitance values. This enables the system to have the lowest possible capacitance without causing attenuation of the current while keeping the floating potential response time at a minimum. In order to accommodate for both a high and a low temperature system, an identical setup was generated with a larger capacitor range of 1 nF to 100 nF. This is to accommodate the higher density, and therefor higher current, systems of fusion plasmas.

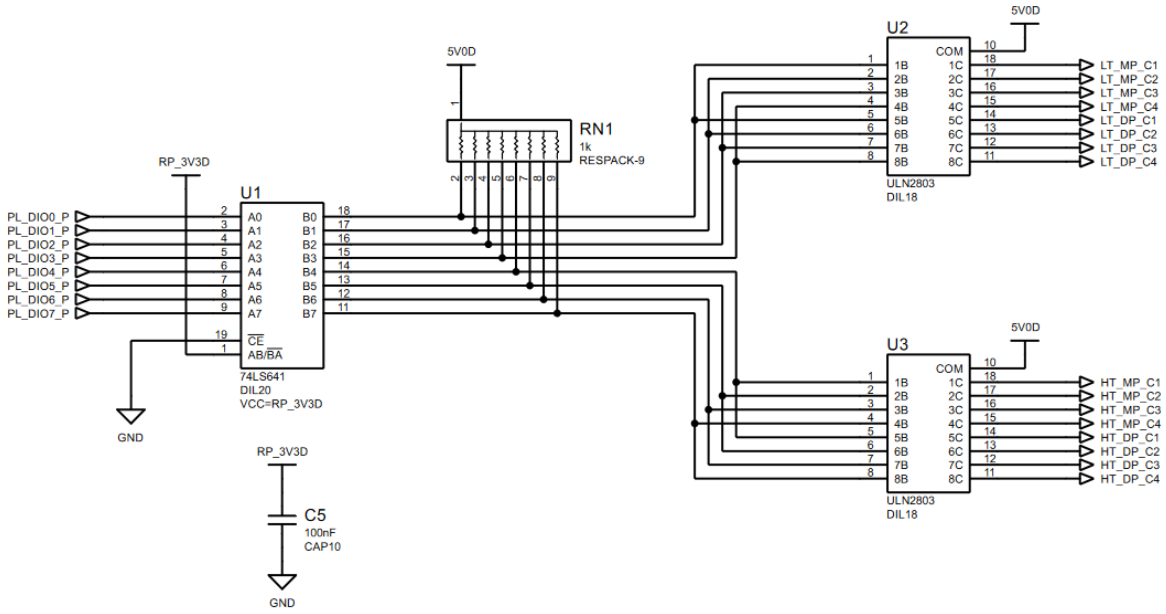


Figure 3.13: Circuit diagram showing the connections between the switch relays and the Red Pitaya GPIO pins

The first iteration of the electronics is shown in Figure 3.14. In this configuration the board is separated into two regions; the current measurement (a), and the capacitor switching circuit (b). In addition to this without any use of potential divider the voltage range from a HiPIMS pulse is too large to be collected by the $\pm 20\ V$ ADC of the Red Pitaya. Therefor a potential divider was installed across the voltage sense by using two 100 kΩ resistors to limit current drain but provide an adequate voltage range. This was then accounted for in the Red Pitaya by multiplying input voltages by a factor 2.

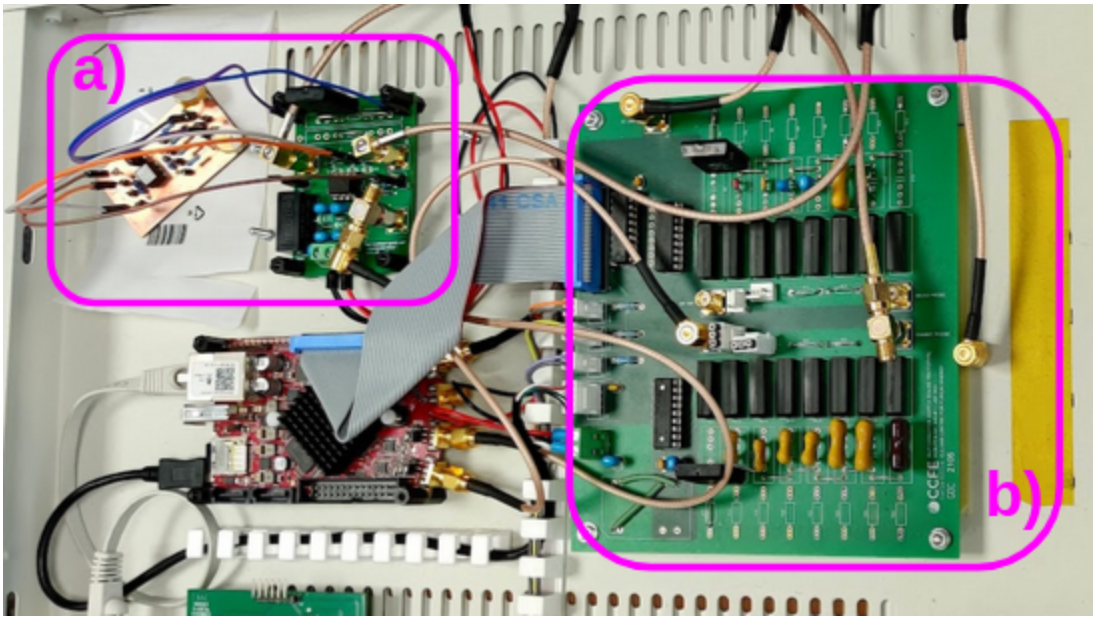


Figure 3.14: The capacitor switching board showing a) the current sense circuit matching circuit diagram in Figure 3.5 b) the capacitor switching circuit matching circuit diagram in Figure 3.12

The current sense was quickly found to be inadequate as the capacitance in the cable was not negligible compared to the value of the capacitors used for decoupling. A new board was designed that would allow the dummy probe to be used as well as additional trimmer capacitors to balance any discrepancy between the two cables. This new board can be seen installed in Figure 3.15

At higher speeds the instrumentation amplifier does not have the required bandwidth to perform fast current measurements. For this reason a new circuit, Figure 3.16, has been developed that implements all of the improvements discussed above with multiple ground planes and careful impedance matching to ensure the clearest signal. A voltage sense was also implemented to ensure minimal current loss that could have been occurring due to the potential divider. Two OPA655U operational amplifiers are used to measure each the current and the voltage. The first is always a buffer to the signal and the second adjusts for the desired gain. The op-amps are capable of a maximum slew rate of 295 V/μs and have a gain bandwidth product of 240 MHz.

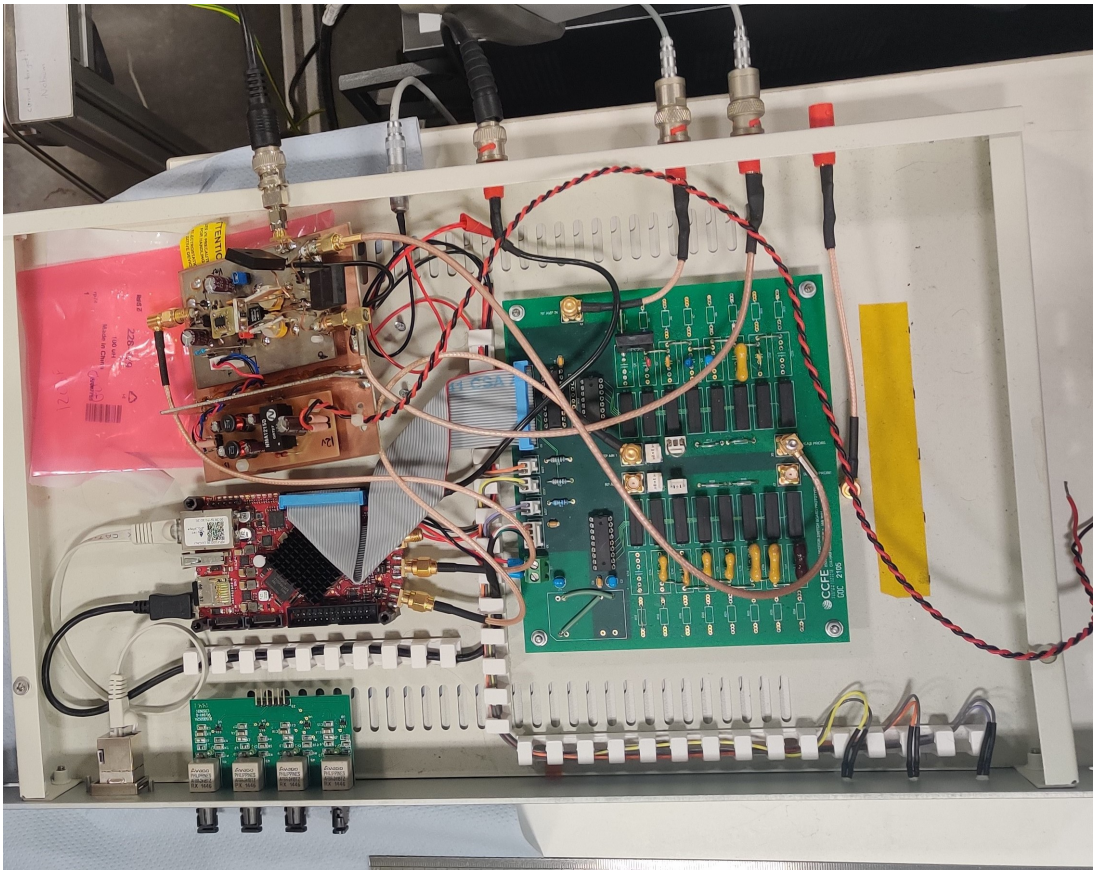


Figure 3.15: The installation of a custom made IV sense circuit that accommodates a dummy probe and trimming capacitors to match cable capacitance

The new electronics have been fully commissioned but have not been means tested in a plasma environment with the device due to the return of the amplifier used to generate the initial signal that was borrowed from MIT. The signals, as viewed from an oscilloscope, show that this electronic configuration is capable of exceeding a 1 MHz parameter output resolution. The circuit diagram can be found in Figure 3.16.

The final circuit that was produced in order to measure the voltage and current. This circuit was custom built to minimise noise and current loops along with carefully selected trimmer capacitors to mitigate cable capacitance caused by a miss-matched length of coaxial cable. This circuit is best included in the appendices as it was never used to gather results, as it was not commissioned in time to gather results.

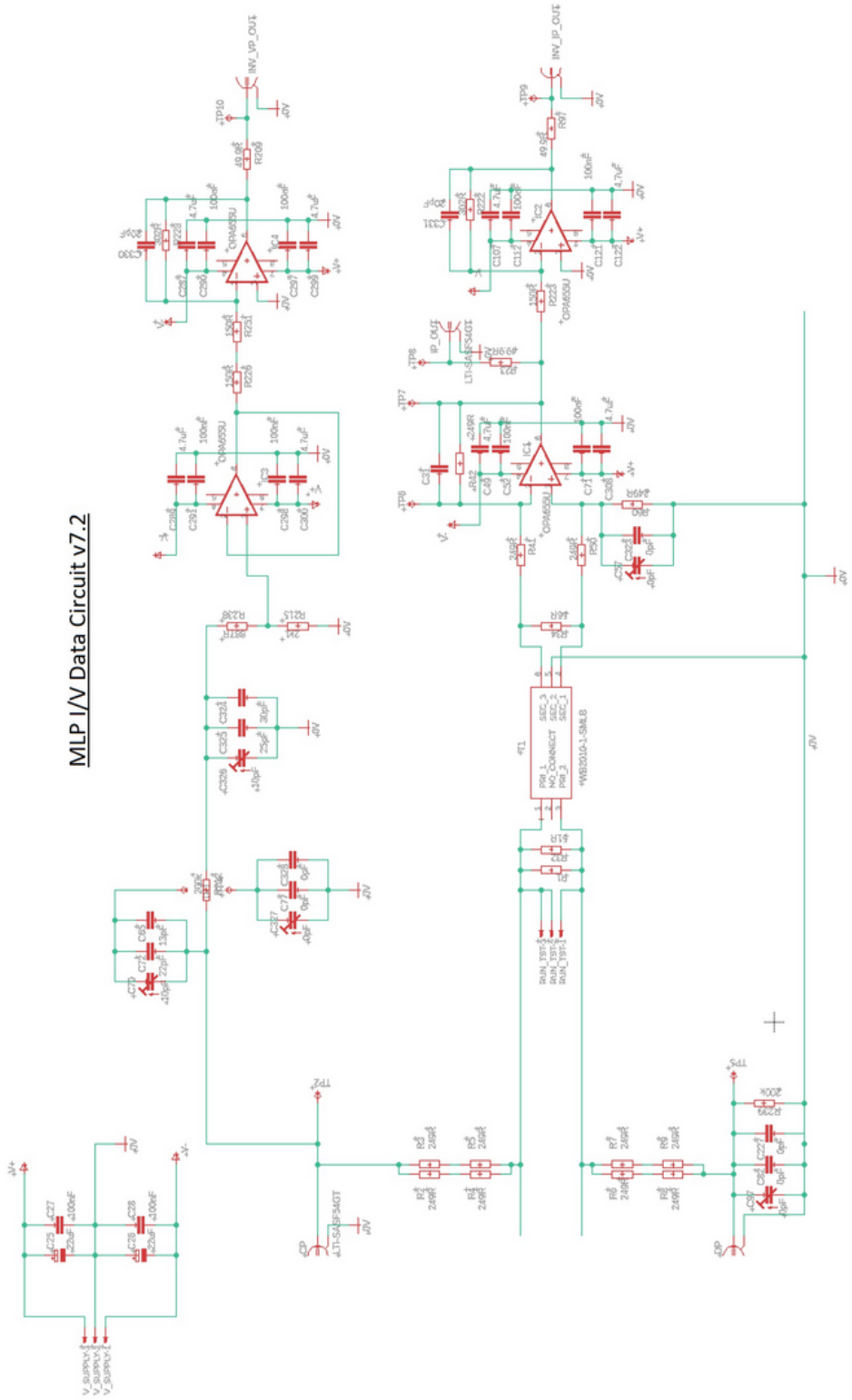


Figure 3.16: Circuit diagram showing the final implementation of the IV sense circuit for high bandwidth application. Circuit includes two input ports to accommodate the Langmuir probe and the dummy probe. Trimmer capacitors can be adjusted to match cable capacitance and both the current and voltage sense have step down dividers to ensure that the whole data range is sampled

Chapter 4

Experimental Setup

This chapter will include the core systems used in experimental testing and detail the experimental setups used to obtain data to prove the efficacy of the prototype. The system is located in the Department of Electrical Engineering and Electronics at the University of Liverpool. The setup consists of 3 major systems which will be discussed; the plasma vessel, the Langmuir probe and the power supply's used to drive the plasma.

4.1 Plasma System and Magnetron

The plasma system, abstractly shown in Figure 4.1, consists of the chamber, the power supplies and the magnetron source. The chamber is an aluminium tube of internal diameter of 270 mm and 300 mm long. At one end is a circular magnetron, which will be discussed in detail later in this section, positioned in the centre of the tube. The magnetron can have its position inside the tube changed while remaining on the centre line. Both ends of the tube are vacuum sealed and a viewing port allows a direct line of sight perpendicular onto the magnetron. In addition to this a flange is also located on the circumference of the tube perpendicular to the plane of the magnetron. This flange is covered by a plate that has an off-centre port that allows the insertion of the probe stem. This has the capability of adjusting the vertical position of the probe in the vessel, as well as its radial position through the rotation of the plate. Another flange is located at 90 degrees to both the viewing port and probe flange, which is connected to a Pfeiffer

Vacuum Duo 10 MC rotary backing pump. This allows the system to reach a base pressure of 20 mTorr. This connection is also equipped with a Edwards EXT 75DX turbo, to further reduce the pressure to order 0.1 mTorr. The system also has various ports which give access a series of other devices, such as:

- Mass Flow Controller - controls the flow of gas into the vessel
- 2 pressure gauges - Measures the pressure within the vacuum vessel
  - an MKS 627 pressure transducer for measuring experimental pressure that provides accurate pressure readings down to 20 mTorr
  - an Edwards Apg100-XJG pirani used to monitor pressure from atmosphere during initial pumping

The entire vessel also acts as an electrical ground for all systems, including the probes, that are used on it.

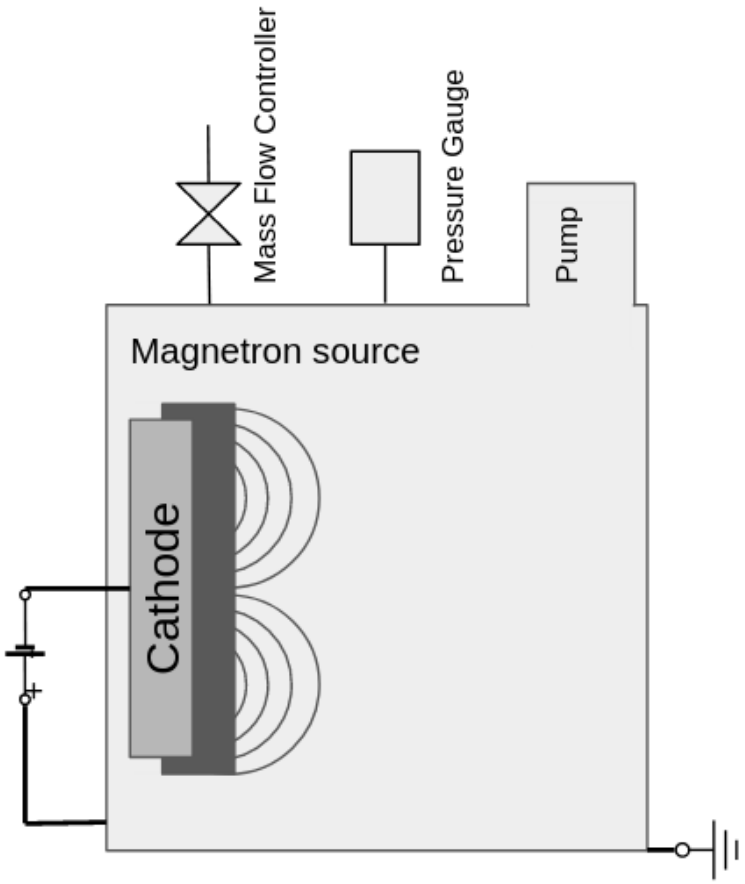


Figure 4.1: The plasma system used to test the function of the UFLP with associated components

The magnetron, which has a type-1 unbalanced field, itself is fitted with a 76.2 mm diameter, 6.35 mm thick tungsten target plate. The field strength and orientation can be seen in Figure 4.2. The target plate is water cooled by a ICS Cool Energy iC 03C, which pumps cooled water that has a temperature in the range of $11°C$ to $17°C$. This water is pumped directly to the target plate in order to dissipate heat efficiently, to prevent the target from heating up and melting.

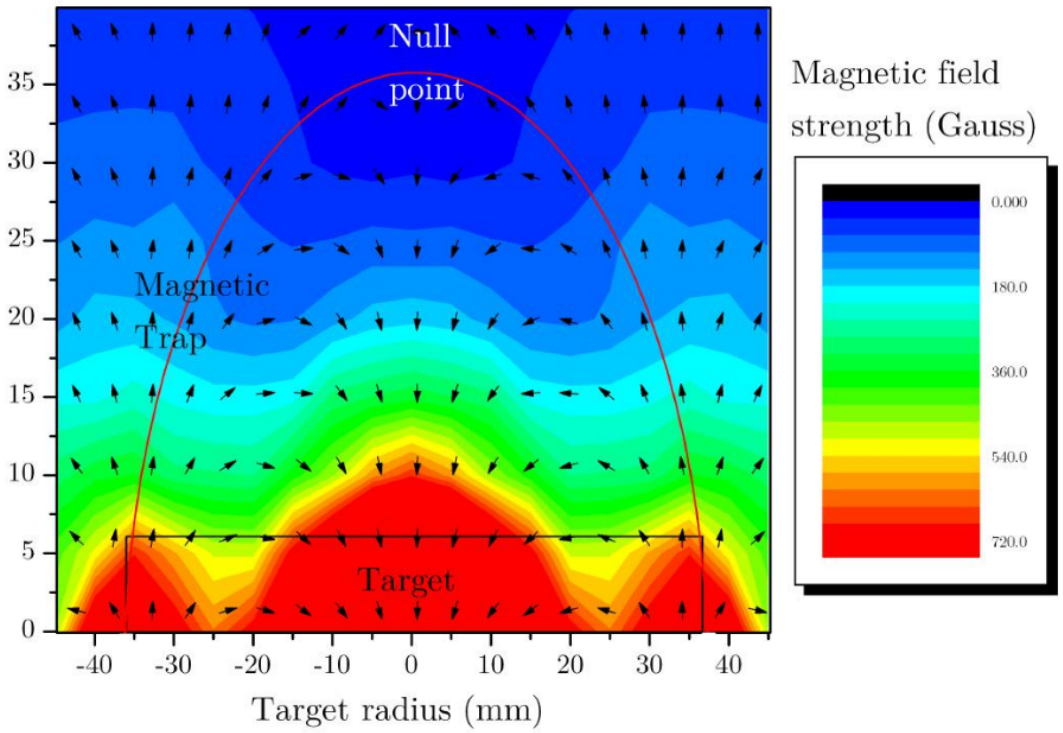


Figure 4.2: The magnetic field strength of a 70mm diameter magnetron showing the field lines. Also highlighted is the region referred to as the "magnetic trap", inside which electrons are trapped within the electric field and showing the magnetic null line [99]

4.2 Langmuir Probe

Two different Langmuir probes were used for taking measurements, both of which were built in house. The following process describes the configuration of both probes, which only differ in the shape of probe tip equipped. One consists of a square flag probe that measures 20x20 mm and is 0.5 mm thick, seen in Figure 4.3. The other is a probe tip made from tungsten wire. This larger probe was able to draw larger currents which was

used for collecting data on the initial low density DC plasmas. The construction of the wire tip will be explained for clarity, which was used for the majority of experiments.

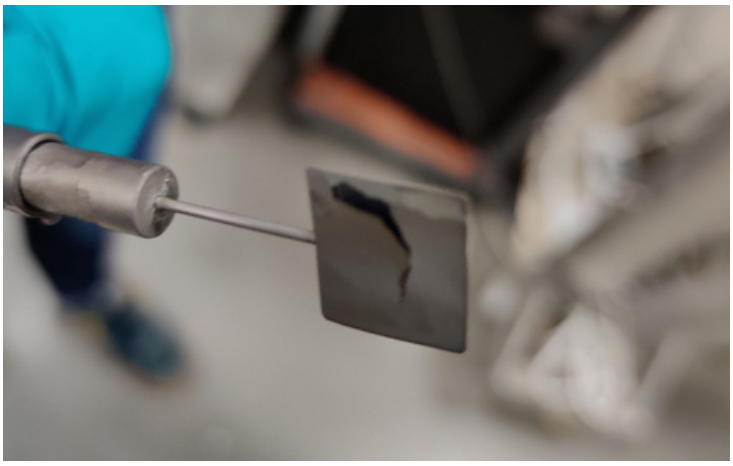


Figure 4.3: Picture of the flag probe tip, used to draw more current from a low density plasma

The wire probe consists of a probe tip, made from a length of 0.5 mm diameter 99.95% tungsten wire. Ceramic tubing with an outer diameter of 2 mm was positioned to ensure that only 10 mm of the probe tip is exposed. An additional ceramic tube of outer diameter 1 mm is recessed inside of the larger tube by approximately 3 mm, to ensure the tungsten wire does not make contact with the outer ceramic, as shown in Figure 4.4. This prevents a short circuit in the event of conductive material being deposited on the inside of the ceramic. The ceramic tubing then runs into the probe stem, where the tungsten tip is soldered to a wire that runs through the remaining length of the probe stem before being connected to the live of a female BNC connector inside an RF shielded casing.

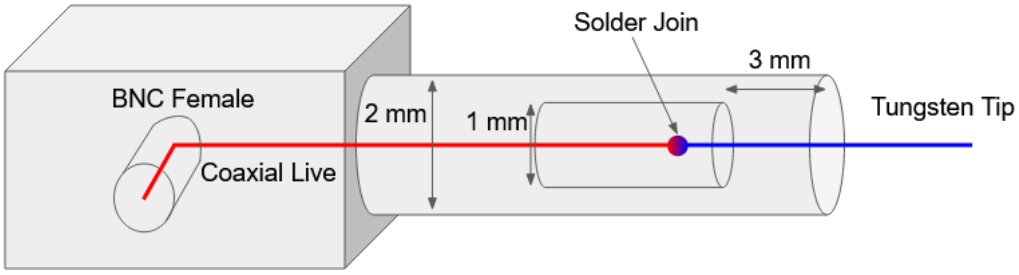


Figure 4.4: Diagram to explain the construction of a probe where the live of a coaxial cable is soldered to a tungsten probe tip. Probe stem length shortened for purpose of diagram.

In order to account for the capacitive effects a dummy probe of identical configu-

ration to the main probe is also constructed. However, the tip is covered by longer ceramic tubing to ensure it makes no contact with plasma. Down the probe stem the wires of the main probe and the dummy probe are also coiled, to ensure equal exposure to electric fields or interference. Further to this, vacuum epoxy resin is used to seal the probe stem ensuring that a vacuum can be maintained. A schematic of this probe configuration has been shown previously in Figure 3.4 and the constructed probe is shown in Figure 4.5.

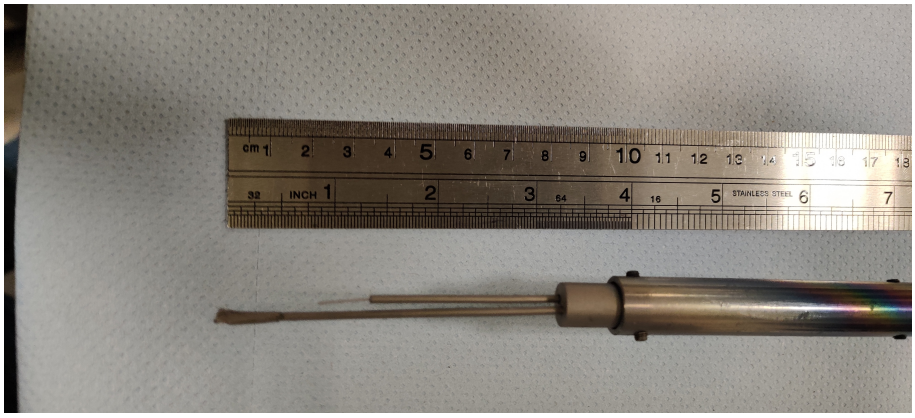


Figure 4.5: Picture of the probe and dummy probe stem where the probe tip dimensions are 0.5 mm in diameter and 10 mm in length. The concealed dummy probe is identical to the main probe, but is covered so as to not expose it to the plasma

When used in the UFLP configuration the signal is first generated by the Red Pitaya, detailed in section 2.2, before passing into a NF HSA-4101 high speed bipolar amplifier. This amplifier was kindly loaned by the Plasma Science and Fusion Center at Massachusetts Institute of Technology, for the development and advancement of a digital alternative to the mirror Langmuir probe. It comes equipped with a modifyable gain, which the user will have to carefully calibrate to ensure it allows the $\pm 1\ V$ output of the Red Pitaya to exceed at least 3.325 times that of the expected electron temperature (in electron volts) of the system. The amplifier boasts a slew rate of 5000 $V/\mu s$, which far exceeds any requirement that is needed for a low temperature system - but would be limited by its voltage rails of $\pm 71\ V$ for a fusion plasma device.

The main probe is also capable of being used as a regular Langmuir probe via the use of connecting it to an Impedans ALP-1000. This is an off the shelf trigger enabled Langmuir probe analysis tool, that when connected to a probe can perform a configured voltage sweep and measure the current. Since it can be triggered to a signal it can be

connected to the trigger signal of the HiPIMS pulse, which is produced by University of Liverpool's in house kick pulse generator. This allows the ALP-1000 to make use of a delay generator to measure each part of the pulse with the desired voltage to form an IV curve for each part of the pulse, over many cycles. This raw current and voltage data is then saved and analysed in Python to return floating potential, ion saturation flux, electron temperature and electron density.

The position of the probe in all cases is approximately 15 mm from the target plate positioned above the racetrack, detailed in Figure 4.6. This is to maximise density for larger currents into the probe. The position of the dummy probe relative to the main probe is not critical, as following the same path is mostly to ensure it is exposed to the same electromagnetic fields and is the same length, rather than in the same plasma. This holds true as long as the sheaths of the two probes do not intersect.

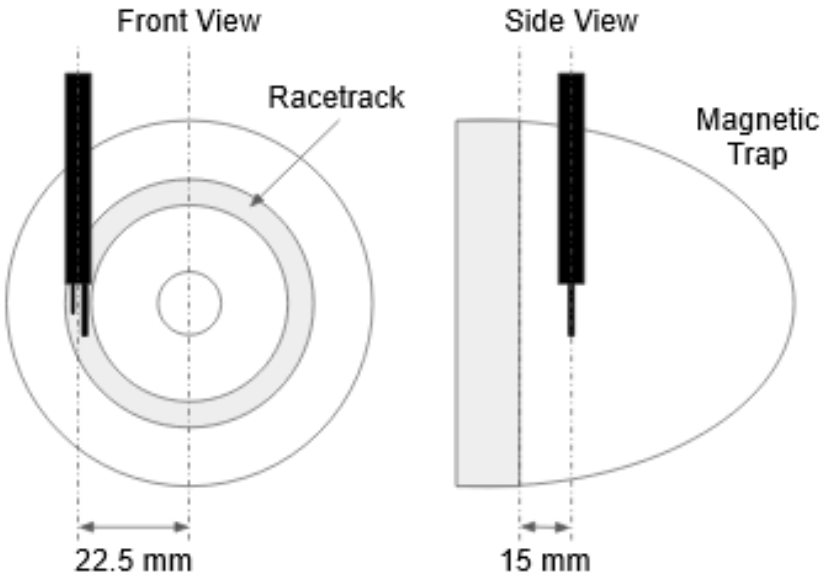


Figure 4.6: Diagram illustrating the position of the probes relative to the magnetron target plate

4.3 Power Supplies

Power is supplied to the magnetron source via one of two different power sources. This can either be an Advanced Energy, Pinnacle 18kW supply, which can be operated in either a DC mode or a pulsed DC mode with a minimum frequency of 5 kHz with a minimum

off time of 5 μs at this frequency. The device can also be powered by an in-house custom built HiPIMS power supply unit which is described in detail in [39]. The voltage and current of both of these power supplies passes through a junction box, where the voltage and current are measured by a Tektronix P5 100 voltmeter and a Pearson 3972 current monitor respectively. These are connected to an Tektronix DPO 3034 Oscilloscope for monitoring the power to the target plate.

Chapter 5

Results and Discussion

In this chapter, the data gathered from installation on a low temperature - low pressure plasma device with a magnetron is presented and is concluded with how this information will impact the installation onto MAST-U. A brief introduction to the variation between the different tests is given and the results in those conditions is presented. It should be noted that the primary purpose of testing in the low temperature environment at Liverpool is not to perform any form of plasma physics analysis, but to show the efficacy of the diagnostic that has been built.

5.1 Installation at Liverpool

In the low temperature plasma department at the University of Liverpool all testing was performed on the same plasma chamber described in chapter 4. This same magnetron is connected to 3 power supplies which can be operated in direct current, pulsed direct current and HiPIMS respectively, each of which will be shown in this section.

5.1.1 Direct Current Plasma

The first real world test of the device was ensuring it could give realistic results for a steady state low-density DC plasma.

Upon initial tests it was found that the magnitude of the current was too small to be detected by the current sense circuit designed. Using a probe of such small dimensions ($r_p = 0.25$mm, $L_p = 10$mm) resulted in currents in the order of 10's of μA. In order to draw more current a larger probe tip had to be used. This can be seen in Figure 4.3. A probe tip this large will perturb the plasma that it is exposed to, but it will still draw a current that can be fit to Equation 1.3.23. The nature of using Langmuir probes insists that small currents are to be measured. In Figure 5.1 it can be seen that the signal to noise ratio is very high. This decreases rapidly as the applied voltage approaches the floating potential. This is because near the floating potential the current approaches zero. The time averaged value of the current drops below the noise floor and gives a poor signal to noise ratio.

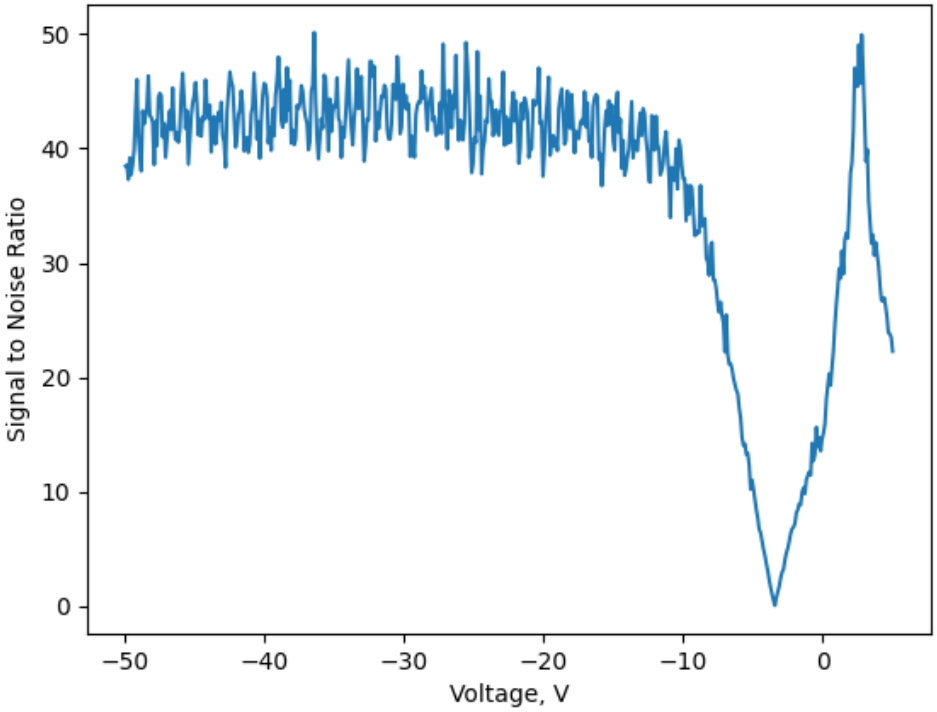


Figure 5.1: The signal to noise ratio across a Langmuir probe sweep using an Impedans Langmuir probe analysis system on a DC powered Argon plasma with 200 W input power supply with a gas pressure of 7 mTorr with a floating potential approximately -4 V

In addition to the variation in signal to noise ratio, the standard deviation of the data is also linked to the magnitude of the current drawn by the probe, illustrated in Figure 5.2. For this reason it should be expected that drawing any current at a voltage higher than the floating potential will result in a higher level of noise than below it.

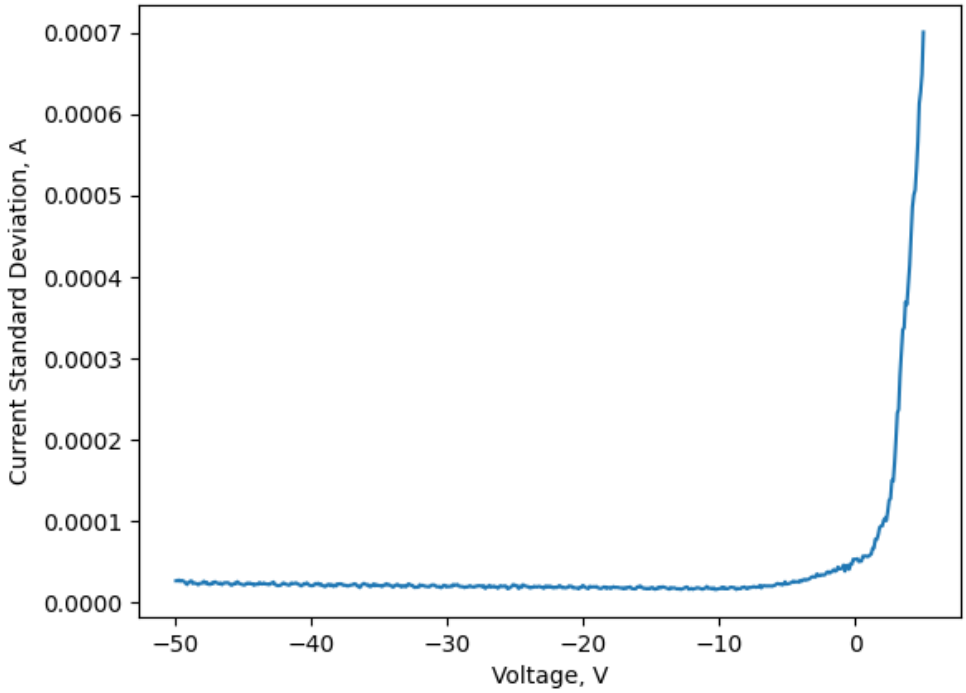
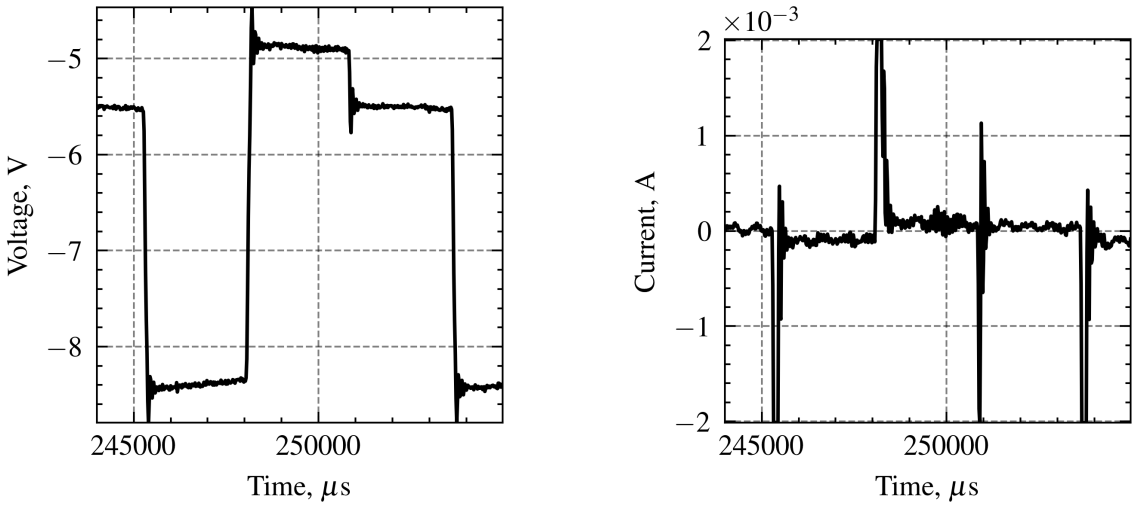


Figure 5.2: The standard deviation of the measured current across a Langmuir probe sweep using an Impedans Langmuir probe analysis system on a DC powered Argon plasma with 200 W input power supply with a gas pressure of 7 mTorr

Particularly for these higher noise levels a form of smoothing has to be implemented to ensure that the current measurement is as accurate as possible. This can be implemented in HDL easily by considering the division as a bit shift of some power of two summed value of currents.

$$\frac{\sum_{n=0}^{n=2^x} I_n(V_p)}{2^x} = \overline{I(V_p)} \tag{5.1.1}$$

This acts as a low pass filter, causing higher frequency fluctuations than the data window to be filtered out prior to being used in calculation of the next parameter set. Figure 5.3 shows an example of the system exposed to a plasma. The 3 bias states can clearly be seen and each bias state returns a corresponding current state. There is a non-negligible variation in the current that appears to have some periodicity. Sharp current peaks can be seen at the transition of each state, this is current imposed by the capacitor due to a large rapid change in voltage.



(a) (b)

Figure 5.3: Measurements taken at 50 kHz using a single probe multiplexed at dynamic bias voltages at values $V_{+,-,0}$ = 0.64Te V, -3.325Te V and 0 V in a DC plasma which shows small perturbations in measured current across the duration of a stable voltage. (a) Voltage, (b) Current

Figure 5.4 shows some of the results collected in a DC powered argon plasma with a gas pressure of 26 mTorr with the UFLP running at an output frequency of 110 kHz. Given this is a steady state plasma there is very little periodic variation in the data, and any fluctuations viewed could be actual fluctuations of plasma parameters, as they are low in magnitude. The iteration of electronics used for this data prohibited voltages that exceed ± 14.4 V due to exceeding the voltages on the rails of the instrumentation amplifier. This means that the input pressure had to be as high as possible to both increase the magnitude of the current and decrease the value of the floating potential. At small temperatures, this results in all 3 bias states to fit comfortably within the limits of the voltage rails of the current measurement. The pressure value required was higher than what could be achieved by just increasing the value of the flow rate on the mass flow controller. To achieve a higher pressure a butterfly valve on the turbo was used to strangle the vacuum and turbo pumps to increase the pressure.

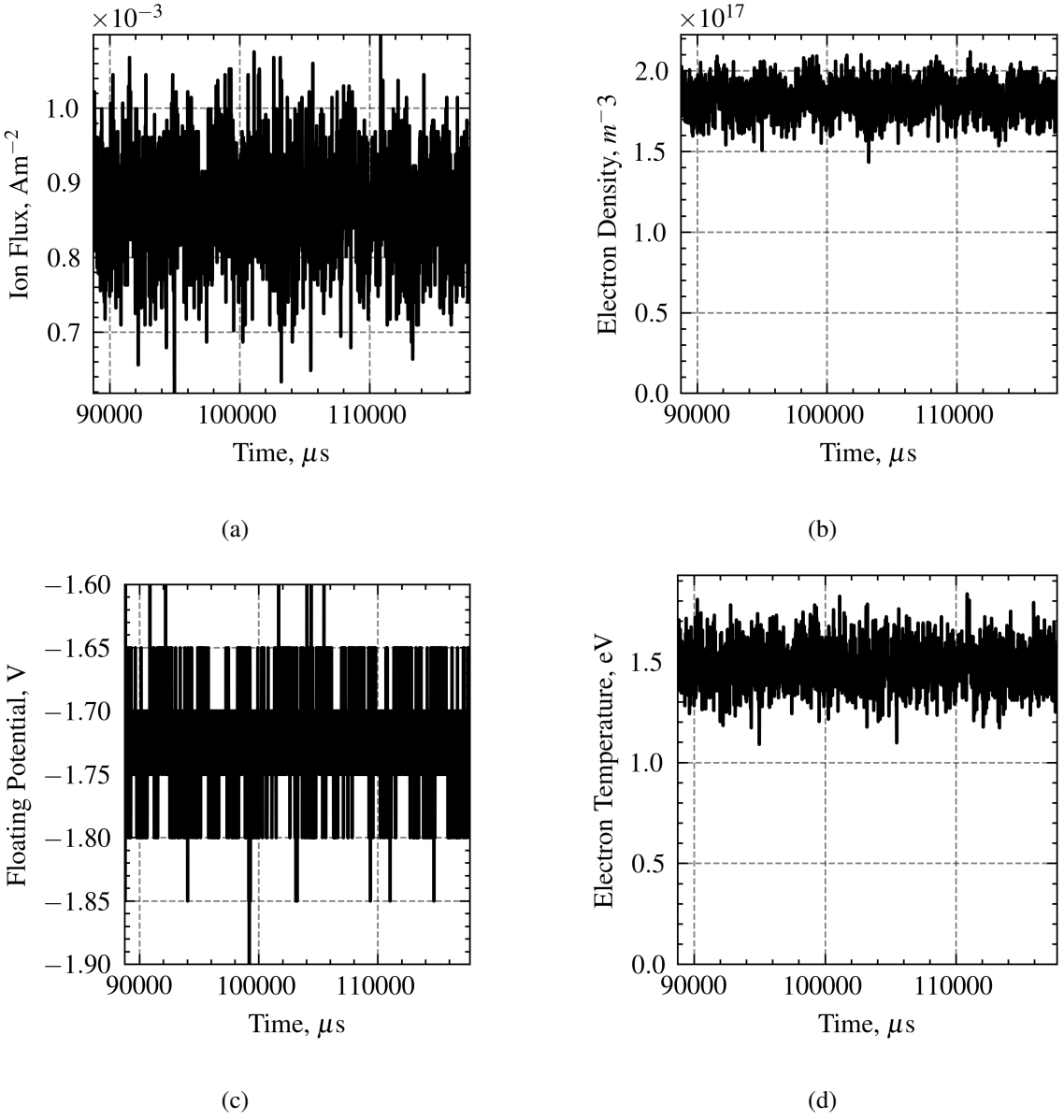


Figure 5.4: Measurements taken at 110 kHz in a DC plasma at 35 mTorr using a single probe multiplexed at dynamic bias voltages at values $V_{+,-,0}$ = 0.64Te V, -3.325Te V and 0 V in a DC plasma. (a) ion flux, (b) plasma density, (c) floating potential and (d) electron temperature

A quick confirmation that the device is working as expected would be to change the pressure mid-way through data collection. By increasing the pressure from 21 mTorr to 35 mTorr an increase in density and therefore current would be expected. By increasing the density but maintaining the power to the plasma, the temperature is expected to drop as the same energy is now divided between more particles. A drop in temperature also causes a drop in floating potential. All of this can be clearly seen in Figure 5.5.

Ideally some periodic perturbation would be added to the mass flow, but unfortunately the equipment is not capable of this.

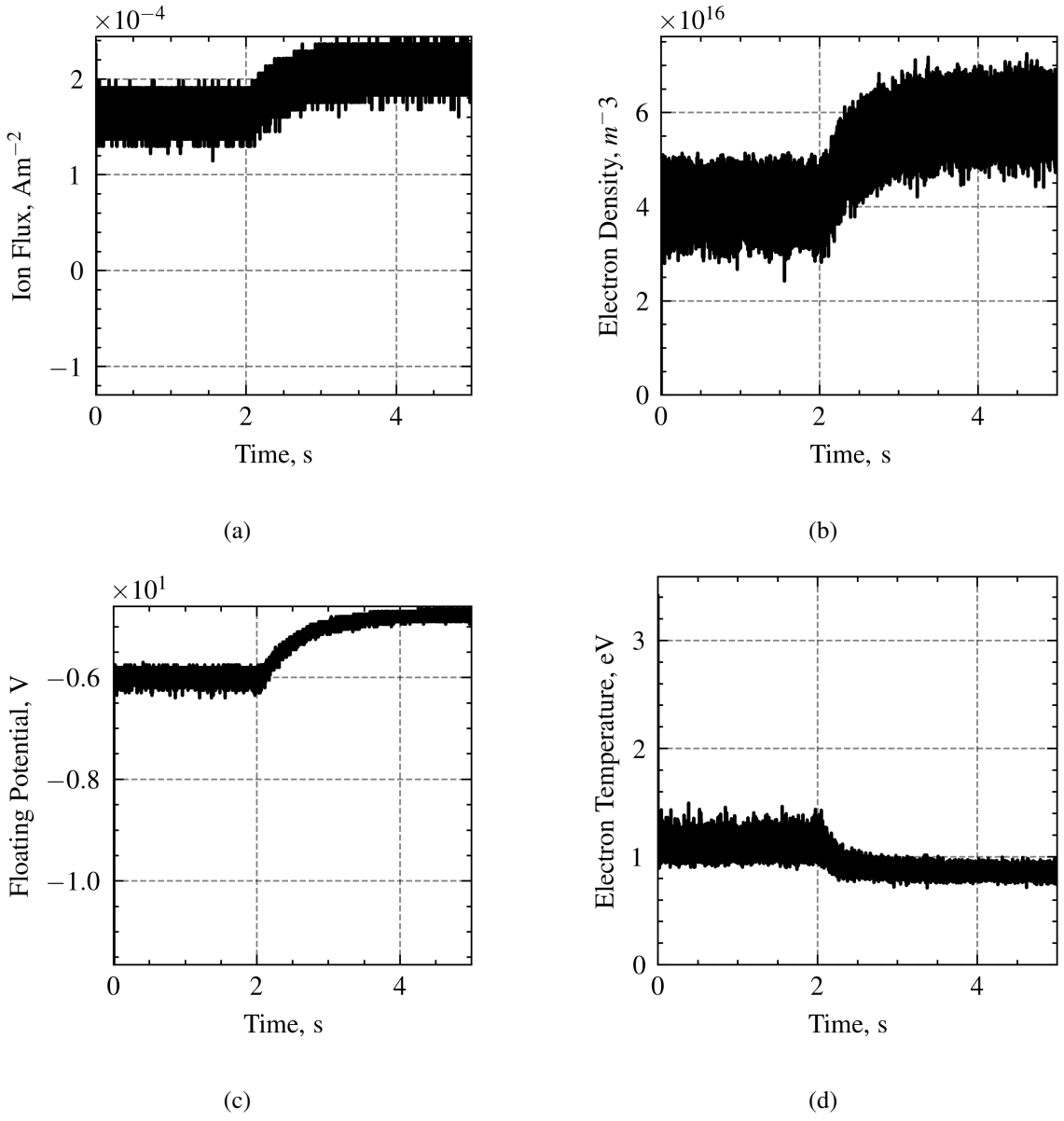


Figure 5.5: Measurements taken at 110 kHz in a DC plasma using a single probe multiplexed at dynamic bias voltages at values $V_{+,-,0}$ = 0.64Te V, -3.325Te V and 0 V with a change in pressure at 2 seconds from 21 mTorr to 35 mTorr. (a) ion flux, (b) plasma density, (c) floating potential and (d) electron temperature

5.1.2 HiPIMS Plasma

In the HiPIMS driven plasma, the electron density is much higher; typically of order $10^{18}\ m^{-3}$ in the region of the magnetic trap. This results in much higher currents being drawn to the probe, so the size of the probe can be reduced to a tungsten wire that is 10mm long with 0.5 mm diameter. This will give better results in the plasma as the flag probe used in subsection 5.1.1 will have disrupted the plasma due to its large size. Figure 5.6 shows the new smaller probe tip inserted into the plasma while implementing the double probe configuration explained in Figure 3.4. The probe is located just inside of the magnetic trap parallel to the target plate positioned 15 mm away from the surface.

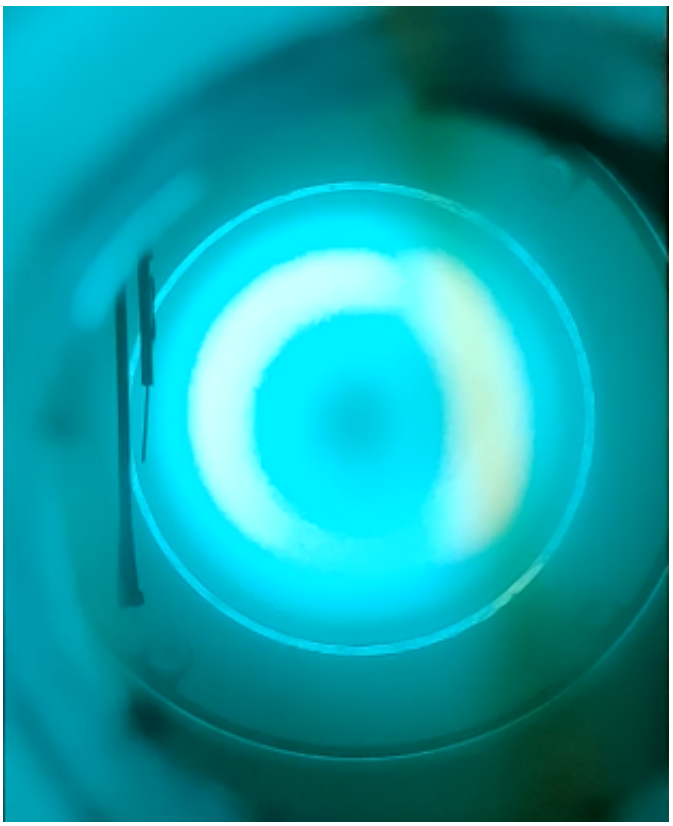
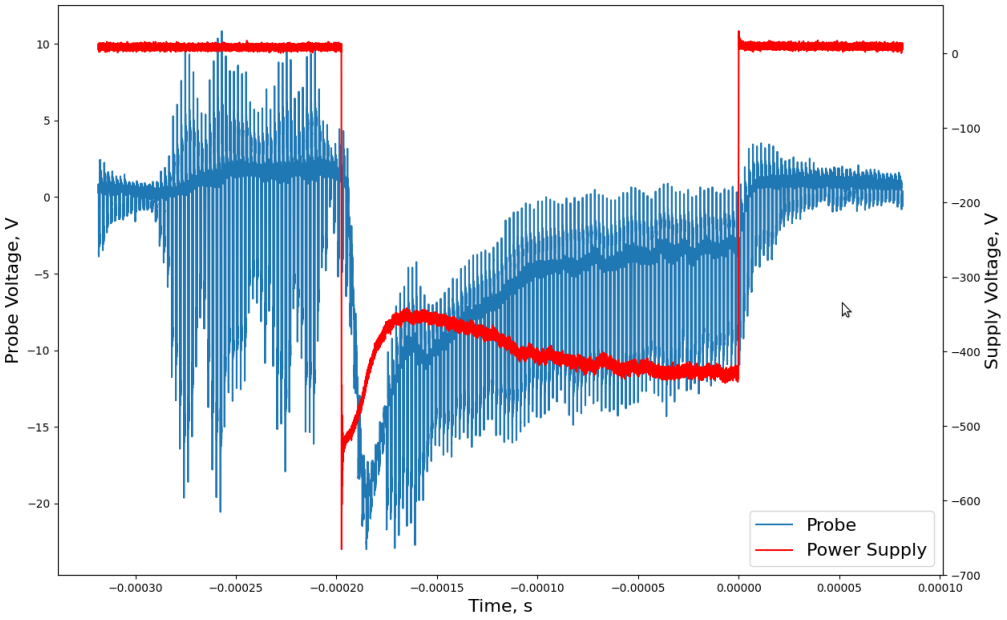
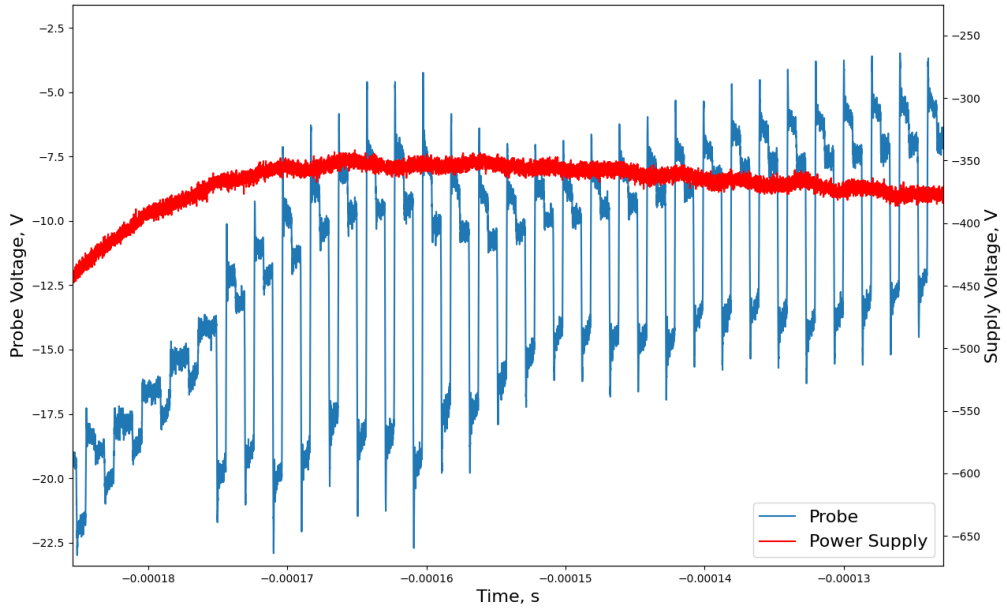


Figure 5.6: Langmuir probe and dummy probe immersed in plasma as seen through a viewing port

Figure 5.7 shows the time evolution of the voltage measured at the probe against the profile of the HiPIMS supply voltage. First the temperature must be calculated to be very low which accounts for the small bias range, then the temperature peaks and plateaus. Prior to the pulse, the algorithm is still attempting to calculate valid temperatures.



(a)



(b)

Figure 5.7: Time evolution of power supply voltage and measured probe voltage: across duration of HiPIMS pulse (a), zoomed in on region of highest temperature (b). Figure shows the dynamic change of the bias levels as the pulse progresses due to the UFLP calculating a higher electron temperature

This causes the bias ranges to trace the entire range attempting to converge, but once the pulse starts it immediately finds a good fit and returns a valid electron temperature and therefor bias range. Once the pulse has finished, the plasma is still

present but is rapidly losing energy - a period known as the afterglow. Since this is a region of decreasing temperature, the bias range can be seen to be decreasing throughout the duration of it, until the electron temperature becomes so low the algorithm no longer continues to converge.

HiPIMS generated plasmas are a short lived with very high temperatures and densities as discussed in subsection 1.2.2. As the desired measurement of the HiPIMS system only occurs for 200 μs, in order to do any comparison to a conventional probe a triggered Langmuir probe system must be used. This is an inbuilt feature of the Impedans ALP-1000 [100]. By connecting it to the same triggering signal of the HiPIMS power supply it can generate a 1 μs offset every pulse and use this to measure the IV curve at that point in time. To measure the entire 200 μs pulse takes approximately 220 seconds. This is because the pulse frequency of the magnetron is 50 Hz. The probe takes a measurement by producing a 1 μs offset at every requested voltage. Data was measured from -50 V to +5 V in steps of 1 V. The total duration of the pulse was 200 μs.

$$\frac{1}{50[Hz]} \cdot 55[V] \cdot \frac{200[\mu s]}{1[\mu s]} = 220\ s \tag{5.1.2}$$

Another observation from Figure 5.7 indicates that the sudden change in probe voltage that occurs at $-200\,\mu s$ is actually a change in the value of the floating potential. This $-20\,V$ change occurs in approximately $20\,\mu s$. This change in voltage is so rapid that an extremely small capacitor would be required to successfully decouple it from the power supply. At the same time however, a substantial current has to be drawn in order to account for the large density of the plasma. Another effect that is frequently seen is that the value of the temperature is overestimated. AC coupling through the capacitor works by ensuring that the time averaged current passing through it is zero. If the temperature is underestimated then the current in the positive state will be of a greater magnitude than in the negative state. This will AC couple the resultant current to offset all currents by a large negative amount, which causes particular issues because the current in the floating state is no longer zero. An effect that is discussed in detail in subsection 3.2.1.

The implementation of this offset correction finally allows the device to track the initial turning on of an $E_p = 0.52$ J HiPIMS pulse, as can be seen in Figure 5.8.

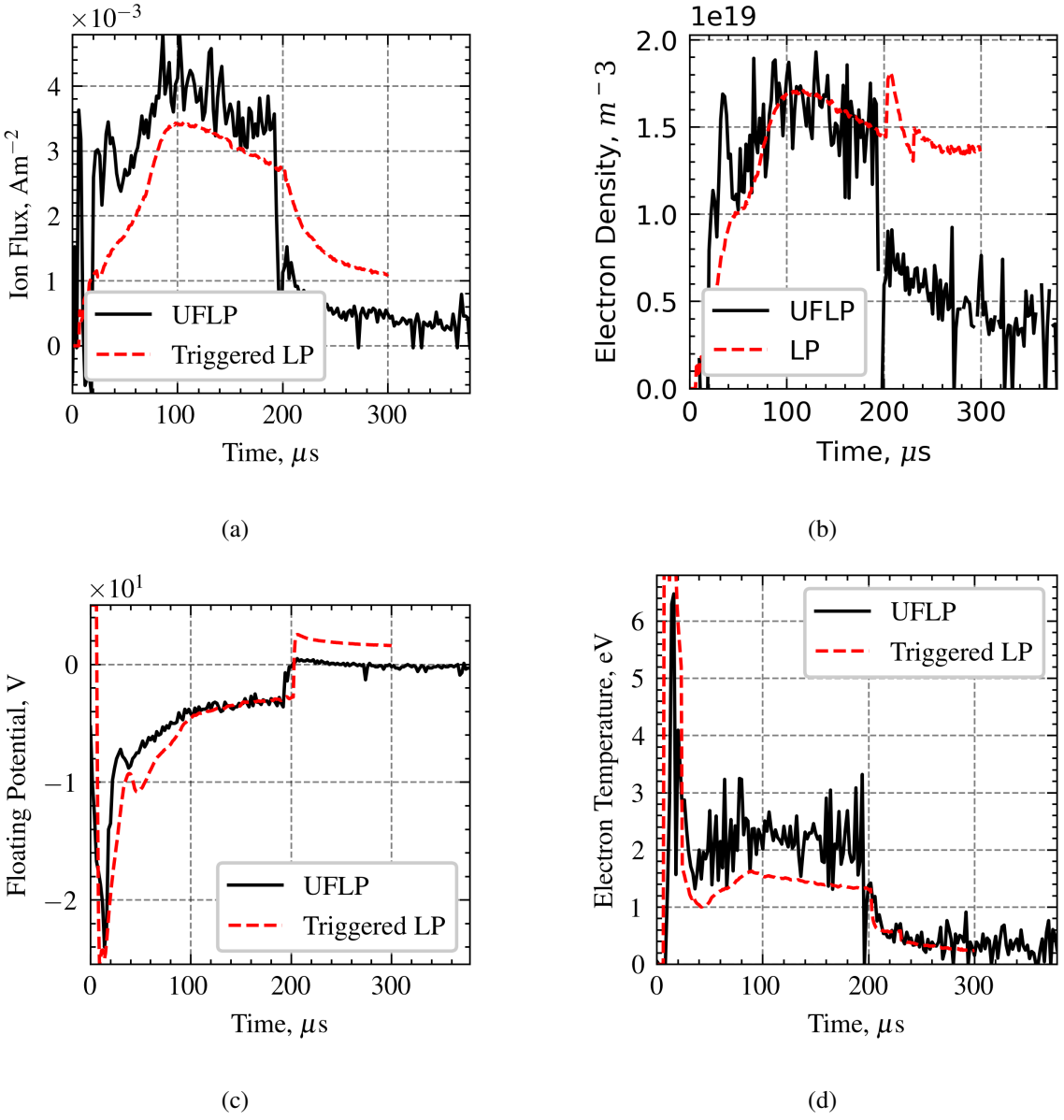


Figure 5.8: Measurements gathered at 500 kHz using a single probe multiplexed at dynamic bias at values $V_{+,-,0}$ = 0.64Te V, -3.325Te V and 0 V in a E_p = 1.72 J HiPIMS plasma. (a) ion flux, (b) plasma density, (c) floating potential and (d) electron temperature

Unfortunately spokes were not observed in a HiPIMS setting. This is down to a lack of temporal resolution caused by limitations in the electrical design that was successfully tested. As explained in section 2.1, spoke are known to be able to be resolved due to Nyquist theorem in the 333 kHz to 666 kHz range. As seen in Figure 5.9 this is outside of the boundaries of an FFT performed on 500 kHz data. For clarity the aliased effects are also included on the scale, which shows that there could be some phenomena

observed at 40 kHz (or 460 kHz). But the signal of these frequencies are so low in amplitude that it is more likely to just be detecting random fluctuations that attempting to resolve some periodic fluctuation.

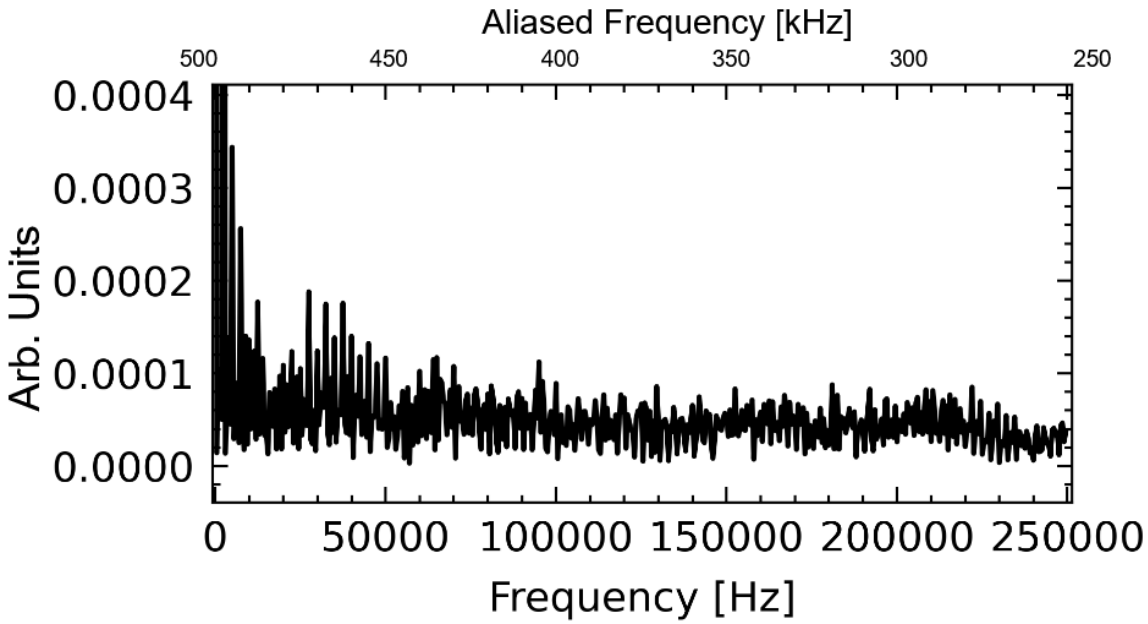


Figure 5.9: FFT of the results shown in Figure 5.8

By assuming that the spokes will have a total passing duration of 4.5 μs, a Python simulation can be computed to see how the algorithm would cope with such a fast data stream. Spokes are simulated by inducing a sine wave that has 15% of the ion saturation current amplitude, 30% of the electron temperature amplitude and 5% of the floating potential amplitude. This is over-layed onto the HiPIMS parameters taken from a conventional langmuir probe sweep from the same data set shown in Figure 5.8. This is comparable to spoke magnitudes seen in Lockwood-Estrin [40]. It is worth noting that the ion saturation current and floating potential will follow the trace at very high frequencies as in Python this is a very small correction and capacitive decoupling is presumed to be perfect.

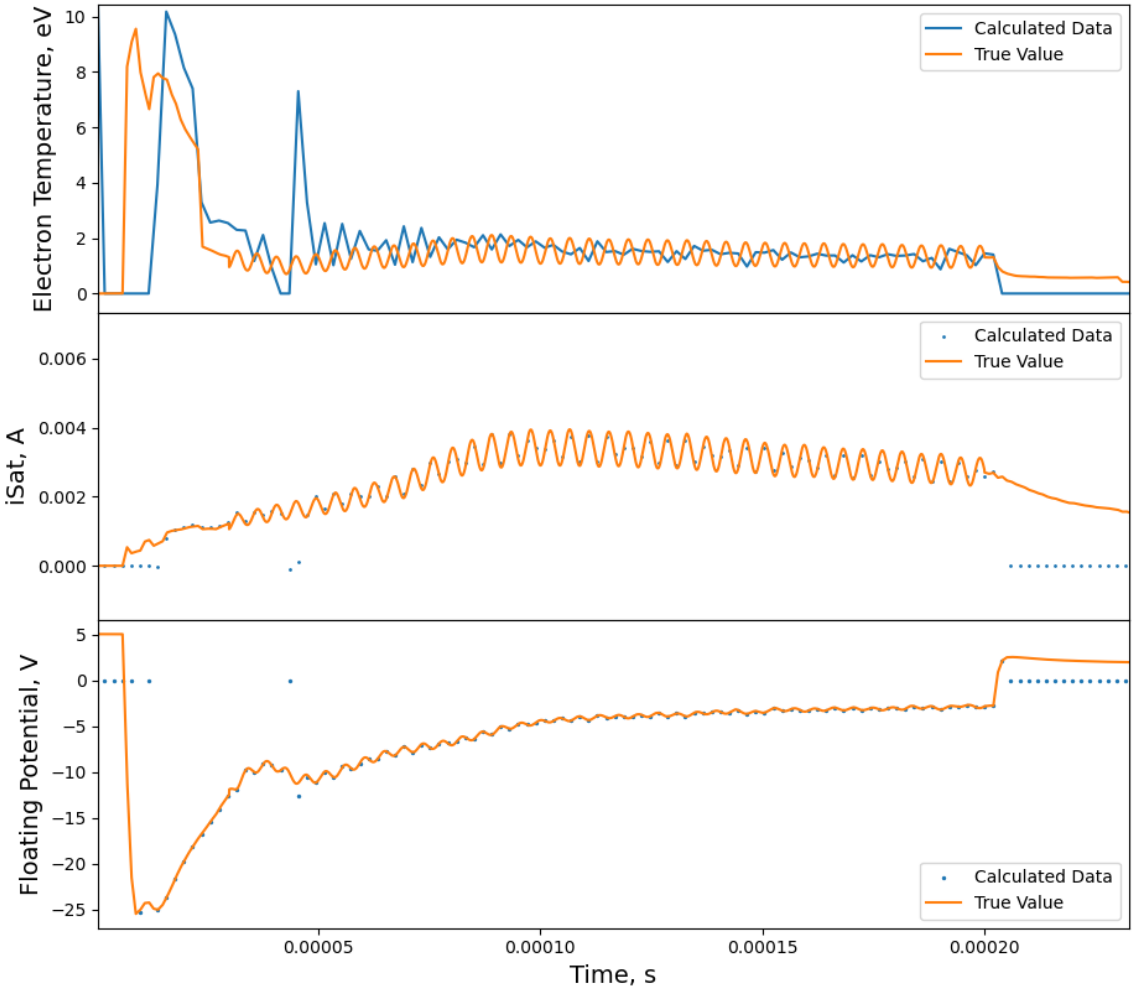


Figure 5.10: The results of a Python simulation that is computing spokes crossing a UFLP langmuir probe operating at 500 kHz with a spoke transit time of 4.5 μs. This shows that the algorithm does not successfully converge to a correct temperature that is tracked as spokes have too large of a linear velocity.

While operating the device in an attempt to detect spokes, the device is not quick enough or accurate enough to resolve the individual spokes. It is also worth noting that while this simulation considers the convergence of the algorithm and has built capacitance, it does not consider current flowing through the capacitor due to a non-zero time averaged current. Since filaments move significantly slower than spokes, filaments simulated with a total transit time of 32 μs, as in Figure 5.11, it can be seen that a filament would be successfully resolved with the devices current design.

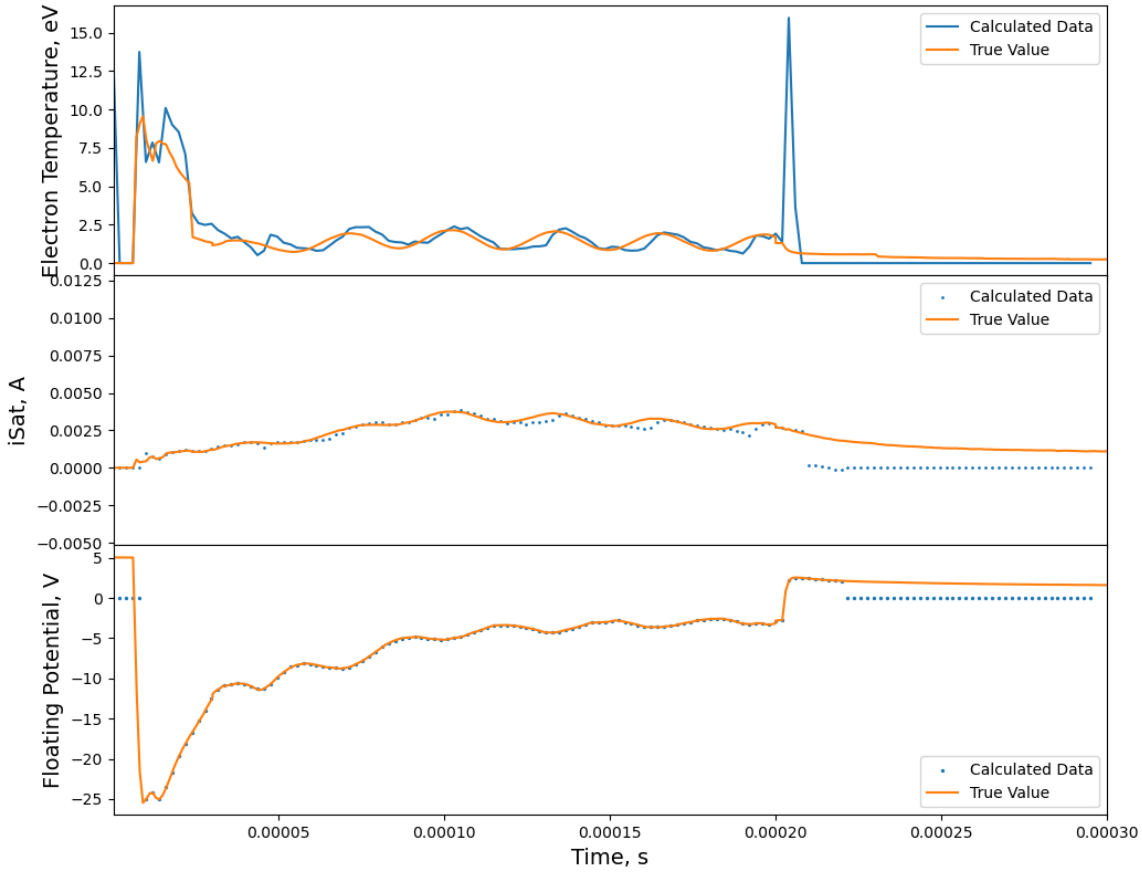


Figure 5.11: The results of a Python simulation that is computing spokes crossing a UFLP langmuir probe operating at 500 kHz with a filament transit time of 32 μs. Shows that the algorithm successfully converges to a correct temperature if it is applied to a similar filament that would be seen in MAST-U.

5.2 Implications for Installation onto MAST-U

The device has been tested on a real world plasma system and has returned time-resolved parameters of electron temperature, ion saturation current and floating potential at 500 kHz. Unfortunately this is not high enough time resolution to resolve spokes in a magnetron system. Spokes on a 0.25 mm radius probe have between a 3-6 μs period. This results in a nyquist frequency of 666 - 333 kHz, as explained in section 2.1. Slower spokes should be able to just be resolved, but only with between 2 and 3 data points per spoke. The limitation now rests with the FPGA and a faster clock speed ADC will be required to achieve higher time resolutions. While the device was not able to observe spokes, it was proven to accurately trigger and calculate close to accurate parameters of the duration of

the 200 μs HiPIMS pulse. It showed no measurable delay at the beginning of the pulse, contrary to the 90 μs delay shown in previous work done by McCarthy et al [88]. Spokes are known to have a greater linear velocity than filaments observed in the MAST tokamak by 5-10 factors. Given the evidence presented in this thesis, filaments should be able to be observed if this device was to be installed onto MAST-U.

The dummy probe was able to effectively cancel the cable capacitance via the use of an oscilloscope and tuning of the trimmer capacitance until the net measured current is zero with no plasma turned on. It has been noticed on some voltage current scans that there appears to be a capacitive effect during the HiPIMS pulse which could be distorting the final results. It is worth noting that in the magnetron system a total of 1.2 m of coaxial cable was used. For implementation onto MAST-U close to 50 m could be required to connect the FPGA and amplifier located in the south annex to the probes in the vessel. This will incur a significant capacitance (on the order of 1 nF), so a dummy probe will have to be utilised. This will either require the design and installation of a double probe system where one probe is isolated from the plasma, as seen in Figure 3.4, or using one of the "dead" probes located in the vessel as a dummy probe may be sufficient with the use of trimmer capacitors to calibrate the line.

Currently the collection of data is triggered by a software trigger that is activated via the Python API. Functionality to connect this trigger to a GPIO port has been installed but not utilised. The trigger only serves the purpose of data output and does not stop the device from collecting data. The device is currently configured to start collection on a single rising edge of a clock pulse and maintain either for a specified number of clock cycles (converted to an acquisition time in seconds in the API) or until a corresponding falling edge.

The benefits of a high speed probe to be installed onto MAST-U are to return high resolution time resolved data pertaining to the edge of the plasma. As discussed in section 1.3 no diagnostics in fusion are capable of returning electron temperature, ion saturation current and floating potential in real time. The access of this data in real time could prove invaluable to systems such as the plasma control system or the real time protections systems on MAST-U as the data could be vital for studies into ELM suppression. In addition to this, through the operation of multiple UFLP's, ideally located

along the same magnetic flux line, the formation of filaments could be studied, as seen in Figure 1.14.

Chapter 6

Conclusions

In this chapter the project will be summarised with consideration to achievements that have been made over pre-existing systems and improvements that can be made by the following PhD student who will be taking over development of this device in March 2023.

6.1 Summary

In summary, a number of goals of this project have been achieved. The original proof of concept developed by Vincent and McCarthy [87, 88] has been re-established with a new architecture and a new set of algorithms. The approach has been strengthened by the implementation of some real world considerations and working knowledge of electrical systems and components.

A capacitor switching circuit was developed that has a duel function of low temperature or high temperature systems. The range is modifiable further through small edits to the bit stream or replacement of some capacitor values. Currently the given range is effective for the currents that the device was subjected to in the low temperature system but there is no suitable region where the system is not frequency limited by the decoupling of the capacitor. This was partially addressed by the implementation of an algorithm to remove excess current in the zero state position, but this further leans on the assumption that the capacitor is correctly decoupling. If a change in floating potential

should be many times faster than the duration of an individual state, this assumption breaks down further.

Several iterations of a current and voltage sense circuit working at high bandwidths were tested, each with off the shelf components. These are connected to the capacitor switching circuit and feed information directly into the FPGA. The system was shown to correctly be able to measure current and voltage at high bandwidths.

The FPGA prototype itself was designed and built with real world considerations, ignoring some of the standardisation previously used by similar designs. By custom building some of the algorithms and making careful considerations for increasing the efficiency via parrelisation, the time resolution has been improved from 140 kHz set by McCarthy [88] to 500 kHz. The gathered results were compared against a trigger Langmuir probe system using an Impedans ALP-1000, and gathered IV curves over a period of 120 seconds. The IV curves were then analysed in the conventional way to return the 4 parameters before being overlaid to data collected from the UFLP. The efficacy of this frequency was tested in a the known environment of a HiPIMS plasma system with a pulse duration of only 200 μs. Another significant improvement was that the algorithm produced by McCarthy [88] required of the order of 100 μs for the algorithm to go from a initial guess state to an output state. Had this been applied to the HiPIMS system, data at the beginning of the pulse would have been lost. The improvements of data collection is largely down to a more detailed understanding of the way that the algorithm can cause a current offset due to incorrectly applied temperatures, which severely slows down convergence time.

6.2 Future Work

The development of the Ultra-Fast Langmuir probe will continue as a collaboration between University of Liverpool and Culham Centre for Fusion energy with the appointment of a new PhD student commencing March 2023. The next stages for development will include:

- Concept design and implementation of a new probe head / dummy probe system

for installation onto MAST-U.

- Connection of prototype to MAST-U DATAQ system
- Consideration for porting the design to a faster clock rate FPGA
- Configure appropriate capacitor ranges for the plasma that is desired to be resolved.
- Work towards implementation of multiple UFLP's onto MAST-U to aid in studies on filimentary transport.

As well as highlighting the main areas for consideration before the device can be installed onto MAST-U, I will also highlight some regions where I expect there could be difficulties. The main issues for consideration will revolve around a solution regarding the length of cabling required to reach to probe tip from the device could be significant. This will attenuate the available current and perhaps even apply unintended filtering affects to the applied signal as discussed in section 2.1. In addition to this, a power supply solution will have to be sourced that will be capable of driving voltages up to $\pm$200 V (if mounted on the reciprocating probe) or voltages up to approx 30 V (if mounted in the divertor). Both of these cases will have to be able to draw several amperes of current. For reasons discussed in subsection 3.2.1, any new operators will have to consider the plasma phenomena that is intended to be resolved. If there is a fast fluctuation in the value of floating potential this will have to be considered when choosing the capacitor ranges for application to maximise floating potential resolution, but not to attenuate drawn current.

References

[1] M. A. Islam et al. “Energy demand forecasting”. In: *Energy for Sustainable Development: Demand, Supply, Conversion and Management* (Jan. 2020), pp. 105–123. DOI: 10.1016/B978-0-12-814645-3.00005-5.

[2] Xuemei Jiang and Dabo Guan. “Determinants of global CO2 emissions growth”. In: *Applied Energy* 184 (Dec. 2016), pp. 1132–1141. ISSN: 03062619. DOI: 10.1016/J.APENERGY.2016.06.142.

[3] T.E.G. Nicholas et al. “Re-examining the role of nuclear fusion in a renewables-based energy mix”. In: *Energy Policy* 149 (2021), p. 112043. ISSN: 0301-4215. DOI: https://doi.org/10.1016/j.enpol.2020.112043.

[4] Steve Fetter, E.T Cheng, and F.M Mann. “Long-term radioactive waste from fusion reactors: Part II”. In: *Fusion Engineering and Design* 13.2 (1990), pp. 239–246. ISSN: 0920-3796. DOI: https://doi.org/10.1016/0920-3796(90)90104-E.

[5] A. S. Eddington. “The internal constitution of the stars”. In: *Nature* 106.2653 (1920), pp. 14–20. ISSN: 00280836. DOI: 10.1038/106014A0.

[6] F. W. Aston. “Isotopes and Atomic Weights”. In: *Nature* 105.2646 (July 1920), pp. 617–619. ISSN: 0028-0836. DOI: 10.1038/105617A0.

[7] A. Einstein. “Zur Elektrodynamik bewegter Körper”. In: *Annalen der Physik* 517.S1 (Feb. 1905), pp. 194–224. ISSN: 1521-3889. DOI: 10.1002/ANDP.2005517S113.

[8] Fastfission. *Binding Energy Per Nucleon*. Online at: https://commons.wikimedia.org/wiki/File:Binding_energy_curve_-_common_isotopes.svg. Date Accessed: [11/08/2017]. 2008.

[9] V Zerkin. *ENDF: Evaluated Nuclear Data File*. Online at: https://www-nds.iaea.org/exfor/endf.htm. Date Accessed: [07/11/2022]. 2022.

[10] W. M. Nevins and R. Swain. “The thermonuclear fusion rate coefficient for p-11B reactions”. In: *Nuclear Fusion* 40.4 (Apr. 2000), p. 865. ISSN: 0029-5515. DOI: 10.1088/0029-5515/40/4/310.

[11] M. Kikuchi et al. *Fusion Physics*. Publication. International Atomic Energy Agency, 2012. ISBN: 9789201304100.

[12] J D Lawson. “Some Criteria for a Power Producing Thermonuclear Reactor”. In: *Proceedings of the Physical Society. Section B* 70.1 (Jan. 1957), pp. 6–10. ISSN: 0370-1301. DOI: 10.1088/0370-1301/70/1/303.

[13] Dstrozzi. *Lawson Ignition Critereon Triple Product*. Online at: https://commons.wikimedia.org/wiki/File:Fusion_ntau.svg. Date Accessed: [20/01/2023]. 2010.

[14] J. Kenneth. Shultis, Richard E. Faw, and Douglas S. McGregor. *Fundamentals of Nuclear Science and Engineering Third Edition*. CRC Press, 2016, p. 661. ISBN: 1498769314.

[15] A R Christopherson and J D Lawson. “Some Criteria for a Power Producing Thermonuclear Reactor Recent citations A comprehensive alpha-heating model for inertial confinement fusion Some Criteria for a Power Producing Thermonuclear Reactor”. In: *Proceedings of the Physical Society. Section B J D Lawson Proc. Phys. Soc. B* 70 (1957).

[16] G F Matthews et al. “JET ITER-like wall—overview and experimental programme”. In: *Physica Scripta* T145.T145 (Dec. 2011), p. 014001. ISSN: 0031-8949. DOI: 10.1088/0031-8949/2011/T145/014001.

[17] X. Litaudon et al. “Overview of the JET results in support to ITER”. In: *Nuclear Fusion* 57.10 (Oct. 2017), p. 102001. ISSN: 0029-5515. DOI: 10.1088/1741-4326/aa5e28.

[18] Ken Tomabechi et al. “ITER conceptual design”. In: *Nuclear Fusion* 31 (1991), pp. 1135 –1224.

[19] I.E. Tamm. “Theory of the magnetic thermonuclear reactor, part I”. In: *Plasma Physics and the Problem of Controlled Thermonuclear Reactions* (1959), p. 3.

[20] V P Smirnov. “Tokamak foundation in USSR/Russia 1950–1990”. In: *Nuclear Fusion* 50.1 (2010), p. 14003.

[21] Kevin Ollegott et al. “Fundamental Properties and Applications of Dielectric Barrier Discharges in Plasma-Catalytic Processes at Atmospheric Pressure”. In: *Chemie-Ingenieur-Technik* 92.10 (Oct. 2020), pp. 1542–1558. ISSN: 15222640. DOI: 10.1002/CITE.202000075.

[22] James Wesson. “Tokamaks 3rd Edition by John Wesson”. In: *Journal of Plasma Physics* 71.3 (June 2005), pp. 377–377. ISSN: 0022-3778. DOI: 10.1017/S0022377804003058.

[23] Euro Fusion. *Tokamak principle — EUROfusion*. Online at: https://www.euro-fusion.org/2011/09/tokamak-principle-2/. Date Accessed: [05/02/2018].

[24] J. G. Cordey et al. “Scaling of the energy confinement time with β and collisionality approaching ITER conditions”. In: *Nuclear Fusion* 45.9 (Aug. 2005), p. 1078. ISSN: 0029-5515. DOI: 10.1088/0029-5515/45/9/007.

[25] J. File, R. G. Mills, and G. V. Sheffield. “Large Superconducting Magnet Designs for Fusion Reactors”. In: *IEEE Transactions on Nuclear Science* 18.4 (1971), pp. 277–282. ISSN: 0018-9499. DOI: 10.1109/TNS.1971.4326354.

[26] Neil Mitchell et al. “Superconductors for fusion: a roadmap”. In: *Superconductor Science and Technology* 34.10 (Sept. 2021), p. 103001. ISSN: 0953-2048. DOI: 10.1088/1361-6668/AC0992.

[27] *ITER Technical Basis*. ITER EDA Documentation Series 24. Online at: https://www.iaea.org/publications/6492/iter-technical-basis. Date Accessed: [25/06/2023]. Vienna: INTERNATIONAL ATOMIC ENERGY AGENCY, 2002.

[28] I.T. Chapman et al. “Overview of MAST results”. In: *Nuclear Fusion* 55.10 (Oct. 2015), p. 104008. ISSN: 0029-5515. DOI: 10.1088/0029-5515/55/10/104008.

[29] UKAEA. *MAST Upgrade Research Plan*. Tech. rep. Online at: https://ccfe.ukaea.uk/wp-content/uploads/2019/12/MAST-U_RP_2019_v1.pdf. Date Accessed: [25/06/2023]. UKAEA, 2019.

[30] A. Loarte et al. “Plasma detachment in JET Mark I divertor experiments”. In: *Nuclear Fusion* 38.3 (Mar. 1998), p. 331. ISSN: 0029-5515. DOI: 10.1088/0029-5515/38/3/303.

[31] Andrew Kirk and et al. *MAST Upgrade Research Plan*. Tech. rep. Online at: http://www.ccfe.ac.uk/assets/documents/other/MAST-U_RP_v3.pdf. Date Accessed: [25/06/2023]. Culham Center for Fusion Energy, 2015.

[32] Joe Milnes et al. "MAST Upgrade – Construction Status". In: *Fusion Engineering and Design* 96-97 (Oct. 2015), pp. 42–47. ISSN: 0920-3796. DOI: 10.1016/J.FUSENGDES.2015.03.002.

[33] Graham McArdle, Luigi Pangione, and Martin Kochan. "The MAST Upgrade plasma control system". In: *Fusion Engineering and Design* 159 (Oct. 2020), p. 111764. ISSN: 0920-3796. DOI: 10.1016/J.FUSENGDES.2020.111764.

[34] Stephanie Hall, Phillippe Jacquet, and Graham Naylor. "The real-time protection system for MAST-U". In: *Fusion Engineering and Design* 146 (Sept. 2019), pp. 421–425. ISSN: 09203796. DOI: 10.1016/J.FUSENGDES.2018.12.082.

[35] M. R. Gilbert et al. "Perspectives on multiscale modelling and experiments to accelerate materials development for fusion". In: *Journal of Nuclear Materials* 554 (Oct. 2021). ISSN: 00223115. DOI: 10.1016/j.jnucmat.2021.153113.

[36] Andrea Murari et al. "Exploratory Data Analysis Techniques to Determine the Dimensionality of Complex Nonlinear Phenomena: The L-to-H Transition at JET as a Case Study". In: *IEEE Transactions on Plasma Science* 40.5 (2012), pp. 1386–1394. DOI: 10.1109/TPS.2012.2187682.

[37] J. R. Harrison et al. "Overview of new MAST physics in anticipation of first results from MAST Upgrade". In: *Nuclear Fusion* 59.11 (June 2019), p. 112011. ISSN: 0029-5515. DOI: 10.1088/1741-4326/AB121C.

[38] A. W. Morris. "MAST: Results and upgrade activities". In: *IEEE Transactions on Plasma Science* 40.3 PART 1 (Mar. 2012), pp. 682–691. ISSN: 00933813. DOI: 10.1109/TPS.2011.2181540.

[39] P Poolcharuansin and J W Bradley. "Plasma Sources Science and Technology Short-and long-term plasma phenomena in a HiPIMS discharge". In: *Plasma Sources Sci. Technol* 19 (2010), p. 25010. DOI: 10.1088/0963-0252/19/2/025010.

[40] F Lockwood Estrin, S Karkari, and J W Bradley. "Triple probe interrogation of spokes in a HiPIMS discharge". In: *Journal of Physics D: Applied Physics* 50.29 (2017).

[41] D A D'ippolito, J R Myra, and S I Krasheninnikov. "Cross-field blob transport in tokamak scrape-off-layer plasmas". In: *Physics of Plasmas* 9 (2002), p. 222. DOI: 10.1063/1.1426394.

[42] D A D'ippolito, J R Myra, and S J Zweben. "Convective transport by intermittent blob-filaments: Comparison of theory and experiment". In: *Phys. Plasmas* 18 (2011), p. 60501. DOI: 10.1063/1.3594609.

[43] E. Pajuste et al. "Tritium retention in plasma facing materials of JET ITER-Like-Wall retrieved from the vacuum vessel in 2012 (ILW1), 2014 (ILW2) and 2016 (ILW3)". In: *Nuclear Materials and Energy* 27 (June 2021), p. 101001. ISSN: 2352-1791. DOI: 10.1016/J.NME.2021.101001.

[44] B Lipschultz et al. "Plasma-surface interaction, scrape-off layer and divertor physics: implications for ITER". In: *Nucl. Fusion* 47 (2007), pp. 1189–1205. DOI: 10.1088/0029-5515/47/9/016.

[45] N. R. Walkden, B. D. Dudson, and G. Fishpool. "Characterization of 3D filament dynamics in a MAST SOL flux tube geometry". In: *Plasma Physics and Controlled Fusion* 55.10 (Oct. 2013). ISSN: 07413335. DOI: 10.1088/0741-3335/55/10/105005.

[46] I Adamovich et al. "The 2017 Plasma Roadmap: Low temperature plasma science and technology Topical Review". In: *Journal of Physics D: Applied Physics* 32 (2017), p. 46. DOI: 10.1088/1361-6463/aa76f5.

[47] Paul K. Chu. *Low Temperature Plasma Technology : Methods and Applications*. CRC Press (an imprint of Taylor & Francis), 2013. ISBN: 978-1-4665-0990-0.

[48] Edbertho Leal-Quirós. "Plasma processing of municipal solid waste". In: *Brazilian Journal of Physics* 34.4 B (2004), pp. 1587–1593. ISSN: 01039733. DOI: 10.1590/S0103-97332004000800015.

[49] Dengming Xiao. "Fundamental Theory of Townsend Discharge". In: *Gas Discharge and Gas Insulation*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2016, pp. 47–88. ISBN: 978-3-662-48041-0. DOI: 10.1007/978-3-662-48041-0_3.

[50] Peter M. Martin. *Handbook of Deposition Technologies for Films and Coatings*. 3rd ed. Elsevier, 2009, pp. 1–912. ISBN: 081552031X.

[51] Mitsuharu Konuma. *Film Deposition by Plasma Techniques*. Ed. by Gunter Ecker et al. Berlin, Heidelberg: Springer Berlin Heidelberg, 1992. ISBN: 978-3-642-84513-0. DOI: 10.1007/978-3-642-84511-6.

[52] D. H. Boone. "Physical vapour deposition processes". In: *http://dx.doi.org/10.1179/mst.1986.2.3.220* 2.3 (2013), pp. 220–224. ISSN: 17432847. DOI: 10.1179/MST.1986.2.3.220.

[53] Wolf Dieter Münz. "The unbalanced magnetron: current status of development". In: *Surface and Coatings Technology* 48.1 (Oct. 1991), pp. 81–94. ISSN: 0257-8972. DOI: 10.1016/0257-8972(91)90130-O.

[54] J. Musil. "Recent advances in magnetron sputtering technology". In: *Surface and Coatings Technology* 100-101.1-3 (Mar. 1998), pp. 280–286. ISSN: 0257-8972. DOI: 10.1016/S0257-8972(97)00633-6.

[55] G. Bräuer et al. "Magnetron sputtering – Milestones of 30 years". In: *Vacuum* 84.12 (June 2010), pp. 1354–1359. ISSN: 0042-207X. DOI: 10.1016/J.VACUUM.2009.12.014.

[56] W. D. Münz et al. "Industrial applications of HIPIMS". In: *Journal of Physics: Conference Series* 100.8 (Mar. 2008), p. 082001. ISSN: 1742-6596. DOI: 10.1088/1742-6596/100/8/082001.

[57] N. Brenning et al. "A bulk plasma model for dc and HiPIMS magnetrons". In: *Plasma Sources Science and Technology* 17.4 (Aug. 2008), p. 045009. ISSN: 0963-0252. DOI: 10.1088/0963-0252/17/4/045009.

[58] J. G. Clark, M. D. Bowden, and R. Scannell. "Low temperature Thomson scattering on MAST-U". In: *Review of Scientific Instruments* 92.4 (Apr. 2021), p. 043545. ISSN: 0034-6748. DOI: 10.1063/5.0043813.

[59] A. Pospieszczyk. "Spectroscopic Diagnostics of Tokamak Edge Plasmas". In: *Physica Scripta* 2005.T119 (Jan. 2005), p. 71. ISSN: 1402-4896. DOI: 10.1088/0031-8949/2005/T119/013.

[60] J. G. Clark et al. "First divertor Thomson scattering measurements on MAST-U". In: *Review of Scientific Instruments* 93.10 (Oct. 2022), p. 103534. ISSN: 0034-6748. DOI: 10.1063/5.0101635.

[61] J. Adamek et al. “On the transport of edge localized mode filaments in the tokamak scrape-off layer”. In: *Nuclear Fusion* 60.9 (Aug. 2020), p. 096014. ISSN: 0029-5515. DOI: 10.1088/1741-4326/AB9E14.

[62] K. J. Brunner et al. “Real-time dispersion interferometry for density feedback in fusion devices”. In: *Journal of Instrumentation* 13.09 (Sept. 2018), P09002. ISSN: 1748-0221. DOI: 10.1088/1748-0221/13/09/P09002.

[63] R. Scannell et al. “Design of a new Nd:YAG Thomson scattering system for MAST”. In: *Review of Scientific Instruments* 79.10 (Oct. 2008), 10E730. ISSN: 0034-6748. DOI: 10.1063/1.2971971.

[64] M. Bassan et al. “Thomson scattering diagnostic systems in ITER”. In: *Journal of Instrumentation* 11.01 (Jan. 2016), p. C01052. ISSN: 1748-0221. DOI: 10.1088/1748-0221/11/01/C01052.

[65] Albert A. Michelson and Edward W. Morley. “Relative Motion of the Earth and the Luminiferous Ether”. In: *American Journal of Science* 34.203 (1887).

[66] L Z. Zehnder. “Ein neuer interferenzrefraktor”. In: *Zeitschrift fur Instrumentenkunde* 11 (1891), pp. 275–285.

[67] Ludwig Mach. “Ueber einen Interferenzrefraktor”. In: *Zeitschrift fur Instrumentenkunde* 12 (1892), pp. 89–93.

[68] T. O’Gorman et al. “Design of a real-time two-color interferometer for MAST Upgrade”. In: *Review of Scientific Instruments* 85.11 (Sept. 2014), p. 11D861. ISSN: 0034-6748. DOI: 10.1063/1.4894394.

[69] Thomas Middleton Farley. “Analysis of Plasma Filaments with Fast Visible Imaging in the Mega Ampère Spherical Tokamak”. PhD thesis. Liverpool: University of Liverpool, July 2019, pp. 1–214.

[70] H. M. Mott-Smith and Irving Langmuir. “The Theory of Collectors in Gaseous Discharges”. In: *Physical Review* 28.4 (Oct. 1926), pp. 727–763. ISSN: 0031-899X. DOI: 10.1103/PhysRev.28.727.

[71] J. D. Swift, M. J. R. Schwar, and John H. Keller. “Electrical Probes for Plasma Diagnostics”. In: *Journal of The Electrochemical Society* (1971). ISSN: 00134651. DOI: 10.1149/1.2408098.

[72] Sin-Li Chen et al. “Understanding Langmuir probe current-voltage characteristics”. In: *American Journal of Physics* 36.8 (1965), p. 1078. DOI: 10.1063/1.1714492.

[73] G.A. Naylor. “An FPGA based control unit for synchronization of laser Thomson scattering measurements to plasma events on MAST”. In: *Fusion Engineering and Design* 85.3-4 (2010), pp. 280–285. ISSN: 09203796. DOI: 10.1016/j.fusengdes.2010.04.042.

[74] Kai Jakob Brunner. “FPGA-based High Performance Diagnostics For Fusion”. PhD thesis. University of Durham, Mar. 2017.

[75] Andrew Moore and Ron Wilson. *FPGAs For Dummies*. 2nd ed. Hoboken: John Wiley & Sons, Inc., 2017. ISBN: 978-1-119-39047-3.

[76] Clive Maxfield. *The Design Warrior’s Guide to FPGAs*. Burlinton: Newnes, 2004. ISBN: 1865843830.

[77] IEEE. *IEEE Standard VHDL Language Reference Manual*. Online at: https://perso.telecom-paristech.fr/guilley/ENS/20171205/TP/tp_syn/doc/IEEE_VHDL_1076-1993.pdf. Date Accessed: [10/09/2019]. 1993.

[78] IEEE Computer Society. *IEEE Standard Verilog Hardware Description Language*. Online at: http://www-inst.eecs.berkeley.edu/~cs150/fa06/Labs/verilog-ieee.pdf. Date Accessed: [10/09/2019]. 2001.

[79] P. Horowitz and W. Hill. *The Art of Electronics*. Cambridge University Press, 2015. ISBN: 9780521809269.

[80] Aiken Pang and Peter Membrey. *Beginning FPGA : programming metal, your brain on hardware*. Apress, 2017. ISBN: 9781430262473.

[81] Chetvorno. *State diagram for turnstile*. Online at: https://en.wikipedia.org/wiki/Finite-state_machine. Date Accessed: [25/06/2023].

[82] Koheron. *Koheron Software Development Kit*. Online at: https://www.koheron.com/software-development-kit/. Date Accessed: [25/06/2023].

[83] Charles Vincent. “FPGA Based Diagnostics for the Mega-Amp Spherical Tokamak Upgrade”. PhD thesis. The University of Durham, Jan. 2021.

[84] Koheron. *Koheron Software Development Kit Github*. Online at: https://github.com/koheron/koheron-sdk. Date Accessed: [25/06/2023].

[85] Laurence Anthony Lyons. “Construction and Operation of a Mirror Langmuir Probe Diagnostic for the Alcator C-Mod Tokamak”. PhD thesis. Massachusetts Institute of Technology, 2005.

[86] B Labombard and L Lyons. “Mirror Langmuir probe: A technique for real-time measurement of magnetized plasma conditions using a single Langmuir electrode.” In: *Review of Scientific Instruments* (2007). DOI: 10.1063/1.2754392.

[87] C Vincent et al. “The Digital Mirror Langmuir Probe : Field Programmable Gate Array Implementation of Real-Time Langmuir Probe Biasing”. In: *Review of Scientific Instruments* 90.8 (2019), pp. 1–7.

[88] W. McCarthy et al. “First application of a digital mirror Langmuir probe for real-time plasma diagnosis”. In: *Review of Scientific Instruments* 92.10 (Oct. 2021), pp. 1–6. ISSN: 0034-6748. DOI: 10.1063/5.0057318.

[89] Kevin B. Woller, Dennis G. Whyte, and Graham M. Wright. “Isolated nano-tendril bundles on tungsten surfaces exposed to radiofrequency helium plasma”. In: *Nuclear Materials and Energy* 12 (Aug. 2017), pp. 1282–1287. ISSN: 23521791. DOI: 10.1016/j.nme.2017.04.016.

[90] K. B. Woller, D. G. Whyte, and G. M. Wright. “Broad ion energy distributions in helicon wave-coupled helium plasma”. In: *Physics of Plasmas* 24.5 (May 2017). ISSN: 10897674. DOI: 10.1063/1.4983315.

[91] G. M. Wright et al. “An experiment on the dynamics of ion implantation and sputtering of surfaces”. In: *Review of Scientific Instruments* 85.2 (Feb. 2014), p. 023503. ISSN: 0034-6748. DOI: 10.1063/1.4861917.

[92] Martin Greenwald et al. “20 years of research on the Alcator C-Mod tokamak”. In: *Physics of Plasmas* 21.11 (2014), p. 110501.

[93] Belle A. Shenoi. *Introduction to digital signal processing and filter design*. Wiley, 2005, p. 423. ISBN: 9780471656388.

[94] Peter Leban. *Red Pitaya User Manual*. Online at: http://docs-asia.electrocomponents.com/webdocs/144a/0900766b8144a693.pdf. Date Accessed: [09/09/2019]. 2014.

[95] Stemlabs. *Red Pitaya 14-bit version*. Online at: https://redpitaya.com/stemlab-125-14/. Date Accessed: [25/06/2023].

[96] Robert Elliot Goldschmidt. "Applications of Division by Convergence". PhD thesis. Boston: Massachusetts Institute of Technology, June 1964, pp. 1–44.

[97] Texas Instruments. *INA111 Instrumentation Amplifier*. Online at: https://www.ti.com/lit/ds/symlink/ina111.pdf. Date Accessed: [22/10/2022]. 1992.

[98] Mouser Electronics. *W117SIP-1 Reed Relay Datasheet*. Online at: https://www.mouser.com/datasheet/2/357/105A_117SIP_107DIP_171DIP-6475.pdf. Date Accessed: [25/06/2023].

[99] Francis Lockwood Estrin. "The study of spokes in HiPIMS discharges with applications to the production of superconducting thin films". PhD thesis. Liverpool: University of Liverpool, Sept. 2016.

[100] Impedans. *ALP System Advanced Langmuir Probe for Plasma Characterisation and Diagnostics*. Online at: https://www.ccrprocessproducts.com/wp-content/uploads/customfield/F12-134006_Impedans_ALP_System_R1.0.pdf. Date Accessed: [22/02/2023].

Appendix A

FPGA Goldschmidt Algorithm

In this appendix I have included a snippet of the VHDL code I made to perform a Goldschmidt division. The basic step by step explanation of how this algorithm works is explained in subsection 2.5.1. The algorithm returns a valid division signal and also the completed division (quotient). This only runs for a total number of cycles of m, so in this case the total number of iterations will be $\frac{m}{2}$ as N and D must be on a different clock cycle to F. The key benefit to a custom division algorithm like this is the ability to customise the number of clock cycles per division. The only division that may cause issues is $\frac{V_p - V_f}{T_e}$, where T_e has a minimum bit value of 50 to ensure that the bias level doesn't shrink to return currents below the noise floor. As explained by Figure 2.9, this should conveniently minimise any issues with loss of accuracy caused by a reduced iteration count.

A.1 Code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity gold is
   GENERIC(
      n: integer:= 14;
```

```
      p: integer:= 17; -- p - n = points above decimal point
      m: integer:= 32);
   port (
      clk : in std_logic;
      rst : in std_logic;

      div_complete : out std_logic;

      Numerator : in std_logic_vector(n-1 downto 0);
      Denominator : in std_logic_vector(n-1 downto 0);

      Quotient : out std_logic_vector(n-1 downto 0)
      -- 2n - p = power of answer e.g. n=14, p=16, answer is 2_12 =>
         quotient / 2**12 = answer
   );
end gold;

architecture rtl of gold is
   Signal N_Resize : signed(p downto 0);
   Signal N_Multiply : signed(2*p + 1 downto 0);
   Signal Prev_N : signed(p downto 0);

   Signal D_Resize : signed(p downto 0);
   Signal D_Multiply : signed(2*p + 1 downto 0);
   Signal Prev_D : signed(p downto 0);

   Signal Prev_F : signed(p downto 0);
   Signal F_Temp : signed(p downto 0);
   Signal F_solve : signed(p downto 0);

   Signal count: integer RANGE 0 TO m-1;
   TYPE finite_states IS (start, iterate, done, idle);
   Signal current_state: finite_states;
```

```
   Signal Current_Numerator : std_logic_vector(Numerator'range);
   Signal Current_Denominator : std_logic_vector(Denominator'range);
   Signal Last_Numerator : std_logic_vector(Numerator'range);
   Signal Last_Denominator : std_logic_vector(Denominator'range);
begin
   N_Multiply <= Prev_N * F_Temp;
   D_Multiply <= Prev_D * F_Temp;

   -- Solve N
   PROC_N : process(clk)
   begin
      if rising_edge(clk) then
         Prev_N <= N_Resize;
            Case current_state is
               when start =>
                  N_Resize <= to_signed(to_integer(signed(Numerator))
                     , N_Resize'length);
               when iterate =>
                  N_Resize <= shift_right(N_Multiply , n)(N_Resize'
                     range);
               when others => NULL;
            end case;
      end if;
   end process; -- PROC_N

   -- Solve D
   PROC_D : process(clk)
   begin
      if rising_edge(clk) then
         Prev_D <= D_Resize;
            Case current_state is
               when start =>
                  D_Resize <= to_signed(to_integer(signed(Denominator
                     )), D_Resize'length);
```

```
            when iterate =>
               D_Resize <= shift_right(D_Multiply + 1, n)(D_Resize
                  'range);
            when others => NULL;
         end case;
   end if;
end process; -- PROC_N

-- Solve F
PROC_F : process(clk)
begin
   if rising_edge(clk) then
      Prev_F <= F_Temp;
      Case current_state is
         when start =>
            F_Temp <= to_signed(to_integer(signed(Denominator)),
               F_Temp'length);
         when iterate =>
            F_Temp <= 2**(n+1) - D_Resize;
         when others => NULL;
      end case;
   end if;
end process; -- PROC_N

F_counter: PROCESS(clk)
BEGIN
   if rising_edge(clk) then
      if rst = '1' then
         count <= 0;
      else
         Case current_state is
            when start =>
               count <= (count+1);
            when iterate =>
```

```
                count <= (count+1);
            when others =>
                count <= 0;
         END case;
      end if;
   end if;
END PROCESS;

next_state: PROCESS(clk)
BEGIN
   if rising_edge(clk) then
      if rst = '1' then
         current_state <= start;
         div_complete <= '0';
      else
            CASE current_state IS
               WHEN start =>
                  if count = 1 then
                     current_state <= iterate;
                     div_complete <= '0';
                  end if;
               WHEN iterate =>
                  if count = m - 1 then
                     current_state <= done;
                  end if;
                  div_complete <= '0';
               WHEN done =>
                  div_complete <= '1';
                  Quotient <= std_logic_vector(N_Resize(N_Resize'
                     length - 1 downto N_Resize'length - Quotient'
                     length));
                  current_state <= idle;
               WHEN idle =>
                  div_complete <= '0';
```

```
                    current_state <= start;
                END CASE;
            end if;
        end if;
    END PROCESS;

    REQUEST_DIVISION : process(clk)
    begin
        if rising_edge(clk) then
            Current_Numerator <= Numerator;
            Current_Denominator <= Denominator;
            Last_Numerator <= Current_Numerator;
            Last_Denominator <= Current_Denominator;
        end if;
    end process; -- REQUEST_DIVISION
end architecture;
```

Appendix B

Prototype Block Design

A total block design of the UFLP combined with the Koheron based system has been included for clarity to show how some of the Koheron IP interacts with the UFLP. This also shows clearly how the 'sts' and 'ctl' registers receive data.

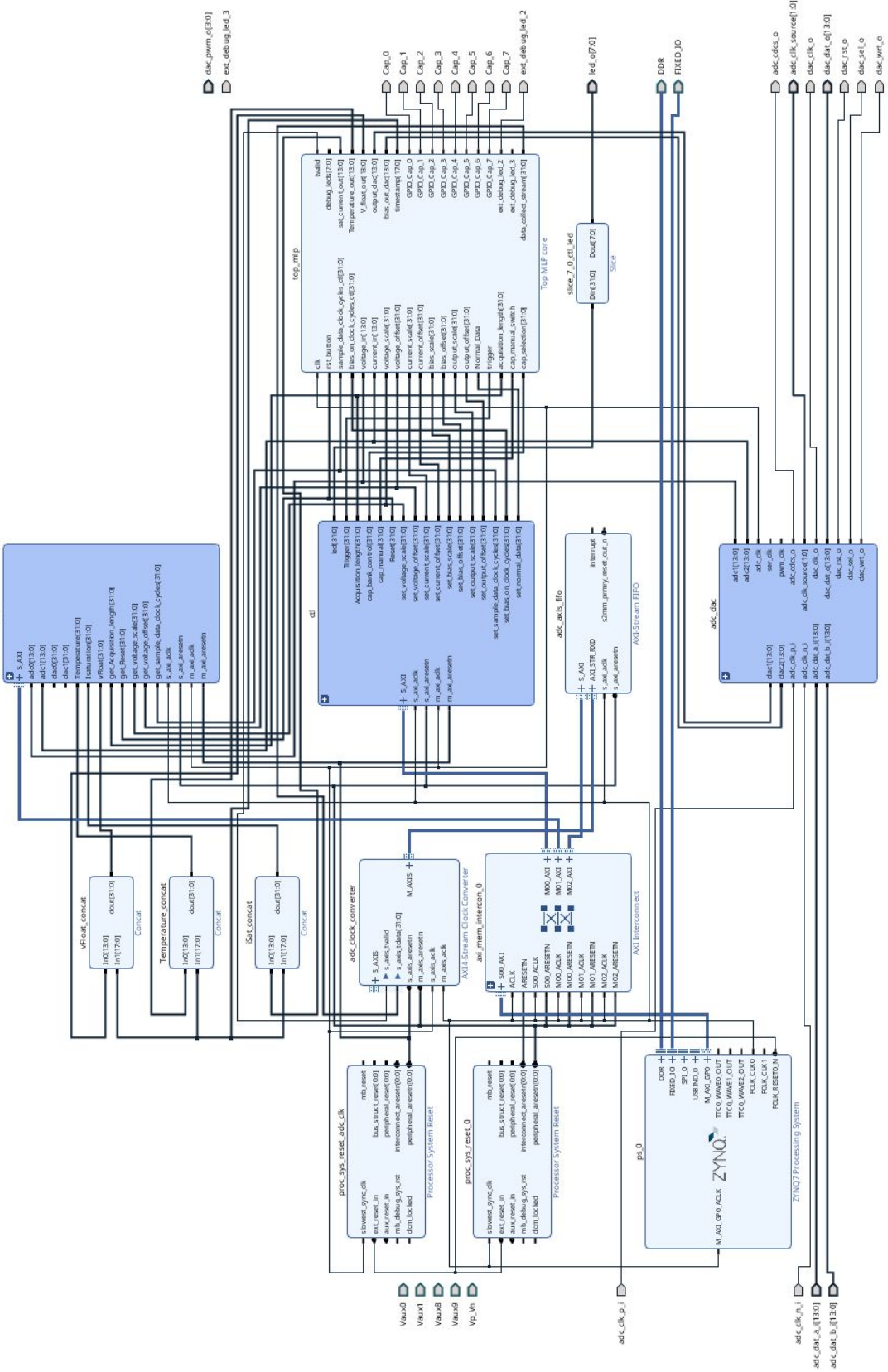


Figure B.1: Block Diagram of the entire Koheron framework integrated with the top module of the prototype.