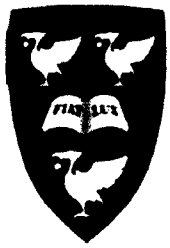

UNIVERSITY OF
LIVERPOOL

Failure Modes of Organic Devices

Thesis submitted in accordance with the requirements of the University of Liverpool for the degree of Doctor in Philosophy

by Joanna Ruth Sessford

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DEPARTMENT OF ELECTRICAL ENGINEERING AND ELECTRONICS

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Abstract

Research into Organic Electronics has increased dramatically over the past 20 years. Organic Electronics cannot compete with single crystal silicon for speed and circuit complexity, but it can be regarded as a competitor because of its potential to produce very large area circuits at low process temperatures and low cost.

Potential applications for conjugated polymer devices include photovoltaic cells (low cost solar panel), optical amplifiers, memory, displays (in conjunction with e-paper and large area LCD's) and radio frequency (RFID). Many of these devices will use Thin Film Transistors (TFTs).

TFT characteristics are therefore discussed with an emphasis on the hysteresis observed; the results observed indicate that one of the causes of hysteresis is ion movement.

A number of different current-voltage equations have been derived for the drain current channel. It is important to develop these equations to determine the effect of treating the real variation in the concentration of carriers, normal to the interface. In addition, how this large variation in the density of carriers gives rise to an enhancement of carrier mobility at the interface is approached, has been examined. It has been shown that for devices fabricated using PTAA; the most appropriate equation is that which assumes the exponential distribution of states depends on electron concentration.

MOS capacitors are important test structures; they are useful because of the light they shed on electrical instability in organic devices, MOS capacitors characteristics have therefore been discussed before the hysteresis they display has been examined.

The following mechanisms of hysteresis in MOS capacitors have been examined: carrier hopping, carrier percolation, gate leakage current, ion movement in the semiconductor and instability in the gate dielectric. The main causes of instability appear to be oxygen ions in the semiconductor and in the gate dielectric.

The hysteresis observed in Schottky diodes has also been examined; contributing factors appear to include ion movement and diffusion. Values for Meyer Neldels energy for Schottky diodes fabricated using Lisicon (undoped) have been calculated to be $5.0.10^{-21}$; this value increases when dopant is added; this is expected as doping introduces more states and at high levels of doping leads to Fermi level pinning.

As Organic Electronics is growing rapidly into an industry, it is vital to have a roadmap; to allow equipment manufacturers and semiconductor technologists to plan targets for the future, this piece of work provides a roadmap for Organic Electronics. One of the major potential uses of Organic Electronics is believed to be in the area of auto id/rf tags, for example, the replacement of the barcode, the roadmap therefore concentrates on this area; it

has been predicted that by the year 2030 full barcode replacement will be available at an economic cost.

Contents

Chapter 1

Introduction

An introduction to the subject of conjugated polymer devices is provided in this chapter. The organisation of the thesis and the motivation behind the work is also discussed along with details of the experimental techniques used.

1.1 Introduction to Conjugated Polymer Devices

Shirakawa, MacDiarmid and Heeger observed electrical conductivity in polyacetylene [1]; this led to extensive research in the area of conjugated polymers. Further investigation in the late 1970's, focussed around polyacetylene and other conjugated polymers including poly(p-phenylenevinylene) (PPV) [2] and poly(p-phenylene) (PPP) [3]. Nearly thirty years has passed since the first observation of electrical conductivity in conjugated polymers, while the focus of this thesis is on polytriarylamine (PTAA) which is a disordered material; the focus of research is now turning towards polycrystalline materials, such as Lisicon (which is touched upon in this work). There are an increasing number of potential applications for conjugated polymers, which takes advantage of their flexibility and relatively low fabrication costs, for example electronic newspapers and RFID tags which will eliminate the need for person operated checkouts in shops.

In the introduction to his thesis in 2000; Lloyd stated that conjugated polymers are all sensitive to oxygen and that this problem needs to be overcome [4], this is still the case.

The work in this thesis concentrates on the failure modes of organic devices, Schottky diodes, metal-oxide-semiconductor (MOS) capacitors and thin-film-transistors (TFTs) are examined. In this thesis, the majority of devices have been fabricated using PTAA, although some Schottky diode results were obtained from devices fabricated using Liscion.

1.2 Motivation and Thesis Organisation

Conjugated polymer physics is a relatively new subject. An overview of conjugated polymers and disordered material has been presented in chapter 2. Many potential applications will rely on TFT's, chapter 3 concentrates on this area. Different approximations can be used to develop the gradual channel equation. It is important to investigate this to examine the impact different approximations can have, this is examined in chapter 4.

Characterisation of MOS capacitors has been discussed in chapter 5, they form the basis of TFTs; they are also useful as they shed light on electrical instabilities in organic devices. Investigating the hysteresis is useful as the direction of hysteresis can indicate the mechanisms which lead to instability; this is discussed in chapter 6.

Schottky diodes including the values of T_c, T_o, the ideality factor, the Meyer Neldel Energy and hysteresis are discussed in chapter 7.

In silicon electronics Moore's law can be used to create a roadmap, organic electronics is growing quickly into an industry it is therefore important to have a roadmap; chapter 8 discusses the technical roadmapping of organic electronics.

1.3 Experimental Techniques Used in this Work

Various experimental tools have been employed during the course of this work. Polymer materials were obtained from Merck. Some devices were fabricated by Avecia (now Merck).

Electrical characteristics of Schottky diodes were performed using a PC-controlled Keithley voltage source and electrometer. Capacitance-voltage measurements were performed on a Hewlett-Packard Impedance Analyser. TFT characteristics were performed using a Hewlett-Packard Transistor Parameter Analyser.

1.4 Contributions

Contributions have been made to the work on stability, which is one of the main problems in this technology.

It has been shown that the delta function produces the same equation as the exponential distribution of states and that for an accurate approximation the exponential distribution of states and the dependence of mobility on the electron concentration, have to be considered. A technical roadmap for the area of organic electronics has also been produced.

1.5 References

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Chapter 2

Review of Conjugated Polymer Theory and Device Applications

Presented in this chapter is a review of conjugated polymers including their chemical structures and the dopant, 2,3-dichloro-5,6-dicyano-1,4-benzoquione, is also discussed briefly.

2.1 Introduction

Organic Electronics cannot compete with single crystal silicon for speed and circuit complexity but it can be regarded as a competitor because of its potential to produce very large area circuits at low process temperatures and at low cost. Polymer circuits can be produced from soluble materials which gives rise to fabrication techniques that their adherents claim is far more compatible with reel to sheet processing. A significant question is whether the devices made in these materials will obey the same device physics as those from solid ordered materials. This, if it were found to be the case would mean that a huge range of commercial software would become available for use by both device and circuit engineers. We therefore need to consider the theory of electrical conduction in such structures and attempt to interpret the conduction in terms of factors such as drift mobility, Debye length, and Einstein's Equation. Ultimately we need to understand whether the relationship between current density and the slope of the Fermi level, as found with single crystal semiconductors, or quasi Fermi level are valid.

2.2 Conjugated Polymers

Conjugated polymers and small molecules are used in a variety of applications, including light-emitting diodes (LEDs], display panels [2], photovoltaic devices [3-5] and image devices [6,7].

Numerical solutions to the Schrodinger equation are used to explain models for ordered conjugated polymers [8]. Conjugation is a description of the alternating system of single and double bonds. A σ (single) bond is formed between each pair of adjacent carbon atoms by the overlap of sp^2 hybrid orbital's [9]. The double bond consists of a π bond formed between two unhybridised p_z between adjacent carbon atoms, as shown in *figure 2.2.1*. In a conjugated system, the electrons in a π bond are delocalised and can therefore move within a few monomers of the bonding nuclei, this contributes to the electrical conductivity [10], because unlike in a system in which there are only single or double bonds present, the bonded orbitals are not localised to the region of the nuclei of the bonded atoms.

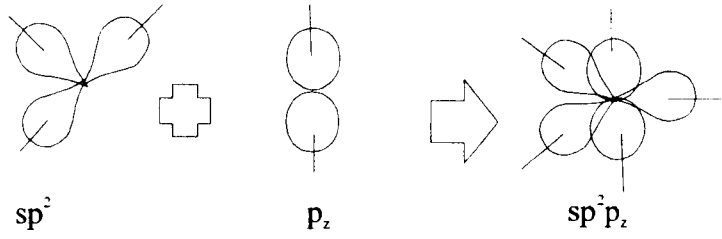

Figure 2.2.1: Overlap of the p_z atomic orbitals with the nearest neighbour for a typical conjugated polymer.

The earliest conjugated polymer is polyacetylene (PA), over 50 years ago Lennard Jones performed research into the π electron structure of polyacetylene [11], however the initial films were very reactive, decomposed in air and could not be melted or processed [10]. During the 70's more controlled methods of production were used and these were developed to allow further study in the 80's [12,13]. The chemical structure shows two σ bonds and one π bond attached to each carbon atom in the chain. Two electrons, one from each atom per bond, are involved in all these bonds. The Pauli Exclusion Principle states that only one electron can occupy a single state at any time, however it is possible for two electrons to occupy a single energy level if they have different spins. The sigma band of energy is full when there are two σ bonds on each atom. The maximum number of electrons contributing to each pi bond attached to the atom is two, this means that the pi energy band is only half full, although pi bonds are more energetic and are as a consequence in a higher position on the energy band diagram. Classical conductor-semiconductor-insulator theory states that this material should be metal, this theory agrees with the physical experimental evidence [14,15]. Peierls, suggested that a one-dimensional lattice would become unstable at the Fermi level, this would result in lattice distortion and lead to the creation of an energy gap by the separation of the anti-bonding states and the bonding states [16].

The bonding state is situated at a lower energy and is fully occupied. The Highest Occupied Molecular Orbital (HOMO), is the highest energy level in this band and forms the edge of the organic equivalent of the valence band. The Least Unoccupied Molecular Orbital (LUMO) is the lowest energy level in this band and forms the edge of the organic equivalent of the conduction band.

The band structure of inorganic crystalline structure is derived from the periodicity of the crystal, if this analysis is used with one-dimensional polymer, a period occurs

after every single bond step. There is therefore a period at twice the distance between atoms of the polymer. This means that the energy band will be split into two, which creates the 'bonding' energy and the 'anti-bonding' energy band. The above ideas mean that, the material will be a semiconductor as long as the forbidden energy gap is small (<2 eV).

The model also predicts that a defect will be created at the point where an electron is removed from the chain, this is most likely in the p_z orbital and makes the material p-type. The conjugation at this point would be broken, and would move energy states from the HOMO and the LUMO into the energy gap. A soliton, is the name given to an energy state which is formed at the centre of the bandgap. A soliton can be neutral (one electron occupying the level), positively charged (no electrons occupying the level) or negatively charged (where two electrons of different spins) occupy the level [17].

A conduction electron (or hole) together with its self-induced polarisation in a polar semiconductor or an ionic crystal forms a quasi-particle, which is called a polaron. Polarons in effect arise from an electron (or hole) trapped in a phonon cloud.

Polarons are another possible excitation in degenerate ground state polymers and have been observed in amorphous silicon [18]. Polarons are a quasi particle unit compromising the self–trapped carrier and the associated atomic displacement pattern.

The associated displacement is caused by the trapped-carrier (for example an electron) moving through constituent atoms in a solid with the electron causing neighbouring positive charges to shift toward it and neighbouring negative charges to shift away.

Polarons can be considered to be a bound soliton-antisoliton pair (one charged and one neutral). This will result in the polaron having a pair of energy levels in the band gap. Heeger predicted that polarons in degenerate ground state polymers are stable [17]. Doubly charged polarons known as bipolarons are not formed in this ground state. The energy of the system is lowered sufficiently by the addition of a second electron to break the resultant polaron. Bipolarons are therefore unstable in degenerative ground state polymers [17].

2.3 Non-Degenerative Ground State Conjugated Polymers

It is important that polymers are stable in air and do not decompose. In polymers with non-degenerative ground states, bipolarons are stable but polarons remain a possible excitation state, it is felt that bipolarons may have a role in charge transport in conjugated polymers with a non-degenerate ground state, particularly polythiophene [19].

One problem with polymers with non-degenerative ground states, is that they may lack the ability to be melted, or dissolved in solvent. This problem can be overcome by the addition of side chains to the rings. It makes the polymer soluble in organic solvents and allows preparation of films by spin-coating or casting. Polythiophene is an example of a non-degenerative ground state polymer, its chemical structure is shown in *figure 2.3.1*.

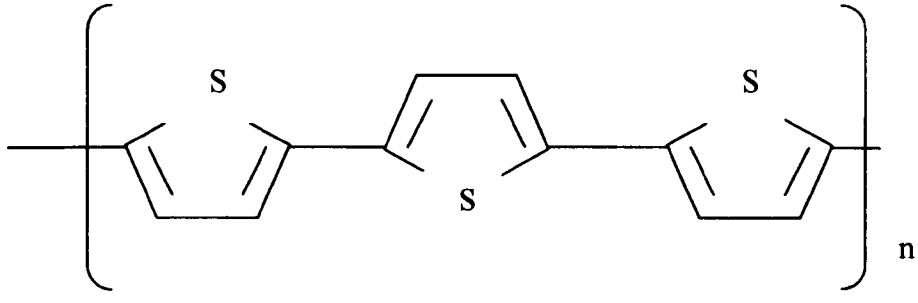

Figure 2.3.1: Chemical structure diagram for PT.

Traditional organic semiconductors have a conjugated backbone which means that electrons are able to move along the molecule. Plastic Electronics require organic semiconductors that have high carrier mobility, low intrinsic conductivity, good stability and low cost fabrication. The carrier mobility of organic semiconductors is associated with the ease in which they can move through material, although this is less of a fundamental quality that it is in silicon. It is much lower than that found in silicon. One of the reasons for this is that they are in general very disordered. Recent developments have made use of p-type materials such as poly(3-hexylthiophene) (P3HT) which has the potential to fill the gap left by silicon in regards to the fabrication of low cost and flexible electronic circuits. [20]

P3HT is produced by the addition of a hexyl side chain to polythiophene. The length of the side chains can be altered and this affects the electrical properties of polymer [21]. P3HT has been found to have a low band gap, (2.14 eV) [22], good solubility,

thermal and environmental stability [23] and an improved mobility [24] compared with its predecessors. These are promising characteristics for a polymer. *Figure 2.3.2* shows a diagram for the chemical structure of P3HT.

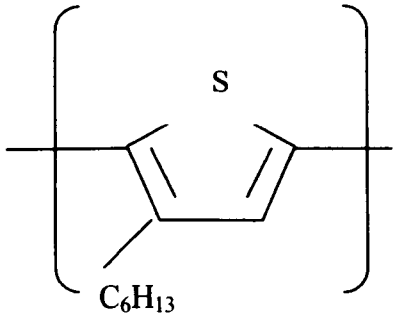

Figure 2.3.2: Chemical structure diagram for P3HT.

2.4 Polytriarylamines (PTAA)

Organic semiconductors with high mobility are hard to process in solution or have poor air stability. Work carried out by Avecia (now Merck) has led to the production of a new class of solutions polytriarylamines (PTAA). [25] PTAA is felt to be interesting because the materials have improved stability in air and field-effect transistor devices remain stable and operate with mobility values above 10^{-3} $cm^2V^{-1}s^1$. [26]

The general chemical structure for PTAA is shown in *figure 2.4.1*. They are versatile, as varying the substituent's X and Y and end caps Z, changes the mobility, ionisation potential, glass transition temperature, film forming properties, morphology and substrate interactions. [20]

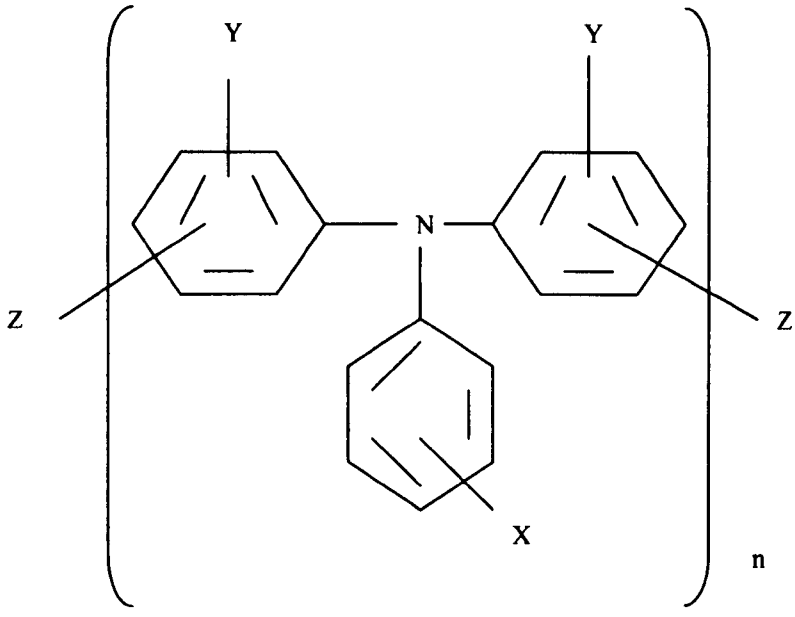

Figure 2.4.1: General formula of triaylamine polymers.

2.5 Disordered Materials: An Analytical Treatment

Ordered materials tend to be crystalline, these are materials which have a regular crystal form and have symmetry of properties such as energy gap and conductivity [27]. It has been suggested that ordered films could promote and enhance the performance of a huge number of electronic devices, where conducting polymer is the active material [28]. One draw back of ordered material is the expensive manufacturing costs.

Disordered materials occur when molecules or atoms can be anywhere. A traditional example of this is amorphous silicon, although by some this is now regarded as being relatively ordered. Most polymers are more disordered than amorphous silicon, although some polymers are polycrystalline, which means that there are clusters of crystalline material, but their boundaries are not crystalline, an example of a polycrystalline material is pentacene. Pentacene has been demonstrated to have one of the highest carrier mobilities based on thin film transistors [29].

The majority of polymers are regarded as being amorphous; examples of amorphous materials include Poly-3-hexylthiophene (P3HT) and Polytriarylamine (PTAA).

While conduction and valence bands can be defined for crystalline materials, it is not possible to define these bands for an amorphous material this is because all the electrons are localised and are unable to reach energy levels where they can be regarded as being free. One result of electrons being localised, is that hopping is the

most dominant conduction mechanism in both polycrystalline and amorphous materials [30].

The probability that an electronic state with energy, E, is occupied by an electron is given by the Fermi-Dirac function:

$$f(E) = \frac{1}{1+\exp\left(\frac{E-E_F}{kT}\right)} \qquad 2.5.1$$

The diagram in *figure 2.5.1* illustrates the Fermi-Dirac function.

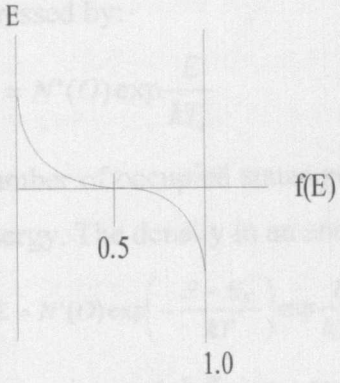

Figure 2.5.1: The variation in the fraction of states occupied with increase in energy.

In the conduction band there are a large number of allowed states but (in the intrinsic semiconductor) there will only be a few electrons in the conduction band and hence the probability of an electron occupying one state is small.

The valence band has a large number of allowed states but most of these are occupied by an electron. The probability of an electron occupying one of the states in the valence band is therefore nearly unity.

The Fermi level is the energy at which the probability of occupation by an electron is exactly one half.

In conventional semiconductor devices, carriers from dopant states, occupy the conduction band states which have a relatively high density. In organic semiconductors, it is also assumed that carriers will occupy states further away from the Fermi level, rather than levels closer to it. Integrating from the Fermi level therefore gives a good approximation, when the difference between E and E_F is more than the value of a few kT. Therefore, if $E >> E_F$ *equation 2.5.1* can be approximated to be:

$$f(E) = \exp\left(-\frac{E - E_F}{kT}\right) \qquad 2.5.2$$

The density of states at energy E, can be represented by an exponential function. There are a number of possible reasons for this distribution. Probably the most favoured is the existence of a Gaussian Distribution of states. The tail of such a distribution is an exponential function. It is defined by kT_C which is a constant for almost all disordered semiconductors. T_C is not a real temperature, rather it is an algebraic convenience. If the N'(E) we have is the rate of increase in the density of such states and N'(0) is its value for the arbitrarily chosen zero for energy, N'(E) can be expressed by:

$$N'(E) = N'(O)\exp\frac{E}{kT_c} \qquad 2.5.3$$

The number of occupied states per unit energy is equal to the number of carriers per unit energy. The density in an energy range dE is :

$$n'(E)dE = N'(O)\exp\left(-\frac{E - E_F}{kT}\right)\exp\frac{E}{kT_c}dE \qquad 2.5.4$$

On rearranging and defining a term T_0 by

$$\frac{1}{T_o} = \frac{1}{T} - \frac{1}{T_c} \qquad 2.5.5$$

where T_0 is the quantity defining an exponential distribution of carriers. Therefore *equation 2.5.4* can be simplified to:

$$n'(E)dE = N'(O)\exp\frac{E_F}{kT}\exp\frac{-E}{kT_o}dE \qquad 2.5.6$$

The carrier concentration below the Fermi level is negligible and can therefore be neglected. The total carrier concentration with all energies taken into account, can therefore be found by integrating between E_F and infinity:

$$\int_{E_F}^{\infty} n'(E)dE = N'(0)\exp\frac{E_F}{kT}\int_{E_F}^{\infty}\exp\frac{-E}{kT_o}dE \qquad 2.5.7$$

Integrating gives:

$$n = N'(0)kT_o\exp\frac{E_F}{kT}\exp\frac{-E_F}{kT_o} \qquad 2.5.8$$

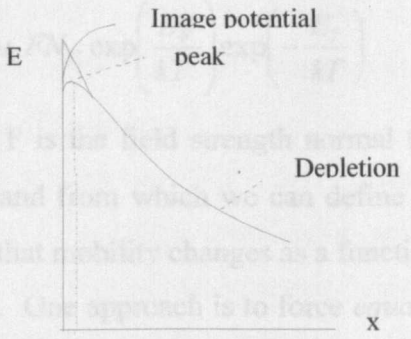

Figure 2.5.2: The formation of a potential barrier due to the added image and depletion potentials.

We now consider the application of this relationship to a simple metal semiconductor contact. A Schottky barrier is illustrated in *figure 2.5.2*, it is formed because of the differences in the work function between the metal and semiconductor. The barrier to electrons leaving the material causes its peak to be inside the semiconductor surface. This is a result of the image force of an electron leaving the metal. The peak of the barrier is when this image field is equal and opposite to the field due to the depletion region.

The carriers below E_B (the peak) are trapped in localised states, therefore only the carrier concentration above E_B need to included:

$$\int_{E_B}^{\infty} n'(E)dE = N'(O)\exp\left(\frac{E_F}{kT}\right)\int_{E_B}^{\infty}\exp - E\left(\frac{1}{kT}-\frac{1}{kT_c}\right) \qquad 2.5.9$$

Therefore the total carrier concentration can be given by:

$$n = N'(O)kT_o N'(O)kT_o \exp\frac{E_F}{kT}\exp\frac{-E_B}{kT_o} \qquad 2.5.10$$

This enables the current voltage characteristic of the barrier to be modelled if we know the variation of E_B with the forward applied voltage.

Suppose we integrate across the total distribution of traps so that the limits are $E=\infty$ to E_F the resulting relationship for n the total electron density is

$$n = N'(O)kT_o \exp\frac{E_F}{kT_C} \qquad 2.5.11$$

which is quite different for the relationship for carriers at a single transport level such as a conduction band edge E_C.

$$n = N_C \exp\left(\frac{E_F}{kT}\right)\exp\left(-\frac{E_C}{kT}\right) \qquad 2.5.12$$

and assuming ohmic contacts we have for a transport level E_T

$$J = q\mu_0 F N_C \exp\left(\frac{E_F}{kT}\right)\exp\left(-\frac{E_T}{kT}\right) \qquad 2.5.13$$

where F is the field strength normal to the interface, N_C is the effective density of states and from which we can define a mobility μ_0. The Universal Mobility Law states that mobility changes as a function of carrier density, this is therefore an unlike model. One approach is to force *equation 2.5.12* to look like *equation 2.5.11* and to do this within *equation 2.5.13* so the extra terms needed to maintain the validity of *equation 2.5.12* can be included in a term we will call the effective mobility μ_{eff}. This must then be the quantity that we measure with TFT or diode characteristics.

$$J = FqN_C \exp\left(-\frac{E_T}{kT}\right)\mu_0\left[\exp\left(\frac{E_F}{kT_C}\right)\right]^{\frac{T_C}{T}-1}\exp\left(\frac{E_F}{kT_C}\right) \qquad 2.5.14$$

or

$$\mu_{eff} = \mu_0\left[\exp\left(\frac{E_F}{kT_C}\right)\right]^{\frac{T_C}{T}-1} \qquad 2.5.15$$

and from *equation 2.5.11*

$$\mu_{eff} = \mu_0\left(\frac{n}{N'(0)kT_0}\right)^{\frac{T_C}{T}-1} \qquad 2.5.16$$

We have therefore a dependence of mobility on the total integrated carrier density. We will find later that we can obtain the value of T_c from the exponential characteristic of a diode. For the saturation region of the forward characteristics the carrier density must be changed by adding a dopant to the solution prior to depositing the film (T_c=900K). The exponential characteristics of a diode give approximately T_c=450K. In the case of P3HT there is a point on the curve that corresponds to a nominally undoped film. This we attribute to residual doping of about $10^{16}cm^{-3}$. The higher value of T_c is associated with dopant levels, there is no obvious reason why T_c should be double. It is important to note that nowhere have we assumed variable range hopping. The Universal Mobility Law comes from the assumption of classical device physics to an exponential distribution of states.

2.6 Dopants

Doping in conjugated polymers is fundamentally different from doping with an inorganic semiconductor, such as silicon [31]. Polymers are doped by several

percent, while doping in inorganic semiconductors involves parts per million [32]. However only a small fraction of the added dopant is ionised and therefore electrically active.

Polymers such as P3HT are fractionated to increase the regioregularity of the polymer to ~ 100%. Purification removes the molecules that have irregular bond angles. So it leads to better ordering of the chains. After fractionation, the films remain p-type, as they remain in air. However it has been proposed that dopant contributes to the higher mobility of the 'as-synthesised' material by acting as 'stepping stones' for carriers to move from one polymer chain to another [33,34]. To replicate the beneficial effects of acceptor-like impurities in a controlled way, polymer can be doped with another compound such as 2,3-dichloro-5,6-dicyano-1,4-benzoquinone (DDQ).

Because of the Pauli Exclusion Principle the extra carriers are distributed into higher carrier energies and, therefore, can more readily hop to adjacent states. There is therefore an increase in mobility.

2.7 2,3-dichloro-5,6-dicyano-1,4-benzoquinone (DDQ)

DDQ has been used as an electron acceptor to dope a number of different polymers for example polyaniline (PANI) and poly(4,4-dioctylcyclopentadithiophene) (p-type) [35,36].

Doping polymers, such as P3HT with DDQ has been found to significantly increase the bulk mobility as well as the field effect mobility [37], similar results have been found when PTAA is doped with DDQ [38].

The chemical structure of the compound, DDQ, is shown in *figure 2.7.1.*

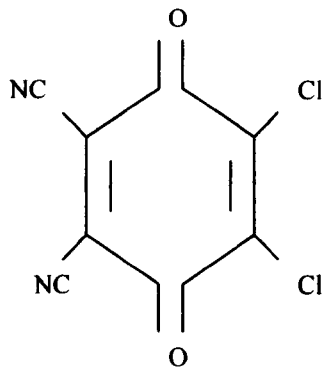

Figure 2.7.1: The chemical structure of DDQ.

2.8 Summary

The majority of polymers are amorphous which means that variable range hopping is the most dominant conduction mechanism. In the past 50 years the stability of polymers, in air, has improved. Polymer is starting to provide a means of producing low cost and flexible electronic circuits. The Universal Mobility Law is to be a result of applying classical device physics to an exponential distribution of states. Doping polymers with dopants such as DDQ increases the mobility by increasing the number of carriers in higher energy levels.

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Chapter 3

Thin Film Transistor: Fabrication and Theory

Thin Film Transistors (TFT)s were first investigated in the 1930's; they are important as they are used in many device applications. In this chapter the effect of the fabrication process on TFT characteristics are discussed, as well as the ideal and experimental characteristics of TFTs.

3.1 Introduction

In addition to the potential applications stated in the previous chapter for conjugated polymer devices, applications include photovoltaic cells (low cost solar panel), optical amplifiers, memory, displays (in conjunction with e-paper and large area LCDs) and radio frequency identification tags (RFID). Many of these devices will use Thin Film Transistors (TFT)s and OLEDs.

A polymer TFT is made of non-single crystal semiconductor film deposited on an insulating substrate [1]. TFTs were first investigated in the early 1930's, the first device patents described controlling the sheet resistance of a semiconductor using an electric field [2,3]. However TFT operations are very similar to Metal Oxide Semiconductor (MOS) transistors [4,5]. This led to TFTs and Metal Oxide Semiconductor Field Effect Transistors (MOSFET)s competing against each other for a share of the market place. Weimer performed most of the original work investigating TFTs in the 1960's [6,7,8], but as the development of the MOSFET increased and potential applications for TFT development moved across to better technology, the interest in TFTs died away. However when in the 1980's, large area integrated electronics for example flat panel displays became desirable, there was a renewed interest into TFTs. Materials used to fabricate TFTs for displays at the moment are either amorphous [9] or polycrystalline silicon [10]. The field of organic semiconductors has experienced rapid development during the last decade leading to recent reports on the feasibility of higher performance integrated circuits fully made of organic components [11,12,13]. The structure typically involves a deposited or grown dielectric to form the gate of the device. It is however difficult to compare these devices with normal crystalline MOSFETs because of the quality of the material used [14]. The wide bandgap of amorphous silicon reduces the leakage current, which leads to an increase in the ratio of the on-off current, but both types of devices have low mobilities [9]. The two materials currently used are polycrystalline silicon and amorphous silicon, the disadvantage with both these materials is that they are costly and deposition is carried out at temperatures demanding high quality expensive glass. An alternative semiconductor that can be deposited cheaply and easily is therefore in demand. Conjugated polymers can be deposited relatively easily onto most substrates. The fabrication of electrodes on a grown oxide layer forms the basis of some TFTs, with the polymer being deposited on top. This ease

of deposition opens up many possibilities for solution-processed semiconductors including the application of TFT's [14].

3.2 Conjugated Polymer Thin Film Transistors (TFT)s

A large proportion of polymer TFTs operate in the accumulation mode. This is as a result of the extreme difficulty of separating excitons that are created when under the influence of gate field and trapping of the minority carrier at deep levels at the interface.

Conjugated polymer TFTs have traditionally been fabricated on silicon dioxide, however there is an increasing move to use flexible substrates which are more appropriate to a low cost market. The structure of a TFT is shown in *figure 3.2.1.* The performance of polymer TFTs on flexible substrates (e.g. plastic substrates) has increased as a result of the demand for paper-like plastic electronic products. This is because solution-processable fabrication methods such as screen and inkjet printing could, in principle be used [15], if small feature sizes were possible. It would also allow the use of roll-to-roll fabrication methods.

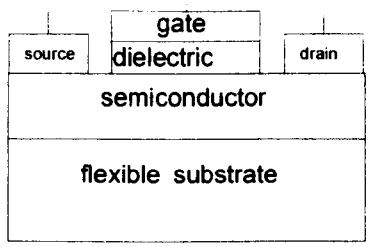

Figure 3.2.1: The simple top gate thin film transistor.

To enable polymer TFT devices to be used in applications such as active matrix flat panel displays, they need to have a sufficiently high carrier mobility and low off-current. [16]

F. Garnier and his collaborators at CNRS, first demonstrated devices with significant mobilities, on/off ratios and saturation using oligomeric thiophenes [17]. There has also been a large amount of interest in pentacene and poly(3-alkylthiophene) [18, 19,20]. Then in 1996 high field mobilities were found using regioregular P3HT [21]. Regioregular P3HT has been found to show field mobilities of (0.01 – 0.1 cm^2/Vs) and reasonable on/off ratios (>100 in air and 10^6 in an inert gas). [22,23]

Treatment with oxygen plasma after electrode fabrication, has been shown to enhance the electrical characteristics: saturation carrier mobilities of 0.02-0.025 cm^2/V s and an on-off ratio of approximately 10^4 have been seen, for TFT's devices on plastic substrates [26]. However, there is degradation in the devices performance by prolonged treatment which appears to be a consequence of plasma damage to the substrate and electrodes. [16]

Recently the development of PTAA, has led to the production of field-effect transistor devices which remain stable and operate with mobilities above 10^{-3} $cm^2V^{-1}s^{-1}$ [25].

3.3 A Fabrication Method for Thin Film Transistors

Stage 1

An oxide is grown on the top surface of the aluminium substrate this forms the gate dielectric.

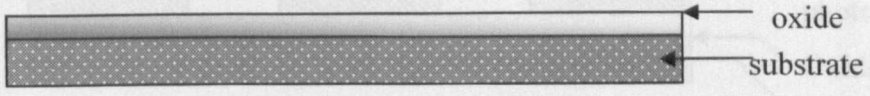

Figure 3.3.1: Stage 1 of fabrication process.

For an aluminium substrate the oxide is grown by anodisation. A platinum anode is used and a citric acid solution, which has had nitrogen bubbling through it. Prior to anodisation; the aluminium is heated at 100°C in the presence of nitrogen. During the anodisation approximately 35V is put across the cathode (the aluminium) and the anode. After the anodisation has been completed, the aluminium oxide is heated at 100°C in the presence of nitrogen for two hours.

Stage 2

Positive photoresist is spun onto the surface and soft-baked in an oven.

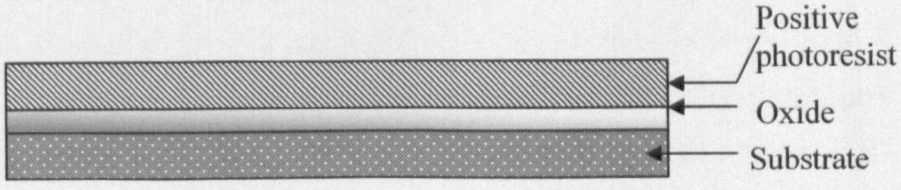

Figure 3.3.2: Stage 2 of fabrication process.

Stage 3

Exposure of the photoresist through dark-field photolithography masks constructed from chromium and quartz defines the area of resist to be removed. Development of the pattern produces windows in the photoresist.

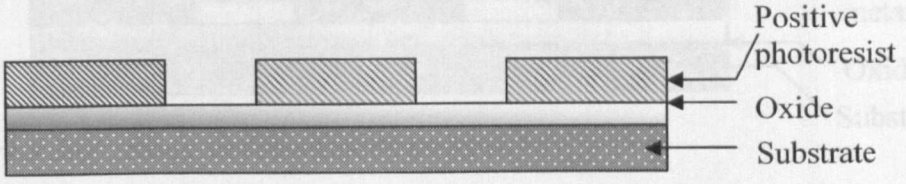

Figure 3.3.3: Stage 3 of fabrication process.

Stage 4

Evaporation of the source/drain contact metal on top of the photoresist produces predefined areas where the metal is in contact with the oxide.

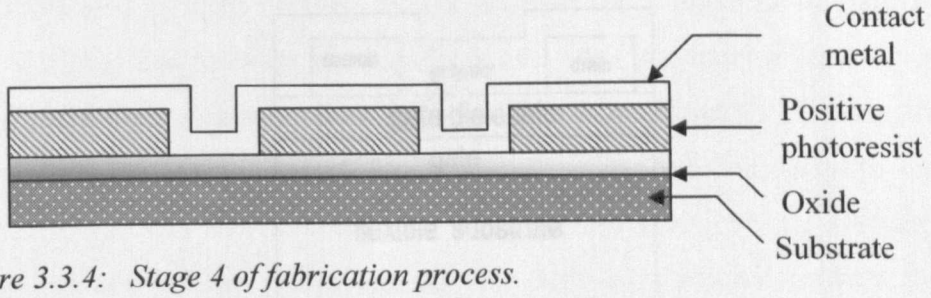

Figure 3.3.4: Stage 4 of fabrication process.

Stage 5

Removal of the photoresist leaves patterned metal electrodes on the surface of the oxide.

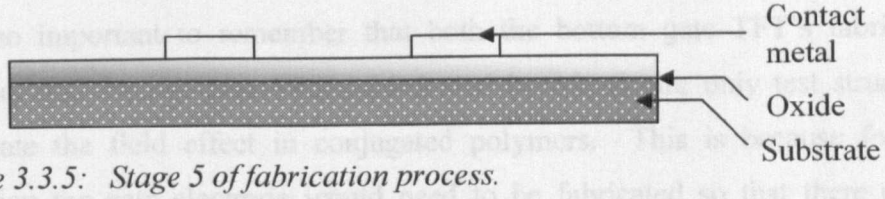

Figure 3.3.5: Stage 5 of fabrication process.

Stage 6

The polymer is then cast or spun onto the contact metal.

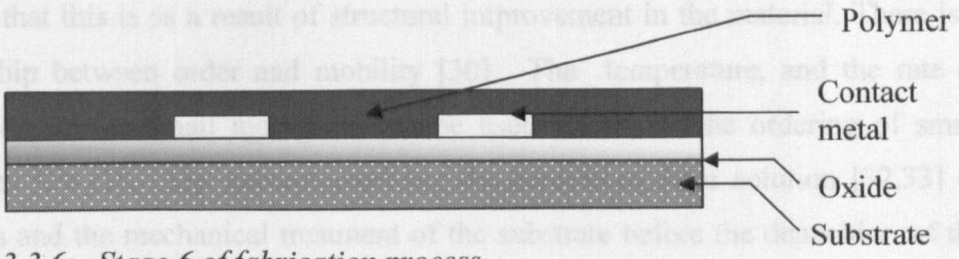

Figure 3.3.6: Stage 6 of fabrication process.

Figure 3.3.7, shows the final structure of the devices that have been constructed at Liverpool. It should be remembered that some of the devices in this report have been fabricated by Merck and are therefore top-gate structures.

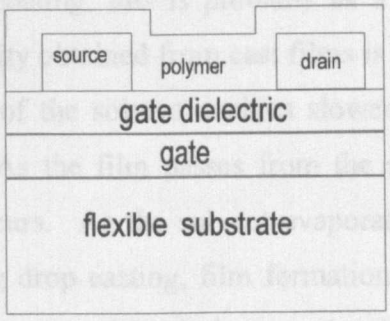

Figure 3.3.7: The bottom gate thin film transistor suitable for testing electrical properties. There is no electrical isolation of the transistor and no process for producing cross-overs.

It is also important to remember that both the bottom gate TFT's fabricated at Liverpool and the top gate TFT's fabricated by Merck are only test structures to investigate the field effect in conjugated polymers. This is because for device integration the gate electrode would need to be fabricated so that there could be multiple devices on the same substrate. This would lead to the introduction of more fabrication steps to deposit and pattern the contact material and to deposit the gate dielectric. Design alterations would be needed to avoid overlap capacitance between gate and source and the gate and drain which would decrease the speed of operation. Interconnect lines may have to cross and individual transistors often have to be isolated.

3.4 TFTs and the Effect of the Fabrication Process

There has been a large improvement in mobilities over the past ten years [24,26-29]. It is felt that this is as a result of structural improvement in the material. There is a relationship between order and mobility [30]. The temperature, and the rate of vacuum-deposition small molecules can be used to control the ordering of small molecules [29-31]. The solvent used for the deposition from solution [32,33] of polymers and the mechanical treatment of the substrate before the deposition of the organic semiconductor, can also be used to control the ordering.

A thin film of P3HT can be deposited using a variety of methods, including spin casting [18,27], drop casting [22,34], printing [35], Langmuir-Blodgett deposition [36] and by dip coating [28].

The off-current of devices, which are prepared by casting are usually higher than those, fabricated by spin coating, this is probably as a result of cast films being thicker [22,28]. The mobility obtained from cast films is usually higher, this may be because slow evaporation of the solvent enables slower growth of films and thus allows ordering [22,37]. As the film passes from the solution phase to the solid phase self-organisation occurs. As the solvent evaporates from the surface of the polymer solution following drop casting, film formation proceeds inward from the outer rapidly drying shell, thus resulting in improved order. Thicker drop-cast films exhibit a higher degree of structural order in the FET channel since molecules can self-organise over a longer time at the inner core of the drying solution [28].

If films are spin-cast, the rapid drying and the radial velocity of the polymer solution during drying prevents self-organisation [28].

Different groups have reported a range of mobilities for the dip coating process, one group has reported very high mobilities [28] and other groups have reported lower values [28,38,39].

Dip coating the regioregular P3HT leads to improved structural order and high hole mobilities [28]. However it has also been reported that the carrier mobilities for dip coating a single layer are typically nearly 2 orders of magnitude lower than the carrier mobility's in an FET prepared by spin coating [38].

There has been some debate to whether top or bottom gate devices are preferable. Polymer films crystallise from the top and therefore this region is felt to have the highest mobilities, therefore traditionally the gate needs to be on top of the film, to

provide the high mobilities. However, crossovers are easier to produce if a bottom gate configuration is used.

3.5 The Ideal TFT Characteristics

Figure 3.5.1 shows the ideal TFT transfer characteristics [14].

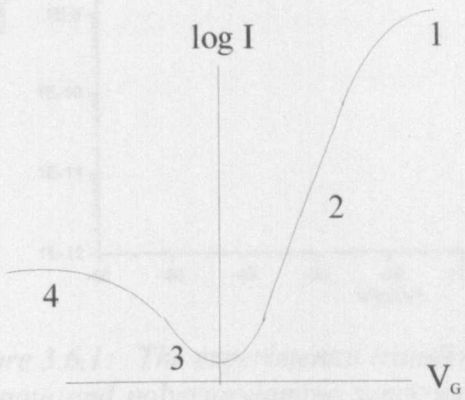

Figure 3.5.1: The ideal transfer characteristic of a thin film transistor made on n type material.

The region 1 is the high current region of operation for a transistor produced on highly disordered material. Here there is a channel fully formed: the potential drop down the channel reduces the field in the gate dielectric. The current is determined by drift. This is also the case with region 2, but there is little drop in the potential down the channel because the current is low. At 3 the dominant carrier are holes. This requires holes to be generated by electrons leaving the semiconductor and entering the drain and the hole flows back in the opposite direction. The rate of supply of such holes is limited by generation rates and exciton formation and fortunately it saturates, at 4.

Polycrystalline material behaves in a similar way except that the exponential rise in current for positive gate voltage may be governed by diffusion.

3.6 Experimental TFT Transfer Characteristics

Thin-film transistors produce characteristics such as those shown in *figure 3.6.1.*

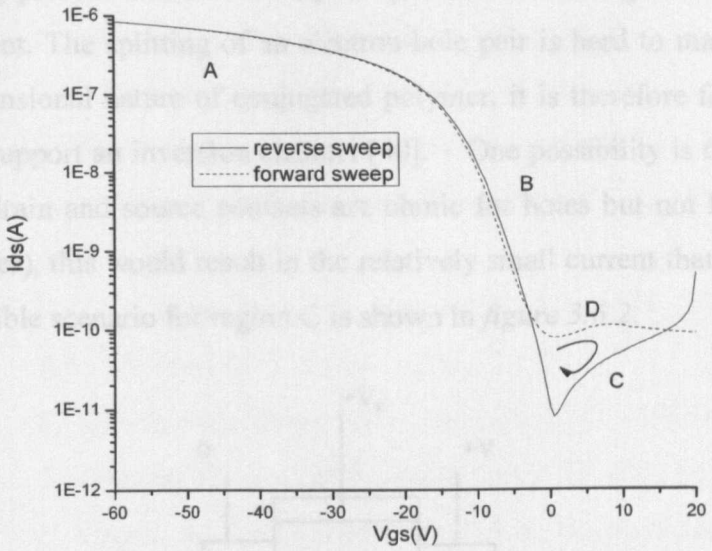

Figure 3.6.1: The experimental transfer characteristic of a p channel TFT with a top gate and polytriarylamine semiconductor, where L=130μm, W=29.7mm and τ_{ox}=1μm. There is minimal hysteresis in the high current drift region.

The characteristic is swept from positive to negative gate voltage. The high current regime shows anti-clockwise hysteresis. Because this is a logarithmic plot the change of current levels after a prolonged negative bias is relatively high but good compared with most materials. This is associated with either ion movement in the organic material or perhaps the slow trapping of carriers across the interface between the dielectric and the semiconductor. In contrast in the low current region there is clockwise hysteresis and this is conventionally associated with ion movement in the dielectric. Note the dip (C) in the current is evidence of an imperfect source contact. It should be noted that when the source and drain approximate to Schottky barriers the source is reverse biased and the drain is forward biased. The form of the curve after the transistor has been turned hard-on may be due to the drift of ions into the depletion region shorting the reversed junction at the source.

If a positive gate field is applied the polymer will be depleted of holes. While if a positive gate field was applied to an inorganic semiconductor the surface of the semiconductor would be inverted and a channel region composed of a negative charge would be formed. Note that inversion in the case of a polymer is different than with ordered silicon. Fermi-level pinning in the former leads to a reduction in the effective carrier mobility. Trapping in the case of disordered material means that

there is a high density of states through which carriers can easily hop so that the field effect mobility is increased. In opposition to this is the probability of both carriers being present and the consequent problem of freeing the holes to produce channel current. The splitting of an electron-hole pair is hard to maintain, because of the 1-dimensional nature of conjugated polymer, it is therefore felt that the material may not support an inversion channel [40]. One possibility is that there is inversion but the drain and source contacts are ohmic for holes but not for electrons (a Schottky barrier), this would result in the relatively small current that is seen. A diagram of a possible scenario for region C is shown in *figure 3.6.2.*

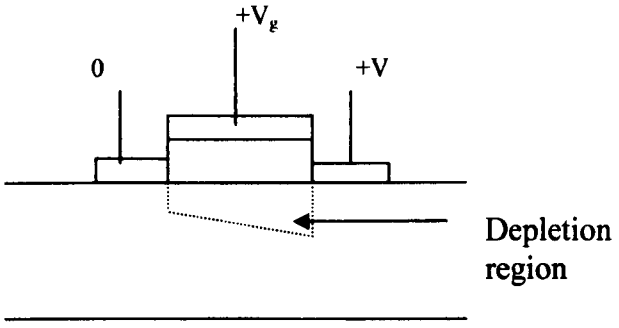

Figure 3.6.2: An illustration of a TFT in region C

3.7 Summary

TFTs were first investigated in the 1930's but were side tracked as MOSFET was developed, in the 1980's the interest in TFTs remerged. Many applications of conjugated polymers use TFTs. Conjugated polymer TFT's were originally fabricated on silicon dioxide, however fabrication is now increasingly moving towards the low cost market offered by flexible substrates. The mobility of TFTs has increased with structural improvements over the past 10 years and plasma treatment of the substrate has been found to further enhance electrical characteristics as has the use of adhesion promoters between the gate dielectric and semiconductor which have improved effective mobility. The role of defects has become clearer over this period of time.

The fabrication of TFT's has been described in the chapter and the effect of fabrication processes on characteristics have been discussed.

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Chapter 4

The Gradual Channel Equations for Thin Film Transistors

The characteristics of TFTs have been discussed in a previous chapter. In this chapter the drain current is derived using five different sets of approximations. This is important to determine the effect of treating the real variation in the carrier concentration normal to the surface. In addition how this large variation in carrier density gives rise to an enhancement of carrier mobility at the interface is examined.

4.1 Introduction

Figure 4.1.1 shows a cross-section of an organic thin film transistor (TFT). Applying a positive voltage draws electrons from the channel; these electrons are replaced from the source. The source and drain contacts are both ideally ohmic, this means that they can pass charge to and receive charge from the body of the transistor. Changing the 'gate' voltage V_g controls the flow of the continuous channel current. The polymer surface is accumulated so that when the body is slightly p type the surface has a higher concentration of holes.

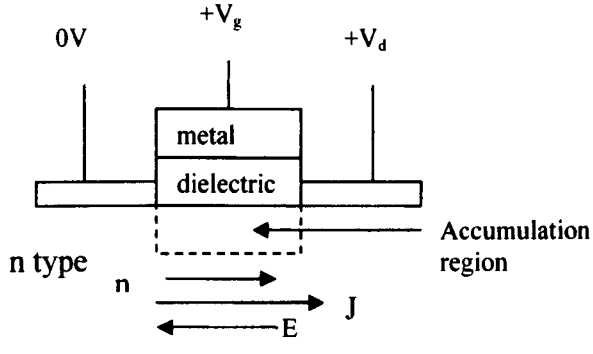

Figure 4.1.1: Cross section of an n channel TFT.

A number of different current-voltage equations are derived here for the drain current in the channel. They are each based on different approximations and must be described and compared in this chapter. It is important to develop these equations to determine the effect of treating the real variation in the concentration of carriers, normal to the interface. In addition we then look at how this large variation in the density of carriers gives rise to an enhancement of carrier mobility as the interface is approached.

The first equation is the delta function. It assumes that all carriers are at the same energy and have the same average velocity. The second equation is the simple classical equation. It assumes that in steady state there will be matching drift and diffusion current densities in planes parallel to the interface. The third equation also takes account of the exponential distribution of states.

However these first three equations do not take into account that as energy levels fill, electrons will have higher mobility. Therefore the higher the overall concentration of electrons is, the higher the mobility will be, this leads to the universal mobility law. The fourth equation, therefore, also includes the universal mobility law. The final equation is for the delta function with the universal mobility law.

4.2 The Delta Function Equation

The first equation assumes that the concentration of electrons is constant in the channel and falls to zero at some well defined distance from the interface.

The geometric capacitance of the oxide is:

$$Q_o = -C_o(V_g - V_x) \qquad 4.2.1$$

where Q_o is the charge per unit area of the oxide, C_o is the oxide capacitance per unit area, V_g is the gate voltage and V_x is the voltage in the polymer, at the edge of the depletion region. There is a negative sign because if a positive gate voltage is applied, negative ions would be induced in the polymer.

Current density can be expressed by:

$$J = qn\mu F \qquad 4.2.2$$

Multiplying the charge of a single electron by the concentration of electrons can be equated to the total charge per unit area across the thickness of the polymer. Therefore using an alternative expression for charge density and Q=CV current density can also be expressed by:

$$J = -\frac{C_o}{dz}(V_g - V_x)\mu F \qquad 4.2.3$$

F is the field at position x, which can also be expressed as dV_x/dx, therefore current can be expressed as:

$$I_D = \mu C_o W(V_g - V_x)\frac{dV_x}{dx} \qquad 4.2.4$$

Separating variables and integrating for x = 0 to x = L and V = 0 to $V_x = V_d$ gives:

$$I_D = \mu C_o \frac{W}{L}\left(V_g V_d - \frac{V_d^2}{2}\right) \qquad 4.2.5$$

Because of the effect of charge in the oxide and work function effects, a threshold gate voltage, V_t, is introduced:

$$I_D = \mu C_o \frac{W}{L}\left((V_g - V_t)V_d - \frac{V_d^2}{2}\right) \qquad 4.2.6$$

4.3 The Classical Equation

In the second case we develop a new treatment based on materials with a single transport energy. The treatment is then similar to that for a single crystal

semiconductor. The transport energy is then E_C. The intrinsic carrier concentration can be expressed by:

$$n_i = N_c \exp-\left(\frac{E_c - E_i}{kT}\right) \qquad 4.3.1$$

where n_i is the intrinsic electron concentration, N_c is the effective density of states at a conduction band edge and E_i is the intrinsic Fermi energy.

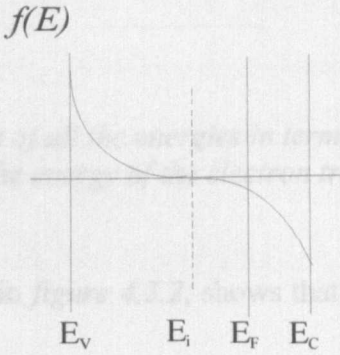

Figure 4.3.1: The single crystal picture showing the band edges and the positions of the intrinsic and extrinsic Fermi level.

The equilibrium concentration of electrons in extrinsic material can be expressed as:

$$n_o = N_c \exp-\left(\frac{E_c - E_F}{kT}\right) \qquad 4.3.2$$

where n_o is the equilibrium concentration of electrons and E_F is the extrinsic Fermi level.

The diagram in *figure 4.3.1* shows how the fraction of states occupied changes with the position in the gap of the Fermi level. They accumulate at E_c and E_v but it is impossible for electrons to accumulate between these energy levels. Electrons accumulate above the conduction band edge as shown by the figure. If holes were to accumulate they would accumulate below the valence band edge.

The ratio of the intrinsic electron concentration to the equilibrium concentration of electrons, can be found by taking the ratio of *equation 4.3.1* and *equation 4.3.2*:

$$n_o = n_i \exp\left(\frac{E_F - E_i}{kT}\right) \qquad 4.3.3$$

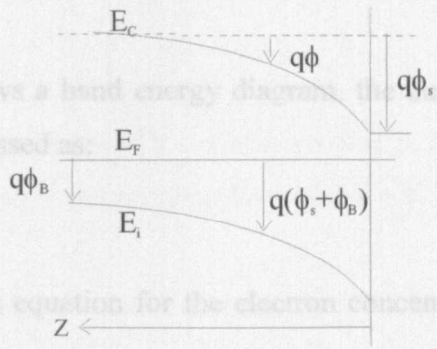

Figure 4.3.2: Definition of all the energies in terms the various potentials defining Fermi levels and the energy of the electron transport levels.

The band energy diagram in *figure 4.3.2*, shows that *equation 4.3.3*, can be adapted to give:

$$n_o = n_i \exp\left(\frac{q\phi_B}{kT}\right) \qquad 4.3.4$$

The equilibrium concentration of holes can be expressed by:

$$p_o = n_i \exp\left(-\frac{q\phi_B}{kT}\right) \qquad 4.3.5$$

Equations 4.3.4 and 4.3.5 can be combined to show that:

$$n_o p_o = n_i^2 \qquad 4.3.6$$

which is essentially a check on the validity of the equations.

The diagram in *figure 4.3.2*, shows an energy diagram, when a gate voltage is applied across a polymer and semiconductor.

As shown by the diagram in *figure 4.3.2.* The electron concentration can be shown to be:

$$n = n_i \exp\left(\frac{q\phi_B + q\phi}{kT}\right) \qquad 4.3.7$$

$$n = n_o \exp\left(\frac{q\phi}{kT}\right) \qquad 4.3.8$$

Equation 4.3.6 can be adapted, so that:

$$np = n_i^2 \qquad 4.3.9$$

where p is the hole concentration, combining *equations 4.3.8 and 4.3.9*, gives the hole concentration:

$$p = p_o \exp\left(-\frac{q\phi}{kT}\right) \qquad 4.3.10$$

Figure 4.3.2, shows a band energy diagram, the current density at a distance z can therefore be expressed as:

$$J = qn(z)\mu\frac{dV_x}{dx} \qquad 4.3.11$$

By substituting an equation for the electron concentration into *equation 4.3.11* and given $dz = {}^{d\phi}/_{F_z}$, the following expression can be derived:

$$Jdz = \frac{dI}{W} = qn_0\mu\exp\left(\frac{q\phi_z}{kT}\right)\frac{d\phi}{F_z}\frac{dV_x}{dx} \qquad 4.3.12$$

Poisson's Equation enables an expression for field F_z as a function of ϕ

$$\frac{dF_z}{dz} = \frac{qn}{\varepsilon_o\varepsilon_s} \qquad 4.3.13$$

Integration between F_z and 0 and between ϕ_z and 0 gives:

$$F_z \approx \left(\frac{2kTn_0}{\varepsilon_o\varepsilon_s}\right)^{1/2}\exp\left(\frac{q\phi_z}{2kT}\right) \qquad 4.3.14$$

Substituting *equation 4.3.14* into *equation 4.3.12* and integrating between I and 0 on one side, between ϕ_s and 0 on the other side and then simplifying gives:

$$I = W\left(2kT\varepsilon_o\varepsilon_s n_i\right)^{1/2}\exp\left(\frac{q\phi_s}{2kT}\right)\frac{dV_x}{dx} \qquad 4.3.15$$

Using the continuity of Displacement from Gauss's Theorem:

$$\varepsilon_{ox}F = \varepsilon_s F \qquad 4.3.16$$

Therefore

$$\frac{\varepsilon_{ox}\left(V_g - V_t\right) - V_x}{x_t} = \varepsilon_s\left(\frac{2kTn_i}{\varepsilon_o\varepsilon_s}\right)\exp\left(\frac{q\phi_s}{2kT}\right) \qquad 4.3.17$$

Rearranging *equation 4.3.17*, substituting it into *equation 4.3.15* and integrating between L and 0 and between V_D and 0, where L is the channel length, gives:

$$I = \mu\frac{W}{L}\frac{\varepsilon_{ox}\varepsilon_o}{x_t}\left[\left(V_g - V_t\right)V_d - \frac{V_d^2}{2}\right] \qquad 4.3.16$$

However the oxide capacitance, C_o is:

$$C_o = \frac{\varepsilon_{ox}\varepsilon_o}{x_t} \qquad 4.3.17$$

Therefore:

$$I_D = \mu C_o \frac{W}{L}\left((V_g - V_t)V_d - \frac{V_d^2}{2}\right) \qquad 4.3.18$$

which is identical to *4.2.6*. This is a surprising result since the exponential drop in carrier concentration in the semiconductor is very different from a delta function.

4.4 Exponential Distribution of States TFT Equation

This derivation is similar to that of the previous equation, the main difference is that T_c is used instead of T. T_c is a quantity defining an exponential distribution of states, which replaces the measurement temperature:

$$Jdz = \frac{dI}{W} = qn_i\mu \exp\left(\frac{q\phi_z}{kT_c}\right)\frac{d\phi}{F_z}\frac{dV_x}{dx} \qquad 4.4.1$$

Using the above equation, Poisson's equation and integrating gives:

$$I = \mu W(2kT_c\varepsilon_o\varepsilon_s n_i)^{1/2} \exp\left(\frac{q\phi_s}{2kT_c}\right)\frac{dV_x}{dx} \qquad 4.4.2$$

Combining Gauss's Law with the previous equation and integrating between L and 0 and between V_d and 0, gives:

$$I = \mu\frac{W}{L}\frac{\varepsilon_{ox}\varepsilon_o}{x_t}\left[(V_g - V_t)V_d - \frac{V_d^2}{2}\right] \qquad 4.4.3$$

or

$$I_D = \mu C_o \frac{W}{L}\left((V_g - V_t)V_d - \frac{V_d^2}{2}\right) \qquad 4.4.4$$

There are therefore identical equations for drain current using the following assumptions: a delta function, a distribution defined by a transport level and Debye Length, and exponential distribution of states with energy. It perhaps implies that a transport energy is applicable where there is an exponential distribution.

4.5 The Universal Mobility Law

As stated in the introduction of this chapter, the major problem with the previous equations is that they do not take into account the dependency of mobility on carrier density. A new model which incorporates this needs to be produced, to enable this to happen the relationship between carrier density and mobility needs to be derived.

Vissenberg and Matters have carried out analytical calculations using percolation theory and found that mobility increases with carrier density [1]. The derivation in this section does not use percolation theory but produces similar results, in that it shows that mobility increases with carrier density.

If band-type conduction is assumed:

$$\sigma = n_f q \mu_f \qquad 4.5.1$$

where n_f is the carrier concentration and μ_f is the mobility if carriers are free. The carrier concentration can be expressed as:

$$n_0 = N_c \exp\left(-\frac{E_c - E_F}{kT}\right) \qquad 4.5.2$$

where E_c is the energy of the conduction band edge, E_f is the extrinsic Fermi band and N_c is the effective density of states at a conduction band energy.

The exponential approximation to the tail of a Gaussian distribution of states can be approximated to be:

$$g(E) = \frac{N_o}{kT_c}\exp\left(\frac{E - E_o}{kT_c}\right) = \frac{N_i}{kT_c}\left(\frac{E - E_i}{kT_c}\right) = \frac{N_{co}}{kT_c}\exp\left(\frac{E - E_c}{kT_c}\right) \qquad 4.5.3$$

where N_o/kT_c is the density of states (per unit volume per unit energy) at an arbitrary energy level E_o, N_i/kT_c is the density of states at intrinsic level E_i and N_{co}/kT_c is the density of states at energy level E_c, E_c is the energy of the conduction band edge. This treatment should be compared with that described in Chapter 2. They amount to the same approach but in Chapter 2, the Fermi Dirac function is assumed to apply not only to the density of traps but also the rate of change of trap density with energy, while the approach used here is only applicable to an exponential distribution. Using either approaches, therefore, we can proceed to find the variation of mobility with carrier density.

As a result, therefore, of the exponential distribution of states and the application of the Pauli Exclusion Principle, leads to:

$$\mu = Kn^m \qquad 4.5.4$$

4.6 Full Equation with Universal Mobility Law

Doping leads to filling of the unoccupied states, this in turn leads to an increase in mobility. As the acceptor concentration increases further carriers continue to fill the

next highest levels and charge carrier levels can easily hop, as a result of the states being closely spaced together.

The current flowing between the contacts at some distance z from the interface is given by:

$$J = nq\mu F_x \qquad 4.6.1$$

Combining the two above equations gives:

$$J = Kn^{(m+1)}qF_x \qquad 4.6.2$$

This flows through a strip of area Wdz to give a current dI

$$dI = WKn^{(m+1)}qF_x dz \qquad 4.6.3$$

Poisson's equations states that:

$$\frac{d^2\phi}{dz^2} = \frac{qn}{\varepsilon_o\varepsilon} = \frac{qn_0}{\varepsilon_o\varepsilon}\exp\frac{q\phi}{kT} \qquad 4.6.4$$

And using F (=-dϕ/dx) as the integration factor:

$$-\frac{dF}{dz}F = -\frac{qn_0}{\varepsilon_o\varepsilon}\exp\frac{q\phi}{kT}\frac{d\phi}{dz} \qquad 4.6.5$$

Integrating between F_s and 0 and between ϕ_s and 0 gives:

$$\int_0^{F_s} FdF = -\frac{qn_0}{\varepsilon_o\varepsilon}\int_0^{\phi_s}\exp\frac{q\phi}{kT}d\phi \qquad 4.6.6$$

or

$$F_s \cong \left(\frac{2kTn_0}{\varepsilon_o\varepsilon}\right)^{\frac{1}{2}}\exp\frac{q\phi_s}{2kT} \qquad 4.6.7$$

where ϕ_S is the band bending at the surface, combining the above equations, with the equation for current density and $F = -\frac{d\phi}{dx}$ gives:

$$dI \approx WKn^{(m+1)}qF_x\frac{-d\phi}{\sqrt{\frac{2kTn_0}{\varepsilon_o\varepsilon}\exp\left\{\frac{q\phi_s}{kT}\right\}}} \qquad 4.6.8$$

At the surface, the electron concentration may be expressed as $n = n_o\exp\left(\frac{q\phi_S}{kT}\right)$.

This can be substituted into the previous equation to give:

$$dI \approx WK\left(n_0\exp\left(\frac{q\phi_s}{kT}\right)\right)^{(m+1)}qF_x\frac{-d\phi_s}{\sqrt{\frac{2kTn_0}{\varepsilon_o\varepsilon}\exp\left\{\frac{q\phi_s}{kT}\right\}}} \qquad 4.6.9$$

Rearranging and simplifying the above equation and integrating between 0 and the maximum surface bending, ϕ_s gives:

$$dI \approx WKn^{m+1/2} qF_x \sqrt{\frac{\varepsilon_o \varepsilon}{2kT}} \int_0^{\phi_s} \exp\left(\frac{q\phi_S\left(m+\frac{1}{2}\right)}{kT}\right) d\phi_s \qquad 4.6.10$$

$$dI \approx WKn_i^{m+(1/2)} \frac{F_x}{(2m+1)} \sqrt{2\varepsilon_o \varepsilon kT} \exp\left(\frac{q\phi_s\left(m+\frac{1}{2}\right)}{kT}\right) \qquad 4.6.11$$

Using Gauss' Law gives:

$$\exp\left\{\frac{q(m+1/2)\phi_s}{kT}\right\} = \frac{C_o^{2m+1}(V_g - V_t - V_x)^{2m+1}}{(2\varepsilon_o \varepsilon n_i kT)^{(m+1/2)}} \qquad 4.6.12$$

Substitution gives:

$$dI = \frac{WK}{(2m+1)} \frac{C_o^{2m+1}(V_g - V_T - V_x)^{2m+1}}{(2\varepsilon_o \varepsilon kT)^m} F_x \qquad 4.6.13$$

Substituting for J=I(Wdz) and F_x=-dV_x/dx, and integrating both sides give:

$$I_D \int_0^L dx = \pm \frac{KW}{(2m+1)} \frac{C_o^{2m+1}}{(2\varepsilon_o \varepsilon kT)^m} \int_0^{V_D} (V_g - V_t - V_x)^{2m+1} dV_x \qquad 4.6.14$$

Therefore, the general equation for the current flowing between the drain and source contacts is:

$$I_D = \frac{K}{(2m+1)(2m+2)} \frac{W}{L} \frac{C_o^{2m+1}}{(2\varepsilon_o \varepsilon kT)^m} \left[(V_g - V_t)^{2m+2} - (V_g - V_t - V_d)^{2m+2}\right] \qquad 4.6.15$$

The above equation does not contain the mobility. This is because for an exponential distribution of states the idea of constant drift mobility loses its meaning.

When however m=0 we have a single transport level and K=μ. Under these conditions *equation 4.6.16* becomes *equation 4.4.4*. For the Meyer Neldel Energy of 40meV we have m=0.6. and (2m+2) is equal to 3.2. If we rewrite *equation 4.6.15* as

$$I = \mu C_0 \left(\frac{W}{2L}\right)\left((V_g - V_t - V_d)^2 - (V_g - V_t)^2\right) \qquad 4.6.16$$

so that m=2. The effect on the carrier mobility of the exponential distribution is therefore very significant.

4.7 The Delta Function with Universal Mobility Law

The equation derived in the last section was significantly different from those previously defined. In the derivation in this section the universal mobility law will be used but the error of assuming a constant channel thickness will be examined.

Substituting the universal mobility law into an equation for current density leads to:

$$J = Kn^{(m+1)}qF \qquad 4.7.1$$

The charge per unit is given by $Q_o = -C_o(V_g - V_t - V_x)$, for a unit area of the channel with thickness Δz, the volume is equal to Δz, and $Q_o/\Delta z$,=qn; therefore:

$$J = \pm qK\left(\frac{Q_o}{q\Delta z}\right)^{m+1} F = \pm qK\left(\frac{C_o(V_g - V_t) - V_x}{q\Delta z}\right)^{m+1}\frac{dV}{dx} \qquad 4.7.2$$

The current can also be expressed by $I = JW\Delta z$; where W is the width of the TFT, therefore:

$$J = \pm qKW\Delta z\left(\frac{C_o(V_g - V_t) - V_x}{q\Delta z}\right)^{m+1}\frac{dV}{dx} \qquad 4.7.3$$

Integrating over L where the potentials are 0 and V_d gives:

$$I = \pm\left(\frac{K}{q^m\Delta z^m}\right)\frac{W}{L}C_o^{m+1}\left(\frac{(V_g - V_t - V_d)^{m+2} - (V_g - V_t)^{m+2}}{m+2}\right) \qquad 4.7.4$$

When however m=0

$$I = \pm K\frac{W}{L}C_o\left((V_g - V_t)V_d - \frac{V_d^2}{2}\right) \qquad 4.7.5$$

Which if K=μ gives:

$$I = \pm\mu\frac{W}{L}C_o\left((V_g - V_t)V_d - \frac{V_d^2}{2}\right) \qquad 4.7.6$$

4.8 Above Pinch-Off Equations

Shockley [2] used the term 'pinch-off' to describe the saturation process in unipolar field effect transistors, in such transistors the channel lies between two depletion regions, which expand with saturation until the channel thickness is zero, the channel is therefore effectively pinched between the depletion regions. The term is also used for field effect transistors as the channel region is pinched between the drain depletion region and the gate.

In the channel the pinch-off point corresponds to the edge of the drain depletion layer. When pinch-off has occurred the drain current should remain constant and be

independent of the drain voltage. The current is due to carriers that flow down the channel, when they reach the pinch off point they are injected into the depletion region, near the drain. Theoretically the current should remain constant because a constant gate voltage is assumed and because the current is only dependent on the potential drop between the start of the channel and the pinch-off point where the channel ends. However practically the increase in drain potential, will lead to the pinch-off point moving towards the source, this results in the shortening of the channel length, increasing the effective aspect ratio and hence its device constant there is therefore an increase in the drain current.

The equations derived in sections 4.2, 4.3 and 4.4 are identical, the equation derived is shown below:

$$I_D = \mu C_o \frac{W}{L}\left((V_g - V_t)V_d - \frac{V_d^2}{2}\right) \qquad 4.8.1$$

This equation however only applied below pinch-off, when $(V_g-V_t)>V_d$. *Equation 4.7.1* is a parabola, therefore for higher values of V_d (above pinch-off) it is necessary to alter the equation. The peak of the parabola is assumed to correspond to the maximum current which then becomes independent of V_d, the current at the peak can therefore be determined by differentiating with respect to V_d as shown below this gives:

$$\frac{dI_D}{dV_d} = \mu C_o \frac{W}{L}\left((V_g - V_t) - V_d\right) = 0 \qquad 4.8.2$$

Therefore $V_g-V_t=V_d$, substituting this back into *equation 4.8.1* gives an equation for above pinch off:

$$I_D = \mu C_o \frac{W}{2L}(V_g - V_t)^2 \qquad 4.8.3$$

The equation above is applicable for values of V_d which are larger than $V_g-V_t=V_d$, because the current almost saturates after this point, the diagram in *figure 4.8.1* illustrates this:

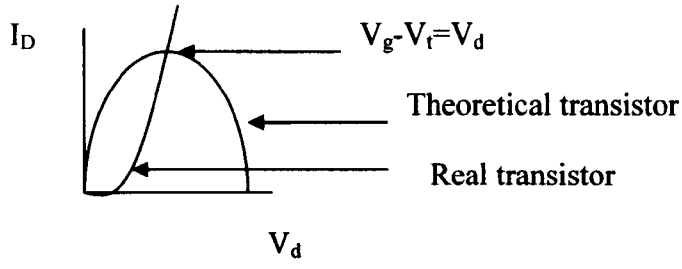

Figure 4.8.1: Current-Voltage plot to illustrate below and above pinch-off.

The Full Equation with Universal Mobility Law as expressed in *equation 4.6.15*, can be differentiated with respect to V_d to give:

$$\frac{dI_D}{dV_d} = \pm\frac{K}{(2m+1)}\frac{W}{L}\frac{C_o^{2m+1}}{(2\varepsilon_o\varepsilon kT)^m}\left[(V_g - V_t - V_d)^{2m+1}\right] = 0 \qquad 4.8.4$$

Therefore $V_d = V_g - V_t$, substituting this back into *equation 4.6.15* gives, an equation for above pinch-off:

$$I_D = \pm\frac{K}{(2m+1)(2m+2)}\frac{W}{L}\frac{C_o^{2m+1}}{(2\varepsilon_o\varepsilon kT)^m}(V_g - V_t)^{2m+2} \qquad 4.8.5$$

The Delta Function with Universal Mobility Law as expressed in *equation 4.7.4*, can be differentiated with respect to V_d to give:

$$\frac{dI_D}{dV_d} = \pm\frac{K}{q^m\Delta z^m}\frac{W}{L}C_o^{m+1}\left[(V_g - V_t - V_d)^{m+1}\right] = 0 \qquad 4.8.6$$

Therefore $V_d = V_g - V_t$, substituting this back into *equation 4.7.4* gives, an equation for above pinch-off:

$$I_D = \pm\frac{K}{q^m\Delta z^m}\frac{W}{L}\frac{C_o^{m+1}}{(m+2)}\left[(V_g - V_t)^{m+2}\right] = 0 \qquad 4.8.7$$

4.9 Drain Current Equation and PTAA

If equation *4.8.1* is compared with equation *4.6.15*, it can be seen that if m = 0, the two equations are identical. Calculating a value for m using *equation 4.6.15* may therefore help to indicate which set of assumptions is true.

Equation 4.8.5 is the version of full equation with universal mobility law above pinch off, using this equation, the values K, W, L, m, k, T, C_o, ε_o, ε can be considered to be constants, therefore let:

$$x = \frac{K}{(2m+1)(2m+2)}\frac{W}{L}\frac{C_o^{2m+1}}{(2\varepsilon_o\varepsilon kT)^m} \qquad 4.9.1$$

Therefore:

$$\log(I_D) = \log(x) + (2m+1)\log(V_g - V_t) \qquad 4.9.2$$

The output characteristics for a TFT fabricated by Merc (measured at Liverpool) using PTAA are shown in *figure 4.9.1,* the pinch off point is also shown, when V_T has been approximated to be 2.5V.

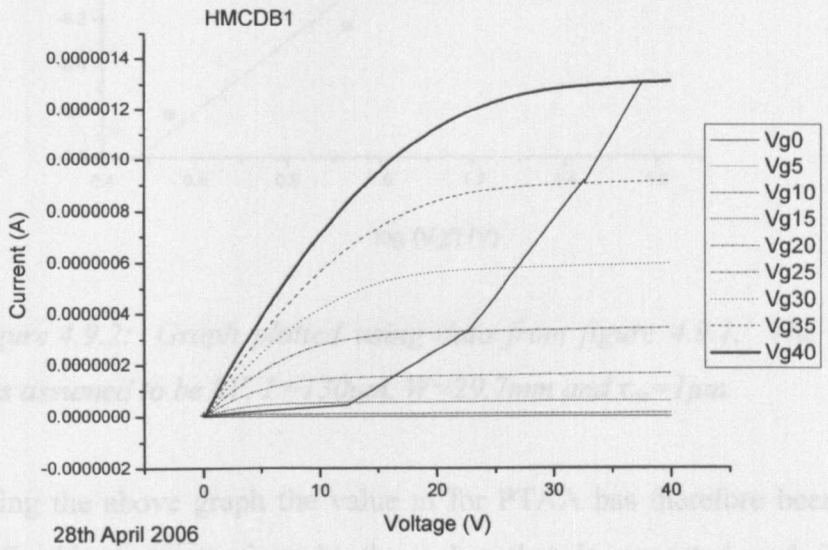

Figure 4.9.1: Output Characteristics of a TFT fabricated using PTAA by Merck, where L=130μm, W=29.7mm and τ_{ox}=1μm.

Using the data shown in the output characteristics and assuming that the threshold voltage is 0V, $\log(I_D)$ can be plotted against $\log(V_d)$, as shown by *equation 4.9.2* the gradient can therefore be used to find a value for m and the intercept can be used to find a value for K.

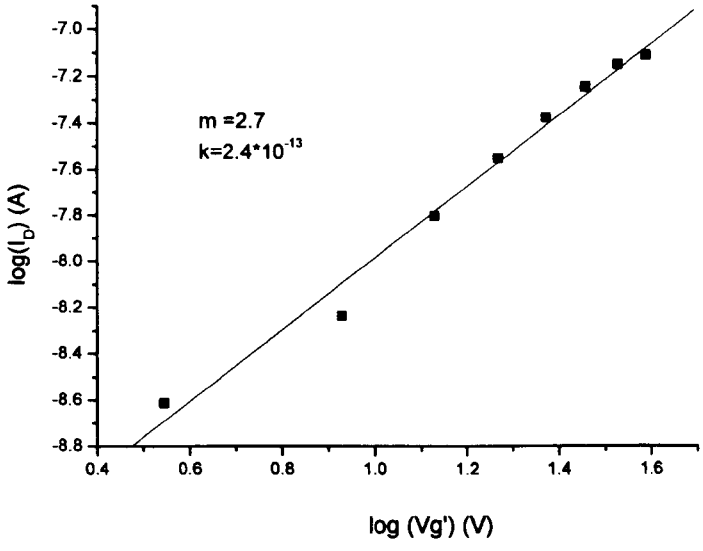

Figure 4.9.2: Graph plotted using data from figure 4.9.1. The threshold voltage was assumed to be 0V, L=130μm, W=29.7mm and τ_{ox}=1μm.

Using the above graph the value m for PTAA has therefore been calculated to be 0.27, this is approximately the value that is expected and indicates that the assumption that exponential distribution of states and that mobility depends on electron concentration is correct. The value of T_c can also be calculated to be 372Kelvin. The value of *K* has been found to be $2.4*10^{-13}$ using *equation 4.9.1*. The dimension of *K* depends on the value of m.

The graph in *figure 4.9.3*, compares the output characteristics found practically, with those found by the first 3 equations (the identical equation derived in sections 4.2 to 4.4), for various gate voltages.

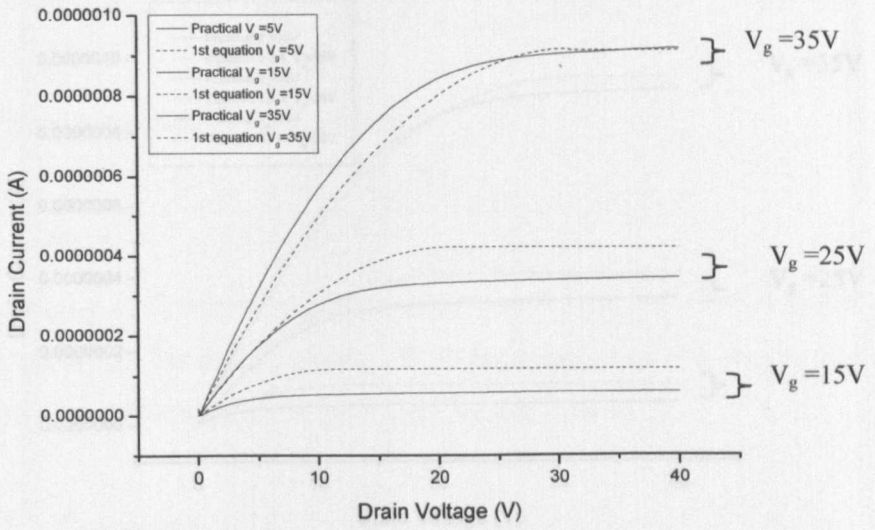

Figure 4.9.3: Graph comparing the practical results with those found using the equations derived in sections 4.2 to 4.4.

Figure 4.9.4 compares the output characteristics found practically with those found by the full equation.

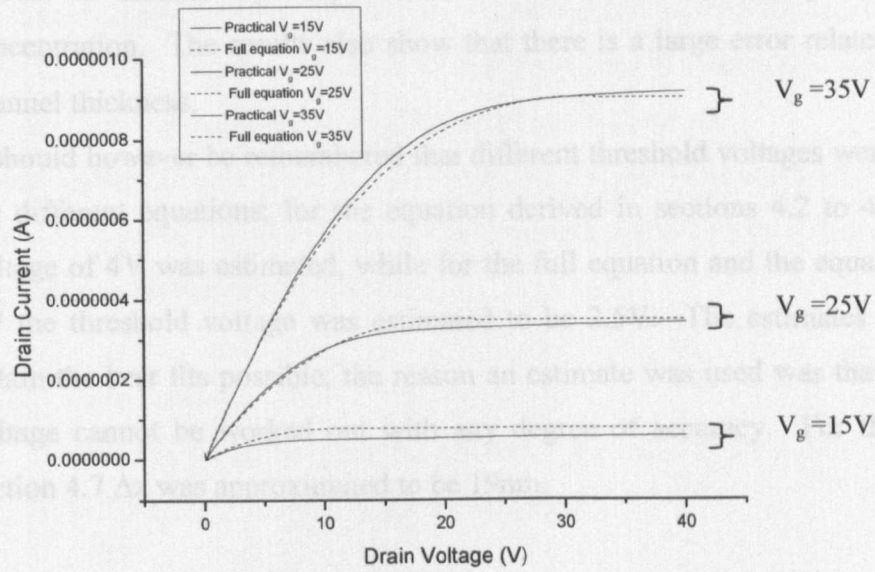

Figure 4.9.4: Graph comparing the practical results with those found using the equations derived in sections 4.6.

Figure 4.9.5 compares the output characteristics found practically with those found using the delta function with the universal mobility law.

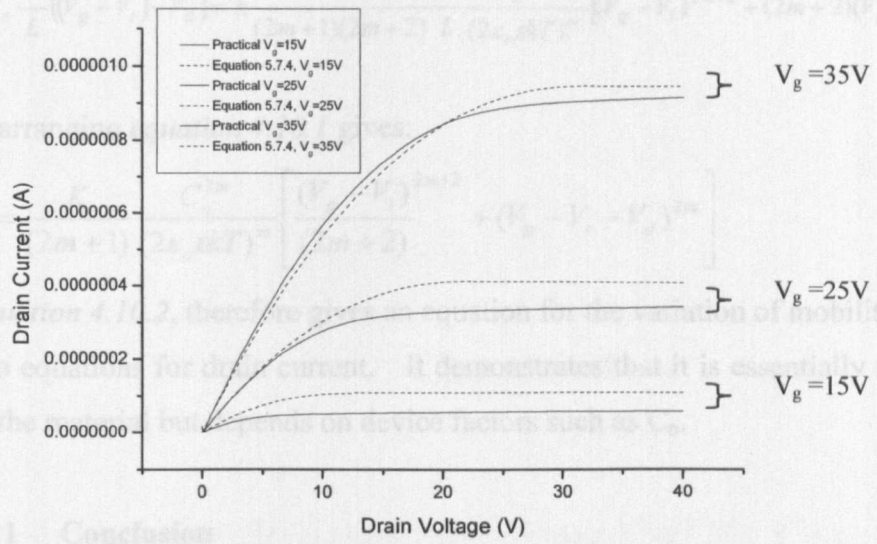

Figure 4.9.5: Graph comparing the practical results with those found using the equation derived in sections 4.7.

It can been seen that the full equation, fits the results obtained practically substantially better than the other equations, this enhances the indications that it is correct to assume that exponential distribution of states depends on electron concentration. The results also show that there is a large error related to assuming channel thickness.

It should however be remembered that different threshold voltages were assumed for the different equations; for the equation derived in sections 4.2 to 4.4 a threshold voltage of 4V was estimated, while for the full equation and the equation in section 4.7 the threshold voltage was estimated to be 2.5V. The estimates were made to obtain the best fits possible, the reason an estimate was used was that the threshold voltage cannot be worked out with any degree of accuracy. For the equation in section 4.7 Δz was approximated to be 19nm.

4.10 Mobility

Equating *equations 4.8.2* and *4.8.4*, which have both been derived by differentiating the identical equation derived in sections 4.2 to 4.4 and the equation derived in 4.6 for the drain current, gives:

$$\mu C_o \frac{W}{L}\left(\left(V_g - V_t\right) - V_d\right) = \pm \frac{K}{(2m+1)(2m+2)} \frac{W}{L} \frac{C_o^{2m+1}}{(2\varepsilon_o \varepsilon kT)^m} \left[(V_g - V_t)^{2m+2} + (2m+2)(V_g - V_t - V_d)^{2m+1}\right] \quad 4.10.1$$

Rearranging *equation 4.10.1* gives:

$$\mu = \frac{K}{(2m+1)} \frac{C_o^{2m}}{(2\varepsilon_o \varepsilon kT)^m} \left[\frac{(V_g - V_t)^{2m+2}}{(2m+2)} + (V_g - V_t - V_d)^{2m}\right] \quad 4.10.2$$

Equation 4.10.2, therefore gives an equation for the variation of mobility between the two equations for drain current. It demonstrates that it is essentially not a property of the material but depends on device factors such as C_o.

4.11 Conclusion

This chapter shows the derivation of the channel equation, using 5 different sets of assumptions. It was found that whether a delta function, a classical ordered band picture or an exponential distribution of states are assumed, the equations derived are identical. However the equation which took into account both exponential distribution of states and the dependence of mobility on electron concentration was very different, as was the equation which took into account the delta function with the universal mobility law. Although interestingly for *equations 5.6.16 and 5.8.14*, if m=0 they both become identical to the delta function equation, classical ordered equation and the exponential distribution of states equation.

It was shown that for devices made using PTAA the final equation derived had the best fit, therefore it is correct to assume that exponential distribution of states depends on electron concentration.

4.12 References

[1] M.C.J.M Vissenberg and M. Matters, *Phys. Rev. B*, **57**, 12964 (1998)

[2] W. Shockley. *Proc. IRE* **40,** p1365, 1952.

Chapter 5

Metal Oxide Semiconductor (MOS) Capacitors

MOS capacitors were first proposed in 1951, they are useful test structures as they form the basis of TFTs. In this chapter the electrical properties and characteristics of MOS capacitors are discussed. The Debye length has also been derived for both ordered and disordered materials. This is important as it confirms that assumptions regarding the depletion edge and high accumulation layer capacitances are valid.

5.1 Introduction

MOS capacitors are important electronic devices; they are a useful test structure, but also form the basis of the Thin Film Transistor, of DRAM and the CCD (charge coupled devices).

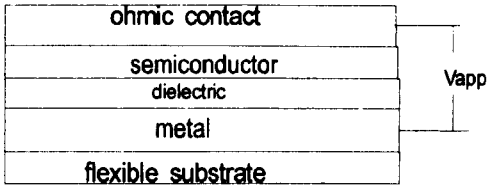

Figure 5.2.1: The cross-section of an MOS capacitor on flex.

Moss [1] first proposed the MOS capacitor in the form of a voltage variable capacitor in 1951. A similar structure with superficially similar electrical characteristic can be produced with organic semiconductors.

A series of semiconducting devices characterised by a voltage sensitive capacitance that resides in the space-charge region at the surface of the semiconductor bounded by an insulating layer was later investigated by Pfann and Garrett [2]. In the sixties Frankl [3] and Lindner [4] carried out further analysis of this structure. It is important in the context of this thesis because of the profound detailed information it contains. The mechanisms of transport and electrical instability are discussed in this thesis. The theory of the MOS capacitor in ordered material is a good starting point for the discussion of CV plots in disordered organic material.

Organic Metal-Oxide-Semiconductor (MOS) Capacitors, are two terminal devices, which consist of a metal on glass or flex substrate. On the metal there is a dielectric, and on top of this there is an organic semiconductor. The final layer is of a highly conducting metal such as gold which provides an ohmic contact to the polymer.

5.2 Electrical Properties of the MOS Capacitor

An MOS capacitor can be considered to consist of a parallel plate capacitor with one electrode a metal known as the gate and the other electrode, the semiconductor with a low resistance contact known as the substrate. The electrodes sandwich, an insulator such as silicon dioxide or aluminium oxide.

When a positive bias is applied to the gate, electrons accumulate at the semiconductor/insulator interface. The accumulation layer widths are very thin, usually between 10nm and 100nm depending on the peak carrier concentration and therefore the bias [5]. When a negative bias is applied to the gate, electrons in the

semiconductor are repelled from the surface and a depletion layer forms. There is a flow of positive charge which consists of minority carriers (holes) which are attracted to the interface, and a larger number of fixed positively charged donor atoms in the depletion region. This combination of positive charges balances the negative charge on the gate electrode. If the negative bias is increased, a large number of holes are attracted to the semiconductor/insulator interface and an inversion (p type) region is formed at the surface. One should bear in mind that traps and Fermi level pinning are beneficial to electrical conduction and the term inversion is perhaps misleading.

Figure 5.2.1 illustrates the results that are ideally expected when a small ac signal is superimposed on to the voltage which is ramped across an MOS capacitor's electrodes and the small signal capacitance is measured. A slow ramp voltage is used, going from positive to negative, and is added to the ac signal to vary the amount of energy level bending at which the capacitance is measured.

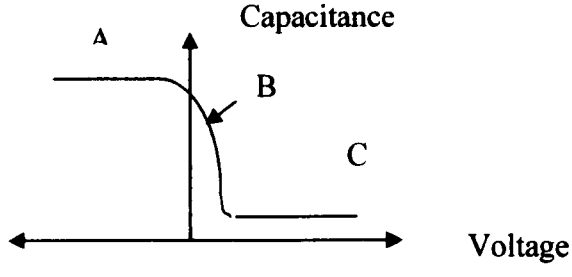

Figure 5.2.1: High frequency C-V plot for an ideal MOS capacitor with p-type semiconductor.

Region A is the accumulation region capacitance, holes accumulate at the semiconductor/insulator surface when a negative bias is applied to the gate, as shown in *figure 5.2.2(a).*

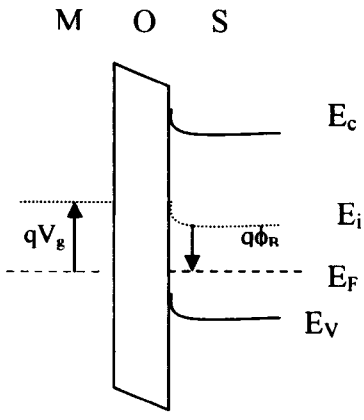

Figure 5.2.2(a): Accumulation.

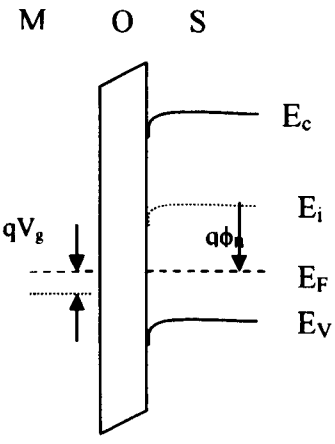

Figure 5.2.2(b): Depletion.

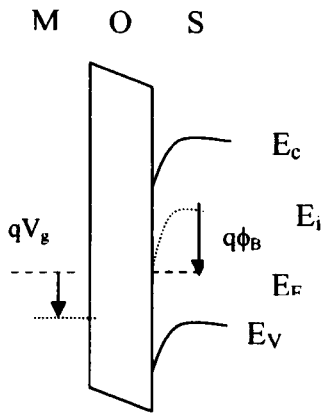

Figure 5.2.2(c): Inversion.

Region B is the depletion region capacitance; holes in the semiconductor are repelled from the surface forming a depletion layer, when a positive bias is applied to the gate. It is shown in *figure 5.2.2(b).*

Region C is the 'inversion' region capacitance, the negative charge balancing the positive charge on the gate consists of electrons (minority carriers) which are attracted to the interface and the exposure of negatively charged acceptor atoms in the depletion region. Inversion in the case of organics is rather more complex and will be discussed later. If the positive bias is increased, a large number of electrons are attracted to the semiconductor/insulator interface and an inversion region is formed at the surface, as shown in *figure 5.2.2(c).* This figure applies to a single crystal ordered material, in the case of disordered material; the level labeled E_C and E_V can be considered to be transport levels, or a single level within an exponential distribution of levels.

5.3 Analytical Treatment of the Variation of Capacitance with Ramp Voltage

Capacitance-Voltage measurements are the most important method of characterisation of the MOS capacitor. The simplest equivalent circuit for the MOS capacitor when it is under accumulation can be expressed by a capacitor representing oxide, C_{ox} in series with a capacitor representing carrier C_{acc} (or depletion) space charge as shown in *figure 5.3.1.* It should however be remembered that in *figure 5.3.1*, there are 4 capacitor plates, whereas in the MOS capacitor there are only 2.

The central two plates in the equivalent circuit are at the same potential, and overall the combined middle plates are electrically neutral, the charge on one plate being equal and opposite to that on the other.

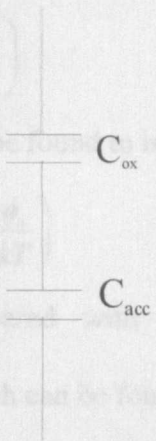

Figure 5.3.1: The representation of the geometric capacitance of the gate dielectric with that of the semiconductor accumulation layer.

$$\frac{1}{C_T} = \frac{1}{C_{ox}} + \frac{1}{C_{acc}} \qquad 5.3.1$$

The smaller of the two capacitances will always dominate this series situation. The accumulation capacitance is written as:

$$C_{acc} = \frac{\partial Q_{acc}}{\partial \phi_s} = \frac{\varepsilon_s A}{L_D} \qquad 5.3.2$$

where Q_{acc} is the charge associated with the accumulation layer and ϕ_S is the surface potential. L_D is the Debye Length which is a measure of the electrical width of the accumulation layer, the Debye length can be derived as shown below [6].

The free carrier concentration n, either electrons or holes, can be found using Poisson's equation, which states that:

$$\frac{d^2\phi}{dz^2} = -\frac{qn}{\varepsilon_o \varepsilon_s} \qquad 5.3.3$$

where for an ordered semiconductor

$$n = n_o \exp\left[\frac{q\phi}{kT}\right] \qquad 5.3.4$$

Using the field F as an integrating factor an expression for F can be obtained providing the exponential term is much greater than 1.

$$F = \left\{ \frac{2n_o kT}{\varepsilon_o \varepsilon_s} \exp\left[\frac{q\phi(x)}{kT} \right] \right\}^{1/2} \qquad 5.3.5$$

Applying Gauss's Law at the surface of the semiconductor the total charge Q_0 in unit area of the accumulation region can be found by:

$$Q_0 = \left(\frac{2n_o \varepsilon_o \varepsilon_s kT}{q} \right)^{1/2} \exp\left(\frac{q\phi_s}{2kT} \right) \qquad 5.3.6$$

The capacitance can therefore be found to be:

$$C_s = \frac{dQ}{d\phi_s} = \left(\frac{qn_o \varepsilon_o \varepsilon_s}{2kT} \right)^{1/2} \exp\left(\frac{q\phi_s}{2kT} \right) \qquad 5.3.7$$

If *equation 5.3.7*, is compared with the parallel plate capacitor equation $\left(C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{t_{ox}} \right)$, the Debye length can be found to be [6]:

$$L_D = \left(\frac{2\varepsilon_o \varepsilon_s kT}{q^2 n_s} \right)^{1/2} \qquad 5.3.8$$

where n_s is the carrier concentration at the interface with the dielectric.

The accumulation capacitance, C_{acc}, will be very large for negative values of V_G (assuming the polymer is p-type), this is because Q_{acc} has an exponential dependence on ϕ_s. The large value of C_{acc} means that the measured capacitance in this region will be approximately the same as C_{ox}. The above equation is equivalent to a parallel plate capacitor with an average distance of L_D. The oxide thickness can therefore be extracted:

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{t_{ox}} \qquad 5.3.9$$

where ε_o is the permittivity of free space, ε_{ox} is the relative permittivity of the oxide and A is the area of the gate electrode.

Assuming an ideal MOS capacitor, on ordered material, the capacitor is said to be in the flat band condition when the gate voltage is zero and the band bending at the surface is also zero. The simple equivalent circuit includes the flat band capacitance C_{FB}, as well as the dielectric capacitance. C_{FB} is given by

$$C_{FB} = \frac{\varepsilon_0 \varepsilon_S}{L_D} \qquad 5.3.10$$

where ε_S is the permittivity of the semiconductor. When V_{app} is positive and before inversion, the MOS capacitor is depleted. The width of this region is determined by

any residual dopant after chemical processing in the case of a polymer. With an ordered semiconductor the technology of introducing dopant is well developed and this will determine the Debye Length and the width of the depletion region. In the ideal case where there is no dopant the intrinsic carrier concentration n_i determines the width of surface region and it is approximately equal to the Debye length shown in *equation 5.3.8* where n_i is inserted.

Figure 5.3.2, illustrates what is known about charge in the depletion region.

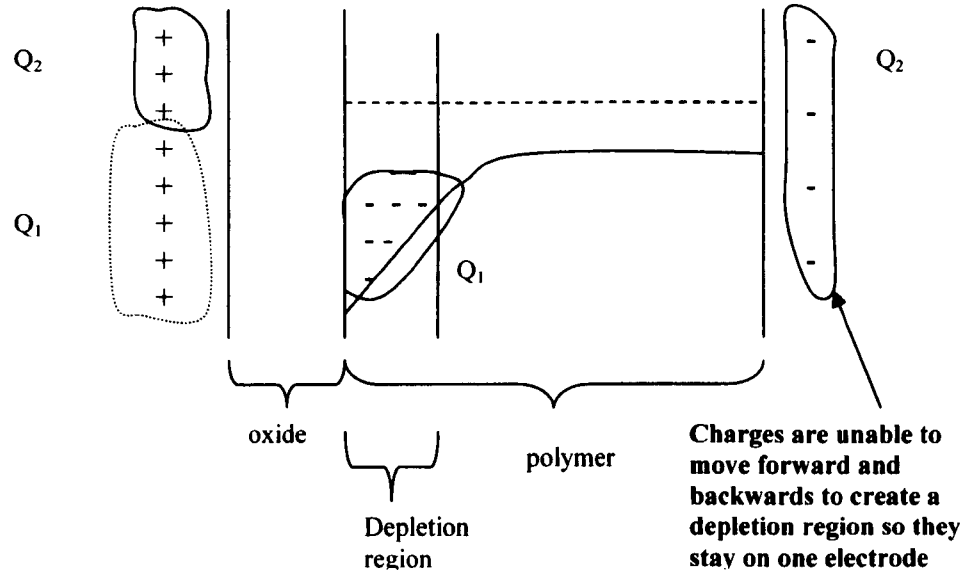

Figure 5.3.2: Charge in the depletion state of a capacitor

An expression for depletion capacitance [7] is given by :

$$C_{dep} = \left(\frac{qN_D \varepsilon_0 \varepsilon_s}{2\phi_s} \right)^{1/2} = \frac{\varepsilon_0 \varepsilon_s}{W} \qquad 5.3.11$$

where W is the width of the depletion layer.

The value of C_{dep} becomes similar to the value of C_{ox} as the depletion region widens, (due to an increase in the gate voltage) this leads to a drop in the measured capacitance.

For an inversion layer, a large increase in capacitance is expected at low frequencies. This is because the minority carrier density rises exponentially with increase in surface potential. This is only true if the minority carriers can follow the changes in gate voltage, which does not happen at high frequencies.

This is because, in this system, the electrons are provided by either generation or transport from the contact in the depletion region as the material attempts to reach charge equilibrium; but if the rate of generation of electrons is less than the rate of

change of the ac signal, then the charge cannot follow the changes in gate voltage. This means at low frequencies the capacitance raises to C_{max}, the oxide capacitance. The forms of an ideal C-V plot for both high and low frequencies are shown in *figure 5.3.3* [8].

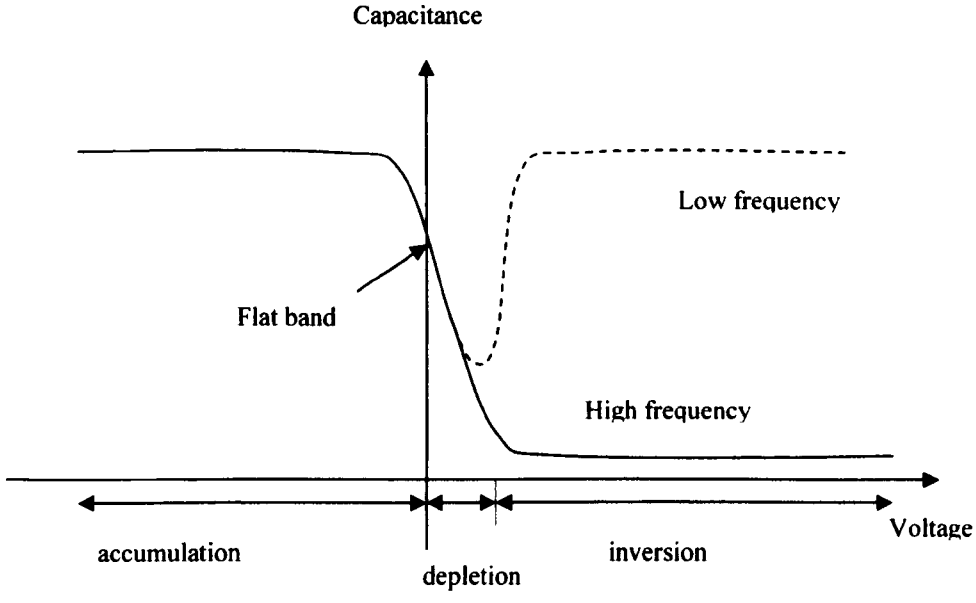

Figure 5.3.3: A C-V plot for an ideal silicon MOS capacitor with a p-type semiconductor, for high and low frequencies.

A slight increase in voltage will lead to an increase in the holes in the inversion region; however this is not possible at high frequencies, so the depletion region width will not be changed. This is because the carrier's generation and recombination rate cannot follow the applied voltage.

5.4 MOS Organic Capacitor Characteristics

A MOS capacitor for positive and negative voltages using an n type polymer is shown in *figure 5.4.1*. The voltages applied are ascending (or descending) d.c. voltages to which is added a small ac signal. The dc voltage is usually substituted by a ramp which is cycled from negative to positive voltage.

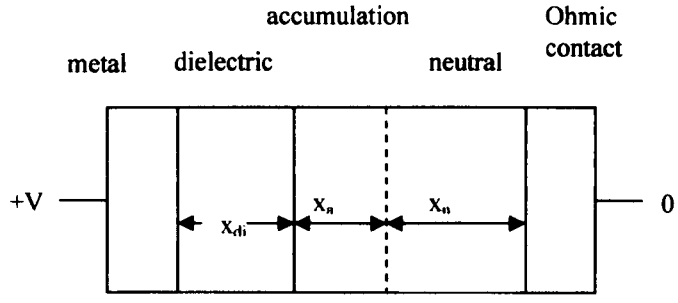

Figure 5.4.1a: A positive voltage applied to an MOS capacitor.

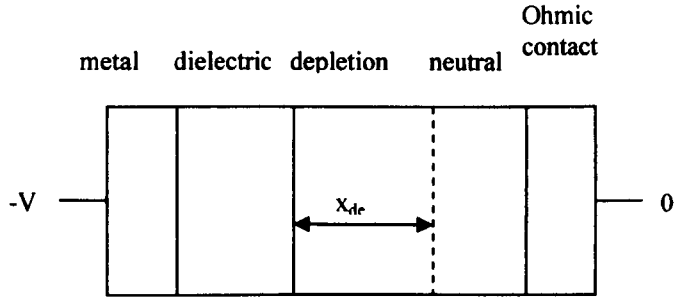

Figure 5.4.1b: A negative voltage applied to an MOS capacitor.

The form of a capacitance-voltage (CV) plot for an organic semiconductor is shown in *figure 5.4.2*, the maximum value which corresponds to accumulation is very frequency dependent. The minimum values, corresponds to the local rise in the density of states which prevents movement of the energy of the states with respect to E_F.

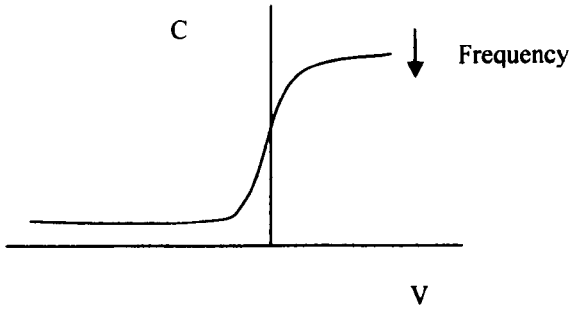

Figure 5.4.2: Capacitance-Voltage plot.

The number of carriers introduced by the applied voltage is increased by less than is required to significantly change the surface potential. It should also be remembered that excitons are unlikely to be generated close to the interface.

The semiconductor C_s, is defined by $dQ_s / d\phi_s$, where Q_s is the charge per unit area in the surface and ϕ_s is the surface potential.

It is given by the parallel plate formula: $C_s = \frac{\varepsilon_o \varepsilon_s}{L_D}$ *5.4.1*

where ε_s is the dielectric constant of the organic semiconductor, ε is the permittivity of free space and L_D is the Debye Length.

The derivation for *equation 5.4.1* is shown below; Poisson's equation can be used to find the equation below:

$$F_s = \left[\frac{2n_o kT_c}{q\varepsilon_o \varepsilon_s}\right]^{1/2} \exp\left[\frac{q\phi_s}{2kT_c}\right] \qquad 5.4.2$$

where T_c is the characteristic temperature of the distribution of states.

Using Gauss's Law the charge can be found to be:

$$Q_s = \left[\frac{2n_o kT_c \varepsilon_o \varepsilon_s}{q}\right]^{1/2} \exp\left[\frac{q\phi_s}{2kT_c}\right] \qquad 5.4.3$$

Therefore the surface capacitance, C_s, can be found:

$$C_s = \left[\frac{n_s q\varepsilon_o \varepsilon_s}{2kT_c}\right]^{1/2} \qquad 5.4.4$$

Hence

$$C_s = \frac{\varepsilon_o \varepsilon_s}{\varepsilon_o \varepsilon_s}\left[\frac{n_s q\varepsilon_o \varepsilon_s}{2kT_c}\right]^{1/2} = \frac{\varepsilon_o \varepsilon_s}{\left[\frac{2kT_c \varepsilon_o \varepsilon_s}{q^2 n_o}\right]^{1/2}} = \frac{\varepsilon_o \varepsilon_s}{L_D} \qquad 5.4.5$$

The Debye Length, L_D, is the distance over which the majority of accumulation charge carriers lie and the definition for an organic material is given by:

$$L_D = \left[\frac{2\varepsilon\varepsilon_o kT_c}{q^2 n_o}\right]^{1/2} \qquad 5.4.6$$

Poisson's equation states that:

$$\frac{dF}{dx} = \frac{q(n-p)}{\varepsilon_o \varepsilon_s} \qquad 5.4.7$$

The two carrier concentrations have different signs, this is because the field is characterised by the distribution of the majority carrier. The majority carrier may vary for different materials, for example there are p-type and n-type materials.

Therefore by integration, it can be found that:

$$F = \left(-\frac{2kT_c n_i}{\varepsilon_o \varepsilon_s}\right)^{1/2}\left[\exp\left(\frac{q\phi_s}{kT_c}\right)+\exp\left(-\frac{q\phi_s}{kT_c}\right)\right]^{1/2} \qquad 5.4.8$$

The charge can be calculated using Gauss's Law, applied to an infinitesimal thin cylinder normal to the interface.

$$Q = \left(-2\varepsilon_o \varepsilon_s kT_c n_i\right)^{1/2}\left[\exp\left(\frac{q\phi_s}{kT_c}\right)+\exp\left(-\frac{q\phi_s}{kT_c}\right)\right]^{1/2} \qquad 5.4.9$$

Therefore the capacitance can be found to be:

$$C_s = \frac{\varepsilon_o \varepsilon_s}{\varepsilon_o \varepsilon_s}\left(\frac{-q^2 \varepsilon_o \varepsilon_s (n_s + n_p)}{2kT}\right)^{1/2} - \frac{\varepsilon_o \varepsilon_s}{\varepsilon_o \varepsilon_s}\left[\frac{q}{kT_c}\exp\left(\frac{q\phi}{kT_c}\right)-\frac{q}{kT_c}\exp\left(-\frac{q\phi}{kT_c}\right)\right] \qquad 5.4.10$$

Therefore the Debye length can be defined as:

$$L_D = \left(\frac{2kT_c \varepsilon_o \varepsilon_s}{q^2 (n_s + n_p)}\right)^{1/2} \qquad 5.4.11$$

The low mobility in the neutral region means that this amount of charge is only delivered at the lowest frequencies. The period over which it is delivered is $\tau/2$, where τ is the period of the ac signal. This is a strong frequency dependence even down to low frequencies.

5.5 Fabrication of Polymer MOS Structures

Samples were constructed by anodising aluminium to form a combined gate contact and a gate dielectric. The electrolytic solution was citric acid which had been dissolved in deionised water and had nitrogen pumped through it, to remove unwanted gases from the electrolyte. The cathode used was platinum and the anode was the aluminium. When a positive voltage is applied to the anode, the water is electrolysed. The ionic oxygen, produced in the solution reacts with the ions in the aluminum to form Al_2O_3. The aluminium oxide grown on the sample in this manner when 35V is applied between the cathode and the anode is approximately 50nm thick [9]. After the films were formed, the samples were washed in distilled water before being annealed in a nitrogen atmosphere for 2 hours. Polymer or a polymer-DDQ composite was then spun onto the surface of the oxide and gold was evaporated on top to contact the polymer. The structure is shown in *figure 5.5.1.*

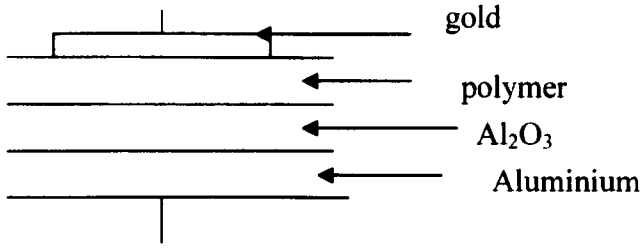

Figure 5.5.1: Sample structure for polymer MOS experiments.

Inversion in the conventional sense is not possible in polymers. This is because the carriers can only move by hopping. There are a number of possible mechanisms controlling C_{min}. It may be due to the depletion region reaching the back of the polymer film. A second possibility is that there is Fermi level pinning. A very large surface state density at a particular energy level could pin the Fermi level preventing further reductions in capacitance. Note that high trap densities mean high hopping rates so the traps involved are likely to be only at the surface.

The maximum capacitance, C_{max}, is dependent on the oxide thickness, however due to the geometric effect of the spreading of the current at the contacts with large dielectric thicknesses the current flow is not one dimensional.

If the variation of 'maximum' capacitance at a set voltage is measured at differences frequencies, mobility may be calculated. Note however there is a depletion layer of unknown thickness so that the total distance over which the carriers move through a neutral semiconductor is not accurately known.

5.6 Polymer Film Thickness

If it is assumed that C_{min} is due to the depletion region reaching the back of the polymer, the width of the depletion region, will be equal to the width of the polymer. Therefore

$$C_{min} = \frac{\varepsilon_0 \varepsilon_s A}{W} \qquad 5.6.1$$

where ε_s=3, ε_0=8.85.10^{-12}, A=7.85.$10^{-7}m^2$, C_{min}=290pF.

Figure 5.6.1, shows the measurements, in vacuum, obtained for a spun film.

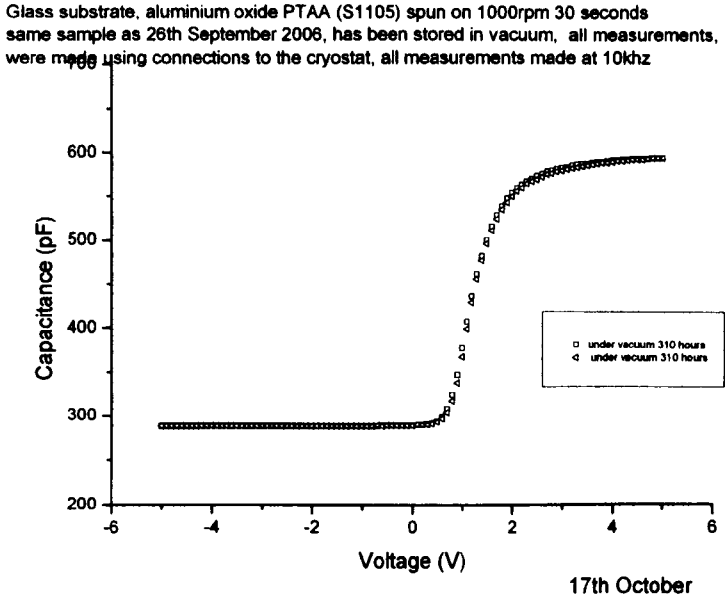

Figure 5.6.1: A C-V plot for a nominally undoped polymer with film showing p type behaviour because of residual impurities. The polymer used was PTAA and the gold contact had an area of 785nm^2.

Using *equation 5.6.1*, the thickness of the spun film is approximately 70nm.

5.7 Equivalent Circuit for an MOS Capacitor made in Organic Semiconductor

The model shown in *figure 5.7.1* is a possible circuit model, for an MOS capacitor, in accumulation the semiconductor capacitance C_{sc} would become the accumulation capacitance.

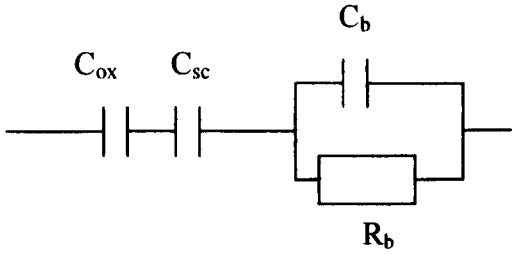

Figure 5.7.1: Circuit Model for an MOS Capacitor, where C_{sc} is the space charge capacitor, C_{ox} is the oxide capacitor, C_b is the bulk capacitor and R_b is the bulk resistance.

The total bulk admittance, at high frequencies is:

$$Y_b = \frac{1}{R_b} + sC_b \qquad 5.7.1$$

where $s = j\omega$.

The capacitors, C_{ox} and C_{sc} are in series, their total capacitance is given by C_1.

If $\frac{1}{C_1} = \frac{1}{C_{sc}} + \frac{1}{C_{ox}}$, the total impedance can be given by: 5.7.2

$$Z_{eq} = \frac{R_b}{1+sR_bC_b} + \frac{1}{sC_s} + \frac{1}{sC_{ox}} = \frac{1+sR_b(C_b+C_1)}{sC_1(1+sR_bC_b)} \qquad 5.7.3$$

The total admittance is therefore:

$$Y_{eq} = \frac{sC_1(1+sR_bC_b)}{1+sR_b(C_b+C_1)}\frac{1-sR_b(C_b+C_1)}{1-sR_b(C_b+C_1)} = sC_1\frac{1-s^2R_b^2C_b(C_b+C_1)}{1-s^2R_b^2(C_b+C_1)^2} - \frac{s^2R_bC_1^2}{1-s^2R_b^2(C_b+C_1)^2}$$

5.7.4

If $C_{eq}(s) = C_1\frac{1-s^2R_b^2C_b(C_b+C_1)}{1-s^2R_b^2(C_b+C_1)^2}$ and $R_{eq}(s) = \frac{1-s^2R_b^2(C_b+C_1)^2}{s^2R_bC_1^2}$ 5.7.5

Then: $Y_{eq} = sC_{eq}(s) + \frac{1}{R_{eq}(s)}$ 5.7.6

The device can therefore be modeled in the following way:

At very low frequencies $C_{eq}=C_1$ and $R_{eq}=\infty$.

At high frequencies

$$C_{eq}(s) = \frac{C_bC_1}{C_b+C_1} \text{ and } R_{eq} = \frac{R_b(C_b+C_1)^2}{C_1^2} \qquad 5.7.7$$

If the model in *figure 5.7.1* was simplified, by removing the bulk resistance, all three capacitors would be in series with each other. The diagram in *figure 5.7.2* shows the energy diagram for this situation. The sum of all charges should be zero. For the device to be in accumulation, a negative bias should be applied to the back contact. This induces an equal and opposite, positive charge in the oxide, as shown. The positive charge in turn induces an equal and opposite charge at the interface as shown. This negative charge leads to a positive charge being induced in the accumulation layer, which will cause the energy level bending shown. Hence:

$$C_{acc} = \frac{dQ_1}{d\phi}. \qquad 5.7.8$$

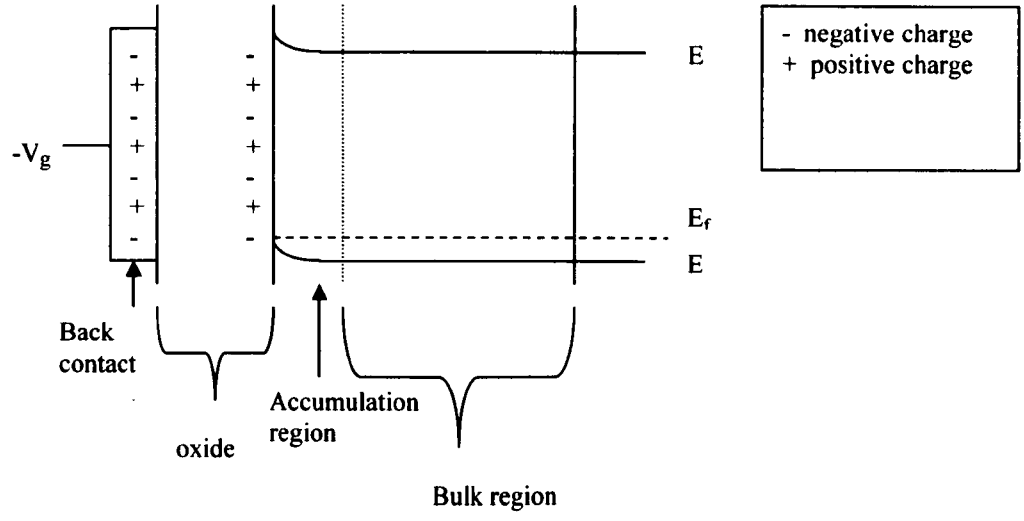

Figure 5.7.2: Band diagram for an MOS Capacitor in accumulation. The levels marked E are two energy levels in the upper and lower distributions of states.

However, there appears to be no charge specifically associated with the bulk region so there would appear to be no bulk capacitance. There is however charge on the ohmic contact metal and there must be a finite potential drop to drive the current in this 'bulk' region. By the simple definition

$$C = \frac{dQ}{d\phi} \qquad 5.7.9$$

there is a bulk capacitance.

If is assumed that the accumulation capacitance is much larger than the oxide capacitance, at low frequencies, then the following approximation can be made:

$$\omega_c = \frac{1}{R_b(C_b + C_{ox})} \qquad 5.7.10$$

Using *figure 5.7.1*, if it is again assumed the depletion region reaches the back of the polymer $C_{min}=C_b=290pF$. The capacitance can then be plotted against frequency as shown in *figure 5.7.3*.

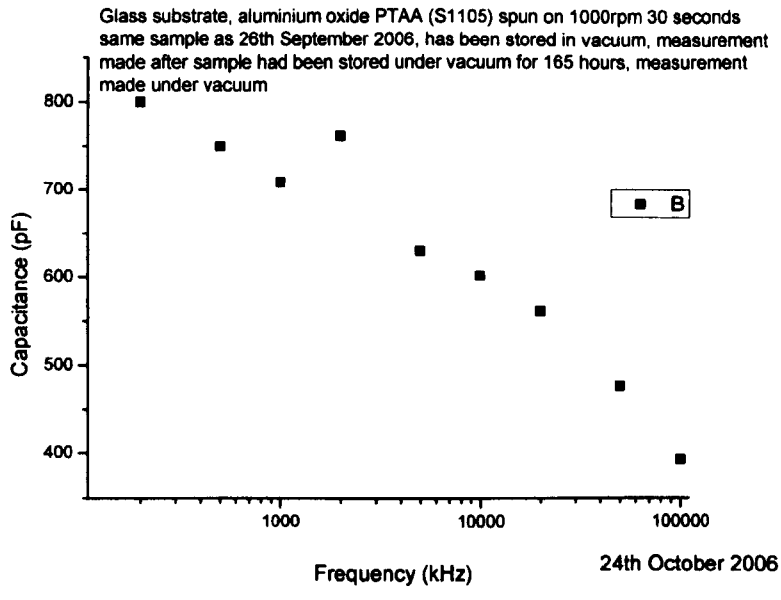

Figure 5.7.3: The variation of capacitance with frequency for an capacitor consisting of an alumina dielectric and a PTAA layer.

Figure 5.7.3, can be used to find an approximate value for C_{max} and ω_c. C_{max} was approximately 810pF and ω_c is 10^5 rad/sec. R_b is then found to be 9kΩ.

R_b can also be expressed by the following equation:

$$R_b = \frac{t_s}{N_A q \mu A} \qquad 5.7.11$$

Where $A=7.85e^{-7}m^2$, $t_s=70nm$, $N_A=10^{22}m^{-3}$ and $q=1.6e^{-19}C$, using these valves, a value for the bulk mobility in the capacitor is found to be $6.1nm^2V^{-1}s^{-1}$.

When a device is in accumulation, a low dopant concentration, leads to a relatively high resistance, this means that the cut off point is much lower than the measured frequency, as shown in *figure 5.7.4*.

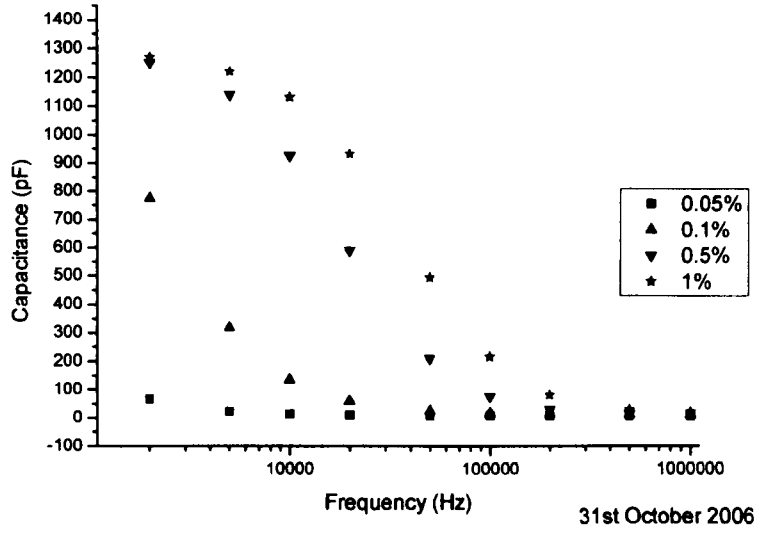

Figure 5.7.4: Capacitance-Frequency plot obtained from MOS capacitors, which have a cast film with variable percentages of dopant.

5.8 Conclusion

This chapter focuses on the Metal-Oxide-Semiconductor (MOS) Capacitor Theory and results. It discusses known effects in silicon and related effects in organic semiconductors. MOS capacitors are important as test structures and because they form the basis of thin film transistors. They are also useful because of the light they shed on electrical instability in organic devices which will be discussed later in this thesis.

The Debye Length has been derived for both ordered and disordered semiconductors. It is important because it confirms that abrupt depletion edge approximation as well as the high accumulation layer capacitance are as good in disordered material as in, for example crystalline silicon. These assumptions are essential for analytical device physics. Explanations of C_{min} and C_{max} in organic material have been discussed alongside experimental results.

5.9 References

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Chapter 6

Nature of Hysteresis

There are many different causes of instability; hysteresis is one sign of the presence of instability. This chapter discusses the different possible causes of instability. The hysteresis observed in devices is also discussed in relationship to the different mechanisms of hysteresis and conclusions are drawn regarding the possible mechanisms involved.

6.1 Introduction

There are many different causes of instability in semiconductor devices and circuits. They may be the result of movement and trapping of carrier ions and may be the result of ambient or other gases. Another possibility is that instability may be produced during the manufacture of the device. Wet processing has almost been eliminated in some industries to avoid the introduction of impurities, for example from solvents and containers. Instabilities can show themselves over a variety of time scales from microseconds to years, they manifest themselves though changes to the basic parameters of the circuits, examples include hysteresis, most instability in polymers are studied at normal operating temperatures which allows the study of some of the mechanisms although higher specifications are usually demanded by much of the market. Hysteresis is observed in MOS capacitors, TFTs and Schottky diodes. The evidence for a particular mechanism comes mainly from the capacitance-voltage plot for MOS capacitors and TFT transfer characteristics; it is also useful to consider Schottky diodes, although the direction of hysteresis in Schottky diodes will not always conform to those observed in MOS capacitors. Instability in Schottky diodes tends to be less as ions can for example be neutralized at the contact.

Structures whose gate insulators are inorganic and which have a high dielectric constant are much less vulnerable to ionic instabilities than those which are organic and have a low dielectric constant, this therefore proves a useful comparison as it indicates that the instability is caused by differences between the structures with problems in the gate dielectric being a likely cause. One of the first signs of electrical instability is a shift in the CV plot or the transfer characteristics of a TFT when a gate voltage is applied.

Most hysteresis that has been observed is in an anticlockwise direction and the direction of hysteresis can sometimes be used to identify the mechanism, as will be described later in this chapter.

It should also be remembered that the time required for the shift in the CV or IV plots is also potential evidence of the mechanism, for example percolation of carriers is relative quick compared to ion motion, which is usually in the order of seconds.

6.2 Carrier Hopping

One possible cause of hysteresis is carrier movement between the semiconductor and gate dielectric. The carriers can be either in the form of electrons or holes or a combination of both. A carrier that originates in the semiconductor and is then trapped in the dielectric may not be able to reverse the transition even if the field is removed or reversed. This is a result of semiconductor traps coincident with the trapped energy being scarce this results in carrier back tunnelling being an unlikely event.

Figure 6.2.1 illustrates how a hole may be trapped. Above a single energy level there is a greater chance of hopping occurring although initially it is unlikely that there are many holes; however below this energy level, hopping is unlikely. It should be remembered that it has been assumed that a positive voltage is applied for a prolonged period of time.

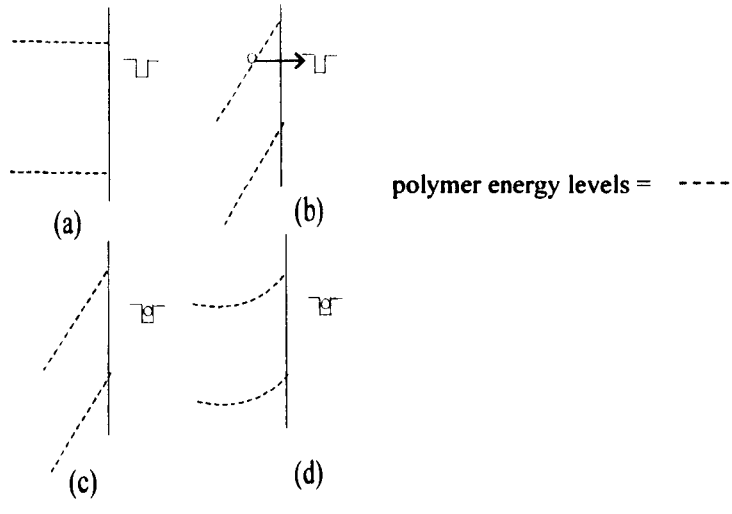


Figure 6.2.1(a): A trap lower in energy than the lowest energy at which conduction takes place.
Figure 6.2.1(b) and (c): Show that with a negative gate bias tunnelling becomes possible.
Figure 6.2.1(d): Removal of the bias leaves the electron trapped.

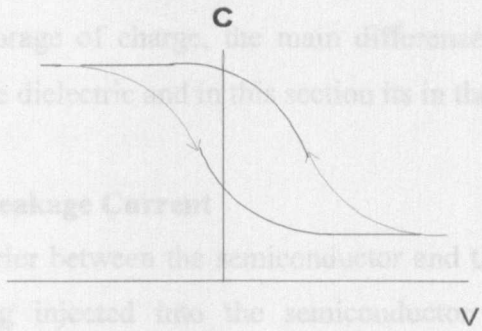


Figure 6.2.2: Anticlockwise which corresponds to this mechanism.

Therefore there is anticlockwise hysteresis. There will however be many such traps in the dielectric and they can either be distributed in energy levels or be monoenergetic and be spread with distance into the dielectric. Some holes will be able to tunnel back, some will not depending on their energy in the presence of an applied field.

6.3 Carrier Percolation

If an MOS capacitor is fabricated using a p-type material, hole injection will occur when the ohmic contact to the semiconductor is positively biased. Holes with high energy and therefore high mobility will travel through the material until they percolate down in energy to the widely spaced levels where they become trapped, as shown in *figure 6.3.1.*

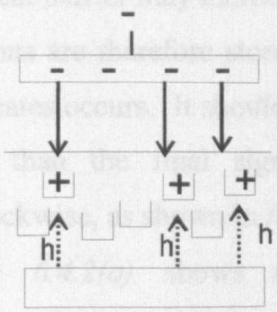


Figure 6.3.1: Hole percolation.

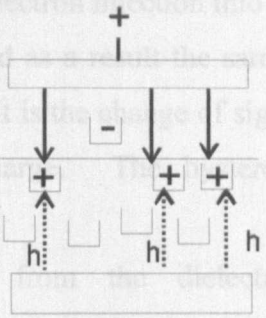


Figure 6.3.2: Production of a positive charge.

A positive charge in the gate electrode may be produced by a fraction of the trapped electrons, as shown in *figure 6.3.2.* The effect of the resulting field across the interface is to accumulate the semiconductor so that higher energy traps are filled. Therefore there is anticlockwise hysteresis, as shown by *figure 6.2.2.*

Although the carrier hopping and carrier percolation methods are different they both involve the storage of charge, the main difference is in the previous section this storage is in the dielectric and in this section its in the semiconductor.

6.4 Gate Leakage Current

A reduced barrier between the semiconductor and the dielectric may result in some electrons being injected into the semiconductor from the back contact; these electrons are likely to enter the gate dielectric and may even flow into the gate electrode. *Figure 6.6.1(a)* shows electrons tunnelling from the semiconductor to the dielectric.

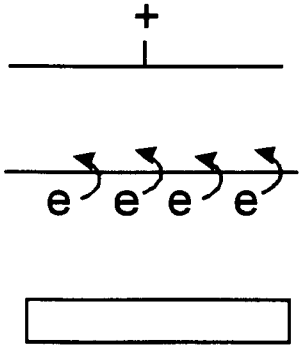


Figure 6.4.1(a): Electrons tunnelling from the semiconductor to the dielectric.

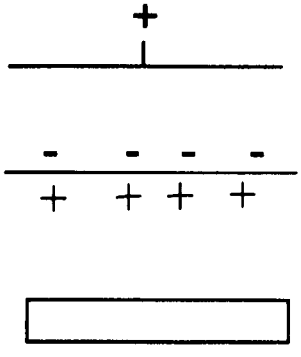


Figure 6.4.1(b): Positive charge will be induced.

A positive charge will be induced in the semiconductor, as shown in *figure 6.4.1(b).* The local barrier may increase to prevent further electron injection into the dielectric. Electrons are therefore stored in the dielectric and as a result the same shift as the slow states occurs. It should be remembered that it is the change of sign that matters rather than the final sign of the trapped charge. The hysteresis is again anticlockwise, as shown in *figure 6.2.2.*

Figure 6.4.2(a) shows electrons tunnelling from the dielectric into the semiconductor. A positive charge will then be induced into the dielectric as shown in *figure 6.4.2(b).* The hysteresis will again be anticlockwise.

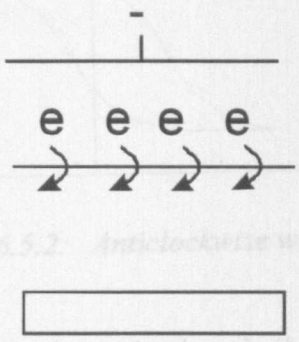


Figure 6.4.2(a): Electrons tunnelling from the dielectric to the semiconductor.

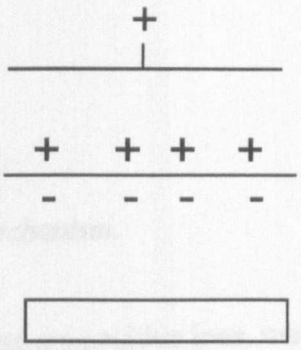


Figure 6.4.2(b): Charge will be induced.

6.5 Ion Movement in the Semiconductor

TFT films are usually cast or spun from solution; however the solvents are relatively impure for microelectronics, when the films dry ions may therefore be left in the film. The density of active ions can be measured and no density less than $10^{15}cm^{-3}$, can be found, this however is a small percentage of the total concentration of impurities.

Although the films are not very dense, very large molecular structures are not likely to be able to move through the structure by either drift or diffusion.

Small ions may however be able to move through the film and the gate voltage may have an effect on their movement speed. *Figure 6.5.1(a)* shows negative ions in a p-type semiconductor; when a positive voltage is applied; these ions are attracted towards the interface and positive charge is induced as shown in *figure 6.5.1(b).* The surface is being accumulated with charge therefore there is anticlockwise hysteresis as shown in *figure 6.5.2.*

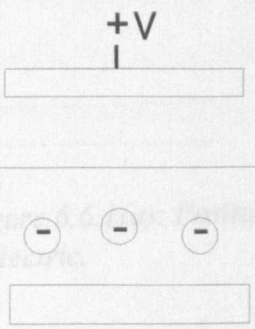


Figure 6.5.1(a): Negative ions in the semiconductor.

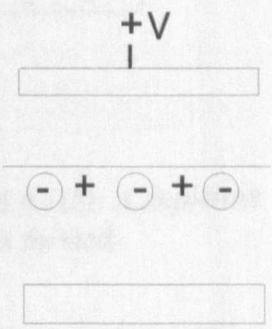


Figure 6.5.1(b): Positive charge will be induced.

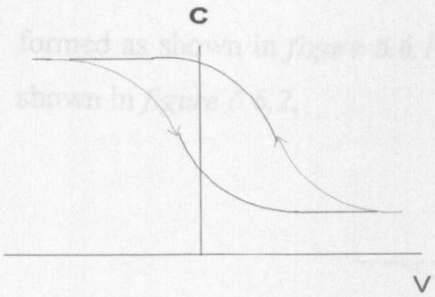


Figure 6.5.2: Anticlockwise which corresponds to this mechanism.

If instead of negative ions in the p-type semiconductor there are positive ions, when a positive voltage is applied, these ions will be repelled away from the surface and carriers will then accumulate at the interface. Hysteresis will again be anticlockwise.

6.6 Instability in the Gate Dielectric

Ions which are present in the gate dielectric may drift and diffuse through the material. When these ions are close to the gate dielectric they produce a small amount of charge in the semiconductor.

More charge is induced in the dielectric as a result of the ions drifting or diffusing. In effect there is a transfer of charge from the gate to the semiconductor. *Figure 6.6.1* illustrates the process; assuming a p-type semiconductor with a positive voltage applied; positive ions are repelled, from the gate as shown in *figure 6.6.1(a).*

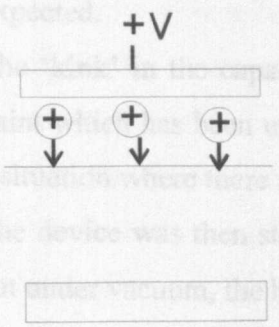


Figure 6.6.1(a): Positive ions in the dielectric.

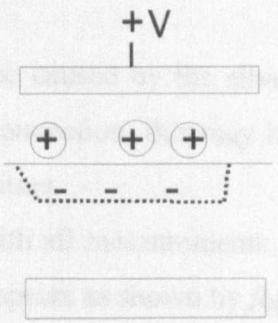


Figure 6.6.1(b): A depletion region is formed.

Positive ions have been repelled towards the interface from the gate. This results in negative carriers being induced in the semiconductor; and a depletion region is

formed as shown in *figure 6.6.1(b)*. There will therefore be clockwise hysteresis as shown in *figure 6.6.2*.

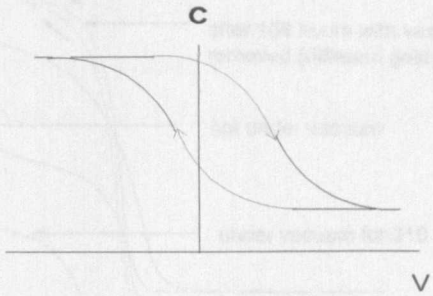


Figure 6.5.2: Clockwise hysteresis which corresponds to this mechanism.

If negative ions are present, when the positive voltage is applied, the negative ions will be attracted towards the positive gate voltage. This will result in negative carriers being repelled from the gate and an accumulation region will be formed at the interface. There will therefore be clockwise hysteresis.

6.7 Hysteresis Observed in Devices

Typically anticlockwise hysteresis is observed from MOS capacitors. The results in *figure 6.7.1* are for a capacitor which has been fabricated using aluminium oxide and PTAA. The device was placed in a cryostat; all measurements were made at a frequency of 10kHz. Before the vacuum was applied, the capacitance-voltage characteristics were measured, there was found to be an anticlockwise hysteresis as expected.

The 'kink' in the capacitance-voltage plot may be caused by the silver conduction paint which has been used to make an electrical connection; this may in effect make a situation where there are two back to back capacitors.

The device was then stored under the vacuum, with all measurements being carried out under vacuum, the hysteresis reduces and disappears as shown by *figure 6.7.1*.

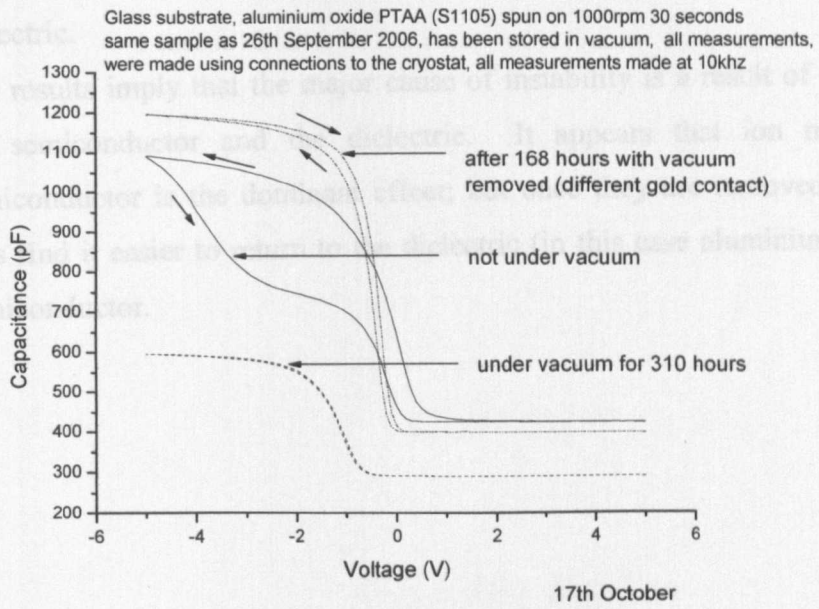


Figure 6.7.1: Capacitance-voltage plot, for a PTAA MOS capacitor, to show the effect of applying a vacuum. The gold contact had an area of 7.85nm^2.

One possibility is that ions or moisture in the device are drawn to the surface and out of the device by the vacuum, hence after time in the vacuum hysteresis is removed. The clockwise hysteresis observed after the vacuum has been released as shown in *figure 6.7.1*, could have been a result of ions entering the dielectric.

These results perhaps indicate that ion movement is the main cause of hysteresis; the effect would appear to be more dominant in the semiconductor layer hence the anticlockwise hysteresis observed before the vacuum was applied. The measurements after the vacuum has been removed suggest that ions find it easier to return to the dielectric than to the semiconductor hence the clockwise hysteresis.

The accumulation capacitance varies as a result of low hole mobility at higher frequencies. Removing air from the capacitors surroundings, acts to de-dope the material, this changes the resistance of the bulk material. The change in bulk resistance with air exposure leads to the variation in accumulation capacitance.

6.8 Conclusion

Possible causes of hysteresis have been examined. The majority of causes of instability produce anticlockwise hysteresis. These include carrier hopping, carrier percolation, gate leakage current and ion movement in the gate dielectric. The main

cause of clockwise hysteresis appears to be instability (ion movement) in the gate dielectric.

The results imply that the major cause of instability is a result of ion movement in the semiconductor and the dielectric. It appears that ion movement in the semiconductor is the dominant effect; but once they are removed by the vacuum; ions find it easier to return to the dielectric (in this case aluminium oxide) than the semiconductor.

Chapter 7

Schottky Diodes

Schottky diodes are essential in many organic circuits. This chapter discusses the effect of dopant including the effect on T_c values and Meyer Neldels energy. The effect of polymer in Schottky diode fabrication is also discussed as is hysteresis in Schottky diodes.

7.1 Introduction

The Schottky diode is named after Walter Schottky; in 1938 he developed a theory that predicted the Schottky effect [1]. Schottky diodes will be an essential part of many circuits including the rfid circuit, were they will be used in the rectifier to form a 4 diode bridge. There are however problems with diodes in organic integrated circuits, as they cannot operate at high frequencies.

Schottky diodes are useful for characterising polymers and the effect of doping. This including finding the values of T_c, T_o, the ideality factor and the Meyer Neldel energy. In 1937 Meyer and Neldel [2]; reported a compensation effect for the activated conductivity of oxide semiconductors. T_o defines the exponential distribution of carriers while T_c is a quantity defining an exponential distribution of states.

The physical significance of the Meyer Neldel energy is that if there are a large number of defects, a bell shaped Gaussian distribution will be produced, the tail of which is equivalent to E/kT_c; which is a measure of defects through which current passes.

For an intrinsic disordered material T_c will be appropriate 450K and the Meyer Neldel energy will be $6.2.10^{-21}$ Joules, however if the material is heavily doped, the Meyer Neldel energy will double as a result of Fermi level pinning.

For a more ordered material such as a single crystal semiconductor the value of Meyer Neldel energy will be infinity.

7.2 Fabrication of Polymer Schottky Diodes

A gold stripe is evaporated onto a glass substrate to form a contact. If PTAA (provided by Merc) is being used, the substrate is then left in ohmic contact solution for 10 minutes before being rinsed in propanol, the purpose of this is to ensure that the polymer forms an ohmic contact with the gold. After the treatment to form an ohmic contact if it is needed, the polymer is cast onto the substrate it is then left to dry under vacuum for ten hours, before an aluminium stripe is evaporated onto the polymer at right angles to the gold stripe, the aluminium stripe is the rectifying contact, which forms a Schottky junction in this case. The rectification arises from the presence of a potential barrier between the two materials.

7.3 Typical Characteristics of a Schottky Diode

The typical structure of a Schottky diode is a polymer sandwiched between a gold and aluminium contact as shown in *figure 7.3.1.*

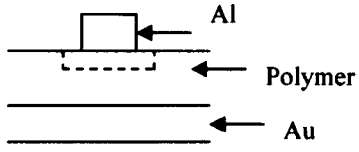


Figure 7.3.1: The structure of a Schottky diode.

The graph in *figure 7.3.2,* shows the typical current-voltage (I-V) characteristics for a Schottky diode.

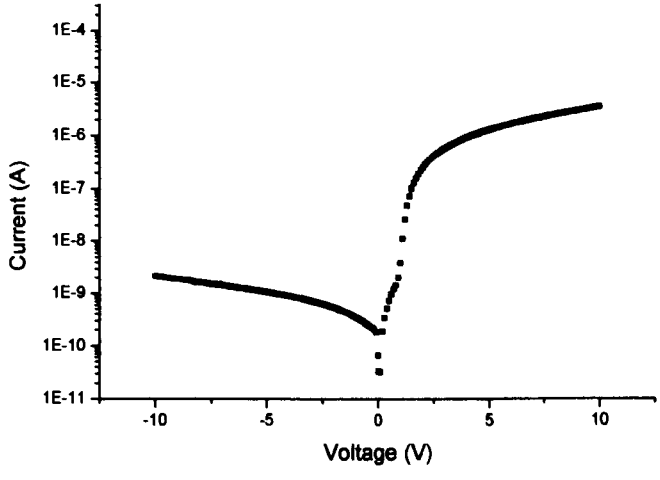


Figure 7.3.2: Typical I-V characteristics for a Schottky diode, fabricated using PTAA and with a contact area of 4μm².

The positive potential applied to the gold electrode leads to a decrease in the barrier, which means the holes find it easier to overcome the barrier and this leads to an increase in current.

When a positive bias is applied the holes move in the opposite direction, holes cannot exist in the metal so instead of being absorbed by the metal an electron leaves the metal and joins with the hole to form an exciton, the aluminium contact is negatively biased with respect to the gold contact which results in more electrons being supplied.

The reverse current in the I-V graph shown is lower than the forward current because of the Schottky barrier, the negative potential causes the barrier to increase, which

means that the holes find it harder to overcome the barrier and this leads to a reduction in the current (and therefore a lower reverse current).

The current under a reverse bias is due to the concentration of holes with enough energy to overcome the energy difference between the metal Fermi level and the valence band. The holes will travel towards the gold, while electrons will travel through the depletion region to the aluminium, an example of this occurring in a perfect diode with no hysteresis is shown in *figure 7.3.1*.

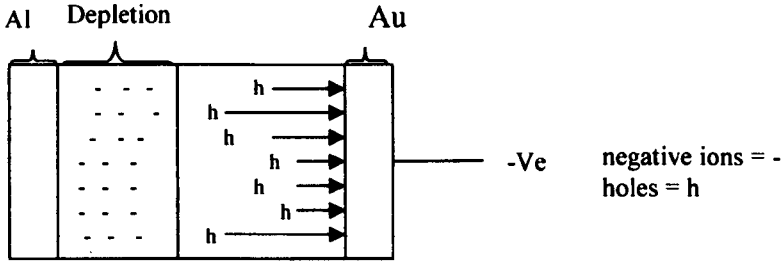


Figure 7.3.1: A perfect diode with no hysteresis, with a reverse bias applied towards the gold contact.

7.4 The Effect of Dopant

The diagram in *figure 7.4.1*, shows the effect of doping Lisicon with DDQ, the diodes were fabricated as described earlier, with DDQ being dissolved in tetraline and then added to the Lisicon, the mixture was then subjected to ultrasound, this agitates the solution and allows the DDQ and Lisicon to be mixed effectively.

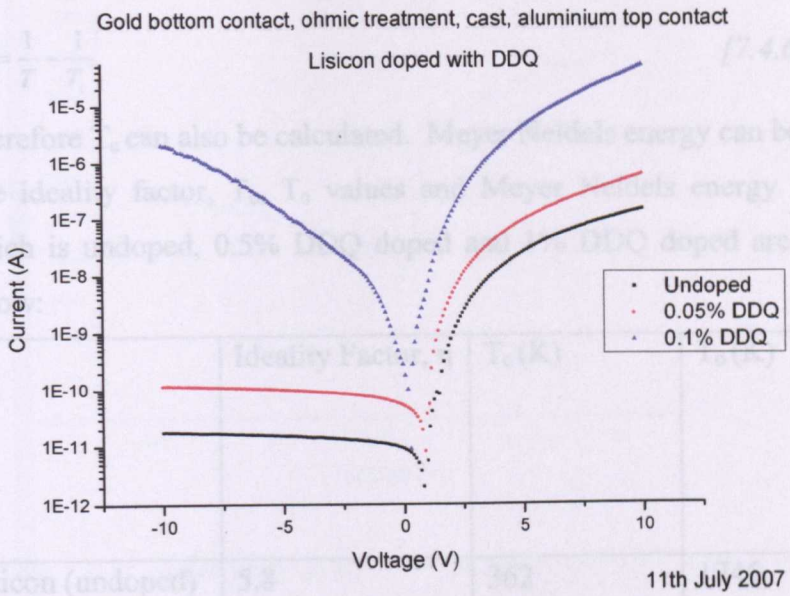


Figure 7.4.1: An I-V plot for a Schottky diode with an area of 4μm², to show the effect of doping polymer with DDQ.

For forward characteristics, the ohmic contact improves, as the level of dopant increases as there is less voltage across the contact and therefore higher levels of injection.

The Ideality Factor, and values for T_c and T_o can be calculated, as shown below:

Current can be expressed by:

$$I = I_o \exp\left(\frac{qV}{\eta kT}\right) \qquad [7.4.1]$$

However:

$$I = I_o \exp\left(\frac{qdV}{kT_o}\right) \qquad [7.4.2]$$

Where I_o is an arbitrary current.

Comparing *equations [7.4.1]* and *[7.4.2]* shows that $T_o = T\eta$ *[7.4.3]*

The value for T_o can be found by using *equation [7.4.2]* and by using two different values for both current and voltage, it can be shown that:

$$(2.3)\log\left(\frac{I_1}{I_2}\right) = \frac{q}{kT_o}\left(V_{app1} - V_{app2}\right) \qquad [7.4.4]$$

$$T_o = \frac{q}{(2.3)k}\frac{\left(V_{app1} - V_{app2}\right)}{\log\left(\frac{I_1}{I_2}\right)} \qquad [7.4.5]$$

Where T_o can be found using *equation [7.4.6]* [5]:

$$\frac{1}{T_o} = \frac{1}{T} - \frac{1}{T_c} \qquad [7.4.6]$$

Therefore T_c can also be calculated. Meyer Neldels energy can be found by kT_c.

The ideality factor, T_c, T_o values and Meyer Neldels energy values for Lisicon which is undoped, 0.5% DDQ doped and 1% DDQ doped are shown in the table below:

	Ideality Factor, η	T_c (K)	T_o (K)	Meyer Neldels Energy (Joules)
Lisicon (undoped)	5.8	362	1745	$5.0*10^{-21}$
Lisicon (0.05% DDQ)	5.5	366	1657	$5.1*10^{-21}$
Lisicon (0.1% DDQ)	3.74	409	1123	$5.6*10^{-21}$

Table 7.4.1: An indication of Ideality Factor, T_c, T_o and Meyer Neldel Energy.

Doping introduces more states which leads to a higher T_c and therefore leads to decreases in the ideality factor. The Meyer Neldel energy also increases, with doping. The values of Meyer Neldel energy obtained suggest the material is extremely disordered.

7.5 The Effect of Polymer in Schottky Diode Fabrication

The polymer used in Schottky diodes, will have an effect on current flow mechanisms and current density.

The graph in *figure 7.5.1* is a current-voltage plot of a Schottky diode fabricated using P3HT.

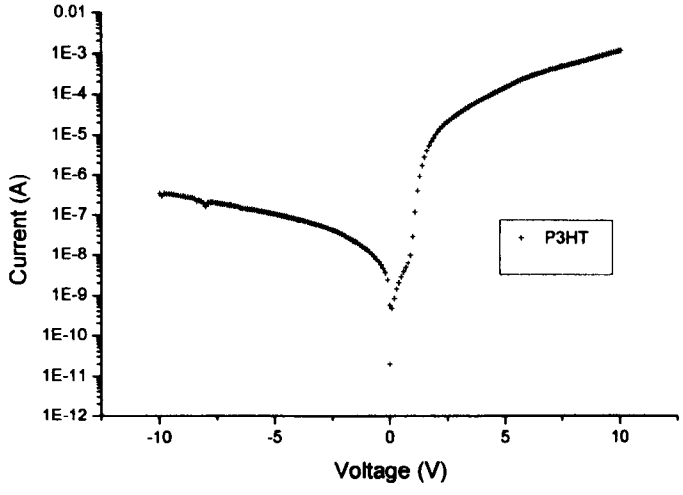


Figure 7.5.1: A Schottky diode fabricated using P3HT, with a contact area of 4μm².

The diagram in *figure 7.5.2*, shows the expected Current-Voltage Graph for a Schottky diode fabricated using P3HT.

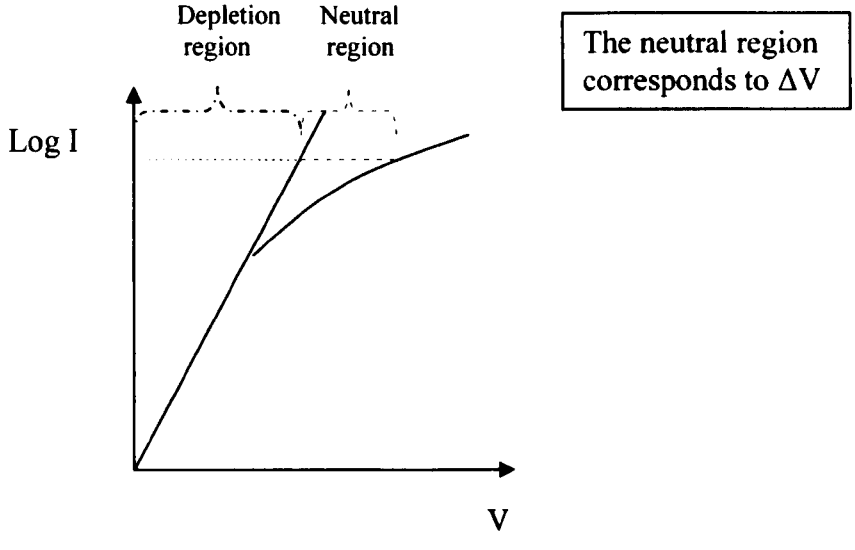


Figure 7.5.2: Current-Voltage graph for a Schottky diode fabricated using P3HT.

The diagram in *figure 7.5.3* shows a schematic for a Schottky diode fabricated using P3HT, the current process is drift. The neutral region, contains an equal number of positive holes and negative acceptors.

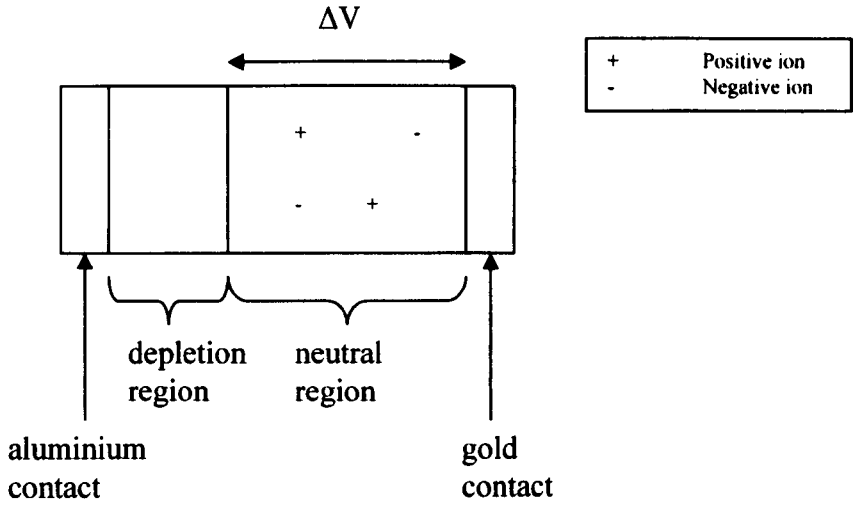


Figure 7.5.3: Schematic of Schottky Diode fabricated using P3HT.

P3HT has a high residual doping level. An equation for current density, when the current mechanism is drift can be derived.

The current density in the neutral region can be expressed as:

$$J = nq\mu F \qquad [7.5.1]$$

Poisson's equation states that:

$$\frac{dF}{dx} = \frac{qn}{\varepsilon\varepsilon_o} \qquad [7.5.2]$$

Rearranging *equation [7.5.2]* and substituting into *equation [7.5.1]* gives:

$$J = \varepsilon\varepsilon_o \frac{dF}{dx}\mu F \qquad [7.5.3]$$

Integration gives:

$$Jx = \mu\varepsilon\varepsilon_o \frac{F^2}{2} \qquad [7.5.4]$$

However $F = \frac{dV}{dx}$, therefore

$$\frac{dV}{dx} = \left(\frac{2Jx}{\mu\varepsilon\varepsilon_o}\right)^{1/2} \qquad [7.5.5]$$

Rearranging and integrating gives:

$$J = \frac{9}{8}\mu\varepsilon\varepsilon_o \frac{V_{app}^2}{x_t^3} \qquad [7.5.6]$$

This relationship is known as the trap-free square law, the Mott-Gurney square law and Child's law for solids [3].

The current density for the space charge limited mechanism can be derived, in a similar manner to that shown for drift current.

The mobility can be defined as $\mu = Kn^m$ using the equation for current density (*equation 7.5.1*), an equation for carrier concentration can be found:

$$n = \left[\frac{J}{qKF}\right]^{1/(m+1)} \qquad [7.5.7]$$

Using Poisson's expression:

$$\frac{dF\varepsilon_o\varepsilon_s}{qdx} = \left[\frac{J}{qKF}\right]^{1/(m+1)} \qquad [7.5.8]$$

If this equation is rearranged and integrated, an equation can be found for field:

$$\left[\frac{qx}{\varepsilon_o\varepsilon_s}\left[\frac{J}{qK}\right]^{1/(m+1)}\frac{2+m}{1+m}\right]^{(1+m)/(2+m)} = F = -\frac{dV}{dx} \qquad [7.5.9]$$

Further integration, results in an equation for current density for space charge limited currents:

$$J = \frac{-V^{(2+m)}}{x^{(3+2m)}}\frac{(3+2m)^{(2+m)}}{(2+m)^{(3+2m)}}\left[\varepsilon_o\varepsilon_s(1+m)\right]^{(1+m)}\left[\frac{K}{q^m}\right] \qquad [7.5.10]$$

An example of a Schottky diode fabricated using PTAA is shown in diagram 7.6.1. The current mechanism for Schottky diodes fabricated using PTAA is space-charge limited, this is displayed in *figure 7.5.3*. Space-charge limited currents occur when the charge concentration on the plates of the contacting metal is smaller than the concentration in the semiconductor. Space-charge is therefore possible in semiconductors that contain very large density of traps in the bandgap or contain charge carriers with a low mobility. The presence of this charge results in a non-linear field rather than the expected ohmic relationship.

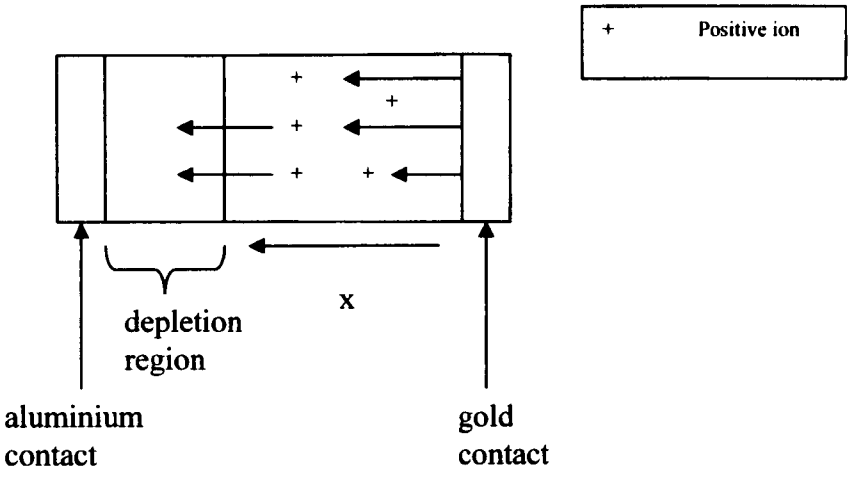


Figure 7.5.3: Schematic of Schottky Diode fabricated using PTAA.

7.6 Hysteresis in a Schottky Diode

The graph in *figure 7.6.1*, shows typical I-V characteristics for a Schottky diode, with hysteresis.

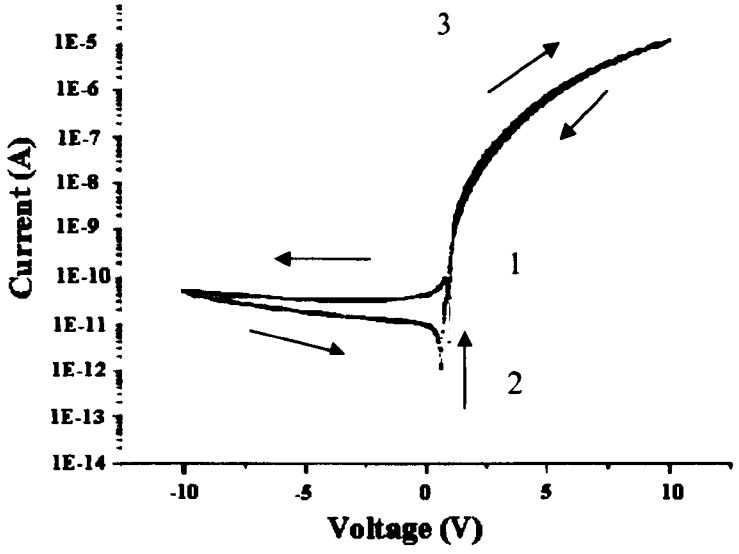


Figure 7.6.1: Typical I-V characteristics for a Schottky diode, fabricated using PTAA and an aluminium top contact of 785nm [4].

It should be remembered that the positive voltage displaced on the x-axis of *figure 7.6.1* corresponds to a negative voltage being applied to the aluminium contact as illustrated in *figure 7.6.2*.

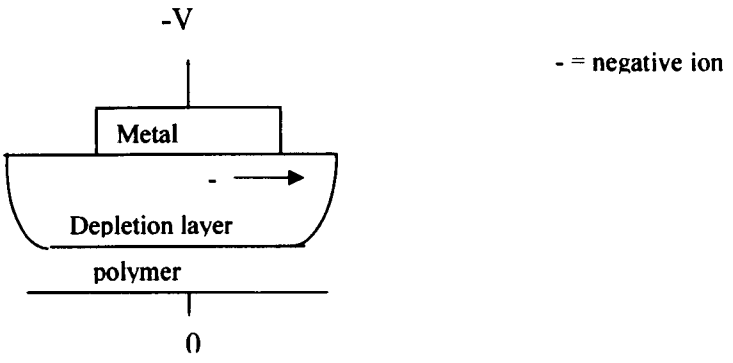


Figure 7.6.2: Diagram showing the effect of applying negative voltage to a Schottky diode.

The graph in *figure 7.6.1*, shows a clockwise hysteresis in the forward bias and an anticlockwise hysteresis in the reverse bias. The process that leads to the creation of hysteresis at low currents in Schottky diodes needs to be examined as this is important for the low power operation of high yield circuits.

If a negative voltage is applied to the polymer, the negative ion species move away from the interference and will accumulate at the edge of the metal, this is shown in *figure 7.6.2*. This accumulation of ions at the edge of the metal is effectively a battery, as it acts as a storage point for ions and the potential drop associated with the image force in the metal gives a field which is associated with the voltage on the battery. It is the accumulation of these negative ions, when the aluminium contact is at its most negative bias that leads to a drop in the current at any given voltage and therefore results in the clockwise hysteresis observed in the forward bias.

The dip at point 1, in *figure 7.6.1*, occurs at a negative voltage, the region is heavily doped and this leads to the narrowing of the depletion region. When the depletion region becomes very narrow (when there is 0V applied or very small voltages), there is an electron tunnel current, which draws in holes from the p-type polymer as shown in *figure 7.6.3*. This is equivalent to holes tunnelling into the metal.

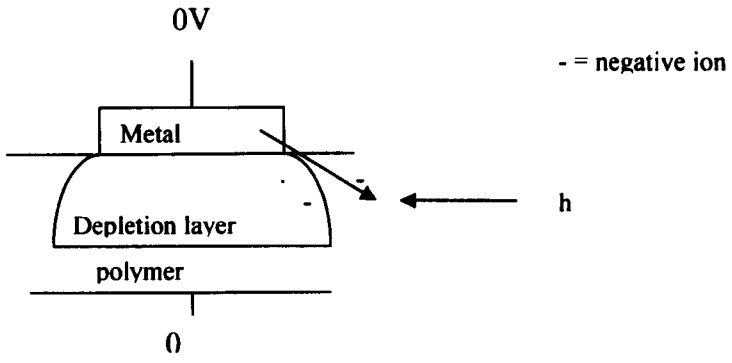


Figure 7.6.3: Diagram showing the effect of applying negative voltage to a Schottky diode.

At point 2 in *figure 7.6.1*, there is 0V, this is the charge storage base. The diode has recovered by point 3, in *figure 7.6.1*.

When a positive bias is applied to the metal, the depletion region is widened and acceptors drift towards the top (positive contact), as shown in *figure 7.6.4*. The combination of these actions leads to the lowering of the dopant concentration in the polymer and there is therefore a rapid expansion until it meets the back of the polymer. The current and the field at the interface remain relatively constant. However after prolonged exposure to a positive bias on the metal, the acceptor concentration is drastically reduced and this lowers the potential and hence creates the anticlockwise hysteresis observed in *figure 7.6.1*, for the reverse characteristics.

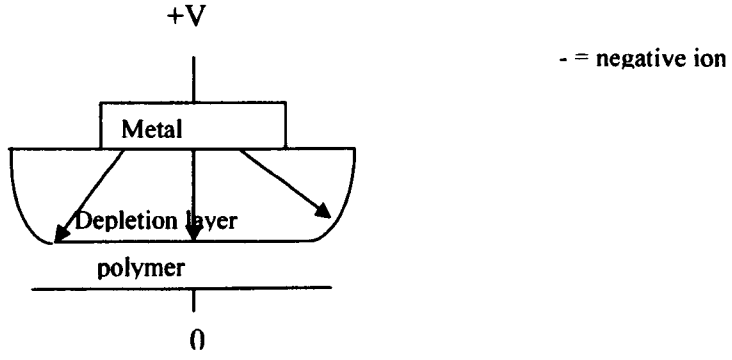


Figure 7.6.4: Diagram showing the effect of applying positive voltage to a Schottky diode.

7.7 Conclusion

The fabrication and typical characteristics of Schottky diodes have been examined. It has been shown that doping increases the number of states, which results in a higher value of T_c and therefore a decrease in the ideality factor. The Meyer Neldel Energy also increases with doping.

Drift, the current mechanism for Schottky diodes fabricated using P3HT has been examined, as has space charge limited current, the mechanism for diodes fabricated using PTAA.

7.8 References

[1] W. Schottky, *Naturwissenschaften* **26**, 843 (1938).

[2] W. Meyer and H. Neldel, *Z. Techn. Phys* **12**, 588 (1937).

[3] M.A. Lampert and P. Mark, *Current Injection in Solids*, (Academic Press, New York, 1970).

[4] S. Prior, private communication.

[5] D. Donaghy, M. Raja, S. Badriya, S.J. Higgins and W. Eccleston, *Journal of Non-Crystalline Solids*, **352**, 1641 (2006).

Chapter 8

The Technical Roadmapping of Organic Electronics

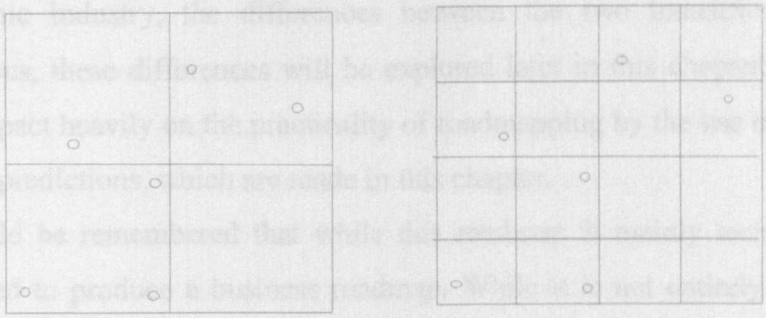
As organic electronics grows into an industry having a roadmap becomes increasingly important. This is because it is essential for equipment manufacturers and semiconductor technologists to plan targets for the future.

This chapter discusses organic electronics on the world scene. It goes on to discuss the different parameters which will have an impact on the roadmap. A roadmap for both the UK and Western Europe has been developed.

8.1 Introduction

Organic electronics is growing quickly into an industry, and as with silicon it is becoming important to have a roadmap. The aim of a roadmap is to allow equipment manufacturers and semiconductor technologists to plan targets for the future. This ensures that the equipment is available when it is needed and that new products become available as older markets decline. This usually involves adding functionality to the existing product to entice customers to change and buy the new products.

In electronics this process has been largely based on the scaling down of the feature size of integrated components. The main reason that this is important is that the yield of working circuits is increased, when there are a fixed number of defects on a substrate as shown in *figure 8.1.1*. In *figure 8.1.1(a)* a substrate with several defects is shown, it is clear that there is only one working circuit so the cost of this circuit is that of producing a process for the entire substrate. If the minimum feature size is reduced by a factor 2, there are ten working circuits so the cost of each is reduced by 90%, as shown in *figure 8.1.1(b)*.



(a) 1 working chip
Cost of chip 1 euro cent

(b) 10 working chips
Cost of chip 0.1 euro cent

Figure 8.1.1: An example of the benefits of scaling in terms of production.

Fabrication cleanliness has also led to an increase to the yield of working circuits in silicon. It should be remembered that if the findings for earlier microelectronic technology follow through, that the development time is always longer than expected from the roadmap. This is as a consequence of only a limited number of technological problems being foreseen. The second finding is that once the

technology has been established the size of the market is almost always larger than expected, this is a result of the lack of our imagination. To be accurate, roadmapping needs to be developed based on both devices and circuits.

It should also be remembered that there is no fully accepted theoretical foundation for understanding electrical conduction in organics, it is therefore necessary for this knowledge to grow rapidly, as it is essential for reliable devices, circuits and later business systems and business models to be built.

The roadmap for organic electronics has been based on the roadmapping for silicon which is based on Moore's Law.

Moore's Law is attributed to Gordon E. Moore who is the co-founder of Intel, it is an empirical observation made in 1965, that the number of transistors on an integrated circuit for minimum component cost doubles every 24 months. While the prediction still holds, it is now felt that a better approximation is that the number of transistors on an integrated circuit for minimum component cost doubles every 18 months. It has been assumed that the organic electronic industry will perform in accordance to Moore's Law. This however may not produce an accurate roadmap, as although there are many similarities between silicon technology and the developing organic electronic industry, the differences between the two industries are at least as numerous, these differences will be explored later in this chapter. The differences will impact heavily on the practicality of roadmapping by the use of silicon as a base for the predictions, which are made in this chapter.

It should be remembered that while this roadmap is mainly technical, it could be extended to produce a business roadmap. While it is not entirely logical to have a roadmap which is UK based, rather than based on a European or Global scale, the statistics for the population and market size are well established in the UK and it is likely that the UK market reflects that which would be seen in Europe, and so can easily be expanded.

8.2 World Scene

Organic electronics depends partially on the extent to which the Liquid Crystal Display (LCD), can be undercut in price, which is therefore related to the potential for reducing the price of LCD. There is also the potential for a price war, as there are extensive plans and investments in South Korea, to win a much higher fraction of the world's markets in LCDs. Potentially a situation could be created where the price of

LCD falls rapidly, this will mean that organic technology could be squeezed out of this area, as it is unlikely there will be space for a new and potentially disruptive technology. This would imply that there would at least initially be a lack of market drive, there is however an alternative view, which is that European companies will have developed a low-cost disruptive technology. It is also important to remember that the East Asian industries have not totally ignored organic industries. [1]

There are also many areas of application which will not be in direct competition with LCD's, these include active wallpaper and e-paper. The advantages of active wallpaper will be that a person can program designs of their choice for their wallpaper and change the design whenever they desire. While E-paper will enable the downloading of contents of newspapers and magazines, as the move away from hard copies of items continues to take place to help preserve our environment and reduce our carbon footprint, this is likely to become increasingly used.

Displays have a relatively high unit cost and therefore their turn-over will be relatively large. The volume of auto-id units, the most commonly talked of example of which is tags, is likely to be far larger, however these will tend to be far cheaper units and therefore the turnover will be much less.

It is in the area of auto id/rf tags, for example, the replacement of the barcode, that it is believed that organic electronics to be potentially disruptive, this chapter will go on to examine this in more detail. The rf tag business is a rapidly developing area in the USA and it is felt that this will spread to Western Europe.

Potential applications will be discussed, in a later section; however there are two distinct but large areas of auto-id which occur within the general heading of retail. One is the tagging of cartons and or palates at the warehouse level. At the moment this is based on barcodes and is called 'Slap and Ship', the second is single item tagging which is far more difficult but if achieved will supersede 'slap and ship' with more expensive silicon tags. It is however difficult to predict when this will occur, the main problem is that of collision and the need to generate a number of similarly exacting functions in organic electronics. Collision occurs when the signals from multiple identical packages are mixed.

8.3 The Impact of Scaling on the Roadmap

Silicon represents the only example of a successful quantitative roadmap, in the absence of equivalent numbers for organics; the numbers for silicon are used, to obtain the growth in component count and the increase in functionality.

A large proportion of the success of silicon roadmapping is as a result of the MOSFET transistor for which scaling factors and rules are at best roughly obeyed [1]. Scaling has an amazing effect on the rate at which the total number of gates on a chip can be increased year by year: it leads to Moore's Law. For silicon after each scaling there follows an increase in both functionality and performance, which the consumer was and is ready to accept, an example of this is the Pentium chip.

Moore's Law leads to the use of less accurate business models being cut-out, as it simply dictates the maximum number of transistors that will be included on a chip in a particular year. It should however be remembered that one of the reasons Moore's Law is perceived as being accurate, is that it is represented graphically on a log-linear plot. However as long as it is believed it highlights the needs for higher performance manufacturing equipment to specifications defined well in advance. It also acts to warn package manufacturers of coming demands and allows system and component designers to be warned of the coming improvements in performance and changes in cost.

Moore's Law states the number of transistors which make up a chip at various points of time, this very roughly defines the level of functionality, it is then possible to determine the growth of the market which will be based on the sizes of the population and the nature of the products. Moore's Law can be approximated over forty years by assuming that the number of transistors doubles every eighteen months. One of the reasons for this is a consequence of improved cleanliness, and the remainder is the result of scaling. The effect of fabrication cleanliness is measured by the rise in the amount of active area, whereas the increase in functionality is measured by the increase in the number of components.

The component count is known over the forty year period starting in 1967 to have risen from 10 to 10^9. *Figure 8.3.1* shows how the component count changes with time.

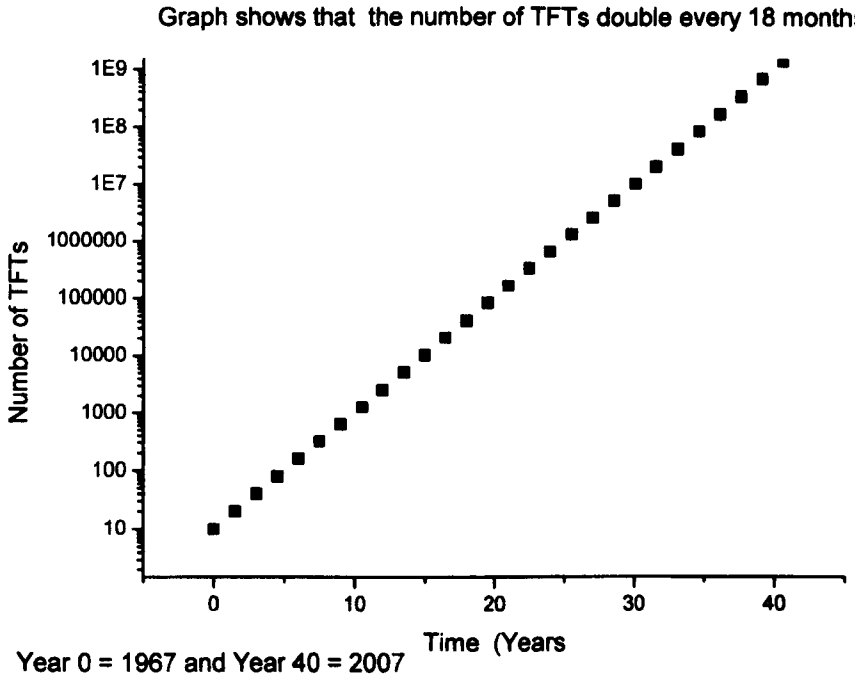


Figure 8.3.1: Changes in Component Count with Time.

There are however complications of applying Moore's Law, or a form of it, to organics. These complications include [1]:

- The technology must have well-defined scaling rules.
- The basic device physics for organics is felt to be significantly different from silicon, so it is necessary to understand whether various approximations used with single devices are applicable, for example how controlled is off-current, in Schottky diodes and TFTs.
- It will also become apparent that the following list of essentials is less than complete:
    1. modified accurate equations should be available from which we can deduce scaling rules.
    2. source and drain contacts should be, to a high degree, ohmic. Since they are usually imperfect, there will be depletion regions which lower the real channel length. This affects scaling.
    3. the range of potential products resulting from it should be large: the technology should be ubiquitous.

Scaling provides good management tools, it impacts on unit cost, margins, system performance and running cost.

The primary quantity involved in scaling is the minimum feature size, which is described later.

8.4 Silicon and Organic Technology

As previously stated, the basic device physics, given our present level of understanding is significantly different from silicon, it is therefore felt that various approximations made using single crystal devices, may not be applicable. Examples of these approximations include: can abrupt depletion layer edges be assumed for all material systems, does Einstein's Relation apply, how controlled is off-current and what is the consequence of the dependence of mobility on carrier concentration?

8.5 An Expression for Moore's Law

Moore's Law supplies the constant which the number of transistors in a chip are multiplied by, to give the total number of transistors in a chip at a specific time. It does not provide an exact figure but rather an estimation that is used in roadmapping applications.

It can be represented by:

$$\frac{dD}{dt} = BD \qquad 8.5.1$$

so that

$$D = D_o \exp(Bt) \qquad 8.5.2$$

where D is the density of transistors, t is the time, B is the business constant and D_o is a constant that depends on the point of time chosen as zero.

It should however be remembered, that as described in a later section of this chapter, there usually was a market that was ready to absorb improvements in the minimum feature size and as a consequence of this the business constant became fixed by the technology, however there is no guarantee that this will hold true for organics.

8.6 Minimum Feature Size

The minimum feature size λ is the length of the shortest line that can be reproduced on a substrate. Minimum feature is defined by both the print method and device physics. It should be remembered that the minimum feature size is not necessarily equal to the distance between the source and drain of the smallest transistor, because this is dependent on physics manufacture, material and the mode of operation of the device and is therefore usually longer. The minimum feature size has reduced from 15μm to approximately 65nm, over the past forty years.

It can be assumed that: $\delta\lambda \propto \lambda$ *8.6.1* and $\frac{\delta\lambda}{dt} \propto \lambda$ *8.6.2*

This is because at the beginning reductions are relatively large, however while its relatively easy to reduce the minimum feature size at the beginning, as time goes on it is more difficult to sustain a linear rate of reduction.

Where λ is the minimum feature size, t is the time and k is a constant.

Therefore: $-\int_{\lambda}^{\lambda_o} \frac{d\lambda}{\lambda} = kt$ *8.6.3*

Integrating between the limits gives: $Log_e \frac{\lambda}{\lambda_o} = -kt$ *8.6.4*

This can be rearranged to give: $\frac{\lambda}{\lambda_o} = \exp(-kt)$ *8.6.5*

Therefore $\lambda = \lambda_o \exp(-kt)$ *8.6.6*

where k can be approximated to be $4.33ns^{-1}$.

The relationship between minimum feature size and time, is shown in *figure 8.6.1*.

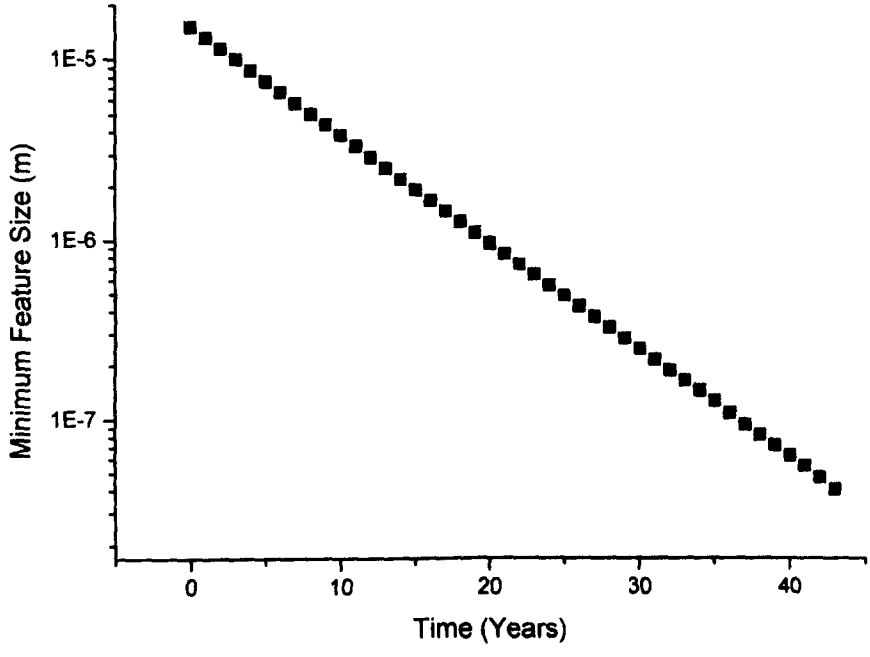


Figure 8.6.1: Relationship between minimum feature size and time, for silicon devices.

8.7 A TFT Equation for Disordered Organics

In organics, carrier mobility changes with carrier density, therefore one question that needs to be answered is whether the current below pinch-off scales with 1/L, where L is the channel length. It has been shown that the intrinsic dopant concentration can be lowered to about $10^{16}cm^{-3}$ [1], that the carrier concentration in the body of a film controls the body carrier mobility, and much the same relationship exists at the interface.

Conduction in organic semiconductors is a result of variable range hopping of carriers through traps which have a density that depends on the proximity of segments to adjacent segments of polymer chain. The wavelength and hence the energy of the carrier is determined by the length of these segments. If the energy levels are assumed to have a Gaussian distribution, then the energy levels can be approximated to an exponential function which allows the replacement of the temperature T in many of the equivalent equations used in silicon by T_c the characteristic temperature of the distribution of states. T_0 characterises the carrier distribution in the same way and incorporates both T and T_c. The carrier mobility μ depends on the integrated carrier density and can be expressed by:

$$\mu = Kn^m \qquad 8.7.1$$

where:

$$m = \frac{T_c}{T} - 1 \qquad 8.7.2$$

Equation 8.7.1 is similar to the University Mobility Law. The Universal Mobility Law relates mobility to the number of carriers introduced by dopant and is described in detail in chapter 2. The introduction of dopant leads to increases in both the trap and carrier density, but *equation 8.7.3* is still obeyed. K, T_c and T_0 are substantially different to the values obtained from adding carriers without attendant doping molecules. The mode of conduction along a channel of an accumulated channel at high currents is drift: as with silicon. It is also drift in the sub-threshold region, unlike silicon where diffusion is dominant. In order to demonstrate this it is assumed diffusion is dominant, the validity of Einstein's Relationship is also assumed [1]:

$$J = qD\frac{dn}{dx} = \left(\frac{q\mu kT_o}{q}\right)\left(\frac{n(0)}{L}\right) = q\mu n(0)\left(\frac{kT_o}{L}\right) \qquad 8.7.3$$

Where L is the channel length, n(0) is the carrier density at the source end of the channel, kT_o/q is approximately 100mV from measurements that have been made on

capacitors, it is also an equivalent drain voltage. Above this threshold voltage (100mV) the current is controlled by drift, this is well below the threshold of a circuit driver transistor and has little significance in circuits, it can therefore be assumed that current flow is by drift alone. With this assumption and *equation 8.7.3*, an equation has been developed for the drift-current voltage characteristics, which has a good chance of covering the full range of current I_{unsat} seen in a typical device [1]:

$$I_{unsat} = \frac{KC_D^{(2m+1)}W}{(2\varepsilon_o\varepsilon_p kT)^m L}\left[\frac{V_{g'}^{2(m+1)} - (V_{g'} - V_d)^{2(m+1)}}{(2m+1)2(m+1)}\right] \qquad 8.7.4$$

and for the effective carrier mobility in saturation:

$$\mu_{sat} = \frac{KC_D^{2m}}{(2\varepsilon_o\varepsilon_p kT)^m}\left[\frac{V_{g'}^{2m}}{(2m+1)(m+1)}\right] \qquad 8.7.5$$

K is a constant, C_D is the geometric capacitance per unit area of the gate, $V_{g'}$ is the gate minus the threshold voltage V_t, ε_o is the permittivity of free space and k is the Boltzmann's constant. It should be remembered that the relative permittivity of the polymer is used, this equation is not suitable for use with pentacene.

8.8 Thickness of the Organic Layer

For organic transistors the thickness of the organic layer is important because the source and drain contacts are ohmic and off-current falls with decreasing thickness. There is a thickness below which there is a substantial fall in the field effect mobility, it is believed that this is related to the Debye length of the surface accumulation layer [1]. Where the off-current is a strong function of gate voltage, it is controlled by the interface rather than the body, the off-current can therefore be defined as the lowest measured current. This is usually attributable to the body effects. The Debye length which has previously been defined, is assumed to be the thickness of an accumulation layer.

8.9 Gate Dielectric and Over-Scaling

It is important to determine whether the gate dielectric scales with thickness and whether over-scaling is a useful feature in the context of organics. It is necessary for there to be a continuous reduction of gate dielectric thickness, with single crystal semiconductors. The depletion regions at the source and drain are reduced because of the need to reduce the punch-through in inversion devices. The reduction to

depletion regions, is achieved by increasing the dopant concentration in the substrate, this however increases the threshold voltage, which leads to an increase in both the power supply voltage and dissipation, however the threshold voltage may then be reduced by thinning the gate dielectric. The principal of over-scaling is used to enable an additional reduction in the supply voltage, this can be achieved by reducing the dielectric by more than would be required by the increased concentration of dopant. This in effect trades dissipation for the increased speed that has resulted from the reduction of feature size. Dielectric thickness is commonly defined as the geometric thickness divided by the relative permittivity, where a high relative permittivity reduces the effective thickness of the gate dielectric below the geometric thickness, however the electric breakdown which is found with thin dielectrics does not occur. This breakdown is usually associated with particles deposited during processing, rather than being intrinsic.

The accumulation mode of TFTs with ohmic contacts, ideally means that there are no depletion regions around the source and drain, metallic contacts reduce the possibility of punch-through. If the gate dielectric thickness is scaled by comparison, with silicon, it can be regarded as being over-scaled and is carried out in order to increase the drive capability of the TFT. This occurs through the reduction of threshold V_t and the increase in the slope of the transfer characteristic.

The simple application of the continuity of dielectric displacement across the interface between the gate material and the organic semiconductor, can be used to find the intrinsic threshold voltage, V_t:

$$V_t = \left(\frac{x_d \varepsilon_p}{\varepsilon_d}\right) F_{IT} + \phi_s \qquad 8.9.1$$

where F_{IT} is the field just within the organic material at whatever carrier density is needed to reach the defined threshold. It is assumed that the charge in the channel is proportional to F_{IT} and hence F_T can be calculated by Gauss's Law. *Equation 8.9.1* does not include the effect of work function differences and fixed charge associated with the dielectric. For organic transistors, the surface potential $\phi_s << V_t$ and V_t decreases with increasing ε_d (dielectric permittivity) and with decreasing gate dielectric thickness (x_d). It should however be remembered that increasing the relative permittivity of the gate reduces the mobility [3].

8.10 The Concept of Active Area

In the discussion in the Introduction section of this chapter, it has been assumed that the entire area is covered with transistors, but they are usually well spaced, this leads to the active area concept. The active area is defined as the total region subject to high electrical stress and/or where large current densities flow. Thus, for Thin Film Transistors (TFTs), the active area is usually defined as being the combined area of the channel added to that associated with the overlaps of the gate with source and drain. The active area is illustrated by *figure 8.10.1*. The capacity to reduce the channel length is at the heart of Moore's Law. There are two major factors, the first is a requirement to be able to physically reduce the channel length from the multi-micron to the sub-micron level. The second is that the physics of the material and the device should allow it. For example most TFTs are not ideal in that most real devices do not have precisely defined source and drain edges.

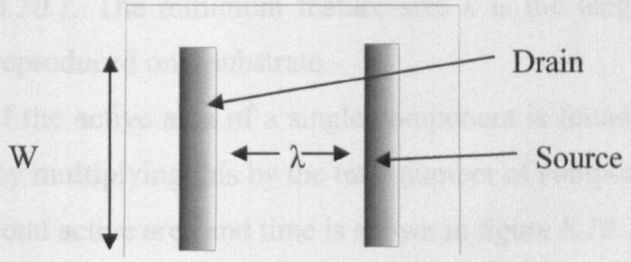


Figure 8.10.1: Illustration of Active Area.

The arguments in the Introduction, still apply but the area will be reduced to a fraction of its original size. The reduction of TFT active area is important and the factors which prevent scaling down the TFT need to be considered. With devices that have pn junctions as source and drain there is a strong possibility of punch through of drain to source, where the depletion region overlaps that of the source, it gives a high channel current, which cannot be controlled by the gate. Ideally there should be no depletion regions for ideal ohmic contacts so this effect will be reduced. Transconductance g_m is defined as the ratio between the output current and input voltage. A result of this is that the role of dopant is changed and gate thickness reduction is thus no longer required, however reducing the gate thickness also increases the g_m of the device, which is of great importance on output devices. Within the circuit the added g_m is almost exactly negated by the increase of load

capacitance of adjacent TFTs. The edge definition of source and drain contacts are very important since they are likely to lead to a fluctuation of channel length and a variation of parameters between devices, which may be more important than the minimum feature size.

To calculate the active area, it is assumed that the minimum feature size is equal to the alignment error. It is also assumed that the driver has an aspect ratio of 1000; the load has an aspect ratio of 1/10 of the driver, thus it is assumed that the aspect ratio is 1000. The aspect ratio is given by:

Aspect Ratio = W/L *8.10.1*

Where L is the minimum feature size.

The total active area can be found by combining the active area of a single component, with the component count. The active area can be considered to include the area of the source and drain and that associated with the channel, therefore the active area of a single component can be found by $(\lambda+\lambda+\lambda)*A$, as shown in *figure 8.10.1.* The minimum feature size λ is the length of the shortest line that can be reproduced on a substrate.

If the active area of a single component is found, the total active area can be found by multiplying this by the total number of components. The relationship between the total active area and time is shown in *figure 8.10.2.*

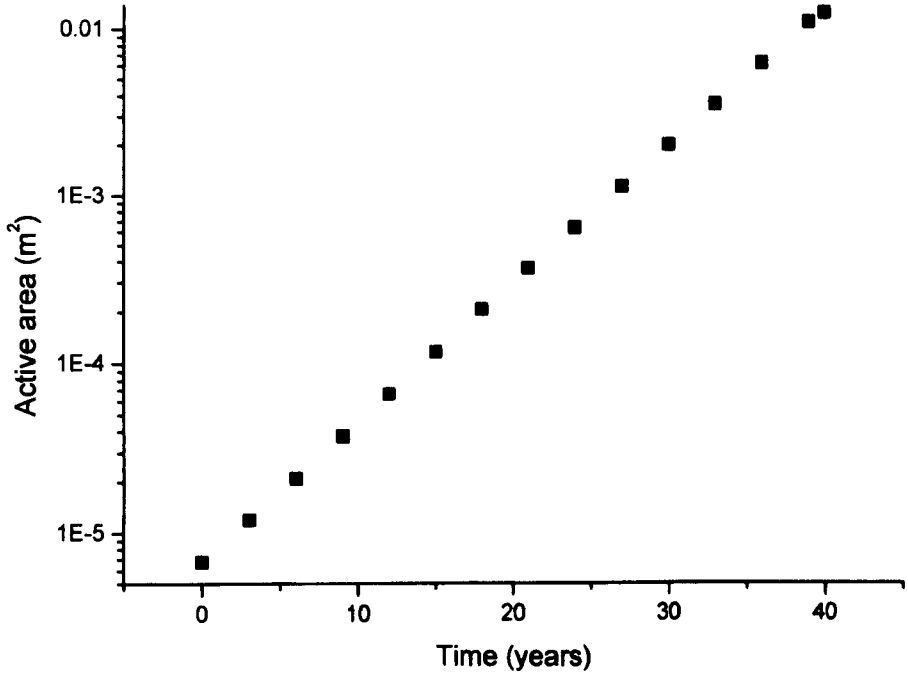


Figure 8.10.2: Relationship between total active area and time.

8.11 Functionality

A commonly discussed application of organic electronics is to replace the bar-code with rf activated tags. Collision is the name given to the problem of finding how many identical products are in a basket. This target is ambitious as it must include anti-collision circuitry. Anti-collision circuitry is important as it allows identical tags to be detected individually. In relationship to profitability this is a problem since to be cost effective it must enable the removal of check-outs, the tag must also cost less than the lowest priced item. An alternative route is therefore to improve security by reducing the loss of items by theft either in transit or from the shelves[4]. This involves single item tagging, it is felt that this would undercut existing security systems without drastically reducing margins. The tag would be killed at the check out or by the sale assistant. A 'sleep' tag would give more functionality as returnable items for example clothes, would use a sleep facility, so that the tag could be reactivated on return of the goods and subsequent placement in the sales areas. Such functionality would involve non-volatile memory. A third level of functionality would involve the kill, sleep and some stock data and a fourth would include the full barcode replacement including anti-collision. Anti-collision is important, so that if more than one 'identical' item is bought, the number of items can be detected and appropriately charged for. All these are shown in *figure 8.11.1*, exponential growth is apparent, the bar-code replacement being sometime in the distance future, largely because of the very high component count, that is required, the logic is that the benefits of greatly improved security would off set the loss of margins on lower priced items. The kill tag is represented by A in diagram 8.11.1, the sleep tag by B, the third level of functionality by C and the fourth (full barcode replacement) by D.

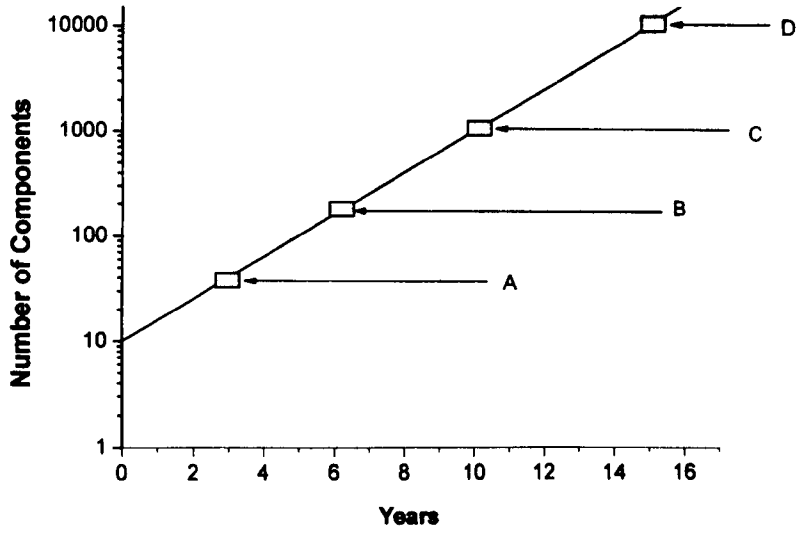


Figure 8.11.1: The timescale for emergence of tags with higher functionality. The prediction is based on estimates of component counts.

8.12 Potential Applications

The initial application is felt likely to be security tags on high priced items such as clothes, alcoholic beverages and tobacco, these tags would be killed once the item had been through checkout.

The second application would involve the sleep function, so that if an item is returned, the tag can be 'woken-up' and the item can be placed back on the shelf, this will particularly useful for items such as clothes.

The third application will include the kill function, the sleep function and some stock data, it is anticipated that at this stage the tag will be on all clothes, alcohol, tobacco, toiletries, food and beverages.

The fourth application will include all of the above functions and anti-collision functionality and replace the need for cashier operated tills.

Silicon based RFID tags are used in the following areas: drugs, other healthcare applications, retail apparel, consumer goods, tires, postal, books, manufacturing parts and tools, archiving (documents, samples), military, pallet/case, smart cards/payment key fobs, smart tickets/banknotes/secure docs, air baggage, conveyances/other freight, animals, vehicles, people, car clickers and passport pages[5], it is anticipated that the organic rf tag will provide a cheaper alternative and therefore move into these areas.

As well as potentially saving money, by replacing person operated tills and improving security, they will also improve the speed at which stock is replaced on supermarket shelves and where fresh food is involved, tracking products will help to avoid waste.

However consumers may be reluctant 'to allow' items to be tagged which may slow growth in this area, as privacy campaigners are beginning to express concerns, that items could be 'seen' in your possession. This is a particular concern for such campaigners as potentially anyone from burglars to the government, could tell what a person has bought, where from and how much they paid for it and potentially the name of the person who bought the item.[6]

8.13 Potential Market Size

The table below shows the items that will be tagged in each stage of functionality.

Functionality 1	Functionality 2	Functionality 3	Functionality 4
Clothes*	Clothes (except underwear)	Clothes	Clothes
Children's toy*	Children's toy*	Children's toy	Children's toy
Alcohol*		Alcohol	Alcohol
DVD (rental and sale)	DVD (rental and sale)	DVD (rental and sales)	DVD (sales)
Tobacco		Tobacco	Tobacco
Videos	Videos	Videos	Videos
Computer software	Computer software	Computer software	Computer software
Computer hardware	Computer hardware	Computer hardware	Computer hardware
Other electronic goods	Other electronic goods	Other electronic goods	Other electronic goods
Perfume		Perfume	Perfume
Make-up		Make-up	Make-up
Footwear	Footwear	Footwear	Footwear
Nursery + baby goods	Nursery + baby goods (excluding dummies etc)	Nursery + baby goods	Nursery + baby goods
Sports merchandise e.g. squash racquets	Sports merchandise	Sports merchandise	Sports merchandise
Camping Equipment		Camping Equipment	Camping Equipment
Photographic equipment	Photographic equipment	Photographic equipment	Photographic equipment
Luggage	Luggage	Luggage	Luggage
household goods* e.g. bed linen, pictures	Household goods	Household goods	Household goods
DIY tools and goods*	DIY tools and goods*	DIY tools and goods	DIY tools and goods
		Food	Food
		Non-alcoholic beverages	Non-alcoholic beverages
		Toiletries	Toiletries
		Magazines	Magazines
		Newspapers	Newspapers

* indicates that the high price range end of the market only will be tagged

Figure 8.13.1: Table of potential applications.

8.14 Potential Market Size Broken Down

8.14.1 Supermarkets

Supermarkets are a huge business, on the 17th April 2007, The Independent Newspaper reported that, the chief executive of Tesco was about to unveil expected annual sales of £42.7bn, which is larger than the GDP of Peru [7]. It should also be remembered that Tesco is not the only supermarket chain in the UK; in fact it only has approximately 30.6% of the total supermarket share [8].

There are approximately 5 billion trips to supermarkets in the UK per year [9]. There are statistics which show these shopping trips by basket size, using these figures and taking the median from the range [10], it can be estimated that there are 80.182 billion items bought in supermarkets per year. Sainsbury has carried out research to breakdown the UK weekly trolley into categories [11]. The categories were:

- Fruit, vegetables and salad
- Cupboard items
- Dairy
- Ready/prepared meals
- Meat
- Drinks – hot and cold
- Crisps and biscuits
- Breads/bakery
- Cakes and Desserts
- Fish
- Alcohol

It was assumed that all food in the dairy, ready/prepared meals, meat and fish categories would be stored in the fridge or freezer. Only 2.5% of the percentage share of the trolley fell into the cakes and desserts section, as not all items in this category would be stored in the fridge or freezer, this category was not included with those that would be stored in the fridge or freezer. Therefore, the total percentage of supermarket items sold per annum in the UK that need be stored in the fridge or freezer can be found to be 31.9% [11]. Therefore in the UK per annum there are 25.6 billion items sold which need to be stored in the fridge or freezer sections of supermarkets.

Alcoholic items, which are relatively high cost items, account for 2% of the average basket. [11]

When using these figure to estimate the number of tags needed it should however be remembered that, it is assumed that there is no loss in transit, by theft and no items are disposed of without being sold for example because they have reached their sell by date.

No estimation was made to include smaller or corner shops, the effect this type of shop would have on the market for tags is however felt to be negligible, as the majority of these shops have only one person working for them and are therefore unlikely to have the profit margins necessary to use rf tags. It should also be remembered, as more and more supermarkets appear on our doorsteps, offering goods at prices that corner or smaller shops cannot compete with the number of these smaller shops is drastically reducing.

8.14.2 DVDs and Videos

In figures based on the year 2005/2006, 222 million DVDs and videos were sold per year; while in the same time period 137 million DVD's and videos were rented. [12]

8.14.3 Tobacco

The number of packets of tobacco which are bought in the average year was also estimated. The following assumptions were made:

- All cigarettes were bought in packs of 20
- No tobacco was sold
- Less than 1% of the male population smoke 1 cigar per week and an insignificant number of women, so this figure was not included [13]
- Underage smokers were not included.
- People on holiday or on business trips to the UK were not included.

The number of packs of cigarettes bought can be calculated using the above assumptions, statistics on the number of smokers in the population and the number of cigarettes that they smoked. The calculations shows that the UK population bought 8.21321 million packs of cigarettes in the year 2004, given the assumptions above it is likely that this is an underestimate. [13,14]

It is however expected that with smoking bans coming into place across the UK in enclosed public areas and work places; and with the NHS increasingly advertising against smoking that this figure will drastically decrease.

8.14.4 Books

The number of books sold in the UK, were also investigated, 348 million books were bought by people aged between 12 and 74, in addition to atlases and maps bought by people outside this age range. This figure does exclude books bought for organisations, for example universities, libraries and companies [15].

8.14.5 Computers

According to the Independent on Sunday newspaper up to 8 million computers are sold every year and in the 18 months, previous to the 10th June 2007, 1.8 million wi-fi terminals had been sold. [16] While 65 million printer cartridges are sold in a year. [17]

8.14.6 Prescriptions Dispensed

An idea of the vast market that is available for tags in the pharmaceutical industry can be shown by the fact 686 million prescriptions were dispensed in the UK in 2004. [18]

8.14.7 Televisions, VCR's and DVD Players

The Retail Pocket Book 2004, contains percentages of the number of working televisions per household and the age of the T.V. sets, from this it can be worked out that there were 7.455482 million televisions bought between April 2002 and March 2003, over the same time period it can be calculated that 3.550455 million VCR's were bought and 1.788174 million DVD players were bought. [19]

8.14.8 Clothes

It is possible to make a rough estimation the adult clothes market, if the following assumptions are made:

- The average cost of unworn clothes is equal to the average cost of all clothes bought
- The average cost of clothing was approximately the same in 2003 and 2006

It was calculated that the total number of women's clothing items bought was approximately 615 million items and the total number of men's clothing items bought was approximately 383 million items.[19,20]

The total market for children's clothes was also estimated, the following assumption was made:

- The average cost of clothing was approximately the same in 2003 and 2006

It was therefore estimated that the total number of children's clothing items bought was approximately 646 million [19,21].

8.14.9 Baggage Transported by Airlines

Airlines transport approximately two billion bags per year [22]. There is also a relatively high ratio of luggage going missing, across the worlds 24 largest airlines approximately 5.6 million bags went missing in a year. This is an average of 15.7 bags per 1,000 travellers, while in 2006 for every 1000 British Airway passengers, 23 bags went missing. [23]

This area is another potential market for organic technology, however it is perhaps likely at least for the near future this market will be taken by silicon technology; as this technology already exists and the additional potential costs are not huge when compared with price of an airline ticket.

8.14.10 Summary of Potential Market Size

The potential market for different items is summarised in the table below.

Item	Potential market (items sold per year)	Year figures based on
Adult's Clothes	998 million	2003
Children's Clothes	646 million	2003
Alcohol (sold in supermarkets)	1.60364 Billion	
DVD and video (sales)	222 million	2005/2006
Tobacco	8.213231 million packs of cigarettes per year	2004
DVD and video (rental)	137 million	2005/2006
Computers	Up to 8 million	
Printer Cartridge	65 million	2006
Televisions	7.455482 million	2002/2003
VCRs	3.550455 million	2002/2003
DVD players	1.788174 million	2002/2003
Baggage Airlines Transport	two billion bags	2007
Pharmaceutical Items (prescriptions dispensed)	686 million	2004
Books (sold)	Over 348 million	2005
Supermarket purchases	80.182 billion	2003

Figure 8.14.1: Table of the Potential Market Areas

8.15 Determining Market Growth for Products Obeying Moore's Law

The diagram below shows the cost per component of the rfid tag. This is based on the assumption that every time the minimum feature size is reduced by a factor of 2; the cost is reduced by 90%. It should be remembered that the effect of fabrication cleaning has not been included in this estimation. It has been assumed that in 2007 the cost of producing 1 component is 1 Eurocent and that the kill tag will be on the market by 2010.

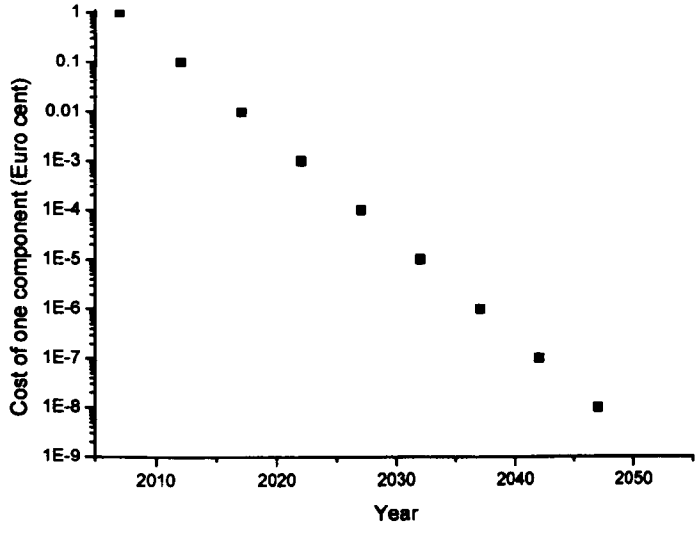


Figure 8.15.1: The variation in the cost of a single component with time.

Figure 8.15.2, shows the cost of various tags at various points in time. It should be remembered that as extra functionality is added more components are needed; which may cause increases in cost.

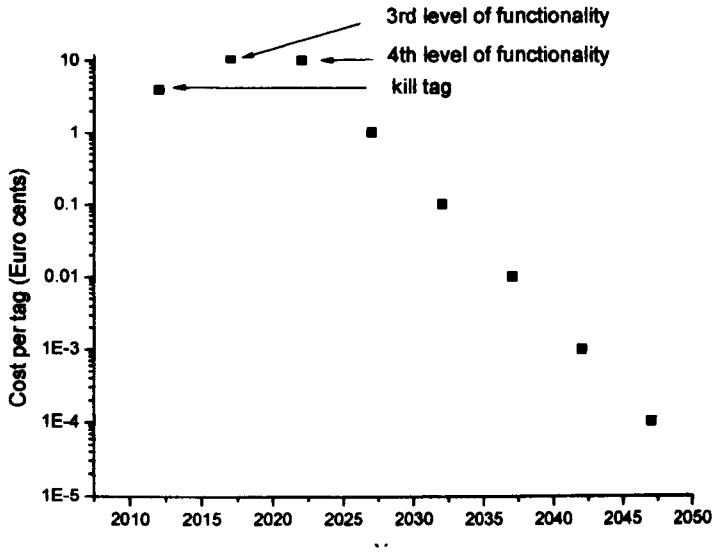


Figure 8.15.2: The variation of tag cost with time.

Figure 8.15.3, shows in more detail how the cost of tags reduces with time.

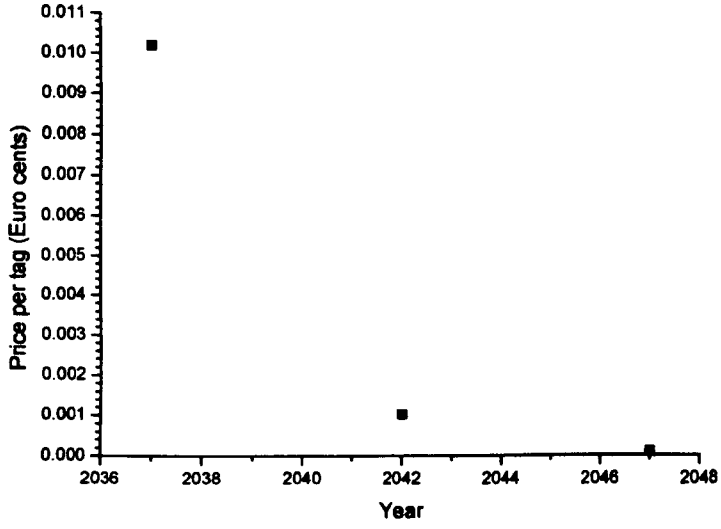


Figure 8.15.3: The variation of tag cost with time.

Making the environment cleaner reduces the defect density and therefore increases the yield of working devices. A more beneficial technique is to reduce the minimum feature size; this scales devices down in size, reducing the probability of a device, coinciding with a defect; this has a huge effect on increasing the yield. It also provides additional functionality by increasing the speed of the circuit.

It should be possible to determine the time for a chip containing any fixed number of transistors to become profitable. This in reality means that there will be an economic yield on a chip which will provide functionality that has a ready made market.

In the case of a simple rfid security tag, we would expect it to be used on items that are relatively expensive. However existing shop security tags would probably be used in preference to the rfid tag, as it would be expensive, to replace readers and the existing mechanisms. The market for such a tag is limited and would saturate fairly quickly.

A 'sleepertag' could for example be awakened if the item were to be returned and would therefore go back on the shelf. It is clear that the sleeper tag would need to be achieved relatively quickly after the kill tag. It has been estimated that the kill tag needs 40 components and the sleepertag needs 200 components. It has been assumed that with the increase in functionality and the promise of full barcode replacement, there will be a linear growth from the introduction of the kill tag to the date the 3rd level of functionality is introduced.

This is because it is expected that when companies come to replace the existing readers due to 'natural decay' they will be replaced with the rf reader.

The third generation would include the 'sleepertag' but would also have some stock information; for example it may record the maximum temperature seen by goods and the date they were shipped from the supplier. This has been estimated to require approximately 1100 components, and will therefore have a longer development time. However as can be seen by *figures 8.15.2* and *8.15.3*, this 3rd level of functionality will be relatively expensive and the additional functionality may be regarded as not being worth the extra cost by businesses.

The fourth generation which is full barcode replacement including anti collision will initially be relatively expensive. It is therefore felt that checkouts in supermarkets will only start to disappear when full barcode replacement becomes economic.

Figure 8.15.2, shows that by 2032 a tag will cost approximately 1 Euro Cent, which is significantly cheaper than the cheapest supermarket item, it is therefore felt to be at this point the checkout will disappear and supermarket will make relatively large savings. The full barcode replacement will contain all the functions associated with earlier generations excluding the kill tag; as well anti collision.

The diagram in *figure 8.15.4*, shows an estimation of the tags required per year, in the UK based on the previous discussion.

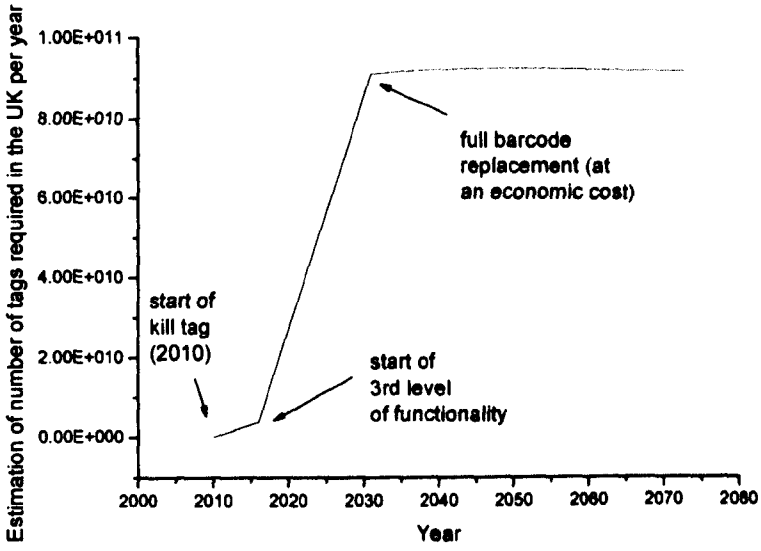


Figure 8.15.4: The estimation of number of tags required in the UK per year.

It has been assumed that the population increases are accompanied by a potential growth in the market, it has been also assumed that the number of products with RFID tags bought in the UK per person is the same as the number of RFID tags bought in Western Europe per person, this leads to *figure 8.15.5*.

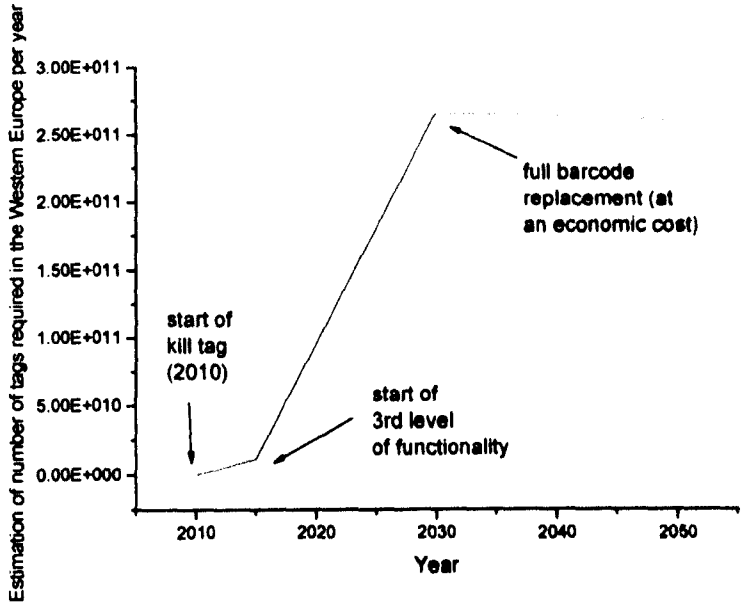


Figure 8.15.5: The estimation of number of tags required in Western Europe per year.

The earlier generations of tags will probably disappear; when the cheap barcode replacement tags comes into being.

There maybe a 5th generation but this has to thought out very carefully, to be sure that it brings sufficient new functionality to make it attractive to supermarket chains. An item level tag that can be read inside a carton at some distance would help to reduce shrinkage but it may not be at 13.56 MHz.

8.16 Conclusion

Organic electronics is rapidly growing into an industry. The predictions in this chapter are based on the growth seen in the silicon industry, it is too early to see where the organic industry is on the timescale, if indeed this industry is on the timescale. It should also be remembered that, the basic device physics for organics is felt to be significantly different from silicon, so it is necessary to understand whether various approximations used with single devices are applicable. This chapter shows how the rf tags functionality may increase with time leading to a full anti-collision tag, which will replace cashier operated tills. The potential market in the UK has also been calculated, this would indicate that there is a huge potential market for organic electronics. It should however also be remembered that there is competition for the potential market of organic electronics and other technologies such as LCD and silicon may win some potential markets.

8.17 References

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Chapter 9

Conclusions and Recommendations for Further Work

Presented in this chapter are the main conclusions of this thesis. In the further work section of this chapter; ideas and areas which need further work are suggested.

9.1 Conclusions

In Chapter 3, the fabrication process of TFTs was described. The transfer characteristic of TFTs were also explained and the effects of fabrication processes were discussed. It was also concluded that ion movement was one of the likely causes of hysteresis in TFTs.

Five equations for the gradual channel equation for TFT's have been derived using based on different approximations. It was found that equations for drain current were identical if either the delta function, the distribution defined by a transport level and the Debye length or the exponential distribution of states with energy assumptions were used, this may imply that a transport level is applicable where there is an exponential distance of states. The fourth equation however was very different it assumed both exponential distribution of states and the dependences of mobility on electron concentration; it was shown that this equation had the best fit for devices fabricating using PTAA. This was probably because PTAA is a very disordered material. The final equation was that of the delta function with universal mobility law; this produced a different equation from those previously defined and highlighted the need for the channel thickness to be taken into account. It was however observed that when $m = 0$, there is a single transport level and $K=\mu$, and that fourth and fifth equations becomes identical to the previous equations. It has been shown that the effect on the carrier mobility of the exponential distribution of states is extremely significant. It has also been demonstrated that mobility is essentially not a property of the material but depends on device factors, such as the oxide capacitance.

Chapter 5 examines MOS capacitors which are an important test structure. MOS capacitors were fabricated using alumina and PTAA, using the results obtained from C-V measurements the thickness of polymer spun films have been estimated as has the surface mobility of capacitors. Known effects in silicon and related effects in organic semiconductors have been discussed. The Debye length has been derived for both ordered and disordered semiconductors, which is important as it shows that the abrupt depletion edge approximation as well as the high accumulation layer capacitance are as good in a disordered material as in an ordered material.

Chapter 6 discusses the different causes of hysteresis. It was found that the major cause of hysteresis in MOS capacitors was likely to be a result of oxygen ions in the semiconductor and dielectric. It was also shown that before treatment with the

vacuum, the ions in the semiconductor were the dominant instability mechanism; while after vacuum treatment, ions appeared to return to the dielectric with more ease than to the semiconductor; hence ions in the dielectric became the dominant cause of instability.

Chapter 7 concentrates on Schottky diodes; the fabrication methods and characteristics are discussed. Values for the ideality factor, T_c, T_o and Meyer Neldels Energy were used to examine the effect of doping. The values of Meyer Neldels energy increase when dopant such as DDQ is added, it was concluded that this was a result of doping producing more states. The current flow mechanism in Schottky diodes is dependent on the type of polymer used; the different mechanisms involved were therefore discussed. Hysteresis in Schottky diodes was also observed and it was found that the mechanisms were associated with ion and diffusion flow.

In the three types of device examined; Schottky diodes, MOS capacitors and TFT's ion movement appears to be a major cause of hysteresis, one possible solution to the instability problems that have been observed, therefore is to develop a cheap encapsulation method, to prevent devices being exposed to the atmosphere.

As organic electronics is growing into an industry it is important to have a roadmap, chapter 8 discusses the importance of having a roadmap. Scaling, the minimum feature size and the active area will all have a large impact on the roadmap, these are therefore discussed individually. The timescale for emergence of tags with higher functionality is shown and potential applications are discussed. The number of tags required in the UK and Western Europe per year has also been estimated. It has been predicted that by the year 2030 full barcode replacement will be available at an economic cost.

Stability is still a major problem in organic electronics, before circuits are seen in items such as RFID tags and flexible plastic applications such as an electronic newspaper, this problem will have to be solved a possible method of achieving this may be found by understanding the mechanisms involved, while another option is by encapsulation.

9.2 Further Work

Transients include high frequency behaviour and logic. For organic devices such as Schottky diodes and TFT's there is a large emphasis on transients, as it is essential to under the behaviour of transients for the RFID tag, which will operate at 13.5 MHz.

It is assumed that for each value of gate voltage the current will be given by the DC current for that value, however this is not the case and therefore needs to be investigated.

There is no accurate method to predict the characteristics of MOS capacitors at high frequency, this is due to the percolation effect, further work is therefore needed in this area.

Five versions of the gradual channel equal for TFTs have been derived, however further work is needed to determine temperature dependence.

One of the biggest problems that needs to be overcome in the area of organic electronics, is stability, much work is needed in this area. Different mechanisms for example slow trapping and ionic movement may work together, at the moment in respect to this, it is not obvious what is happening. Further work is therefore needed in this area. If the sensitivity of devices to air cannot be removed cheap effective methods of encapsulation may be needed.

In comparison to single crystal and amorphous materials, polycrystalline materials have had little attention. Research into organic devices is beginning to focus on polycrystalline devices. This is because they are less disordered and more structured than conjugated polymers; this results in higher mobilities.

Increasing the mobility is important; as this will lead to faster on-off switching and the ability for devices to work predictability at high frequencies.

The gate voltage effects surface potential controlled by the grain boundary therefore there are a lot of similarities between polycrystalline and disordered material, however the temperature effect may be different, this needs to be explored further.

Work also needs to be carried out to determine an accurate gradual channel equation for TFTs fabricated using polycrystalline materials.

The different polycrystalline materials available for example Lisicon and triisopropylsilyethynyl (TIPS) need to be compared. Polycrystalline materials mechanisms need to be further examined and the appropriate equations need to be derived and mechanisms need to be fully understood and further investigated. The end aim is to combine organic devices to form circuits; this is necessary to form rectifiers, oscillators, logic circuits and memory; so that devices such as the RFID tag can be created. It is therefore essential that work is carried out; to enable crossovers to be fabricated cheaply and with the minimum number of process stages.

A roadmap has also been devised for Western Europe; it would however be useful to expand this to the developed world and eventually across the entire world.

Appendix: Publications

Conference Poster: J. Sessford, N. Sedghi, M. Raja, D. Donaghy, W. Eccleston, "The Technical Roadmapping of Organic Electronics", International Conference on Organic Electronics (ICOE), Philips High Tech Campus, Eindhoven, Netherlands, June 2007.

Journal Paper: J. Sessford, W. Eccleston, "Analysis of Electrical Instability in Organic Devices", (submission pending).