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Development and Design of Polymer Circuits based on Polymer Thin-film Transistors

by

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ABSTRACT

After first reported twenty years ago, organic thin-film transistors have become a focus of research and development not only in academic institutes but in a rapidly increasing number of companies.

The successes in the material study and device characterisation work with polymers brings improved performance to polymer transistors such as reasonable high mobility, low off-on current and better stability. However, it is still very difficult and complicated to build working circuits through integrating the polymer transistors, because it requires more manufacturing processes and essential components such as VIAs (vertical interconnections) and crossover structures. As well as the manufacturing process, the development of circuit design with calculation and simulations based on a more exact polymer transistor model has been undertaken. These have provided the basis of layout of masks for photolithography and all this work is included in the thesis.

Using regio-regular poly(3-hexylthiophene) as the channel semiconductor and high-K alumina grown by anodization as the gate dielectric, bottom-contact thin-film field-effect transistors have been studied, and are described in this thesis. There is a focus on a device model based on the published relation between conductivity and mobility which may be explained with the variable range hopping model. The dependence of the mobility on the gate bias voltage and temperature have been found from this model. The contact resistance at source/drain electrodes and its impact on the surface potential along the channel are also explained.

Based on the new transistor model, subcircuits including the inverter, ring oscillator and others widely used in polymer circuits are analyzed and simulated. The focus is on the relationship between device characteristics and circuit performance. Suitable circuit configurations for the p-type polymer inverter have been found to be the saturated-load inverter.

The work related to process prototyping of polymer circuits consists of polymer transistors, VIAs and crossover structures. Three possible solutions of making VIAs, selective anodization, etching with stop layer and copper platting on aluminium are explained with example circuits. Using Cadence Virtuoso, one set of eight masks have been designed for transistor-based circuits, CCD devices and vertical transistors etc.

To verify the process design and mask layout for polymer circuits, experimental work was undertaken in a clean room environment and the results are presented and discussed. Possible solutions of critical peeling problems are suggested.

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Chapter 1

INTRODUCTION OF ORGANIC ELECTRONICS

This chapter does a brief introduction on the subject of organic electronics circuits; including history, current research achievements and challenges, as well as discussion various applications and possible applications. The motivation and organisation of the thesis along with the research techniques are also given here.

1.1 Background of organic electronics

The history of organic electronics begins with an accidental discovery from Shirakawa, MacDiarmid and Heeger together in 1977 [1], [2], [3]. They found that the simple conjugated polymer; Polyacetylene (PA), when partially oxidised increased its electrical conductivity by many orders. After this discovery, more organic materials such as Poly(3-hexylthiophene) (P3HT) and Polytriarylamine (PTAA) have been studied, the focus being on their electronic properties and synthesis methods [4], [5] [6]. New theoretical approaches have been developed to explain their electronic properties. Various efforts have been adopted to improve their electronic properties including doping and high regio-regularity [7].

In the last 10 years, the benefit of the earlier theoretical work and the experience of synthesising work have made a wide range of applications possible, such as OLED (organic light emitter diode) [8], [9] [10], OTFT (organic thin film transistor) and "electronic ink" displays. Additionally, bioelectronics sensors and RFID (radio-frequency identification tags) using organic circuits have been proposed and are in development. The application of organic materials as active layers in electronic devices has the advantages of low cost, mechanical flexibility and easy fabrication especially for the applications requiring large coverage area.

1.2 Current work review

At present there are three groups of organic semiconductors used in electronics: small molecules; oligomers (short-chain organic); and polymers (long-chain organic). As a general rule, oligomers deposited by evaporation in vacuum, like pentacene [11] [12], have a highly ordered molecular structure which enhances the charge transport. Their fabrication requirements are critical and the costs involved are higher, thus reducing their commercial appeal. On the other side, long-chain polymer (such as P3HT and PTAA), are deposited by spin coating or inkjet printing at low temperatures. The thin-film transistors manufactured on such substrates usually have a lower electrical performance (lower mobility) than oligomer-based devices.

Field-effect transistors with pentacene deposited by vacuum evaporation have mobility values as high as 15 $cm^2V^{-1}s^{-1}$, current on/off ratios as large as 10^8, near-zero threshold voltage, and sub-threshold slopes as low as 1.6 V/decade with reported by the researchers at the Pennsylvania State University [13]. The transistors have been fabricated on heavily doped thermally oxidized silicon substrates treated with octadecyltrichlorosilane, a silane coupling agent. Even so, polymer devices have a considerable potential in large-area low-cost flexible application; although so far, the electrical performances of most polymer thin-film transistors are often limited by the low carrier mobility.

1.3 Motivation and Thesis Organization

This thesis focuses on the development of the polymer circuit technology based on the previous P3HT based devices research carried out in our research group. This circuit technology was required to be compatible with the bottom-gate device structure and with our main manufacturing processes for TFTs, (such as aqueous anodization for an alumina based gate dielectric and spin coating for the top layer of semiconducting polymer). While developing the technology, particular attention was given to the compulsory circuit structures, such as crossovers between connection wires and vertical interconnection (VIA). Conflicts between different processes also have to be avoided. Substantial efforts were put into avoiding the conflicts between different processes. Also experimental datas including the IV measurements on polymer TFTs, and the polymer conductivities against various dopping levels have been provided by Dr M. Raja for the study of device performance.

To demonstrate and evaluate the process design, simple circuits with photolithography masks were designed with the Cadence system. This mask has included the layouts of the ring oscillator, shift register and charge coupled device (CCD) as well as some basic subcircuits and test structures. The choice of CCD was motivated by their considerable potential for use in sequencing the parallel outputs of non-volatile

memory in RFID circuits.

A primary effort of this research has involved in producing polymer circuits in a clean room environment. Metallization, lithography and anodization is the main process utilised. This is a prototyping activity required mainly for testing devices and circuit designs. A test system of computer-controlled equipment for circuit measurement and a set of instruments for aqueous anodization have also been set up.

A brief description of the chapters in this thesis is as follows:

Chapter 2 begins by describing the background theory of polymer semiconductors. The conduction mechanisms in disordered organic materials are briefly discussed. Based on the most recent concepts of charge transport in polymer semiconductors, a DC model of polymer transistor has been independently developed. The model is compared with the conventional transistor model. Based on this model, the methods used to obtain effective field effect mobility are also discussed.

Chapter 3 focuses on the calculation and simulation of polymer circuits using the new DC model of a polymer transistor. Several basic sub units which might be used in complex polymer circuits are studied. Inverters with active loads are the most interesting since they are widely used and circuit performance is highly dependent on the design of this

sub circuit. They may not be optimised for speed, but they are designed to accommodate the anticipated spread in gate threshold voltage. Lower aspect ratio loads are one example. In some situation, the analytical expressions obtain were really complex they were further simplified, while paying the necessary attention to the physical meaning the assumptions made. In order to obtain a numerical result of circuit calculation, polymer circuits are simulated in MathCAD using our new equation; results are compared with experimental data on transistor characteristics. Also parasitic resistance via the polymer layer among transistors were studied with AC simulations on a simple inverter layout.

Chapter 4 discusses the requirements of a polymer circuit fabrication process including transistor configuration, materials, VIA and crossover structures. With these considerations in mind, two prototypes of a polymer circuit fabrication sequence are designed.

Chapter 5 concludes the results of the experimental work in the clean room. The outcome of the lift-off process is discussed. The results of test experiments on selective anodization using different photoresist materials and with various minimum feature sizes are also presented and discussed.

Chapter 6 finally summarises the work done and results presented in the thesis. Suggestions for future work can be seen in this chapter.

1.4 Experimental techniques

Highly region-regular poly(3-hexythiophene) (P3HT) employed in this research work was synthesised and fractionated in the Department of Chemistry at the University of Liverpool, using methods demonstrated by McCullough and Trznadel [14]. Other molecules such as 2,3-dichloro-5,6-dicyano-1,4-benzoquinone (DDQ) used as doping material were obtained from Aldrich Chemical Co. and crystallized at Liverpool.

The inorganic gate dielectric (aluminium oxide), used in the polymer TFTs, was grown using aqueous anodization with a constant voltage at room temperature. A simple cell was constructed for this purpose. A conventional optical lithography system was used to define patterns. The chromium masks for lithography were designed with Cadence Virtuoso Layout Design system in an UNIX environment and were produced by Compugraphics Ltd.

Electrical characterisation (current-voltage measurements) was obtained using a Keithley voltage source and electrometer controlled by a PC. The capacitance-voltage characteristics were obtained using a Hewlett-Packard Analyser. The polymer TFTs were also characterised using a PC controlled HP 4145B Transistor Parameter Analyser.

A dedicated circuit measurement environment for circuit testing, with multiple inputs and output signals, was designed and developed. The input signals are generated by four Hewlett-Packard 33220A Function/Arbitrary Waveform Generators and boosted up from 0-10V to 0-60V with an analogue signal booster made by the Departmental Electrical workshop. The input and output signals can be visualized and saved to a computer with a Hewlett-Packard 54624A 4-Channel 100 MHz Oscilloscope. The whole system also including a DC power supply (output range: 50W 100V 0.5A) is connected via a GPIB interface to a RM Pentium III computer.

1.5 Contributions

In this research, the design, the prototypes of polymer circuits based on the current polymer device technology using lithography and aqueous anodization process was achieved. Test circuits including ring oscillators, shift registers and charge-coupled devices (CCDs) have been conceived, designed and simulated with the new polymer transistor model. The effects of different parasitic resistances were also discussed with AC simulations. These simulations were undertaken using a MathCAD package provided with device characteristic data and the results of it have been compared to the experimental results. Also one set of eight lithography masks have been designed with a Cadence Virtuoso layout

design package in a UNIX environment with designed process. A computer controlled apparatus for circuit measurement has been designed and built.

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Chapter 2

POLYMER TRANSISTOR MODELLING

Semiconducting polymer material with higher mobility and stability in air are highly commended for organic electronic applications. Knowing the mechanisms of the conduction process in the polymer material is important for increasing the mobility by optimized molecule structures and doping. In this chapter a model of the organic thin film transistor, which includes temperature dependence and instability, is introduced. Earlier work used percolation methods but here we have applied the concepts of classical device physics to an exponentially increasing density of states. This device model was further used in the next chapters for the simulation, calculation and design of the polymer circuits.

2.1 Introduction

The field effect transistor, especially metal-oxide-semiconductor field-effect transistor (MOSFET) has been the most important device for the integrated circuit in the silicon industry over the last several decades. It also shows a similar important position in the current developing organic technology. The polymer thin-film field-effect transistor, i.e. the field-effect transistor, in which a thin film of organic polymer material is used as the active semiconductor, may form the basis of future low-cost microelectronics technology on large area, flexible substrates. For effective circuit design and application development with these innovative polymer transistors, it is essential to understand their operating mechanism and DC/AC models.

2.2 Basic device operation of an organic transistor

The standalone organic transistor has been widely used in device characterization. A brief introduction of the structure and basic operation of a conventional organic field-effect transistor is given here. An organic field-effect transistor (FET) consists of several layers formed of insulating, semiconductor and electrical conducting material. The basic structure of an organic thin-film transistor is illustrated in Figure 1.

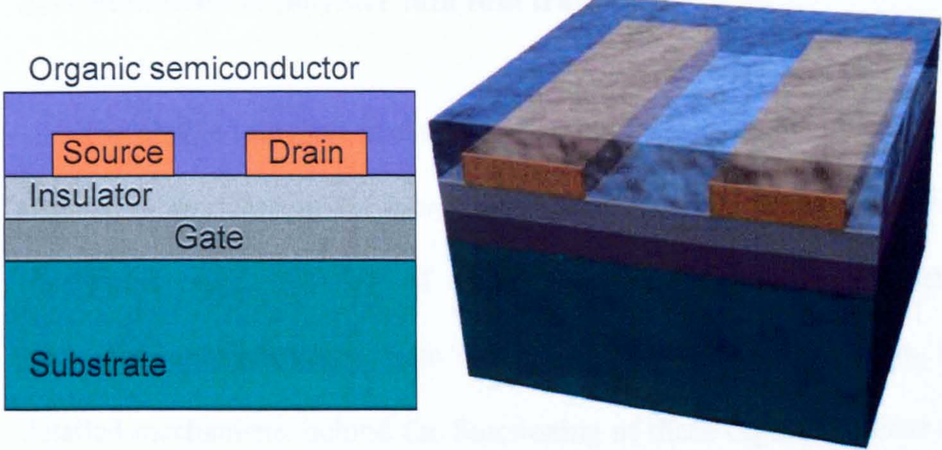

Figure 1: Schematic diagram of the organic thin-film transistor

The basic function of the organic thin-film field-effect transistor is the same as that of conventional metal-insulator-semiconductor field-effect transistors. By applying a voltage to the gate electrode, it is possible to modulate the current between two other terminals; the source and drain electrode. However we should note that organic FETs typically operate in accumulation rather than inversion and the majority carriers are typically holes (p-type semiconductor). Therefore we will focus our discussion here on p-type organic semiconductors only. If the source and drain electrodes are connected to ground, and a positive voltage is applied on the gate, the semiconductor becomes depleted of mobile charge carriers. In this state the transistor is switched 'OFF'. When a negative voltage is applied to the gate terminal, the positive charge is induced to semiconductor-insulator interface and a conductive channel is generated between the source and drain electrodes. The transistor is turned 'ON'.

2.3 Conduction in polymer thin film transistor

The charge transport in disordered organic semiconductors has been studied by considering the temperature and gate voltage dependence of the charge carrier mobility of organic field-effect thin-film transistor. Even if these studies have been carried out for mare than 10 years, the detailed mechanisms behind the functioning of these organic devices are still not fully understood. The conduction in solution-processed organics have been studied experimentally through the thermally activated field-effect mobility and its gate voltage dependency [1], [2]. The carrier transport in disordered semiconductors is generally described by the hopping process, i.e. the thermal activated tunnelling between localized states, rather than by the activation of carriers to a transport level [2]. One of the reasons that hopping is widely accepted is that it explains the results of experiments in which the field-effect mobility of holes in the disordered organic transistor is influenced by the temperature and also the applied gate bias [1]. These observations have thus far been modelled using multiple trapping and release [3], variable range hopping (VRH) [4] and grain boundary charging [5].

The multiple trapping and release model, as proposed originally for amorphous silicon thin-film transistor [6], [7], was found to give a reasonable description of the characteristics of the organic transistor [8].

In this model, the assumption is made that the charge transport occurs via hopping between states above a critical energy. Most of the charge carriers are trapped in the localized states below this critical energy, also known as the transport energy. Charges trapped in these states are released and excited to the transport level when they receive enough energy. The amount of temporarily released charge carriers to extended-state transport level (similar to the valence band for classical p-type semiconductor) depends on the energy level of the localized states, the temperature, and the gate voltage. However, while extended-state transport may occur in highly ordered materials, we do not expect it to play a role in disordered organic films, where the low-mobility charge carriers are strongly localized. An alternative model was proposed by Vissenberg and Matters [2]. In this model, the motion of the charge carriers in organic semiconductors is typically described by hopping transport, which is a phonon-assisted tunnelling mechanism from site to site. Briefly, the dependence stems from the fact that as the gate voltage increases the injected charge-carriers tend to fill the traps so trapping becomes less efficient and charge transport improves. Combining the hoping model with the Gaussian disorder representation has resulted in a useful description of organic transistor operation [2]. Because of the hopping of carriers between localized states which are distributed in energy, the experimentally determined charge carrier mobility has a thermally activated behaviour and depends on the charge carrier density.

The model gives a very reasonable description of the organic FET operation in accumulation [2].

In the rest of this chapter, the device model of the organic field effect transistor will be studied focusing firstly on the influence of applied gate bias, followed by the influence of working temperature.

2.4 Device model of the polymer thin film transistor

In the modelling of the transistor, difficulty of defining the threshold voltage was pointed out by Horowitz et al [9], because most organic transistors only operate in accumulation and no channel current in the inversion regime is observed. Therefore the switch-on voltage of the organic transistor is defined as the onset of charge accumulation instead of the threshold voltage in the inorganic transistor which is used to describe the onset of charge inversion [10]. Flatband voltage (V_{FB}), is used as the switch-on voltage for the organic transistor.

Using a P3HT transistor as an example, the current-voltage characteristics of a typical P-type organic transistor with Al_2O_3 gate dielectric and gold source/drain electrodes is shown in Figure 2 with the IV measurement data provided one of our group member, Dr Muni Raja. We can see the drain-source voltage is always negative.

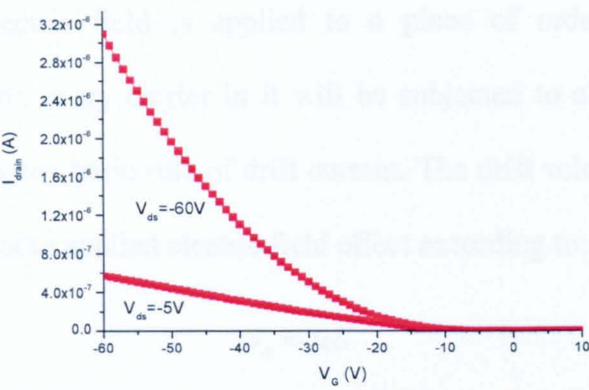

Figure 2: Current-voltage characteristics of transistor with P-type material P3HT

At the switch voltage (the flatband voltage) only the charge carriers in the bulk of the semiconductor carry the current, while in the accumulation model the charge carrier induced by the field-effect predominantly carries the current. In Figure 3 a schematic of an organic accumulation-mode FET shows these two components of the drain current, field effect current and bulk current. The field effect current is related to the ease in which the depletion layer thickness increases with positive gate voltage, while the bulk current is related to the conductivity of the semiconductor.

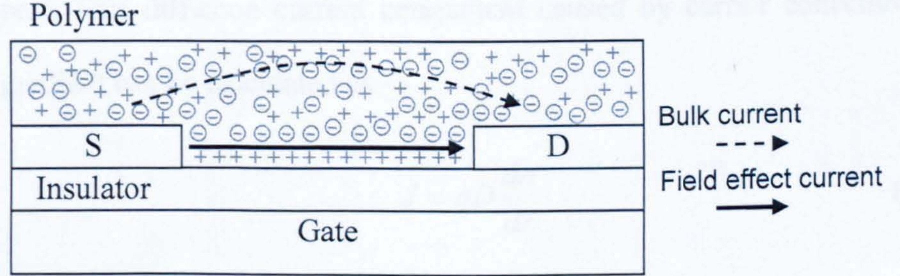

Figure 3: Conduction in organic accumulation-mode FET

To model the drain current in the organic transistor we need to go back to the basics of the conduction in semiconductor, drift and diffusion.

When an electric field is applied to a piece of ordered crystalline semiconductor, every carrier in it will be subjected to a force and will move. This is the basic rule of drift current. The drift velocity of carriers is proportional to applied electric field effect according to:

$$v_d = \mu E \tag{2.1}$$

where μ is drift mobility, v_d is the drift velocity and E is the electric field strength. Mobility is clearly a measure of how easily charge carriers move under the influence of an electric field. The drift current density J is related to mobility as:

$$J = nq\mu E \tag{2.2}$$

where q is the electronic charge.

When the carrier concentration varies in the semiconductor, carriers will tend to move from the high carrier density part to the low density part. This diffusion current component caused by carrier concentration gradient can be calculated as

$$J = qD\frac{dn}{dx} \tag{2.3}$$

where D is the constant diffusion coefficient.

As important parameters, mobility (μ) and diffusion coefficient (D) are used in silicon technology to measure the drift and diffusion behaviour in semiconductors. To link these two parameters, Einstein's relation [11] has been derived for the non-degenerate semiconductor as:

$$D = \frac{\mu kT}{q}. \tag{2.4}$$

This expression may also hold in organic semiconductors but this needs to be established with a higher degree of certainty.

The current density in a TFT channel in some direction x is given by a combination of drift and diffusion contributions:

$$J = qD\left(\frac{dn}{dx}\right) + qn\mu E_x \tag{2.5}$$

which can be reduced by using Equation (2.4):

$$J = (\mu kT)\left(\frac{dn}{dx}\right) + qn\mu E_x \tag{2.6}$$

where E_x is the electric field down the channel.

To compare the contribution of drift and diffusion components, we make the following assumptions: (a) the carrier distribution in the x direction has a linear relationship as: $\frac{dn}{dx} = \frac{n(0)-n(x)}{L}\bigg|_{n(x)=0} \approx \frac{n(0)}{L}$, and (b) when $V_s = 0\text{V}$, the field along E_x the x direction is constant and equal

to $-\frac{V_D}{L}$, where L is the channel length, $n(0)$ is the carrier concentration at $x=0$ and V_D is the drain voltage. Then the diffusion current is:

$$J_{x,diffusion} \approx -qn(0)\mu\frac{kT/q}{L} \tag{2.7}$$

and the drift current is:

$$J_{x,drift} = -qn(0)\mu\frac{V_D}{L}. \tag{2.8}$$

Here we can conclude that the drift current is the major part of the conduction process because kT/q, which is 25.9 mV at 300K, can be neglected compared to V_D. This assumption simplifies the derivation of the organic thin film device model. It is in strong contrast to inversion devices where the sub-threshold is controlled by diffusion.

The conventional DC model of the thin film transistor is described using the field-effect mobility μ, which is also widely used to evaluate the performance of organic thin film transistor materials. For inorganic MOSFET the value of field-effect thin film mobility can be obtained from the saturation regime of the transistor, where the source-drain current I_D is related with gate bias V_G' ($V_G' = V_G - V_T$) as follows:

$$I_D = \mu C_o\left(\frac{W}{L}\right)\frac{V_G'^2}{2} \tag{2.9}$$

where W is the channel width, L is the channel length and C_o is the

capacitance per unit area of the gate insulator.

Also in some reports, the measured field-effect mobility is determined in linear operation mode. The calculation is based upon the linear source-drain current equation:

$$I_D = \mu C_o \left(\frac{W}{L}\right)\left(V_G' V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{2.10}$$

where V_{DS} is the drain voltage measured with respect to the source. The field effect mobility can then be calculated from the linear relationship between drain current and gate voltage with the following equation:

$$\mu = \frac{dI_D}{dV_G} \frac{L}{WC_o V_{DS}} \tag{2.11}$$

with the assumption that the mobility is independent of gate bias voltage.

The field-effect mobility which comes from these equations is the usual way to evaluate the performance of organic transistors and compare them to the existing devices, although it would not be adequate for the purpose of detailed modelling of circuit performance. In organic field-effect transistors, the mobility depends on the charge carrier density, which results from the transport of carriers within the organic semiconductor being governed by the hopping between localized states.

A.R. Brown in 1994 [12], reported that the measured field-effect

mobility of the organic transistor is related to the measured conductivity σ by a power law:

$$\mu = K_1 \sigma^{\gamma} \tag{2.12}$$

where K_1 and γ are empirical parameters calculated from the power-law fitting on the measured data.

When changing the carrier concentration by adding dopant, it was found that the measured conductivity and the dopant concentration N_d also fitted a simple power relation.

The dependency of bulk mobility on conductivity for doped P3HT has been measured and represented with different percentages of P3HT/DDQ. The value of the constants can be extracted from the measurement result provided by co-workers, Dr M. Raja etc. [13]

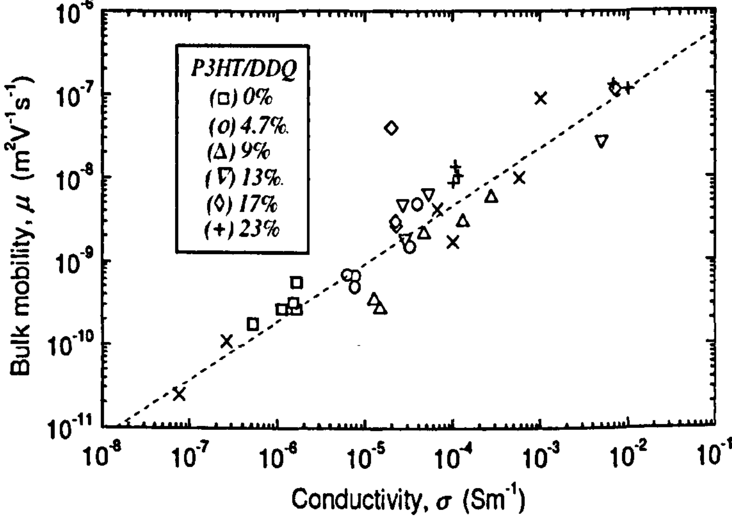

Figure 4: Bulk mobility against conductivity for doped P3HT

Therefore the direct relation between mobility and dopant concentration referred to as the universal mobility law, can be expressed as:

$$\mu = K_2 N_d^{\ \delta} \tag{2.13}$$

where K_2 and δ are constants.

With two assumptions that the bulk drift mobility is equal to the field-effect mobility and that there is a simple proportional relationship between the added dopant content per unit volume (N_d) and the concentration of mobile charge carriers per unit volume (n), they proposed that the field-effect mobility μ and the charge carrier concentration may be linked by a universal empirical relationship:

$$\mu = Kn^m \tag{2.14}$$

where m is apparently a universal constant and K is associated with the particular material.

Introducing the dependence of mobility on charge carrier concentration, the current density J can be presented as:

$$J = qKn^{m+1}E_x. \tag{2.15}$$

with the field-effect along the direction of current, E_x and the charge density, n. The charge density in polymer is controlled by the field effect in z direction associated with the gate voltage. The cross section of an

organic thin film transistor as shown in Figure 5 is used to explain the derivation of the drain current equation. From the Poisson equation and the relationship between field effect and potential, we have

$$\frac{dE_z}{dz} = -\frac{d^2\phi}{dz^2} = -\frac{qn}{\varepsilon_s\varepsilon_0}. \quad (2.16)$$

$$E_z \cdot dE_z = \frac{qn}{\varepsilon_s\varepsilon_0} \cdot d\phi. \quad (2.17)$$

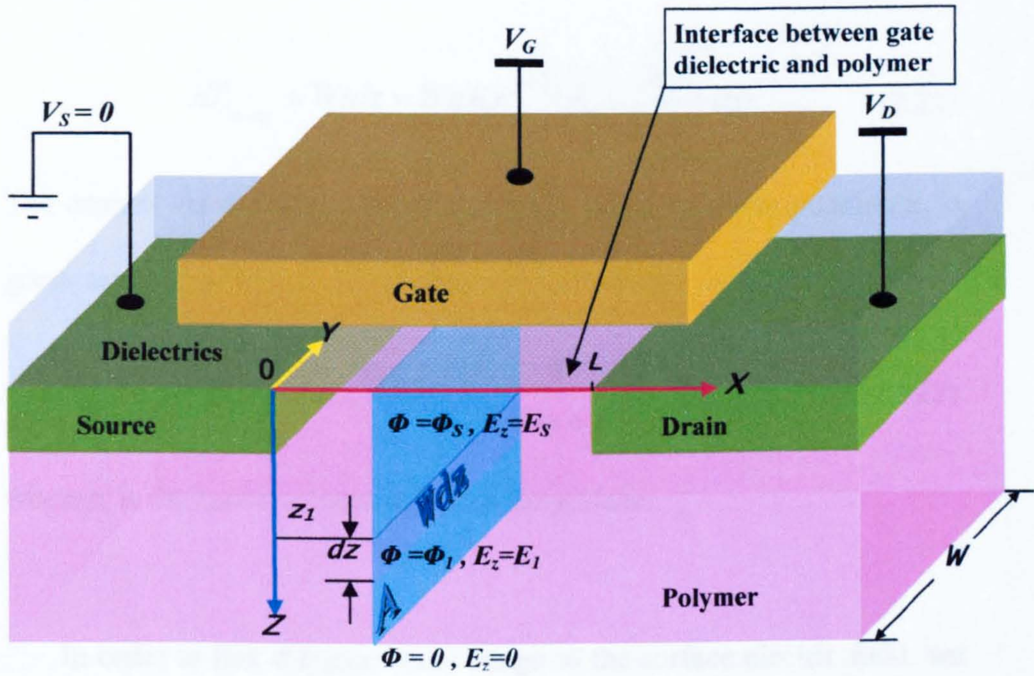

Figure 5 Current integration in organic field effect transistor

The electric field in z direction at arbitrary point, $z = z_1$, in the polymer can be attained by integrated both site of equation (2.17) from $\phi = \phi_1$ to $\phi = 0$.

$$\int_0^{E_1} E_z dE_z = \frac{qn_0}{\varepsilon_s\varepsilon_0} \int_0^{\phi_1} \exp(q\phi/kT)\, d\phi \quad (2.18)$$

$$E_1 \approx \pm\sqrt{\frac{2kT}{\varepsilon_s\varepsilon_0}}\cdot n_1^{1/2} \tag{2.19}$$

where

$$n_1 = n_0 \exp\left(\frac{q\phi_1}{kT}\right). \tag{2.20}$$

Considering the incremental current flows through the small section *Wdz* in cross-section A:

$$dI\big|_{z=z_1} = Wjdz = WqKn^{m+1/2}E_x \cdot \sqrt{\frac{\varepsilon_s\varepsilon_o}{2kT}}d\phi \tag{2.21}$$

The current via the whole cross section A, which is at the position x, is given as:

$$I\big|_A = WK\sqrt{2kT\varepsilon_s\varepsilon_0}\cdot\frac{1}{2m+1}\cdot n_s^{m+\frac{1}{2}}E_x \tag{2.22}$$

where n_s is the carrier concentration at the surface.

In order to link the gate bias voltage to the surface electric field, we apply the Gauss's law at the polymer-dielectric interface such that $\varepsilon_0\varepsilon_{ox}E_{ox} = \varepsilon_0\varepsilon_s E_s$, where E_s and E_{ox} is surface electric field in the polymer semiconductor and the oxide. And we have,

$$\varepsilon_0\varepsilon_{ox}\left(\frac{V_G - V_x}{d_{ox}}\right) = \varepsilon_0\varepsilon_s\sqrt{\frac{2kT}{\varepsilon_0\varepsilon_s}}\cdot n_s^{1/2} \tag{2.23}$$

where $V_G - V_x$ is the voltage across the oxide, d_{ox} is the thickness of the gate oxide. This gives us the expression for surface carrier concentration

n_s of applied gate voltage V_G as,

$$n_s = \frac{C_o^2 \cdot (V_G - V_x)^2}{2kT\varepsilon_0\varepsilon_s} \tag{2.24}$$

where $C_o = \frac{\varepsilon_0\varepsilon_{ox}}{d_{ox}}$ is the capacitance per unit area. Substituting (2.24) into (2.22),

$$I|_A = WK \cdot \frac{1}{2m+1} \cdot \frac{C_0^{2m+1} \cdot (V_G' - V_x)^{2m+1}}{(2kT\varepsilon_0\varepsilon_s)^m} E_x \tag{2.25}$$

where V_G' equals to gate voltage V_G minus the threshold voltage V_T.

Integrating the current via every cross section down to the channel, the channel length L of the transistor and the source/drain voltage can be taken into account:

$$\int_0^L I dx = WK \frac{1}{2m+1} \cdot \frac{C_0^{2m+1}}{(2kT\varepsilon_0\varepsilon_s)^m} \int_0^{V_D} (V_G' - V_x)^{2m+1} dV_x . \tag{2.26}$$

Therefore the drain current is presented as

$$I = \frac{KC_o^{(2m+1)}W}{(2\varepsilon_o\varepsilon_s kT)^m L} \left[\frac{V_G'^{2(m+1)} - (V_G' - V_D)^{2(m+1)}}{2 \cdot (2m+1)(m+1)} \right]. \tag{2.27}$$

In saturation mode, the drain current can be reduced by pinch-off. This occurs when $V_D = V_G'$.

$$I = \frac{KC_o^{(2m+1)}W}{(2\varepsilon_o\varepsilon_s kT)^m L} \left[\frac{V_G'^{2(m+1)}}{2 \cdot (2m+1)(m+1)} \right] \tag{2.28}$$

When m=0, i.e. the dependence between the carrier concentration and

mobility is ignored, these two equations are reduced to the conventional equations based on the gradual channel model.

By comparing the equations (2.9) and (2.28), an expression for the effective field effect mobility can be obtained as:

$$\mu = \frac{KC_o^{2m} V_G'^{2m}}{(m+1)(2m+1)(2\varepsilon_0\varepsilon_s kT)^m} \tag{2.29}$$

Also from the linear operation mode of field effect transistor, comparing the equations (2.10) with (2.27), we have:

$$\mu = \frac{KC_o^{2m}}{(2\varepsilon_o\varepsilon_s kT)^m}\left[\frac{V_G'^{2(m+1)} - (V_G' - V_D)^{2(m+1)}}{(2m+1)(m+1)(2V_G' V_{DS} - V_{DS}^2)}\right] \tag{2.30}$$

At the pinch-off point, $V_G' = V_D$, the same value of field effect mobility can be found from these two expressions.

In a recent report from AVECIA, UK, the interface effect between the gate insulator and organic semiconductors have been studied and new findings relating to low-*k* insulator used in organic transistor have been presented [14]. In their research, the field effect mobility was calculated from the gradient of I_{DS} vs. V_G as equation (2.11). However, applying equation (2.27) to (2.11), we have a different expression of field effect mobility from equation (2.30):

$$\mu' = \frac{KC_o^{2m}}{(2\varepsilon_o\varepsilon_s kT)^m}\left[\frac{V_G'^{2m+1}-(V_G'-V_D)^{2m+1}}{(2m+1)\cdot V_{DS}}\right]. \qquad (2.31)$$

The reason is that equation (2.11) introduces a hidden assumption where the field effect mobility μ is independent on V_G, i.e. $\frac{d\mu}{dV_G}=0$. According to equation (2.30), this assumption applies only when m=0. To correct the error of equation (2.31), the extra component associated with V_G needs to be added to the final mobility value:

$$\mu = \mu' + \frac{KC_o^{2m}}{(2\varepsilon_o\varepsilon_s kT)^m}\left[\frac{\left[V_G'^{2m+1}-(V_G'-V_D)^{2m+1}\right]\left[1-(2V_G'-V_{DS})(m+1)\right]}{(2m+1)(m+1)(2V_G'-V_{DS})V_{DS}}\right]. \qquad (2.32)$$

As we know gate capacitance per unit area $C_o=\frac{\varepsilon_{ox}\varepsilon_0}{d_{ox}}$ is proportional to the permittivity. Therefore the mobility calculated either from equation (2.29) in saturation region or equation (2.30) in linear region should increase with increasing gate insulator permittivity when V_G is independent of C_o.

The parameter extraction of m and K is based on the linear fitting between the measured data and the drain current equation in saturation region. From equation (2.28), we have

$$\log \frac{dI}{dV_{G'}} = \log\left[\frac{KC_o^{(2m+1)}W}{(2\varepsilon_o\varepsilon_s kT)^m L(2m+1)}\right] + (2m+1)\log V_{G'} \qquad (2.33)$$

The I-V characteristic data of P3HT transistors has been attained from Dr David Donaghy and it is presented in Figure 6 together with a linear fit based on equation (2.33). The values for m and K for polymer drain equation (2.27) and (2.28) were found as 0.365 and 7.85×10^{-16} respectively.

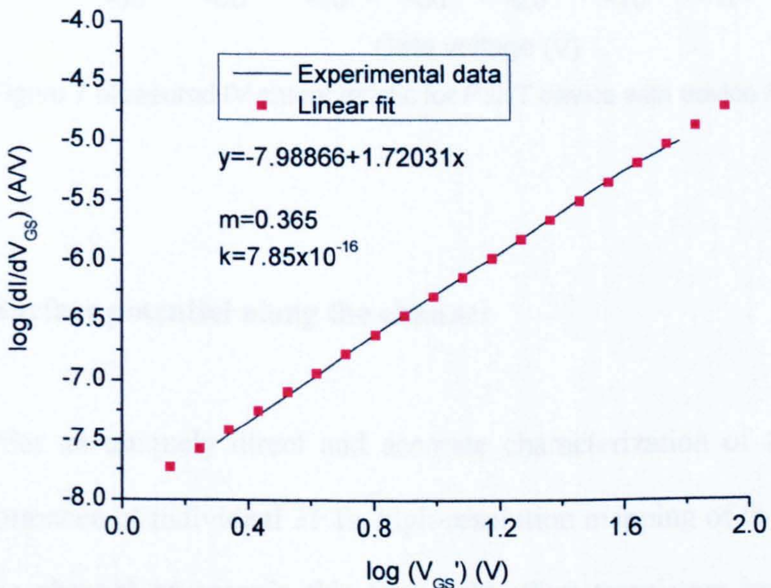

Figure 6 Parameter attraction of m and K with linear fitting

As shown in Figure 7, the measured drain current of P3HT transistor is plotted and compared with the IV curves generated from the new equations (2.27) and (2.28) developed for polymer transistor and the conventional equations. The new equations give a better fit to the experimental data.

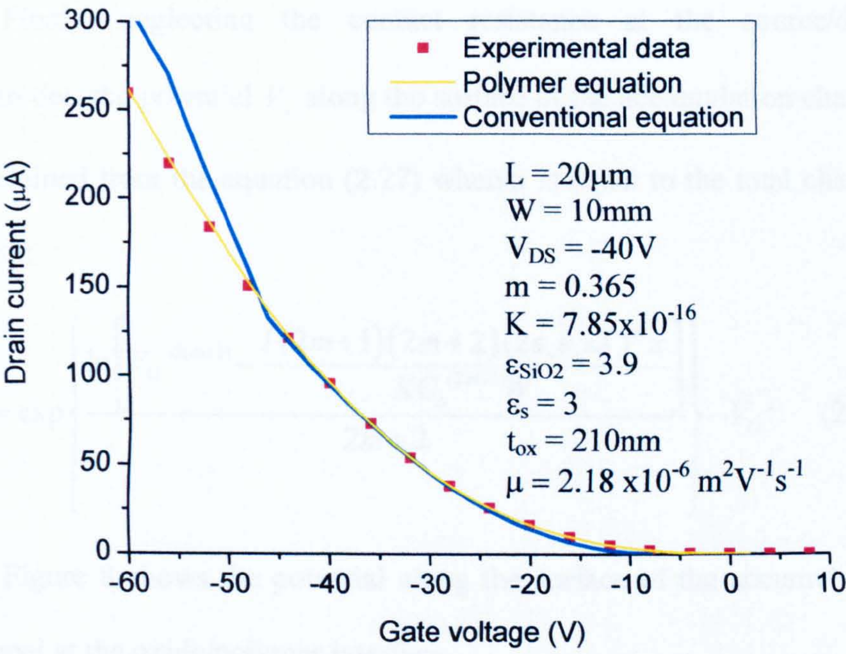

Figure 7 Measured IV characteristic for P3HT device with device models

2.5 Surface potential along the channel

For an uniquely direct and accurate characterization of the device performance of individual TFTs, high-resolution mapping of the potential in the channel of organic thin-film field-effect transistors by scanning Kelvin probe microscopy has been undertaken [15], [16]. The MathCAD simulation on surface potential is also undertaken successfully with the new drain equation. The simulation has shown similar potentiometry along the transistor channel except for voltage drops at the interfaces due to contact resistance. This will be discussed later in this section with its corresponding model of organic transistor.

Firstly, neglecting the contact resistance at the source/drain electrodes, the potential V_x along the surface of the accumulation channel is obtained from the equation (2.27) when x is equal to the total channel length:

$$V_x = \exp\left\{ \frac{\ln\left[V_G'^{2(m+1)} - \frac{I(2m+1)(2m+2)(2\varepsilon_o\varepsilon_s kT)^m x}{KC_o^{(2m+1)}W} \right]}{2m+2} \right\} - V_G' . \quad (2.34)$$

Figure 8 shows the potential along the surface of the accumulation channel at the oxide/polymer interface.

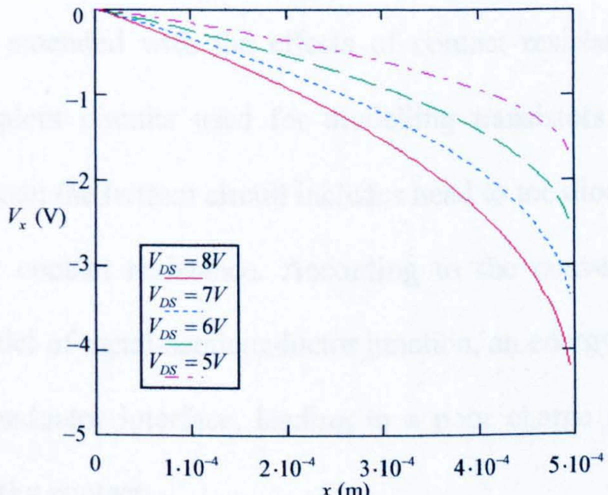

Figure 8: Surface potential along the channel

The surface potential of operating organic thin-film field effect transistors has been measured by means of scanning Kelvin probe force microscopy and reported by R. H. Friend from Cambridge [15]. It is demonstrated that the measured potential reflects the electrostatic

potential of the accumulation layer at the semiconductor/insulator interface [15]. Also it was shown that the experimentally observed drops in the surface potential above the source and drain contacts can be explained as a consequence of polymer material defects near the contacts [17]. The issue of contact resistance was hardly mentioned in papers dealing with organic TFTs because the performance of the device was so low that the current flowing was only limited by the resistance of the channel. However, with improvement of the charge-carrier mobility, limitations by contact resistance are becoming increasingly more impoartant. The model of the organic thin-film field-effect transistor needs to be amended with the effects of contact resistance. Figure 7 shows equivalent circuits used for modelling transistors with contact resistance. Note: the bottom circuit includes head to toe diodes to account for Schottky contact resistance. According to the conventional Mott-Schottky model of metal-semiconductor junction, an energy barrier at the metal-semiconductor interface, leading to a poor charge injection, will form a Schottky contact.

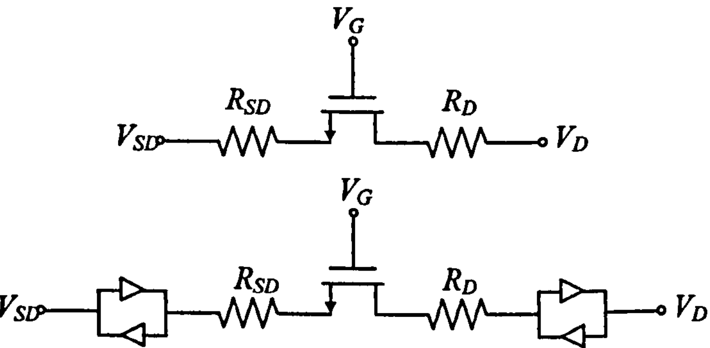

Figure 9: Equivalent circuits of a TFT including contact resistance

When including the effects for linear contact resistances, the drain current equation can be rewritten by introducing an additional voltage drop $R_C I_D$, where R_C is the contact resistance. This is done by replacing V_D with $V_D - R_C I_D$. We then have the drain current equation with contact resistance as:

$$I_D = \frac{KC_o^{(2m+1)}W}{(2\varepsilon_o\varepsilon_s kT)^m L}\left[\frac{V_G'^{2(m+1)} - (V_G' - V_D + I_D R_C)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right]. \quad (2.35)$$

After some manipulation we obtain the amended surface potential equation as:

$$V_x = V_G' + I_D R_C - \exp\left[\frac{\ln V_G'^{2(m+1)} - \frac{2\cdot(2m+1)(m+1)(2\varepsilon_o\varepsilon_s kT)^m x}{KC_o^{(2m+1)}W} I_D}{2(m+1)}\right].$$

(2.36)

The exaction of contact resistance can be done by fitting the measured surface potential with the above equation. Also a simulation result can be produced with given device parameters and contact resistance as shown in Figure 10. A more general model, with non-ohmic contact resistance that varies with the gate voltage has been studied by Street and co-workers [18]. These results showed a strong dependency of contact resistance on gate bias; an increasing gate bias will lead to

decreasing contact resistances.

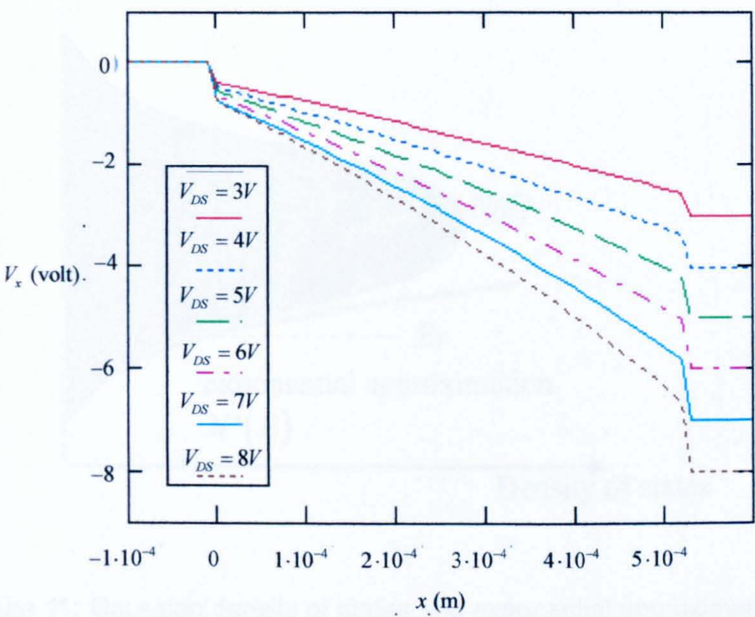

Figure 10: Surface potential in the channel with contact resistance

2.6 Temperature dependence of field effect mobility

VRH shows us that field effect mobility strongly depends on carrier concentration. To obtain the carrier concentration, i.e. the number of carriers per unit volume, in material we first evaluate the electron density in a small incremental energy range: dE. This density $n(E)$ is given by the product of the density of states $N(E)$ per unit energy, and by the probability of occupying the states $F(E)$. Thus, the carrier concentration n can be given by integrating in the whole energy range:

$$n = \int N(E) f(E) dE . \tag{2.37}$$

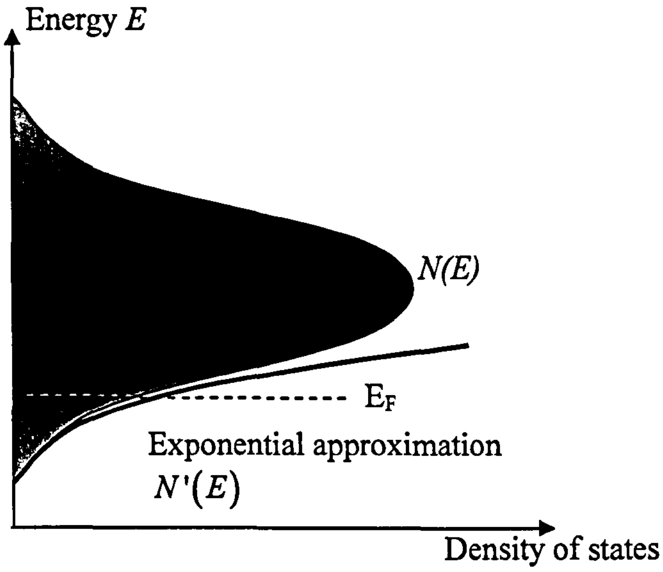

Figure 11: Gaussian density of states and exponential approximation on tail of state distribution.

In the early 1980s, the photocurrent transient spectroscopy of the density of states in amorphous semiconductor has been studied and Gaussian energy distribution has been found [19]. For a system with low carrier density in low temperature the Fermi level is in the tail states of the Gaussian which can be approximated by an exponential DOS:

$$N'(E) = N'(0)\exp\left(\frac{E}{kT_C}\right) \tag{2.38}$$

where T_C is a characteristic temperature which defines the distribution and should be independent of T. $N'(E)$ is the density of states per unit volume and energy.

The Fermi-Dirac distribution function $F(E)$ is given by:

$$F(E)=\frac{1}{1+\exp\left(\frac{E-E_F}{kT}\right)} \tag{2.39}$$

where k is Boltzmann's constant, T the absolute temperature, and E_F the Fermi energy, which is the energy with a one half probability of occupation. In the energy range for electron energies higher than the Fermi level E_F, the occupancy can be reduced to a Maxwell-Boltzmann distribution as:

$$F(E)=\exp\left(\frac{E_F-E}{kT}\right). \tag{2.40}$$

We assume the carriers which contribute to hopping via localized traps mainly occupy the energy range above the Fermi level because there are higher densities of trap. Also these traps are not fully occupied nor are they empty. The ease of hopping is much higher in this energy range.

The hopping carrier density is given as:

$$n=N'(0)\int\exp\left(\frac{E_F}{kT}\right)\exp\left(\frac{E}{kT_C}-\frac{E}{kT}\right)dE \tag{2.41}$$

if T_0 is introduced as

$$\frac{1}{T_0}=\frac{1}{T}-\frac{1}{T_C} \tag{2.42}$$

and represents an effective temperature associated with the distribution of

carriers with energy. Integrating between $E=E_F$ and $E=\infty$

$$n = N'(0)kT_0 \exp\left(\frac{E_F}{kT_C}\right). \tag{2.43}$$

Returning to (2.43) suppose $T_0 = T$, i.e. $T_C = \infty$, then:

$$n = N'(0)kT \exp\left(-\frac{E - E_F}{kT}\right). \tag{2.44}$$

This shows that all the conductions happen to be in the same energy level. For a single level, we have the well known equation for a free carrier density n_f in terms of the effective density of states N_C:

$$n_f = N_C \exp\left(-\frac{E_C - E_F}{kT}\right) \tag{2.45}$$

so that $N'(0)(-kT) = N_C$. For the general case where the carriers are not confined to a small energy range we can write:

$$\sigma = n_f q \mu_f \tag{2.46}$$

The mobility of the free carrier can be attainted by comparing VRH with the conductivity in band-type semiconductor:

$$\sigma = N_C \exp\left(-\frac{E_C - E_F}{kT}\right) q\mu_f \, . \tag{2.47}$$

The effective mobility μ_{hop} (which in this case is the hopping mobility) can be obtained by comparing VRH with the conductivity in band-type

semiconductor:

$$\mu_{hop} = \frac{\mu_f N_C \exp\left(-\frac{E_C}{kT}\right)}{\left[N(0)kT_0\right]^{\frac{T_C}{T}}} \cdot n_{hop}^{\left(\frac{T_C}{T}-1\right)} = K \cdot n_{hop}^{\ m} \tag{2.48}$$

where

$$m = \frac{T_C}{T} - 1 \tag{2.49}$$

and

$$K = \frac{\mu_f N_C \exp\left(-\frac{E_C}{kT}\right)}{\left[N(0)kT_0\right]^{\frac{T_C}{T}}} \, . \tag{2.50}$$

Therefore the drain current equation when considering temperature effect can be rewritten as:

$$I = \frac{\mu_f N_C \exp\left(-\frac{E_C}{kT}\right)}{\left[N(0)kT_0\right]^{\frac{T_C}{T}}} \frac{C_o^{(2\frac{T_C}{T}-1)} W}{(2\varepsilon_o \varepsilon_s kT)^{\frac{T_C}{T}-1} L} \left[\frac{V_G'^{\,2\frac{T_C}{T}} - (V_G' - V_D)^{2\frac{T_C}{T}}}{2 \cdot \left(2\frac{T_C}{T} - 1\right) \frac{T_C}{T}} \right] . \tag{2.51}$$

The equation implies that an increasing temperature leads to an increasing drain current.

2.7 Hysteresis instability

An important point of concern of organic devices is their stability. For organic devices, there are several forms of the instabilities which affect their performance and which have been observed and reported, such as bias stress and threshold voltage shifting in transistor. Organic field-effect transistors using PTAA as semiconductor layer and anodic alumina as gate dielectric have been studied and reported by L. A. Majewski et al. [20] The output characteristics during ramping up and down is compared and shown in Figure 12, revealing moderate hysteresis ($\Delta I_D / I_D < 10\%$). The occurrence of hysteresis effects is one of the problems of organic device which is getting more critical when reducing the threshold voltage.

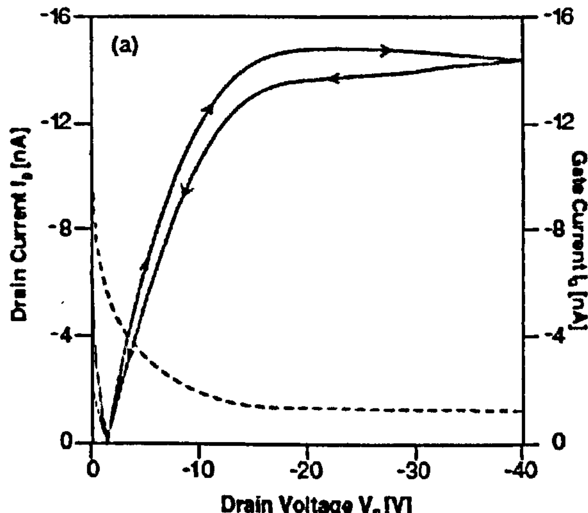

Figure 12 (—) Output hysteresis and (---) gate leakage current I_G against V_D, at $V_G = -20$ V [20]

Hysteresis may be due to both traps filling at the polar insulator surface and/or electret properties of the insulator bulk. A small number or ions, or highly polar $Al(OH)_3$, has to be expected in anodised Al films. Also the asymmetric diffusion of dopant in organic semiconductor is also suggested to be one of the causes for the hysteresis effects. Similar phenomena are observed in non-anodic SiO_2-based transistors as well, and are often referred to as 'gate bias stress'. However a detailed understanding of the hysteresis effects in organic semiconductor/insulator structure and a full list of the surface/space charges components associated with these effects are still lacking. Moreover, chemical effects from defects and impurities in semiconducting polymer and the impact of increased temperature on hysteresis which are still mostly unknown and very often ignored in the literature.

The various types of charges and states associated with polymer-aluminium oxide system are summarized in Figure 13; this information should be used as a guideline for future experiments and data attraction. They include fast surface sates located at the oxide-polymer interface mainly because of the disruption of the band gap systems. In addition, there may be space charges present within the oxide layer due to mobile impurity ions or due to traps in disordered Al_2O_3 and dipolar $Al_2(OH)_3$ fixed at oxide surface.

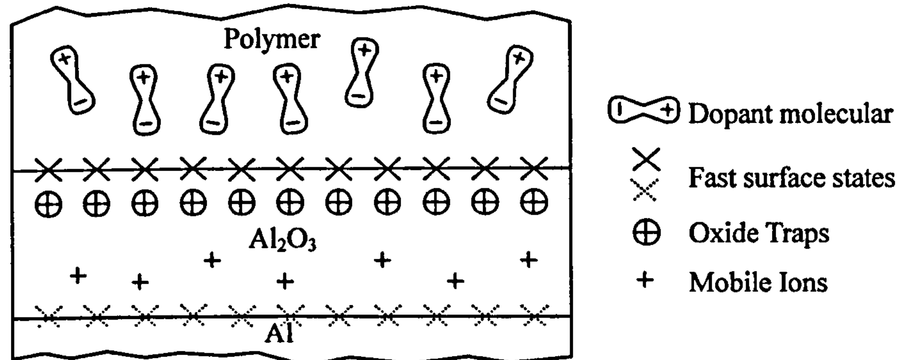

Figure 13 Charges and states associated with Al-Al_2O_3-Polymer structure

In recent reports from Prof. D. M. Taylor's group [21], MIS capacitors based on organic semiconductors have been studied by applying the conductance technique advocated by Nicollian and Goetzberger [22], in order to identify the source of the threshold voltage instability in polymer transistor. The dopant density in the semiconductor and the trapped charge density at the interface were measured after annealing in vacuum for different times. The result shows that annealing the devices under vacuum decreases the concentration of deep traps which were considered that these were more likely to affect the threshold voltage and field-effect mobility in transistors [21].

The hysteresis effect on circuits can be profound especially when higher specifications, such as high speed and stability, are usually demanded by much of the market. Therefore polymer circuit design with fault tolerance on the instable device parameters is required with

sacrifices of a lower off/on current ratio and a lower operating speed, the effects of the device instability can be avoided to a minimum level.

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Chapter 3

POLYMER CIRCUIT CALCULATION AND SIMULATION

A selection of subcircuits is introduced in the first half of this chapter. These subcircuits include the TFT switch, current source/mirror and active resistor. Subcircuits offer a reusable and quick way of constructing a circuit. The study on these subcircuits also shows the requirement of the organic device to improve the circuit performance. Inverters with different loads and voltage bootstrapping are analyzed in the second half of this chapter. The impact of the leakage currents via the parasitic resistances among transistors will be analysed together with the simulation results in MathCAD.

3.1 TFT SWITCH

As a basic component, the switch is used in many applications in integrated-circuit design, such as multiplexing, modulation and transmission gate in digital circuit. Demonstrated by Cambridge Display Technology Ltd., a UK-based pioneer of polymer light emitting diode (P-OLED) technology, TFT switches have been successfully used in their active matrix polymer LED (AMPLED) display for addressing. Each pixel in the LED matrix has been driven by one TFT switch, and the control signals of the TFT switch are programmed to control the brightness of individual pixels. Similar work is also presented by other research groups, such as Philips [1], [2].

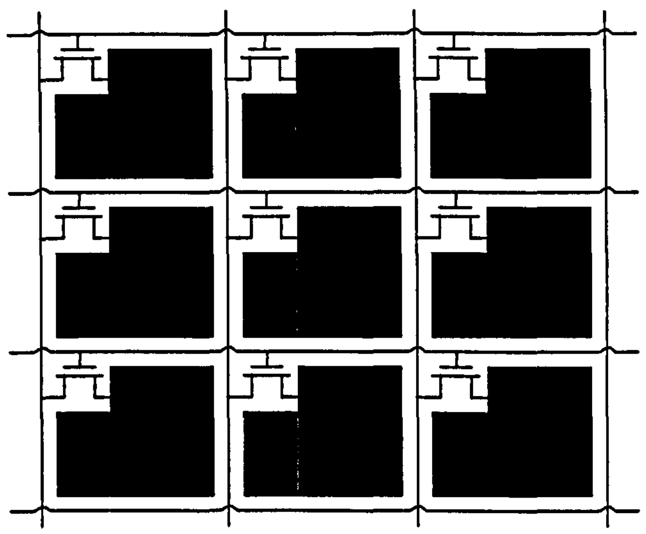

Figure 1: Active matrix polymer LED driven by TFT switches

The characteristics of the switch that are compatible with polymer electronics are studied in this section. Figure 2 shows a voltage controlled switch and its non-ideal model.

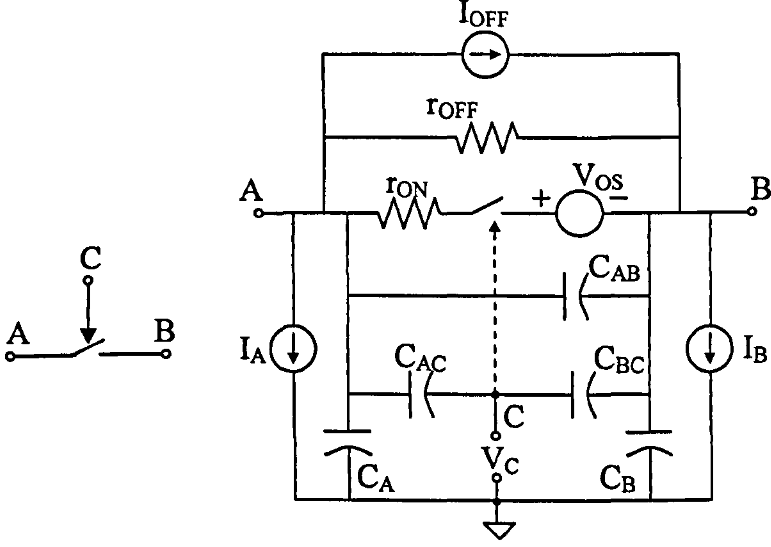

Figure 2: Symbol and non-ideal model for voltage controlled switch

The main TFT parameters of a switch are its ON resistance, r_{ON}, and its OFF resistance, r_{OFF}. The state of the switch is controlled by the voltage V_C. For an ideal case, when the switch is on, terminal A and B should be short-circuited, which requires ON resistance to be zero, and when the switch is turned off, the OFF resistance between terminal A and B should be infinite. However the reality is that the ON resistance is never zero and the OFF resistance is never infinite.

When a TFT transistor is turned on as a switch, the voltage drop across the transistor should be small and the gate voltage large. Therefore, the ON resistance of the transistor switch is equal to the channel resistance in the non-saturation region:

$$r_{ON} = \frac{V_{DS}}{I_D} = \frac{1}{I_D / V_{DS}}. \tag{3.1}$$

Applying the drain current equation of the polymer transistor, we have:

$$r_{ON} = (2m+1)\frac{(2\varepsilon_o \varepsilon_s kT)^m L}{K C_o^{(2m+1)} W} \cdot \frac{1}{(V_{GS} - V_T - V_D)^{2m+1}}. \tag{3.2}$$

Figure 3 shows the drain current of a polymer transistor as a function of a voltage across the drain and source terminals. This diagram is plotted by MathCAD for equal increasing steps of V_{GS} (0V – 6V) for W/L=100/1.

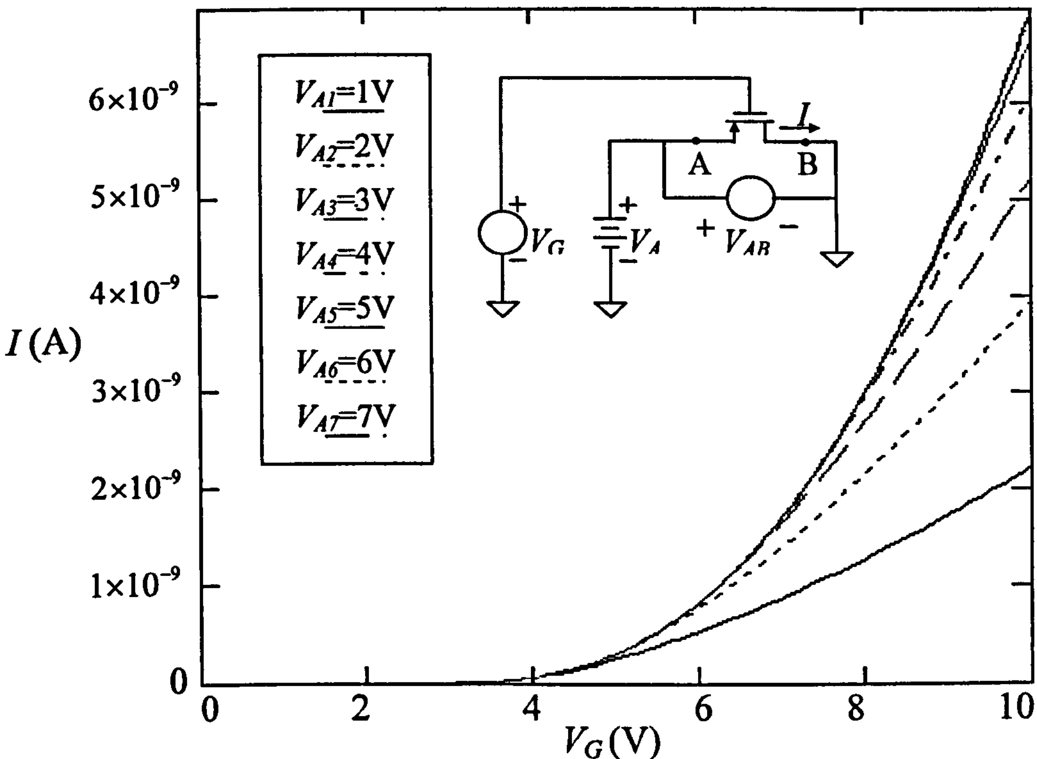

Figure 3: I-V characteristic of a polymer transistor operating as a switch

In Figure 4, ideal r_{ON} as a function of V_{GS} is shown for different channel width-length ratios. r_{ON} approaches infinity when V_{GS} approaches V_T and decreases with larger W/L. When V_{GS} is less than V_T, the switch is turned off. The performance of the OFF state depends on the drain-bulk and source-bulk currents and also the sub-threshold current from drain to source.

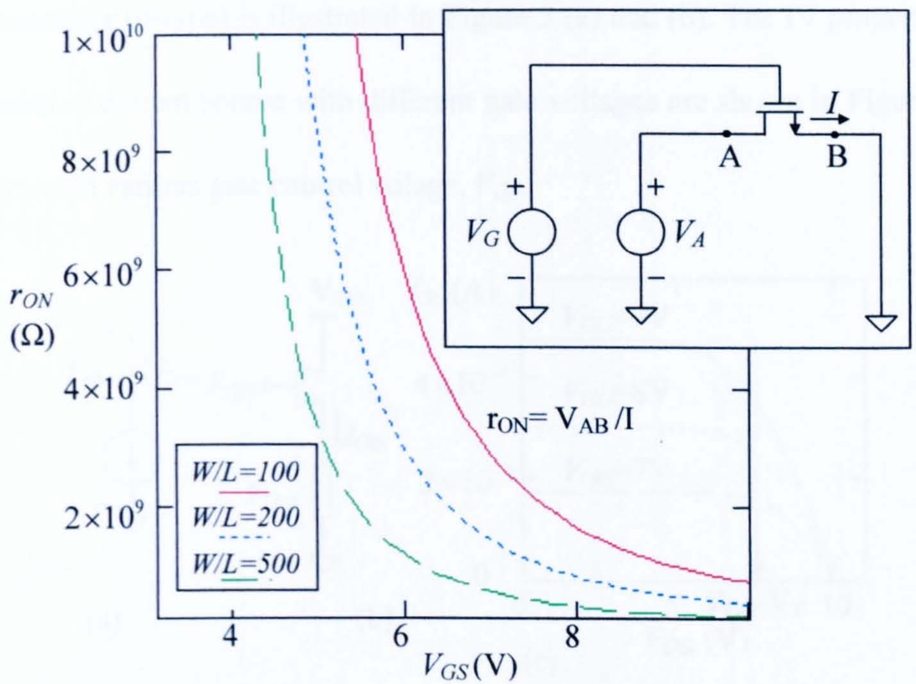

Figure 4: Illustration of ON resistance for different aspect ratio

3.2 Simple transistor current source

An ideal current source is a concept used in network theory and analysis. It delivers or absorbs electrical energy such that the electrical current is independent of the voltage across its terminals. The voltage across an ideal current source is completely determined by the circuit connected to the source. However this kind of ideal current source does not exist and the TFT current source is treated as non-ideal; it has finite output. The symbol of current source and its configuration with a n-type

transistor (n-type) is illustrated in Figure 5 (a) and (b). The IV properties with of current source with different gate voltages are shown in Figure 5 (c) with various gate control volage, V_{GG}.

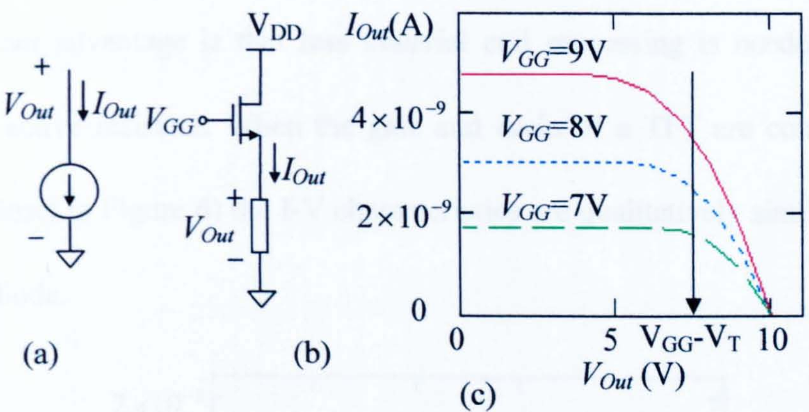

Figure 5: Current source with n-type polymer TFT transistor

When $V_{out} < V_{GG} - |V_T|$, the transistor is ideally turned off and the drain current remains constant. The output current equals to the OFF current of the transistor, $I_{out} = I_{OFF}$.

3.3 Active resistor

As essential components, TFT based active resistors are widely used in integrated circuits with the advantages of smaller required space. Another advantage is that less material and processing is needed with TFT active resistors. When the gate and drain of a TFT are connected (see inset in Figure 6) the I-V characteristics are qualitatively similar to a p-n diode.

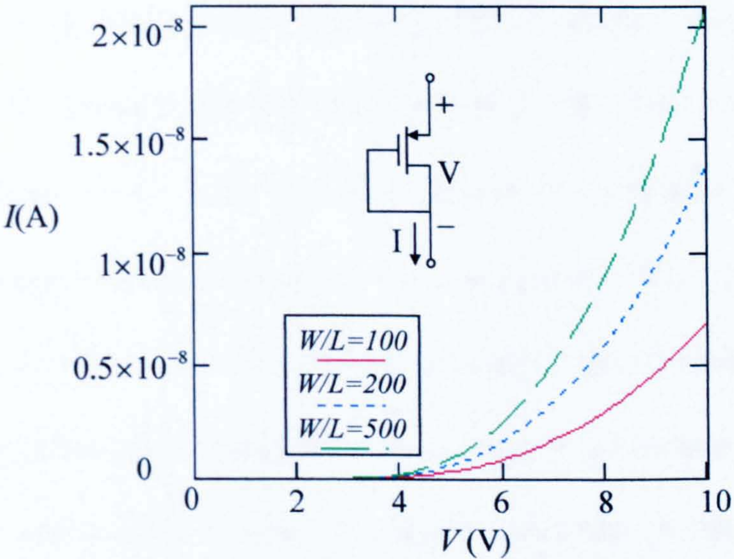

Figure 6: P-channel active resistor and its I-V characteristics

When the drain of the transistor is connected to the gate, the drain current is controlled by the gate voltage. Therefore this TFT transistor can be viewed as a nonlinear resistor and the resistance between source and drain terminals can be found from the equation for the drain current of

the saturated TFT transistor with $V_{GS} = V_{DS}$:

$$V = V_T + \left[2 \cdot (2m+1)(m+1) \frac{(2\varepsilon_o \varepsilon_s kT)^m}{KC_o^{(2m+1)}} \cdot \frac{L}{W} \cdot I \right]^{\frac{1}{2(m+1)}} . \quad (3.3)$$

3.4 Current mirrors

It could be a problem to generate a constant and accurate current using a fixed reference voltage because of different working temperatures and various manufacturing processes. If temperature increases, both threshold voltage V_{th} and mobility μ are changed and this will introduce significant errors. These are quite different in behaviour for highly disordered polymers compared with crystalline silicon. The current mirror is widely used in analogue circuits and A/D modules. This is important because it is expected that the mixed signal circuits will have a major role to play in polymer organic electronics. It duplicates the reference current, which is either generated by a complex circuit on chip or via input from a dedicated current source. A basic current mirror using two transistors connected in parallel is shown in Figure 7. These two transistors operate in saturation mode with the same gate-source voltage:

$$V_{GS1} = V_{GS2} = V_{DS1} . \quad (3.4)$$

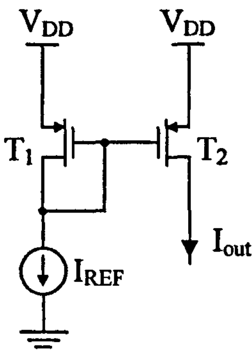

Figure 7: Basic TFT current mirror

Assuming the threshold voltages of the transistors are the same, $V_{T1} = V_{T2} = V_T$, we have the drain current of the saturated transistors as:

$$I_{REF} = \frac{KC_{OX}^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W_1}{L_1}\right)\left[\frac{(V_{GS}-V_T)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right], \tag{3.5}$$

$$I_{out} = \frac{KC_{OX}^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W_2}{L_2}\right)\left[\frac{(V_{GS}-V_T)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right]. \tag{3.6}$$

Combining Equation (3.5) and (3.6), the output current:

$$I_{out} = I_{REF}\frac{W_2/L_2}{W_1/L_1}. \tag{3.7}$$

Thus I_{out} will be a multiple of I_{REF}, and the scaling constant $K_{scaling} = \frac{I_{out}}{I_{REF}}$ is determined by the transistors' geometry. In practice the output of the current mirror has finite output resistance: I_{out} will be a function of V_{out}.

3.5 Pass transistor

A Pass transistor behaves as an analogue switch. The result is that a logic 0 on the control input causes the pass transistor to have a high resistance, so that the switch is off, and a logic 1 on the input causes the pass transistor to have a low resistance. By applying a clock signal on the control terminal, input signal is periodically repeated on the output terminal. This sub circuit can be used in memory circuits and LED circuits, such as shift registers.

As an analogue switch, the following important parameters of the pass transistor need to be considered.

(1) On-resistance: the resistance of the pass transistor when switched on.

(2) Off-resistance: the resistance of the pass transistor when switched off.

(3) Signal range: the minimum and maximum voltages allowed for the signal to be transmitted. If this is exceeded, the switch may be destroyed by excessive currents. If the current is too small then it may be lost in noise.

There are many factors that affect on-resistance R_{ON} such as temperature, input voltage, supply voltage, and gate length. The value of R_{ON} can be derived by taking the partial derivative of I_D over V_{DS}. If the Width/Length ratio is increased in order to reduce R_{ON}, then the parasitic capacitance of the gate oxide will increase proportionately resulting in lower bandwidth.

A simple example of a pass transistor is shown in Figure 8. Pass transistor MP is driven by the periodic clock signal and acts as an access switch to either charge or discharge the parasitic capacitance C_x, depending on the input signal V_{in}. Thus, the two possible operations when the clock signal is active (CK=1) are the logic "1" transfer (charging the capacitance C_x to a logic-high level) and logic "0" transfer (discharging the capacitance C_x to a logic-low level).

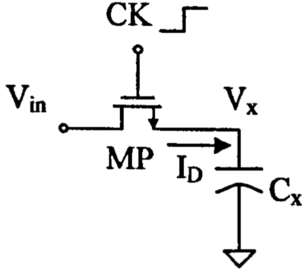

Figure 8: Pass transistor charged up by periodic clock signal

First we consider the charging process, assuming that the capacitor voltage is 0 initially; $V_x(t=0)=0\ \text{V}$. A logic '1' is applied to the input which corresponds to $V_{in}=V_{OH}=V_{DD}$. When the clock signal at the gate of the pass transistor rises from 0 to V_{DD}, the pass transistor starts to conduct and will operate in the saturation region of this cycle. The capacitor is charged up through the pass transistor operating in the saturation region. Note that with a polymer (as other TFT devices) there is no substrate connection so none of the charge is lost through this route. Also there is no back-bias effect on the source junction as C_x charges. We have:

$$C_x\frac{dV_x}{dt}=\frac{KC_o^{(2m+1)}W}{(2\varepsilon_o\varepsilon_s kT)^m L}\left[\frac{\left(V_{DD}-V_x-V_T\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right]. \tag{3.8}$$

Integrating the above equation, we have the charging time *t'* for a certain voltage V_x' as:

$$t'=2C_x(2m+1)(m+1)\frac{\left(2\varepsilon_0\varepsilon_s kT\right)^m L}{KC_o^{(2m+1)}W}\int_0^{V_x'}\frac{dV_x}{\left(V_{DD}-V_x-V_T\right)^{2(m+1)}} \tag{3.9}$$

Solving the equation, we can find the capacitor voltage as a function of time, $V_x(t)$. The simulation result from MathCAD is shown in Figure 9.

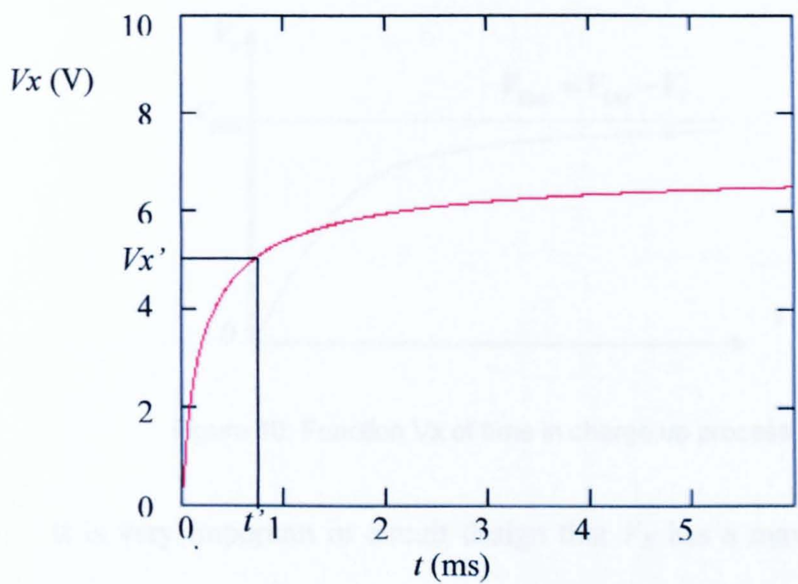

Figure 9: Simulation of charging process via pass transistor

The expression (3.9) of charging time can be simplified when $m = 0$.

$$\begin{aligned} t' &= 2C_x \frac{L}{KC_oW} \int_0^{V_x'} \frac{dV_x}{\left(V_{DD} - V_X - V_T\right)^2} \\ &= 2C_x \frac{L}{KC_oW} \left[\left(\frac{1}{V_{DD} - V_X' - V_T} \right) - \left(\frac{1}{V_{DD} - V_T} \right) \right] \end{aligned} . \tag{3.10}$$

The function of changing voltage can be found as:

$$V_x(t) = \left(V_{DD} - V_T\right) \frac{\left(\frac{KC_0W\left(V_{DD} - V_T\right)}{2C_xL} \right)t}{1 + \left(\frac{KC_0W\left(V_{DD} - V_T\right)}{2C_xL} \right)t} . \tag{3.11}$$

As shown in Figure 10, the voltage rises from 0 V and for large t will approache a maximum limit given by:

$$V_{\max} = V_{DD} - V_T . \tag{3.12}$$

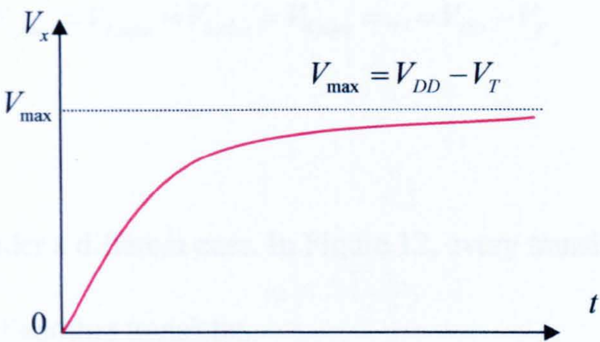

Figure 10: Function Vx of time in charge up process

It is very important in circuit design that V_X has a maximum limit which is less then the control input by V_T. For example, a logic '1' is transferred through several transistors in series as shown in Figure 11.

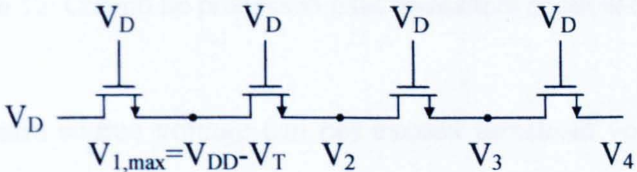

Figure 11: Logic '1' transferred in a series of transistors

To simplify this circuit, every internal node voltage is set to be 0 V initially. The first transistor is working in saturation mode as explained above. The second one and the others are working in critical saturation mode. Thus, no matter how many pass transistors are in the series, the maximum limit voltages are equal:

$$V_{1,\max} = V_{2,\max} = V_{3,\max} = V_{4,\max} = \ldots = V_{DD} - V_T \quad (3.13)$$

Let's consider a different case. In Figure 12, every transistor is driven by the output of another transistor.

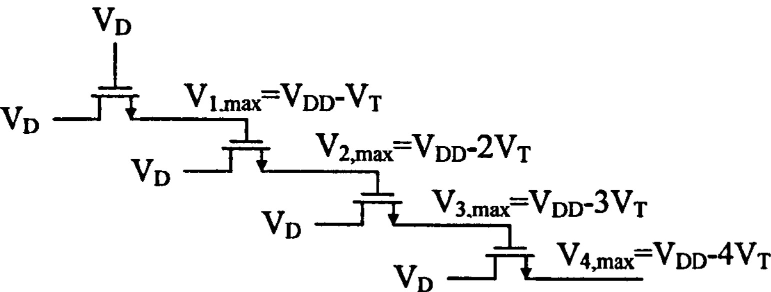

Figure 12: Charge up process in pass transistors controlled by others

The drain source voltage can not exceed threshold voltage, in other words, voltage decreases at every stage.

To analyze the discharge process, we assume the capacitor voltage is logic '1': $V_x(t=0) = V_{\max} = V_{DD} - V_T$. A logic '0' is applied on the input of the pass transistor $V_{in} = 0\text{V}$. At the time $t = 0$, the clock signal turns on the pass transistor with a control input rising from 0 to V_{DD}. The capacitor is discharged by the transistor and the current flow is in the opposite direction of the charge process as shown in Figure 13.

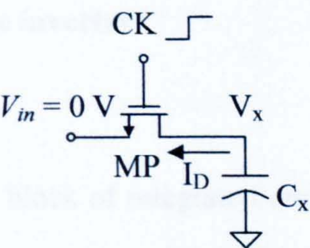

Figure 13: Discharge process through a pass transistor

This means the x node can be regarded as the drain electrode of the transistor and its operation mode can be found from the voltages $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD} - V_T$. Condition $V_{DS} \le V_{GS} - V_T$ is satisfied in the whole discharge process, thus the pass transistor works in a linear mode and discharge time can be found from the current equation or simulation result with MathCAD shown in Figure 14.

$$-C_x \frac{dV_x}{dt} = \frac{KC_o^{(2m+1)}W}{(2\varepsilon_o \varepsilon_s kT)^m L}\left[\frac{\left(V_{DD}-V_T\right)^{2(m+1)} - \left(V_{DD}-V_T-V_x\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right]. \quad (3.14)$$

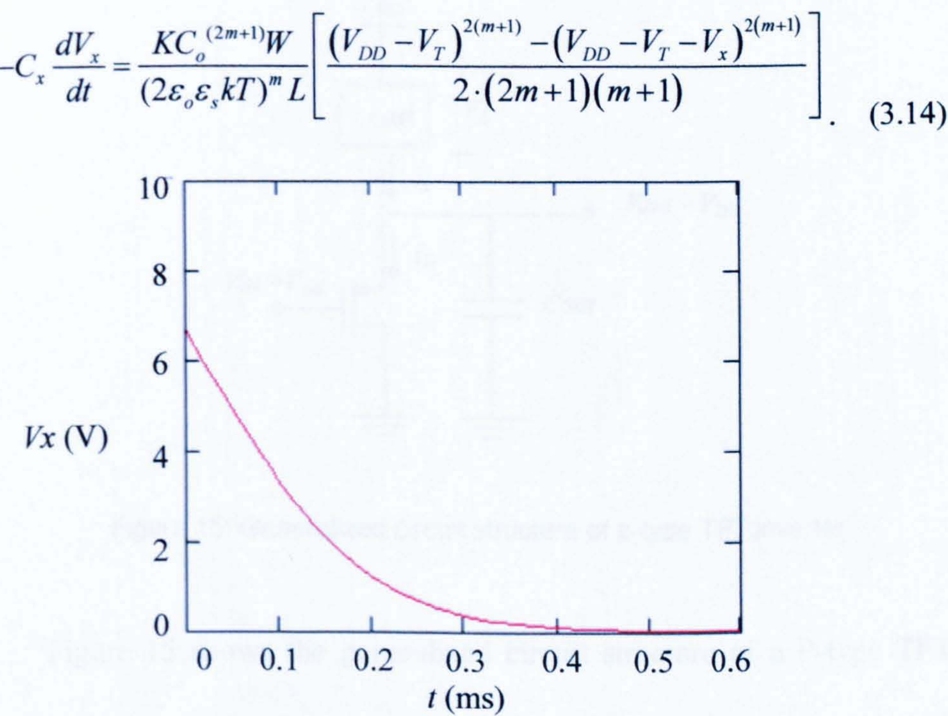

Figure 14: Simulation result of discharging via transistor

3.6 Analysis of the inverter

The basic building block of integrated circuit is the inverter gate. It performs a Boolean operation on a single input variable as the most fundamental TFT logic gate. The inverter design analysis is similar to more complex logic circuits, such as NAND and NOR gates. It therefore forms a significant basis for digital circuit design. The basic characteristics of various TFT inverter circuits will be discussed and analyzed in this section, focusing on the link between device characteristics and circuit performance.

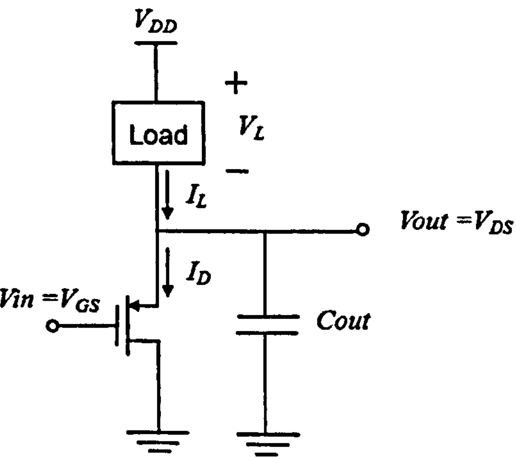

Figure 15: Generalized circuit structure of p-type TFT inverter

Figure 15 shows the generalized circuit structure of a P-type TFT inverter. The input voltage of the inverter circuit is also the gate-to-source

voltage of the P-type TFT transistor ($V_{in} = V_{GS}$), while the output voltage of the circuit is equal to the drain-to-source voltage ($V_{out} = V_{DS}$). The load device is represented as a two-terminal circuit element with terminal current I_L and terminal voltage V_L. One terminal is connected to V_{DD}, the power supply voltage.

The output terminal of the inverter shown in Figure 15 is connected to the input of another TFT inverter. Consequently, the next circuit can be represented as a capacitance, C_{out}. Since the DC gate current of a TFT transistor is negligible for all practical purposes, there will be no current flow into or out of the input and output terminals of inverter in DC steady state.

For this simple circuit, we see the load current is always equal to the drain current:

$$I_D(V_{in}, V_{out}) = I_L(V_L) \quad (3.15)$$

The voltage transfer characteristic describing V_{out} as a function of V_{in} under DC conditions can then be found by analytically solving the above equation for various input voltage values.

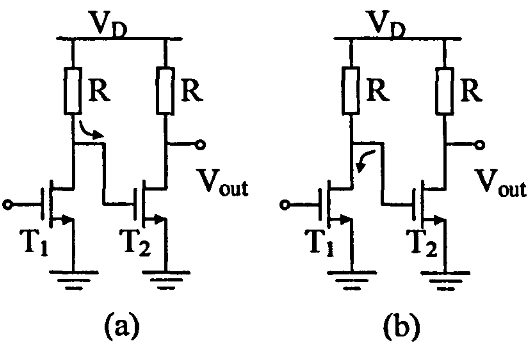

Figure 16: Charge and discharge in cascaded inverters with resistor loads

A key performance indicator of an inverter is the switching speed; the sum of discharging delay and charging delay. It is more common and simple to estimate circuit performance in terms of mobility, although in polymer circuits, this will introduce errors by neglecting the fact that effective mobility varies with the oxide thickness. In circuit design and calculation, mobility is considered more important than a physical fact.

Consider a simple inverter with a resistor load driving a second identical inverter as shown in Figure 16.

The gate of the enhancement transistor T_2 is assumed to be charged and the output voltage, V_{out} is therefore low. Suppose the idealised transistor T_1 is now turned on without delay so that it discharges T_2 as

shown in Figure 16 (b). The discharge time τ_D for T_2 is found to be proportional to gate overlap capacitance plus spurious capacitance and inversely proportional to the discharge current *I*.

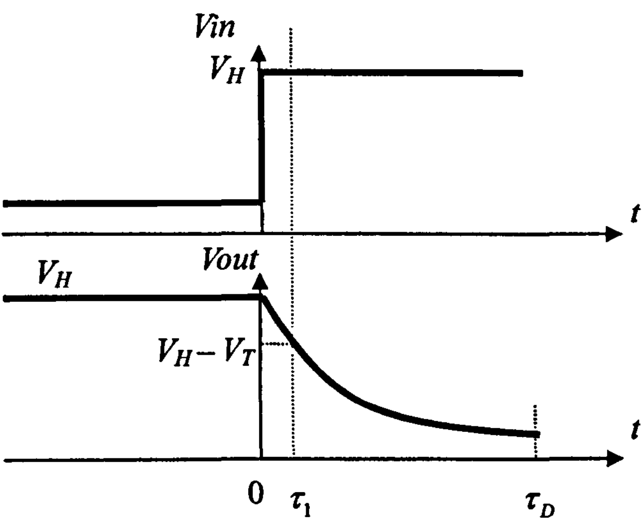

Figure 17: Timing diagram of discharge process in TFT inverter

In the discharge process 0-τ_1, the transistor T1 is working in saturation mode. The threshold voltage V_T is much smaller then the highest output voltage V_H and the transistor works in linear region in the time period τ_1 - τ_D with a deceasing drain current, therefore the time period 0 - τ_1 is much shorter than the time period τ_1 - τ_D and can be neglected. Suppose an idealized transistor T1 is discharged by another identical transistor T2. The gate charge Q_D is proportional to the product of the channel area and the capacitance per unit C_o, i.e., $Q_D \propto C_o WL$.

Therefore the discharge time of gate capacitor can be simplified as:

$$\tau_D = \frac{Q}{I_D} \propto \frac{C_o WL}{C_o \mu W / L} = \frac{L^2}{\mu}. \qquad (3.16)$$

This shows the origin of the concern about the value of the equivalent mobility.

The characteristics of the inverter circuit actually depend very strongly upon the type and the characteristics of the load device. Although there are several types of inverter configuration with different load devices that can be used in silicon circuits, the CMOS inverter is the most popular and successful. The options for the organic inverter are very limited. Ideally organic complementary inverters have lower power consumption and better noise margins [3], [4]. However the field-effect mobility of the current n-channel TFT is much lower than that of the p-channel TFT. Two circuit configurations of the inverter have been widely used in current organic circuits using p-type organic materials and are presented in Figure 18. [5] [6]

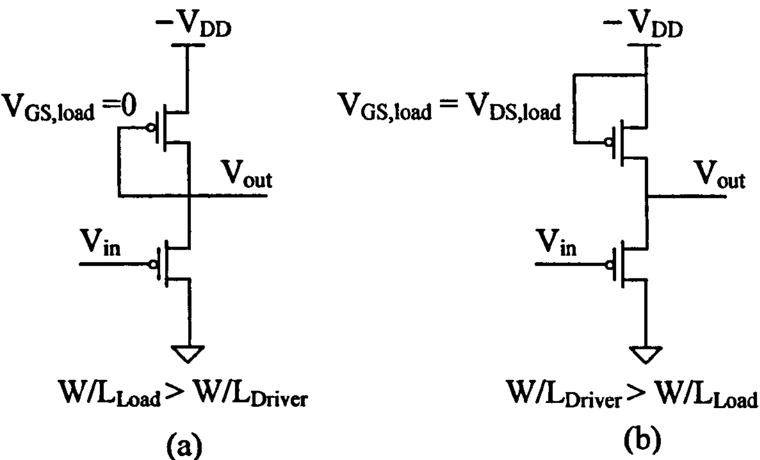

Figure 18: Schematic of "$V_{GS} = 0$" inverter (a) and saturated load inverter (b)

Figure 18 (a) shows the circuit configuration of inverter using "V_{GS}= 0" logic. The source of the load transistor has been connected to the gate. Note that the load transistor is chosen to be wider than the driver transistor. When the input $V_{in} = 0V$, the output begins with $0V$, i.e. the gate voltage of driver and of the load are both zero. The load transistor however, is wider and can supply a higher current than the driver. As the current in the two transistors must remain the same, the drain voltage of the load transistor will have to decrease, and so the output node will be pulled down towards $-V_{DD}$ obtaining a low output. When the input is low, $V_{in} = -V_{DD}$, the driver transistor is turned on and the output will be pulled up against the small current provided by the load.

The key indicator of inverter performance is the switching speed, which depend on the sum of the delays related to pull-down and pull-up. In "V_{GS}= 0" logic, the switching speed is relatively low, limited by the pull-down delay as the low pull-down current provided by the load is much smaller than the transient pull-up current provided by the driver transistor. Therefore the second circuit configuration of the inverter; saturated load inverter as shown in Figure 18 (b), is used to increase the switching speed. In this circuit configuration, the driver is wider than the load transistor. When the input is low ($V_{in} = -V_{DD}$), the gate voltages of the driver and the load transistors are initially equal to $-V_{DD}$ and the output voltage starts increasing because the driver transistor is wider than the load transistor. The width ratio is normally taken as about 10. On the other hand, when the input is high ($V_{in} = 0V$), the load transistor will be at first heavily turned on and pull down the output node against the driver, which is almost off. The switch speed is increased considerably, as the pull down current is provided by the load transistor that is fully on. One of the drawbacks of this is that the inverter has an asymmetric input-output characteristic because the driver transistor is larger than the load and could have positive threshold, which happens in some of the p-type polymer transistors. To overcome this, an additional stage of two

identical FETs, which is called level shifter, can be used to adjust the threshold voltage of the driver transistor to negative values and make the inverter more symmetrical. The schematic of the saturated load transistor with level-shifter is shown in Figure 19. By setting the shifting voltage V_{SS} as a positive value, the input-output characteristics shift by V_{SS}.

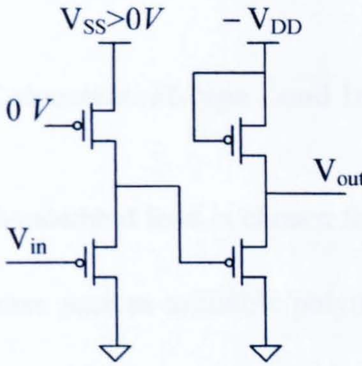

Figure 19: Schematic of saturated load inverter with level-shifter

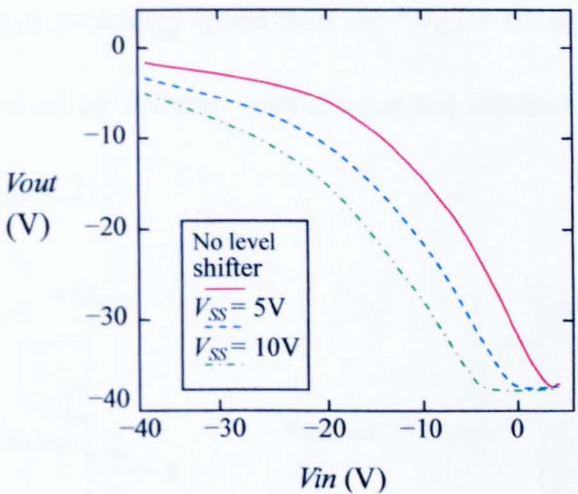

Figure 20: Transfer characteristic of saturated load inverters with level shifters

This inverter is more stable than the "$V_{GS}=0$" inverter; the driver

transistor and the load transistor stress equally during the pull-up and pull-down cycles. However, this doubles the number of transistors. Therefore, in the following discussion we will only focus on the saturated enhancement-type load inverter which has a negative threshold voltage. The modelling based on the new equation is given in the next section.

3.7 Saturated Enhancement-type Load Inverter

The saturated enhancement load is chosen for further polymer circuit studies not only because present available polymer transistor technology is mainly based on p-type polymer transistor, but also because it has a relative higher switching speed than the "$V_{GS} = 0$" inverter. The circuit configuration of an inverter with a saturated enhancement-type load is shown in Figure 21.

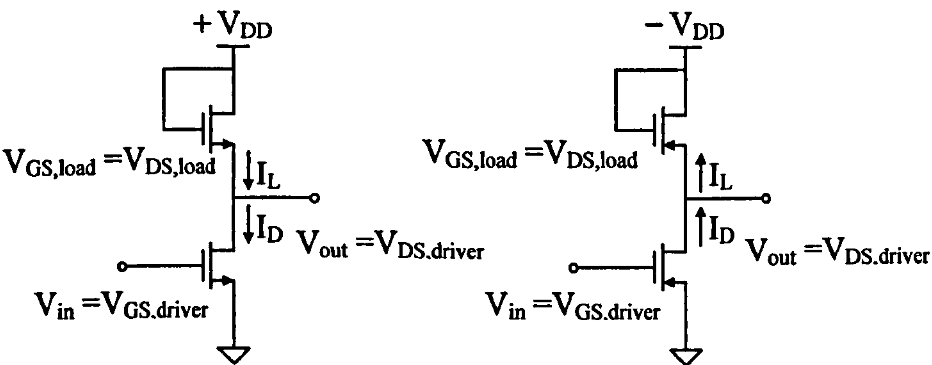

Figure 21: Saturated enhancement-load inverter circuits based on (a) n-channel and (b) p channel transistor

For the load transistor, the condition of saturation is always satisfied, hence the load transistor operates in the saturation region as long as it is on. The load current can be expressed as:

$$I_{D,load} = \frac{KC_o^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W}{L}\right)_{load}\left[\frac{\left(V_{DD}-V_{out}-V_T\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right]. \quad (3.17)$$

For input voltages smaller than V_T, the driver transistor is cut-off and does not conduct a drain current. In this case, the output (high) voltage level is determined by the load transistor. As the input voltage is increased beyond V_T, the driver transistor starts conducting a nonzero drain current, initially in saturation mode. Since the current is equal to the load current in steady-state, i.e., $I_{D,driver}=I_{D,load}$:

$$\frac{KC_o^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W}{L}\right)_{load}\frac{\left(V_{DD}-V_{out}-V_T\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)} = \frac{KC_o^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W}{L}\right)_{driver}\left[\frac{\left(V_{in}-V_T\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right], \quad (3.18)$$

$$V_{out} = V_{DD}-V_T-\left[\frac{(W/L)_{driver}}{(W/L)_{load}}\right]^{\frac{1}{2(m+1)}}\left(V_{in}-V_T\right). \quad (3.19)$$

The output voltage level starts to decrease with increasing input voltage, and the driver transistor enters the linear operating region:

$$\frac{KC_o^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W}{L}\right)_{load}\frac{\left(V_{DD}-V_{out}-V_T\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}=$$
$$\frac{KC_o^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W}{L}\right)_{driver}\left[\frac{\left(V_{in}-V_T\right)^{2(m+1)}-\left(V_{in}-V_T-V_{out}\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right]. \tag{3.20}$$

The typical DC voltage transfer characteristic (VTC) of the saturated enhancement-inverter circuit is shown in Figure 22.

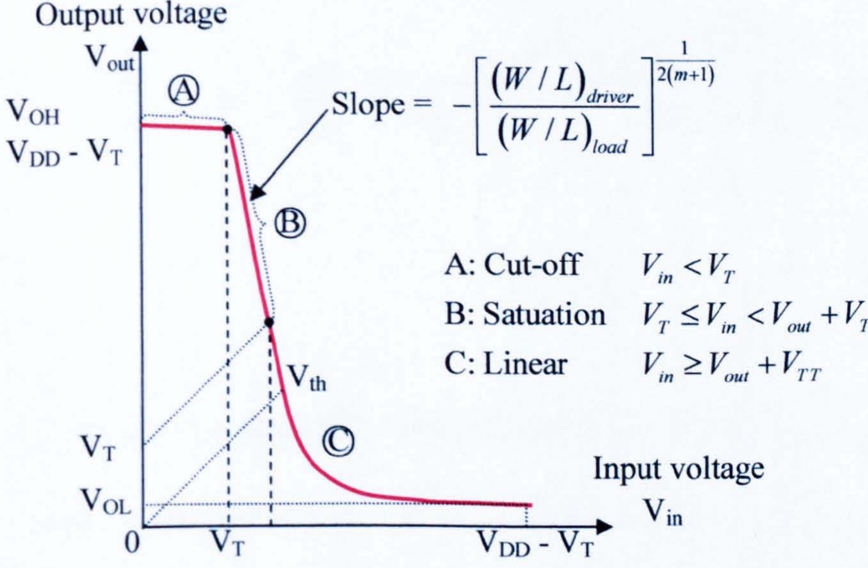

Figure 22: VTC of the saturated enhancement-inverter circuit

When input voltage of the inverter is $V_{in} = V_{DD} - V_T$, the output voltage should be much lower than the threshold voltage in order to turn off the next-stage inverter. Therefore, the transistor dimension ratio between driver transistor and load transistor can be found as:

$$\frac{KC_o^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W}{L}\right)_{load}\frac{\left(V_{DD}-V_{OL}-V_T\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)} =$$
$$\frac{KC_o^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W}{L}\right)_{driver}\left[\frac{\left(V_{DD}-2V_T\right)^{2(m+1)}-\left(V_{DD}-2V_T-V_{out}\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right]$$

(3.21)

$$k_R = \frac{k_{driver}}{k_{load}} = \frac{(W/L)_{driver}}{(W/L)_{load}} = \frac{\left(V_{DD}-V_{OL}-V_T\right)^{2(m+1)}}{\left(V_{DD}-2V_T\right)^{2(m+1)}-\left(V_{DD}-2V_T-V_{out}\right)^{2(m+1)}}.$$

(3.22)

The inverter threshold voltage is defined as $V_{th} = V_{in} = V_{out}$. From voltage transfer characteristic (VTC) shown in Figure 22, we can find this threshold voltage in linear region by solving the following equation:

$$\left(\frac{W}{L}\right)_{load}\left(V_{DD}-V_{th}-V_T\right)^{2(m+1)} = \left(\frac{W}{L}\right)_{driver}\left(V_{th}-V_T\right)^{2(m+1)} \quad . \quad (3.23)$$

The value of V_{OL} is determined by the voltage divider formed by the resistance of the drive transistor with V_{GS}=0 and the resistance of the load transistor with V_{GS}=0. Thus, the separation of logic levels depends mainly on the ratio between the width of the load and of the driver transistor, if they have the same length. The chosen ratio should be large enough (K_R>10) to ensure that the distance between the logic high and low level is close to the bias voltage V_{DD}, and its subsequent inverters can be switched on/off without losing logic integrity.

The dynamic behaviour of the inverter essentially determines the overall operating speed of digital system. The question of the inverter's dynamic response is reduced to finding the charge-up and charge-down times of a single load capacitance, which is charged and discharged through one transistor. Figure 23 shows a schematic of a saturated load inverter with a capacitor load.

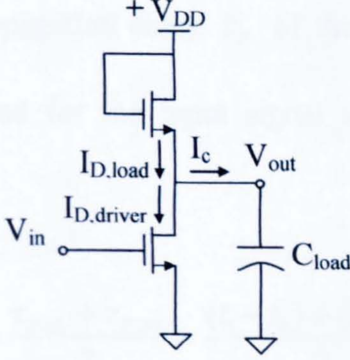

Figure 23: Schematic of a saturated enhancement-load inverter

The delay time definitions are briefly presented before we start the derivation of delay time. Figure 24 shows the input and output voltage waveforms of a typical inverter circuit. By definition, the propagation delay time τ_{PHL} is the time required for the output voltage to fall from V_{OH} to V_{th}, and τ_{PLH} is defined as the time required for the output voltage to rise from V_{OL} to V_{th}, assuming a falling pulse input.

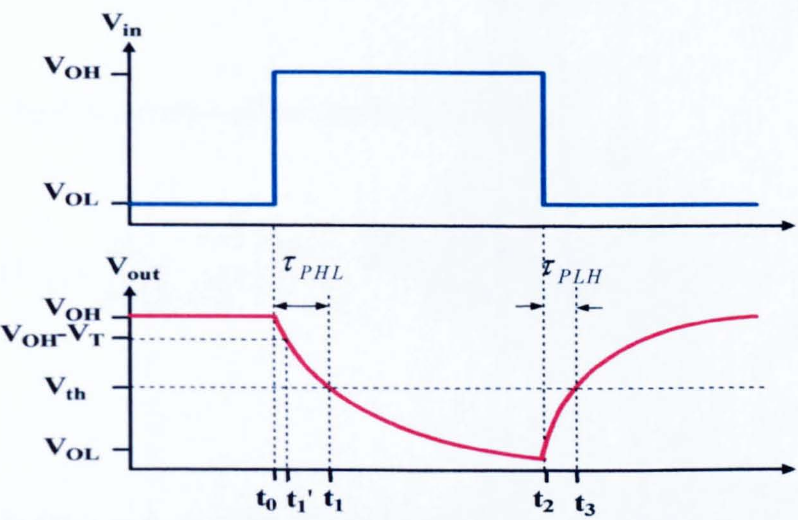

Figure 24: Timing diagram of discharging and charging process of a saturated enhancement-load inverter

The average propagation delay τ_P of the inverter is given by the average time required for the input signal to propagate through the inverter.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \frac{(t_1 - t_0) + (t_3 - t_2)}{2} \quad . \tag{3.24}$$

The propagation delay times shown in Figure 24 can be found accurately by solving the state equation of the output node in the time domain. The differential equation associated with the output node is given below. Note that the capacitance current is also a function of the output voltage:

$$C_{load}\frac{dV_{out}}{dt} = i_C = i_{D,load}\left(V_{out}\right) - i_{D,driver}\left(V_{in},V_{out}\right), \quad (3.25)$$

where the drain current of the saturation load is

$$i_{D,load}\left(V_{out}\right) = \frac{KC_{OX}{}^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\frac{W}{L}\right)_{load}\left[\frac{\left(V_{DD}-V_{out}-V_{T0}\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right]. \quad (3.26)$$

The drain current of the driver transistor varies in different regions. A piecewise function can be used as its expression:

$$i_{D,driver}\left(V_{in},V_{out}\right) = \begin{cases} \dfrac{KC_o{}^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\dfrac{W}{L}\right)_{driver}\left[\dfrac{\left(V_{in}-V_{T0}\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right] & \text{, saturation region } t_0 \rightarrow t_1' \\ \dfrac{KC_o{}^{(2m+1)}}{(2\varepsilon_o\varepsilon_s kT)^m}\left(\dfrac{W}{L}\right)_{driver}\left[\dfrac{\left(V_{in}-V_{T0}\right)^{2(m+1)}-\left(V_{in}-V_{T0}-V_D\right)^{2(m+1)}}{2\cdot(2m+1)(m+1)}\right] & \text{, linear region } t_1' \rightarrow t_1,\ t_2 \rightarrow t_3 \end{cases}.$$

(3.27)

Therefore, the propagation delay times τ_{PHL} and τ_{PLH} are found from the following integrals:

$$\tau_{PHL} = t_1 - t_0 = \left(t_2 - t_1'\right) + \left(t_1' - t_0\right)$$
$$= C_{load} \cdot \int_{V_{OH}}^{V_{OH}-V_T} \frac{dV_{out}}{i_{D,load}\left(V_{out}\right) - i_{D,driver,saturation}\left(V_{in}, V_{out}\right)} +$$
$$C_{load} \cdot \int_{V_{OH}-V_T}^{\frac{1}{2}(V_{OH}-V_{OL})} \frac{dV_{out}}{i_{D,load}\left(V_{out}\right) - i_{D,driver,linear}\left(V_{in}, V_{out}\right)} ,$$

(3.28)

$$\tau_{PLH} = t_3 - t_2$$
$$= C_{load} \cdot \int_{V_{OL}}^{\frac{1}{2}(V_{OH}-V_{OL})} \frac{dV_{out}}{i_{D,load}\left(V_{out}\right) - i_{D,driver,linear}\left(V_{in}, V_{out}\right)} . \quad (3.29)$$

With polymer technology the switching speed is inherently low because of low mobility. The switching speed is determined by charging delay as the low charging current provided by the load is much smaller that the transient discharge current provided by the driver. The delay times calculated using load capacitance C_{load} may slightly overestimate the actual inverter delay, but this is not considered a significant deficiency in a first-order approximation.

The symbolic expression of the propagation delay time with the new equation can not be simplified any further, but using the mathematic package MathCAD we can simulate the numeric result of the inverter output and propagation delay times can be found from the simulation result in Figure 25 . The simulations here are all based on n-channel transistors in order to avoid conversion between the positive and negative sign. The result of the p-channel transistor is identical but with a negative sign.

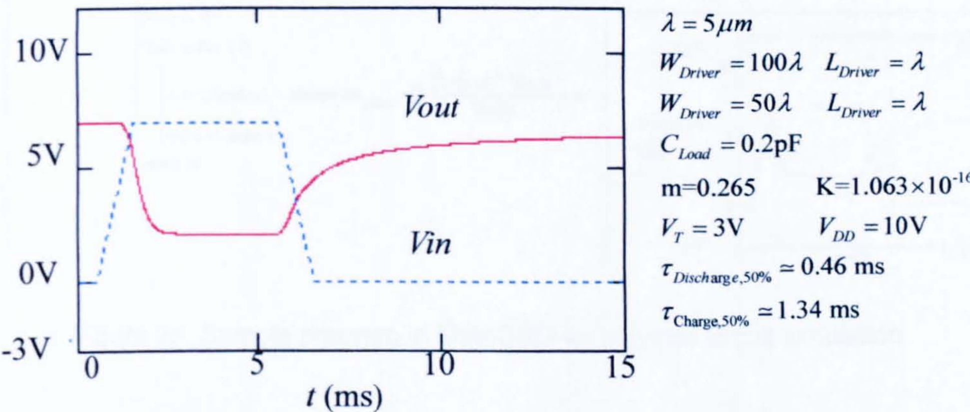

Figure 25: Simulation of dynamic behavior of inverter in MathCAD

From the above simulation result we can see the inverter has an asymmetric input-output characteristic and the output range decreases because of threshold voltage.

The program shown in Figure 26 as an example can also used to simulate other more complex circuits.

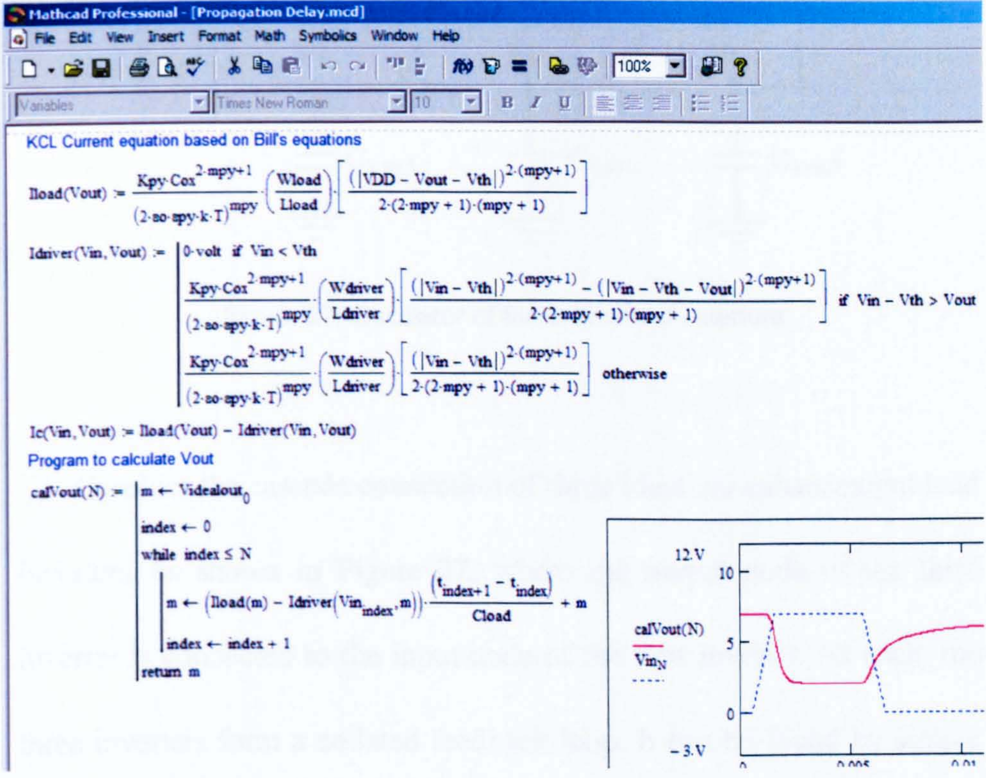

Figure 26: Sample program in MathCAD for polymer circuit simulation

3.8 Ring oscillator circuit

The ring oscillator circuit illustrates some of the dynamic operation characteristics of inverters, which were introduced in the previous section. At the same time, this circuit will provide us with a simple demonstration of an application circuit based on a polymer transistor and an

approximate measurement of the maximum speed that the polymer transistor technology can achieve.

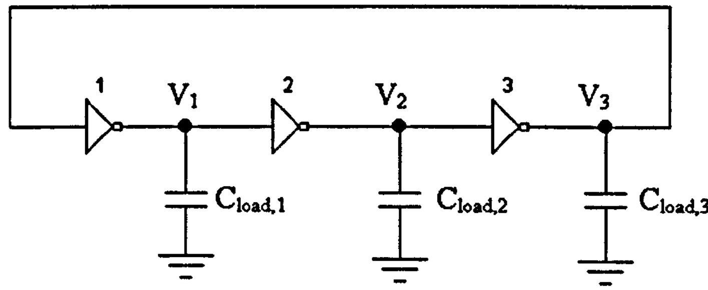

Figure 27: Oscillator of three identical inverters

Consider the cascade connection of three identical enhancement load inverters, as shown in Figure 27, where the output node of the third inverter is connected to the input node of the first inverter. As such, the three inverters form a collated feedback loop. It can be found by simple inspection that this circuit does not have a stable operating point, and the only possible operating point at which the input and output voltages of all inverters are equal to the logic threshold V_{th}, is inherently unstable. In fact, a closed loop cascade connection of any odd number of inverters will display a stable behaviour. Such a circuit will oscillate once any of the inverter input or output voltages diverge from the unstable operating point, V_{th}. Therefore, the circuit is called a ring oscillator.

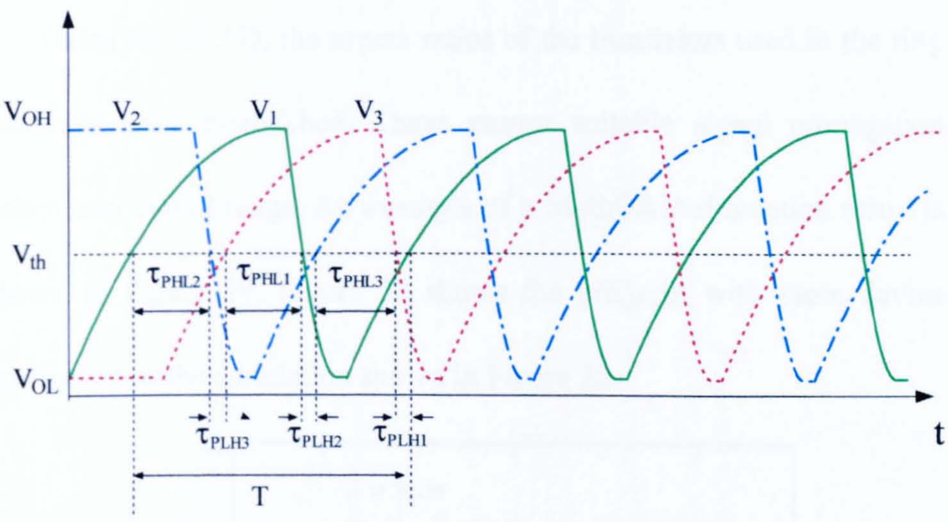

Figure 28: Signal propagation in three-stage oscillator

Figure 28 shows a typical output voltage and output waveforms of three inverters during oscillation. As the output voltage V_1 of the first inverter stage rises from V_{OL} to V_{OH}, it triggers the second inverter output V_2 to fall, from V_{OH} to V_{OL}. Note that the difference between the V_{th}-crossing times of V_1 and V_2 is defined as the signal propagation delay τ_{PHL2}, for the second inverter. As the output voltage V_2 of the second inverter falls, it triggers the output voltage to rise from V_{OL} to V_{OH}. Again, the difference between the V_{th}-crossing times of V_2 and V_3 is defined as the signal propagation delay τ_{PHL3}, for the third inverter. It can be seen from Figure 28 that each inverter triggers the next inverter in the cascade connection, and the last inverter again triggers the first, continuing the oscillation.

Using MathCAD, the aspect ratios of the transistors used in the ring oscillator were established. These ensure suitable signal propagation delays and output range. An example of a MathCAD simulation result is shown in Figure 29. Figure 30 shows the program with same device parameters as the simulation shown in Figure 25.

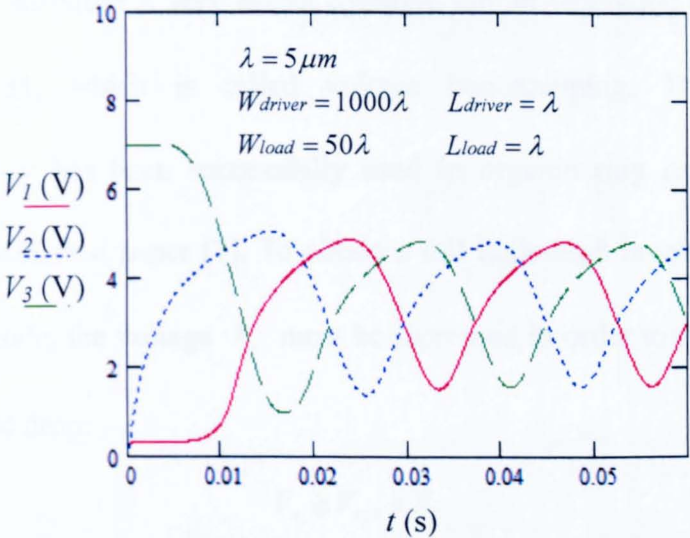

Figure 29: Simulation of ring oscillator with initial stimulus

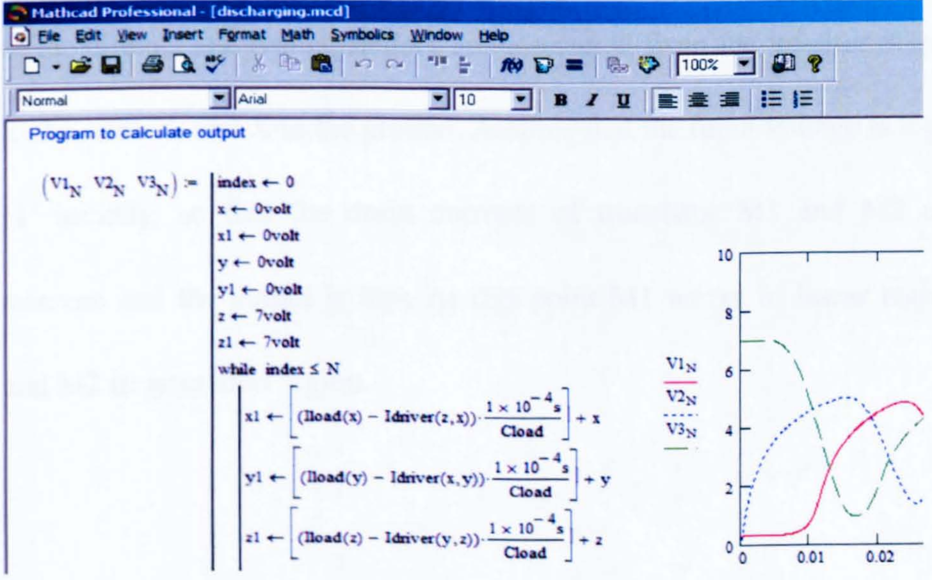

Figure 30: MathCAD program for ring oscillator simulation

3.9 Voltage bootstrapping

The output voltage levels of the enhancement-load inverter and the pass transistor may suffer from threshold drop as we have discussed in the previous section. To overcome this threshold voltage drop problem, we will introduce a very useful dynamic circuit technique as shown in Figure 31, which is called voltage bootstrapping. This classical technology has been successfully used in organic ring oscillator in a recent published paper [7]. To obtain a full logic-high level (V_{DD}) at the output node, the voltage V_x must be increased in order to overcome the threshold drop:

$$V_x \geq V_{DD} + V_T. \tag{3.30}$$

Therefore a third transistor M3 and two capacitors have been added to the circuit. The two capacitors are connected from the inverter output to the node X, and X to the ground. Assume that the input voltage is logic '1' initially, so that the drain currents of transistor M1 and M2 are nonzero and the output is low. At this point M1 works in linear region and M2 in saturation region.

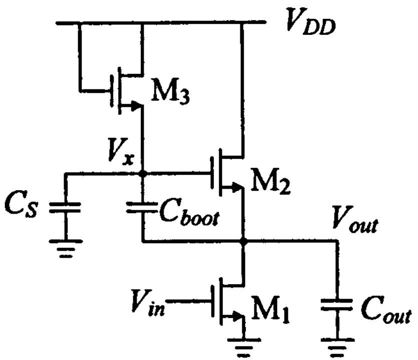

Figure 31: Voltage bootstrapping configuration for enhancement circuit

Now assume that the input switches from its logic high level to 0 V at $t = 0$. So the driver transistor M1 will turn off and the output V_{out} voltage will start to increase. This change in the output level will now be coupled to V_x through the bootstrap capacitor, C_{boot}. Assuming in this charge-up process C_{boot} and C_s have approximately identical transient currents following through them, we have:

$$C_s \frac{dV_x}{dt} = C_{boot} \frac{d(V_{out} - V_x)}{dt}, \quad (3.31)$$

$$\frac{dV_x}{dt} = \frac{C_{boot}}{C_s + C_{boot}} \cdot \frac{dV_{out}}{dt}. \quad (3.32)$$

From (3.32) we can see that an increase in the output voltage will generate a proportional increase in the voltage V_x. Integrating both sides of this equation, we have:

$$\int_{V_{DD}-V_T}^{V_x} dV_x = \frac{C_{boot}}{C_s + C_{boot}} \cdot \int_{V_{OL}}^{V_{DD}} dV_{out}, \quad (3.33)$$

$$V_x = (V_{DD} - V_T) + \frac{C_{boot}}{C_s + C_{boot}} (V_{DD} - V_{OL}) \quad (3.34)$$

If the capacitor C_{boot} is much larger than C_s, we can obtain the maximum value of V_x,

$$V_x(\max) = 2V_{DD} - V_T - V_{OL} \quad (3.35)$$

And the minimum required ratio of C_{boot} / C_s in order to overcome the threshold voltage drop is:

$$\frac{C_{boot}}{C_s} = \frac{2V_T}{V_{DD} - V_{OL} - 2V_T} \quad (3.36)$$

3.10 Parasitic resistance

In current circuit technology, the semiconducting polymer is deposited by drop casting or the spinning method. This kind of deposition has the advantage of manufacturing with low cost, and also providing a uniform and thin polymer layer. However the drawback is that all the transistors use the same semiconductor layer and are connected together. This problem becomes more critical with increasing conductivity and mobility of polymer materials. Leakage currents in a polymer circuit are analysed here. The critical transistors are those which are isolated by the 'pass' transistors when storing charge on the gate.

As we know the current is proportional to the voltage across the resistor and inversely proportional to its resistance. This resistance can be estimated from the area and resistivity. As an example, a photo of a two-stage shift-register circuit is shown in Figure 32(a) with its schematics shown in Figure 32(b). We estimate that the leakage current between input A of the inverter and the ground terminal B will be high because the potential difference is high while the geometrical distance is small. Also the leakage current between input A and output B cannot be ignored.

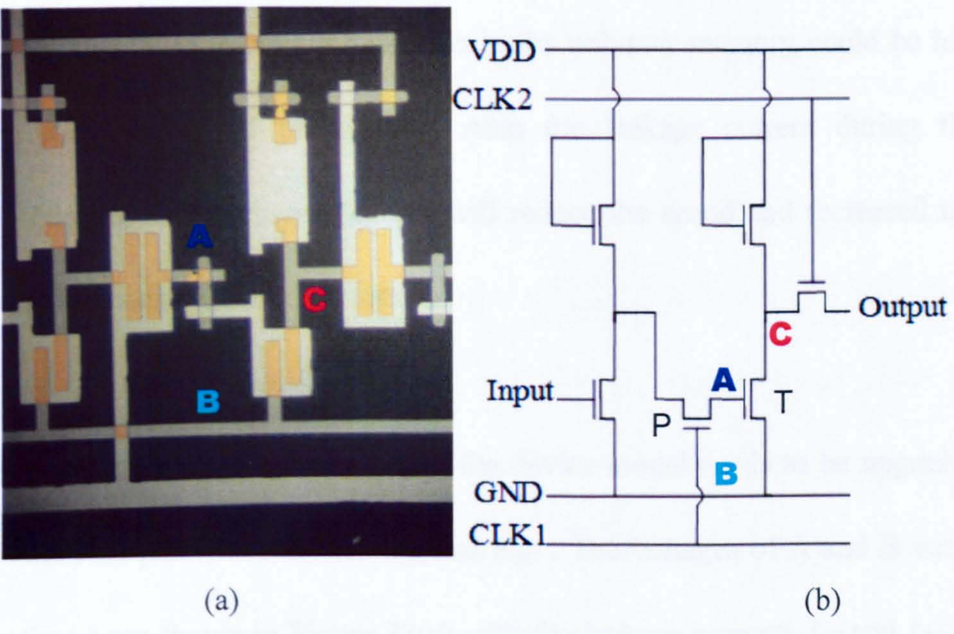

Figure 32: Layout of a shift register (a) with its circuit configuration (b)

Consider position A at the gate electrode of 'driver' transistor T and position B at the drain, which serve as the input/output of the inverter. Assuming a logic '1' signal (high voltage) is passed via point A and then through the 'pass' transistor P, the output of the inverter B is discharged to a stable low voltage. After the 'pass' transistor is turned off by the period clock signal, the charge at A should ideally remain in the metal in between the 'pass' transistor P and the 'driver' transistor T until the next active clock signal comes. However, in practice part of the charge will leak though the 'pass' transistor P as a reverse current flows through the semiconducting polymer to the next stage B and the ground C as leakage currents. This implies information in the polymer memory could be lost during the signal propagation. Also the leakage current during the charging and discharge process will reduce the speed and increased the power consumption.

For circuit simulation work, the device model needs to be upgraded with the parasitic resistors R_{AB} and R_{AC} . The voltages of A and B verse time t are shown in Figure 33(a) with the leakage currents I_{AB} and I_{AC} in Figure 33(b). As shown in Figure 33(a) the signals do not continue to remain stable as ideally expected but start coming to '0' after they reach

their peak values. The charge and discharge processes with leakage current are longer than the ideal case (no leakage currents).

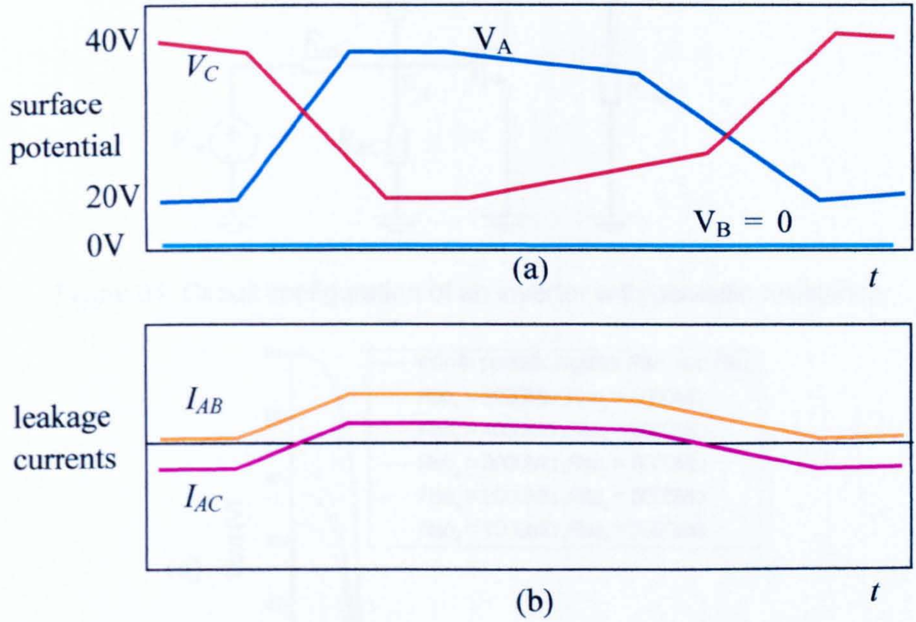

Figure 33: Signal propagation in shift register with leakage currents

For integrating the estimated parasitic resistances into the simulation of simple inverter, we will start with the equivalent circuit shown in Figure 34. R_{AB} indicates the parasitic resistor between the output and the input of the inverter and R_{AC} is parasitic resistor between the input and the ground. From the simulation result shown in the Figure 34, it is shown that the variation of parasitic resistor R_{AB} has more effect on the transfer characteristic as compared to R_{AC}.

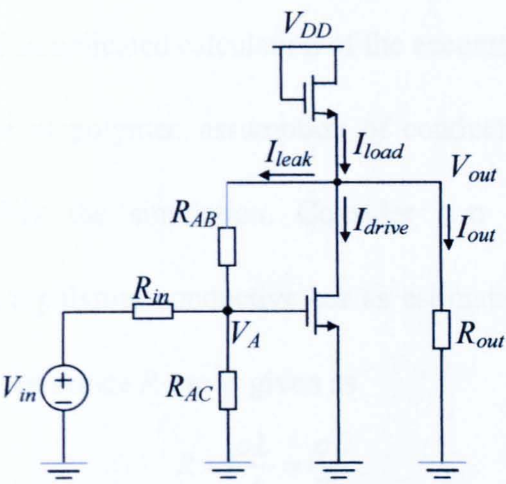

Figure 34: Circuit configuration of an inverter with parasitic resistance

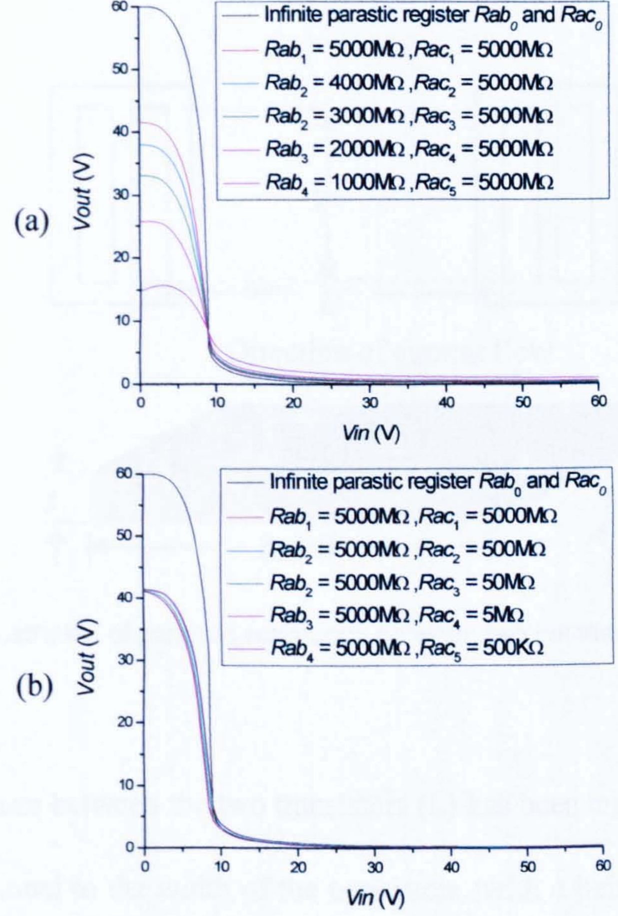

Figure 35: Transfer characteristic of inverters with various parasitic resistors (a) *Rab* between the input and the output, (b) *Rac* between the input and the ground (Ideally $Rab \to \infty$ and $Rac \to \infty$; for calculation purpose high values were chosen)

Here, instead of complicated calculation of the accurate resistance formed by a wide layer of polymer, assumption of conductive polymer bar is made to simplify the simulation. Consider two parallel transistors connected with a polymer conductive bar as estimations of the parasitic resistances, the resistance R can is given as

$$R = \frac{\rho L}{A} = \frac{\rho L}{Wt}. \tag{3.37}$$

where ρ is resistivity in Ω-cm, and A is the cross section area as shown in Figure 36.

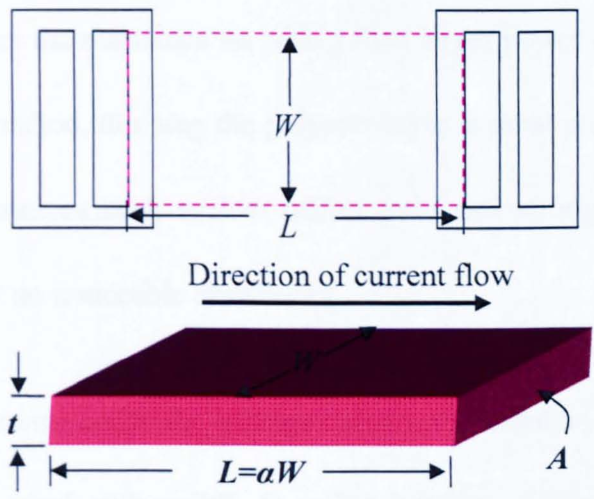

Figure 36: Illustration of parasitic resistance between two parallel transistors

The distance between the two transistors (L) has been taken here like being proportional to the width of the transistors (with α being a spacing parameter). Replacing the resistivity in Equation (3.37) with conductivity and integrating the power-law relationship between conductivity and

mobility, we have

$$R = \frac{\alpha}{\sigma t} = \frac{\alpha}{t}\left(\frac{K_1}{\mu}\right)^{\frac{1}{\gamma}} \propto \frac{\alpha}{t\mu^{\frac{1}{\gamma}}}. \tag{3.38}$$

As shown in this equation, to achieve a smaller leakage current between transistors we can increase the parasitic resistor by (1) reducing the thickness of the polymer layer; (2) increasing the spacing between transistors or (3) using a polymer material with lower mobility. However low mobility gives poor field-effect transistor performance and large spacing increases the resistance on wiring thus larger power consumption. Only the first method, thinning the polymer layer is most preferable with additional advantages such as low off/on ratio and strong field effect dependency but no noticeable drawbacks.

Moreover, to minimize the leakage current, the metal wiring needs to be insulated as much as possible. In a first instance, a second dielectric can be employed to achieve this. Also polymer patterning using a lift-off process with a top passivation layer and an inkjet-printing technology in order to disconnect the semiconducting layer can be considered.

3.11 References

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Chapter 4

POLYMER CIRCUIT PROCESS DEVELOPMENT AND LAYOUT DESIGN

Polymer device structures, such as TFTs, [1] [2] and Schottky diodes [3], [4], [5] have been widely used in circuits. Their manufacturing process focuses on the improvement of device performance with high field-effect mobility, low leakage current and high polymer stability. To build up polymer circuits, additional components and processes are required [6].

In this chapter a brief review of current device technology including structure, material and available process is provided [7]. The processes required for circuit components, VIA and cross-over structures, are introduced with focus on selective anodization technique. The last part of this chapter presents the layout design of the polymer circuit, CCD and the vertical transistor.

4.1 Transistor structure configuration

Transistor characteristics strongly depend on the device structure configuration and also the materials used as the active insulating layers. Therefore a review and discussion of our polymer transistor with emphasis on configuration, material and integration will be presented in this section.

Although there are some innovative structures designed for organic thin film transistors, such as top contact [8] and vertical transistors [9], [10], most of the reported organic thin film transistors are designed in three different kinds of configuration. They are shown in Figure 1. According to the gate position, they could be called bottom gate transistors [11] or top gate transistors [1]. For the bottom gate transistor, the source/drain electrode might be on the top of semiconductor or under the semiconductor: they are then termed top-contact and bottom-contact transistor respectively [12].

For the top contact layout as shown in Figure 1(C), the semiconducting organic material is deposited on the insulator, then the source and drain contacts are placed in position. This structure [13] is widely used in the study of the polymer transistors because it maximizes

the smoothness of the polymer thin film layer. The source and drain electrode are normally formed with the thermal evaporation with a shadow mask; there is no need for the lithography process unless very small channels are desirable. Therefore the chemical and electrical characteristics of the polymer thin film layer will not be affected by the chemicals normally used in lithography patterning. This is because thermally grown silicon dioxide is the normal choice for early experimental work.

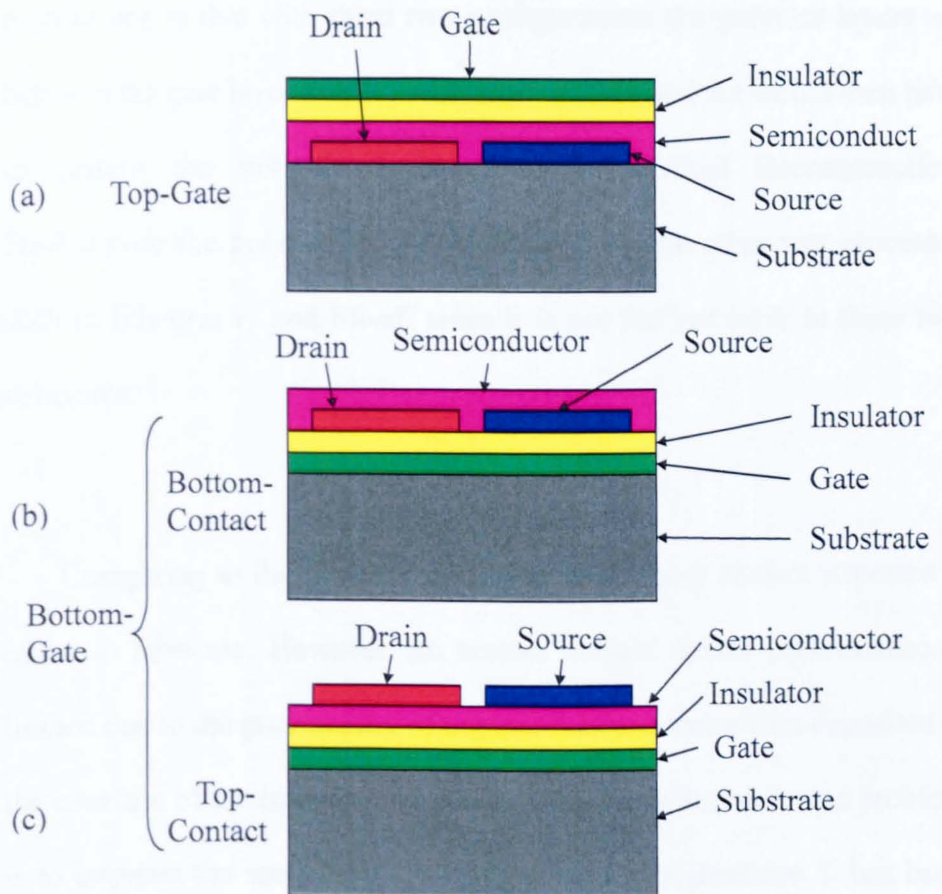


Figure 1: Different configurations of organic thin film transistors

(a) top-gate transistor (b) bottom contact transistor (c) top contact transistor

The top gate configuration as shown in Figure 1 (a), is widely used in all polymer devices in order to overcome the channel length limitation involved with the printing technology. To minimize the channel length, the source and drain are deposited as the first layer either on the patterned substrate by inkjet printing [1], [14], or by stamping technology.

There are several reasons why we do not use top-gate and top-contact configurations in our polymer circuit design. The most evident one is that with these two configurations the polymer layers are between the gate layer and the source/drain layer and we would then have to pattern the polymer layer from the vertical interconnection. Furthermore the polymer might be affected by the other wet processes such as lithography and lift-off since it is not the last layer in these two structures.

Comparing to the top contact device, the bottom contact structure is easier to fabricate. However the bottom contact device performance is limited due to the poor quality of organic semiconductor film deposited at the interface of the contacts and the channel. The solution to this problem is to improve the smoothness of the gate and gate insulator. It has been found that the annealing process is able to improve the morphology of the contact between the polymer layer and the gate insulator at the transistor

channel. The mobility and stability of the bottom contact transistor can then be improved. This structure also allows the polymer layer to be cast or spun as the last layer on top of the backbone of the circuit. Therefore it can avoid the storage problem and the degeneration of the polymer during transport.

4.2 Materials for the polymer circuit

Since the late 1970s when the first non-insulating polymer material was discovered [15], the researchers have achieved significant progress with semiconducting organic materials, although there is still room for much improvement in stability and mobility. Early on, it was realized that for high performance organic TFTs, the organic semiconductor was not the only critical component. It is also very essential and important to find out a suitable gate insulator with high insulating performance and low manufacturing cost. Furthermore, material requirements of VIAs and crossover structure have to be considered. Different materials for various device components, such as contacts, organic semiconductors, gate insulators and also substrates, have been studied and demonstrated in published papers [16]. Presented here is a brief overview of these widely used materials, together with the reason for our choice of the materials in polymer circuit development.

With a relatively easy process, solution processable p-type semiconducting polymers such as P3HT and PDHTT have been studied and reported as well as pentacene, a small-molecule organic that has a higher mobility. The latter needs to be evaporated under high-vacuum conditions, but this may not be consistent with low manufacturing costs. The difference between the mobilities of polymer and pentacene comes from their different structures and conduction mechanisms.

For charge transport in polymers, large crystalline domains with a long-range structural order that aids in charge transport by hopping would lead to high mobility. A sufficiently long alkyl side-chain would provide the solubility needed for processing and structural regio-regularity which helps promote molecular self-assembly to achieve a desirable structural order for charge transport.

Molecular self-organization is difficult for region-random polythiophene on which the chains are not positioned regio-regularly along the backbone. As one of the most important regio-regular polythiophenes semiconductor used in current organic electronics technology, regio-regular head-to-tail poly(3-hexylthiophene), or rr-HT-P3HT has been demonstrated to produce excellent FET characteristic results [17]. The mobility and current on/off ratios are as

high as 0.1 cm^2 V^{-1} S^{-1} and 10^6 respectively. However the performance rapidly degrades on continued air exposure. This effect at present is still not well understood. Further work may be necessary to obtain more information on the effect of oxygen on P3HT. From the current reported results, rr-HT-P3HT with a stable performance as a semiconductor in FET fabricated under ambient conditions is still being developed.

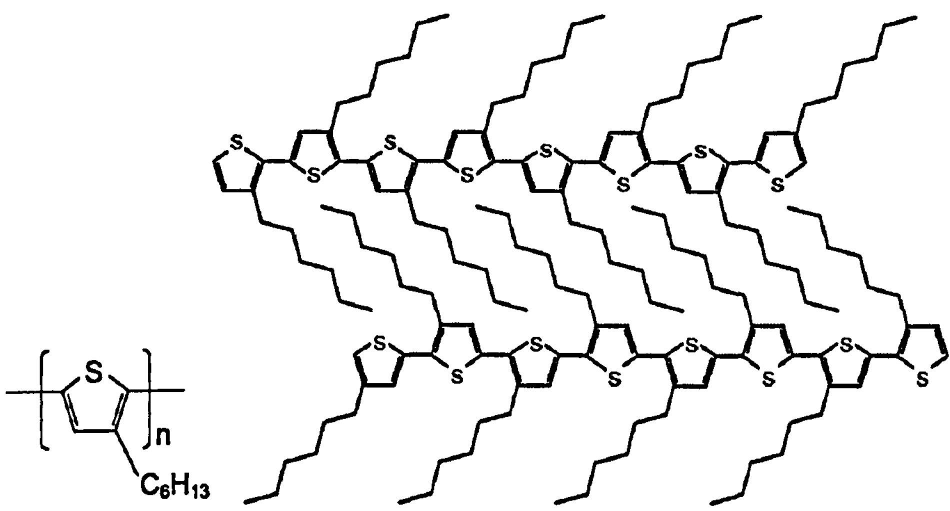


Figure 2: Highly regio-regular head-to-tail poly(3-hexylthiophene)

The gate insulating materials are also extremely crucial for reliable and high-performance organic devices. Both organic and inorganic dielectric materials have been reported as gate insulators for polymer transistors with reasonable performance. For a long time silicon dioxide thermally grown on silicon, dominated as the gate-dielectric material for organic TFTs and are widely used for screening new organic materials. However, the realization of polymer circuits on an expensive substrate

like a silicon wafer removes the advantage of organic electronics: low cost and easy processing. With a focus on a substrate-independent dielectric with low deposition temperature, a large number of high quality inorganic gate dielectric materials and their deposition methods have been investigated. The reported preparation methods for inorganic dielectrics include thermal grown (SiO_2 [18]), sputtering (Al_2O_3, Ta_2O_5 [19] and SiO_2 [20]), anodization (Al_2O_3[21] and TiO_2 [22]) and chemical vapour-deposited (CVD) (SiN_x [23]).

Solution-processable polymer gate dielectrics and their low-cost fabrication methods are of interest because they can be deposited by spin-coating, spray-coating, or printing, rather than by vacuum deposition. Examples of organic gate insulators are Polyvinylpyrrolidone (PVP) [25], Polymethyl methacrylate (PMMA) [26], photoresist [27] and Polymide (PI) [28] [29]. However, thickness uniformity and pinhole density are critical challenging issues for the organic gate insulator, especially when a large area application is required. Most evaluations are based on discrete transistors and little is known of the long-term effects of various dielectric materials on device performance. It must be compatible with the organic semiconductor (interfacial diffusion, mixing and reaction may occur over time and change the characteristic of transistors).

Inorganic insulators present most of the desired features except that they usually have to be deposited under high vacuum and high temperature conditions. Also most of the high-ε inorganic insulators require expensive deposition methods like sputtering [13], [20]. The electrochemical anodic oxidation [30] does not require high temperature and vacuum conditions and is potentially of lower cost and is compatible with plastic substrates.

Gate dielectrics with higher dielectric constant are of interest in order to reduced power consumption. The aluminium oxide grown by the anodization process normally gives a dielectric constant of about 4.2, which are similar to the dielectric contact of silicon oxide, 3.9. However it has recently been claimed that high-k insulators may enhance the formation of local states that in turn induce carrier localization and reduce carrier mobility [24] . Further material researches on the gate dielectrics are being developed.

4.3 Fabrication technologies

Different deposition technologies have been described to form a basic component of polymer devices, such as vacuum evaporation [31] and inkjet printing of the semiconductor, also e-beam evaporation [32]

and anodization for gate insulator [30].

Printing technology shows the advantages of low cost and easy processing compared with the high temperature and vacuum evaporation process. However, so far current printing technology can not achieve high quality films with uniform thickness and smoothness. This is an extremely important issue for the highest performance polymer devices.

4.4 Process design of crossover and VIA

Crossover and vertical interconnection (VIA) between different levels of metal layers are essential components for semiconductor circuits because combining several transistors into an integrated circuit requires the use of VIAs between the source and drain electrodes of one transistor and the gate electrode of another transistor.

The performance of VIAs, crossovers and the ease of their fabrication, is mainly dependent on the insulator used for the transistor. Firstly for electrical isolation, the crossover structure requires a good insulator which is able to insulate both top and the side of the bottom metal layers from a top metal layer. Reasonably high breakdown voltage is also a critical requirement. On the contrary, VIA structures requires a

good contact between the metal layers without any residual insulator from the previous processes or unexpected oxide on the bottom metal. Secondly for physical and geometrical requirements, the top metal needs to adhere well to the bottom metal layer and the insulator layer. Furthermore the insulator layer must not be too thick otherwise the thin top metal layer could be damaged and disconnected on the edges of the thick insulator layer. These structures also depend on the structure and manufacturing process used for the polymer transistor. In 2001, researchers in Cambridge University and Epson Cambridge Laboratory presented their VIA-hole interconnections and insulators for crossovers with all-polymer top-gate transistors which have been made by inkjet printing of solvent on polymer insulators [33] or photolithography combining oxygen plasma etching [1]. An alternative solution reported by other researchers is to make VIA contacts with a mechanical punching process [34]. But this is not practical for use in high volume production. Here we introduce three possible solutions for the formation of VIAs and crossovers on a bottom-aluminium-gate transistor with a high-k gate dielectric of anodized aluminium oxide.

4.4.1 Selective anodization with photoresist shield

From the measurements on polymer capacitors and transistors, the anodized alumina shows high performance of uniform thickness, good surface smoothness and a high dielectric constant, which organic dielectric materials cannot reach. However, the anodic oxidation process used for forming the anodized gate structure has the disadvantage of requiring some additional process steps to shield the bottom chromium connectors. Otherwise the anodization on the aluminium cannot be carried out once a thin layer of alumina has been grown on the surface. The reason for this is the alumina and chromium are connected in parallel to the electrolyte and majority part of the surface current flows via chromium but not aluminium which is covered by high-k alumina. Therefore the first method to form VIAs using selected anodization is introduced here. The basis of this solution is to shield the chromium during anodization with dielectric photoresist so that the current will only go via the aluminium surface to drive the aluminium anodization process. As shown in Figure 3, after deposition of connector and gate layer, the pattern of connector has to be covered by a layer of insulating photoresist to avoid contact defects during anodization.

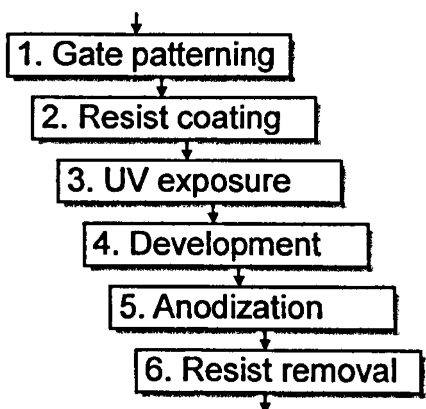


Figure 3: Selective anodization with photoresist protection

In order to understand the selective anodization process in detail, a typical circuit component, the first part of the manufacturing process to form transistor gate electrodes is shown as a demonstration in Figure 4. As we can see in Figure 4(B), after aluminium (coloured in green) is deposited on top of the substrate, the photoresist is patterned using lithography process to shield the region which is not required to be anodized. The photoresist is used as a corrosion resistant material during the anodization process. The expected result of this selective anodization is shown in Figure 4(C). From the cross section we can see alumina also covering the sides of the aluminium. The thickness of the alumina layer depends on the electric field at the interface of the aluminium and the anodization time. After anodization, the photoresist can be easily removed with photoresist remover. The main reason of this design using selective anodization is that removing Al_2O_3 from Al surface with a

chemical method is usually difficult. In etchant solution, both Al_2O_3 and Al are able to be etched off. Also the length of anodization time and the density of etchant could vary the etching progress.

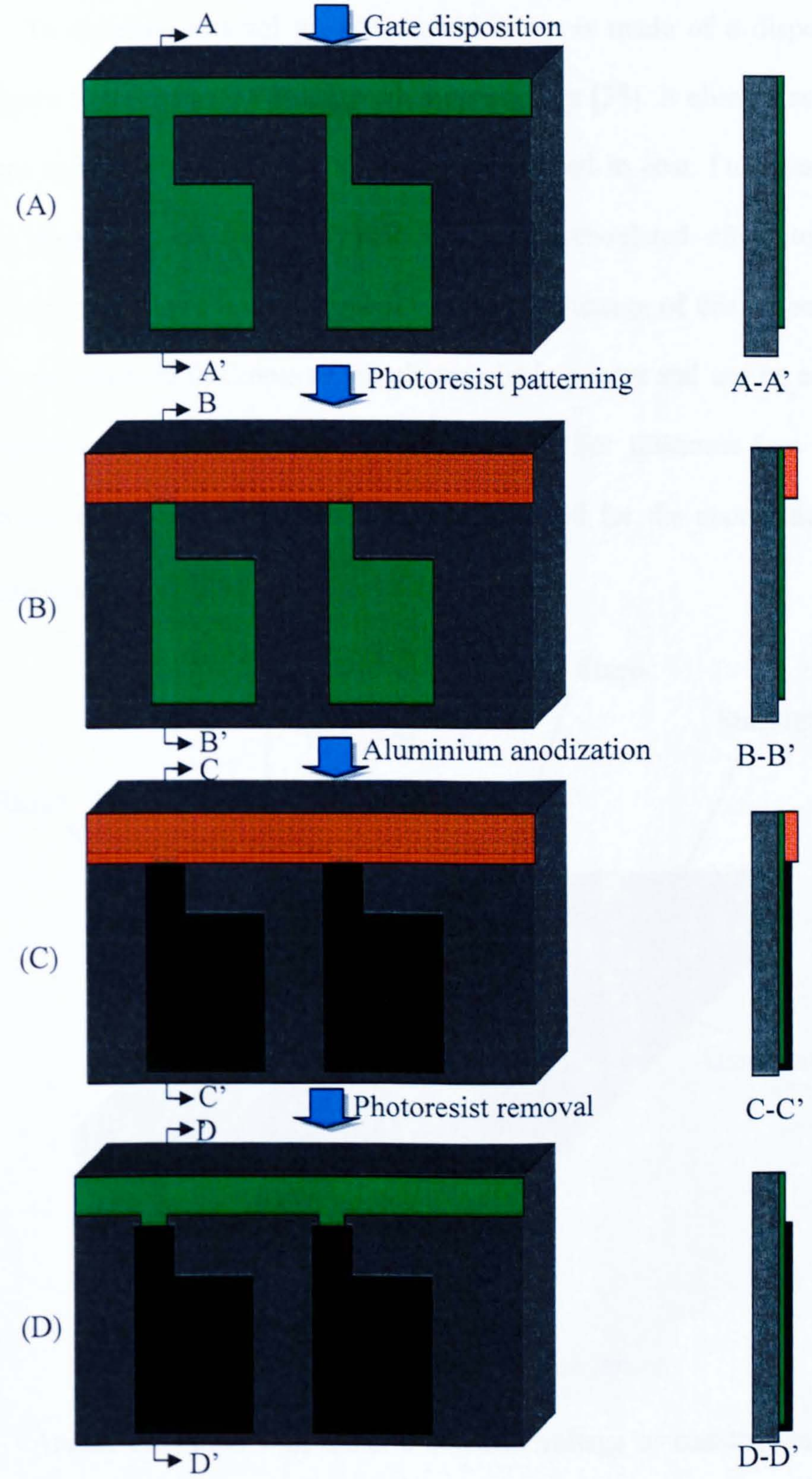


Figure 4: Illustration of selective anodization (I)

To simplify, a novel process in which use is made of a dispenser (Figure 5) has been reported by other researchers [35]. It eliminates two steps and the production process is much reduced in cost. Furthermore, this dispensing process can avoid the developer-related effect to the aluminium during the development. Another advantage of this process is that the achieved thickness of the photoresist is greater and can be easily increased by controlling the amount of resist. For thickness less than 1.5 μm resist, peeling occurs if the voltage used for the anodization is increased.

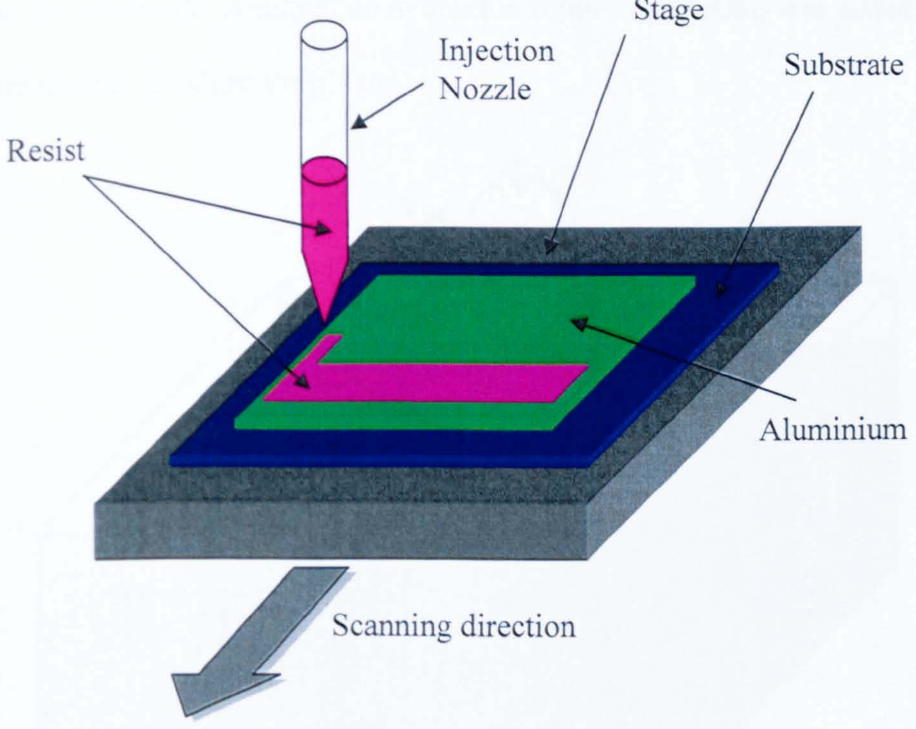


Figure 5: Schematic of resist dispenser

Anodic oxidation with either a constant voltage or constant current can be used in the growth of aluminium oxide. The thickness of grown

oxide depends on the applied voltage and also the anodization time. The set up for the constant voltage anodic oxidation of aluminium is shown in Figure 6. The anode consists of an aluminium metal layer which is evaporated and patterned on a pre-cleaned glass substrate. Thick photoresist, AZ 4562 provided by Clariant GmbH, was employed to avoid the anodization on selected areas of the aluminium surface. The cathode consists of a cleaned gold strip. The electrolyte was a mixture of ethylene glycol (CH_2OHCH_2OH) and 3% by weight of tartaric acid $(CHOH)_2(COOH)_2$. The acid is thought to increase the ionic conduction in the electrolyte. Ammonium hydroxide solution (NH_4OH) was added to the mixture to adjust the pH to 7.

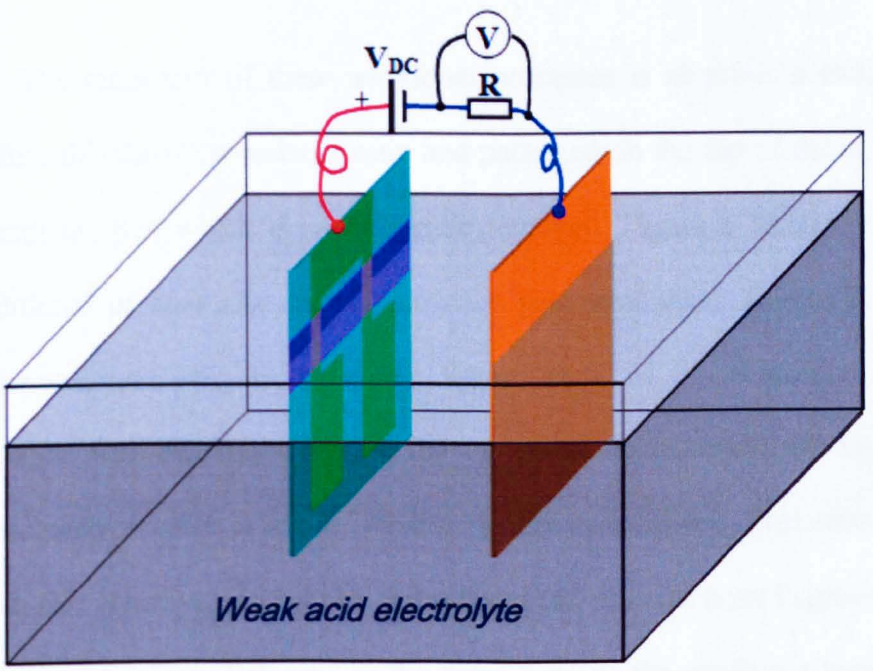


Figure 6: Set up for constant voltage anodic oxidation of aluminium.

For anodic oxidation, the gates and crossover must be electrically connected so that a voltage can be applied to all of them. Practical circuits require that the gates are to be separated for different functions. Therefore an additional isolation process, as shown in Figure 7, is needed after anodization.

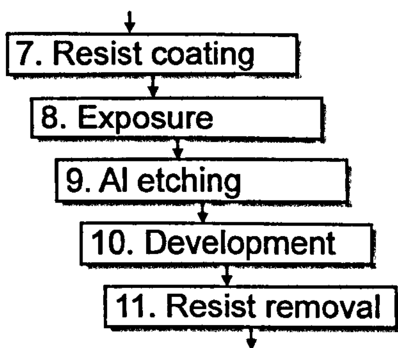


Figure 7: Additional processes for gate isolating after anodization

The main part of these additional processes is aluminium etching. Before this the photoresist is spun and patterned on the top of the circuit except the part which is needed to be removed. Figure 8 illustrates the additional process after anodization for gate insulation. Shown in the cross section G-G' in the above figure, parts of the aluminium are exposed after etching, therefore the top metal layer should not lay on these parts in order to avoid introducing any unnecessary short contacts. With this selective anodization technology, the alumina layer is grown as the transistor gate dielectric at the same time as the insulating layer of crossover structure.

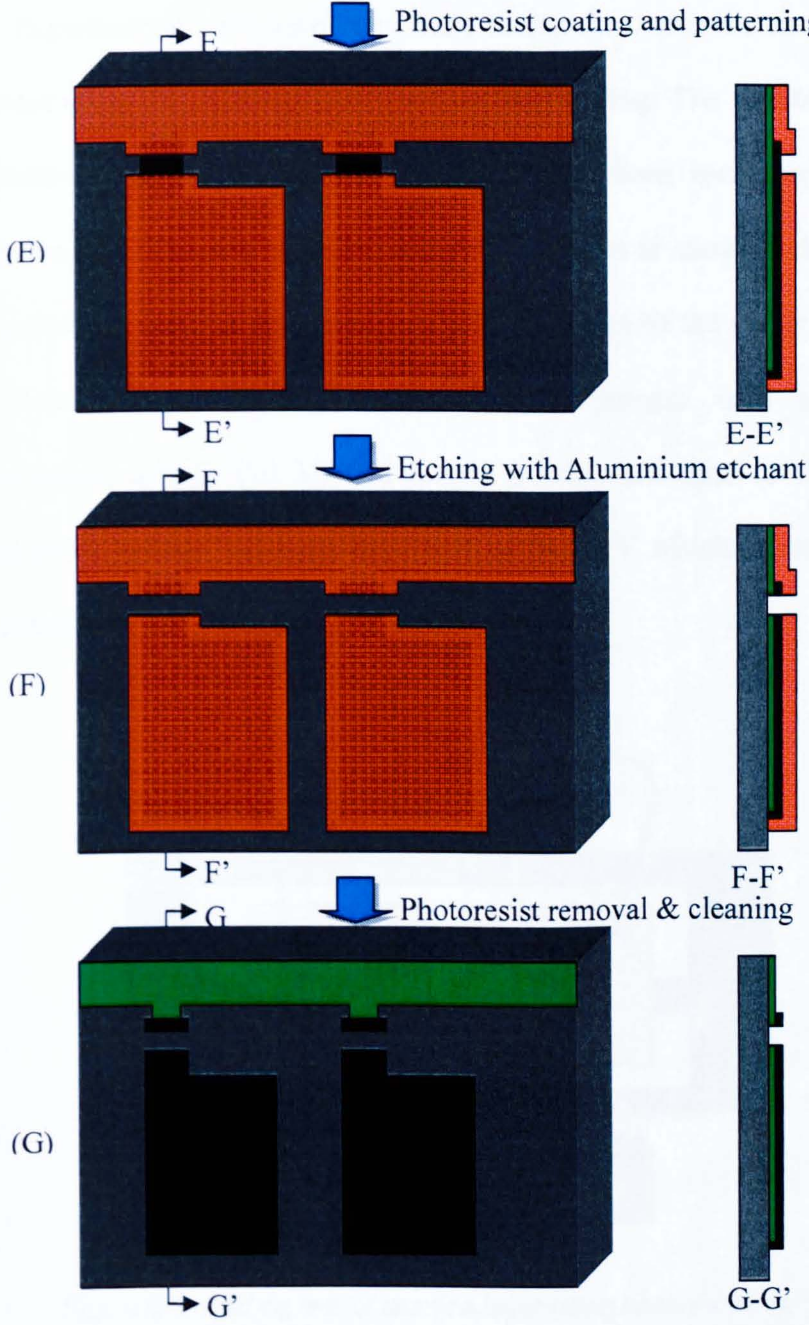


Figure 8: Illustration of selective anodization (II)

To insulate the gate electrodes, many additional processes are required. Alternatively, a laser cutting process can be used to isolate the aluminium on the glass substrate.

Experimental tests have been done to test this selective anodization process using the existing mask for transistor testing. The resistance and breakdown voltage of the alumina layer have been measured by IV measurement. The test structure and configuration is shown below. The breakdown voltage is decreased to about 10 V due to the rough edge of aluminium. By improving the anodization process with a higher anodization voltage (80 V) and longer anodization time (5 minutes), breakdown voltage has been improved to be 25 V which is reasonably acceptable.

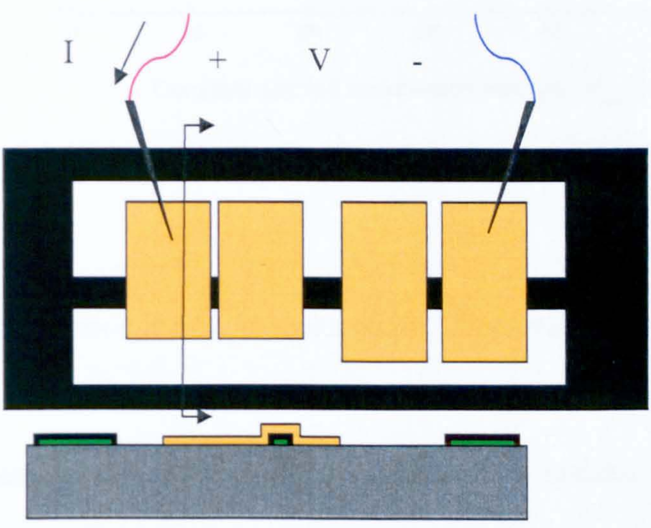


Figure 9: Insulating test of alumina layer using IV measurement

The breakdown voltage of the alumina layer is a critical limitation since the high supply voltage is required by the polymer transistor because of the low mobility semiconducting polymer materials.

Measured data of an aluminium oxide layer with different applied anodization voltages is shown in Figure 10. The thickness and breakdown voltage can be increased by applying a higher anodization voltage.

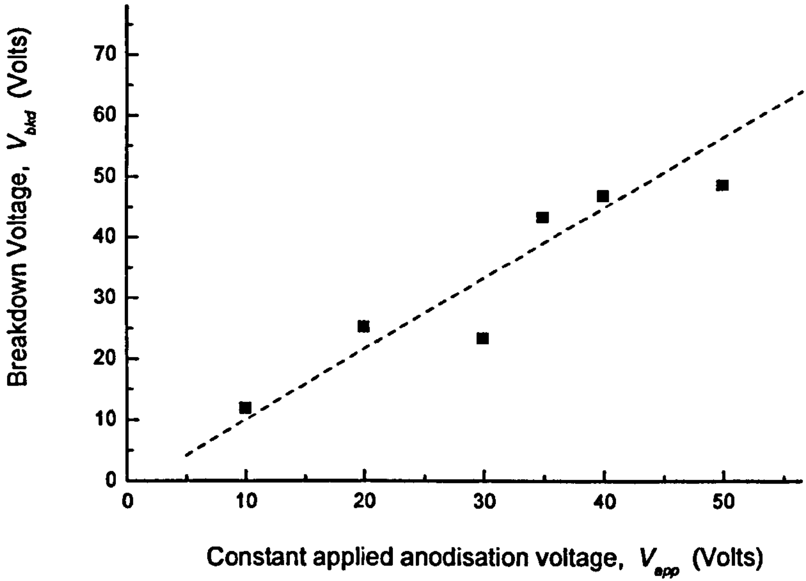


Figure 10: Breakdown voltages with different applied anodization voltages

The next question is how to make contact from the top metal layer to the bottom aluminium layer which is insulated by alumina. With chemical methods like the etching, it is difficult to remove the alumina layer and open a vertical hole for VIA contact without forming a defect to the bottom aluminium layer because the chemical characteristics of aluminium and alumina are similar. Also contact between aluminium and the other metal can be a problem since aluminium is not a stable metal in air and oxidises fairly easily. Relatively stable metals like gold or chromium are deposited before the aluminium to make an interconnection

between the aluminium and the other metal. Two possible VIA structures and their process design are introduced here with aluminium as the bottom metal and alumina as the insulator. The basis of these two VIA structures is to use a stable metal as the connecting layer with an aluminium gate layer and source/drain metal layer that can be laid out on it. The metal used for the connection layer is required to be compatible with the aluminium etching process and the lithography process. Also it should not be oxidized in air. Furthermore, the exposure of the metal connector to electrolyte will impact on the anodization process. At the beginning of anodization, after a very thin layer of alumina is grown on the aluminium surface, the dominant part of the current flow will be through the surface of the connector instead of the aluminium surface and the anodization process terminates. Therefore, the isolation of the connector during anodization needs to be undertaken. In first attempt, thick photoresist is employed to block the connector before anodization (Figure 11c) and removed after it (Figure 11d). Top metal layer (gold) is connected to the bottom gate with connector (Figure 11f). The minimum thickness of the photoresist is 2.5μm.

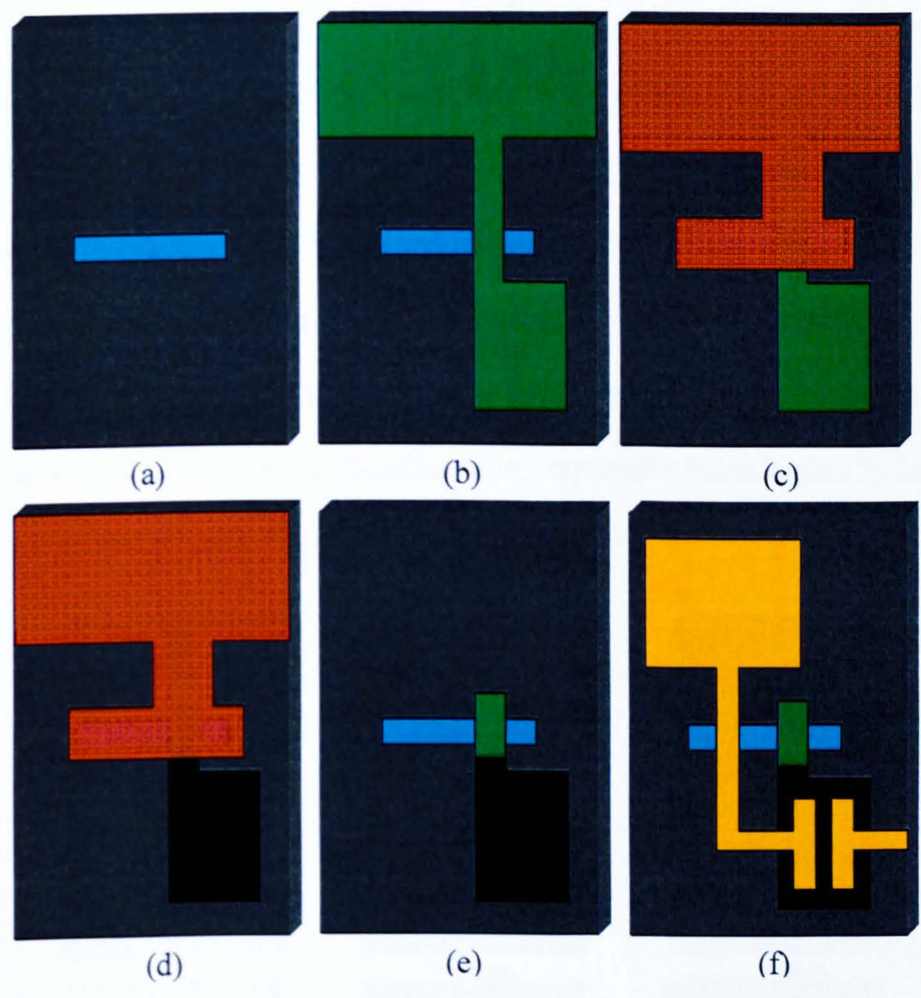


Figure 11: VIA process using thick photo resist to block connectors

4.4.2 Etching on chromium stop layer

In the second attempt, connectors were covered by an aluminium layer to prevent any contact to the electrolyte during anodization. Using etchant to remove aluminium and alumina, the VIA hole is opened on the connector (Figure 12d). The advantage of this VIA process is that anodization to grow alumina is more guaranteed since aluminium is the only material exposed to the electrolyte, especially when higher voltages are needed to grow thicker alumina.

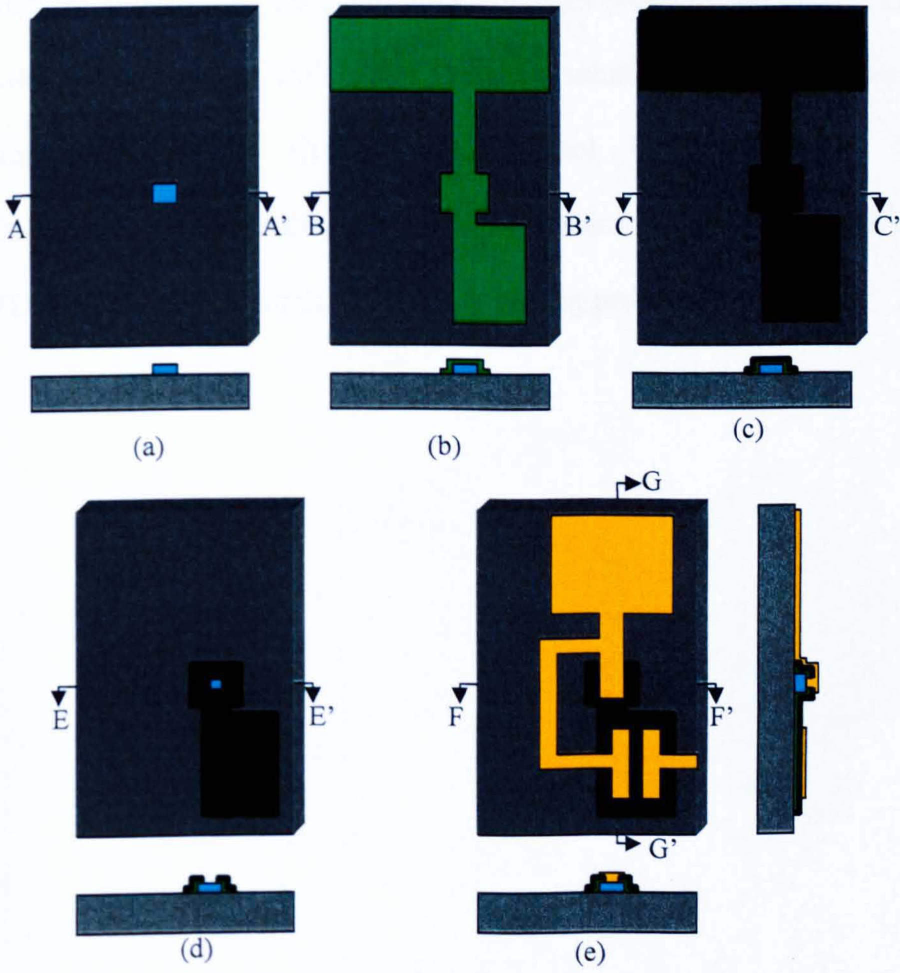


Figure 12: VIA hole by etching aluminium and alumina on bottom connector

4.4.3 Copper plating on aluminium surface

The aluminium can be easily anodized in air and in room temperature and its oxide has a similar reaction to both acid and alkali solutions. This brings the difficulty in opening VIA holes by removing selected alumina from the aluminium surface. Although by controlling the etching time (the aluminium oxide layer could be cleaned from the aluminium surface), the aluminium surface can still be oxidized in air again when it is taken out of the etchant solution. Plating copper on the aluminium is a possible solution to overcome the aluminium oxidation problem and make proper contact to aluminium via copper. The safer solution of copper plating on aluminium without Cyanide and Nickel is provided by EPI Electrochemical Products, Inc. [36]. The crossover of a transistor with VIA in Figure 13 illustrates the copper plating process.

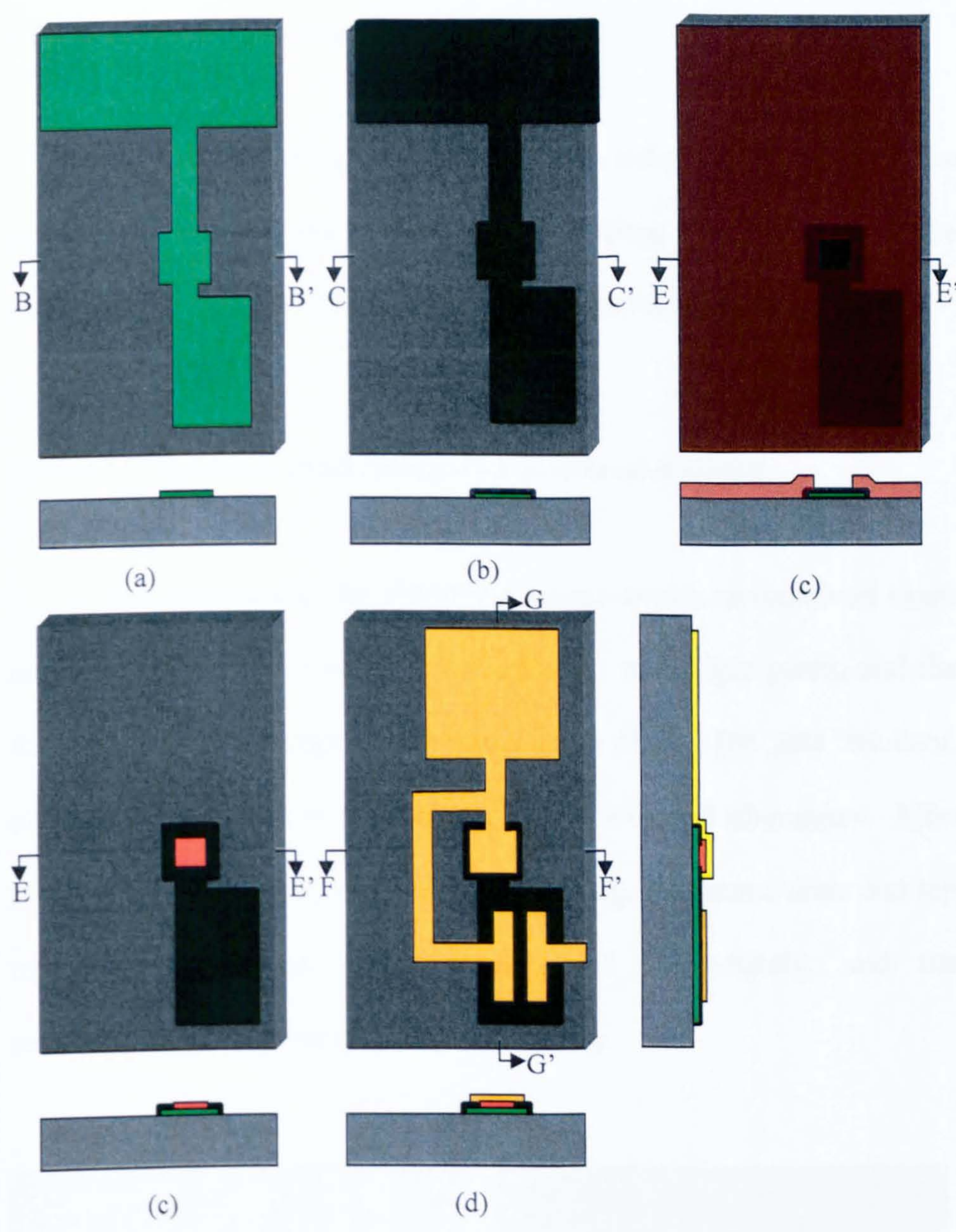


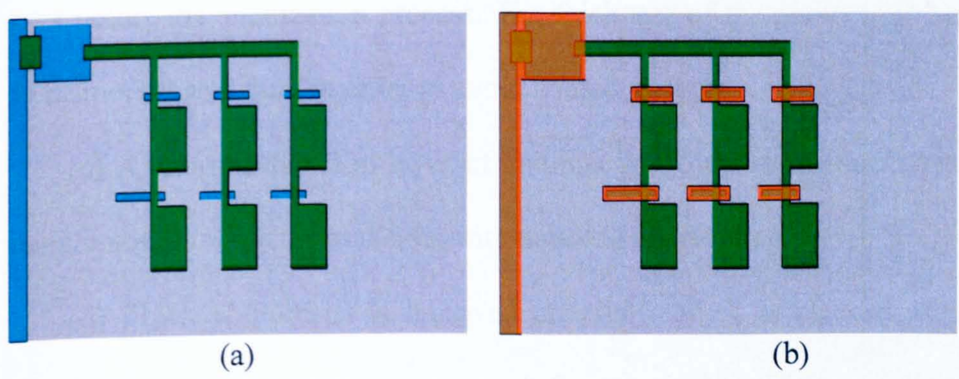
Figure 13: VIA process using copper plating on aluminium

4.5 Ring oscillator layout

With this insulating technology, VIA-hole and crossover are produced in the polymer circuit. To demonstrate the new process, the fabrication of a ring oscillator is illustrated as below.

Method 1: Selective anodization with photoresist shield

In this architecture, the chromium interconnections (coloured cyan) are defined first, followed by the aluminium gate (light green) and the thick photoresist (orange) as an anodization mask. The gate insulator, alumina (dark green) is then grown on the exposed aluminium. After removal the unnecessary connection by etching, the source/drain and top metal interconnection (gold) are defined immediately, and the semiconducting polymer is spun above the top.



(a) (b)

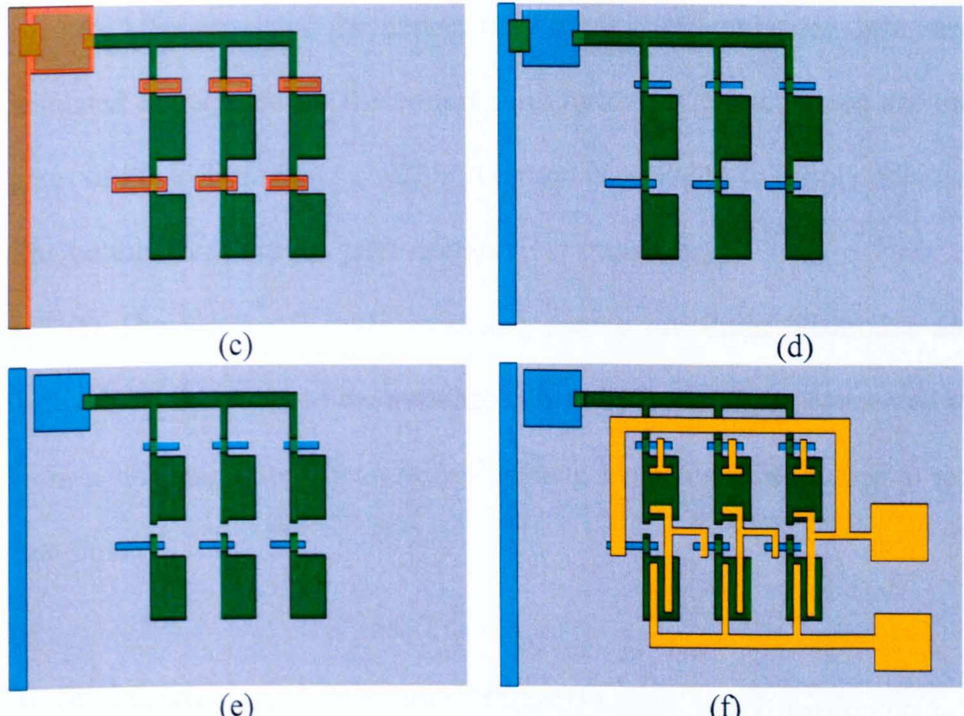


Figure 14: Manufacturing process using selective anodization for ring oscillator

(a) The bottom chromium layer (cyan) of interconnections and aluminium layer of gates deposited by thermal evaporation and the lithography process.

(b) Thick photoresist (orange) is patterned to cover all the chromium area before the anodization process. The thickness of the photoresist has to be more than 2.5um in order to avoid contact defects.

(c) A uniform thin film layer of alumina is grown on the surface of the aluminium, both top and side, with aqueous anodization.

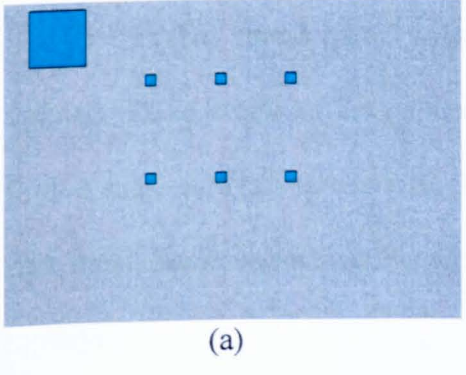
(d) Thick photoresist is removed and the surface is cleaned after anodization. Chromium connectors are left uncovered so that connections can be made through them to the anodized gates.

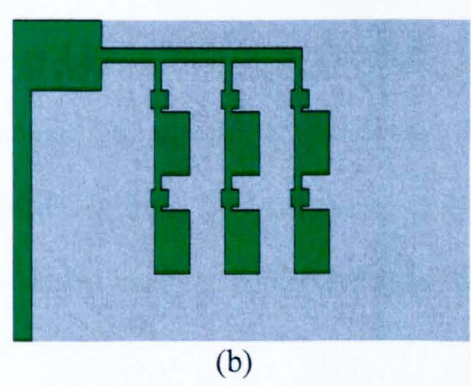
(e) After removing the unnecessary aluminium connector, gates are insulated as required by the circuit configuration. The top three are the gates of the load transistors with a common connection to supply voltage. The bottom three are the gates of the driver transistor.

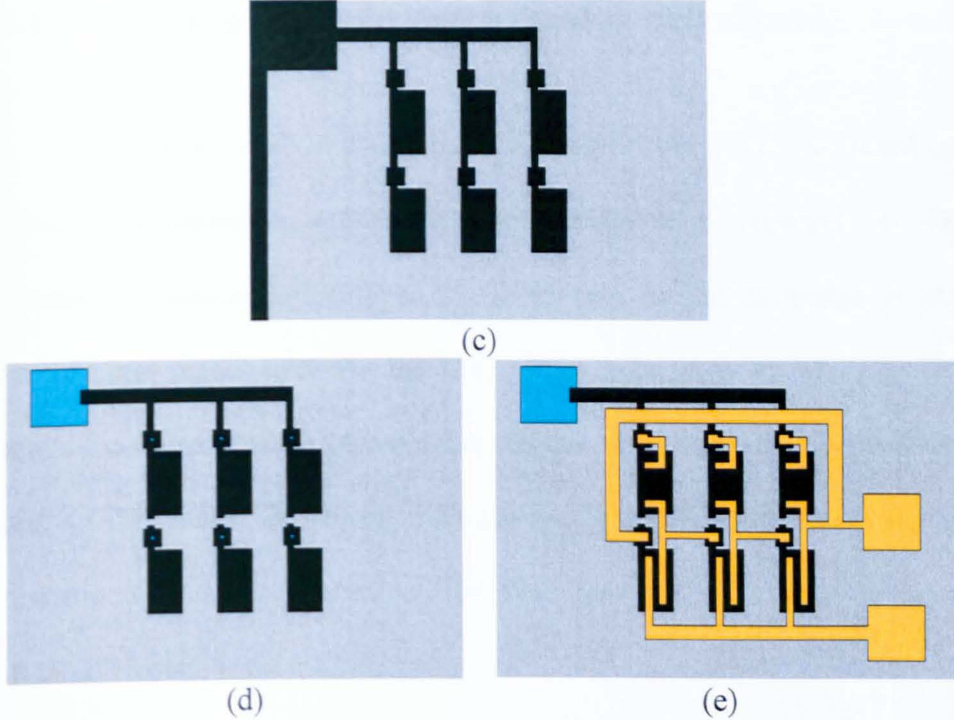
(f) The top metal layer including source are drain electrodes are defined. Three stages of the enhancement-load inverter are connected to form a ring oscillator circuit with feedback from the third output to the first input.

Method 2: Etching on chromium stop layer

In method two, the chromium interconnections (coloured cyan) are defined first, followed by the aluminium gate (light green). This is similar to method one, except that the aluminium gate covers all of the chromium patterns. Using the lithography process, the aluminium can be removed to make a VIA hole so that the connection between the bottom gate and the top gold source/drain electrodes (gold) can be built up as required.


(a)


(b)



(c)

(d) (e)

(a) The bottom chromium layer (cyan) of interconnections is deposited by thermal evaporation and lithography.

(b) A continuous layer of aluminium is deposited to cover all chromium interconnectors, and then patterned

(c) The aluminium is anodized which is the only metal exposed to electrolyte.

(d) VIA-hole opening and gate disconnected by the etching process.

(f) The top metal layer including source and drain electrodes is defined. Three stages of the enhancement-load inverter are connected to form a ring oscillator circuit with a feedback from the third output to the first input. Semiconducting organic material needs to be deposited as the top layer.

4.6 Photolithography mask design based on method one

Our first set of layout designs for the polymer circuit is based on selective anodization with thick photo resist as a protector of the chromium interconnection layer. In this section, the layout design of one set of eight masks used for the lithography process is introduced. The mask can be used for implementation of the ring oscillator, shift register and a CCD device. A vertical transistor, a logic gate circuit and various test structures are also included. The descriptions of the masks are listed in table below:

Table 4.1 Layers in photolithography mask for polymer circuit

Name	Description	Color
CHR	Lift-off Chromium layer off connectors and pads.	
ALU1	Aluminium layer for gate electrodes in transistors	
ALU2	Aluminium layer using as CCD electrodes	
ALU3	Another Aluminium layer for CCD devices	
ANOD	Patterned resist to protect chromium during anodization	
ETCH	Using in etching process to remove unnecessary aluminium	
AU	Gold layer for source/drain electrodes of transistors	
POLY	Top contact layer for CCD device	

4.6.1 Pattern for Alignment

With manual alignment equipment, the sample is held on a vacuum chuck and is carefully moved into position below the mask. There are

several lithography processes to be undertaken. A simple pattern is designed for alignment as shown in Figure 15 which includes a "half-full diamond" and a set of five crosses in different sizes. At the beginning, the "half-full diamond" patterns are used for the rough alignment between the two masks. Then crosses are used for fine alignment.

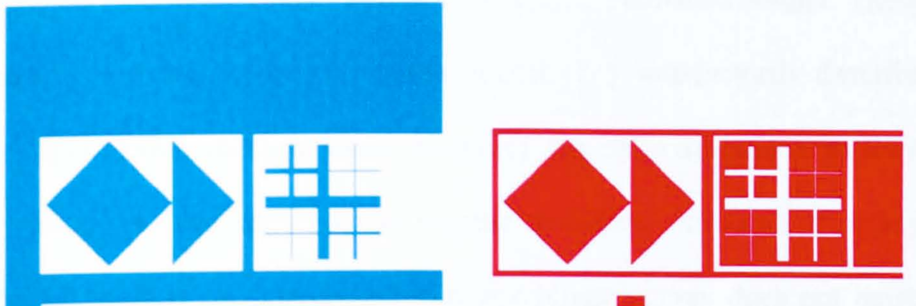


Figure 15: Patterns for mask aligning

4.6.2 Contact measurement structure

There are five layers of metal in this set of masks including three aluminium layers (ALU1, ALU2 and ALU3), one chromium layer and one gold layer. The contact between every two metal layers needs to be studied as well as the alumina between the aluminium layers.

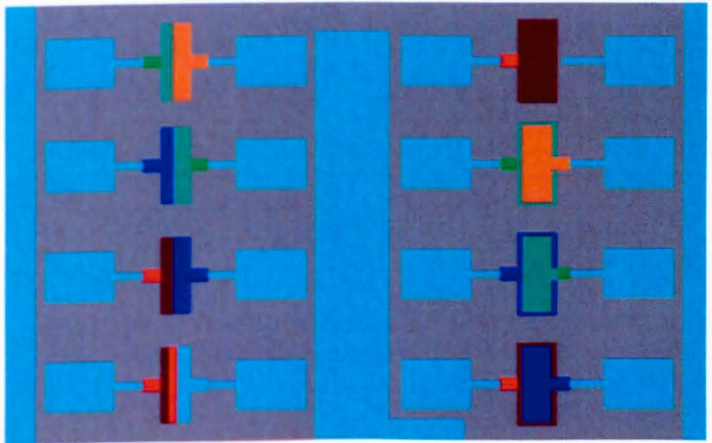


Figure 16: Structure design contact measurement

4.6.3 Parameter exaction for organic thin-film transistor

The parameters of the transistor including mobility, threshold voltage and constant contact resistance can be abstracted from the transfer characteristic of a stand-alone transistor. The basic equations derived for conventional transistors are used in most of the published results. These equations are easy to use and at first glance they satisfactorily describe the experimental characteristics. However the approximations in their derivations are not applicable to organic materials. Although a widely accepted method for interpreting current-voltage curves does not exist, some studies of extracting key parameters for organic transistors can be found from other researchers [37]. In this research, the new equation based on the power law is used. As shown in Figure 17 and Figure 18, a set of stand-alone transistors with different channel width/length ratio is designed for the device characteristic measurement of stand-alone transistors and transistor with connected source and drain.

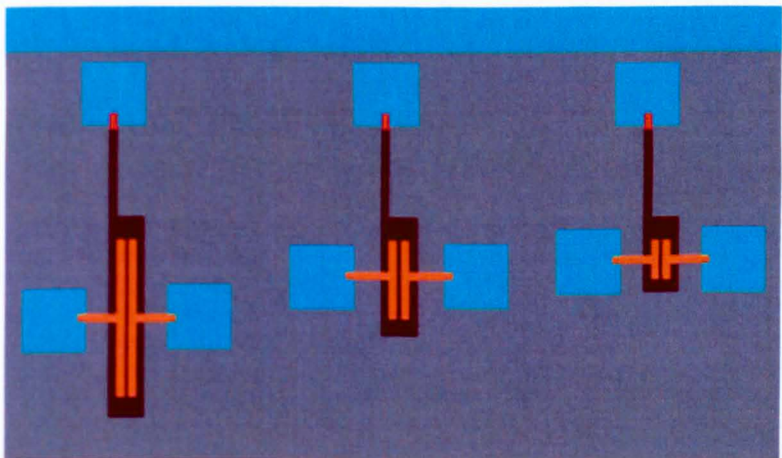


Figure 17: Stand-alone transistor used for device characterization

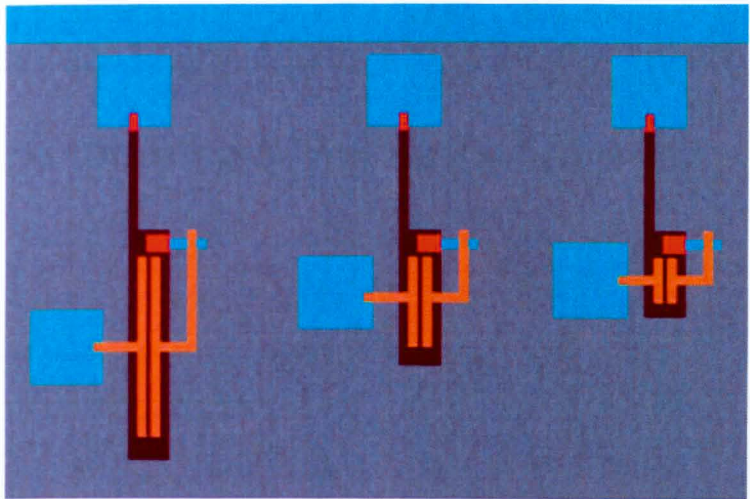


Figure 18: Transistors with gate and source connected

4.6.4 Speed measurement of ring oscillator

The measurement of the propagation time of ring oscillators is widely used to estimate the speed of transistor based circuits. Ring oscillators are constructed with an odd number of inverter stages. The reason we chose the ring oscillator as the test structure for speed measurement is not only that the identical inverters are the basic subcircuits in digital systems but also the crossover structure is not necessarily required in ring oscillation. A three-stage transistor and its layout are shown in Figure 19 as an example.

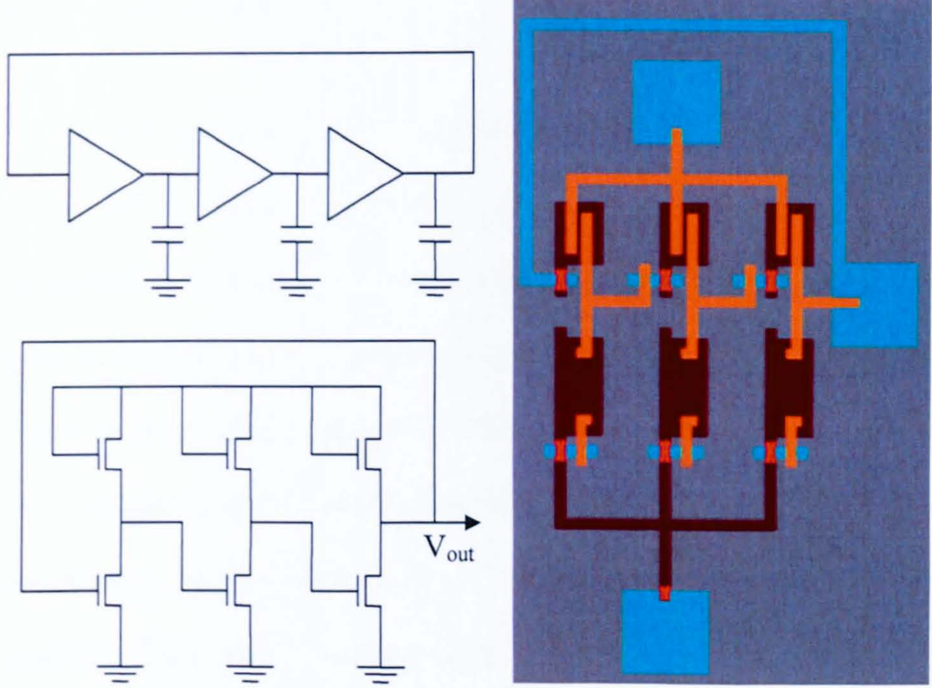


Figure 19: A three-stage ring oscillator and its layout

A ring oscillator consists of n inverters (n is a odd number) and the inverter delay time results to

$$\tau_{delay} = \frac{1}{2n \cdot f_{ocs}}$$

with f_{ocs} being the oscillator frequency. The optimised operating point with certain supply voltage and device ratio can be found from the simulation of the ring oscillator and verified by the experimental measurement. Adjustable DC voltage sources and a high-precision oscilloscope are in need for the practical testing.

4.6.5 Shift register

A shift register device includes transistor pass gates and latches connected in series and disposed along a data bit line; each latch connected to a corresponding transistor pass gate. Each transistor pass gate is controlled by a separate control signal input line that provides a signal to the transistor pass gate connected to it. The signals are provided in a staggered time pattern beginning with a latch disposed last in succession, shifting data from one position to the next succeeding position. Each latch is capable of storing one bit of data. Comparing to the random access memory using six transistors or a large capacitor for one memory bit, the shift register utilizes less space while reducing the amount of power consumed during operation. An example of a shift register including its circuit schematic (Figure 20) and layout (Figure 21) is given as below.

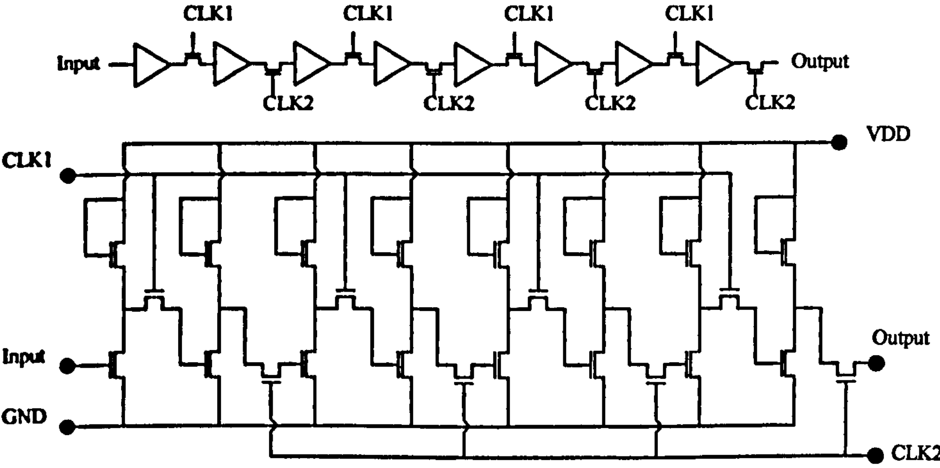


Figure 20: Schematic of shift-register based on saturated-load inverters

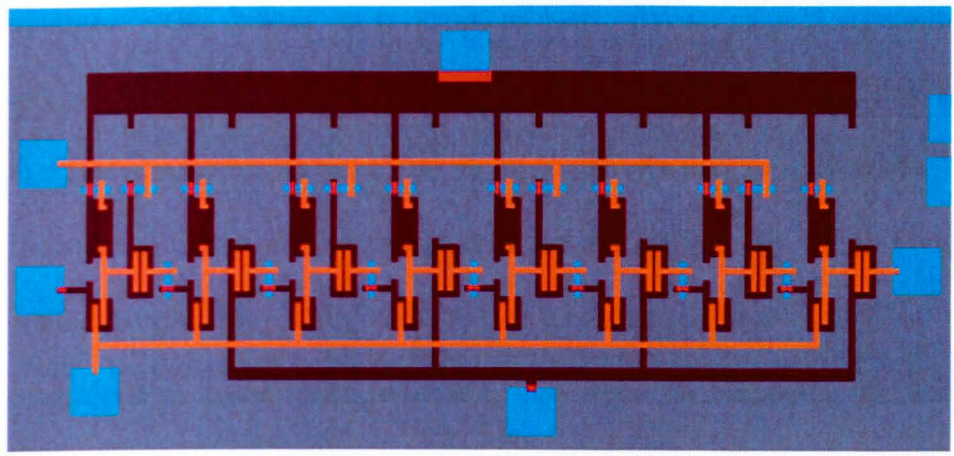


Figure 21: Layout of shift-register based on saturated-load inverters

As we can see the transistors in the layout are small, which might not be able to provide large current output since the mobility of the polymer is relatively low. The reason of this design with small source and drain electrodes is to lower the yield possibility on the overlapping area. Since this is a prototype design, it mainly focuses on the process verification and speed estimation. The speed of the circuit is inversely proportional to the channel length squared. A low-noise amplifier can be used to boost up the output voltage in circuit measurements.

4.7 Couple Charge Device

A CCD is a shift register in which sampled values of an analogue signal are stored in the form of charges on a series of capacitors. The concept of this semiconductor device was first introduced in 1970 by Boyle and Smith [38]. Charge is stored within the confinement of

potential wells created in a semiconductor. By moving the potential minima, the charge packets representing information, are moved through the semiconductor. Thus, a variety of functions can be performed by having the means of generating or injecting charge into the potential wells, transferring it through the semiconductor and detecting its magnitude at some other locations. The major applications for these devices are in: analogue signal processing where the charge can be injected and sampled at various points along the device; as imaging devices where the charge is generated under each electrode optically before being transferred for processing; and as serial memory devices. They are important for producing sequencers in RFID tags where parallel outputs from non volatile memory must be converted to serial outputs before being fed back to the antenna. In this section the basic principle of Charge Coupled Devices (CCD) is discussed with an emphasis on those fabricated with polymer technology.

The simple structure and process of CCD show the feasibility of producing CCD memory circuits with low-cost polymer circuit technology. A 3-phase polymer CCD is shown in Figure 22. The carriers are controlled by switching gate flow through the semi-conducting polymer.

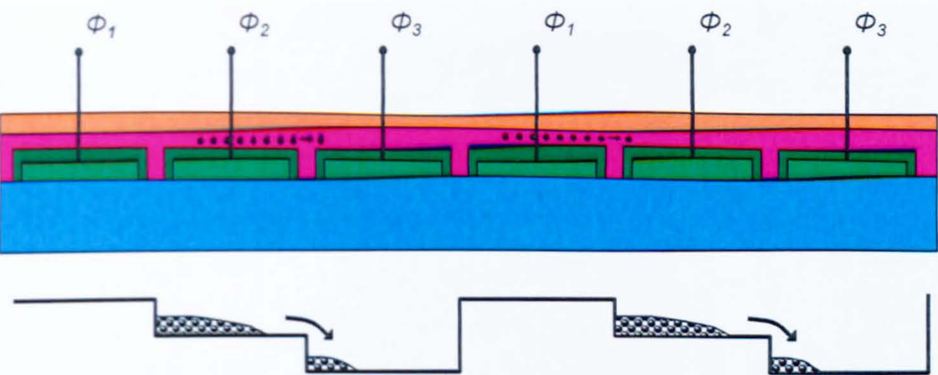


Figure 22: Three-phase CCD structure and charge transfer example

Using the lithography process, the size of small gaps between electrodes equals the minimum feature size. To avoid the need of making the small gaps required for the single-level structure shown in Figure 22, overlapping structure can be used to fabricate the three-phase CCD as shown in Figure 23.

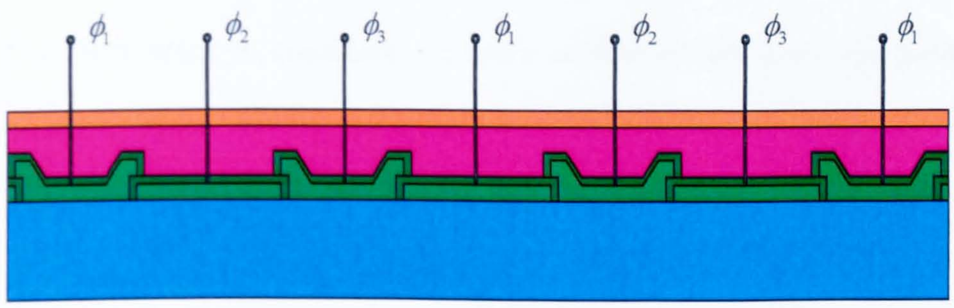


Figure 23: Three-phase CCD using overlapping levels of oxidized aluminium

Figure 24 shows a three-phase CCD together with its basic input and output structures. Electrodes are connected to three clock lines from the main body of the CCD.

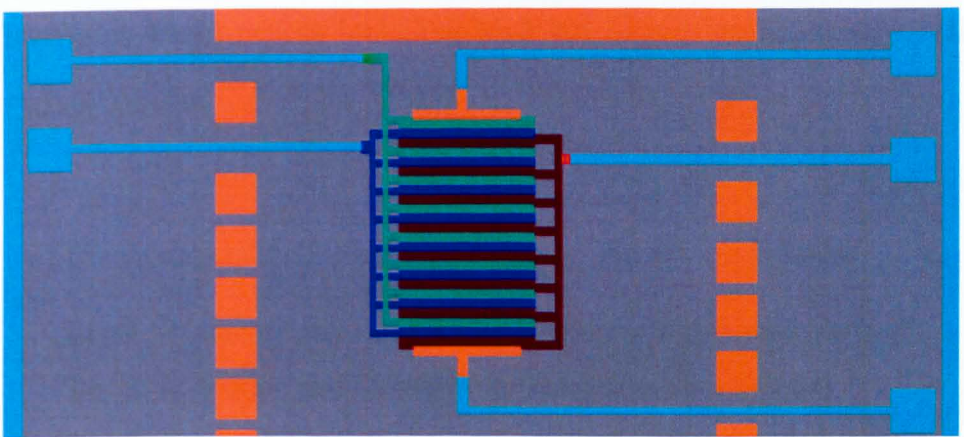


Figure 24: Layout of the three-phase CCD

The critical problem of CCD fabrication lies in the insulating layer between different electrodes. Although two-phase CCD requires less cross-over structures and VIAs, the two different gate insulating layers are required. Two insulating layers of two-phase CCD can be fabricated in different insulating material or in same material but different thickness. Our first attempt considers currently available dielectric materials, alumina, which can be generated easily by aqueous anodization. The various thicknesses of the alumina film can be obtained using various anodization voltages and time periods.

However, the unavoidable crossover required by the CCD device without any gaps challenges the current anodization process. New circuit technology including chromium interconnection and individual aluminium anodization has been tested to overcome the cross-over problem. Some crossover samples have been worked out with a view to

increasing performances including high breakdown voltages and small leakage currents.

The Process of the 2-Phase CCD device is shown as follows:

Step 1: Evaporate and Lift-off Chromium as interconnection layer
Step 2: Evaporate and lift-off first Aluminium layer (green)
Step 3: Long anodization to generate Alumina film (dark green)
Step 4: Evaporate and lift-off second Aluminium layer (red)
Step 5: Short anodization to generate second Alumina film (dark red)
Step 6: Selected etching off connector
Step 7: Evaporate and lift-off gold layer (orange) as input layer
Step 8: Cast or spin polymer as semi-conducting layer

From the cross-section shown below in Figure 25, we can see the insulating layers with different thicknesses. This structure is designed with two aqueous anodization processes which might cause the peeling problem. Another possible solution for making the two-phase CCD is to use a second insulating material such as an organic insulator.

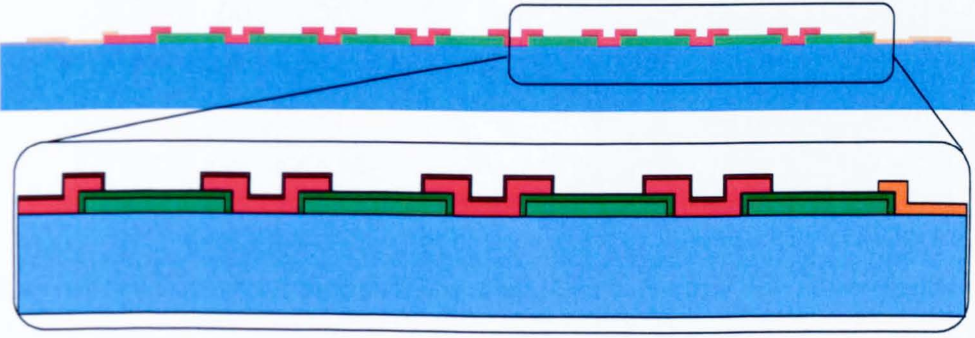


Figure 25: Cross-section diagram of two-phase CCD

The charge stored and transferred within the CCD must first be injected into the device before it can be transferred. The most commonly used method is usually called the "fill and spill" or potential equilibration method. Figure 26 shows the basic CCD structure together with the input diode, input gate, output diode and output gate which are the common elements that inject and detect charge packets. Figure 26 (b) shows the clock waveforms and output signal for the CCD, and Figure 26 (a) illustrates the corresponding potential wells and the charge distributions.

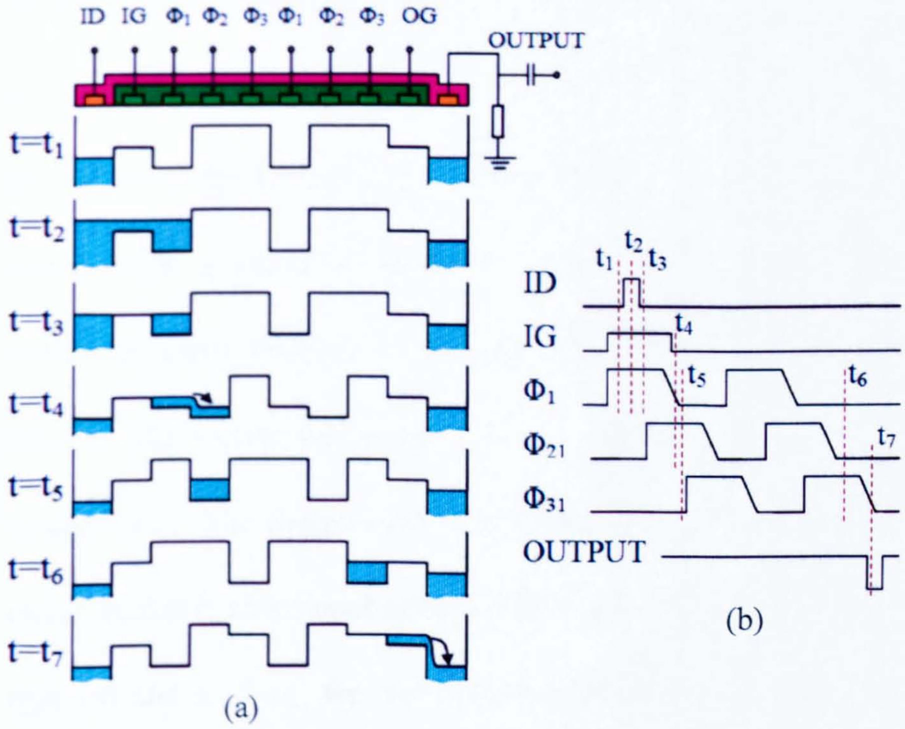


Figure 26: Signals and charge distribution of three-phase CCD device

At $t = t_1$, clock line ϕ_1 is at a high voltage and ϕ_2 and ϕ_3 are at a low voltage. The input diode (ID) and output diode (OD) are biased with a high positive inversion of the surface under the input gate (IG) and

output gate (OG). The potential well under ϕ_1 will be deeper than the potential wells under ϕ_2 and ϕ_3 because a higher voltage is applied to ϕ_1 at $t = t_1$. At $t = t_1$, the voltage of the ID is lowered so that the electrons travel through the IG. At the end of the injection, the surface potentials under the IG and ϕ_1 electrode will be the same as the input diode potential. Electrons are now stored under the IG and the first ϕ_1 electrode. At $t = t_3$, the voltage of ID is returned to a high value; electrons under IG and the excess electrons under the first ϕ_1 electrode. At $t = t_4$, the voltage applied to ϕ_1 is returning to the low value while the ϕ_2 electrodes have a high voltage applied to them. The electrons stored under ϕ_1 are then transferred to the ϕ_2 electrode because the surface potential under ϕ_2 is higher. This process is called charge transfer. The voltage on ϕ_1 has a slowly falling edge, because of the charge $t = t_5$. The charge-transfer process is completed and the original charge packet is now stored under the first ϕ_2 electrode. This process is repeated and at $t = t_6$ the injected charge packet is stored under the second ϕ_3 electrode. At $t = t_7$, the voltage of the ϕ_3 electrodes is returning to the low value and pushing the electrons to the output diode, thereby giving an output signal proportional to the size of the charge packet at the output terminal.

4.8 Vertical transistor

Compared to inorganic transistors, polymer field effect transistors normally have a poor performance with low current output and high operating voltages. This relatively poor performance results from the limit of minimum channel length and the inherent low mobility of organic semiconductor materials. Most of the polymer circuit applications, such as passive RFID tags and Organic LED displays, require a large current output and low threshold voltage in order to reduce the power consumption and increase the operating speed of the polymer circuit.

Since the speed of a transistor is inversely proportional to L^2 (L is channel length), various technologies have been developed to realize the short channel length in order to manufacture faster integrated circuits. It is however necessary to also limit the overlap capacitances as part of the basic structure processing. Conventional horizontal device design puts practical limits on the channel length. The conventional polymer transistor has a lateral relationship between the source and drain. Under this design, the space between the source and the drain needs to be minimized in order to reduce voltage needed and to increase current output. However, the fabrication techniques used to set the spacing between the source and drain leave the two electrodes relatively far apart,

thereby practically limiting the performance capabilities of the conventional horizontal transistor.

The vertical polymer transistor overcomes these limitations with its innovative architecture. Shown in Figure 27 this device architecture provides a very short channel length between the source and drain allowing low operating voltages and high current outputs. The channel length is determined by the thickness of the insulting alumina film between the source and drain layers. Similar to conventional top-contact transistors, the vertical transistor has its active layer between its gate terminal and moreover its source/drain terminals which have very small overlapping areas on the gate. These have given the vertical transistor the advantages of high speed with small overlap capacitors. Another noticeable advantage of this architecture is its potential feasibility in a low-cost reel-to-reel process. Unlike the horizontal transistor, the channel length in the vertical transistor depends on alumina thickness instead of the minimum feature size of the lithography process. Also the three terminals of the transistor are aligned and finalized using a one-off lithography process combining etching and the lift-off processes. This is very important because it is difficult to achieve accurate aligning with a small minimum feature size, also with low-cost equipments especially in reel-to-reel manufacturing.

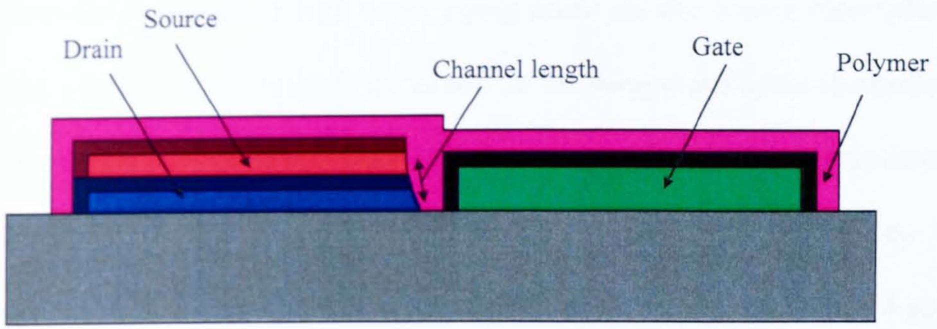


Figure 27: Cross section of vertical polymer transistor (a)

A critical problem in this structure is the anodization of the second aluminium layer. From the result of our experimental work, we have encountered the peeling problem in the aluminium anodization process on the top of anodized aluminium. Therefore an alternative structure of a vertical polymer transistor is designed as shown in Figure 28.

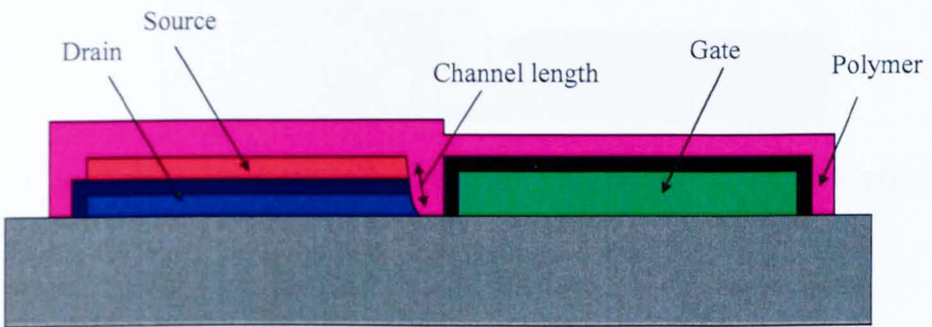
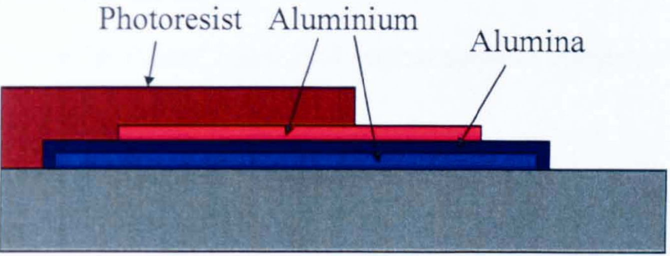


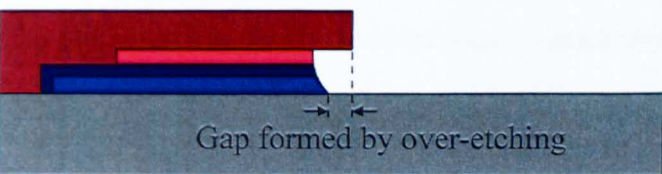
Figure 28: Cross section of vertical polymer transistor (b)

The manufacturing of a vertical transistor is designed with a sequence of three anodization processes, one etching process and one lift-off process. A complete process sequence is shown in Figure 29. First, the aluminium drain electrodes are defined and anodized so that they are insulated with an alumina layer. A second layer of aluminium source

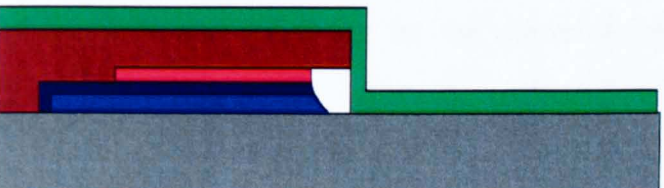
electrodes is deposited with overlapping areas on the source electrodes. Then a layer of photoresist is patterned on the source and drain electrodes. After this, a controlled etching process and a lift-off process on this same photoresist pattern is applied to generate the offset gap. The gap is required to be about 3 um to avoid contact defects between source/drain and gate electrodes.



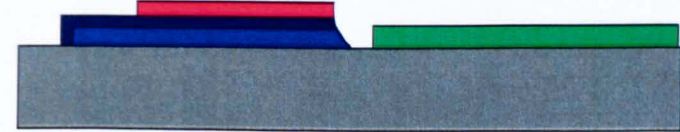
(a) Lithography process on two overlapping aluminium layers



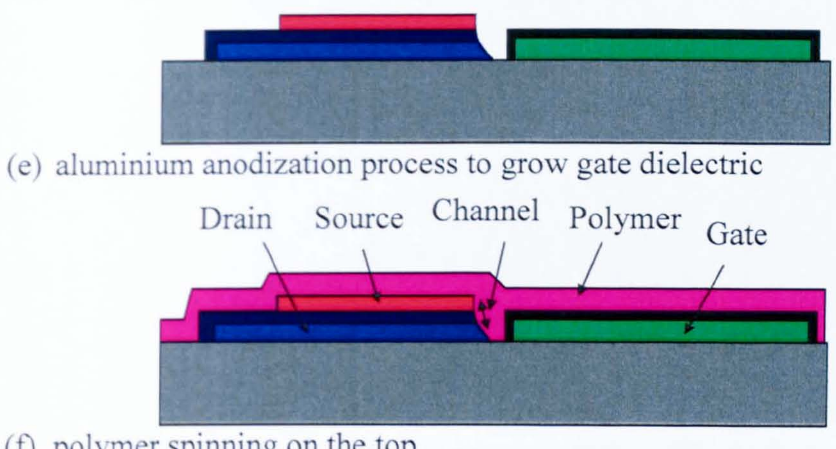
(b) over-etching process of aluminium and alumina layers to generate offset gap



(c) evaporation of gate aluminium layer



(d) aluminium lift-off process to from gate electrode



(e) aluminium anodization process to grow gate dielectric

(f) polymer spinning on the top

Figure 29: Process design of vertical polymer transistor

The drain current is proportional to the channel width. In order to increase the channel width in same area, a comb and fingers configuration as shown in Figure 30 could be used in mask design. In this configuration, every source/drain stripes are shared by channels on both sides. Therefore the overlap area between source/drain and gate electrodes is reduced to a half and the total area of the transistor is only two thirds of the total area taken up by the conventional transistor configuration.

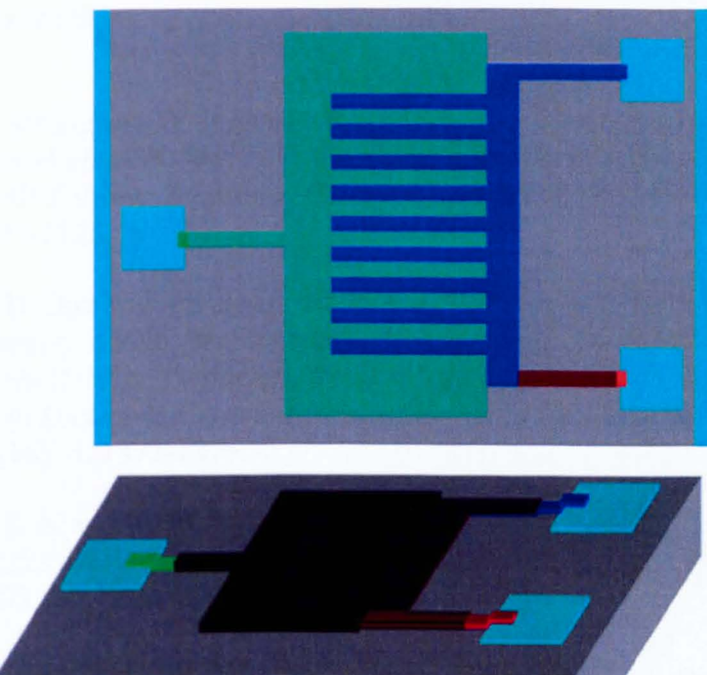


Figure 30 Layout of vertical polymer transistor

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Chapter 5

DISCUSSION OF THE EXPERIMENTAL RESULTS

Process prototyping and mask layout design are introduced in previous chapters. The experimental work was undertaken in a clean room environment to verify the process design and mask layout. Processing difficulties have been encountered in the experiments which are limited by our current available technology and materials especially in the lift-off and selective anodization processes. Some of these critical difficulties have been overcome using alternative methods. In this chapter part of the experimental result with photos are presented and the critical problems in processing will be discussed with solutions suggested.

5.1 Lithography and lift-off process

"Lift-off" is one of many conventional methods for patterning films that are deposited. A pattern is defined on a substrate using photoresist. A film, usually metallic, is blanket-deposited all over the substrate, covering the photoresist and areas in which the photoresist has been cleared. During the actual lift-off, the photoresist under the film is removed with solvent, taking the film with it and leaving only the film which was deposited directly on the substrate.

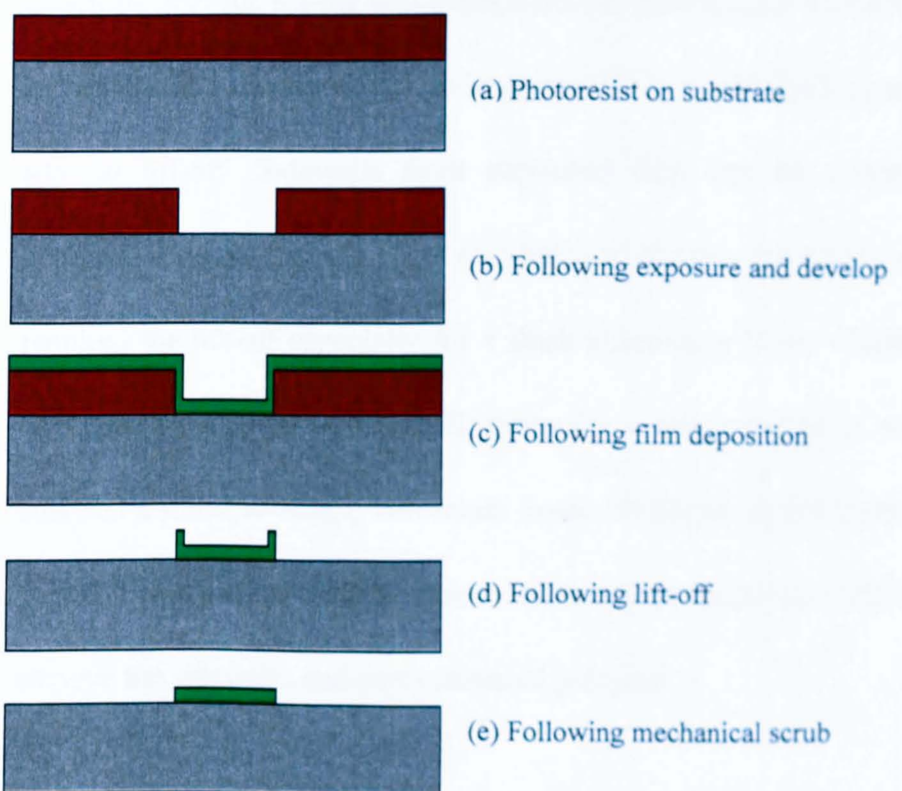


Figure 1: Standard lift-off process

The standard lift-off processing we used in our circuit

implementation involves only one mask step and the photolithography is completely standard. The main disadvantage of this method is that metal film is deposited on the sidewall of the photoresist and will continue to adhere to the substrate following resist removal. This sidewall may peel off in subsequent processing, resulting in particulates and shorts, or it may flop over and interfere with the etching or deposition processes which might follow.

Lift-off can be accomplished by immersing in acetone liquid. The length of time for lift-off will depend on the film quality. Generally, the higher the film quality, the more impermeable it is and the longer it will take to lift-off. Sidewalls from deposited film can be removed by applying ultrasonic gently. This also helps to shorten the length of time required for lift-off especially for a thick aluminium layer, which could have thickness of 200-400nm. However for a pure gold layer which is soft and a thin (50-80nm) chromium layer, ultrasonic might increase the peel off problem. A directed stream of deionised water can also help to remove the sidewalls and particulates of polymer.

The minimum feature size which is limited in this process, has to be considered in the circuit mask design. Transistor gate lengths usually

have a minimum value for the process. To reduce the unexpected transistor capacitance and resistance, the transistor gate width needs to be as small as possible. Therefore with a fixed gate width-length ratio, the gate length is required to be the minimum feature size.

Minimum feature size obtained in our current lithography and lift-off process is 5 μm. When the gap is less than this minimum feature size, the required pattern may not be able to be obtained. As an example shown in Figure 2, the gaps between the electrodes are designed to be 5μm. But the edges of the patterns are not straight and sharp enough and parts of the metal pattern are connected together, which damages the function of the circuit.

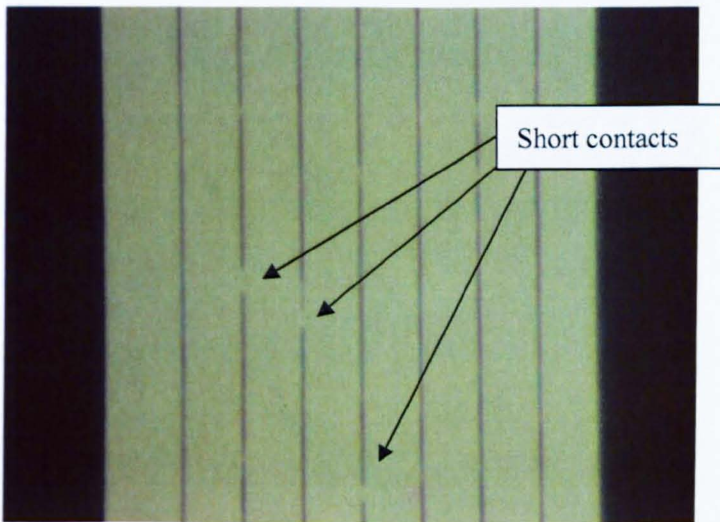


Figure 2: Unexpected short contacts occur in lift-off process

Another critical problem I have faced during the clean room work relates to the lift-off process of gold for source and drain electrodes. The gold layer is soft and it doesn't stick very well on the glass. It peels off easily from the sample during lift-off and the cleaning process, especially when the gold layer is not the first metal layer. In most of the research, gold source/drain configuration has given a good ohmic contact to polymer materials and the dimension of source/drain electrode is designed to be small so that the overlap capacitance can be reduced as much as possible. This kind of TFT configuration with gold source/drain electrodes will increase the probability of the peal-off occurring during the lift-off process.

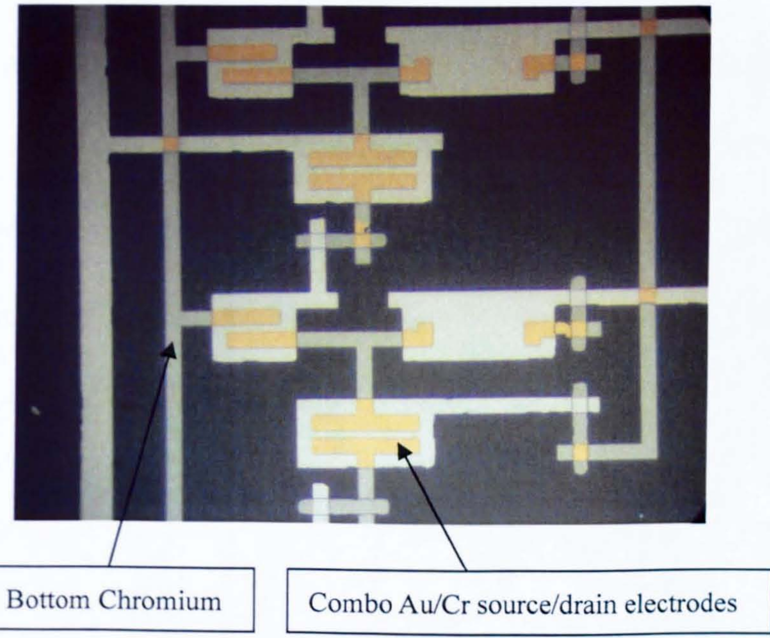


Figure 3: Gold/Chromium source/drain electrodes

To overcome this problem, a thin layer of chromium is used as adhesion layer. The source/drain layer is formed with a sandwich layer of bottom chromium and top gold which is evaporated and patterned with the lift-off process. As shown in Figure 3, the source and drain electrodes of the gold and chromium are well patterned and the gold source/drain electrodes remain on the transistor after lift-off. The minimum channel length shown in this photo is 10 μm.

Another attempt was undertaken with adhesion promoter, Hexamethyldisilazane (HMDS) which is widely used in the semiconductor industry to improve photoresist adhesion to oxides. The HMDS reacts with the oxide surface in a process known as silylation, forming a strong bond to the surface. At the same time free bonds are left which readily react with the photoresist, enhancing the photoresist adhesion. This process works not only on silicon dioxide, but other oxides (Al_2O_3 in this case) as well.

5.2 Aligning error

An alignment error between different layers is another unavoidable problem which we need to consider in our mask design. The aligning error is controlled to be less than 10 μm using gradual aligning with a set of crosses in different sizes. Using a digital camera the alignment error can be observed (Figure 4). The aluminium layer (in white colour) overlaps with the chromium layer (in gray colour) and the offset difference is not noticeable in this photo. The smallest stripe on it is 5 μm.

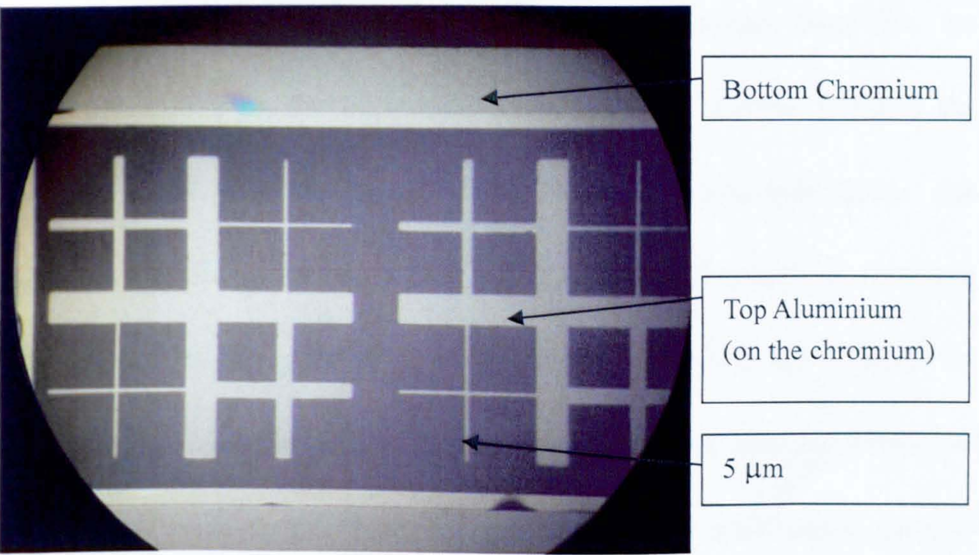
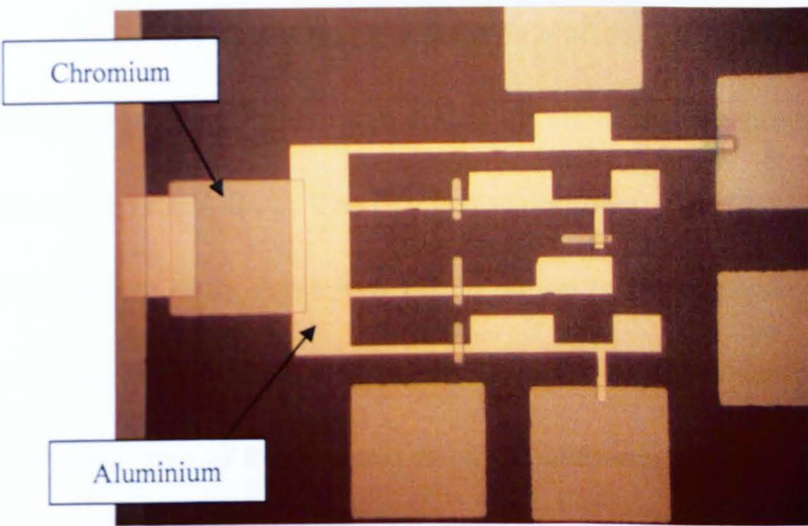


Figure 4: Alignment error observed though a digital camera

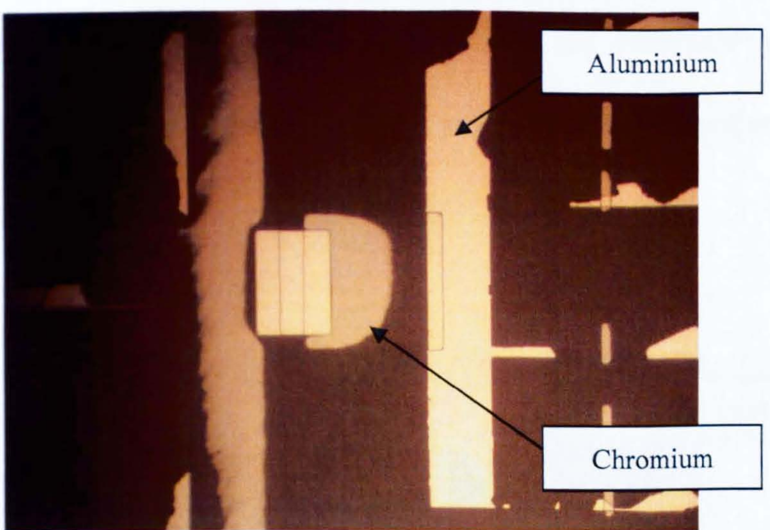
5.3 Selective anodization process

Aqueous anodization is one of the most critical processing we met in the circuit implementation. The gate dielectric which critically determines the device performance is grown using this anodization process. Also the anodization is required by the circuit crossover structures in circuits. However this process is different from the one used in device characterization because the aluminium layer has been patterned in prior to anodization.

Furthermore aluminium is not the only metal on the substrate during the anodization process, since we used a chromium layer for the interconnections on the bottom of the aluminium. Figure 5 shows the photos which were taken on a sample with aluminium gates and chromium interconnections before and after the anodization. As shown in Figure 5(b), a big part of the chromium is etched off during the anodization since chromium is more chemical active and the density of chromium oxide is not high enough to stop the anodization process (unlike the aluminium oxide).



(a) before anodiaztion



(b) after anodization

Figure 5: Etching during anodization on aluminium and chromium

After research on similar applications [1], it was decided that photoresist should be used to protect the chromium layer during the anodization process. Two test experiments were undertaken to check the feasibility.

In order to validate that the resistance of the polymer layer is high enough to protect the chromium during the anodization process, a number of tests were carried out. The first test experiment is designed as follows. We evaporate some aluminium stripes on top of the chromium connecter using the shadow mask. Photoresist is spun on the sample, and after developing, part of the photoresist on the aluminium stripes is removed. The chromium connector is connected to the anode of the voltage source so that anodization current can be provided via the connector to the aluminium stripe. The sample is then put into the electrolyte for anodization.

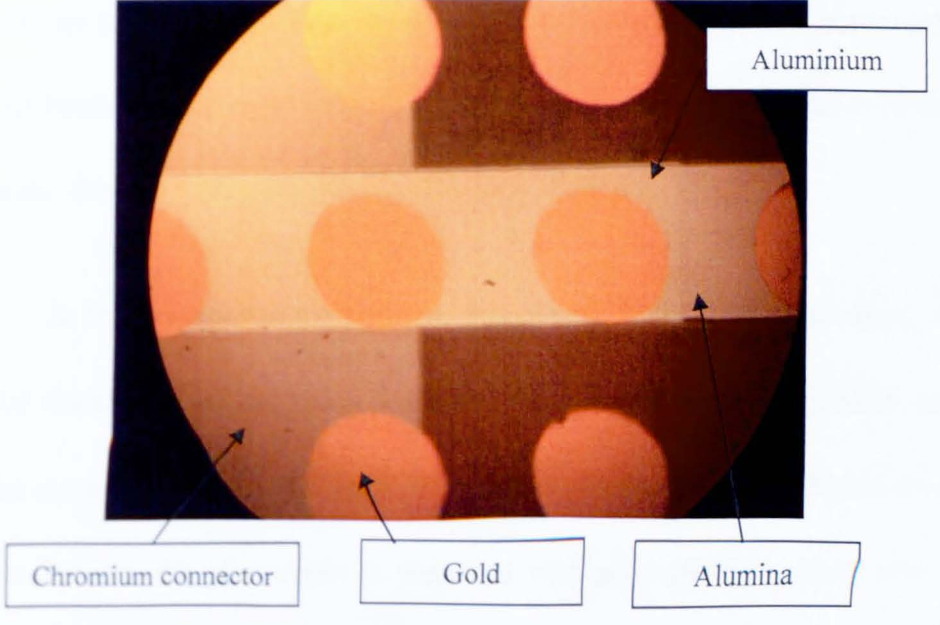


Figure 6: Selective anodization test experiment

Figure 6 shows the result of anodization. Gold dots are deposited using a shadow mask in order to make contacts for IV measurement. As shown in Figure 6, aluminium stripes have been anodized without any defects. The edges of the alumina are clear. From the IV measurement on two of the gold dots, the alumina layer grown on the aluminium stripes has shown its high dielectric strength as a gate insulator. The dimentions of the gold dots and the width of the aluminium stripes are about 2 mm which are much larger than the circuit component. Another discovery from this experiment is that the anodized aluminium stripes look slightly smaller than their original size once a thin layer of aluminium on the surface has been anodized into transparent alumina. This might result in a smaller size of layout than expected. Therefore a second test experiment has been undertaken to help us to observe the anodization process on the small devices with minimum feature size of 10 μm.

In the second test experiment, a layer of photoresist is patterned on the aluminium surface using a standard lithography mask. This mask has the same scale of size as those we used in polymer circuit layouts. After anodization, the photoresist is removed with photoresist remover and a well-defined alumina pattern is shown on the aluminium in Figure 7. The

changing of pattern is not noticeable.

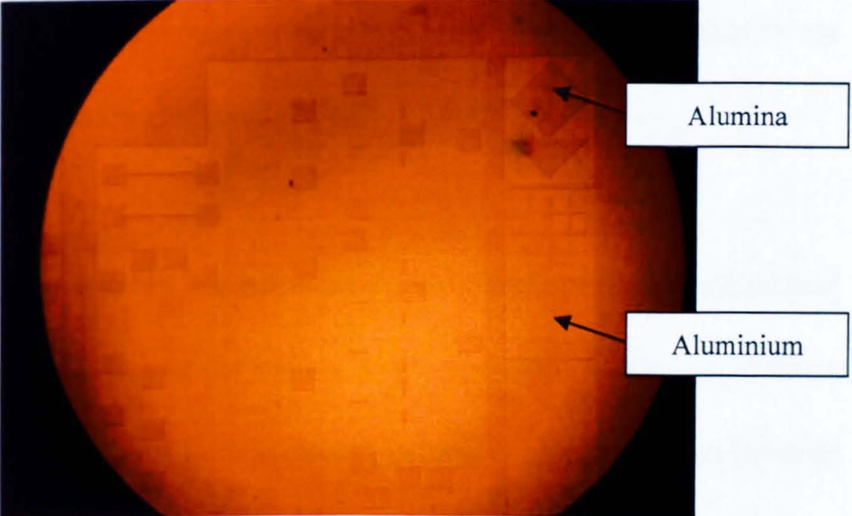


Figure 7: Alumina pattern on aluminium from anodization with photoresist

Although we have successfully undertaken the test experiments to verify the feasibility of a designed selective anodization process with photoresist protection, there are still some differences between the test experiments and the proper circuit anodization process, which might cause unexpected problems. For test one: the components are not the same scale as those we used in our circuit. The scale of the test structure is about 2-4 mm while the components in the circuit are in scale of 10-40 um. For test two: although the photoresist layer has been patterned into a similar scale, there are not suitable masks for the bottom chromium layer. Hence we cannot examine the anodization on the chromium layer with photoresist protection with this mask.

The anodization at the edge of the pattern could damage the photoresist. This could be a problem when the photoresist pattern is not much bigger than the chromium layer.

After these two text experiments, an additional mask is designed and made as a shield for the chromium layer. According to test experiment two, the size change of the aluminium pattern is about 5 μm so the size difference is suggested to be 10um. As shown in Figure 8 the chromium layer is covered by a photoresist layer.

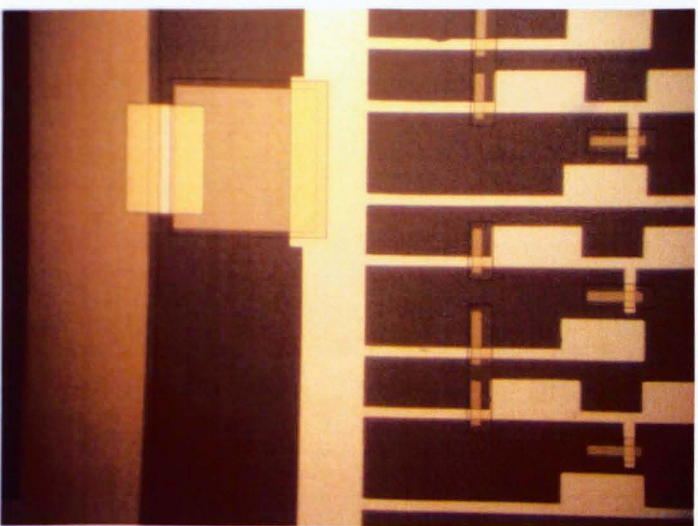


Figure 8: Photoresist pattern as protection for chromium

However as shown Figure 9, the photoresist layer also *peeled off* during anodization. The reason for this could be one or a combination of the following: The dielectric constant of the photoresist is perhaps not

high enough to protect the chromium. The photoresist patterned with the lithography process is not perhaps thick enough or the edge difference may not be big enough to avoid contact defects. Physically, the photoresist does not stick on the chromium surface very well especially when it is dipped into electrolyte and another effect is that the chromium surface gets hot when a current flows thought it.

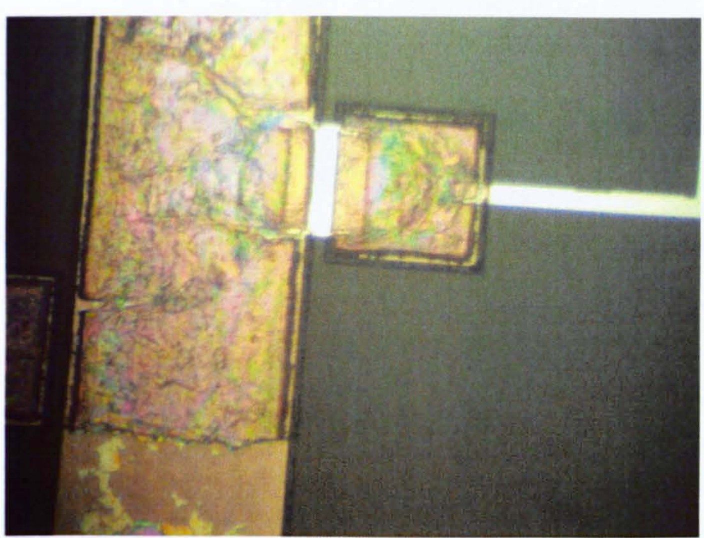


Figure 9: Photoresist layer peels off after anodization

One suggested solution of this problem is a longer hard bake time (two times the normal process time, about 12 minutes) and higher hard bake temperature, 120°C. This has been tried to improve to the resist stability and its dielectric performance. The result of the experiment didn't show too much improvement and the problem still exists.

Later, a thick photoresist material, AZ4562 has been tried. As claimed on the specification, a photoresist layer with a thickness of 6-8μm could be obtained with a normal lithography process. However from the following photo, the pattern is not very clear and accurate. There are a lot of remnants left on the aluminium surface which might decrease the smoothness and dielectric performance of the alumina layer grown on it.

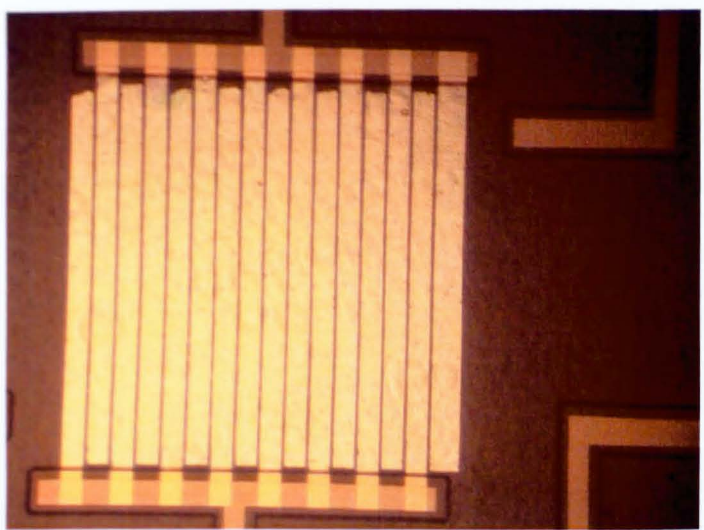


Figure 10: Thick photoresist as anodization protection

Using weak citric acid solution as an anodization electrolyte with a low supply voltage (5-10*V*), the peeling problem is relieved, but it results in a low breakdown voltage and a long anodization time (30 minutes). For a proper solution for polymer circuits, a stable organic insulator with

greater thickness and stability in the electrolyte during anodization is required. A possible option can be thick PVP or polymide deposited by inkjet printing. Note here a high accuracy pattern of these organic insulators is not necessarily required as they will be removed after anodization and it can be left big enough to avoid the defects due to the aligning error.

5.4 Reference

1. T. Arai, H.I., Y. Hiromasu, M. Atsumi, S. Ioku, K. Furuta, *Aluminum-based gate structure for active-matrix liquid crystal displays.* IBM Journal Of Research And Development, 1998. 42(3-4): p. 491-499.

Chapter 6

CONCLUSION AND RECOMMENDATION FOR FURTHER WORK

This chapter summarises the main conclusions in the thesis, future works needed in circuit development with an easy manufacturing process and compatibility of future possible applications.

6.1 Conclusions

The charge transport of the carriers in P3HT is thought to be best described by the Variable Range Hopping (VRH) model proposed for the most amorphous organic semiconductors. The mobility of the polymer increases with increased doping density obeying the universal mobility law. A new drain current equation has been developed based on this relationship. Experimental data obtained for a doped P3HT (Poly(3-hexylthiophene)) TFT and PTAA (Polytriarylamine) TFT produce a better fit to the new equation than the conventional gradual channel equation. For the new equation the values of m and K for P3HT and PTAA were 0.675 and 2.267×10^{-26} (in SI units), and 0.265 and 1.063×10^{-16} (in SI units) respectively.

Reusable subcircuits with polymer technology such as a current source, a current mirror and an inverter with active load are studied. However with the new drain current equation, the symbolic expressions of circuit speed are difficult to obtain because of un-reducible integrals introduced by the power law. Therefore a numerical simulation method with the mathematic package MathCAD is developed and a simulation of a charge/discharge process via an inverter is presented as an example.

Prototype design of the polymer circuit is the main task. Nowadays there is much research on polymer devices including different technologies, such as low cost and simple processes for integration into a circuit. The polymer circuit process is designed based on our existing research of polymer TFTs using aqueous anodized aluminium as the gate. The advantages of this kind of transistor are low threshold voltage and small area capacitors.

According to the process design, one set of eight lithography masks have been designed with the Cadence virtuoso layout system. This layout design includes a ring oscillator, a shift register and a CCD device. Some test structures and subcircuits are also included in the mask design.

Our circuits can be well defined by using mature lithography technology, unlike inkjet printing technology used by others. High smoothness of the metal surfaces also promises a good contact between polymer and source/drain electrodes. Several photo resist materials and an adhesion promoter, HMDS (Hexamethyldisilazane) have been employed to improve the quality of the lift-off process.

As an innovative design, a selective anodization process has been developed in this research to overcome the contact defects which occurs on the chromium. Two different photoresist materials have been evaluated as protective layers in the anodization process. The result is not satisfactory because the polymer layer peels off during the anodization process. Two test experiments have been setup to investigate this problem. The results show the problem could be that the resistance of the polymer layer is not high enough, either because of their low or high dielectric strength. Therefore good-quality thick photoresist with a high dielectric strength is required.

6.2 Future work

The stability of a circuit and device is one of the most important aspects of reliability. As it was noticed, polymer devices such as TFTs have characteristics that are not ideal due to several possible forms of instability which can be caused by the movement and trapping of charge carriers. They appear to be the result of the ingress of ambient gases. Also they may be produced by the introduction of impurities during the manufacture of the device. One of the most noticeable instabilities of the polymer transistors is that performance rapidly degrades on continual exposure to air. This includes falling mobility, shifting threshold voltage and increasing off-current with time. Most of these instability effects cannot be fully explained and modelled, but the changing of the basic design parameters of the device has to be taken into account in circuit design. Therefore as a suggestion for further research, modelling of devices with time and temperature dependence is necessary. Polymer circuits with fault tolerance can be designed and simulated with these device models. Also in system level design, self-testing and self-repairing functions with duplicated components can be integrated to improve the stability and lifetime of the circuit.

The device modelling work requires a further analysis of the conduction mechanism of organic material. A physically meaningful model for more or less ordered materials is important for comparison.

The process development in this PhD work is based on conventional lithography and the anodized gate dielectric. These processes provide reasonable device performance with high quality dielectrics and small channel length. Also three sets of circuit manufacturing processes have been developed based on this device technology. More clean room experiments need to be undertaken to evaluate these processes. However, to meet the requirement of future low cost polymer circuits on flexible substrates, current manufacturing processes on glass need to be transferred to be compatible with flexible substrates and reel-to-reel processing. Further work should extend the device developments on flex to the use of flexible substrates. Different deposition methods on flexible substrates have been demonstrated by other research groups. Among these, the soluble processing, such as inkjet printing is considered as the most compatible to the future large-area and flexing applications. However, this kind of process suffers from poor surface quality and large channel length. Maintaining good performance after the whole process of

integrating our transistors is a major target. Inkjet lithography can be our next step on polymer TFT circuit development, although the limitation of feature size suggests that it may only be used to provide electrically isolated transistor islands.

Finally, once a stable TFT circuit with improved performance is visible; innovative device structures i.e. organic Charge Couple Devices (CCD), it is a potential structure for ADC and dynamic memory which may have value as a sequencer in RF chip design. The speed of the CCD circuits could be much faster than those based on TFTs with a higher output. Vertical transistors with short channels could overcome the relatively poor performance results from the inherent low mobility of organic semiconductor materials but reduction of an overlap capacitance is an equally high priority. The architecture of the vertical transistor could enable two key electrical performance characteristics; a high working current and a low operating voltage.

Overall the integration of components at low cost and small feature size has top priority and this will be the focus of research worldwide in the coming decade.

Appendix A

DERIVATION OF THE DRAIN CURRENT EQUATION OF POLYMER TRANSISTORS

The derivation of the polymer transistor model comes from the study of conduction mechanism and carrier concentration in polymer materials. Some assumptions and estimations have been made to simplify the analysis.

Step (A)

The common current density equation can be written as

$$J = nq\mu E_x \tag{A.1}$$

where n is the carrier concentration, E_x is the electronic field applied along the current direction x and μ is the field effect mobility. Here we introduce the semi-empirical relation between the mobility and the carrier concentration in polymer which can be expressed as a power law,

$$\mu = Kn^m$$

where K and m are the constants which depend on the material.
Also. we will assume that the carriers follow an exponential distribution with energy (instead of the normal-used Gaussian carrier distribution):

$$n = n_0 \exp\left(q\phi/kT\right)$$

This reflects the assumption that the conduction in disordered polymers mainly happens in the lower energy levels.

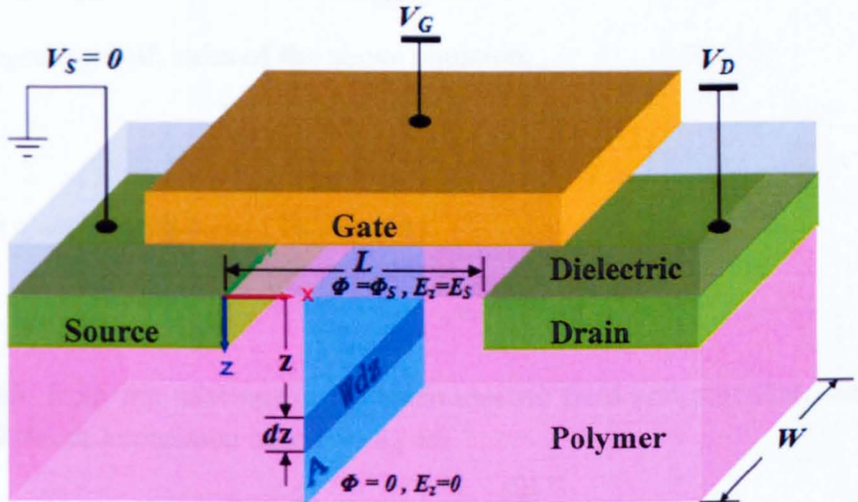


Figure 1: The 3D structure of the polymer transistor

Therefore we can find the current which flows through an arbitrary cross section WdZ as shown in the Figure 1.

$$dI = WJdz = Wnq\mu E_x = WqKn^{m+1}E_x$$

$$dI = WqK{n_0}^{m+1}\exp\left[(m+1)\left(q\phi/kT\right)\right]E_x dz \tag{A.2}$$

Step (B)

Employ Poisson equation on the half-space from infinite-far to surface z,

$$\frac{d^2\phi}{dz^2}=-\frac{\rho}{\varepsilon_{poly}\varepsilon_0}=-\frac{-qn}{\varepsilon_{poly}\varepsilon_0}=\frac{qn}{\varepsilon_{poly}\varepsilon_0}$$

From the relationship between electric field and potential, we have

$$\frac{dE_z}{dz}=-\frac{d^2\phi}{dz^2}=-\frac{qn}{\varepsilon_{poly}\varepsilon_0}$$

$$dE_z=-\frac{qn}{\varepsilon_{poly}\varepsilon_0}\cdot dz$$

$$E_z\cdot dE_z=\left(-\frac{qn}{\varepsilon_{poly}\varepsilon_0}dz\right)\cdot\left(-\frac{d\phi}{dz}\right)=\frac{qn}{\varepsilon_{poly}\varepsilon_0}d\phi$$

$$E_z\cdot dE_z=\frac{qn_0}{\varepsilon_{poly}\varepsilon_0}\cdot\exp\left(q\phi/kT\right)d\phi$$

Integrating both sides of the above equation,

$$\frac{E_z^{\,2}}{2}=\frac{qn_0}{\varepsilon_{poly}\varepsilon_0}\cdot\frac{kT}{q}\cdot\left\{\exp\left(\frac{q\phi_z}{kT}\right)-1\right\}$$

The electric field E_Z can be found as

$$E_z\simeq-\sqrt{\frac{2kT}{\varepsilon_{poly}\varepsilon_0}}\cdot\sqrt{n_0\exp\left(q\phi/kT\right)}$$

Again from the relationship between electric field and potential, we can find the dz expression based on E_Z as,

$$dz=-\frac{d\phi}{E_z}=\frac{d\phi}{\sqrt{\frac{2kT}{\varepsilon_{poly}\varepsilon_0}}\cdot\sqrt{n_0\exp\left(q\phi/kT\right)}}$$

Substituting the dz in equation(A.2), we have

$$dI=WqKn_0^{\,m+\frac{1}{2}}\exp\left[(m+\frac{1}{2})(q\phi/kT)\right]E_x\sqrt{\frac{\varepsilon_{poly}\varepsilon_0}{2kT}}d\phi \qquad \text{(A.3)}$$

Step (C)

Integrating Φ from 0 to Φ_s, where Φ_s is the surface potential of polymer at the interface between the polymer and the dielectric as shown in Figure 1, we have the current flows though the cross section A as,

$$I = \int_A dI = \int_{\phi=0}^{\phi_s} WqK{n_0}^{m+\frac{1}{2}} \exp\left[(m+\frac{1}{2})(q\phi/kT)\right] E_x \sqrt{\frac{\varepsilon_{poly}\varepsilon_0}{2kT}} d\phi$$

$$I = WKE_x \sqrt{\frac{\varepsilon_{poly}\varepsilon_0}{2kT}} \cdot \frac{kT}{\left(m+\frac{1}{2}\right)} \cdot {n_0}^{m+\frac{1}{2}} \exp\left[(m+\frac{1}{2})(q\phi_s/kT)\right] \tag{A.4}$$

Step (D)

In order to relate surface voltage to the applied gate voltage, consider an infinitely small surface at the interface between the gate dielectric and the polymer. From Gaussian law, we have

$$\varepsilon_{ox}\varepsilon_0 E_{ox} = \varepsilon_{poly}\varepsilon_0 E_s$$

$$\varepsilon_{ox}\varepsilon_0\left(\frac{V_G-V_x}{x_t}\right) = \varepsilon_{poly}\varepsilon_0 \sqrt{\frac{2kT}{\varepsilon_{poly}\varepsilon_0}} \cdot n_0^{\frac{1}{2}} \exp\left[\frac{1}{2}\cdot(q\phi_s/kT)\right]$$

where $E_s = \sqrt{\frac{2kT}{\varepsilon_{poly}\varepsilon_0}} \cdot \sqrt{n_0 \exp(q\phi_s/kT)}$. Thus

$$C_0(V_G-V_x) = \varepsilon_{poly}\varepsilon_0 \sqrt{\frac{2kT}{\varepsilon_0\varepsilon_{poly}}} \cdot n_0^{\frac{1}{2}} \exp\left[\frac{1}{2}(q\phi_s/kT)\right]$$

where $C_0 = \frac{\varepsilon_0\varepsilon_{ox}}{x_t}$ and x_t is gate dielectric thickness. From the above

equation, we can extract the following term which have been used in equation(A.4).

$${n_0}^{m+\frac{1}{2}} \exp\left[(m+\frac{1}{2})(q\phi_s/kT)\right] = \left[\frac{C_0(V_G-V_x)}{\left(2kT\varepsilon_{poly}\varepsilon_0\right)^{1/2}}\right]^{2\left(m+\frac{1}{2}\right)} = \frac{C_0^{2m+1}(V_G-V_x)^{2m+1}}{\left(2kT\varepsilon_{poly}\varepsilon_0\right)^{m+\frac{1}{2}}}$$

Substituting it into equation (A.4), we have,

$$I = WqKE_x\sqrt{\frac{\varepsilon_{poly}\varepsilon_0}{2kT}}\cdot\frac{kT}{\left(m+\frac{1}{2}\right)q}\cdot\frac{C_0^{\,2m+1}\left(V_G - V_x\right)^{2m+1}}{\left(2kT\varepsilon_{poly}\varepsilon_0\right)^{m+\frac{1}{2}}}$$

$$= WKE_x\cdot\frac{1}{2m+1}\cdot\frac{C_0^{\,2m+1}\left(V_G - V_x\right)^{2m+1}}{\left(2kT\varepsilon_{poly}\varepsilon_0\right)^{m}}$$

Step (E)

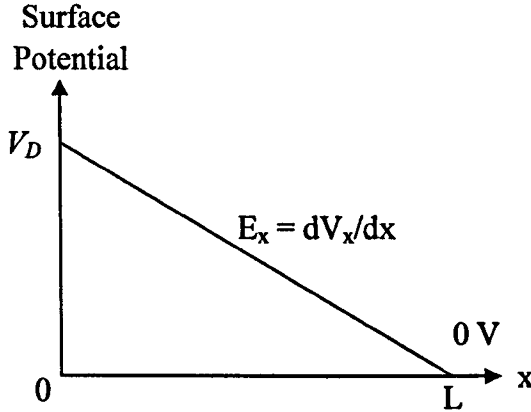


Figure 2 The surface potential along the channel

By making an assumption of gradually decreased potential along the channel (Figure 2), i.e.,

$$E_x = \frac{dV_x}{dx}$$

Therefore the current equation can be rewritten as,

$$I = WK\cdot\frac{1}{2m+1}\cdot\frac{C_0^{\,2m+1}\left(V_G - V_x\right)^{2m+1}}{\left(2kT\varepsilon_{poly}\varepsilon_0\right)^{m}}\frac{dV_x}{dx}$$

Multiply by dx and then integrate over the whole channel length for dx from L to 0 and dVx from V_D to 0.

$$\int_0^L Idx = WK\frac{1}{2m+1}\cdot\frac{C_0^{\,2m+1}}{\left(2kT\varepsilon_{poly}\varepsilon_0\right)^{m}}\int_0^{V_D}\left(V_G - V_x\right)^{2m+1}dV_x$$

$$IL = WK\frac{1}{2m+1}\cdot\frac{C_0^{\,2m+1}}{\left(2\varepsilon_{poly}\varepsilon_0 kT\right)^m}\left[-\frac{\left(V_G - V_x\right)^{2m+2}}{2m+2}\right]_{V_x=0}^{V_D}$$

$$= WK\cdot\frac{1}{2m+1}\cdot\frac{C_0^{\,2m+1}}{\left(2\varepsilon_{poly}\varepsilon_0 kT\right)^m}\cdot\left[\frac{\left(V_G - V_D\right)^{2m+2} - V_G^{\,2m+2}}{2m+2}\right]$$

Divide by L, the drain current of polymer transistor as a function of terminal voltages can be written as:

$$I = \frac{W}{L}\cdot\frac{K}{(2m+1)\cdot(2m+2)}\cdot\frac{C_0^{\,2m+1}}{\left(2\varepsilon_{poly}\varepsilon_0 kT\right)^m}\cdot\left[\left(V_G - V_D\right)^{2m+2} - V_G^{\,2m+2}\right]$$