Scaling potential and MOSFET integration of thermally stable Gd silicate dielectrics

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Abstract

We investigate the potential of gadolinium silicate (GdSiO) as a thermally stable high-k gate dielectric in a gate first integration scheme. There silicon diffuses into gadolinium oxide (Gd_2O_3) from a silicon oxide (SiO_2) interlayer specifically prepared for this purpose. We report on the scaling potential based on detailed material analysis. Gate leakage current densities and EOT values are compatible with an ITRS requirement for low stand by power (LSTP). The applicability of this GdSiO process is demonstrated by fully functional silicon on insulator (SOI) metal oxide semiconductor field effect transistors (MOSFETs).

1. Introduction

A key issue for scaling of low standby power (LSTP) complementary metal oxide semiconductor (CMOS) technology is the realization of transistor gate stacks with high-k insulators and metal electrodes [1]. Rare earth oxides are attractive candidates that offer high k-values in combination with reasonably large band offsets to silicon [2][3]. In a classical gate first process integration scheme, however, a high temperature processing step is required after

gate stack fabrication. Thus a low crystallization temperature of rare earth oxides is undesirable as enhanced leakage paths along grain boundaries are expected.

While amorphous binary rare earth oxides are not stable at high process temperatures, they can be stabilized by introducing silicon into their atomic matrices before [4] or during processing [5][6][7]. Amorphous structure of these silicates is preserved at temperatures up to 1000°C necessary for gate first processing.

Gadolinium silicate (GdSiO), investigated in this work, is attractive with its high dielectric constant of k~16 [4][8] compared to ~10 for La silicate [9]. GdSiO layers are prepared by intermixing of thermally grown silicon oxide (SiO_2) interlayers and evaporated gadolinium oxide (Gd_2O_3). As little is known about thin GdSiO layers, we investigate different thickness ratios and annealing procedures up to 1000°C.

Structural characterization is carried out using transmission electron microscopy (TEM) and medium energy ion scattering (MEIS). Metal oxide semiconductor (MOS) capacitors with TiN electrodes are used to study the electrical properties of the layers. Metal oxide semiconductor field effect transistors (MOSFETs) on silicon on insulator (SOI) substrates are used to demonstrate applicability of GdSiO in a gate first process.

2. Experimental

Surfaces of p-type silicon (100) substrates with resistivity of 12-18 Ωcm have been prepared by RCA clean, HF-dip and subsequent dry thermal oxidation to 4 nm thickness. Thinner oxides down to 1 nm thickness have been achieved by wet chemical etching in

diluted HF. Gd_2O_3 films have been deposited by e-beam evaporation of granular material. A deposition rate of 0.01 nm/s has been chosen and molecular nitrogen has been added during deposition. Post deposition annealing (PDA) for 30 min at 400°C has been applied to some samples. Rapid thermal annealing (RTA) up to 1000°C has been used to form GdSiO from the initial Gd_2O_3 / SiO_2 bi-layer. Different RTA schemes have been used: RTA1 in an inert ambient (N_2 or Ar) and RTA2 with inert gas but open vacuum valve. MOS capacitors with titanium nitride (TiN) electrodes have been formed by reactive sputtering from a Ti target [10] and a lift-off technique. SOI n-MOSFETs with GdSiO and TiN electrodes have been fabricated in a gate first integration scheme with source/drain junction annealing for 20 s at 930°C (process details [11]).

Structural characterization has been carried out using TEM and MEIS. Layers without metal electrodes have been used for the latter methods. TEM examination of electron transparent samples prepared using focused ion beam thinning techniques has been carried out at 200 kV in a JEOL2000FX. MEIS was performed using a 100 keV He^+ beam with two scattering angles 70.5° and 125.3°. MOS capacitors have been characterized by capacitance voltage (C-V) and current voltage measurements with an AGILENT 4294A impedance analyzer and 4156B parameter analyzer, respectively.

3. Results and Discussion

TEM cross sectional images and extracted physical thicknesses of gate stacks before and after RTA1 are shown in Fig. 1 and Tab. 1, respectively. In all three cases a bilayer appears between the TiN electrodes and the silicon substrate, as a dark Gd-based region on top of the SiO_2 interfacial layer with a light contrast. Corresponding C-V characteristics (Fig. 2) show an increase in oxid capacitance due to formation of GdSiO [8]. Low frequency accumulation

capacitances yield an EOT = 3.5 nm and 2.5 nm before and after annealing considering a quantum correction of 0.3 nm. The frequency dispersion in accumulation observed for 100 kHz and higher is attributed to the bilayer of SiO_2 / Gd_2O_3 or GdSiO that is present in all three cases and series resistance effects [12][13]. The frequency dependent bump in depletion indicates a high density of interface states which can be reduced by annealing in a forming gas ambient [14]. Leakage current densities are below 10^{-7} A/cm² (not shown here) for a gate bias of V_{FB}-1.5 V (V_{FB} is the flatband voltage), which is well into accumulation [15].

Assuming an SiO_2 interlayer with k = 3.9 dielectric constants of the Gd-based region has been derived from EOT values. For GdSiO k-values of 16 are found for theses layers in agreement with thicker films [4][8]. K-values of the Gd_2O_3 or GdSiO regions have been calculated from EOT values assuming a SiO_2 interlayer with k = 3.9. A k-value of ~ 16 is found for GdSiO in good agreement with thicker layers [4][8].

To explore the scaling potentials of GdSiO, a Gd_2O_3 thickness of 3 nm has been deposited in a single run on thermal oxides ranging from 1 nm to 3.8 nm. GdSiO formation at 900°C by RTA1 resulted only in a slight modification of EOT (Fig. 3). This is attributed to residual oxygen in the process chamber that can diffuse through the films and reacts at the silicon/SiO_2 interface [4]. In this case the EOT cannot be reduced as interfacial layer re-growth counteracts the consumption due to silicate formation. In contrast, significant improvement in EOT down to 1.3 nm was obtained for RTA2 and in combination with a preceding PDA treatment. RTA2 with open vacuum valve is assumed to reduce interfacial re-growth significantly and consumption of the interfacial layer dominates during silicate formation.

Furthermore, EOT values well below 2 nm can be achieved even with 2.5-3 nm initial SiO_2 thickness. This may be used to tailor the available amount of oxygen when capped stacks are

used in device fabrication and no additional oxygen from the ambient is available to balance oxygen deficiency of evaporated Gd_2O_3 films.

MEIS analysis have been performed to study the element distribution in the gate stacks (Fig. 4). Note that all MOS capacitors were annealed before metal deposition to allow MEIS measurements. Before high temperature annealing the maximum of the silicon signal and that of gadolinium are very well separated. This indicates only minor diffusion during the low temperature PDA, if the effects of the system resolution and energy straggling are accounted for. After an RTA2 treatment, however, the silicon signal is spreaded across the whole stack indicating a full GdSiO formation starting from these thin initial Gd_2O_3 layers. After the annealing treatment the pure Gd_2O_3 appears to be removed completely.

After RTA1 treatments generally an EOT of less than 1.8 nm could not be achieved. The RTA2 treatment however, very low leakage currents below J = 10^{-7} A/cm² are obtained that allow further reduction of EOT. The combination of PDA and RTA2 yields the best scaling trends.

The leakage current vs. EOT scaling trend is shown in Fig. 5. Typically five measurements are shown for each layer resulting in a more or less pronounced spread of leakage currents for a certain EOT value. For RTA1 an EOT of 1.8 nm has been found to be a lower limit that can hardly be reduced. Corresponding leakage currents are in the order of 10^{-4} to 10^{-3} A/cm². Very low leakage currents below J = 10^{-7} A/cm² are obtained for RTA2 which allow a significant reduction of EOT. The combination of PDA and RTA2 yields the best scaling trend. An EOT of 1.3 nm at J = 0.02 A/cm² has been achieved, in line with ITRS LSTP targets for 32nm multi-gate devices [1].

Finally in Fig. 6 the output and transfer characteristics of n-MOSFETs with GdSiO/TiN gate stacks fabricated by a gate first process demonstrate acceptable functional transistor behavior. An EOT of 3.3 nm has been derived… from inversion capacitance (not shown here) and corresponding leakage current density remains below 10^{-5} A/cm².

4. Conclusion

Scaling of thermally stable GdSiO high-k dielectrics has been investigated. The initial SiO_2 thickness may be used to tailor the available amount of oxygen in the gate stack without compromising EOT. The equivalent oxide thickness has been scaled to EOT = 1.3 nm by carefully choosing the annealing procedure. Furthermore GdSiO has been successfully introduced into fully functional SOI n-MOSFETs with TiN metal gate electrodes.

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List of tables and figures

Tab. 1:

	SiO_2/high-k[nm]	**$k_{Gd\text{-}based}$**
w/o annealing	1.6-1.8 / 5.8	13.3-15.1
900°C	1.2 / 5.2	15.6
1000°C	1.4-1.5 / 4.8-5.1	16.6-17.0

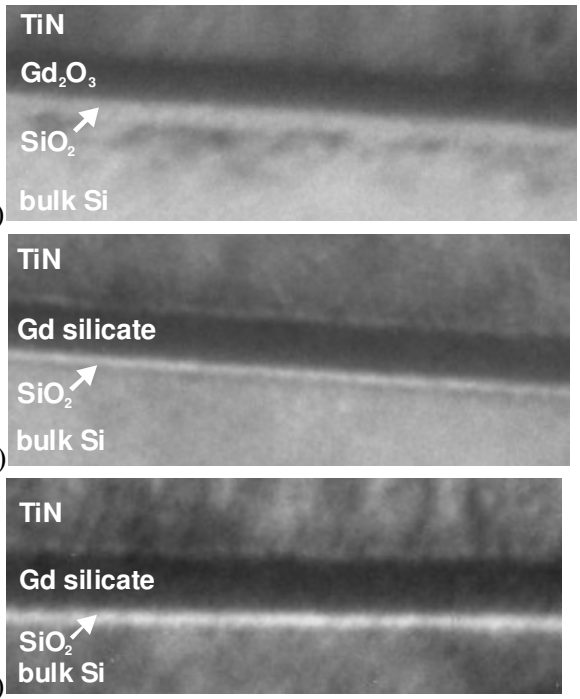
a)
TiN
Gd2O3
SiO2
bulk Si
b)
TiN
Gd silicate
SiO2
bulk Si
c)
TiN
Gd silicate
SiO2
bulk Si

Fig. 1:

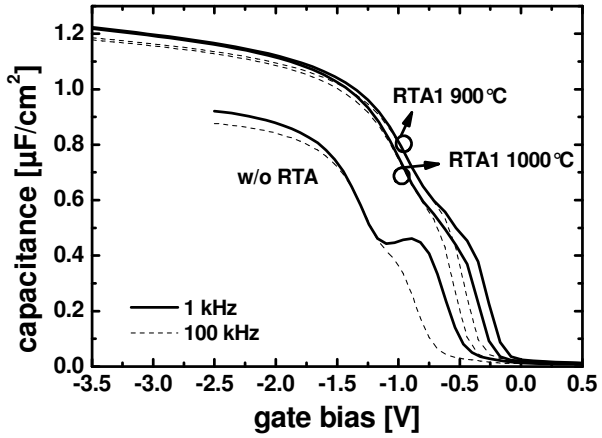
capacitance [μF/cm²]
gate bias [V]
RTA1 900℃
RTA1 1000℃
w/o RTA
1 kHz
100 kHz
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-3.5
-3.0
-2.5
-2.0
-1.5
-1.0
-0.5
0.0
0.5

Fig. 2:

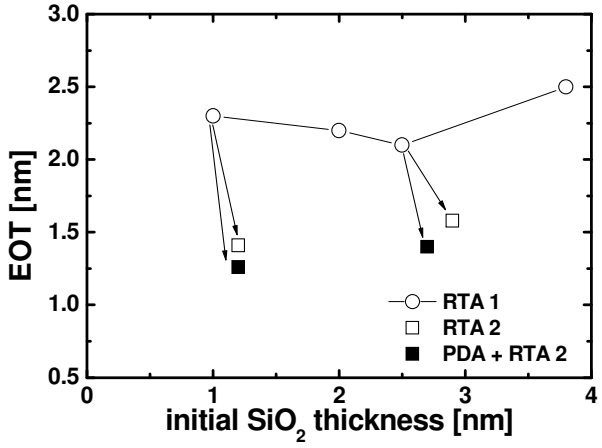
3.0
2.5
2.0
1.5
1.0
0.5
EOT [nm]
0
1
2
3
4
initial SiO2 thickness [nm]
RTA 1
RTA 2
PDA + RTA 2

Fig. 3:

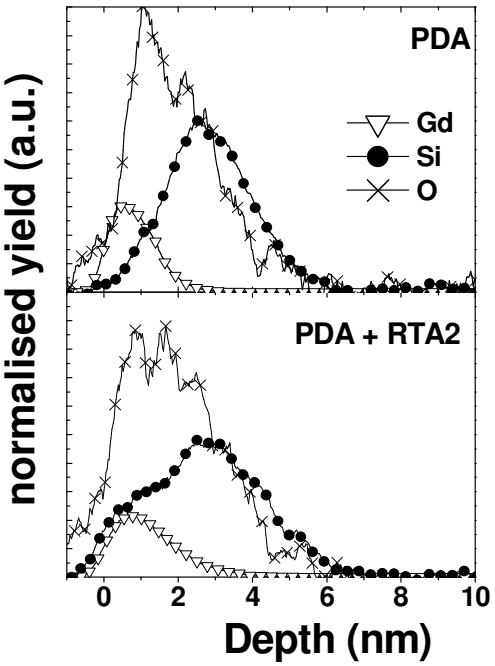

Fig. 4:

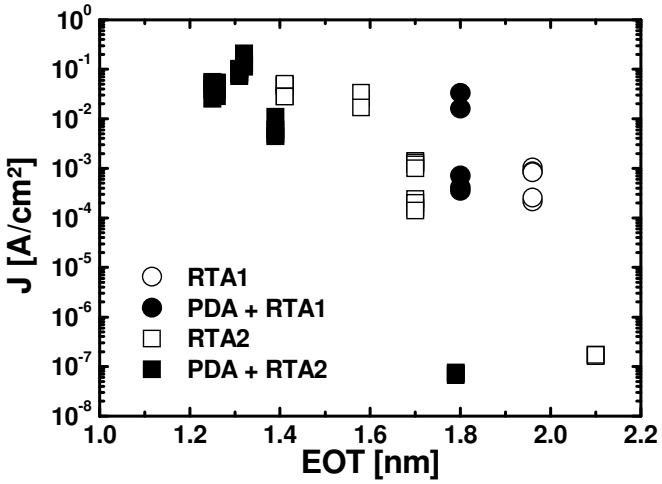

Fig. 5:

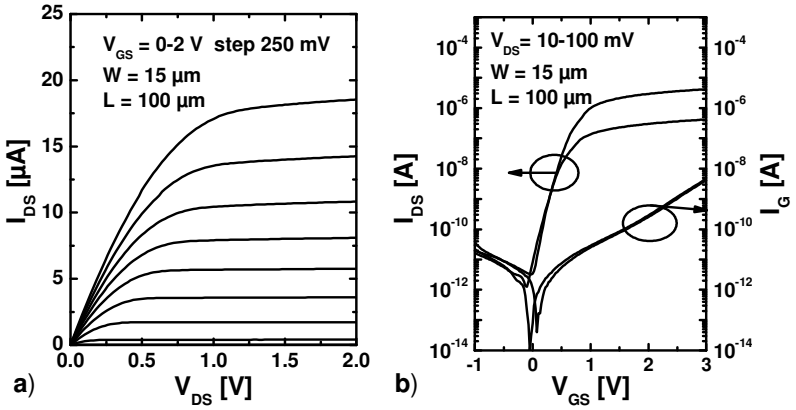
V_GS = 0-2 V step 250 mV
W = 15 µm
L = 100 µm
I_DS [µA]
V_DS [V]
a)
V_DS= 10-100 mV
W = 15 µm
L = 100 µm
I_DS [A]
I_G [A]
V_GS [V]
b)

Fig. 6: