An overview of CMOS activities for the ATLAS upgrade

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Introduction

Why HV-CMOS, HV-MAPS, HV/HR-MAPS, DMAPS... in the ATLAS upgrade?
- Motivated for the need of low-cost large area detectors
- With less material (avoid bump bonding)

With the requirements of
- Being able to cope with the radiation level ($> 10^{15} \text{n}_{eq}/\text{cm}^2$)
- and the high rate ($\sim \text{MHz/mm}^2$)

What can HV-CMOS detectors offer?
- Produced in commercially available technologies $\rightarrow$ reliable, mature, low-cost
- HV $\rightarrow$ fast charge collection by drift and high radiation tolerance
- HR $\rightarrow$ to widen the depletion region of the sensor and improve signal, now available in most foundries
- R/O electronics embedded inside the sensor area
- Possibility of monolithic sensors with standalone R/O
**ams 0.35 μm/180 nm**

**Key features:**
- **Technology node** 0.35 μm/180 nm
- **Wells** No possibility of isolating n-wells from the collecting deep n-well. No CMOS electronics in the sensor area. Can induce cross-talk.
- **Metal layers** 4/6
- **HR** 20 (standard value) – 1k Ω·cm (since 2015/6)
- **HV** -150 V < HV < 0 V
- **Depletion region** 140 μm thick
- **Backside biasing** Not possible
- **Stitching** Not possible

**Prototypes:**
- **ams 0.35 μm** → Initial R&D developments, H35CCPDv1-2, H35DEMO, HVStrip, CHESS1-2 (strips)
- **ams 180 nm** → CCPDv1-8, CLICpix=CCPDv3, C3PD, MuPix1-8 (Mu3e), MuPix8/ATLASPix

*I. Peric, NIMA 650 pp. 158-162, 2011*
ams 0.35 µm – H35DEMO

Summary:
- Submitted in October 2015 (eng. run)
- It includes:
  - 2 matrices of pixels with R/O coupled to FEI4. Pixels without comparators.
  - 2 monolithic matrices of pixels with standalone R/O. Pixels with nMOS/CMOS comparators. Digital blocks (FE-I3 style) are in the periphery of the matrices.
  - Different pixel flavours
  - Test structures for TCT/e-TCT and sensor capacitance measurement
- Pixel size: 50 µm x 250 µm for 1-to-1 connection to FEI4
- Timing resolution: 25 ns
- Readout speed: 320 MHz
- Rad-hard design
- Resistivity: 20 Ω·cm, 80 Ω·cm, 200 Ω·cm, 1k Ω·cm
- Detection efficiency > 99% in test beams

Neutron irradiation at Ljubljana + e-TCT

- 80 Ω·cm
  - Max. at $10^{15}$ n$_{eq}$/cm$^2$
  - At max. fluence > 50 µm

- 200 Ω·cm
  - Max. at $10^{15}$ n$_{eq}$/cm$^2$
  - At max. fluence > 50 µm

1k Ω·cm chip thinned to 100 µm with backside contacts

Backside biasing
Fully depleted @ -40 V!!
Sensor surface

E. Vilella, JINST 11 C01012, 2016

E. Cavallaro, JINST 11 C01012 2016

E. Vilella, PIXEL Workshop, 2016
ams 0.35 µm – CHESS strip development

**CHESS1 is a test chip:**
- Submitted in August 2014
- It includes:
  - Test transistors
  - Passive pixels of different length (45 µm x 100-800 µm)
  - Standalone amplifiers
  - Active pixels with embedded amplifiers
  - Passive arrays for charge collection studies
- Resistivity: 20 Ω·cm (standard value)

**CHESS2 is full reticle demonstrator:**
- Submitted in 2016
- Design by SLAC and UCSC, support from KIT
- It includes:
  - Array of 128 by 32 stripletswith full digital encoding and readout
  - Array of 16 by 32 pixels with multiplexing
  - Test structure for LVDS/CMOS and CMOS/LVDS transmission + pixels arrays for e-TCT and capacitance measurements
- Cell size and timing resolution: 40 µm x 630 µm, 25 ns
- Readout speed: 320 MHz
- Rad-hard design
- Resistivity: 20 Ω·cm, 50-100 Ω·cm, 200-300 Ω·cm, 600-2k Ω·cm
ams 180 nm – Prototypes

- **CCPDv1 (2011)**  
  Basic design. **Pixel size** 33 µm x 125 µm, readout with FEI4 pixel readout ASIC.

- **CCPDv2 (2012)**  
  Improved radiation tolerance (850 Mrad), linear transistors replaced with enclosed ones.

- **CCPDv3 (2013)**  
  Large matrix with 25 µm x 25 µm implemented, readout with CLICpix pixel readout ASIC.

- **CCPDv4 (2014)**  
  Pixel position encoded as pulse length.

- **CCPDv5 (2015)**  
  Comparator with time walk compensation.

- **CCPDv6**  
  Chip version in AMS aH18 process, a new version of H18 process that offers more flexibility such as the use of HR substrates.

- **CCPDv7**  
  Chip version with a new guard ring geometry that allows higher bias voltage of up to -150 V.

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**Pixel encoding (connection to FEI4)**  
A. Miucci, JINST 9 C05064, 2014

**Neutron irradiation + e-TCT**  
A. Affolder, JINST 11 P04007, 2016

**Efficiency in test beam**  
- **99.7%**  
  96.2%  
  84% hits with < 25 ns resolution  
  M. Benoit, arXiv:1611.02669v1, 2016
ams 180 nm – MuPix8/ATLASPix and new design

MuPix8/ATLASPix:
- Submitted in January 2017 (eng. run)
- It includes:
  - Matrices of pixels for ATLAS
    - Pixel size: 25 µm x 25 µm, 25 µm x 50 µm, 33 µm x 125 µm, 50 µm x 60 µm, 40 µm x 125 µm
  - MuPix8
    - Pixel size: 80 µm x 81 µm
    - Matrix with 200 x 128 pixels
    - Pixels with CSA and output driver only
    - Hit info: x-address, y-address, 10-bit TS, 6-bit amplitude
    - Time resolution: 6.25 ns
    - Nominal power consumption: 300 mW per matrix
    - Hit driven, triggerless R/O (MuPix8, Simple ATLASPix)
    - Triggered R/O (M ATLASPix)
    - Resistivity: 20 Ω·cm, 50-100 Ω·cm, 100-400 Ω·cm, 600-1.1k Ω·cm

New design:
- Studies considering the integration of RD53-like periphery logic
LFoundry 150 nm

**Key features:**

- **Technology node** 150 nm
- **Wells** Deep p-well (PSUB) to isolate n-wells from deep n-well (collecting electrode). Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **HR** $10 \, \Omega \cdot \text{cm} - \sim 4k \, \Omega \cdot \text{cm}$
- **HV** $-120 \, \text{V} < \text{HV} < 0 \, \text{V}$
- **Depletion region** $\sim 170 \, \mu\text{m}$ thick @ -110 V
- **Backside biasing** Possible
- **Stitching** Possible

**Prototypes:**

- CCPD_LF (VA/VB), LF-CPIX Demo. (VA/VB), MonoPix Demo., COOL, LF_ATLASPix, LFHVMAPS_FEI3

*P. Rymaszewski, JINST 11 C02045, 2016*
LFoundry 150 nm – Prototypes

**LF_CPIX Demonstrator (VA)**
- Submitted in August 2014
- Design by Bonn, CPPM, KIT
- 33 μm x 125 μm pixels
- R/O coupled to FE-I4
- Sub-pixel encoding, res: 2k Ω·cm

**LF_CPIX Demonstrator (VB)**
- Submitted in April 2016
- Design by Bonn, CPPM, IRFU
- 50 μm x 250 μm pixels
- R/O coupled to FE-I4
- No sub-pixel encoding

**MonoPix Demonstrator**
- Submitted in August 2016
- Design by Bonn, CPPM, IRFU
- 50 μm x 250 μm pixels
- Standalone R/O
- Resistivity: 2k Ω·cm

**COOL chip**
- Designed by SLAC, submitted in August 2016
- 50 μm x 250 μm pixels
LFoundry 150 nm – Results from CCPD_LF

Summary:
- 2k Ω·cm
- Thinned to 100 µm - 300 µm
- Backside contact for HV
- 33 µm x 125 µm pixels, 3 x 2 pixels = 2 FE-I4 cells
- Sensor R/O includes: pulse input, CSA, comparator with 4-bit trim DAC and output stage for voltage amplitude encoding
- Sensor chip attached to R/O chip

TID irradiation with X-ray

Chips functional after irradiation, but with 20-30% less gain

Neutron irradiation at Ljubljana + e-TCT

High threshold (2600 e⁻) → 79% hits in-time
Low threshold (190 e⁻) → 91% hits in-time

Eva Vilella – CLIC Workshop – 9th March 2017
**LFoundry 150 nm – Fully monolithic designs FEI3-style**

**MonoPix Demonstrator**

- It is possible to embed all these electronics inside the sensor area (PSUB)

**LFHVMAPS_FEI3**

- Fully monolithic sensors with standalone R/O


R. Casanova, submitted to JINST
TowerJazz 180 nm

Key features:
- **Technology node** 180 nm
- **Wells** Deep p-well to isolate n-wells from p-epi layer. Full CMOS electronics are possible in the sensor area.
- **Metal layers** 6
- **Gate oxide** 3 nm (good for radiation tolerance)
- **HR** 1k – 8k Ω·cm
- **HV** -6 V < HV < 0 V
- **Epi-layer** 18 – 40 µm thick
- **Backside biasing** Possible
- Small n-well diode $\rightarrow$ low sensor capacitance ($\sim$5 fF) $\rightarrow$ higher gain, better SNR, faster signal and potentially lower power consumption

CERN-TJ modified process:
- Normally, small electrodes produce weak fields under deep p-wells and signal collection after irradiation becomes difficult on edges (efficiency drop towards pixel edges)
- CERN-TJ $\rightarrow$ Add planar n-type layer to significantly improve lateral depletion and charge collection after irradiation. Implemented in Investigator test chip.

Prototypes:
- ALPIDE (ALICE upgrade chip), MISTRAL, ASTRAL, CHERWELL, Explorer, Investigator, MALTA, MonoPix
TowerJazz 180 nm – Results from Investigator

- **Investigator chip** has pixels with → 50 µm pitch, 3 µm size collection electrode and 20 µm spacing
  25 µm p-epi layer
- Investigator irradiated in IJS Ljubljana (TRIGA) in several steps up to $1.0 \cdot 10^{15}$ neq/cm$^2$ (NIEL $1.0 \cdot 10^{15}$ neq/cm$^2$, 1 Mrad TID)
- Measurements up to $10^{16}$ neq/cm$^2$ are ongoing
- Little change to signal after irradiation
- First test beam measurements indicate no efficiency loss on pixel boundaries after $1.0 \cdot 10^{15}$ neq/cm$^2$ (standard process not working after this fluence)

MPV = 19 mV pre-rad
16 mV after $1.0 \cdot 10^{15}$ neq/cm$^2$

$\sigma = 1.96$ ns pre-rad
2.78 ns after $1.0 \cdot 10^{15}$ neq/cm$^2$
TowerJazz 180 nm – New prototypes

New developments towards a dedicated CMOS chip that matches ATLAS specifications:
- Analog front-end with CSA + discriminator optimized for 25 ns in-time efficiency and low threshold operation
- 2 cm x 2 cm chip size with < 50 µm x 50 µm pixels
- Monolithic design includes readout architecture which copes with ATLAS outer layer hit rate requirement

<table>
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<tr>
<th></th>
<th>TJ MALTA chip</th>
<th>TJ MonoPix chip</th>
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<tbody>
<tr>
<td>Pixels</td>
<td>512 x 512</td>
<td>512 x 526</td>
</tr>
<tr>
<td>Active area</td>
<td>18 mm x 18 mm</td>
<td>18 mm x 10 mm</td>
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<tr>
<td>Features</td>
<td>Hit memory in active matrix</td>
<td>Hit memory in active matrix (2 FF per pixel)</td>
</tr>
<tr>
<td></td>
<td>All hits are asynchronously transmitted</td>
<td>Synchronous column drain architecture</td>
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<tr>
<td></td>
<td>over high speed bus to EoC logic</td>
<td>Hit address asserted to bus with 40 MHz</td>
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<tr>
<td></td>
<td>No clock distribution over active matrix</td>
<td>6-bit ToT encoding at end of column</td>
</tr>
<tr>
<td></td>
<td>to minimize power and digital-analog crosstalk</td>
<td></td>
</tr>
<tr>
<td>Design</td>
<td>CERN</td>
<td>Bonn</td>
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</table>
Other technologies

**XFAB:**
- **Technology node**: 180 nm (SOI)
- **Wells**: Deep pw, full CMOS
- **Metal layers**: 7
- **HR**: 100 Ω·cm
- **HV**: > -200 V
- **Backside biasing**: Not possible
- **Design/Testing**: Bonn, CERN, CPPM

**ESPROS:**
- **Technology node**: 150 nm
- **Wells**: Deep pw, full CMOS
- **Metal layers**: 6
- **HR (n-type bulk)**: 2k Ω·cm
- **HV**: > -20 V
- **Depletion region**: ~50 µm
- **Backside biasing**: 50 µm + p-implant
- **Design**: Bonn, Prague

**Global Foundries:**
- **Technology node**: 130 nm
- **Metal layers**: 8
- **HR**: 10 Ω·cm – 3k Ω·cm
- **HV**: > -30 V

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**Test transistors**
- 25 x 25 µm²
- 50 x 50 µm²
- 100 x 100 µm²

**XBT01**
- 700 Mrad
- $5 \times 10^{14} \text{n}_{eq}/\text{cm}^2$
- N. Wermes, 2016

**XBT02**
- 40 µm x 40 µm pixels
- 50 Mrad
- $5 \times 10^{14} \text{n}_{eq}/\text{cm}^2$

**EPCB01**
- Techno. exploration
- 40 µm x 40 µm pixels
- M. Havranek, JINST 10 P02013, 2015

**EPCB02**
- Improvement of first version
- 700 Mrad
- $5 \times 10^{14} \text{n}_{eq}/\text{cm}^2$

**HV2FEI4-GF**
- 33 µm x 125 µm pixels
- 26 cols x 14 rows
- Irradiated to 600 Mrad
- Glued to FEI4

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**N. Wermes**
Summary

• At present time, lots of R&D dedicated to the development of HV/HR-CMOS/MAPS detectors:
  • In different commercially available HV-CMOS technologies
    • ams 0.35 μm, ams 180 nm, LFoundry 150 nm, TowerJazz 180 nm, XFAB 180 nm, ESPROS 150 nm, Global Foundries 130 nm...
  • A large number of prototypes and a few demonstrators have been produced
  • Encouraging results
  • Good radiation tolerance

• Option to readout HV-CMOS sensors with existing R/O ASICs:
  • FEI4
  • CLICpix

• Recent alternative of monolithic HV-MAPS with standalone R/O:
  • With digital circuits in the periphery or in the sensor area depending on the technology

• Steps towards the integration of periphery circuits in prototypes