Design of Low Power Electronic Circuits for Bio-Medical Applications

Thesis submitted in accordance with the requirements of the University of Liverpool for the degree of Doctor in Philosophy

by

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The operational transconductance amplifier, OTA is one of the basic building blocks in many analogue circuit applications. The low power consumption is an essential parameter in modern electronic designs for many areas particularly for portable devices and biomedical applications. For biomedical applications, the low-power low-voltage OTA-C filters operating at low-frequency ranges are desired. The low-power, low-voltage operation of electronic devices is very important for applications such as hearing aids, pacemakers, and EEG. The importance of such operation is due to the need to implant these electronic circuits inside the body of the patient for long times before re-charging or replacing the batteries as for pacemakers and future hearing aids. The small size lightweight wearable EEG systems are preferable for applications ranging from epilepsy diagnosis to brain-computer interfaces. The low power consumption is achieved by operation at very small levels of current. So, in such applications the operation in the nano-ampere current range is essential to ensure power consumption of nW or few µW. Such very small currents are obtained through the operation of MOS transistors in their sub-threshold regime. The design space in such applications is restricted by their specifications which in turn based on the nature of the application.

In this work, the design and implementation of OTA-C filter topologies for two bio-medical applications are made and discussed. Those applications are represented by hearing aids and EEG applications.

In hearing aids, the work focused on cochlear implant and specifically on its most important stage represented by the filter. Four OTA-C filter topologies are proposed and two of them are tested experimentally. For the filter in a hearing aid system, besides its low power operation, it is required to operate with a relatively high dynamic range of 60dB and above. The dynamic range is the operation space of the
filter that specified by the range of signals which can process properly. It is bounded by the maximum power signal less than its distortion overhead level to the minimum power signal more than its noise floor. The maximum signal level the filter can perform properly represents its input linear range. The challenge in CMOS OTA sub-threshold operation is the very small input linear range which makes it extremely difficult to build low-power consumed OTA-C filters with a wide dynamic range, $DR$. In this work, an OTA with an input linear range of $\pm 900\text{mV}$ for total harmonic distortion, $THD<5\%$ is proposed using MOSFET bumping and capacitor attenuation techniques, combined for the first time. The minimum signal level the filter can distinguish from noise is still relatively small with the use of appropriate OTA architecture and using the $g_m/I_D$ methodology for MOSFET sizing. So, programmable CMOS OTA-C band-pass filter topologies operating in sub-threshold region with a dynamic range of $65\text{dB}$ for use in bionic ears were proposed. The power consumption for the proposed filters is in nano-Watt range for their frequency range of $(100-10k)$ Hz. Also, a 4-channel OTA-C filter bank is designed and tested.

The EEG signals have small amplitudes and frequency bands ranges of $\mu$V’s and $(1-40)$ Hz respectively. The important issue is to design filters with small noise floor with white dominant. This is achieved with the proposed OTA which is of relatively simple architecture and with operation in the deep weak-inversion region using $\pm 1.5\text{V}$ supply rails. The OTA-C filter has power consumption in the pico-Watt range for $\delta$, $\theta$, and $\alpha$ signals and less than $3nW$ for $\beta$ signals. Another topology is suggested for future work.
Dedicated to my parents, aunt & sisters
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LIST OF ABBREVIATIONS

ABI  Auditory Brainstem Implants
AGC  Automatic Gain Control
ADC  Analogue to digital converter
AER  Address-Event Representation
AMS  Austria micro systems
B    Bulk of MOSFET
BAHA Bone Anchored Hearing Aids
BCI  Brain-Computer Interface
BTE  Behind-the-Ear
CIC  Completely-in-the-Canal
CIs  Cochlear Implants
CLBTs Compatible Lateral Bipolar Transistors
C-level Comfortable level
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>D</td>
<td>Drain of MOSFET</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processing</td>
</tr>
<tr>
<td>EEG</td>
<td>Electroencephalography</td>
</tr>
<tr>
<td>EKV</td>
<td>MOSFET model made by C. Enz, F. Krummenacher and E. Vitloz.</td>
</tr>
<tr>
<td>FD SOI</td>
<td>Fully depleted silicon on insulator wafer technology</td>
</tr>
<tr>
<td>$FOM$</td>
<td>Figure of merit</td>
</tr>
<tr>
<td>G</td>
<td>Gate of MOSFET</td>
</tr>
<tr>
<td>HA</td>
<td>Hearing Aid</td>
</tr>
<tr>
<td>ITC</td>
<td>In-the-Canal</td>
</tr>
<tr>
<td>ITE</td>
<td>In-the-Ear</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff’s current law</td>
</tr>
<tr>
<td>$M$</td>
<td>Number of cascaded stages</td>
</tr>
<tr>
<td>MEI</td>
<td>Middle Ear Implants</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
</tbody>
</table>
**LIST OF ABBREVIATIONS**

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTA-C</td>
<td>Operational Transconductance Amplifier - Capacitor</td>
</tr>
<tr>
<td>PFM</td>
<td>Pulse-Frequency Modulated</td>
</tr>
<tr>
<td>S</td>
<td>Source of MOSFET</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
</tr>
<tr>
<td>SPAHA</td>
<td>Subcutaneous Piezoelectric Attached Hearing Actuator</td>
</tr>
<tr>
<td>T-level</td>
<td>Threshold level of</td>
</tr>
<tr>
<td>UV</td>
<td>Ultra violet</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very Large Scale Integration</td>
</tr>
<tr>
<td>$a(s)$</td>
<td>Feed forward stage in a system</td>
</tr>
<tr>
<td>$e(s)$</td>
<td>Error signal in a system</td>
</tr>
<tr>
<td>$f(s)$</td>
<td>Feedback stage in a system</td>
</tr>
<tr>
<td>$H(s)$</td>
<td>Transfer function of the OTA-C filter</td>
</tr>
</tbody>
</table>
**LIST OF SYMBOLS**

- $a$  
  Capacitive attenuation ratio

- $a^{-1}$  
  Number of times of increase of the input linear range due to capacitive attenuation technique

- $A_v$  
  Open loop voltage gain

- $C_{dep}$  
  Depletion region capacitance

- $C_{gb}$  
  Gate-bulk capacitance

- $C_{gd}$  
  Gate-drain capacitance

- $C_{gs}$  
  Gate-source capacitance

- Cls  
  Cochlear Implants

- $C_L$  
  Total capacitance at the OTA output node “load capacitance”

- $C_{OX}$  
  Gate-oxide capacitance

- $DR$  
  Dynamic range

- $E$  
  Electric field

- $f_0$  
  Centre frequency

- $f_c$  
  Flicker noise corner frequency

- $f_H$  
  High frequency

- $f_l$  
  Low frequency

- $f_T$  
  OTA transition frequency

- $G_m$  
  OTA transconductance

- $g_m$  
  MOSFET transconductance
\( g_{mb} \) MOSFET bulk transconductance

\( g_s \) Summation of MOSFET’s transconductance and bulk transconductance

\( g_{sd} \) MOSFET source-drain conductance

\( I_B \) OTA bias current

\( IC \) Inversion coefficient

\( I_D \) MOSFET drain current

\( I_G \) MOSFET gate current

\( I_N \) Normalised current

\( I_{out} \) MOSFET output current

\( k \) Boltzmann constant

\( K \) Process and transistor dependent parameter

\( K_F \) Flicker noise coefficient

\( K_{Fn} \) Flicker noise coefficient in n-channel MOSFET

\( K_{Fp} \) Flicker noise coefficient in p-channel MOSFET

\( K_p \) Polynomial pole coefficient in filter transfer function

\( K_z \) Polynomial zero coefficient in filter transfer function

\( L \) MOSFET effective length

\( L' \) MOSFET effective length with channel length modulation

\( M \) Number of cascaded stages

\( m \) Ratio of the single diffusor aspect ratio to that of the input MOSFET
ABSTRACT

$M_B$  Bumping MOSFET

$M_{SD}$  Source degradation MOSFET

$n$  MOSFET body effect coefficient “slope factor”

$N$  Number of shot-noise sources

$n^+$  High impurity n-type silicon

$n_e$  Effective body effect coefficient

$p$  Pole in filter transfer function

$Q$  Quality factor

$q$  Electron charge

$Q_I$  Charge density of inversion layer in the weak inversion region

$Q_B$  Depletion region charge density

$Q_{FG}$  Floating gate residual charge

$Q_I$  Charge density of inversion layer in the strong inversion region

$R$  Resistor

$r$  Capacitor ratio in a capacitive attenuator

$r_o$  MOSFET output resistor due to channel length modulation effect

$S$  Sub-threshold swing

$S_t$  Ratio of bump MOSFETs aspect ratio to that of input MOSFETs

$T$  Absolute temperature

$THD$  Total harmonic distortion

$u$  Velocity
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$U_T$</td>
<td>Thermal voltage</td>
</tr>
<tr>
<td>$V_B$</td>
<td>OTA bias voltage</td>
</tr>
<tr>
<td>$V_D$</td>
<td>Drain voltage</td>
</tr>
<tr>
<td>$V_d$</td>
<td>OTA differential input voltage</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>Gate-drain voltage</td>
</tr>
<tr>
<td>$V_G$</td>
<td>Gate voltage</td>
</tr>
<tr>
<td>$V_{GB}$</td>
<td>Gate-bulk voltage</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate-source voltage</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>Input voltage</td>
</tr>
<tr>
<td>$V_{in1}$</td>
<td>OTA non-inverting input terminal</td>
</tr>
<tr>
<td>$V_{in2}$</td>
<td>OTA inverting input terminal</td>
</tr>
<tr>
<td>$V_L$</td>
<td>OTA Input linear range</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>Output voltage</td>
</tr>
<tr>
<td>$V_{PP}$</td>
<td>Peak to peak voltage</td>
</tr>
<tr>
<td>$V_{rms}$</td>
<td>Volt root- mean-square- value</td>
</tr>
<tr>
<td>$V_S$</td>
<td>Source voltage</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>Threshold voltage</td>
</tr>
<tr>
<td>$W$</td>
<td>MOSFET effective width</td>
</tr>
<tr>
<td>$\Delta f$</td>
<td>Frequency bandwidth</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>Sub-threshold electrostatic coupling coefficient of the MOSFET gate and channel</td>
</tr>
</tbody>
</table>
Effective sub-threshold electrostatic coupling coefficient between the MOSFET gate and channel

Thermal noise current

Shot noise current

MOSFET RMS value of noise voltage

OTA RMS value of noise voltage

Flicker noise power

Thermal noise power

OTA input-referred noise power

RMS value of output noise power

RMS value of total input-referred noise power for a system consisting of many stages

MOSFET total noise power

Factor affected by the MOSFET operation regime which equals to $\frac{1}{2}$ and $\frac{2}{3}$ for sub-threshold and above threshold respectively

Channel length modulation parameter

Average mobility of electrons

Low-field mobility

Average mobility of holes

Surface potential
CHAPTER ONE

Introduction and Review

1.1 Introduction

Analogue integrated OTA-C filters are the most important building stages in wearable and implantable medical devices such as cochlear implants, CI and Electroencephalography, EEG systems. Such devices are used for many purposes such as diagnosing medical problems, restoring lost body functions, and brain–computer interface (BCI) systems [1.1]. Due to the nature of physiological signals and the corresponding application scenarios, the filters designed for such low frequency applications should meet stringent specifications. The most important specifications are represented by efficient power consumption, low voltage operation, low input-referred noise, high performance and flexibility.

The objective of designing circuits with low power consumption in the range of micro watts is to increase the battery life-time. This means that the systems can operate for a long time in terms of years instead of days or weeks before the need to recharge or replace their batteries. The low voltage operation allows the use of small size batteries which is reflected in a decrease of the entire size of the system. Also, many other specifications like price should be taken in account, hence, the choice of whether to use analogue or digital configurations for the filter and the other stages of such systems. Furthermore the choice of DSP strategies for the entire system depends on the trade-offs in satisfying the required specifications. Therefore, adopting hybrid mixed-signal implementation should give the best compromise for these applications. Therefore, a
system consisting of analogue and digital parts is feasible since in CMOS technology this can be accomplished on the same chip.

A filter has a dynamic range of operation limited by two constraints. The first one is the upper limit above which the output is distorted. This limit is represented by the filter input linear range. The lower limit is the input-referred noise floor. In this work, both limits of the dynamic range of the proposed filters are discussed in detail. Besides, the upper limit is increased, especially for the filters which are proposed for hearing aids application. This work provides the trade-offs in satisfying the specifications for cochlear implants and EEG applications.

1.2 Thesis Contribution

In this work, an OTA with a large input linear range of ±900 mV is presented. This is accomplished by combining MOSFET bumping and capacitor attenuation techniques together, for the first time. In this approach, the proposed OTA has a simple structure and relatively low noise. The proposed OTA is used to construct four, 2\textsuperscript{nd} order OTA-C band-pass filter topologies suitable for hearing aids applications. Two of those filters are tested experimentally. A parallel 4-channel OTA-C filter bank for hearing aids applications is also proposed and experimentally tested. Finally, a 4\textsuperscript{th} order OTA-C band-pass filter suitable for EEG applications is proposed, built, and tested experimentally.

1.3 Project Aim

The target of this research is to develop low power electronic circuits that can be used as a frequency extraction stage in modern biomedical applications such as hearing aids and EEG systems. Hearing aids are used to overcome hearing deficiencies that
arise from simple problems related to outer or middle ear to severe problems due to
damage in the inner ear.

Electroencephalography is a tool to record signals that represent the brain
electrical activity which are measured by electrodes placed on the scalp. The EEG
signals lie within four different frequency bands namely δ, 0, α, and β, characterised by
their low voltage amplitudes and frequency. Those signals reflect different human
activities and are very important in clinical tests for diagnosis ranging from epileptic fits
to brain death and other brain disorders. Recently EEG signals are also used in
computer-brain interface systems, CBI which represents a direct communication
pathway between the brain and an external device [1.2]. This application is aimed to
augment, assist or repair human cognitive or sensory-motor functions. An example of
this is the enabling of signals from the brain to control some external activity to help a
person suffering from paralysis to write a book, control a prosthetic limb or a motorised
wheelchair. The CMOS OTA-C filters operate with very small power that on the one
hand enables utilizing batteries as long as possible. Moreover, this opens up the scope to
innovate very small size electronic circuits to be completely implanted inside the patient
body for longer times than those currently available. The designs are inspired by the
operation of the biological human auditory system. Also, earlier hearing technologies
and auditory models are studied to identify their properties to allow comparison with the
results obtained in this work. EEG signals are also studied. The acquired knowledge in
such biological systems is exploited in proposing an OTA-C filter suitable for EEG
applications.

1.4 Organisation of Thesis

The thesis is divided into seven chapters. The 1st chapter gives a brief introduction
about the filters used in biomedical applications. This is followed by a summary of the
human auditory system, hearing deficiencies, hearing aid technologies, and a review of
previous work in this context represented by proposed cochlea implant technology and OTA-C filters. The 2nd chapter presents MOSFET regions of operation with a focus on the sub-threshold regime. The range of operation of the OTA-C is determined by its dynamic range. Because of the great importance on this factor on the filter performance, its constraints are discussed in details. These constraints are represented by its upper and lower limits. The upper limit is the input linear range of the filter i.e. the maximum allowable input before distortion while the lower limit represents its input-referred noise floor. Discussing these two limits is done by allocating the 3rd and 4th chapters for this purpose. The 3rd chapter describes some of most commonly techniques used to increase the input linear range “increasing the upper limit of the dynamic range”. The proposed OTA is introduced in the same chapter and compared with some other designs. This OTA is utilised to construct the OTA-C filters suited for cochlear implants. Since the lower limit of the filter dynamic range is the input-referred noise floor therefore the 4th chapter explains in detail the noise in integrated circuits, their types and representations. The 5th chapter presents the proposed OTA-C filter topologies and the 4-channel filter bank suitable for cochlear implants. Also, the derivations of filters transfer functions are detailed and their frequency response and noise curves obtained experimentally are compared with other published work. The 6th chapter describes the realisation of the proposed OTA and OTA-C filter for EEG applications and a comparison is made with prior work made by other researchers. Conclusions are drawn in the 7th chapter, together with suggestions for further work.

1.5 Hearing Aids and OTA-C Filters for their Applications

The main parts of the human ear and their anatomy are now briefly presented and their functions described. Hearing deficiencies are then explained and the hearing loss categories are classified according to the physiological impairments. The hearing aids used according to hearing losses are summarised. The human auditory system has unique features, so the necessary specifications for the electronic circuits used for
hearing aids applications are mentioned. In the introduction the use of CMOS OTA-C filters in analogue hearing aids is later presented with a critical review of proposed approaches in the field of cochlea implant design. A number of CMOS OTA-C filter designs of are reviewed.

1.6 The Human Ear

A brief description of the anatomy of the outer, middle and inner ear [1.3] is now presented. The human ear is a system that operates like a transducer, translating the acoustic energy into electrical nerve energy, which then passes to the brain. Figure 1.1 shows the human ear with its three parts, namely; the outer, middle, and inner ear.

![Figure 1.1 Human Ear taken from [1.3]](image)

The outer ear consists of the pinna, the concha, and the ear canal. It provides for the efficient transmission of the acoustic wave from the environment to the eardrum. Also, as a result of its depth and shape, it protects both eardrum and the middle ear from
the external environment and direct injury. It performs some other actions represented by increasing the pressure of the acoustic wave for some frequencies causing resonance in its cavity. Finally, the outer ear can be thought of as a sound directional amplifier aiding an individual in recognizing and localizing sounds.

The middle ear is a cavity within the skull bone, filled with air. It is represented by the eardrum in addition to the chain of three small bones: malleus, incus, and stirrup, known as the ossicular chain. It is suspended in this cavity by small muscles. The malleus is promptly attached to the eardrum, while the incus and the stirrup are attached to the malleus and oval window respectively. The acoustic wave that reaches the eardrum is transmitted to the oval window as a mechanical vibration. It is worth noting that the ossicular chain, oval window and eardrum provide acoustic impedance matching. This leads to more efficient transfer of the mechanical vibration to the inner ear.

The inner ear is a fluid-filled bony structure embedded deeply in the temporal bone of the skull. It consists of the cochlea and auditory nerve. Generally, the inner ear performs the conversion of the mechanical vibration represented by the pressure wave coming from the oval window into electrical nerve signals or “spikes” to be communicated with the central nervous system and hence to the brain. The sound pressure wave propagates down the fluid and membrane structure of the cochlea by their combined movement. Since the fluid is incompressible and according to the fluid mass conservation, the round window moves in opposition to the stirrup, as obtained experimentally [1.4].

The basilar membrane is narrow and stiff and is situated at the cochlea basal end. Hence, the membrane-displacement waves propagate quickly with a long wavelength. As the wave travels down the cochlea, the membrane stiffness decreases, the waves become slower, shorter, and increase in amplitude. At some point, known as the best place for the given input frequency, the membrane vibrates with maximum
amplitude. Beyond that position, the basilar membrane becomes too flexible and highly damped to support wave propagation at that frequency, and dissipates rapidly, the wave energy beyond it. It is worth noting that the maximum displacement position of the basilar membrane is observed to vary approximately logarithmically with the frequency of the input [1.5].

From the electrical engineering point of view, the cochlea can be considered as a frequency analyzer and feature extractor for the acoustic input. Also, the outer hair cells within the cochlea have active characteristics in controlling the gain of certain frequency bands [1.6].

1.7 Hearing Deficiencies

Hearing deficiencies can be classified into the following main reasons

1.7.1 Conductive impairment

This impairment is in the outer or middle ear, making them unable to pass acoustic energy properly to the inner ear. In this case the acoustic wave suffers from attenuation. This type of impairment can be overcome by using a simple hearing aid. This hearing impairment may be due to a disease in the outer ear or damage to the ear drum.

1.7.2 Sensorineural impairment

This impairment occurs in the inner ear. It may be a result of exposure to high volume levels or bacterial infection which leads to damage of the inner ear, or due to aging of the basilar membrane which causes changes in its features by make it stiffer and less elastic. In this case the acoustic wave suffers attenuation and distortion. A more
complicated hearing aid is needed for such types of impairment compared to that related with outer or middle ear defects.

1.8 Hearing Loss Categories

As a result of the two above sources of physiological impairments, the following four categories of hearing loss appear.

1.8.1 Attenuation Loss

This type of loss takes place due to conductive or sensorinueral impairments. It appears as attenuation in amplitude of a range of frequencies. Its effect on hearing is to perceive one part of sound or speech to be quieter than the other. This loss can be measured by the use of an audiogram [1.7]. One of the techniques is linear amplification that uses a constant gain to compensate for such attenuation. There are other techniques which depend on non-linear amplification [1.8]. Some other techniques are used to explain the nature of hearing impairments and suggest or eliminate compensatory signal-processing schemes for them [1.9].

1.8.2 Compression Loss

In this case, due to sensorinueral impairment, the dynamic range of sounds is compressed resulting in the inability to recognize sound levels. This is because the threshold level (T-level) becomes higher or the maximum level of comfortable listening of loud sounds (C-level) is changed. This loss can be measured using the audiogram by setting the categorical loudness scaling [1.7]. An appropriate signal processing scheme for compensation in accordance to the loss level can be used. This is done by reducing the dynamic range to that of the patient.
1.8.3 Perceptual Loss

This type of loss also belongs to sensorinueral impairment, whereby due to background noise, the speech intelligibility is reduced. When the signal to noise ratio, SNR is high, it reduces the noise ability in masking the sound fundamental elements. For low SNR levels, the noise effect becomes obvious. In this case, the hearing-impaired can not distinguish speech. The adaptive signal processing scheme for compensation of such loss is used [1.10].

1.8.4 Bi-aural Loss (Bilateral hearing loss)

This type of loss is a result of sensorinueral impairment. Because of impairment in analysing the information from both ears, the patient is unable to recognize between speech and noise as well as failure in localising sound sources. An adaptive signal processing scheme with two inputs from different sound sources can reduce the problem [1.11].

1.9 Hearing Aids

A hearing aid is an electro-acoustic, body-worn apparatus which typically fits in or behind the wearer's ear, and is designed to amplify and modulate sounds for the wearer.

There are following basic types of hearing-aid technologies

1.9.1 Conventional Hearing Aids

These have a microphone input followed by a processing stage to change acoustic characteristics as required. The processed signal goes to the ear drum and auditory system. This type of hearing aid includes four styles as explained below
1. **Completely-in-the-Canal (CIC)**

This style is shown in Figure 1.2 (a). It is the smallest type of hearing aid made and is almost invisible in the ear. All its components are housed in a small case that fits deeply inside the ear canal. These hearing aids are restricted to persons with ear canals large enough to accommodate the insertion depth of the instrument into the ear and it is suitable for mild to moderate hearing losses. Also it is most difficult to place and adjust.

2. **In-the-Canal (ITC)**

This is slightly larger than the CIC as shown in Figure 1.2 (b), but is still unobtrusive. It fits down in the canal of the ear and is relatively unnoticeable. It is easier to use compared to the CIC type despite that it has a slightly larger battery than the CIC. It is suitable for use with mild to moderate hearing impairment.

3. **In-the-Ear (ITE)**

This is a larger device which fills the "bowl" of the ear as in Figure 1.2 (c). Due to its larger size, it can accommodate bigger audio amplifiers and more features such as a telephone switch. It is easier to use than CIC or ITC models. These hearing aids can be used for a wider range of hearing losses.

4. **Behind-the-Ear (BTE)**

This is presented in Figure 1.2 (d) which shows circuitry and microphone fitting behind the ear. It meets a wide range of hearing needs, including severe hearing impairments. Due to its robust design, this style is especially recommended for children. It aids can provide more amplification than smaller devices due to the large amplifier and battery.
CHAPTER ONE

Introduction and Review

LOW POWER ELECTRONIC CIRCUITS FOR BIOMEDICAL APPLICATIONS

Saad A. Hasan

Figure 1.2 Conventional hearing aids technologies

(a) CIC (Completely in the Canal)

(b) ITC (In the Canal)

(c) ITE (In the Ear)

(d) BTE (Behind the Ear)
1.9.2 Bone Anchored Hearing Aids (BAHA)

The BAHA soft band and implanted system is more beneficial over traditional bone-conduction hearing aids. The BAHA is an auditory prosthetic which can be surgically implanted. It uses the skull as a pathway for sound to travel to the inner ear. For people with severe conductive losses, the BAHA is used to bypass the external auditory canal and middle ear, and send the acoustic vibrations to the cochlea [1.12]. For people with unilateral hearing loss, the BAHA uses the skull to conduct the sound from the deaf side to the side with the functioning cochlea.

1.9.3 Subcutaneous piezoelectric attached hearing actuator (SPAHA)

This is a more advanced hearing aid proposed for compensation of conduction loss [1.13]. It is based on a piezoelectric bending actuator. The device lies flat against the skull which would allow it to form the basis of a subcutaneous bone-anchored hearing aid. The bone-bending excitation is obtained through a local bending moment rather than the application of a point force as in the BAHA. Cochlear velocity measurements are created by the actuator, leading to a high efficiency, making it a possible future candidate for electromagnetic bone-vibration actuators [1.13].

1.9.4 Middle Ear Implants (MEI)

The MEI implant is directly fixed to one of the ossicles in the middle ear, leaving the ear canal free. This is preferable especially for patients more sensitive to foreign objects inside their ear canals. Another advantage is the ability to cancel the feedback loop effect which is apparent in conventional hearing aids [1.14].
1.9.5 Cochlea Implants (CI)

This consists of two basic units, the electrode array and the signal processing unit. The array of electrodes is surgically implanted either inside or against the outside of the cochlea to directly mimic the auditory nerve. The signal processing units consist of many stages generally represented by microphone, the preamplifier and automatic gain control, band-pass filter bank, envelope detector, compressor, and the modulator. Figure 1.3 shows the block diagram of the cochlear implant “bionic ear”. The acoustic input is converted to electrical signals by the microphone, and then processed by the pre-amplifier and automatic gain control stage. The band-pass filter divides the signal into different frequency bands, and then the envelope “peak” of each band is detected by the envelope detector. The dynamic range of each band is compressed to fit to the patient and then sent to the modulator. The modulated signal bands are then sent to the electrode array which in turn, provides stimulation of the patient’s neurons [1.15], [1.16]. The number of patients who use the cochlear implants is 200000 around world [1.17].

![Figure 1.3 Block diagram of a bionic ear consisting of M-channels signal processor](image)

The challenge related to the CI is the relatively high power consumption, which needs to be reduced from milli-volts to micro-volts [1.18] in order to increase the
battery life time. Many approaches have been proposed to cope with this difficulty and are described in section 2.8. The aim is to satisfy the necessary specifications, outlined in section 2.6, to meet the features of the biological cochlea.

1.9.6 Auditory Brainstem Implants (ABI)

This is a surgically implanted device to provide a sense of sound to profoundly deaf individuals. In this case, the patients are suffering from illness or injury damaging their cochleas or auditory nerves. So, the stimulation of the brain stem of the recipient is required. This is obtained with the suitable technology and the brain surgery for device implantation. Much effort is being spent in this context to develop and use the auditory brainstem implants to stimulate nerves by electrodes and transfer directly the information to auditory brain stem [1.19].

1.10 The Coding Strategies of Cochlear Implant

The essential objective of using the signal processor is to decompose the input signal into its frequency components. This is accomplished by dividing the input signal into different frequency bands then sending the filtered signals to the appropriate electrodes.

The coding strategy can allow identification of the approaches used to alter the acoustic input features to satisfy convenient nerve stimulation within the cochlea. Developing coding strategies with appropriate noise reduction algorithms leads to the specification of advanced cochlear implants. This enables the hearing-impaired to get the best understanding of the acoustic signal on the one hand, whilst increasing the discrimination ability between the signal and noise for better patients communication in noisy environments, on the other hand[1.15].
There are many coding strategies. Some of those are Maximum Spectral Peak Extraction [1.20], Compressed Analogue [1.21], Continuous Interleaved Sampling [1.22], and Spectral Maxima Sound Processor [1.23].

1.11 Specification of Hearing Aid Design

The hearing aids have some specifications that are always considered by designers. This is to mimic some unique aspects offered by the biological auditory system and to make it acceptable for most users. The HA design should consume a minimum possible power to increase the battery life time. This is very important especially for fully implanted future cochlear aids. They should operate with small voltage rails to use small batteries which mean small size devices. The operational reliability using appropriate signal processors and flexibility by adopting or proposing good designs are important. Finally, the hearing aid devices should satisfy all or most of the above requirements with a minimal possible cost.

1.12 The use of CMOS OTA-C Filters in Analogue Hearing Aids

In analogue circuits, filters can be considered as basic building blocks [1.24]. Filters can be utilised in many audio applications such as speech recognition, processing for cochlear implants, and other applications. OTA-C filters are the most power efficient choices for low power, low-voltage, and low frequency applications. They use the transconductance of transistors, usually operating in sub-threshold and use buffering directly. For micro-power audio applications, generally either OTA-C or log domain filters are used. They are preferred over other approaches such as MOSFET-C and switch capacitor filters. The MOSFET-C filters have additional requirements represented by an amplifier with a high gain and higher bandwidth than that of the filter itself. The switch capacitor filters suffer from sampling errors and problems which may
appear due to clock feed-through. In spite of the successful use of log domain filters in micropower applications, they have some disadvantages. One of these is the noise signal which is affected by the input signal level. Also, the log domain filters performance is highly sensitive to device mismatch. Such mismatch causes distortion due to the non-linear nature of those filters, such that their performance needs to be assessed using specific tests [1.25]. OTA-C filters on the other hand, offer the low power and wide tuneable frequency range required in hearing aids applications. One major limitation of sub-threshold OTA-C filters is represented by their narrow input linear range. From the above points, it can be concluded that the OTA-C filters can represent the best choice for such applications when their linear range is increased properly.

1.13 Review of Hearing Aid Design Approaches using OTA-C Filters

The biological cochlea is a good example of a complete system. It can sense 0.5nm of eardrum motion at its best frequency. Its input dynamic range spans 12 orders of magnitude in sound intensity that is 120 dB. It operates over a frequency range of about 3 decades with a power dissipation of merely a few tens of microwatts [1.26].

Hearing aids and particularly cochlear implants play an important role to help people suffering from severe hearing problems. It is now possible to restore partial hearing for people with such deficiencies. Efforts of many scientists and researchers from various disciplines results in many approaches in the field of cochlea implant design. A review of some approaches in that context based on CMOS OTA-C filters which have been proposed and successfully tested, is summarized below.

Lyon et al in 1988 [1.27] produced the widely known, Lyon and Mead silicon cochlea model. The analogue electronic cochlea has been built in MOSIS CMOS VLSI technology using micropower techniques with sub-threshold operation. The key point of the model and circuit is a cascade of 480 stages of 2nd order filters which are simple,
linear and, with controllable Q parameters to capture the fluid-dynamic physics of the traveling-wave system in the cochlea. The effects of adaptation and active gain present in the outer hair cells in biological cochlea are implemented. An exponential variation of time constants is easy to achieve using a linear voltage gradient on transistor gates, yielding a log frequency scale. The total current supplied to all cochlea stages is only about a microampere. Measurements on the test chip suggest that the circuit matches both the theory and observations from real cochleas.

Watts et al in 1992 [1.28] proposed a sub-threshold transconductance amplifier, OTA with source degeneration using diode-connected transistors, one on each side of the differential pair. This leads to decrease the effective value of electrostatic coupling coefficient between the gate and channel of the OTA MOSFETs. The input linear range was increased by a factor of 2.4 from 60mV\text{PP} to 144mV\text{PP} with a supply voltage of 5V. The price of this improvement was a decrease in the common-mode operating range and an increase in thermal noise. The proposed OTA was used to construct 2\textsuperscript{nd} order low-pass filters. Then a cochlear consisting of 51 cascaded stages of those low-pass filter sections was implemented and tested successfully. The proposed cochlea was built in the MOSIS double-poly, double-metal 2µm CMOS technology. It had a dynamic range of 55 dB and consumed a power of 11µW. The test chips consumed 7.5mW of power.

Sarpeshkar et al in 1998 [1.29] presented an analogue electronic cochlea, which processed sounds with 61 dB dynamic range. It was supplied by a voltage of 5V and consumed 0.5mW power. The cochlea was built in a 1.2µm CMOS process and consisted of 117 stages of 2\textsuperscript{nd} order low-pass filters. It covered the frequency range of (100-10k) Hz and had the widest dynamic range of any artificial cochlea built to that date. The wide dynamic range was attained through the use of a wide-linear-range transconductance amplifier. The filter topology was low-noise, with a dynamic gain control, AGC at each stage. The cochlea robust operation was achieved by using automatic offset-compensation circuitry.
Deng et al in 2004 [1.30] produced a simple, auditory perception model for noise-robust speech feature extraction. Continuous-time, 32 programmable analogue OTA-C filter channels for efficient low-power and real-time implementation were used. Each channel contains two band-pass or low-pass 2nd order filters, a full-wave rectifier, and a 1st order low-pass filter. The filters could be configured in parallel or cascade filter bank topologies. Their input linear range was 2.4\text{V}_{pp}. A prototype chip was fabricated in a 0.5\text{m} CMOS technology with 5V voltage rail. Results of the proposed model confirmed the robustness of its auditory features to noise of different statistics, significantly outperforming aspects at elevated noise levels, down to 10 dB SNR.

Chan et al in 2007 [1.31] presented an analogue integrated circuit containing a pair of silicon cochleas with an address event interface. Each section of the cochlea was implemented with 32 stages of cascaded 2nd order low-pass filter sections. Each filter section was followed by both inner hair cell and spiking neuron circuits. The cascaded stages had exponentially decreasing cut-off frequencies. The exponential decrease was obtained by using CMOS compatible lateral bipolar transistors to create the bias currents of the 2nd order sections. Power supply voltage was 4.5V and an input linear range up to 140 mV_{pp} was achieved. The chip was built in a 3-metal 2-poly 0.5\text{m} CMOS process.

Liu et al in 2010 [1.32] described an event-based binaural silicon cochlea for spatial audition and auditory scene analysis. It consisted of a matched pair of 64-stage cascaded analogue 2nd order filter banks with 512 pulse-frequency modulated (PFM) address-event representation, AER outputs. It was fabricated in a 4-metal 2-poly 0.35\text{m} CMOS process with a supply voltage of 3.3V. The analogue core and the digital part consumed power of 33mW and 25mW respectively. The cochlea dynamic range was measured to be 36dB with 25mV_{pp} to 1500mV_{pp} at the microphone preamplifier output.
1.14 Conclusion

A general introduction about the use of analogue integrated OTA-C filters in biomedical applications such as hearing aids and EEG systems has been presented, emphasizing the need for low-power low-voltage circuits. The main contribution of this work was then introduced and explanations of the project aims mentioned. A brief description of the biological human auditory system was then presented with a short summary of their anatomy and essential functions. The nature of hearing deficiencies was then discussed and classified according to the place and nature of the impairment. Hearing aids for such losses were presented and their specifications also mentioned. The uses of the sub-threshold OTA-C filter in hearing aids were found to be more suitable, after comparing it with other filters. Finally, a review of some successfully implemented CMOS cochleas and OTA-C filters which are perfect for use in cochleas were presented.

References


CHAPTER ONE

Introduction and Review


CHAPTER TWO

The MOSFET in Sub-threshold Regime

2.1 Introduction

The Metal Oxide Semiconductor Field Effect Transistor, MOSFET consists of four terminals gate, G, drain, D, source, S, and bulk, B respectively. Recently, a large variety of very large scale integration, VLSI analog computation systems have been realized, that operate in the sub-threshold regime. CMOS technology found its way into most analogue and digital applications making it preferred over bipolar or GaAs approaches. This is due to its low power consumption, ease of scaling-down capability, and more recently, the relative ease of putting analogue and digital CMOS circuits on the same chip so as to optimise the system performance. In low power applications, small voltage supplies and very small current levels in the ranges of (1-3) V and (1n-1µ) are respectively required [2.1]. This field of application was motivated by the development of low power electronic watches and extended fast to cover many other applications such as in telecommunications, portable, and biomedical fields [2.2].

2.2 MOSFET operation

2.2.1 Regions of operation

The MOSFET is a voltage controlled current source device. Its output current is obtained by applying appropriate voltages to the gate, drain, source, and bulk terminals. For the NMOSFET of Figure 2.1 below, it is considered that three of its terminals
represented by drain, source, and bulk are connected to ground. According to the value of the gate voltage, $V_G$, the three following operation modes will appear [2.2].

![NMOSFET symbol](image1)

![NMOSFET cross-sectional view](image2)

Figure 2.1 NMOSFET (a) symbol, (b) cross sectional view
1. Accumulation

For $V_G < 0$, the charge carriers represented by holes in the substrate are attracted and “accumulated” on the surface under the gate oxide. The total capacitance between the gate terminal and ground in this case is that associated with the gate oxide, $C_{OX}$. No current is flowing between source and drain in this case. The value of $C_{OX}$ is as follows

$$C_{OX} = C_{gs} + C_{gd} + C_{gb}$$

(2.1)

where

$C_{gs}$, $C_{gd}$, and $C_{gb}$ represent the gate to source, gate to drain, and gate to bulk capacitances.

2. Weak Inversion

For small negative $V_G$ values, the surface is still in accumulation. For small positive $V_G$ values the surface under the gate oxide is depleted from existing holes, leaving in their place acceptor ions with negative charge contribution. Also a small concentration of electrons is attracted under the gate due to this positive voltage. This results in a small concentration of electrons flowing from source to drain, assuming a positive voltage is applied to the drain. The MOSFET in this case is said to operate in the weak inversion region and the electrostatics are dominated by the acceptor charge. The associated capacitance under the gate terminal is known as the depletion capacitance. Therefore, the total capacitance between the gate and substrate terminals is represented by the series equivalent of gate oxide and depletion capacitances.
3. Strong Inversion

With further increase of the positive value of $V_G$, more electrons are attracted under the gate and the depletion region width continues to increase. At a certain value of $V_G$ known as the threshold voltage a heavily n$^+$ channel under the gate is constituted between the source and drain, a gradual channel is formed whereby the electrostatics are dominated by the channel electrons and a strong electron current flows from source to drain. In this case, the MOSFET is in its ‘on’ state. If $V_G$ is increased further, the channel charge density will increase leading to increasing current. The depletion region is relatively unchanged.

2.2.2 MOSFET current/voltage Relations

1. Strong inversion region

The value of current for a MOSFET in Figure 2.1 depends on the charge density, $Q_I$ in its direction of flow. The magnitude of the free electrons charge density, $|Q_I|$ is much more than that in depletion region, $|Q_d|$. The total flowing charge due to charge density of $Q_I$ coulombs/metre through a cross section equals to the multiplication of $Q_I$ by the charge velocity, $u$ in meters/second as follows

$$I_{DS} = Q_I u$$  \hspace{1cm} (2.2)

and

$$Q_I = -W C_{OX} (V_{GS} - V_{TH})$$  \hspace{1cm} (2.3)

where $|Q_d|$ is the charge density that is proportional to the term $(V_{GS} - V_{TH})$ since the inversion operation mode takes place as $V_{GS} = V_{TH}$. $C_{OX}W$ is the total capacitance per unit
length. It is assumed above that the NMOSFET in Figure 2.1 has a drain voltage of zero. Considering now the charge density for a drain voltage of $V_D$, with source voltage and substrate at zero volts, it is obvious that the channel voltage changes in this case. Consequently, the difference between the gate and channel changes along the distance from source to drain is by $V_G$ to $V_G - V_D$ respectively. Hence, at an arbitrary point, $x$ in the inversion layer the charge density and the current are as follows

$$Q_1(x) = -W C_{Ox} \left(V_{GS} - V(x) - V_{TH}\right)$$

(2.4)

$$I_{DS} = Q_1(x) \cdot u$$

(2.5)

where $V(x)$, is the voltage at point, $x$.

The charge velocity $u$ is equals to $(\mu_n E)$ where $\mu_n$ is the average mobility of electrons (assumed to be constant) and $E$ is the electric field.

$$I_{DS} = W C_{Ox} \left(V_{GS} - V(x) - V_{TH}\right) \mu_n \frac{dV(x)}{d(x)}$$

(2.6a)

where the electric field, $E$ is defined as in equation (2.6b) below

$$E = -\frac{dV(x)}{d(x)}$$

(2.6b)

To find the total MOSFET current from source to drain, both sides of the equation (2.6a) are integrated. This corresponds to variations in MOSFET effective length and voltage difference of (0 to $L$) and (0 to $V_{DS}$) respectively as follows in equations (2.7) and (2.8)

$$\int_{0}^{L} I_{DS} \cdot dx = \int_{V=0}^{V_{GS}} W C_{Ox} \mu_n \left(V_{GS} - V(x) - V_{TH}\right) \cdot dV$$

(2.7)
\[ I_{DS} = \mu_n C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} \right) V_{DS} - \frac{1}{2} V_{DS}^2 \]  

(2.8)

where the term, \( V_{GS} - V_{TH} \), is known as the overdrive voltage and \( V_{DS} \) is the drain-source voltage. It is important to notice that the electric field due to \( V_{DS} \) leads to a drift of charge carriers to the drain in the strong inversion case. The dependence of the drain-source current on the values of \( V_{DS} \) and the overdrive voltage is discussed in the two following cases:

I. For \( V_{DS} \leq \left( V_{GS} - V_{TH} \right) \)

The MOSFET is said to be in the unsaturated or triode region. It operates as a resistor with the current-voltage relation governed by equation (2.8) above, with the quadratic term in \( V_{DS} \) close to zero.

II. For \( V_{DS} > \left( V_{GS} - V_{TH} \right) \)

When increasing the \( V_{DS} \) beyond the overdrive voltage, the drain-source current value is recognised to be relatively constant. In this case, the MOSFET is said to be operated in the saturation region; it operates as a current source. As the value of \( V(x) \) becomes close to the overdrive voltage, the charge density in the inversion layer, \( Q_I \) at the drain end of the channel reaches to zero. This will take place at a distance, \( x \leq L \) where the inversion layer disappears and the channel is said to be “pinched off”. The associated channel shrinkage is referred to as channel length modulation as a result of increasing \( V_{DS} \) beyond the overdrive voltage. The current equation is obtained from integrating equation (2.6) above as in below

\[
\int_0^{\frac{V_{GS} - V_{TH}}{V}} I_{DS} \cdot dx = \int_{V=0}^{V} WC_{ox} \mu_n \left( V_{GS} - V(x) - V_{TH} \right) \cdot dV
\]

(2.9)

\[
I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} \right)^2
\]

(2.10a)
The dependence on \( V_{DS} \) can be modelled as

\[
I_{DS} = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})
\]  

(2.10b)

where \( \lambda \) is the channel length modulation parameter which equals the reciprocal of early voltage. \( L' \leq L \), where \( L' \) is the effective channel length after shrinking due to channel length modulation.

2. Small-signal model of the MOSFET

Equations (2.8) and (2.10) (a), (b) above describe the dc operation of the MOSFET. In the case of analogue operation of transistors, the voltage and current values are composed of large DC components with some small ac deviation around them. When the signal perturbation on MOSFETs is small enough, an approximate small-signal model can be proposed. Such an approximation takes small changes around MOSFET bias points and the operation of the MOSFET can be considered to be linear. The parameters of this linear system can be obtained from the DC model. Many researchers discussed the important requirements for good MOSFET modelling for large-signal and small-signal models for analogue and mixed analogue-digital design [2.3]-[2.5]. The small-signal model of an ideal MOSFET is shown in Figure 2.2 below.

![Figure 2.2 Ideal MOSFET small-signal model](image-url)
In this model, the MOSFET has an open circuit input with an input voltage of \( v_{gs} \) and its output is governed by the dependent current source, \( g_m v_{gs} \). The MOSFET output varies linearly with \( v_{GS} \) and its transconductance \( g_m \), the most essential parameter in this model. It is clear from equation (2.10a) above, that the current value is independent of \( V_{DS} \) since \( L' \approx L \). The MOSFET in this case produces a current as a response to overdrive voltage. Its transconductance, \( g_m \) represents a figure of merit that identifies how well this conversion is done. It can be considered as the ratio of change of current to voltage which obtained for above-threshold case [2.6] as follows:

\[
g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \bigg|_{V_{DS,\text{Constant}}} \tag{2.11}
\]

\[
g_m = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH}) \tag{2.12}
\]

\[
g_m = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_{DS}} \tag{2.13a}
\]

\[
g_m = \frac{2I_{DS}}{V_{GS} - V_{TH}} \tag{2.13b}
\]

It is worth noting that the MOSFET model of Figure 2.2 above assumes an ideal MOSFET. However, the MOSFET drain-source current is also affected by channel length modulation resulting from increasing \( V_{DS} \) more than the overdrive voltage. So, this effect can be added to the small signal model as a resistor, \( r_o \) connected between MOSFET’s drain and source as in Figure 2.3 below. The value of the resistor, \( r_o \) can be derived by differentiation of Eqn. 2.10b, as follows
\[ r_O = \frac{\partial V_{DS}}{\partial I_{DS}} = \lambda V_{DS} \quad (2.14) \]

![MOSFET small-signal model after adding channel modulation effect](image)

Figure 2.3 MOSFET small-signal model after adding channel modulation effect

The MOSFET small signal model parameters and the subscripts in Figure 2.3 above are expressed in small letters.

3. Weak inversion region

It has been assumed above that at \( V_{GS} < V_{TH} \), the MOSFET turns off abruptly. This is not the case since a weak inverted channel still exists at those low \( V_{GS} \) values as mentioned earlier in section 2.2.1. The associated current flow is denoted as sub-threshold current. In this case the sub-threshold current, \( i_{DS} \) shows an exponential dependence on \( V_{GS} \) [2.6], [2.7]. This type of operation is very beneficial in low-power applications such biomedical applications, solar powered calculators, battery-operated watches, and many other applications.

The dominance of the acceptor charge in sub-threshold implies that the surface potential, \( \psi_s \), is independent of position on the weak inverted channel and only depends on gate-bulk voltage, \( V_{GB} \). Thus the depletion region charge density, \( Q_B \) and
consequently the depth of depletion region can be assumed to be independent of position along the weak inverted channel [2.6]; all surface points along the weak inverted channel are of the same potential with respect to substrate. It follows that there is no horizontal electric field, leading to the conclusion that the channel current is due to the diffusion mechanism. From above, it can be concluded that the drain-source current, $i_{DS}$, along any point in the channel consists two components; the first one is the drift current that is proportional to the electric field or derivative of surface potential, and the second component is the diffusion current which proportional to the derivative of the charge density such that:

$$i_{DS} = W\left(-\mu_n Q_l \frac{\partial \psi}{\partial x} + \mu_n U_T \frac{\partial Q_l}{\partial x}\right)$$  \hspace{1cm} (2.15)

The first term in equation (2.15) is the drift current which is obtained in part 1 in this section, while the second term represents the diffusion current. The magnitude of the free electron charge density, $|Q_l|$ is less than that in depletion region, $|Q_B|$. There is a charge density, $Q_I'$ gradient from source to drain terminals which causes the diffusion mechanism. The charge densities at $x=0$ and $x=L$ are shown in equation (2.16)

$$|Q_I|_{x=0} = Q_{I0} \text{ and } |Q_I|_{x=L} = Q_{IL}$$

$$Q_{I0} \propto \exp\left(-\frac{V_S - \kappa V_G}{U_T}\right) \text{ and } Q_{IL} \propto \exp\left(-\frac{V_D - \kappa V_G}{U_T}\right)$$  \hspace{1cm} (2.16)

where

$V_S$, $V_D$, $V_G$, and $U_T$ are the source voltage, the drain voltage, the gate voltage, and the thermal voltage. The thermal voltage, $U_T$ is expressed as follows

$$U_T = \frac{kT}{q}$$  \hspace{1cm} (2.17)
where \( k \), \( q \), and \( T \) are the Boltzmann’s constant of \( 1.38 \times 10^{-23} \), the electron charge of \( 1.6 \times 10^{-19} \) C, and the absolute temperature in Kelvin. \( U_T \) is equal to about 26 mV at room temperature. The variable \( \kappa \) represents the sub-threshold coupling coefficient of the MOSFET. It is expressed as follows

\[
\kappa = \frac{\partial \psi_s}{\partial V_G} = \frac{C_{ox}}{C_{ox} + C_{dep}} \tag{2.18}
\]

where \( C_{dep} \) is the capacitance of depletion region. It can be considered that \( \kappa \) represents a measure of quality or fitness that the gate voltage can control the charge carriers and consequently the current in the weak inversion layer. Typically, \( \kappa \) has a value of 0.7. It is important to refer that sometimes \( \kappa \) is exchanged with its reciprocal, \( n \) which equals \( 1/\kappa \) and is denoted by the sub-threshold slope factor \([2.8]\). For long channel devices, \( \kappa \) can be considered as constant. Figure 2.4 show this gradient in charge density. From equations, (2.15) and (2.16), the drain-source current, \( i_{DS} \) is obtained as follows

Figure 2.4 Inversion layer charge density versus distance from source to drain in the MOSFET weak inversion operation mode; (a) Linear region, (b) Saturation region
\[ i_{DS} = W \mu_n U_T \frac{\partial Q_i}{\partial x} \]  
\[ (2.19a) \]

\[ i_{DS} = \frac{W}{L} \mu_n U_T (Q_{i0} - Q_{i0}) \]  
\[ (2.19b) \]

\[ i_{DS} = \frac{W}{L} \mu_n U_T \left( -Q_{i0} \left( 1 - \frac{Q_{il}}{Q_{i0}} \right) \right) \]  
\[ (2.19c) \]

\[ \frac{Q_{il}}{Q_{i0}} = \exp \left( -\frac{V_D - \kappa V_G - (V_S - \kappa V_G)}{U_T} \right) = \exp \left( -\frac{V_{DS}}{U_T} \right) \]  
\[ (2.19d) \]

By substituting equation (2.19d) in (2.19c)

\[ i_{DS} = \frac{W}{L} I_0 \exp \left( \frac{\kappa V_G - V_S}{U_T} \right) \left( 1 - \exp \left( -\frac{V_{DS}}{U_T} \right) \right) \]  
\[ (2.20) \]

where \( I_0 \) is a process dependent constant. For the NMOSFET, it is found as follows

\[ I_0 = \mu_n C_{ox} U_T^2 \frac{1 - \kappa}{\kappa} \exp \left( -\frac{\kappa V_{TH}}{U_T} \right) \]  
\[ (2.21) \]

From equation (2.20) above, the last term is approximately unity for the value of \( V_{DS} > 4U_T \) where the error is less than 2%. So, equation (2.20) can be simplified to be as follows

\[ i_{DS} = \frac{W}{L} I_0 \exp \left( \frac{\kappa V_G - V_S}{U_T} \right) \]  
\[ (2.22) \]

It is interesting to see that equation (2.22) shows the drain-source current independence of \( V_{DS} \). Therefore, the required condition for the MOSFET to operate in saturation region in sub-threshold regime is to ensure that \( V_{DS} > 4U_T \). Hence, \( V_{DS} \) of only
100 mV is needed for MOSFET to operate as a current source in this regime. The bulk potential affects the threshold voltage and from equations (2.21) and (2.22) above, the drain-source current is affected. Assuming that all other potentials are constant, the MOSFET drain-source current can be considered as a function of bulk potential which becomes like a second gate in the MOSFET. Its effect in the small signal MOSFET model can be modelled as a dependent current source of $g_{mb}v_{bs}$ as shown in Figure 2.5 below. Therefore, Figure 2.5 represents the small signal MOSFET model in weak inversion region with the parameters of $g_m$, $r_o$, and $g_{mb}$ expressed as follows:

\[ g_m = \frac{\partial i_{DS}}{\partial v_{GS}} \bigg|_{v_{DS}, v_{BS} \text{ constant}} = \frac{i_{DS}}{U_T} \kappa \]  \hspace{1cm} (2.23)

\[ g_{mb} = \frac{\partial i_{DS}}{\partial v_{BS}} \bigg|_{v_{DS}, v_{GS} \text{ constant}} = \frac{i_{DS}}{U_T} \left( \frac{C_{dep}}{C_{dep} + C_{OX}} \right) = \frac{i_{DS}}{U_T} (1 - \kappa) \]  \hspace{1cm} (2.24)

\[ g_{ds} = \frac{\partial i_{DS}}{\partial v_{DS}} \bigg|_{v_{GS}, v_{GS} \text{ constant}} = \frac{W}{L} I_0 \frac{\exp \left( \frac{\kappa V_G - V_s}{U_T} \right)}{U_T} \exp \left( \frac{-V_{DS}}{U_T} \right), \quad V_{DS} \leq V_{DSAT} \]  \hspace{1cm} (2.25)
In equation (2.25) above, the \( g_{ds} \) should reach to zero at saturation since the last exponential term approaches zero for \( V_{DS} \geq 100\text{mV} \). However, \( g_{ds} \) still has a finite value beyond saturation due to the Early effect as in equation (2.26) below.

\[
g_{ds} = \frac{1}{r_{O}} = \frac{I_{DS}}{U_{T}}, \quad V_{DS} > V_{DSAT} \tag{2.26}
\]

where

\[
i_{DS} = I_{DS} + i_{ds}
\]

\[
v_{GS} = V_{GS} + v_{gs}
\]\n
\[
v_{BS} = V_{BS} + v_{bs}
\]

\[
v_{DS} = V_{DS} + v_{ds}
\]

In equation (2.27) above, the capital letters and subscripts refer to the DC operation while the small letters and subscripts refer to the small signal ac operation. The summations of them reflect the normal operation with voltage and current values of DC large signal components with small signal ac deviations around them.

2.3 The Test Chip

2.3.1 Introduction

The test chip is shown in Figure 2.6 below. It is fabricated in the AMS mixed signal process using 0.35µm, double poly, 3 metal, CMOS C35 Technology and has dimensions of 2.6mm×2.6mm. It consists of many circuits represented by three groups of MOSFETs, various OTAs, proposed OTA-C filter topologies, a 4-channel filter bank for hearing aids, and an OTA-C filter for EEG applications as detailed in next sections.
Figure 2.6 2.6mm×2.6mm Fabricated test chip

2.3.2 Architecture

The test chip blocks labelled 1-11 are explained as follows:

1. 1st group of 12 test MOSFETs with three different aspect ratio of (6 µm /6 µm), (30 µm /6 µm), and (12 µm /12 µm) for each four MOSFETs.

2. The 4-channel OTA-C band-pass filter bank.

3. 2nd group of 6 test MOSFETs with three different aspect ratio of (6 µm /6 µm), (30 µm /6 µm), and (12 µm /12 µm) for each two MOSFETs.
4. The proposed OTA-C band-pass filter topology 1 for hearing aids. The proposed OTA MOSFETs dimensions are mentioned in table (3.1).

5. Another proposed OTA-C band-pass filter topology 1 for hearing aids with another OTA dimensions. Those are represented by (15 µm /3 µm) for differential and mirror MOSFETs, (30 µm /3 µm) for bumping MOSFETs, and (30 µm /6 µm) for bias MOSFET.

6. The proposed OTA-C band-pass filter for EEG applications.

7. The proposed OTA for hearing aids.

8. The proposed OTA for EEG applications.

9. Different OTAs represented by the simple OTA and the OTA with bumping MOSFETs.

10. 3rd group of 12 test MOSFETs with three different aspect ratio of (6 µm /6 µm), (30 µm /6 µm), and (12 µm /12 µm) for each four MOSFETs.

11. The proposed OTA-C band-pass filter topology 2 for hearing aids.

The measured output and transfer characteristics to the MOSFET groups will be presented in the next section. Also, they will be compared with simulation results. The other details including the measured results related with the proposed OTA, the OTA-C filters and filter bank for hearing aids, and the OTA-C filter for EEG applications will be presented in chapters three, five, and six respectively.
2.4 Measured and simulated MOSFETs transfer characteristics

The transfer characteristics for the MOSFETs were obtained using the Semiconductor Parameter Analyzer 4155B with $V_{DS}$ set at 0.1V. The simulated results for the MOSFETs were obtained using Cadence circuit simulator, SpectreS with BSIM3v3.1 models and parameters from the AMS process for 0.35µm CMOS C35 Technology. Some of these parameters are presented in Table 2.1 below.

Table 2.1: Key device parameters for BSIM3v3.1 model in AMS process for 0.35µm CMOS C35 Technology

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Unit</th>
<th>NMOST</th>
<th>PMOST</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate oxide Thickness</td>
<td>$T_{OX}$</td>
<td>nm</td>
<td>7.57</td>
<td>7.75</td>
</tr>
<tr>
<td>Effective substrate doping</td>
<td>$N_{CH}$</td>
<td>cm$^{-3}$</td>
<td>2.61×10$^{17}$</td>
<td>1.01×10$^{17}$</td>
</tr>
<tr>
<td>Effective mobility</td>
<td>$\mu_o$</td>
<td>cm$^2$/Vs</td>
<td>475</td>
<td>148</td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>$V_{TH0}$</td>
<td>V</td>
<td>0.49</td>
<td>-0.69</td>
</tr>
<tr>
<td>Flicker noise coefficient</td>
<td>$K_F$</td>
<td>____</td>
<td>2.17×10$^{-26}$</td>
<td>1.19×10$^{-26}$</td>
</tr>
<tr>
<td>Gate-Oxide Capacitance</td>
<td>$C_{OX}$</td>
<td>F/µm$^2$</td>
<td>4.5×10$^{-15}$</td>
<td>4.4×10$^{-15}$</td>
</tr>
</tbody>
</table>

2.4.1 Transfer Characteristics

Figure 2.7 shows the transfer characteristics for MOSFETs with $W=6$µm and $L=6$µm at $V_{DS}=0.1$V. The measured curve represents the mean for ten MOSFETs having the same above dimensions. Four of those MOSFETs are of the 1st group at the left edge of the chip “block 1”, the other two are of the 2nd group “block 3” in middle of the chip. The last four MOSFETs are of 3rd group at the right side of the chip “block 10”. The
mismatch in weak inversion is calculated as the standard deviation of results from those ten curves and found equal to 2.5%.

Figure 2.7 Measured and simulated transfer characteristic for MOSFETs with \(W=6\mu m\), \(L=6\mu m\) and at \(V_{DS}=0.1V\)

The measured curve shown below in Figure 2.8 represents the mean curve of the ten MOSFETs in the three groups mentioned above but with different dimensions of \(W=30\mu m\) and \(L=6\mu m\) at \(V_{DS}=0.1V\). The mismatch in the weak inversion region in this case is 2%.
Transfer characteristics of Figures 2.7 and 2.8 are plotted in the same graphs with their simulation counterparts and show good agreement. However the mismatch percentage is expected to be very small between the simulated and measured curves in each Figure.

2.4.2 Sub-threshold swing

The sub-threshold slope is the slope of the current, $I_{DS}$ in the logarithmic scale versus the gate-source voltage, $V_{GS}$. The inverse of the sub-threshold slope called the sub-threshold swing, $S$. It shows the required reduction in $V_{GS}$ value which in turn reduces the sub-threshold current, $I_{DS}$ by one order of magnitude. So, its unit is mV/decade. It is calculated as in equations (2.28) [2.6] and (2.29) [2.9] below
According to equation (2.29) above, the ideal value of \( \kappa \) is 1 so that the optimal value of \( S \) is 60mV/decade. A small \( S \) value implies low threshold voltage for the same value of the sub-threshold leakage current. For bulk MOSFETs, \( \kappa \) does not reach 1 but for fully depleted (FD) silicon-on-insulator (SOI) MOSFETs [2.10], it may approach to 1. The values of \( S \) for simulated and measured curves are calculated using equation (2.28) since its required variables are obtained directly from Figures 2.7 and 2.8. The error between simulated and measured results is also calculated using the following relation in equation (2.30). Table 2.2 below shows the \( S \) values for both Figures with the error found between simulated and measured results.

\[
S = \frac{dV_{GS}}{d\left(\log I_{DS}\right)} \quad (2.28)
\]
\[
S = \frac{U_T}{\kappa} \ln(10) \quad (2.29)
\]

\[
Error = \frac{|Simulation \ results - Measured \ results|}{Simulation \ results} \times 100\% \quad (2.30)
\]

Table 2.2: \( S \) values for Figures 2.7 and 2.8 with the error

| Figure number | \( S \) (mV/decade) | \( S \) (mV/decade) | Error in \( S \) (
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2.7</td>
<td>80</td>
<td>81.5</td>
<td>1.875</td>
</tr>
<tr>
<td>2.8</td>
<td>80</td>
<td>81</td>
<td>1.25</td>
</tr>
</tbody>
</table>
From Table 2.2 above, it is obvious that $S$ simulated value represents the typical value for bulk MOSFET at room temperature. The measured $S$ values are close to the typical values in both Figures which results in small error.

From equation (2.29) above, $\kappa$ values for the simulation and experimental cases are calculated in Table 2.3 below utilising $S$ values in Table 2.2 above.

Table 2.3: $\kappa$ values for Figures 2.7 and 2.8 with the error

<table>
<thead>
<tr>
<th>Figure number</th>
<th>$\kappa$ Simulated (mV/decade)</th>
<th>$\kappa$ Measured (mV/decade)</th>
<th>Error in $\kappa$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.7</td>
<td>0.748</td>
<td>0.734</td>
<td>1.87</td>
</tr>
<tr>
<td>2.8</td>
<td>0.748</td>
<td>0.74</td>
<td>1.06</td>
</tr>
</tbody>
</table>

The threshold voltage, $V_{TH}$ of the measured curve of Figure 2.7 which represents the mean threshold of the ten MOSFETs is obtained. The same exercise is repeated for the measured curve of Figure 2.8. Table 2.4 below shows the threshold voltages of the measured curves of Figures 2.7 and 2.8 with the error compared with parameter used in simulation.

Table 2.4: Threshold voltage for Figures 2.7 and 2.8 with the error

<table>
<thead>
<tr>
<th>Figure number</th>
<th>$V_{TH}$ Simulated (mV)</th>
<th>$V_{TH}$ Measured (mV)</th>
<th>Error in $V_{TH}$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.7</td>
<td>490</td>
<td>499</td>
<td>1.83</td>
</tr>
<tr>
<td>2.8</td>
<td>490</td>
<td>496</td>
<td>1.22</td>
</tr>
</tbody>
</table>
2.5 Conclusion

In this chapter the operation of the MOSFET in both strong and weak inversion regions is presented and discussed. The derivations of the current-voltage equations are mentioned. The test chip which contains the proposed circuits in this work is introduced. The measurements for MOSFETs were made from both sides and the middle of the chip, and a good agreement indicates a small degree of variability across the wafer. The experimental transfer characteristics for those MOSFETs show small mismatch. Also the mismatch between the experimentally measured and transfer characteristics simulated with nominal values from the AMS foundry was very low. The inverse of the sub-threshold slope parameter, $S$ values were obtained for simulated and measured curves. The calculations show $S$ measured values in good agreement with those of simulation. The variation between the threshold voltages of experimental and simulation results is obtained. The good match between MOSFETs simulated and measured features explains the low error percentages in $S$ values which confirm that match. Thus, the comparable simulated and measured results for the proposed OTA and OTA-C filters in later chapters can be considered as a result of this match in MOSFETs features.

References


CHAPTER TWO

MOSFET in Sub-threshold Regime


CHAPTER THREE

OTA Linearization Techniques and the Proposed OTA

3.1 Introduction

The CMOS operational transconductance amplifier, OTA represents the main building block for many analogue VLSI systems. It consists of MOSFETs which are essentially, voltage-controlled current source devices and can be considered as having inherently, transconductance characteristics. The commonly used OTA configuration is that with differential input voltage with a single or differential output current that can be easily controlled by controlling its bias current.

3.2 The simple OTA

The simple OTA shown in Figure 3.1 consists of five MOSFETs in a differential configuration. Two input MOSFETs M1 and M2 share equally the current of the bias MOSFET “current sink MOSFET” represented by the current source \( I_B \). Finally there are the two current mirrors MOSFETs M3 and M4 that perform the subtraction of currents to create the output current, \( I_{\text{out}} \) [3.1] as follows

\[
I_{\text{out}} = I_B \tanh \left( \frac{kV_d}{2U_T} \right)
\]  

(3.1)
where $I_B$ and $V_d$, are the OTA bias current and the differential input voltage which equals $(V_{in1}-V_{in2})$ where $V_{in1}$ and $V_{in2}$ are the non-inverting and inverting input terminals. The differential operation offers the advantages of rejection of common-mode signals and of cancellation of the noise from the bias current MOSFET.

![Figure 3.1 Simple OTA.](image)

A disadvantage of the simple differential OTA is represented by its limited input linear range [3.2] which causes the OTA output current to be saturated by small differential input voltage. This arises due to the exponential current-voltage relationship in MOSFETs when operating in the sub-threshold regime mentioned in chapter two. From chapter two in equation (2.23) below, the MOSFET transconductance, $g_m$ is as follows

$$g_m = \frac{\kappa \beta}{U_T}$$
In the sub-threshold regime, the transconductance is a function of the MOSFET drain current, $I_D$ and its sub-threshold coupling coefficient, $\kappa$. From equation (2.23) which repeated above, it can be concluded that in sub-threshold regime, the value of $g_m$ is known once the current, $I_D$ is known. It is easy to show that the transconductance, $G_m$ of the simple OTA of Figure 3.1 is as follows

$$G_m = \frac{\partial I_{out}}{\partial V_d} = \frac{\kappa I_B}{2U_T}$$

(3.2)

It is worth noting that the input linear range of the simple OTA is $\sim \pm 6mV$. It can be seen that the MOSFET and the simple OTA transconductances are the same since the MOSFET drain-source current, $I_{DS}$ has half the value of the bias current, $I_B$ of the OTA. The OTA transition frequency, $f_T$ which represents the bandwidth of the OTA can be expressed as

$$f_T = \frac{1}{2\pi r_{out}C_L}$$

(3.3)

where $r_{out}$, $C_L$ are the total OTA effective small-signal load resistance and capacitance at the OTA output node. The resistance $r_{out}$ is expressed as follows

$$r_{out} = \frac{1}{g_{ds2} + g_{ds4}}$$

(3.4)

where $g_{ds2}$ and $g_{ds4}$ are the drain-source conductances of the OTA MOSFETs M2 and M4 respectively.

### 3.3 Techniques to increase the OTA linear range

A number of techniques had been proposed to increase the OTA input linear range. Some of these techniques are summarised below and involve either widening the
tanh function of Eqn. 3.1, or decreasing the ratio of transconductance to bias current to give a wider linear range.

3.3.1 Source Degeneration Technique

The technique of source degeneration is well known, and was first used in vacuum-tube design; it was then referred to as cathode degeneration, and was described in [3.3]. Later, it was used in bipolar amplifier design, where it is referred to as emitter degeneration. The idea behind source degeneration is to convert the current flowing through a MOS transistor into a voltage through a resistor or diode (or diode-connected transistors), and then to feed this voltage back to the source of the transistor to decrease its current. Figure 3.2 shows four different techniques where source degradation is used to improve linearity. The simplest technique is to include a resistor between the two legs of a simple differential pair as shown in Figure 3.2 a. This technique effectively reduces current in the differential pair M1 and M2 by reducing the differential input voltage. Then the OTA transconductance \( g_m \) is reduced to an effective transconductance, \( g_{m\text{effective}} \) as follows

\[
g_{m\text{effective}} = \frac{g_m}{1 + g_m R}
\]

where \( R \) is the resistor of Figure 3.2 and needs to have a large value compared to \( 1/g_m \) so as to reduce \( g_{m\text{effective}} \).

Figure 3.2 (b and c) show the 2\(^{\text{nd}}\) and 3\(^{\text{rd}}\) techniques which also use source degradation with a transistor \( M_{SD5} \) or two transistors \( M_{SD5} \) and \( M_{SD6} \) to act as single or double so-called ‘diffussors’ respectively. The diffussor conductivity in Figure 3.2 b is governed by both the potential \( V_{GC} \) and \( m \) for the single diffussor, \( M_{SD5} \). On the other hand, the conductivity of the double diffussor is set by \( m \) only. The factor \( m \) represents the ratio of diffussor MOSFET “single diffusor” or MOSFETs “double diffusors” aspect
ratio to that of the differential MOSFETs. The linear range is increased by 8 fold and 4 fold for \( m \) values of 0.25 and 0.5 for single and double diffusors respectively [3.4]. This increase is obtained by setting the 2\(^\text{nd}\) derivative of their output current equations shown below to be equal to zero. [3.5], [3.6]

\[
I_{out} = I_g \left( \frac{kV_d}{2U_T} - \tanh^{-1} \left( \frac{1}{4m+1} \tanh \left( \frac{kV_d}{2U_T} \right) \right) \right) \quad (3.6)
\]

\[
I_{out} = I_g \left( \frac{kV_d}{2U_T} - \tanh^{-1} \left( \frac{\sinh \left( \frac{kV_d}{2U_T} \right)}{2m + \cosh \left( \frac{kV_d}{2U_T} \right)} \right) \right) \quad (3.7)
\]

However the disadvantage of the single diffusor technique is represented by the need to incorporate additional circuitry to get an input signal level to be around \( V_{GC} \).
CHAPTER THREE  OTA Linearisation Techniques and the Proposed OTA

LOW POWER ELECTRONIC CIRCUITS FOR BIOMEDICAL APPLICATIONS  Saad A. Hasan
Figure 3.2 Source degradation linearization techniques for the simple differential OTA; (a) Single resistor diffuser; (b) single MOSFET diffuser; (c) double MOSFETs diffusers; (d) diode connected MOSFETs.

Figure 3.2 d shows the 4th source degeneration technique. It is represents simple OTA differential pair with a diode connected source degradation transistor in each of its two branches. The diode connected transistor has the effect of reducing the transconductance by decreasing $\kappa_e$, the effective value of electrostatic coupling coefficient “ratio” between the gate and channel as mentioned earlier in chapter one [1.28]. Hence, $\kappa$ shifted by substrate bias and given as follows

$$I_{out} = I_B \tanh \left( \frac{\kappa_e V_d}{2U_T} \right)$$  \hspace{1cm} (3.8)
As shown in equation (3.9), by using two source degeneration diode-connected transistors, \( M_{SD5} \) and \( M_{SD6} \), placed as one transistor per branch, \( \kappa_e \) is decreased and the linear range of the OTA becomes more than double that of the simple OTA. If the number of diode-connected transistors is increased to four (two transistors per side), the linear range will be increased by more than four times that of the simple OTA. The price is the necessary increase in the minimum supply voltage and a decrease of the common-mode operating range because \( M_{SD5} \) and \( M_{SD6} \) add an additional series voltage drop between the differential pair \( M_1 \) and \( M_2 \) and the current sink, \( I_B \). In addition, there is an increase in thermal intrinsic noise as a result of increasing the number of noise sources, represented by \( M_{SD5} \) and \( M_{SD6} \).

### 3.3.2 Bumping MOSFETs Technique

Bumping is a technique for linearising the tanh function that presented in equation (3.1) and hence extending the linear range of a sub-threshold differential pair [3.8].

As shown in Figure 3.3 below, a bump differential OTA consists of three legs: two outer legs represent the simple differential pair of \( M_1 \) and \( M_2 \). A middle leg containing two series connected transistors \( M_{B5} \) and \( M_{B6} \), operate as a simple current correlator to the circuit [3.9].

The current through the transistors in the middle leg is a bump-shaped function of the differential voltage, \( V_d \) centred around the origin. Thus, the differential output
current $I_{out}$ from the outer two legs, is the usual tanh like function of the differential input voltage $V_d$ except for a region near the origin as in equation (3.1), where the bump transistors are in conduction and they steal current, such that they take a bump current away from the tanh like current function of the differential pair outer legs. It can be shown that the current flowing through the bump transistors is represented as in equation (3.10) [3.9] below

$$
I_{bump} = \frac{I_B}{1 + \frac{4}{St} \cosh^2 \left( \frac{\kappa V_d}{2U_r} \right)}
$$

(3.10)

Figure 3.3 Simple OTA with bumping MOSFETs technique of linearisation.

The bump transistors have no detrimental effect on the power consumption or supply voltage required since they only add two transistors in series, and the currents in
the outer leg and central bump transistors sum to $I_B$. The strength, $St$ is the ratio of $W/L$ of the bump transistors $M_{B5}$ and $M_{B6}$ to that of $M1$ and $M2$ in the outer legs as in equation (3.11) below

$$St = \frac{(W/L)_{bump}}{(W/L)_{diff.-pair}}$$ (3.11)

Hence, by controlling $St$, the properties of the OTA $I_{out}$-$V_d$ curve can be controlled. From equation (3.10) above, the effect of the bump transistors on the overall OTA output current can be computed as follows

$$I_{out} = \frac{I_B \tanh \left( \frac{\kappa V_d}{2U_T} \right)}{1 + \frac{St}{4} \sec^2 \left( \frac{\kappa V_d}{2U_T} \right)} = \frac{\sinh x}{\beta + \cosh x}$$ (3.12)

where

$$\beta = 1 + \frac{St}{2} \quad \text{and} \quad x = \frac{\kappa V_d}{U_T}$$

A small $St$ does not significantly affect the OTA transfer characteristics and the "$I_{out}$-$V_d$ curve" and it essentially remains unchanged. A large $St$ will cause a flat zone near the origin. At intermediate values of $St$, the OTA expansive properties of its $I_{out}$-$V_d$ curve due to the bump compete with its compressive properties due to tanh. To obtain a curve which is more linear than a tanh, the 2nd derivative of equation (3.12) is obtained and set to zero. The result represents the point of inflection which is at $St = 2$, resulting in the maximally flat $I_{out}$-$V_d$ curve at that point. The Taylor expansion of the output current of the simple OTA is given as equation (3.13) while that of equation (3.12) after putting bumping MOSFETs is in equation (3.14). It is obvious that equation (3.14) does not contain a cubic distortion term [3.9]. The linearised function in equation (3.14) has a 5th harmonic distortion term much less than that of equation (3.13). Bump linearisation
is a particularly useful technique because it increases the linear range of an OTA without increasing its noise, since the transistors do not sit in the signal path.

\[
\tanh \frac{x}{2} = x - \frac{x^3}{24} + \frac{2x^5}{240} - \frac{17x^7}{40320} + \cdots \quad (3.13)
\]

\[
\sinh \frac{x}{2 + \cosh x} = x - \frac{x^5}{3} + \frac{x^7}{540} - \frac{x^9}{4536} + \frac{x^{11}}{77760} + \cdots \quad (3.14)
\]

### 3.3.3 Capacitor Attenuation Technique

This basic idea of attenuation is summarised by the placement of a voltage divider at the OTA inputs to scale down the input voltage by a certain amount known as the attenuation ratio. Figure 3.4 shows a simple OTA with capacitive dividers represented by \((C_{11}/C_{12})\) and \((C_{21}/C_{22})\), connected to the non-inverting and inverting terminals respectively. The capacitors serve to reduce the OTA transconductance by the amount referred to as the attenuation ratio, and increase the linear range of the OTA by that amount. In general, explicit capacitors can be used; an alternative is to employ a multiple input, floating gate MOSFET. For the OTA constructed from floating gate MOSFETs, the use of multiple input floating gate MIFG MOS transistor to increase the transconductor linear range is feasible [3.10]. The MIFG MOSFET circuit provides natural attenuation as a result of voltage division at its floating gate. Since the floating-gate voltage of the MOS transistor is induced by multiple input voltages via double-poly capacitors, the attenuation ratio and in turn the increase in the linear range can be controlled by controlling the ratio of the capacitive divider [3.11].

However, there are some difficulties in this case which need additional care in design and fabrication [3.12], [3.13]. They can be summarised as the follows.
1. Effects of parasitic capacitances created between the MOSFET floating gate and its four terminals. Also greater difficulty in alignment; errors due to geometric and process parameter variation that may affect the capacitive ratio.

2. Effect of charge trapping in the floating gate that would induce an offset error on the output current, requiring special techniques for removing it.

The linear range is increased by using the MOSFET bulk terminal as input. This technique is known as bulk-driven technique. It can be thought as an implicit capacitive divider since the gate, surface potential, and bulk of the MOSFET form three terminals of a capacitive divider. In this technique, the bulk is chosen as an input instead of the gate because the coupling ratio of the bulk to the surface potential of $1-\kappa$ is less than that of the gate represented by $\kappa$. As a result, the transconductance of the bulk input becomes less than that of the gate terminal. However, there are two main disadvantages in this
technique. The first one is the need to isolate the bulk terminals for all MOSFETs. The second disadvantage is represented by the limited transition frequency, \( f_T \) of the bulk-driven MOSFET due to its high capacitance compared to that of the gate-driven MOSFET \([3.14]\). This is less of a problem with the amplifiers operating in the audio range, of interest here. It is important to mention that there are other techniques that can be used to increase the linear range such as current division \([3.15]\), current cancellation \([3.16]\), and using multiple asymmetric differential pairs \([3.17]\). These techniques all require additional circuitry which compromises the footprint of the amplifier design making them undesirable for the applications considered here.

### 3.4 A Review of Approaches to increase the Linear Range of OTA

A review of some of the aforementioned approaches used to increase the linear range of the CMOS OTA reported in the literature, is summarized below:

Fried et al in 1996 \([3.7]\) proposed a technique for extending the linear range of transconductors based on combining properly ratioed sub-threshold MOSFET differential pairs in parallel. This is accomplished through the use of the bulk terminal as an active terminal. This extends the linear range of the transconductors by a factor close to 2. The linear range is increased to 250mV\(_{pp}\) with the use of four parallel differential pairs.

Grech et al in 2005 \([3.18]\) proposed an OTA architecture with a novel bulk-input differential pair using 0.7V supply. A tunable, wideband and compact designs with a linear range of \(\pm 350\)mV was achieved. Two CMOS process were investigated for the proposed OTA represented by 0.8 \(\mu\)m and 0.35 \(\mu\)m with threshold voltages of 0.7V and 0.5V respectively. The OTA total current was governed by the gate terminal via a dummy pair. The OTA implemented using the 0.8 \(\mu\)m process, was used to implement a 2\(^{nd}\) order low-pass Gm-C filter for cochlear applications.
Hasler et al in 2006 [3.19] adopted the source degeneration and bump linearization techniques to increase the linear input range of an OTA constructed from Fully Depleted Silicon-On-Insulator (FD SOI) MOSFETS, used for hearing aids application. An increase of the linear input range by a factor of 10 (from $12\text{mV}_{pp}$ to $120\text{mV}_{pp}$) compared with the simple OTA was established, whilst operating at a low voltage and low current. With the increase in linearity, there was a trade-off between transconductance bandwidth and noise. However for hearing aid applications, the need to operate only at low frequency means that bandwidth was not considered a significant issue. Simulations showed that use of the OTA within a first order $G_m-C$ filter operating on $\pm 1.5\text{V}$ could improve linearization of the dynamic range by up to 8dB.

C. D. Christopher in 2006 [3.1] proposed a wide linear range transconductance with a high linear range of $\pm0.9\text{V}$ compared to $\pm75\text{mV}$ for the simple OTA. The explicit capacitor attenuation technique was used for this purpose. A wide linear range OTA was used to construct a cascaded differential attenuation filter to further increase the linear range, to $1.414\text{V}_{rms}$. The OTA-C band-pass filter operating in the sub-threshold regime showed an experimental dynamic range of 60.8 dB using a supply voltage of 2.8V.

### 3.5 The Proposed OTA

Figure 3.5 shows the proposed OTA. It comprises of a simple differential OTA circuit with bumping MOSFETs and capacitor attenuators. The bumping MOSFETs M5 and M6 are connected in series to each other and across the OTA rails. The linear range is increased more than 4 fold with ideally, no noise cost. The capacitor attenuators are represented by $(C_{11}/C_{12})$ and $(C_{21}/C_{22})$, connected to non-inverting and inverting OTA terminals respectively. They represent explicit capacitive dividers which allows for simple scaling of the attenuation ratio to adjust the linear range. Therefore, it is an improvement compared to implicit attenuation of bulk-driven input technique. The
capacitive divider ratio in the latter case is determined by the physical parameters of the process, and is intrinsically non-linear due to the dependence on parasitic depletion capacitances of the MOSFET. Thus the divider ratio cannot be controlled independently.

![Proposed OTA](image)

**Figure 3.5 Proposed OTA**

Also, the explicit capacitive divider is a passive element and linear for small signals which means that the attenuation does not introduce harmonic distortion. The capacitor attenuation ratio, \( a \), is represented by the following equation

\[
a = \frac{C_1}{C_1 + C_2} = \frac{1}{r + 1}
\]  

(3.15)
where \( r = C_2 / C_1 \), the number of times that \( C_2 \) is bigger than \( C_1 \). Consequently the effective value of the OTA transconductance, \( G_{m\text{ effective}} \) using capacitor attenuators [3.18], [3.20] will be as in equation (3.16)

\[
G_{m\text{ effective}} = aG_m
\]  

(3.16)

As a consequence, the input linear range is increased by a factor of \( a^4 \). The capacitor values of the proposed OTA are \( C_{11} = C_{12} = 0.5\, \text{pF} \) and \( C_{21} = C_{22} = 7.5\, \text{pF} \). So, the increase in linear range with these capacitor values is 16 fold. The proposed OTA with the combination of both bump linearization and capacitor attenuation together for the first time, offers a simple OTA structure with a minimum number of MOSFETs stacked between its rails. The supply voltages \( V_{DD} \) and \( V_{SS} \) are +1.5V and -1.5V respectively. It will be shown later, that the input linear range of this design is ±900mV at \( THD < 5\% \).

3.6 MOSFET Sizing

Recently two approaches have become widely used as unified synthesis methodologies valid in all regions of operation for determining MOSFET sizing and are now described. The new approaches are based on analysis rather than tool-based synthesis related with the conventional analogue design methods which require complicated synthesis tools, SPICE like and simulators models, analytical or quick hand methods for analogue circuits synthesise.

3.6.1 The \( g_m / I_D \) methodology

The \( g_m/I_D \) method for designing micro-power CMOS analogue circuits is proposed in [3.21] and valid for all regions of operation of the MOSFET. Here \( g_m \) stands for transconductance of the MOSFET and \( I_D \) its drain current. The normalized current \( I_N \)
is defined as the ratio of the MOSFET drain current to its aspect ratio. Therefore, the normalized current is given by

\[ I_N = \frac{I_D}{(W/L)} \]  

(3.17)

Both \( g_m/I_D \) and \( I_N \) are independent of the transistor sizes, therefore the relation between the two is unique for all transistors of the same type for a given fabrication technology. It is worth noting that the validation of this methodology is evident for long-channels for \( L \) values in the range of (3-12) \( \mu m \), while some revision is needed for short channel transistors [3.21]. The \( g_m/I_D \) versus \( I_N \) relationship can be obtained either by using transistor model equations or by experimentation. In the experimental case, the \( g_m/I_D \) versus \( I_N \) curves for many transistors needs to be obtained. Consequently, their mean \( g_m/I_D \) versus \( I_N \) curve used to consider the technology spreads [3.22].

The plot of the \( g_m/I_D \) ratio versus the normalized current, \( I_N \) is used to calculate MOSFET aspect ratios, \( W/L \). Then by choosing the suitable length which represents the compromise between the transistor area and stability on the one hand and dc gain on the other hand, the MOSFET width, \( W \) can be found [3.23].

The \( g_m/I_D \) ratio in that plot is chosen according to the required region of operation of the MOSFET. After making a projection of \( g_m/I_D \) on that plot, the normalised current is obtained. In other words for the given values for any two of \( g_m/I_D \), \( g_m \), \( I_D \) variables; \( W/L \) is determined directly. Finally, equation (3.17) is used to find \( W/L \) since the required value of \( I_D \) is known. The \( g_m/I_D \) versus \( I_D/(W/L) \) curve is obtained and shown in section 3.7 later. The total supply current is chosen and the drain of each transistor can then be found. Using the value of \( I_D \) with an appropriate value of \( g_m/I_D \) based upon the desired operating regime of the transistor, allows the \( W/L \) ratio to be determined. Therefore the primary variables in the synthesis process are the drain currents of each transistor and their preferred \( g_m/I_D \) ratios. The maximum value of \( g_m/I_D \)
OTA Linearisation Techniques and the Proposed OTA

is limited firstly, by the weak inversion maximum value of the technology (about 35\text{V}\text{r} in thin film fully-depleted SO1 MOS transistors and less than 30\text{V}\text{r} in bulk MOS transistors) and secondly, by the stability requirements because as \(g_m/I_D\) increases, with fixed current, \(I_D\) the transistor sizes and parasitic capacitances are increased and the phase margin is reduced [3.21]. It is important to mention that this methodology is adopted when sizing the MOSFETs in this work. The table containing the dimensions of the MOSFETs for the proposed OTA will be presented in the later sections. The MOSFETs dimensions are calculated by considering all MOSFETs to be operating in the weak inversion region.

**3.6.2 The Inversion Coefficient Approach**

This methodology is proposed in [3.24] and is based on the concept of ‘level of inversion’. When the level of inversion is known, it can be used as the design variable for optimising circuit parameters [3.24], [3.25]. The design degree of freedom in this method is three, represented by the drain current \(I_D\), transistor length \(L\), and so-called inversion coefficient, \(IC\). The EKV MOS model is the most appropriate model to work with this approach. This model is continuous and valid in all regions of MOS operation, and can be used for correlating the three degrees of freedom. The inversion coefficient, \(IC\) can be expressed as follows

\[
IC = \frac{I_D}{2n\mu_0C_{OX}(W/L)U_T^2} = \frac{I_D}{2nk_0(W/L)U_T^2}
\]

(3.18)

where \(\mu_0\) is the low-field mobility and \(k_0=\mu_0C_{OX}\). Hence, \(IC\) is as follows

\[
IC = \frac{I_D}{I_0(W/L)}
\]

(3.19)

where \(I_0\) is a process dependent current equals to \(2nk_0U_T^2\). The most convenient method for interpreting the inversion coefficient is by making use of the \(g_m/I_D\) ratio.
3.7 Simulation Results

3.7.1 OTA MOSFETs sizing utilising $g_{m}/I_D$ methodology

The simulations were conducted in the Cadence environment, using circuit simulator, SpectreS with BSIM3v3.1 models and parameters from the AMS process for 0.35µm CMOS C35 Technology. According to $g_{m}/I_D$ methodology, the MOSFET dimensions are obtained after specifying the operation regime on the $g_{m}/I_D$ versus $I_D/(W/L)$ curve. For the proposed OTA, all its MOSFETs are operated in the sub-threshold regime which is represented by high $g_{m}/I_D$ values on the $g_{m}/I_D$ versus $I_D/(W/L)$ curve. The $g_{m}/I_D$ versus $I_D/(W/L)$ curve can not be obtained directly. In this work it is obtained by simulation using both transfer characteristics and $g_{m}/I_D$ versus $V_{GS}$ curves for the NMOS and PMOS transistors. For the $g_{m}/I_D$ versus $V_{GS}$ curve, its x-axis represented by $V_{GS}$ is exchanged with its corresponding $I_D$ values from the transfer characteristics curve. In this way, the $g_{m}/I_D$ versus $I_D$ curve is obtained. It should be remembered that the x-axis should represent the normalised values of $I_D$. This implies the need to divide by the MOSFET aspect ratio, $W/L$ used in obtaining its transfer characteristics unless it equals 1. Hence, the $g_{m}/I_D$ versus $I_D/(W/L)$ curve is obtained. Figure 3.6 below shows these curves and also the final $g_{m}/I_D$ versus $I_D/(W/L)$ curves for both NMOS and PMOS transistors put in the same graph. Table 3.1 below presents the MOSFETs $g_{m}/I_D$ values chosen for the required sub-threshold operation with their appropriate drain current, $I_D$ length, $L$ and width, $W$ values.
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![Graph a](image1)

![Graph b](image2)

1. Source-Gate Voltage $V_{GS}$ (V)
2. Drain Current $I_D$ (A)
3. $g_m/I_D$ (mho/A)
4. $g_m/I_D$ (mho/A)

(a) and (b) represent the characteristics of NMOSFETs.
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LOW POWER ELECTRONIC CIRCUITS FOR BIOMEDICAL APPLICATIONS  
Saad A. Hasan
Figure 3.6 $g_m/I_D$ versus $I_D/(W/L)$ curve; (a) NMOSFET transfer characteristics, (b) $g_m/I_D$ versus $V_{GS}$ curve for NMOSFET, (c) PMOSFET transfer characteristics, (d) $g_m/I_D$ versus $V_{GS}$ curve for PMOSFET, (e) $g_m/I_D$ versus $I_D/(W/L)$ curves for NMOS and PMOS transistors

Table 3.1: The dimensions of MOSFETs of the proposed OTA

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>$g_m/I_D$ $(V^{-1})$</th>
<th>$I_D$ (nA)</th>
<th>$W/L$</th>
<th>$W$ (µm)</th>
<th>$L$ (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>27</td>
<td>80</td>
<td>2.5</td>
<td>15</td>
<td>6</td>
</tr>
<tr>
<td>M3, M4</td>
<td>23</td>
<td>80</td>
<td>2.5</td>
<td>15</td>
<td>6</td>
</tr>
<tr>
<td>M5, M6</td>
<td>27.2</td>
<td>80</td>
<td>5</td>
<td>30</td>
<td>6</td>
</tr>
<tr>
<td>M7</td>
<td>26</td>
<td>240</td>
<td>5</td>
<td>30</td>
<td>6</td>
</tr>
</tbody>
</table>
3.7.2 OTA transfer characteristics and $G_m$ curve

Simulation is made for both simple OTA and OTA with bumping to get the currents distribution in them. Figure 3.7 shows the distribution of the normalised currents in the simple OTA. The contribution of the current $I_{M2}$ that passes through M2 transistor in the value of output current, $I_{out}$ for negative $V_d$ values is clear. This contribution reduces as $V_d$ increases. The same thing is repeated for the current $I_{M1}$ which passes through M1 transistor for positive $V_d$ values. This contribution reduces when $V_d$ decreases. At the origin point of $V_d$ the contribution of currents $I_{M1}$ and $I_{M2}$ is the same. This means that as $V_d$ value equals zero, half of output current, $I_{out}$ value is due to $I_{M1}$ and the other half is due to $I_{M2}$.

Figure 3.7 Normalised currents distribution in the simple OTA
Figure 3.8 below shows the distribution of normalised currents in the OTA with bumping MOSFETs. For Figure 3.8, the contribution of \( I_{M1} \) and \( I_{M2} \) is relatively the same when \( V_d \) value is far away from the origin. Near the origin, the influence of bumping current, \( I_{Bump} \) due to bumping MOSFETs becomes clear as discussed earlier in section 3.3.2. As \( V_d \) value equals zero, a maximum contribution of bumping MOSFETs takes place. The contribution of the currents in each one of the three arms is the same in the value of output current, \( I_{out} \). This means that at zero \( V_d \), \( I_{M1} \), \( I_{M2} \), and \( I_{Bump} \) are equal and each one of them is one third the output current, \( I_{out} \). The slope of the output current \( I_{out} \) curve in its linear region in Figure 3.8 is less than that of the simple OTA of Figure 3.7. This is due to bumping MOSFETs effect that makes that slope which represents its transconductance 2/3 times that of the simple OTA.

Figure 3.8 Normalised currents distribution in OTA with bumping MOSFETs with aspect ratio of bumping MOSFETs double that of input MOSFETs
Figure 3.9 presents the transfer characteristics of the simple, bumped, and proposed OTAs. The effect of the linearisation techniques used is obvious in preventing the proposed OTA output current from becoming saturated even at differential input voltages of about ±1V.

![Graph: Transfer characteristics of simple, bumped, and the proposed OTAs](image)

Figure 3.9 Transfer characteristics of simple, bumped, and the proposed OTAs

The $Gm$ curves for the simple, bumped, and proposed OTAs are shown in Figure 3.10 below.
Figure 3.10 Normalised $G_m$ versus $V_d$ curves representing the input linear range of the simple, bumped, and the proposed OTAs.

According to simulations, the bias current, $I_B$ range of the proposed OTA is shown in Table 3.2 below. It corresponds to the indicated transition frequency, $f_T$ range for the two extremes of its linear region of operation represented by the ±900mV.

Table 3.2: The simulated $I_B$ and $f_T$ ranges of the proposed OTA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{Bmin}$</td>
<td>0.5</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{Bmax}$</td>
<td>570</td>
<td>nA</td>
</tr>
<tr>
<td>$f_{Tmin}$</td>
<td>5.3</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{Tmax}$</td>
<td>2.53</td>
<td>MHz</td>
</tr>
</tbody>
</table>
Table 3.3 shows the linear range obtained in this work compared with some prior work of other researchers mentioned in section 3.4 above.

Table 3.3: A comparison of OTA input linear range using different linearisation techniques

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technique</th>
<th>Supply Voltage (V)</th>
<th>Linear Range Before Linearisation</th>
<th>Linear Range After Linearisation</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3.7]</td>
<td>Source degeneration, SD of Fig. 3.2 (d)</td>
<td>-</td>
<td>≈ 24mV&lt;sub&gt;PP&lt;/sub&gt;</td>
<td>250mV&lt;sub&gt;PP&lt;/sub&gt; at THD &lt;1%</td>
</tr>
<tr>
<td>[3.18]</td>
<td>Bulk-driven Input</td>
<td>0.7</td>
<td>-</td>
<td>±350mV</td>
</tr>
<tr>
<td>[3.19]</td>
<td>SD of Fig. 3.2 (d) + Bumping MOSFETs</td>
<td>±1.5</td>
<td>12mV&lt;sub&gt;PP&lt;/sub&gt;</td>
<td>120mV&lt;sub&gt;PP&lt;/sub&gt; at THD &lt;1%</td>
</tr>
<tr>
<td>[3.1]</td>
<td>Capacitor attenuation</td>
<td>2.8</td>
<td>75mV</td>
<td>±900mV at THD &lt;5%</td>
</tr>
<tr>
<td>[This Work]</td>
<td>Bumping MOSFETs + Capacitor attenuation</td>
<td>±1.5</td>
<td>±6mV</td>
<td>±900mV at THD &lt;5%</td>
</tr>
</tbody>
</table>
The data in the table shows that the linear range obtained in this work is the largest one besides that of [3.1]. The proposed OTA has the largest linear range enhancement ratio among others.

3.8 Experimental Results

The proposed OTA is included on the test chip. The test chip shown in Figure 2.6 was fabricated in the AMS 0.35µm CMOS C35 technology process. The proposed OTA occupies an area of 30,360µm². The area of the capacitor attenuators is about 23,100µm² which constitutes 76% of total area of the OTA.

Figure 3.11 shows the measured and simulated transconductance, $G_m$ versus the differential input voltage, $V_d$ curve. The simulations were performed using nominal values of transistor parameters supplied by AMS. It is worth noting that the fall-off in the OTA transconductance is because of the influence of the transistors characteristics especially their nonlinearities. The measured input linear range of about ±950mV at $THD<5\%$, or at 0.95 of its normalised amplitude confirms the simulation results and is slightly larger than it.

In OTA-C filters, the nonlinearities can be explained sometimes due to the total harmonic distortion, $THD$. However in OTA-C filters, most of harmonics are supposed to be filtered. So, the $THD$ measure for expressing nonlinearities sometimes is not precise as for moderately nonlinear systems like square wave [3.1]. Besides, many systems saturate when they become nonlinear and that is explained due to a gain compression phenomenon. This is especially true for above-threshold systems with large input signals as discussed in depth in [3.26].
Figure 3.11 Simulated and measured input linear range of the proposed OTA.

Figure 3.12 below reflects that variation in transconductance value with the increase of the differential input voltage, $V_d$. It is obvious that when $V_d$ exceeds the OTA linear range, a large decrease in its $G_m$ value takes place due to rise of nonlinearity. It can also be seen below in Figure 3.12 that the measured input linear range of the proposed OTA is more than 950mV at a degradation percentage of 5% from its maximum value for $V_d$ range of (0-1)V.
Figure 3.12 The Measured variation percentage in the input linear range of the proposed OTA.

Table 3.4 below presents the bias current, $I_B$ and transition frequency, $f_T$ ranges for the proposed OTA within its measured linear region of ±950mV.

Table 3.4: The measured $I_B$ and $f_T$ ranges of the proposed OTA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{B\text{min}}$</td>
<td>0.5</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{B\text{max}}$</td>
<td>580</td>
<td>nA</td>
</tr>
<tr>
<td>$f_{T\text{min}}$</td>
<td>6.4</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{T\text{max}}$</td>
<td>2.56</td>
<td>MHz</td>
</tr>
</tbody>
</table>
Table 3.4 shows relatively larger linear bias current and transition frequency ranges compared to those obtained in simulation.

As it is essential to increase the input linear range of the OTA as discussed above, it is also important to decrease its noise. The transistors sizing is very important since it is related to the circuit area and performance including noise. The MOSFET dimensions must be increased appropriately to reduce flicker noise. The MOSFET sub-threshold operation brings the advantage of small input-referred white noise per unit bandwidth since it is the regime of highest $g_m/I_D$ values. The influence of noise on design will be discussed in the next chapter as it represents the other half of the story in low power applications. Therefore for a given power consumption, the sub-threshold operation offers the more efficient MOSFET operation in terms of its noise and bandwidth.

3.9 Conclusion

The upper input limit at which an OTA circuit operates properly without distortion is represented by its input linear range. Some of the most commonly used techniques to increase the OTA input linear range were presented and reviewed in this chapter. The proposed OTA in this work was then presented. It has a simple structure and a wide input linear range of ±900mV as a result of combining both bumping MOSFETs and capacitive attenuation techniques together for the first time. The two recent techniques used to describe the MOSFET behaviour in terms of modern analogue design including the MOSFETs size calculation are discussed. The $g_m/I_D$ methodology is adopted for the calculations of MOSFET dimensions, exploiting the unique relation between the MOSFET $g_m/I_D$ ratio and the normalised drain current, $I_D/(W/L)$. This approach provides an insight about a MOSFET-circuit performance during the design stage. Experimental results were shown to confirm the design approach and showed good agreement with those of simulation. Small discrepancies were explained by
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reference to the larger input linear range, linear current range, and transition frequency range.

References


CHAPTER FOUR

Noise in Integrated Circuits

4.1 Introduction

The word “noise” has an everyday use to refer for example to unwanted sound, but in electrical engineering it has a specific meaning. Electrical noise represents the unwanted current or voltage in an electrical circuit keeping in mind that real signals are a sum of this unwanted signal “noise” and the desired signal [4.1]. It is a limiting factor in system performance. It limits the minimum signal level that a circuit can handle with acceptable quality. Attention is taken to deal with the problem of noise because it constitutes a trade-off with power dissipation, linearity, and bandwidth.

The existence of noise is primarily due to the fact that electrical charge is not continuous but is carried in discrete amounts equal to the charge of an electron which leads to its association with the fundamental processes in the integrated circuit devices [4.2]. It is important to study noise since it represents a lower limit to the size of electrical signals which a circuit can process without significant deterioration in signal quality.

In integrated circuits, noise phenomena can be assumed to be the result of small current and voltage fluctuations that are generated within the devices themselves. Such noise can be considered as intrinsic noise. In this chapter, the extraneous pick-up of noise from external environment or sources which may cause problems for such low-voltage low-power analogue circuits will not be discussed since it is outside the scope of this study.
Unlike a deterministic process such as the output from a sine wave generator, noise can be defined as a random process and its instantaneous value in time domain cannot be predicted at any time when past values are known. Therefore noise should be observed for a long period of time and can then be represented in a statistical model. The model can be used to investigate other important noise properties rather than its instantaneous amplitude. One of the important properties of noise which can be predicted is its average power since most sources of noise in circuits exhibit a constant average power. For circuits consisting of more than one noise source, it is usually necessary to add the effect of all those sources to get the total noise contribution. This superposition is usually used for deterministic voltages and currents. In analysing random signals such as noise, basically the average noise power of two noise waveforms represents the average of their summation. The summation can either be the superposition of power if they are uncorrelated, such as noise produced by different noise sources like a resistor and a transistor, or the average of their resulting power. The latter adds another term represented by the correlation term of the two noise waveforms. This refers to the case of correlated noise sources [see Appendix A].

The average power concept becomes more exploitable when identified with the frequency content of noise. This is called the power spectral density, PSD which represents the amount of power which the signal carries at each frequency. PSD is a powerful tool for analysing the effect of noise in circuits as detailed in the next sections [4.3].

4.2 Types of noise

Two different types of noise can corrupt analogue signals processed by integrated circuits namely: device electronic noise and environmental noise. The latter refers to random disturbances that a circuit may acquire through the supply or ground lines or the
substrate. Such noise is out of the study scope as mentioned in the introduction. The device electronic noise is discussed below [4.3]

4.2.1 Thermal Noise

This type of noise appears in resistors due to the random motion of electrons in a conductor that appears as a fluctuation in voltage even when the average current value equals zero. It arises because the back and forth motion of electrons from the resistor to the metal wire has a zero net charge transfer, but during a short time duration, a net, non-zero current flow is probable. The thermal noise spectrum is proportional to absolute temperature. This noise is represented by a series voltage source $v_{n,\text{Thermal}}^2$ or a shunt current source $i_{n,\text{Thermal}}^2$ [4.2] as follows

\[
\overline{i_{n,\text{Thermal}}^2} = 4kTR\Delta f
\]  
\[
\overline{v_{n,\text{Thermal}}^2} = \frac{4kT}{R}\Delta f
\]

where the over line in current and voltage equations indicates average values

$k$ is the Boltzmann’s constant
$T$ is the absolute temperature
$R$ is the resistor value
$\Delta f$ is the frequency bandwidth of interest in the Hz unit.

In the MOSFET, thermal noise also appears. The most significant source of noise is that generated in channel. This noise can be modelled in long channel devices operating in the saturation regime, as a current source connected between drain and
source terminals that has a mean squared value of $\overline{i_{n,\text{Thermal}}^2}$ or as a voltage source $\overline{v_{n,\text{Thermal}}^2}$ connected in series to its gate as in Figure 4.1 with a mean squared values [4.4] as explained in equations (4.3) and (4.4) respectively.

![Diagram](a) (b)

**Figure 4.1** Thermal noise representation of the MOSFET, (a) Thermal noise current source (b) Thermal noise voltage source

\[
\overline{i_{n,\text{Thermal}}^2} = 4kT\gamma g_{ds0} \Delta f \tag{4.3}
\]

\[
\overline{v_{n,\text{Thermal}}^2} = \frac{4kT\gamma}{\kappa g_m} \Delta f \tag{4.4}
\]

where $g_{ds0}$, $\gamma$, and $g_m$ are channel conductance at zero electric field and a coefficient equal to $\frac{1}{2}$ and $\frac{2}{3}$ in the saturation region in sub-threshold and above-threshold regimes respectively for long channel MOSFETs, and the transconductance in the saturation region. For short channel MOSFETs, $\gamma$ may take larger values [4.4].

Thermal noise has a flat frequency spectrum along the frequency bandwidth of interest, $\Delta f$. Equations (4.3) and (4.4) show that MOSFETs operation at low temperature exhibits...
lower thermal noise in analogue circuits. This approach becomes more attractive with the observation that the charge carrier mobility in MOS devices increases at low temperatures [4.5]. The other thermal noise source is represented by MOSFET ohmic sections, especially the gate resistance. This additional thermal noise can be reduced by careful layout.

4.2.2 Shot Noise

The shot noise is mainly associated with a direct current flow. It results from discrete movement of charge across a potential barrier; it is present in diodes, bidirectional junction transistors, and MOSFETs. It is a mean square value [4.6] as follows,

\[ \overline{i^2_{\text{shot}}}(f) = 2qI_P \Delta f \]  (4.5)

where \( \overline{i^2_{\text{shot}}}(f) \) is the shot noise current source. For most practical electronic devices, equation (4.5) is accurate well into the gigahertz region [4.2]. This is because equation (4.5) is valid for frequencies to the inverse of the carrier transit time through the depletion region, which is extremely small.

Each shot noise and thermal noise source can be represented by a white noise power spectral density. This gives rise to the question of how to distinguish between them and how to calculate white noise in MOSFETs for the present case of the sub-threshold regime. It is interesting to note that the shot and thermal noise have long been considered the results of two distinct mechanisms, but there is evidence that they are not [4.6]. It can be shown theoretically and experimentally that the noise in MOSFETs operating in the sub-threshold regime is essentially the sum of shot-noise components from the forward and reverse currents which represent at the same time the total thermal...
4.2.3 Flicker Noise

This type of noise is found in all devices from different kinds of resistors to semiconductors. Because $1/f$ noise is well spread over the components, it is likely to be caused by a fundamental physical mechanism. Physics based MOSFET noise model is proposed in [4.7]. The model can predict the MOSFET noise features in sub-threshold, linear and saturation regions of operation. The commonly accepted explanation of the $1/f$ noise is based on carrier number fluctuation theory [4.8]. The noise primarily arises at the interface between the gate oxide and the silicon of MOSFET. Inside the gate oxide, specifically near the interface between the gate oxide and silicon substrate, there are energy states or “traps” due to impurities or oxygen vacancies. These traps randomly capture and release charge carriers from the MOSFET channel causing electronic fluctuations which constitutes such noise [4.2]. The oxide charge fluctuations dynamically change the surface potential which changes the MOSFET threshold voltage. For this reason, the flicker noise can also be considered as a result of dynamically varying threshold voltage [4.9]. It is called flicker noise because when it viewed in a light source, flickering is observed. Also it is denoted by pink noise (reddish color present in the lower range of visible spectrum) and $1/f$ noise (because of its inverse proportion to frequency). The existence of flicker noise can be also explained as a result of transistors mobility fluctuations as described in the Hooge model [4.10].

The average power of flicker noise cannot be predicted easily as it is highly dependent on processing and will show considerably variation from one CMOS technology to another. It is considered as a series connected voltage source, $\sqrt{2}v_{n_{1/f}}$ to the MOSFET gate and modeled [4.9] as follows
\[
\overline{\nu^2_{n,(1/f)}} = \frac{K_F}{C_{OX}WL} \frac{1}{f} \Delta f
\]

\(K_F, C_{OX}, W,\) and \(L\) are respectively the flicker noise constant which is process-dependent, the oxide capacitance per unit area, the channel width, and the channel length.

The inverse dependence of flicker noise on frequency shows clearly that this type of noise has a great effect at low frequency response. The flicker noise is also inversely proportional to MOSFET area, \(WL\) \([4.9]\) which should therefore be made large. This explains the reason for using MOSFET areas of several thousands of square microns in low-frequency application circuits. It is important to notice that in order to quantify the significance of \(1/f\) noise with respect to thermal noise for a certain device, both spectral densities of these noise sources should be plotted on the same axes as shown in Figure 4.2 below. This concept is known as flicker noise corner frequency, \(f_c\).

\[20 \log 20 \nu^2_{n,\text{corner}} \]

\(f_c\) (log scale)

**Figure 4.2 Concept of flicker noise corner frequency**
The corner frequency represents the intersection point in frequency axis at which both noise power spectral densities have same value. So, the corner frequency will be a measure of the part of frequency band that is mostly corrupted by flicker noise. It is desirable to minimize $f_c$ to realise MOSFETs with low corner frequencies. The flicker noise corner frequency, $f_c$, can be obtained as follows

$$\frac{4kT\gamma}{\kappa g_m} = \frac{K_F}{C_{ox}WL} \frac{1}{f_c}$$

$$f_c = \frac{K_F}{C_{ox}WL} \frac{\kappa g_m}{4kT\gamma}$$

(4.7)

From equation (4.7), $f_c$ mainly depends on device dimensions and drain current.

### 4.3 Representation of noise in circuits

The noise is estimated by setting the input to zero, then measuring the total noise at the output due to the various sources of noise in the circuit. The noise is always measured on the output of the circuit. The output-referred noise does not allow a fair comparison of the performance of different circuits since it depends on the gain. It can, however be referred back to the input of the circuit by dividing its value by the circuit gain for comparison with an input signal. The input-referred noise is not physically present which explains why it is impossible to calculate it directly or measure it at the input of a circuit. This is especially true for CMOS circuits where the input to a circuit may be the polysilicon gate of a MOSFET that is surrounded by an insulating dielectric. For a noisy circuit of any source impedance, the input-referred noise can be modelled as shown in Figure 4.3 below, by voltage and current sources connected respectively in series and parallel to the input of a noiseless circuit. So, for the case of a low input impedance circuit the noise current will have little effect on the circuit output which
makes the noise calculated at the output to be solely due to the noise voltage source. For a high input impedance circuit, the noise voltage source has little effect and the noise calculated at the output is solely from the noise current source [4.1].

![Figure 4.3 Representation of noise by voltage and current sources](image)

Both input-referred noise voltage and current sources can be calculated due to varying source impedances at the input terminal. Such a style of noise representation complicates calculations. It is difficult to track the correlations between both input-referred noise sources which are due to device noise in one transistor which may add additional terms as mentioned earlier in section 4.1.

### 4.4 Another strategy of noise representation

Another strategy depends on whether the input is a source impedance voltage input or a source admittance current input. As a consequence, the input referred voltage noise in series with source impedance voltage input or the input referred current noise in parallel with source admittance current input are calculated in accordance with the actual input. Hence, the possibility of correlation disappears in this strategy since there is only one input noise source.
In this strategy, superposition is used to calculate the noise power per unit bandwidth separately due to each noise source by suppressing the contribution of other sources each time. Then after calculating the power noise due to all noise sources separately, the products of their mean square noise sources and the squared noise transfer functions from their inputs to circuit output values are summed. The total output noise is obtained by integrating the output noise power over all frequencies. The output noise power can be referred back to the actual input by dividing its value by the magnitude of the squared transfer function from that input to the output. In this fashion, the source impedances effects are already taken into account automatically due computing the transfer functions from input to output, and any noise power due to the source impedance simply adds to the input-referred noise.

It is worth noting that this strategy considers that all noise sources from different devices in a circuit are independent and uncorrelated during calculations. This belongs to the assumption of small signal case where the net effect of all noise sources is still small enough such that the operating point of the circuit is not significantly affected [4.11]. In this work, the calculations of noise are made according to this strategy.

4.5 Noise for MOSFET and OTA

The noise relations for the MOSFETs and CMOS OTA are detailed in this section as follows:

4.5.1 Noise model for MOSFET

The total noise power mean squared value, $\overline{v_n^2}$, in the MOSFET is represented by summing the thermal noise $\overline{v_{n \text{Thermal}}^2}$ and the flicker noise $\overline{v_{n (1/f)}^2}$ as follows

$$\overline{v_n^2} = \overline{v_{n \text{Thermal}}^2} + \overline{v_{n (1/f)}^2}$$

$V^2 / Hz$
\[ \overline{v_n^2} = \frac{4kT\gamma}{\kappa g_m} \int_{f_L}^{f_H} df + \frac{K_F}{C_{ox}WL} \int_{f_L}^{f_H} \frac{1}{f} df = \frac{4kT\gamma}{\kappa g_m} (f_H - f_L) + \frac{K_F}{C_{ox}WL} \ln \left( \frac{f_H}{f_L} \right) \] (4.8)

where the term \((f_H - f_L)\) is the frequency bandwidth of interest, \(\Delta f\), since \(f_H\) and \(f_L\) are the highest and lowest frequencies of interest respectively. The RMS value of the MOSFET noise voltage, \(v_{n, RMS}\), is calculated as follows

\[ v_{n,RMS} = \sqrt{\overline{v_n^2}} = \sqrt{\frac{4kT\gamma}{\kappa g_m} (f_H - f_L) + \frac{K_F}{C_{ox}WL} \ln \left( \frac{f_H}{f_L} \right)} \] (4.9)

It can be concluded from equations (4.8) and (4.9) above, that the thermal noise can be reduced as \(g_m\) is increased. This means noise is reduced at the expense of increasing the bias current and hence increasing the power consumption. The price of reducing the flicker noise is paid by increasing MOSFET dimensions which means expending more area and by extension larger circuits.

**4.5.2 Noise in the simple OTA circuit depending on strategy of 4.3**

Figure 4.4 (a) shows the noise model of the simple OTA. The noise in each MOSFET is represented by its input noise voltage generator described by equation (4.8) above. The input-referred noise voltage \(\overline{v_{n,in}^2}\) for the simple OTA is indicated in equation (4.10) below and shown in Figure 4.4 (b).

\[ \overline{v_{n,in}^2} = \overline{v_n^2} + \overline{v_{m1}^2} + \left( \frac{g_m3}{g_{m1}} \right) \overline{v_{n3}^2} + \overline{v_{n4}^2} \] \[ V^2 / Hz \] (4.10)
Here it has been assumed that $g_{m1}=g_{m2}$ and $g_{m3}=g_{m4}$, where $g_{m1}$, $g_{m2}$, $g_{m3}$, and $g_{m4}$ are the transconductances of the OTA MOSFETs M1, M2, M3 and M4 respectively.

![Figure 4.4 Noise model of the simple OTA](image)

(a) Taking the equivalent sources for each MOSFET (b) The overall equivalent noise model for the simple OTA

From equation (4.10) it can be concluded that the input MOSFETs M1 and M2 contribute directly to the OTA noise while the contribution of mirror MOSFETs M3 and M4 is related by the square of their transconductance ratio to that of the input MOSFETs.

Assuming that: $v_{n1}^2 = v_{n2}^2$ and $v_{n3}^2 = v_{n4}^2$

Hence equation (4.10) is written as follows

$$
\tilde{v}_{n,m}^2 = 2v_{n1}^2 + \frac{g_{m3}}{g_{m1}} \left( \frac{v_{n3}^2}{v_{n1}^2} \right)^2 \frac{V^2}{Hz}
$$

Equation (4.11)
The importance of equation (4.11) in OTA design is represented by the ability to consider the input-referred thermal noise and the input referred $1/f$ noise separately to guide the choice of appropriate MOSFET sizing [4.2]. For above threshold operation, the MOSFET transconductance, $g_m$ is related to its dimensions besides its drain current. Therefore equation (4.11) can be rewritten to show the separated OTA thermal and flicker input-referred noise respectively as in equations (4.12) and (4.13).

$$
\bar{\sigma}^2_{v_n,(1/f)} = \frac{2K_n}{fW_iL_iC_{ox}} \left(1 + \frac{K_{fp}\mu_pL_n^2}{K_{fn}\mu_nL_3^2}\right)\Delta f
$$

(4.12)

where $K_{fp}$, $K_{fn}$ are the flicker noise coefficients in p-channel and n-channel MOSFETs respectively.

Equation (4.12) above explains the equivalent input-referred flicker noise in the simple OTA. The 1st term indicates the contribution of input MOSFETs in flicker noise while the term in parenthesis shows that of the mirrors. The contribution of mirror MOSFETs to flicker noise can be reduced by using longer channel devices than the input counterparts.

$$
\bar{\sigma}^2_{v_n,\text{Thermal}} = 4kT \frac{4}{3\sqrt{2}\mu_nC_{ox}(W/L)_iI_D} \left(1 + \frac{\mu_n(W/L)_i}{\mu_p(W/L)_i}\right)\Delta f
$$

(4.13)

Equation (4.13) above explains the equivalent input-referred thermal noise in the simple OTA. The 1st term in parenthesis shows the thermal noise contribution of input MOSFETs. The 2nd term in parenthesis indicates the thermal noise contribution of the current mirror. Thus from equation (4.13), the mirror thermal noise contribution “the 2nd
term” can be reduced by choosing \((W/L)_1 > (W/L)_3\), i.e. making the input MOSFETs with higher aspect ratio than mirror MOSFETs.

For the OTA operating in the sub-threshold regime, the MOSFET transconductances are directly related to their drain currents. So, the mirror to input MOSFETs transconductance ratio becomes 1. This is because the same currents are flowing in either OTA branches. Thus the input and mirrors MOSFETs will contribute all their noise to the OTA.

4.5.3 Noise in the sub-threshold simple OTA depending on strategy of 4.4

The sub-threshold OTA operates within its linear range region. The small signal model of Figure 2.4 is adopted to represent each MOSFET in the OTA to derive its input-referred noise power per unit bandwidth. Figure 4.5 below shows the small signal noise circuit of the simple OTA.

From Figure 4.5 below, the output noise per unit bandwidth will now be determined by superposition for each noise source separately assuming they are uncorrelated. This is done by replacing the voltage sources with short circuits and the current sources with open circuits. For this OTA, the contribution in output noise of each one of its five MOSFETs is taken with the absence of other MOSFETs as follows
1. MOSFET, M1 small signal model represented by a dependent current source, $V_g$. The parameter $g_s$ refers to the summation of MOSFET transconductance, $g_m$ and bulk transconductance, $g_{mb}$. It is more appropriate to use resistance instead of transconductance in such calculations, so that the dependent current source, $V_g g_s$ is replaced by a resistor, $1/g_s$ and the dependent current source, $i_{x1}$. Then the noise independent current source $\overline{i_1}$ is placed across the M1 drain to source terminals. The noise current, $i_1$ is equally divided into the two resistors $1/g_s$. From Figure 4.5, the current in each one of the two $1/g_s$ resistors, $i_{x1}$ and $i_{x2}$ equals $i_1/2$. The current passing through mirror resistance, $1/g_m$ is $i_m$ which equals $i_{x1}i_1$ then it equals -$i_1/2$. The OTA output current, $i_{out}$ equals $i_{x2}i_m$. So, $i_{out} = i_{x2}i_m = i_{x1}i_1/2 = i_1/2(-i_1/2) = i_1$, which means that all the noise current of MOSFET, M1 is added to the OTA output. Hence, the
transferred function of the MOSFET, M1 from its input to the OTA output is \( a_1 \) which equals \((1/2-(-1/2))\). The squared value of the transfer function, \( \alpha_1^2 \) equals \((1)^2\).

2. MOSFET, M2 is represented by its small signal model with the noise independent current source, \( i_2^2 \) that is placed across its drain to source terminals. The entire procedure made for M1 is repeated for M2, applied to mirror MOSFETs M3, M4, and to the bias MOSFET, M5 as in Figure 4.5 above. The results of this exercise are presented in Table 4.1 below.

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>Noise current source</th>
<th>( i_{out} = i_{x2} - i_m ) Due to each noise current source</th>
<th>Percentage contribution to the OTA output noise (%)</th>
<th>Transfer function ( \alpha_j^2 ) magnitude (A/\sqrt{Hz})</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>( i_1^2 )</td>
<td>( i_y/2 - (i_y/2) = i_1 )</td>
<td>100</td>
<td>((1/2 - (-1/2))^2 = 1)</td>
</tr>
<tr>
<td>M2</td>
<td>( i_2^2 )</td>
<td>( -i_y/2 - (i_y/2) = -i_2 )</td>
<td>100</td>
<td>((-1/2-1/2)^2 = 1)</td>
</tr>
<tr>
<td>M3</td>
<td>( i_3^2 )</td>
<td>( -i_3 )</td>
<td>100</td>
<td>((-1)^2 = 1)</td>
</tr>
<tr>
<td>M4</td>
<td>( i_4^2 )</td>
<td>( i_4 )</td>
<td>100</td>
<td>((1)^2 = 1)</td>
</tr>
<tr>
<td>M5</td>
<td>( i_5^2 )</td>
<td>( i_{x2} - i_x = 0 )</td>
<td>0</td>
<td>((0)^2 = 0)</td>
</tr>
</tbody>
</table>
From Table 4.1 above, it is clear that the input and mirror MOSFETs contribute all their noise to the OTA output while, ideally, the bias MOSFET contributes no noise due to opposing noise contributions from the two OTA arms. Hence, the total shot “white” noise current per unit bandwidth, $i_{\text{out}}^2(f)$ at the OTA output equals

$$i_{\text{out}}^2(f) = \sum_{j=1}^{5} [\alpha_j] \bar{i}_j^2(f) = (1^2 + 1^2 + 1^2 + 1^2 + 0^2) \cdot 2q \left( \frac{I_B}{2} \right)$$

where $j$ represents the number of independent noise current sources.

$$i_{\text{out}}^2(f) = 4 \cdot \left( 2q \left( \frac{I_B}{2} \right) \right)$$  \hspace{1cm} (4.14)

Thus, the total noise current per unit bandwidth, $i_{\text{out,tot}}^2(f)$ due to both white and flicker noise at the OTA equals

$$i_{\text{out,tot}}^2(f) = 4 \cdot \left( 2q \left( \frac{I_B}{2} \right) + K_F \frac{1}{C_{ox} WL f g_m^2} \right) \quad A^2 / Hz$$  \hspace{1cm} (4.15)

The input-referred noise voltage per unit bandwidth, $v_{\text{n,ref}}^2(f)$ is obtained as follows

$$v_{\text{n,ref}}^2(f) = \frac{i_{\text{out,ref}}^2(f)}{G_m^2} \quad V^2 / Hz$$  \hspace{1cm} (4.16)

In general, for $N$ shot noise sources, the input-referred noise in all frequencies can be expressed as follows
\[ \overline{v_{n, in}^2} = \int_{f_c}^\infty \frac{N}{f_c (I_B / V_L)^2} \left( 2q \left( \frac{I_B}{2} \right) + \frac{K_F (I_B / 2)^2}{C_{OX} W L f} \right) df \]  

(4.17)

where \( N, V_L, \) and \( q \) are the effective number of shot-noise sources in the amplifiers, the input linear range, and the charge on the electron respectively. \((I_B / V_L)^2 = G_m^2\) as long as the OTA operates within its linear range in the sub-threshold regime.

Finally, the RMS value of the noise voltage \( v_{n,eq,RMS} \) for the simple OTA is as follows

\[
v_{n,eq,RMS} = \sqrt{\overline{v_{n, in}^2}}
\]

(4.18)

### 4.5.4 Noise in Cascaded Amplifiers

The output noise power and the input referred noise power of a cascade of \( M \) noisy amplifiers shown in Figure 4.6 can be written as follows in equations (4.19) and (4.20) respectively

\[
\overline{v_{out,RMS}^2} = (A_{V1} A_{V2} \ldots A_{VM})^2 \overline{v_{n, in1,RMS}^2} + (A_{V2} \ldots A_{VM})^2 \overline{v_{n, in2,RMS}^2} + \cdots + A_{VM}^2 \overline{v_{n, inM,RMS}^2} \]  

\[
V^2 / Hz
\]

(4.19)

where \( A_{V1}, A_{V2}, \) and \( A_{VM} \) are the open loop voltage gains for \( M \) amplifiers shown in Figure 4.6 below. The equivalent input-referred noise power, \( \overline{v_{n, in,eq,RMS}^2} \) is obtained as in below

\[
\overline{v_{n, in,eq,RMS}^2} = \overline{v_{n, in1,RMS}^2} + \frac{\overline{v_{n, in2,RMS}^2}}{A_{V1}^2} + \cdots + \frac{\overline{v_{n, inM,RMS}^2}}{(A_{V1} A_{V2} \ldots A_{VM-1})^2} \]  

\[
V^2 / Hz
\]

(4.20)
Figure 4.6 Noise performance of a cascade of amplifiers, (a) A cascade of noisy amplifiers with their corresponding input-referred noise sources (b) The equivalent noise model for (a).

From equation (4.20), it is clear that when the open loop voltage gains are greater than unity, which is often the case; the early stages contribute more noise than the later stages [4.11]. Thus the input-referred noise power of the 1st stage has the largest effect on the noise performance of the system constituted from the $M$ cascaded amplifiers. So, care should be taken in designing the early stages since it has a crucial effect on the total input-referred noise of such system and hence its dynamic range.

### 4.5.5 Noise in a system consisting of a feedback loop

Before mentioning the effect of the system with a feedback loop on the noise, the closed loop transfer function of a simple linear system consisting of a negative feedback loop is derived. The system block diagram consists of $a(s)$ and $f(s)$, the feed forward and the feedback stages as shown in Figure 4.7 below. In such systems, the negative feedback makes the output to be fed back such as to decrease the input effect at dc.
Figure 4.7 Block diagram of a system with a feedback loop

To obtain the transfer function of the system, $H(s)$ the following derivation is made

$$\text{Output} = e(s) \times a(s) \quad (4.21)$$

$$e(s) = \text{Input} - \text{Output} \times f(s) \quad (4.22)$$

where $e(s)$ represents the error signal.

Substituting equation (4.22) in (4.21), yields

$$H(s) = \frac{\text{Output}}{\text{Input}} = \frac{a(s)}{1 + a(s)f(s)} \quad (4.23)$$

The system shown in Figure 4.8 below consists of three feed forward stages and a feedback stage. The closed loop transfer function, $H(s)$ for this system is as follows

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = V_{in}(s) \left( \frac{a_1(s)k_2(s)k_3(s)}{1 + a_1(s)k_2(s)k_3(s)f(s)} \right) + v_{n1}(s) \left( \frac{a_1(s)k_2(s)k_3(s)}{1 + a_1(s)k_2(s)k_3(s)f(s)} \right)$$
From equation (4.24) above, the attenuation results from comparing the gains of the noise sources $v_{n1}(s)$, $v_{n2}(s)$, $v_{n3}(s)$, and $v_{n4}(s)$ to the output with that of $V_{in}(s)$. It equals to $1$, $1/a_1(s)$, $1/a_2(s)$, and $1/a_1(s)a_2(s)a_3(s)$ for $v_{n1}(s)$, $v_{n2}(s)$, $v_{n3}(s)$, and $v_{n4}(s)$ respectively. As a result, the noise at the output is attenuated by $1/a_1(s)a_2(s)a_3(s)$ while that at the input is still the same. Therefore, the system of Figure 4.8 with a feedback has the ability to attenuate the output noise but not that at the input.

**4.5.6 Noise in the Proposed OTA**

The proposed OTA is described in chapter three. The reduction in noise occurs since for each noise source, there is a total or partial cancellation of its noise current at the output due to opposing contributions from the two circuit arms. For the proposed OTA
of Figure 3.5, the noise current from the bias MOSFET, M7 and that of bump MOSFETs, M5 and M6 make little contribution to the output noise current. This is because ideally, they branch into equal portions in the two differential arms, which effectively cancel each other at the output \[4.11\]. So, the proposed OTA has just 4 MOSFETs as dominant noise sources rather than 7 MOSFETs. Thus the design has relatively low noise since only 57% of the MOSFETs are significant sources of noise.

The noise model of the proposed OTA can be considered the same as that for the simple OTA seen in Figure 4.5 above since noise sources are the same. However the total input-referred noise is not the same. This is because the RMS noise voltage in the proposed OTA is increased due to the adoption of the capacitor attenuation technique for increasing input linear range. The RMS value of the thermal noise voltage of the proposed OTA is larger than that of the simple OTA by a factor of \(\sqrt{a^{-1}}\) (where: \(a^{-1}\) represents the number of times that the linear range increases using capacitor attenuators; that is, the number of times that \(G_m\) is decreased by the attenuation. The RMS values of the noise voltage \(v_{n, eq,RMS}\) for the simple and proposed OTAs are calculated as follows

1. Calculating the RMS value of the noise voltage \(v_{n, eq,RMS}\) for the simple OTA is as follows

   I. The total noise power mean squared value, \(v_n^2\) for each MOSFET in the simple OTA is calculated for a \(G_m\) value of 135nS and a 1Hz frequency bandwidth according to \(4.8\) above that equals to \(8.17 \times 10^{-14} \, \text{V}^2/\text{Hz}\).

   II. The total noise power mean squared value, \(v_{n, eq,n}^2\) and the RMS noise voltage \(v_{n, eq,RMS}\) for the simple OTA according equations \(4.16\) and \(4.18\) equals to \(32.68 \times 10^{-14} \, \text{V}^2/\text{Hz}\) and \(0.57 \, \mu\text{V}/\sqrt{\text{Hz}}\) respectively.
2. Calculating the RMS value of the noise voltage $v_{n,eq,RMS}$ for the proposed OTA as follows

I. The total noise power mean squared value, $\overline{v_{n,eq}^2}$ and the RMS noise voltage $v_{n,eq,RMS}$ for the proposed OTA are equal to $5.22 \times 10^{-12} V^2/Hz$ and $2.28 \mu V/ \sqrt{Hz}$ respectively.

It is important to notice that the RMS value of the noise voltage $v_{n,eq,RMS}$ for the proposed OTA equals $\sqrt{16}$ times that of the simple OTA as the increase in the linear range due to capacitor attenuation technique is chosen to be 16 fold.

4.6 Conclusion

The intrinsic noise in integrated circuits has been described with particular reference to low power MOSFET circuits. The associated low currents and voltage levels make such circuits particularly susceptible to the effects of noise which makes the understanding of noise to be crucial in the design. The chapter commenced with an introduction then the types of noise and how they can be represented with two strategies of representation. Those strategies are detailed together besides the equations used to represent noise in MOSFETs, OTAs, systems of cascaded stages, and systems with feedback. In general, the noise can be reduced in a circuit by decreasing the number of noise sources such as MOSFETs and resistors constituting the circuit. Also, the noise can be reduced further by expending more power and area to decrease the white noise (thermal/shot noise) and $1/f$ noise respectively. Since, in analogue design any optimisation of a feature in a circuit performance will be at the expense of disturbing another one or increasing the circuit cost or batteries size, so the design specifications is satisfied as a trade off in accordance with the application.
CHAPTER FOUR

Noise in Integrated Circuits

References


CHAPTER FIVE

The Proposed OTA-C Filters for Cochlear Implants

5.1 Introduction

Research in OTA-C filters focuses mainly on two aspects, the transconductor design and the filter topology. Chapter three addressed the first aspect and this chapter answers the second. In this work, four OTA-C band-pass filter topologies are proposed, simulated, and two of them (topologies 1 and 2) are tested experimentally. Also, a 4-channel parallel OTA-C filter bank is proposed and experimentally tested. The design details and the obtained results are mentioned and discussed in the next sections.

5.2 Proposed Filter Topologies

The derivation of the transfer functions of each one of the four topologies besides poles relations are mentioned as follows

5.2.1 Topology 1

The OTA-C band-pass filter in this topology consists of a cascade of 1st order high-pass and 1st order low-pass filters. The OTAs, \( G_{m1} \) and \( G_{m2} \) respectively represent the OTA with bumping MOSFETs shown earlier in Figure 3.3, the capacitive attenuators \( (C_1/C_2) \), \( (C_3/C_4) \), and output capacitors, \( C_A \) and \( C_B \) as shown in Figure 5.1. The capacitor
attenuation ratio, $a$, is set to be 16 by letting $C_2$ and $C_4$ to be 15 fold of $C_1$ and $C_3$ respectively “$r=15/1$”. The OTA, $G_{m3}$, represents a simple differential OTA shown earlier in figure 3.1. The presence of $G_{m3}$ is essential to provide the DC path to ensure that floating capacitance nodes $V_{out}$ and $Y$ are biased correctly. $G_{m3}$ is biased with a small voltage, $V_{B3}$ to make $I_{B3}$ small to guarantee that it will not be active in pass-band. It is worth noting that this topology is similar to that used in [5.3] but with an added output capacitor $C_A$ in order to decrease the noise.

![Proposed OTA-C filter topology](image)

Figure 5.1 Proposed OTA-C filter topology

1. Transfer function derivation

The nodal equations are used to obtain the transfer function for all the proposed filters. For the filter of Figure 5.1, the nodal equations are derived as follows:
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The Proposed OTA-C Filters for Cochlear Implants

I. Node X

For node X, by apply Kirchhoff’s current law (KCL) in each node gives, the sum of currents around node X=0 to obtain

\[
(V_x - V_m) sC_1 + V_x sC_2 - I_{O1} + V_x sC_A + I_{G1} = 0
\]

\[
(V_x - V_{in}) sC_1 + V_x sC_2 - (-V_x G_{m1}) + V_x sC_A + I_{G1} = 0
\]

But the gate current, \( I_{G1} \) for the input MOSFET of the OTA “\( G_{m1} \)” = 0 and this is also the case for all other OTAs.

\[
V_x = \frac{V_{in}}{C_1 + C_2 + C_A + G_{m1}} \tag{5.1}
\]

II. Node Y

For node Y, \( \sum \text{currents around node Y}=0 \)

\[
(V_y - V_{out}) sC_3 + V_y sC_4 - I_{O3} + I_{G2} = 0
\]

\[
(V_y - V_{out}) sC_3 + V_y sC_4 - (V_{out} G_{m3}) + I_{G2} = 0
\]

\[
V_y = \frac{sC_3 + G_{m3}}{s(C_3 + C_4)} \tag{5.2}
\]

III. For \( G_{m2} \)

\[
I_{O2} = V_{out} sC_B + (V_{out} - V_y) sC_3 = (V_x - V_y) G_{m2}
\]
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The Proposed OTA-C Filters for Cochlear Implants

\[ V_{out} = \frac{V_x G_{m2} + V_y (sC_3 - G_{m2})}{s(C_B + C_3)} \] (5.3)

By substituting the values of \( V_x \) and \( V_y \) of equations (5.1) and (5.2) respectively in equation (5.3), give

\[ V_{out} = \frac{V_{in}}{(C_1 + C_2 + C_A) + G_{m1}} \cdot \frac{C_G G_{m2}}{s(C_B + C_3)} + \frac{V_{out}}{s(C_3 + C_4)} \left( s(C_3 + C_4) \right) \]

\[ V_{out} = \frac{V_{in}}{(C_1 + C_2 + C_A) + G_{m1}} \cdot \frac{C_G G_{m2}}{s(C_B + C_3)} + \frac{V_{out}}{s(C_3 + C_4)} \left( s^2 C_3^2 + sC_3 G_{m3} - sC_3 G_{m2} - G_{m2} G_{m3} \right) \]

\[ V_{out} = \frac{V_{in}}{(C_1 + C_2 + C_A) + G_{m1}} \cdot \frac{C_G G_{m2}}{s(C_B + C_3)} + \frac{V_{out}}{s(C_3 + C_4)} \left( s^2 C_3^2 + sC_3 G_{m3} - sC_3 G_{m2} - G_{m2} G_{m3} \right) \]

\[ H_1(s) = \frac{V_{out}}{V_{in}} = \frac{s^2 K_{Z1}}{(sK_{p3} + G_{m1})/s^2 K_{p2} + sK_{p1} + K_{p0}} \] (5.4)

where

\[ K_{p3} = (C_1 + C_2 + C_A) \]
\[ K_{p2} = (C_B (C_3 + C_4) + C_3 C_4) \]
\[ K_{p1} = C_3 (G_{m2} - G_{m3}) \]
\[ K_{p0} = G_{m2} G_{m3} \]
\[ K_{Z1} = C_1 (C_3 + C_4) G_{m2} \]

The detailed derivation can be found in Appendix B.1.
2. Finding the Filter poles

From the transfer function (5.4), it is clear that the filter is always stable and the only possibility for instability is shown in $K_{p1}$ when $G_{m2} < G_{m3}$ which is untrue since $G_{m2}$ is always much greater than $G_{m3}$. It is easy to obtain the filter poles represented by $p_1$, $p_2$, and $p_3$. This is because the transfer function denominator that is a 3rd order polynomial is already factorised to 1st order and 2nd order equations. The poles are obtained as follows

$$p_1 = -\frac{G_{m1}}{C_1 (r+1) + C_A} = -\frac{G_{m1}}{aC_1 + C_A}$$

$$p_{2,3} = -\frac{(G_{m2} - G_{m3})}{2(r(C_B + C_3) + C_B)} \pm \frac{\sqrt{(C_3(G_{m2} - G_{m3}))^2 - 4(rC_3(C_B + C_3) + C_B C_3)G_{m2}G_{m3}}}{2(rC_3(C_B + C_3) + C_B C_3)}$$

(5.5)

where $C_1 = C_3$, $C_2 = C_4$, $C_3 = rC_2$, $C_4 = rC_3$, and $a = r + 1$. Since the value of $G_{m3}$ is small, an approximation can be made by cancelling it, so equation (5.5) will be approximated as follows

$$p_{2,3} = -\frac{G_{m2}}{2(r(C_B + C_3) + C_B)} \pm \frac{\sqrt{(C_3(G_{m2}))^2}}{2(rC_3(C_B + C_3) + C_B C_3)}$$

$$= -\frac{G_{m2}}{2(r(C_B + C_3) + C_B)} \pm \frac{C_3 G_{m2}}{2(rC_3(C_B + C_3) + C_B C_3)}$$

$$= -\frac{G_{m2}}{2(r(C_B + C_3) + C_B)} \pm \frac{G_{m2}}{2(r(C_B + C_3) + C_B C_3)}$$

$$= -\frac{2G_{m2}}{2(r(C_B + C_3) + C_B)} = -\frac{G_{m2}}{r(C_B + C_3) + C_B}$$

$$p_2 = -\frac{G_{m2}}{r(C_B + C_3) + C_B} = -\frac{G_{m2}}{aC_B + rC_3}$$
Therefore, the effective poles can be considered to be two instead of three when the approximation is made. In this case, both poles are in the left hand side of the s-plane meaning that the filter always stable. The filter bandwidth is controlled by independently adjusting its low and high frequency parts. The low frequency is proportional to the bias current of \( G_{m1} \) “\( I_{B1} \)” while the high frequency component is proportional to the bias current of \( G_{m2} \) “\( I_{B2} \”).

### 5.2.2 Topology 2

This filter consists of two OTAs namely, \( G_{m1} \) and \( G_{m2} \) with the capacitor attenuators, \( (C_1/C_2) \) and \( (C_3/C_2) \) and an output capacitor, \( C \) as shown in Figure 5.2. The capacitor \( C_1 \) provides high-pass filtering action while \( C \) and \( C_3 \) have the low-pass filtering effect combining to give band-pass filtering action at \( V_{out} \). The transconductor, \( G_{m2} \) also provides the necessary DC path for the \( V_{out} \) and \( X \) nodes.

![Figure 5.2 Proposed OTA-C filter topology2](image-url)
1. Transfer function derivation

The transfer function for the filter shown in Figure 5.2, is derived as follows

I. Node X

For node X, $\sum$ currents around node $X=0$

$$(V_X - V_{in})sC_1 + V_X sC_2 + (V_X - V_{out})sC_3 - I_{O2} = 0$$

$$(V_X - V_{in})sC_1 + V_X sC_2 + (V_X - V_{out})sC_3 - (V_{out}G_{m2}) = 0$$

$$V_X s(C_1 + C_2 + C_3) = V_{in}C_1 + V_{out}(sC_3 + G_{m2})$$  \(\text{(5.6)}\)

II. For $G_{m1}$

$$I_{O1} = V_{out} \frac{s}{G_{m1}} (V_{out} - V_X) sC_3 = -V_X G_{m1}$$

$$V_X = V_{out} \frac{s(C + C_1)}{(sC_3 - G_{m1})}$$  \(\text{(5.7)}\)

By substituting the value of $V_X$ of equation (5.7) in equation (5.6) yields

$$V_{out} \frac{s(C + C_3)}{(sC_3 - G_{m1})} (C_1 + C_2 + C_3) = V_{in} sC_1 + V_{out} (sC_3 + G_{m2})$$

$$V_{out} \frac{s^2(C + C_3)(C_1 + C_2 + C_3)}{(sC_3 - G_{m1})} = V_{in} sC_1 + V_{out} (sC_3 + G_{m2})$$

$$V_{out} \frac{s^2(C + C_3)(C_1 + C_2 + C_3)}{(sC_3 - G_{m1})} - V_{out} (sC_3 + G_{m2}) = V_{in} sC_1$$

$$V_{out} \left\{ \frac{s^2(C + C_3)(C_1 + C_2 + C_3) - (sC_3 - G_{m1})(sC_3 + G_{m2})}{(sC_3 - G_{m1})} \right\} = V_{in} sC_1$$
\[
V_{out}\left(\frac{s^2(C+C_3)(C_1+C_2+C_3)-(s^2C_3^2-sC_3(G_{m1}-G_{m2})-G_{m1}G_{m2})}{sC_3-G_{m1}}\right)=V_{in}sC_1
\]

\[
H_2(s) = \frac{V_{out}}{V_{in}} = \frac{s^2K_{Z2}-sK_{Z1}}{s^2K_{p2}+sK_{p1}+K_{p0}}
\]

where

\[
K_{p2} = (C(C_1+C_2+C_3)+C_3(C_1+C_2))
\]

\[
K_{p1} = sC_3(G_{m1}-G_{m2})
\]

\[
K_{p0} = G_{m1}G_{m2}
\]

\[
K_{Z2} = C_1C_3
\]

\[
K_{Z1} = C_1G_{m1}
\]

The detailed derivation is provided in Appendix B.2.

2. Finding the filter poles

The denominator of the transfer function of equation (5.8) above is a 2\textsuperscript{nd} order polynomial. The transfer function is always stable if \(G_{m1}>G_{m2}\) in \(K_{p1}\), which is always the case. The two poles are obtained as follows:

\[
P_{1,2} = -\frac{C_3(G_{m1}-G_{m2})}{2(C(C_1+C_2+C_3)+C_3(C_1+C_2))} \pm \frac{\sqrt{(C_3(G_{m1}-G_{m2}))^2-4(C(C_1+C_2+C_3)+C_3(C_1+C_2))G_{m1}G_{m2}}}{2(C(C_1+C_2+C_3)+C_3(C_1+C_2))}
\]

(5.9)
Equation (5.9) can be minimised since $C_1 = C_3$ and $C_2 = rC_1 = rC_3$, so it will be as follows:

$$
\begin{align*}
    p_{1,2} &= -\frac{C_1(G_{m1} - G_{m2})}{2(CC_1(2 + r) + C_1^2(1 + r))} \\
    &\pm \sqrt{(C_1(G_{m1} - G_{m2}))^2 - 4(CC_1(2 + r) + C_1^2(1 + r))G_{m1}G_{m2}} \\
    p_{1,2} &= -\frac{(G_{m1} - G_{m2})}{2(C(2 + r) + C_1(1 + r))} \\
    &\pm \sqrt{(C_1(G_{m1} - G_{m2}))^2 - 4(CC_1(2 + r) + C_1^2(1 + r))G_{m1}G_{m2}} \\
    &\frac{2(CC_1(2 + r) + C_1^2(1 + r))}
\end{align*}
$$

As shown from equation (5.9), the two poles are complex conjugate poles lying in the left hand side of s-plane.

5.2.3 Topology 3

The proposed topology is shown in Figure 5.3. The filter consists of two OTAs namely, $G_{m1}$ and $G_{m2}$ with the capacitor attenuators, $(C_1/C_2)$ and $(C_3/C_4)$ and an output capacitor, $C$. As in topology 2, capacitor $C_1$ has high-pass filtering action while $C$ and $C_3$ give low-pass to give the band-pass filtering action at $V_{out}$. The second transconductor $G_{m2}$ provides the necessary DC path for the $V_{out}$ and $X$ nodes.
1. Transfer function derivation

The transfer function is derived as follows

I. Node X

For node X, \( \sum \) currents around node \( X = 0 \)
\[
(V_X - V_{in}) s C_1 + V_X s C_2 + I_{G1} = 0
\]
\[
V_X = \frac{V_{in}}{s C} \frac{C_1}{C_1 + C_2}
\] (5.10)

II. For \( G_{m1} \)

\[
I_{O1} = V_{out} s C + (V_{out} - V_Y) s C_3 = (V_X - V_Y) G_{m1}
\]
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\[ V_x G_{m1} = V_{out} s(C + C_3)(G_{m1} - sC_3) \]  \hspace{1cm} (5.11)

III. Node Y

For node Y, \( \sum \) currents around node \( Y = 0 \)

\[ (V_y - V_{out}) sC_3 + V_y sC_4 - I_{Gx} + I_{Gz} = 0 \]
\[ (V_y - V_{out}) sC_3 + V_y sC_4 - (V_{out} G_{m2}) = 0 \]

\[ V_y = V_{out} \frac{(sC_3 + G_{m2})}{s(C_3 + C_4)} \]  \hspace{1cm} (5.12)

Substituting the values of \( V_x \) and \( V_y \) in equations (5.10) and (5.12) respectively, in equation (5.11) gives

\[ V_{in} \frac{C_1 G_{m2}}{(C_1 + C_2)} = V_{out} \left( s(C + C_3) - \frac{(sC_3 + G_{m2})(G_{m1} - sC_3)}{s(C_3 + C_4)} \right) \]

\[ V_{in} \frac{C_1 G_{m2}}{(C_1 + C_2)} = V_{out} \left( \frac{(s(C + C_3))(s(C_3 + C_4)) + (sC_3 + G_{m2})(G_{m1} - sC_3)}{s(C_3 + C_4)} \right) \]

\[ H_3(s) = \frac{V_{out}}{V_{in}} = \frac{sK_{z1}}{s^2 K_{p2} + sK_{p1} + K_{p0}} \]  \hspace{1cm} (5.13)

where

\[ K_{p2} = (C_1 + C_2)(C(C_3 + C_4) + C_3 C_4) \]
\[ K_{p1} = C_3(C_1 + C_2)(G_{m1} - G_{m2}) \]
\[ K_{p0} = (C_1 + C_2)G_{m1}G_{m2} \]
\[ K_{z1} = C_1(C_3 + C_4)G_{m1} \]
The detailed derivation is in Appendix B.3.

2. Finding the filter poles

The denominator of the transfer function of equation (5.13) above is a 2nd order polynomial. The transfer function is always stable if \( G_{m1} > G_{m2} \) in \( K \), which is always the case for this design. The two poles are obtained as follows

\[
p_{1,2} = -\left(\frac{G_{m1} - G_{m2}}{2(r(C + C_3) + C)} + \sqrt{\left(\frac{C_1}{G_{m1} - G_{m2}}\right)^2 - 4\left(rC_1(C + C_3) + CC_2\right)G_{m1}G_{m2}}\right) \frac{2(r(C + C_3) + CC_3)}{2(rC_3(C + C_3) + CC_3)}
\]

(5.14)

where \( C_1 = C_3, C_2 = C_4, C_1 = rC_2, \) and \( C_4 = rC_3 \)

As shown from equation (5.14), the two poles are complex conjugate poles lying in the left hand side of \( s \)-plane.

5.2.4 Topology 4

This topology consists of the OTAs, \( G_{m1} \) and \( G_{m2} \) respectively with the capacitor attenuators, \( (C_1/C_2) \), \( (C_3/C_4) \), and \( (C_5/C_6) \) and output capacitors, \( C_A \) and \( C_B \). Each of transconductors \( G_{m1} \) and \( G_{m2} \), with capacitors connected to them representing two cascaded band-pass filter stages. This design offers an improved frequency response represented by a 2nd order roll-off compared to 1st order roll-off obtained from the other proposed filter topologies. The filter output voltage \( V_{out} \) and \( Z \) nodes are DC constrained via the transconductance named \( G_{m3} \) as shown in Figure 5.4.
1. Transfer function derivation

The transfer function for this proposed filter shown in Figure 5.4 is derived as follows

I. Node X

For node $X$, $\sum$ currents around node $X=0$

$$V_x = V_{in} \frac{C_1}{(C_1 + C_2)} \quad (5.15)$$
\[ I_{o1} = V_{o1} sC_A + (V_{o1} - V_Y) sC_3 = (V_X - V_Z) G_{m1} \]

**II. For \( G_{m1} \)**

\[ V_{o1} = \frac{1}{s(C_A + C_3)} (V_X G_{m1} + V_Y sC_3 - V_Z G_{m1}) \]  \hspace{1cm} (5.16)

**III. Node Y**

For node \( Y \), \( \sum \) currents around node \( Y = 0 \)

\[ (V_Y - V_{o1}) sC_3 + V_Y sC_4 + I_{G2} = 0 \]

\[ V_Y = V_{o1} \frac{C_3}{(C_3 + C_4)} \]  \hspace{1cm} (5.17)

**IV. For \( G_{m2} \)**

\[ I_{o2} = V_{out} sC_B + (V_{out} - V_Z) sC_5 = (V_Y - V_Z) G_{m2} \]

\[ V_{out} = \frac{1}{s(C_B + C_5)} (V_Y G_{m2} - V_Z (G_{m2} - sC_5)) \]  \hspace{1cm} (5.18)

**V. Node Z**

For node \( Z \), \( \sum \) currents around node \( Z = 0 \)

\[ (V_Z - V_{out}) sC_5 + V_Z sC_6 - I_{o3} + I_{G3} = 0 \]

\[ (V_Z - V_{out}) sC_5 + V_Z sC_6 - (V_{out} G_{m3}) + I_{G3} = 0 \]
$V_Z = \frac{V_{out}}{s} \left( \frac{sC_5 + G_{m3}}{sC_5 + C_a} \right)$ \hspace{1cm} (5.19)

By substituting the value of $V_X$ of equation (5.15) in equation (5.16),

$V_{OJ} = \frac{1}{s(C_A + C_3)} \left( V_{in} \frac{C_1 G_{m1}}{(C_1 + C_2)} + V_Y sC_3 - V_Z G_{m1} \right) \frac{C_3}{(C_3 + C_4)}$ \hspace{1cm} (5.20)

The value of $V_{OJ}$ of equation (5.20) above is substituted in equation (5.17) to give

$V_Y = \frac{1}{s(C_A + C_3)} \left( V_{in} \frac{C_1 G_{m1}}{(C_1 + C_2)} + V_Y sC_3 - V_Z G_{m1} \right) \frac{C_3}{(C_3 + C_4)}$ \hspace{1cm} (5.21)

Substituting the values of $V_Y$ and $V_Z$ of equations (5.21) and (5.19) respectively in equation (5.18), yields

$V_{out} = \frac{1}{s(C_B + C_5)} \left( C_3 G_{m2} \left( V_{in} \frac{C_1 G_{m1}}{(C_1 + C_2)} - V_{out} \left( \frac{sC_5 + G_{m3}}{sC_5 + C_6} \right) G_{m1} \right) \right.$

$\left. \frac{s(C_A + C_3)(C_3 + C_4) - C_3^2}{s} \right) - V_{out} \left( \frac{sC_5 + G_{m3}}{s} \right) \left( G_{m2} - sC_3 \right) \frac{s}{C_5 + C_6}$

By rearranging and simplifying terms in the above equation, the following transfer function is obtained
2. Finding the filter poles

The denominator of equation (5.22) is a 3rd order polynomial which makes the process of obtaining its poles more complicated than for 2nd order polynomials. However, the three poles are obtained using Maple software. Two of those poles are two complex conjugate poles and the 3rd one is a real pole all of which lie in the left hand side of the s-plane. So, the filter transfer function general in factorised form becomes as follows

\[
H_4(s) = \frac{V_{out}}{V_{in}} = \frac{sK_{Z1}}{s^3K_{p3} + s^2K_{p2} + sK_{p1} + K_{p0}}
\]  

(5.22)

\[K_{p3} = C_3\left(aC_A + rC_3\right)^2\]

\[C_1 = C_3, \quad C_2 = C_4, \quad C_1 = rC_2, \quad C_4 = rC_3, \quad \text{and} \quad C_6 = rC_5\]

\[a=1+r\]

\[K_{p2} = C_3\left(G_{m2} - G_{m3}\right)\left(aC_A + rC_3\right)\]

\[K_{p1} = G_{m2}\left(C_3G_{m1} + \left(aC_A + rC_3\right)G_{m3}\right)\]

\[K_{p0} = G_{m1}G_{m2}G_{m3}\]

\[K_{Z1} = C_3G_{m1}G_{m2}\]

The detailed derivation is in Appendix B.4.
The above $p_1$, $p_2$, and $p_3$ poles represent the real and the two complex conjugate poles respectively. The detailed solution is described in Appendix B.5.

5.3 Design Details

5.3.1 Specifications

The next-generation cochlear implants, CI should have small sizes so they can be completely implanted inside the body of the patient. Low power consumption can be achieved using circuits that operate at very small current levels and by decreasing the MOSFET dimensions. As a consequence, low voltage operation is required which results in small size batteries. The operation of MOSFETs in the sub-threshold regime where the current range is in nano-amperes, produces the best solution for obtaining low-power circuits. The CI band-pass filter design requires covering the audio frequency range of 100Hz to 10 kHz with bandwidths of not more than one octave. Also, the dynamic range of the filters must be more than 60dB [5.1]. The sub-threshold OTA-C filters are proposed for such applications because of their wide tuning range and low power consumption.

5.3.2 MOSFET Sizing

The OTA-C filters are designed to guarantee their fully sub-threshold regime operation which offers low saturation voltage, wide tuning range, and low power consumption. According to the desired linear range, the bumping MOSFET aspect ratio and the capacitor attenuation ratio are selected. The values of the capacitors are chosen to realise the required dynamic range that is more than 60dB. Then sizing of the MOSFETs is made to ensure that the sub-threshold current range is sufficient to provide the desired frequency ranges. The sizing of MOSFETs is important since with their appropriately chosen dimensions and currents, their flicker noise and corner frequency
will be reduced respectively. This leads to white noise domination over flicker noise [5.2]. Dominating the white noise over flicker noise is very beneficial as detailed in section 5.6 below. The MOSFET dimensions, currents, and $g_m/I_D$ values for filter topologies 1 and 2 represent those of the proposed OTA and are shown in Tables 5.1 and 5.2 below. This design ensures that the required specifications mentioned in section 5.3.1 above are met, in particular, the dynamic range and the operation confined within the sub-threshold regime while providing (5-10) kHz frequency range. Each of these two tables shows different dimensions for the OTAs to assess the affect of $1/f$ noise.

Table 5.1: The dimensions of OTA MOSFETs of the proposed topologies 1 and 2

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>$g_m/I_D$ (V$^{-1}$)</th>
<th>$I_D$ (nA)</th>
<th>$W/L$</th>
<th>$W$ ($\mu$m)</th>
<th>$L$ ($\mu$m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>27</td>
<td>80</td>
<td>2.5</td>
<td>15</td>
<td>6</td>
</tr>
<tr>
<td>M3, M4</td>
<td>23</td>
<td>80</td>
<td>2.5</td>
<td>15</td>
<td>6</td>
</tr>
<tr>
<td>M5, M6</td>
<td>27.2</td>
<td>80</td>
<td>5</td>
<td>30</td>
<td>6</td>
</tr>
<tr>
<td>M7</td>
<td>26</td>
<td>240</td>
<td>5</td>
<td>30</td>
<td>6</td>
</tr>
</tbody>
</table>

Table 5.2: The dimensions of OTA MOSFETs of the proposed topologies 3 and 4

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>$g_m/I_D$ (V$^{-1}$)</th>
<th>$I_D$ (nA)</th>
<th>$W/L$</th>
<th>$W$ ($\mu$m)</th>
<th>$L$ ($\mu$m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>27.5</td>
<td>80</td>
<td>5</td>
<td>15</td>
<td>3</td>
</tr>
<tr>
<td>M3, M4</td>
<td>23.5</td>
<td>80</td>
<td>5</td>
<td>15</td>
<td>3</td>
</tr>
<tr>
<td>M5, M6</td>
<td>27.7</td>
<td>80</td>
<td>10</td>
<td>30</td>
<td>3</td>
</tr>
<tr>
<td>M7</td>
<td>26</td>
<td>240</td>
<td>5</td>
<td>30</td>
<td>6</td>
</tr>
</tbody>
</table>
5.4 Simulation Results

The simulations are conducted in the Cadence environment using SpectreS with BSIM3v3.1 models and parameters from the AMS process for 0.35µm CMOS C35 Technology. The simulations are performed to obtain the frequency response and the noise for the four filter topologies.

5.4.1 The Frequency Response

1. Topologies 1 and 2

Figures 5.5 and 5.6 show the simulated frequency responses for topologies 1 and 2 respectively. For both topologies the frequency response programmability of their centre frequencies and bandwidths appear clearly. By tuning the bias voltages \( V_{B1} \), \( V_{B2} \), and \( V_{B3} \) for topology 1 and \( V_{B1} \) and \( V_{B2} \) for topology 2, their currents and by extension their transconductances, can be programmed for the desired frequency response. The centre frequency programming covers the two extremes of the audio frequency range needed for CI for both topologies. The bandwidth programmability ensures a range in a quality factor, \( Q \) of \((1.5 - 5)\) for topology 1 and of \((1.5 - 7.5)\) for topology 2. Each topology has a 1\textsuperscript{st} order roll-off with a value of -20 dB/decade since each one of them is represented by cascading a 1\textsuperscript{st} order high-pass filter with a 1\textsuperscript{st} order low-pass filter.
Figure 5.5 Simulated frequency response of the Topology 1 OTA-C band-pass filter showing the programmability of both centre frequencies and bandwidths
Figure 5.6 Simulated frequency response of the Topology 2 OTA-C band-pass filter showing the programmability of both centre frequencies and bandwidths

2. Topologies 3 and 4

Figures 5.7 and 5.8 show the simulated frequency responses for topologies 3 and 4 respectively with the two cases at the extreme ends of the audio frequency range required for CI. The centre frequency programmability for both topologies is achieved by tuning the bias voltages $V_{B1}$ and $V_{B2}$ for topology 3 and $V_{B1}$, $V_{B2}$, and $V_{B3}$ for topology 4 respectively. Topology 3 has a 1\textsuperscript{st} order roll-off with a value of -20 dB/decade since its band-pass characteristics is obtained by cascading a 1\textsuperscript{st} order high-pass filter with a 1\textsuperscript{st} order low-pass filter. Topology 4 has a 2\textsuperscript{nd} order roll-off with a value of -40 dB/decade since it represents two cascaded band-pass filter stages.
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Figure 5.7 Simulated frequency response of the Topology 3 OTA-C band-pass filter

Figure 5.8 Simulated frequency response of the Topology 4 OTA-C band-pass filter showing
5.4.2 Noise

1. Simulations

Figures 5.9, 5.10, 5.11, and 5.12, show the simulated voltage noise spectrum for topologies 1, 2, 3, and 4 respectively. As mentioned in sections above, careful sizing of MOSFET in the sub-threshold regime can ensure that thermal noise dominates over $1/f$ noise. It is apparent that the $1/f$ noise contribution in the 1st extreme end of the audio frequency of (100-200) Hz is small. There is a small contribution in the second extreme end of (5-10) kHz as it aimed in the design especially for topologies 1 and 2. The MOSFET dimensions in the OTAs of topologies 1 and 2 are larger than those of topologies 3 and 4. However the flicker noise corner frequency values for topologies 3 and 4 are 15Hz and 20Hz for (100-200) Hz band and 160Hz and 190Hz for the (5-10k) Hz band. These values are relatively larger than those of topologies 1 and 2 mentioned in section 5.5.2 below due to their smaller dimensions.
Figure 5.9 Simulated output noise of the Topology 1 OTA-C band-pass filter for the (100-200) Hz and (5-10) kHz frequency bands
Figure 5.10 Simulated output noise of the Topology 2 OTA-C band-pass filter for the (100-200) Hz and (5-10) kHz frequency bands
Figure 5.11 Simulated output noise of the Topology 3 OTA-C band-pass filter for the (100-200) Hz and (5-10) kHz frequency bands.
2. Noise Calculations

Firstly, the input-referred noise is calculated for each transconductor. In equilibrium, for the simple OTA, four of its five MOSFETs contribute noise and each of them carries half of the bias current. The proposed OTA has seven MOSFETs but ideally, only four of them contribute significant noise to the output, as mentioned earlier in chapter two. The output current noise of both simple and proposed OTAs respectively are shown below [5.3]

\[ i_{\text{out, simple}}^2 = 4 \left( 2q \left( \frac{I_B}{2} \right) \right) = 4qI_B \]  

\[ (5.24) \]
The current noise in the two equations above is referred to the input as voltage noise by dividing it by the transconductance squared as follows:

\[
\begin{align*}
\text{\(i_{\text{out,proposed}}^{2} = 4\left(2q\left(\frac{I_B}{3}\right)\right) = \frac{8}{3} qI_B\)}
\end{align*}
\]

\[
\text{(5.25)}
\]

where \(I_B\) and \(V_L\) represent the bias current and the input linear range of the transconductor respectively. The input-referred noise equation for the OTA with the presence of bumping MOSFETs is the same as the simple OTA. This is because the OTA transconductance due to bumping is \((2/3)\) times that of simple OTA.

By the principal of superposition, the contributing effects of each noise source at the output node can be summed by considering one noise source at a time. So, for the filters proposed here, which comprise more than one transconductor, the transfer function from the input of each transconductor to the output is firstly computed. The input-referred power of each transconductor is then multiplied by the square magnitude of its transfer function. At the output node, the filtered powers from each noise source are summed and the total noise at the output is obtained for all topologies as follows

I. Noise of Topology 1

For this topology, shown in Figure 5.1 above, the total integrated noise is calculated as follows
\[ v_{n,eq}^2(s) = v_{n1}^2(s) + v_{n2}^2(s) + v_{n3}^2(s) \]  \hspace{1cm} (5.28)

where \( v_{\text{noise1}}^2(s) \), \( v_{\text{noise2}}^2(s) \), and \( v_{\text{noise3}}^2(s) \) are the input-referred noise powers due to transconductors \( G_{m1} \), \( G_{m2} \), and \( G_{m3} \) respectively.

\[ v_{n1}^2(s) = 4 \frac{q V_L^2}{I_{B1}} \left( \frac{G_{m1}}{sC_1} \right)^2 \cdot H_1^2(s) \]  \hspace{1cm} (5.29)

\[ v_{n2}^2(s) = 4 \frac{q V_L^2}{I_{B2}} \left( \frac{V_m}{V_X} \right)^2 \cdot H_2^2(s) \]  \hspace{1cm} (5.30)

\[ v_{n3}^2(s) = 4 \frac{q V_L^2}{I_{B3}} \cdot \left( \frac{G_{m3}(sC - G_{m1})}{s^2(C(C_3 + C_4) + C_3C_4) + sC_3(G_{m1} - G_{m2}) + G_{m1}G_{m2}} \right)^2 \]  \hspace{1cm} (5.31)

**II. Noise of Topology 2**

For this topology shown in Figure 5.2 above, the total integrated noise is calculated as follows

\[ v_{n,eq}^2(s) = v_{n1}^2(s) + v_{n2}^2(s) \]  \hspace{1cm} (5.32)

\[ v_{n1}^2(s) = 4 \frac{q V_L^2}{I_{B1}} \left( \frac{V_m}{V_X} \right)^2 \cdot H_2^2(s) \]  \hspace{1cm} (5.33)

\[ v_{n2}^2(s) = 4 \frac{q V_L^2}{I_{B2}} \cdot \left( \frac{G_{m2}(sC - G_{m1})}{s^2(C(C_3 + C_4) + C_3C_4) + sC_3(G_{m1} - G_{m2}) + G_{m1}G_{m2}} \right)^2 \]  \hspace{1cm} (5.34)
III. Noise of Topology 3

For this topology shown in Figure 5.3 above, the total integrated noise is as follows

\[ v_{n,eq}^2(s) = v_{n1}^2(s) + v_{n2}^2(s) \]  

(5.35)

\[ v_{n1}^2(s) = 4 \frac{q V_L^2}{I_{R1}} \left( \frac{V_{in}}{V_X} \right)^2 \cdot H_3^2(s) \]  

(5.36)

\[ v_{n2}^2(s) = 4 \frac{q V_L^2}{I_{R2}} \cdot \left( \frac{G_{n2} (sC - G_{m1})}{s^2(C(C_3 + C_4) + C_5 C_4) + sC_3(G_{m1} - G_{m2}) + G_{m1} G_{m2}} \right)^2 \]  

(5.37)

IV. Noise of Topology 4

For this topology shown in Figure 5.4, above, the total integrated noise is calculated as follows

\[ v_{n,eq}^2(s) = v_{n1}^2(s) + v_{n2}^2(s) + v_{n3}^2(s) \]  

(5.38)

\[ v_{n1}^2(s) = 4 \frac{q V_L^2}{I_{R1}} \left( \frac{V_{in}}{V_X} \right)^2 \cdot H_4^2(s) \]  

(5.39)

\[ v_{n2}^2(s) = 4 \frac{q V_L^2}{I_{R2}} \left( \frac{V_{in}}{V_Y} \right)^2 \cdot H_4^2(s) \]  

(5.40)
\[
v_{n3}^2(s) = 4qV_L^2 I_{R3}\frac{G_{m3}(sC \beta - G_{m2})}{(s + b + j\omega)(s + b - j\omega)}^2
\]

(5.41)

5.4.3 The Filter Dynamic Range

For a signal processing system such as a filter, the dynamic range is the ratio of the maximum to the minimum signal levels which are properly processed by it. The maximum signal level is limited by the system non-linearities that cause an appreciable distortion which is determined by the input linear range at an acceptable distortion. The minimum signal level is restricted by the system noise floor that is determined by the input-referred noise. The dynamic range is calculated in terms of decibel, dB units. It can be calculated as in equation (5.42) below [5.2]

\[
DR = 10\log \frac{V_L^2/2}{v_{in\text{- noise}}^2}
\]

(5.42)

where \(DR\) is the dynamic range, \(V_L\) is the maximum input linear range, and \(v_{in\text{- noise}}^2\) is the RMS input-referred noise. The input linear range \(V_L\) is usually calculated at 1\% or 5\% total harmonic distortion, \(THD\).

Tables 5.3 and 5.4 below present the simulated and calculated important parameter values related with the proposed topologies for (100-200) Hz and (5-10) kHz frequency bands respectively.
Table 5.3: The important simulation results related to the OTA-C band-pass filter topologies 1, 2, 3, and 4 at (100-200) Hz frequency band

<table>
<thead>
<tr>
<th>Topology</th>
<th>$I_{B1}$ (nA)</th>
<th>$I_{B2}$ (nA)</th>
<th>$I_{B3}$ (nA)</th>
<th>Power Consumed (nW)</th>
<th>Input-Referred Noise (µVrms)</th>
<th>$V_L$</th>
<th>$DR$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.45</td>
<td>1</td>
<td>0.45</td>
<td>11.7</td>
<td>340</td>
<td>±900</td>
<td>65.44</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>0.5</td>
<td>-</td>
<td>7.5</td>
<td>310</td>
<td>±900</td>
<td>66.24</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>0.25</td>
<td>-</td>
<td>6.75</td>
<td>375</td>
<td>±900</td>
<td>64.59</td>
</tr>
<tr>
<td>4</td>
<td>3.45</td>
<td>0.95</td>
<td>0.25</td>
<td>13.95</td>
<td>415</td>
<td>±900</td>
<td>63.71</td>
</tr>
</tbody>
</table>

Table 5.4: The Important simulation results related to the OTA-C band-pass filter topologies 1, 2, 3, and 4 at (5-10) kHz frequency band

<table>
<thead>
<tr>
<th>Topology</th>
<th>$I_{B1}$ (nA)</th>
<th>$I_{B2}$ (nA)</th>
<th>$I_{B3}$ (nA)</th>
<th>Power Consumed (nW)</th>
<th>Input-Referred Noise (µVrms)</th>
<th>$V_L$</th>
<th>$DR$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>155</td>
<td>20.5</td>
<td>1.4</td>
<td>530.7</td>
<td>345</td>
<td>±900</td>
<td>65.31</td>
</tr>
<tr>
<td>2</td>
<td>136</td>
<td>3.6</td>
<td>-</td>
<td>418.8</td>
<td>318</td>
<td>±900</td>
<td>66.02</td>
</tr>
<tr>
<td>3</td>
<td>133</td>
<td>3.6</td>
<td>-</td>
<td>409.8</td>
<td>385</td>
<td>±900</td>
<td>64.36</td>
</tr>
<tr>
<td>4</td>
<td>171</td>
<td>69</td>
<td>2</td>
<td>726</td>
<td>420</td>
<td>±900</td>
<td>63.6</td>
</tr>
</tbody>
</table>

From Tables 5.3 and 5.4 shown above, it can be seen that the proposed filters consume small power rates in the nW range, in both frequency bands. The dynamic range is always more than 63dB and can be extended further by increasing the capacitor...
values to reduce the thermal noise. However, this will be at the expense of increasing the filter size and increasing the power consumed to attain the bandwidth.

For the proposed OTA-C filters in this work, most of the increase in linear range is obtained as a result of using the simple capacitive attenuators. Using this technique increases the input-referred noise per unit bandwidth quadratically but reduces the bandwidth linearly. Therefore, a net linear increase in dynamic range is achieved due to the quadratic increase in signal maximum power versus linear increase in noise total power [5.4] as detailed later in section 5.6.1. The dynamic range of the proposed OTA-C filters is further increased due to the use of bumping MOSFETs that increase the linear range with a noise free cost as mentioned earlier in chapter four.

5.4.4 Realisation of the Proposed Filter Topologies 3 and 4

The input non-inverting node of $G_{m1}$ transconductors in topology 3 and the non-inverting nodes of $G_{m1}$ and $G_{m2}$ transconductors of topology 4, have no DC path to ground. This means that under normal operating conditions, they will be considered as floating nodes which will compromise stable operation. In order to cope with this difficulty, the standard MOSFETs in those inputs could be replaced with a 2-input floating gate MOSFET [5.5] or quasi-floating gate MOSFET [5.6] by biasing with $V_{DD}$ one of the gates “the bias gate”, and then applying the capacitive attenuated input signal to another gate “the input gate”.

One of the difficulties related with the use of the floating gate MOSFET as a signal processing device is the presence of residual charge, $Q_{FG}$ that may be trapped at its floating gate during its fabrication. Traditionally, there are well known techniques such as to adapt or release the charge by tunnelling, using UV light, or hot electron injection [5.7]-[5.10]. Unfortunately, such techniques need either additional circuitry, which increases the design complexity and circuit footprint, or post-fabrication
processing [5.11]. A new layout technique that makes use of the fabrication process itself is reported which erases this residual charge, hence producing a reliable floating gate MOSFET [5.12]. Therefore this technique is suggested to be used in future to realise the proposed filter topologies 3 and 4. This technique offers the fabrication of the floating gate MOSFET in a standard MOS technology, by leaving the gate of the MOSFET without any resistive connection. Then secondary gates are deposited above the floating gates which are solely capacitively connected to it, as detailed in [5.12].

5.5 Experimental Work

As detailed in chapter two, the test chip in figure 2.6, was fabricated in the AMS process using 0.35µm CMOS C35 Technology. The proposed filters of topologies 1 and 2 occupy areas of 74,400 µm$^2$ and 56,000 µm$^2$ respectively. Figures 5.13 and 5.14 show the measured frequency response and the noise spectrum graphs obtained experimentally together with their simulated counterparts from simulation which shown earlier in section 5.4.1parts 1 and 2.

5.5.1 Frequency Response

The measured frequency response of the proposed filter topologies 1 and 2 is obtained by the digital oscilloscope, DSO1024A. The simulated and measured frequency responses are included in the same graph and shown in Figures 5.13 and 5.14 below. The results are summarised in Tables 5.5 and 5.6 at the end of the next section.

It is important to note that the capacitors used in the proposed filters are the poly-Si type available in the 0.35µm CMOS Technology with an area percentage fluctuation of about (8 - 10) %. This area variation will be reflected as a variation of the frequency poles from their required values. However by slight tuning of the OTAs bias currents, the required frequency response can be obtained. Figures 5.13 and 5.14 show good
agreement between the simulated and measured frequency response of the proposed filter topologies, with comparable values of the measured bias currents needed to get the same frequency response with respect to their simulation counterparts.

Figure 5.13 Simulated and measured frequency response of the proposed (Topology 1) OTA-C band-pass filter
5.5.2 Noise

It is obtained using the digital oscilloscope, DSO1024A by measuring the filter output with no input signal. The Fourier transform of the filter output at no input signal represents the filter output noise spectrum. Figures, 5.15 and 5.16 show the measured RMS output voltage noise spectrum for the two extremes of the frequency bands (100-200) Hz and (5-10) kHz. They are placed in the same graph with those obtained from simulations which were presented above in section 5.4.2 (A). It is apparent that there is a small $1/f$ noise contribution in simulation, in the frequency band of (100-200) Hz. A larger contribution in simulation in the frequency band of (5-10) kHz is recognised. The flicker noise corner frequency values are 10Hz and 91Hz for (100-200) Hz and (5-10kHz).
Hz bands for topology 1 while those of topology 2 for the same bands were 7Hz and 82Hz respectively. In practice, higher bias currents of $I_{B1}$ and $I_{B2}$ are needed for both filter bands for both topologies than those used in simulation, so that the thermal noise floor is lowered, causing the $1/f$ corner frequency to increase for experimental noise results [5.13]. The flicker noise corner frequency values are 20Hz and 100Hz for (100-200) Hz and (5-10k) Hz bands for topology 1 and 10Hz and 85Hz for the same bands for topology 2. The measured integrated RMS input-referred noise values are lower than those obtained by simulation and calculations made in section 5.4.2(B). The measured integrated RMS values for the proposed topologies 1 and 2 in Tables 5.5 and 5.6 above, as expected close to those found by simulation and calculations. It is important to mention that one of the reasons for the small values of input-referred noise in all topologies, besides their appropriate sizing, is the small number of MOSFETs used to construct the proposed OTA.

![Figure 5.15 Measured and simulated output noise of the Topology 1 OTA-C band-pass filter for the (100-200) Hz and (5-10) kHz frequency bands](image-url)
Figure 5.16 Measured and simulated output noise of the Topology 2 OTA-C band-pass filter for the (100-200) Hz and (5-10) kHz frequency bands.

Tables 5.5 and 5.6 present the measured important parameter values related with topologies 1 and 2 for (100-200) Hz and (5-10) kHz frequency bands respectively.

Table 5.5: The important measured results related to the OTA-C band-pass filter topologies 1 and 2 at (100-200) Hz frequency band

<table>
<thead>
<tr>
<th>Topology</th>
<th>$I_{B1}$ (nA)</th>
<th>$I_{B2}$ (nA)</th>
<th>$I_{B3}$ (nA)</th>
<th>Power Consumed (nW)</th>
<th>Input- Referred Noise (µVrms)</th>
<th>$V_L$</th>
<th>DR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.5</td>
<td>1</td>
<td>0.5</td>
<td>12</td>
<td>335</td>
<td>±910</td>
<td>65.66</td>
</tr>
<tr>
<td>2</td>
<td>2.2</td>
<td>0.5</td>
<td>-</td>
<td>8.1</td>
<td>308</td>
<td>±910</td>
<td>66.39</td>
</tr>
</tbody>
</table>
Table 5.6: The important measured results related to the OTA-C band-pass filter topologies 1 and 2 at (5-10) kHz frequency band

<table>
<thead>
<tr>
<th>Topology</th>
<th>$I_{B1}$ (nA)</th>
<th>$I_{B2}$ (nA)</th>
<th>$I_{B3}$ (nA)</th>
<th>Power Consumed (nW)</th>
<th>Input- Referred Noise (μVrms)</th>
<th>$V_L$ (mV)</th>
<th>DR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>160</td>
<td>21.75</td>
<td>1.75</td>
<td>550.5</td>
<td>337</td>
<td>±920</td>
<td>65.7</td>
</tr>
<tr>
<td>2</td>
<td>139</td>
<td>3.65</td>
<td>-</td>
<td>427.95</td>
<td>310</td>
<td>±920</td>
<td>66.4</td>
</tr>
</tbody>
</table>

5.6 Input linear range increase effect on dynamic range

The relation between increasing the filter input linear on its dynamic range is discussed as follows

5.6.1 Linear range and frequency bandwidth of filter topologies

The relation between the input linear range, $V_L$ and the frequency bandwidth for the proposed OTA-C filters is expressed below.

1. For topology 1 as mentioned in section 5.2.1 above, the frequency bandwidth is governed by its three poles which determine the band-pass characteristics as follows

   I. From the transfer function in equation (5.4), the low frequency component representing high-pass characteristics is governed by the 1st pole, $p_1$ as follows
\[ p_1 = -\frac{G_{m1}}{aC_1 + C_A} = -\frac{G_{m1}}{C_{tot}} \]

where \( C_{tot} \) represents the total capacitance for this case. Therefore, \( p_1 \) is proportional to \( G_{m1} \) which is in turn expressed as \( I_B/V_L \) since the filter is operating within its linear input range limits. This means that \( p_1 \) is proportional to \( I_B/V_L \), that is, inversely proportional to \( V_L \).

II. The filter high frequency component representing its low-pass characteristics is governed by the \( s^{2}\text{nd} \) and \( s^{3}\text{rd} \) poles, \( p_{2,3} \) respectively as follows

\[
p_{2,3} = -\frac{G_{m2} - G_{m3}}{2(r(C_B + C_3) + C_B)} \pm \sqrt{\left(C_1(G_{m2} - G_{m3}) \right)^2 - 4\left(rC_1(C_B + C_3) + C_BC_3\right)G_{m2}G_{m3}} \]

\[
p_{2,3} = -\frac{G_{tot1}}{C_{tot1}} \]

where \( G_{tot1} \) and \( C_{tot1} \) represent the total transconductance and capacitance respectively for this case. The poles \( p_{2,3} \) are proportional to \( G_{tot} \). Hence \( p_{2,3} \) are inversely proportional to \( V_L \).

2. For topology 2 as mentioned in section 5.2.2 above, the frequency bandwidth is governed by two poles that determine the band-pass characteristics as follows

\[
p_{1,2} = -\frac{(G_{m1} - G_{m2})}{2(C(2 + r) + C_1(1 + r))} \pm \sqrt{\left(C_1(G_{m1} - G_{m2}) \right)^2 - 4\left(CC_1(2 + r) + C_1^2(1 + r)\right)G_{m1}G_{m2}} \]

\[
p_{1,2} = -\frac{G_{tot2}}{C_{tot2}} \]
where $G_{mtot2}$ and $C_{tot2}$ represent the total transconductance and capacitance respectively for this case. So, the poles $p_{1,2}$ are proportional to $G_{mtot2}$. Hence $p_{1,2}$ are inversely proportional to $V_L$.

From the above analysis, it can be concluded that the frequency bandwidths of the filter topologies 1 and 2, represented by their frequency poles, are inversely proportional to $V_L$. The same can be proven in the same manner, for filter topologies 3 and 4.

5.6.2 Dynamic range and the noise power

The OTA white, input-referred noise power per unit bandwidth mentioned in equation (4.16) earlier, was proportional to $V_L^2$. The filter bandwidth equations for all proposed OTA-C filter topologies are inversely proportional to $V_L$, so the white input-referred noise power becomes proportional to $V_L$. Therefore, the total input-referred noise power is proportional to $V_L$ when the white noise dominates over $1/f$ noise [5.4]. From the equation (5.42) for dynamic range, when increasing the filter linear range, $V_L$ the maximal signal power in the numerator will be scaled by $V_L^2$. On the other hand, the white noise power is scaled by $V_L$ since it proportional to $V_L$. Hence, the dynamic range of the filter is improved by $V_L$ in linear scale and by $10\log (V_L)$ in dB. In other words when the white noise is made to dominate over $1/f$ noise, the increase in linear range leads to increase the system dynamic range.

If $1/f$ noise is dominant, the total input-referred noise of equation (4.16) mentioned earlier is proportional to $V_L^2$, so that, any increase in the maximal signal power in the numerator of equation (5.42) is cancelled by the same increase of the $1/f$ noise. In other words, when the $1/f$ noise is dominant, increasing the linear range has no effect on improving the system dynamic range. Thus the careful MOSFET sizing is
necessary to ensure the dominance of white over $1/f$ noise. This leads to the improvement in system linear range, feasible for improving dynamic range.

### 5.6.3 Dynamic range and the filter frequency bandwidth

It is mentioned above that in each one of the proposed filter topologies, the frequency bandwidth is proportion to the transconductance represented by $I_B / V_L$. Therefore, the increase in the linear range, $V_L$ with a constant $I_B$ value, causes a reduction in the filter frequency bandwidth. Improving the linear range and in turn the dynamic range of a filter comes at the expense of reducing its frequency bandwidth. To cope with this difficulty, the bias current, $I_B$ value should be increased. Increasing $I_B$ does not affect the dynamic range for circuits with dominant white noise since it is independent of $I_B$. This means that the expenditure of more power is the price that should be paid when improving the filter dynamic range through increasing its $V_L$. For circuits with dominant $1/f$ noise, increasing $I_B$ will not improve the dynamic range since this will be cancelled with $1/f$ noise increase due to its dependence to $I_B$.

It is worth noting that the improvement in the input linear range of the proposed OTA compared to simple OTA is about 64 fold. Hence the improvement in dynamic range equals $10 \log_{10} 64$ which leads to 18dB.

### 5.7 The 4-channel filter bank

Early cochlear filter banks were made with serial connection by cascading the filter stages to increase their roll-off characteristics. This comes at the expense of increasing the system noise which is accumulated from one stage to another with the possibility of losing the system functionality. The parallel filter bank on the other hand overcomes the accumulation problems [5.20], so the parallel filter bank approach is adopted in this work. A 4-channel parallel OTA-C filter bank is constructed that consists of 4
individual stages (1, 2, 3, and 4) of topology 1 filters as shown in the block diagram in Figure 5.17 below.

The cochlear can be considered as the audio front-end in the biological auditory system and its frequency response has position dependence along the basilar membrane due to the change of its width and stiffness which cause changes in acoustic wave speed and consequently cause an exponential frequency variation.

![Block Diagram of the 4-Channel OTA-C Filter Bank Consisting of 4-Individual Parallel Stages of Topology 1 filters.](image-url)

Besides the benefit of obtaining low power consumption when the filter MOSFETs operate in sub-threshold regime, the current-voltage exponential relationship in this regime make them well-suited for cochlear applications. The exponential spread of the centre frequencies of the sequential filter stages constituting the filter bank is achieved by using thin poly-silicon wire as a long resistor and connected to bias...
voltages \((V_{B1A}, V_{B1B}, V_{B1C}, \text{ and } V_{B1D})\) with equal space intervals. Suitable tuning voltages are applied at the ends of the resistor. The same approach is adopted for the \((V_{B2A}, V_{B2B}, V_{B2C}, \text{ and } V_{B2D})\) bias voltages. Therefore the linear changes in bias voltage are provided which in turn, translate into exponential frequency changes since all the bias MOSFETs of the different filter stages are working in the sub-threshold regime as mentioned earlier in chapter one [1.27].

5.7.1 The Frequency Response

The filter bank is built on an area of \(329,700 \mu \text{m}^2\). The measured frequency response is shown in Figure 5.18 below

![Figure 5.18 Measured frequency response for the 4-channel OTA-C filter bank](image.png)
As expected, the frequency response shows an equal exponential spread of the frequency bands of its sequential stages.

### 5.8 Figure of Merit

For the electronic circuits used for biomedical applications, the most important parameters are power consumption, power supply voltage, rejection bands steepness, robustness and the dynamic range. Therefore a measure of the performance has been introduced [5.14] - [5.16] and is in common usage. It is referred to as the “Figure of Merit” (FOM) and defined as:

$$FOM = \frac{Power\ Consumed \cdot V_{DD}}{n \cdot f \cdot DR}$$

(5.43)

where $V_{DD}$, $n$, and $f$, are the power supply voltage, order of the filter, and the centre frequency or cut-off frequency for which the results are reported.

Table 5.7 below shows the figure of merit for the proposed filter topologies in this work, according to experimental results for topologies 1 and 2 and simulation results for topologies 3 and 4. The filter of topology 1 has the best value when working in the range (5-10) kHz. However, the filter of topology 2 offers figure of merit values close to that of topology 1 filter in both bands. The figure of merit for topology 3 shows a comparable value to that of topology 1 in (5-10) kHz frequency band and the best figure of merit in (100-200) Hz frequency band. The proposed topology 4 has the largest figure of merit in both frequency bands compared to the other proposed topologies.
Table 5.7: The figure of merit for the four proposed filter topologies in this work

<table>
<thead>
<tr>
<th>Topology</th>
<th>Order</th>
<th>FOM ((100-200)\text{Hz or 150Hz centre frequency})</th>
<th>FOM ((5-10)\text{kHz or 7.5kHz centre frequency})</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3</td>
<td>(9.13\times10^{-13})</td>
<td>(8.37\times10^{-13})</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>(9.15\times10^{-13})</td>
<td>(9.66\times10^{-13})</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>(7.82\times10^{-13})</td>
<td>(9.54\times10^{-13})</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>(10.9\times10^{-13})</td>
<td>(13.4\times10^{-13})</td>
</tr>
</tbody>
</table>

Table 5.8 shows the performance parameters which contribute to the figure of merit values for five different reported filter configurations, all of which work in the sub-threshold regime. The proposed filter topologies in this work are also included for comparison. The comparisons in Table 5.8 are based on experimental results.

Table 5.8: Comparison with other weak inversion topologies presented in literature (only those with experimental results are considered except topologies 3 and 4 in this work with their simulation results)

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Power Consumed</th>
<th>Power Supply</th>
<th>Order</th>
<th>Maximum Frequency</th>
<th>DR (dB)</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(W)</td>
<td>(V)</td>
<td></td>
<td>(Hz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[5.17]</td>
<td>114.8(\mu)</td>
<td>3</td>
<td>3</td>
<td>(\approx 100)</td>
<td>47.1</td>
<td>36(\times10^{-9})</td>
</tr>
<tr>
<td>[5.3 ]</td>
<td>230n</td>
<td>2.8</td>
<td>4</td>
<td>200</td>
<td>67.5</td>
<td>119(\times10^{-13})</td>
</tr>
<tr>
<td>[5.14]</td>
<td>68n</td>
<td>1</td>
<td>6</td>
<td>670</td>
<td>49</td>
<td>3.4(\times10^{-13})</td>
</tr>
<tr>
<td>This</td>
<td>12n</td>
<td>(\pm 1.5)</td>
<td>3</td>
<td>200</td>
<td>65.66</td>
<td>9.13(\times10^{-13})</td>
</tr>
<tr>
<td>work 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CHAPTER FIVE

The Proposed OTA-C Filters for Cochlear Implants

<table>
<thead>
<tr>
<th>Work</th>
<th>C Value</th>
<th>Tolerance</th>
<th>Resistor Value</th>
<th>Resistance</th>
<th>Gain</th>
<th>Figure of Merit</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work 2</td>
<td>$8.1\times10^{-11}$</td>
<td>$\pm 1.5$</td>
<td>200</td>
<td>66.39</td>
<td>$9.15\times10^{-13}$</td>
<td></td>
</tr>
<tr>
<td>This work 3</td>
<td>$6.75\times10^{-11}$</td>
<td>$\pm 1.5$</td>
<td>200</td>
<td>64.59</td>
<td>$7.82\times10^{-13}$</td>
<td></td>
</tr>
<tr>
<td>This work 4</td>
<td>$13.95\times10^{-11}$</td>
<td>$\pm 1.5$</td>
<td>200</td>
<td>63.71</td>
<td>$10.9\times10^{-13}$</td>
<td></td>
</tr>
<tr>
<td>[5.18]</td>
<td>$2\mu\text{F}$</td>
<td>1.25</td>
<td>2</td>
<td>2k</td>
<td>78</td>
<td>$80\times10^{-13}$</td>
</tr>
<tr>
<td>[5.3]</td>
<td>$6.36\mu\text{F}$</td>
<td>2.8</td>
<td>4</td>
<td>10k</td>
<td>65</td>
<td>$68\times10^{-13}$</td>
</tr>
<tr>
<td>[5.19]</td>
<td>$2\mu\text{F}$</td>
<td>1</td>
<td>2</td>
<td>40k</td>
<td>45</td>
<td>$55\times10^{-13}$</td>
</tr>
<tr>
<td>This work 1</td>
<td>$550.5\times10^{-12}$</td>
<td>$\pm 1.5$</td>
<td>10k</td>
<td>65.7</td>
<td>$8.37\times10^{-13}$</td>
<td></td>
</tr>
<tr>
<td>This work 2</td>
<td>$427.95\times10^{-12}$</td>
<td>$\pm 1.5$</td>
<td>10k</td>
<td>66.4</td>
<td>$9.66\times10^{-13}$</td>
<td></td>
</tr>
<tr>
<td>This work 3</td>
<td>$409.8\times10^{-12}$</td>
<td>$\pm 1.5$</td>
<td>10k</td>
<td>64.36</td>
<td>$9.54\times10^{-13}$</td>
<td></td>
</tr>
<tr>
<td>This work 4</td>
<td>$726\times10^{-12}$</td>
<td>$\pm 1.5$</td>
<td>10k</td>
<td>63.6</td>
<td>$13.4\times10^{-13}$</td>
<td></td>
</tr>
</tbody>
</table>

From Table 5.8, it is clearly shown that the proposed filters have the best figure of merit values compared to all other configurations except one reported in [5.14]. The filter in [5.14] has a very small figure of merit which means it has the best figure of merit. It has an excellent performance as a band-pass filter used in biomedical applications such as a wearable acoustic-based breathing detector. However, it fails in other biomedical applications as the cochlear implants since it has a dynamic range of 49 dB which is much less than that required for such applications besides its limited input range represented by only a 40mVpp. Therefore, the four proposed filters in this work have good figure of merit values for filters to be used in cochlear implants.
5.9 Conclusion

The design and the performance of topologies of OTA-C filters for cochlear implants applications are discussed in this chapter.

Four OTA-C filter topologies are proposed, their transfer functions are derived, and their performances are simulated. Two of topologies (topologies 1 and 2) have been fabricated and measured experimentally. The performance parameters show good agreement in both simulated and measured cases. The experimental results show dynamic range values of 65dB and 66dB for topologies 1 and 2 respectively. Relatively small power consumption in nW range for all topologies is obtained while providing frequencies from 100 Hz up to 10 kHz which required for cochlear implants applications. The figure of merit which represents a measure of how good the overall filter performance in terms of the most important performance parameters is calculated and tested and compared with values reported by other researchers for other filter topologies. The results presented here are shown to be better or competitive with the literature reports, particularly for topologies 1 and 2.

References


CHAPTER SIX

Proposed OTA-C Filter for EEG Applications

6.1 Introduction

Electroencephalography, EEG is an important tool to record the electrical activity produced by the brain. Four bands of brain waves, δ (1–4) Hz, θ (4–8) Hz, α (8–12) Hz, and β (13–40) Hz, constitute the EEG signals. Their measured data are used for clinical and research purposes ranging from individual normal activity diagnostics such as sleeping, writing, eye closing, anxious thinking, disease diagnostics, for instance, epilepsy and also extending to brain-computer interfacing [6.1]. The EEG signals represent a variation of the surface potential distribution on the scalp which reflects human functional activities. Those signals can be measured by electrodes which are placed on the scalp, and they typically operate within a small range of voltages of (2–200) µV [6.2]. Integrated circuit solutions become very attractive for the multi-channel, future portable EEG systems [6.3], [6.4]. Achieving discrete and lightweight devices is important and also favourable for EEG applications.

6.2 Design Details

6.2.1 Specifications

The challenges for the realisation of some biomedical applications such as cochlear implants as in chapter five earlier, are to increase the input linear range whilst achieving a dynamic range of not less than 60dB. This needs to be satisfied with
minimum power consumption in the micro-watts range. For other biomedical applications like EEG systems, the priority is on reducing the power consumption that is essential for wearable EEG. This is together with the need to reduce the filter transition bands and noise as EEG signals have very small frequency bands and voltage amplitudes. Therefore, for the very low frequency bands, the filter transition bands should be sharp. Also their small amplitudes impose the need to design filters with a small noise floor, much less than input signal amplitudes. The design of filters with large time constants requires that OTA transconductance should be very small or the capacitor value large. The latter implies large dimensions which are not acceptable for on-chip systems. Therefore the basic approach for obtaining a good EEG filter is to decrease the transconductance of the OTA. Most of the previously reported OTAs employ complex architectures to meet this goal. In this work the proposed OTA is a simple differential OTA operating in deep weak-inversion region with bumping MOSFETs. Such architecture serves to minimise noise since the effective noise sources occur are only four represented by the input and the current mirror MOSFETs. The simple OTA has a limited linear range \[6.5\]. Thus bumping MOSFETs serve to increase the input linear range by decreasing the transconductance, with a free noise cost.

6.2.2 MOSFET Sizing

The sizing of transistors for analogue applications is considered to be a compromise between mismatch and bandwidth. To overcome or at least reduce the transistor mismatch by increasing its dimensions, leads to an increase in parasitic capacitances which serve to reduce bandwidth. The bandwidth is further reduced due to the low bias currents required to detect the low-frequency EEG signals. OTA-C filters with capacitors of a few pico farads require bias currents in the pico-ampere range, to obtain the low-frequency EEG signals. The MOSFET transfer characteristics need to be obtained to assess operating levels. The transfer characteristics for ten MOSFETs with 12µm by 12µm are measured experimentally using the Semiconductor Parameter
CHAPTER SIX

The Proposed OTA-C Filter for EEG Applications

Analyzer 4155B. Those MOSFETs are within the three groups of MOSFETs in middle, left and right sides of the test chip shown earlier in figure 2.6. Figure 6.1 presents the mean curve for those ten MOSFETs together with the results of simulation using BSIM3v3 models with the parameters shown earlier in Table 2.1. From Figure 6.1, it is apparent that the leakage current level is in the order of femto-amperes. Therefore the on-chip current in pico-ampere range starting from 1pA can be used for biasing the OTA-C filter to achieve EEG signals. In this work a value of 10pA is chosen to be the minimum bias current used. The measured curve shows a good agreement with the simulation. The values of sub-threshold swing, $S$ and threshold voltage, $V_{TH}$ are obtained as shown in Table 6.1 for both curves.

![Graph showing measured and simulated transfer characteristic for MOSFETs with $W=12\mu m$, $L=12\mu m$ and $V_{DS}=0.1V$](image)

Figure 6.1 Measured and simulated transfer characteristic for MOSFETs with $W=12\mu m$, $L=12\mu m$ and $V_{DS}=0.1V$
Table 6.1: The sub-threshold swing and threshold voltage for figures 6.1 with the error

<table>
<thead>
<tr>
<th>Figure</th>
<th>$S_{Simulated}$ (mV/dec.)</th>
<th>$S_{Measured}$ (mV/dec.)</th>
<th>Error in $S$ (%)</th>
<th>$V_{TH_{Simulated}}$ (mV)</th>
<th>$V_{TH_{Measured}}$ (mV)</th>
<th>Error in $V_{TH}$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1</td>
<td>80</td>
<td>81.2</td>
<td>1.5</td>
<td>490</td>
<td>497</td>
<td>1.43</td>
</tr>
</tbody>
</table>

The measured values of the sub-threshold swing and threshold voltage are comparable to those of simulation as in Table 6.1 above. This leads to relatively small errors obtained. The proposed OTA for EEG applications is similar to that of figure 3.3. It is important to guarantee the correct biasing of the current sink MOSFET, M7 in the proposed OTA in such low range of currents. Therefore, the MOSFET, M8 is connected as in Figure 6.2 below to eliminate the possibility of the junction leakage currents effect in deep weak inversion region. It is worth noting that the dimensions of MOSFETs of the proposed OTA of Figure 6.2 are obtained using $g_m/I_D$ methodology and the results are shown in Table 6.2 below frequency band is feasible.
Figure 6.2 Proposed OTA for EEG applications

Table 6.2: The dimensions of MOSFETs of the proposed OTA

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>$g_m/I_D$</th>
<th>$I_D$</th>
<th>W/L</th>
<th>W (µm)</th>
<th>L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>28</td>
<td>65</td>
<td>1</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>M3, M4</td>
<td>28.2</td>
<td>65</td>
<td>1</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>M5, M6</td>
<td>28.1</td>
<td>65</td>
<td>2</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>M7, M8</td>
<td>27.8</td>
<td>195</td>
<td>1</td>
<td>12</td>
<td>12</td>
</tr>
</tbody>
</table>
From Table 6.2 above it can be seen that the MOSFETs operate at the highest values of $g_m/I_D$ along the $g_m/I_D$ versus $I_D/(W/L)$ curve of figure 3.6. This shows the operation in the deep weak inversion region. The operation in such region according to figure 3.6 implies small values of aspect ratio of about unity or less to maintain the very small values of $I_D$. For this reason the aspect ratios "$W/L$" of OTA MOSFETs are 1 except that of bumping MOSFETs to ensure their proper operation. This leads to a decrease in value of the normalized current, $I_N$ in $g_m/I_D$ versus $I_N$ curve since $I_D$ is kept unchanged. In other words, the bumping MOSFETs will operate at a higher value of $g_m/I_D$ compared to other NMOSFETs.

The proposed OTA with MOSFET dimensions of Table 6.2 above was simulated to obtain its frequency bandwidth. The frequency response of the proposed transconductor, OTA shows a 281 Hz transition frequency, $f_T$ at -3dB as in Figure 6.3. The bias current was 10pA. This bandwidth is more than two orders of magnitude above the centre frequency of the largest EEG range of 26.5Hz for the $\beta$ band of (13-40) Hz range. So, the operation of the proposed OTA with very low current levels starting from 10pA provides a suitable bandwidth for EEG applications. Thus, the OTA-C filter with very small bias currents for obtaining the EEG bands without distortion in the filtered frequency bands is feasible.
6.2.3 The operation of MOSFETs in deep weak inversion region

For such low power and low frequency applications, the use of very low current cannot be avoided to get the required frequency bands with relatively small capacitor values as mentioned earlier. This requires the operation of filter MOSFETs in the deep weak inversion region as presented in Table 6.2. The challenges of operating OTAs at very low bias currents relate to current mismatch, bandwidth trade-off and noise as discussed below.

Figure 6.3 Simulated frequency response of the proposed OTA showing its transition frequency, $f_T$ at 10pA bias current
1. Mismatch and bandwidth

The current matching of transistors with nominally the same dimensions is worse when they are operating in the weak inversion region than that of strong inversion [6.6], [6.7]. In the case of MOSFET operation in deep weak inversion region, there is no significant decrease in matching from that in weak inversion.

As mentioned above, the measured curve in Figure 6.1 presents the mean curve for ten MOSFETs spread at left, middle, and right sides of the chip. The current mismatch among transfer characteristics of those MOSFETs is found to be 2.2% in the sub-threshold regime. From Figure 6.3, the transition frequency, $f_T$ of the proposed OTA at 10pA exceeds the required centre frequency of the largest EEG band by more than two decades. So, adopting the $g_m/I_D$ methodology in sizing MOSFETs of the proposed OTA gives a good compromise in the current mismatch and bandwidth issue.

2. Noise

It is essential to reduce the noise effect for EEG applications; otherwise the input signals can not be distinguished from noise. A simple OTA architecture results in lower noise because of the small number of effective noise sources. Using a high-order filter topology increases the sharpness of the filter frequency response. At such low frequencies especially for the $\delta$ signal band with a centre frequency of only 2.5 Hz, flicker, or “1/f” noise is expected to be severe. However, in this work the filter operation in the deep weak inversion region ultimately reduces this noise since the corner frequency, $f_c$ can be made very low [6.8] and outside the frequency band.

The design approach for the proposed OTA for EEG applications in this work can be summarised as follows
I. Utilise MOSFET operation in deep weak inversion region with small bias current levels in the pico-amperes range. This serves to greatly reduce the effect of 1/f noise since the associated corner frequency can be made very small. Therefore the 1/f noise will be outside the EEG signal bands which will be affected solely by the white “thermal” noise.

II. Proposing an OTA architecture consisting of a simple differential structure with bumpsing MOSFETs. This OTA has a small number of shot noise sources in order to reduce the white noise.

III. Adopting the $g_m/I_D$ methodology in sizing MOSFETs of the proposed OTA. This methodology is useful to solve the current mismatch-bandwidth trade-off issue related with the operation at very small biasing current levels.

6.3 The OTA-C band-pass filters for EEG

The circuits needed for processing of biological signals are can be considered as a good example of small-size and low-power building blocks. Many topologies of low power integrated EEG front-end amplifiers have been designed and reported as summarised below

6.3.1 Design approaches

In general there are two main approaches for obtaining EEG signals. The first one is represented by the design of a low-pass notch filter with a cut-off frequency as required for such applications. In this case, it is 40 Hz with a notch close to that frequency to increase the sharpness of the filter roll-off. In such designs, LC ladder topologies are commonly used. All filter OTAs are biased with the same current to provide the needed cut-off frequency. The other required specifications are satisfied by the appropriate choice of capacitor values. The different capacitor values are obtained
from design tables according to the filter order and the gain gradient that depends on the cut-off and notch frequencies. Then those capacitor values which are normalised for a unity frequency are converted to produce the required cut-off frequency [6.2], [6.9]. The second approach involves design of band-pass filters to extract each EEG frequency band separately [6.10]. Many topologies can be used in this approach. The filters OTAs are biased with different currents in accordance to the required centre frequency and bandwidth with capacitor values chosen to achieve the required frequency bands.

6.3.2 The OTA-C filter in this work

In this work, the OTA-C band-pass filter topology [6.11] shown in Figure 6.4 below is adopted for EEG signals extraction. It represents an RLC circuit expressed by the OTA-C filter configuration. The resistor is represented by the transconductor $G_{m1}$ with its output connected to its inverting input terminal. The gyrator consisting of transconductors $G_{m2}$ and $G_{m3}$ with a capacitor $C_2$ representing the inductor. The circuit capacitor is represented by $C_f$. It is worth noting that the band-pass action is obtained at the output node, $V_{out}$ due to the contribution of the transconductors $G_{m2}$ and $G_{m3}$ while at node $X$, the low-pass effect appears due to transconductor $G_{m2}$ action.
1. Transfer function derivation

As in previous chapter, the nodal equations are adopted to obtain the transfer function for OTA-C filter for EEG applications of Figure 6.4 as follows

I. For $G_{m1}$

$$I_{O1} = (V_{in} - V_{out})G_{m1} = V_{out}C_1 - I_{O3} + I_{G2}$$

$I_{G2}$ for the OTA “$G_{m2}$” = 0 and also it is the case for all other OTAs

$$I_{O1} = (V_{in} - V_{out})G_{m1} = V_{out}C_1 - (V_x G_{m3})$$

(6.1)
II. Node X

For node X, apply Kirchhoff’s current law, KCL at each node gives the summation of currents around node X=0 to obtain

\[ V_x sC_2 - I_{o2} + I_{o3} = 0 \]
\[ V_x sC_2 = -V_{out} G_{m2} \]
\[ V_x = -V_{out} \frac{G_{m2}}{sC_2} \tag{6.2} \]

Substituting equation (6.2) in equation (6.1) gives

\[ V_{in} G_{m1} - V_{out} G_{m1} = V_{out} sC_1 - \left( -V_{out} \frac{G_{m2}}{sC_2} \right) G_{m3} \]
\[ V_{in} G_{m1} = V_{out} G_{m1} + V_{out} sC_1 + V_{out} \frac{G_{m2} G_{m3}}{sC_2} \]
\[ V_{in} G_{m1} = V_{out} \left( G_{m1} + sC_1 + \frac{G_{m2} G_{m3}}{sC_2} \right) \]
\[ V_{in} G_{m1} = V_{out} \left( \frac{sC_2 G_{m1} + s^2 C_1 C_2 + G_{m2} G_{m3}}{sC_2} \right) \]
\[ V_{in} G_{m1} sC_2 = V_{out} \left( sC_2 G_{m1} + s^2 C_1 C_2 + G_{m2} G_{m3} \right) \]
\[ H(s) = \frac{V_{out}}{V_{in}} = \frac{sC_2 G_{m1}}{s^2 C_1 C_2 + sC_2 G_{m1} + G_{m2} G_{m3}} \tag{6.3} \]
2. Finding the filter centre frequency and quality factor

It can be seen from the transfer function of (6.3) that the RLC OTA-C band-pass filter has a zero at the origin. The denominator is a $2^{nd}$ order equation which is always stable since its roots or “filter poles” are always in the left hand side of the s-plane. The transfer function in equation (6.3) is compared with the standard form of the $2^{nd}$ order system. So, the centre frequency, $\omega_0$ and -3dB quality factor, $Q_{-3dB}$ equations are obtained as in equations (6.4) and (6.5) respectively. They can be tuned by changing the filter transconductances to obtain the required frequency band.

$$\omega_0 = \sqrt{\frac{G_{m2}G_{m3}}{C_1C_2}}$$  \hspace{1cm} \text{(6.4)}

$$Q_{-3dB} = \sqrt{\frac{G_{m2}G_{m3}}{G_{m1}}}$$ \hspace{1cm} \text{(6.5)}

For such applications, it is important to get sharp transition bands since signals have small frequency bands. Therefore, the proposed filter is made a $4^{th}$ order band-pass filter consisting of two cascaded stages of the filter represented by the transfer function in (6.3) above. The block diagram of the proposed filter is shown in Figure 6.5 below.

![Block diagram of the proposed OTA-C filter for EEG applications](image-url)
6.4 Simulation Results

As in chapter five, the simulations are conducted in the Cadence environment using SpectreS with BSIM3v3.1 models and parameters from the AMS process for 0.35µm CMOS C35 Technology. It is important to point out that the simulation parameters including flicker coefficients $K_{Fn}$, $K_{Fp}$, and $C_{OX}$ for NMOS and PMOS transistors supplied by AMS are mentioned earlier in chapter two in Table 2.1. The simulations are performed to obtain the frequency response and the noise spectra for the OTA-C band-pass filter. The supply voltage and the values of capacitors used are:

Supply voltage= ±1.5 V.

$C_1 = 8$ pF and $C_2 = 8$ pF.

6.4.1 The Frequency Response

The frequency response for the proposed OTA-C band-pass filter of Figure 6.5 is obtained by simulation as in Figure 6.6 below.
Figure 6.6 Simulated frequency response of the OTA-C filter for EEG signals

The simulated frequency response shows the four EEG signals with their required bandwidths, and equal transition band slopes for their leading and trailing edges respectively.

Due to the expected variability in threshold voltage, the current values can change in accordance. So, some deviation in frequency response is expected due to such variations. The deviation percentage of 3% in the centre frequencies of the EEG bands is obtained as in Figure 6.7 below. The frequency and gain scales in Figure 6.7 are reduced to zoom in the frequency response to make such deviations clearer.

Table 6.3 below presents the simulated important parameter values related with the OTA-C filter for all EEG frequency bands.
Figure 6.7 Simulated frequency response of the OTA-C filter for EEG signals for nominal (straight lines) and deviation (dashed lines) cases

Table 6.3: The important simulated results related to the OTA-C band-pass filter

<table>
<thead>
<tr>
<th>EEG band</th>
<th>$I_{B1}$ (pA)</th>
<th>$I_{B2}$ (pA)</th>
<th>$I_{B3}$ (pA)</th>
<th>Total Power Cons. (pW)</th>
<th>Input-referred Noise (µVrms)</th>
<th>$V_L$ (mV)</th>
<th>$THD$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\delta$</td>
<td>15</td>
<td>10</td>
<td>10</td>
<td>210</td>
<td>50</td>
<td>$\pm26$</td>
<td>51.3</td>
</tr>
<tr>
<td>$\theta$</td>
<td>25</td>
<td>30</td>
<td>30</td>
<td>510</td>
<td>50</td>
<td>$\pm26$</td>
<td>51.3</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>45</td>
<td>52</td>
<td>52</td>
<td>894</td>
<td>50</td>
<td>$\pm26$</td>
<td>51.3</td>
</tr>
<tr>
<td>$\beta$</td>
<td>187</td>
<td>113</td>
<td>113</td>
<td>2478</td>
<td>50</td>
<td>$\pm26$</td>
<td>51.3</td>
</tr>
</tbody>
</table>
6.4.2 Noise

Figure 6.8 shows the simulated noise spectrum of the output node for the EEG signals. At such low frequencies, the contribution of $1/f$ noise is present and expected to dominate over thermal noise. However, the white, thermal noise is still seen to dominate because of the use of very low bias currents, appropriate transistor sizing, and adoption of a suitable filter topology. The OTA-C filter explained in section 6.3 above consists of three transconductors, two of which ($G_{m1}$ and $G_{m3}$) have band-pass action which further reduces the $1/f$ noise effect. Most of the $1/f$ noise appears in the very small frequencies of $<1$Hz of Figure 6.8 comes from the transconductor $G_{m2}$ due to its low-pass contribution to the filter output.

As mentioned in chapter four, the $1/f$ corner frequency represents the intersection frequency between $1/f$ and thermal noise. It is usually beneficial and for such applications is essential, to reduce the corner frequency to dominate white over $1/f$ noise. This ensures low noise in the frequency band of interest. From Figure 6.8, the thermal noise floor is reduced when the bias current is increased. Hence, the $1/f$ corner frequency increases but still outside of the frequency bands of interest.

The scale in the noise level axis in Figure 6.8 and also in Figure 6.10 below is chosen to be linear for two reasons. The first one is to show the proportion between bias currents and the $1/f$ corner frequency and secondly, to show the inverse proportion between bias currents and the thermal noise floor.

As in chapter five, the input referred voltage noise due to each transconductor is as follows

$$v_{in,proposed}^2 = \frac{8}{3} \frac{qI_B}{G_m^2} = 4 \frac{qV_T^2}{I_B}$$
The OTA-C filter total integrated noise for each filter stage is calculated as follows

\[ v_{noise}^2(s) = v_{noise1}^2(s) + v_{noise2}^2(s) + v_{noise3}^2(s) \]

\[ v_{noise1}^2(s) = 4 \frac{qV_L^2}{I_B} H^2(s) \]  \hspace{1cm} (6.6)

\[ v_{noise2}^2(s) = 4 \frac{qV_L^2}{I_B} \left( \frac{G_{m2}(sC_1 - G_{m1})}{s^2C_1C_2 + sC_2G_{m1} + G_{m2}G_{m3}} \right)^2 \]  \hspace{1cm} (6.7)

\[ v_{noise3}^2(s) = 4 \frac{qV_L^2}{I_B} \left( \frac{V_{out}}{V_X} \right)^2 \]  \hspace{1cm} (6.8)

Then, the total integrated noise for both stages equals

\[ v_{noise\text{total}}^2(s) = v_{noise\text{Stage1}}^2(s) + v_{noise\text{Stage2}}^2(s) \]  \hspace{1cm} (6.9)
Figure 6.8 Simulated noise of the OTA-C band-pass filter for EEG signals

6.5 Experimental Work

The proposed OTA-C filter is included on the test chip of figure 2.6. It occupies an area of 210,000 µm². Figures 6.8 and 6.9 show the measured frequency response and the noise spectra obtained experimentally. The following experimental results represent the mean values of ten different test chips of identical architecture.

6.5.1 The Frequency Response

The frequency response for the proposed OTA-C band-pass filter of Figure 6.5 is obtained using the digital oscilloscope, DSO1024A. The measured frequency response is shown in Figure 6.9 below
The measured frequency response of Figure 6.9 above as expected has comparable EEG frequency bands to those of simulation. As mentioned above each experimental result represents the mean of ten measurements. The standard deviation of the centre frequencies of EEG bands is obtained for the experimental results of the ten test chips. It equals to 2.1%, 2.1%, 2%, and 1.9% for δ, θ, α, and β bands respectively.

6.5.2 Noise

The measured noise spectrum at the filter output is shown in Figure 6.8. It is obtained using the digital oscilloscope, DSO1024A by measuring the Fourier transform of the filter output with no input signal.
Figure 6.10 Measured noise of the OTA-C band-pass filter for EEG signals

Table 6.4 shows the $1/f$ noise corner frequency values for the simulated and measured EEG bands noise curves. From figures 6.7 and 6.9 it obvious that the white noise dominates for all frequencies $\geq 1$Hz. Therefore, there is no $1/f$ noise contribution in any EEG filtered band.
Table 6.4: The $1/f$ noise corner frequency values for EEG bands

<table>
<thead>
<tr>
<th>EEG band</th>
<th>$f_c$ simulation (Hz)</th>
<th>$f_c$ Measured (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\delta$</td>
<td>0.075</td>
<td>0.07</td>
</tr>
<tr>
<td>$\theta$</td>
<td>0.15</td>
<td>0.14</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>0.3</td>
<td>0.28</td>
</tr>
<tr>
<td>$\beta$</td>
<td>0.62</td>
<td>0.6</td>
</tr>
</tbody>
</table>

Usually it is preferable to use PMOSFETs in such applications since their flicker noise is much less than that of NMOSFETs. However, the circuit is designed such that the flicker noise is outside the EEG signal bands so that white noise is dominant. Furthermore, the use of NMOSFETs is more suitable because of the lower threshold voltages. This feature makes NMOSFETs more attractive for future applications with increasingly need to use small size batteries of less than one volt supply. Table 6.5 presents the measured important parameter values related to the OTA-C filter for all EEG frequency bands.

Table 6.5: The important measured results related to the OTA-C band-pass filter

<table>
<thead>
<tr>
<th>EEG band</th>
<th>$I_{B1}$ (pA)</th>
<th>$I_{B2}$ (pA)</th>
<th>$I_{B3}$ (pA)</th>
<th>Total Power Cons. (pW)</th>
<th>Input-referred Noise (µVrms)</th>
<th>$V_L$ (mV)</th>
<th>$1%$ THD</th>
<th>DR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\delta$</td>
<td>17</td>
<td>10</td>
<td>10</td>
<td>222</td>
<td>48</td>
<td>±28</td>
<td>52.3</td>
<td></td>
</tr>
<tr>
<td>$\theta$</td>
<td>27</td>
<td>31</td>
<td>31</td>
<td>534</td>
<td>48</td>
<td>±28</td>
<td>52.3</td>
<td></td>
</tr>
<tr>
<td>$\alpha$</td>
<td>47</td>
<td>55</td>
<td>55</td>
<td>942</td>
<td>48</td>
<td>±29</td>
<td>52.6</td>
<td></td>
</tr>
<tr>
<td>$\beta$</td>
<td>190</td>
<td>115</td>
<td>115</td>
<td>2520</td>
<td>48</td>
<td>±29</td>
<td>52.6</td>
<td></td>
</tr>
</tbody>
</table>
It is clear from tables 6.3 and 6.5 that there are some differences in bias current values between experimentally measured and simulation cases used to provide the required frequency bands. These differences are due to threshold voltage variability. Noise, $V_L$, and $DR$ values are close to each other for both simulation and experimental cases, as expected.

### 6.6 Figure of Merit for the OTA-C Filter

The figure of merit for the OTA-C filter is calculated for the measured results of all EEG signal bands as shown in Table 6.6 below, utilising equation (5.43) mentioned in chapter five.

<table>
<thead>
<tr>
<th>EEG band</th>
<th>$FOM$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\delta$</td>
<td>$12.73 \times 10^{13}$</td>
</tr>
<tr>
<td>$\theta$</td>
<td>$11.78 \times 10^{13}$</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>$12.79 \times 10^{13}$</td>
</tr>
<tr>
<td>$\beta$</td>
<td>$13.3 \times 10^{13}$</td>
</tr>
</tbody>
</table>

Table 6.7 shows the experimental performance parameters used in constructing the figure of merit and its values for five different filter configurations. The configurations mentioned work in weak inversion regime with low centre frequencies of less than 100 Hz besides those obtained for the proposed OTA-C filter in this chapter.
Table 6.7: Comparison with other weak inversion topologies presented in literature

<table>
<thead>
<tr>
<th>Filter Topology</th>
<th>Power Cons. (W)</th>
<th>Power Supply (V)</th>
<th>Order</th>
<th>Centre frequency (Hz)</th>
<th>DR (dB)</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>[6.12]</td>
<td>28µ</td>
<td>3</td>
<td>4</td>
<td>0.1</td>
<td>64.6</td>
<td>3.9×10^{-7}</td>
</tr>
<tr>
<td>[6.13]</td>
<td>60p</td>
<td>1</td>
<td>7</td>
<td>2</td>
<td>43</td>
<td>1×10^{-13}</td>
</tr>
<tr>
<td>[6.2]</td>
<td>11 µ</td>
<td>±1.5</td>
<td>5</td>
<td>37</td>
<td>57</td>
<td>3.12×10^{9}</td>
</tr>
<tr>
<td>[6.14]</td>
<td>8.8n</td>
<td>1.8</td>
<td>3</td>
<td>50</td>
<td>62</td>
<td>17.1×10^{13}</td>
</tr>
<tr>
<td>[6.15]</td>
<td>290n</td>
<td>1.8</td>
<td>4</td>
<td>75</td>
<td>51</td>
<td>341×10^{13}</td>
</tr>
<tr>
<td>This work δ</td>
<td>222p</td>
<td>±1.5</td>
<td>4</td>
<td>2.5</td>
<td>52.3</td>
<td>13.76×10^{13}</td>
</tr>
<tr>
<td>This work θ</td>
<td>534p</td>
<td>±1.5</td>
<td>4</td>
<td>6.5</td>
<td>52.3</td>
<td>11.78×10^{13}</td>
</tr>
<tr>
<td>This work α</td>
<td>942p</td>
<td>±1.5</td>
<td>4</td>
<td>10.5</td>
<td>52.6</td>
<td>12.79×10^{13}</td>
</tr>
<tr>
<td>This work β</td>
<td>2520p</td>
<td>±1.5</td>
<td>4</td>
<td>27</td>
<td>52.6</td>
<td>13.3×10^{13}</td>
</tr>
</tbody>
</table>

It should be noted that the power supplies of ±1.5V are considered to be 3V when calculating the figure of merit values.

From Table 6.7, the figure of merit values obtained in this work are the best among the other reported filters except that mentioned in [6.13]. The reason is represented by the very low power consumption due to the use of a 1V supply voltage and also the higher order filter used in [6.13]. It is important to mention that the filter of [6.13] represents the most recent work which has the best figure of merit until the date of writing the thesis. In future, this work will focus on proposing or adopting a filter topology with higher order for very sharp transition bands. Also, the operation with very small current...
levels will continue to reduce the consumed power. The very low current operation permits using a supply voltage of 1V to reduce the figure of merit value compared to ±1.5V supply according to equation (5.43). This can facilitate realising a filter with a better figure of merit than that reported in [6.13].

6.7 Conclusion

A simple differential OTA with bumping MOSFETs was proposed and used in the design of an OTA-C band-pass filter for EEG applications. The simplicity of the OTA architecture used offers the benefits of reducing circuit complexity and noise. Using very small on-chip currents starting from 10pA, allowed the reduction of $1/f$ noise by reducing the corner frequency, and power consumption. The filter size was also reduced. These attributes make the design suitable for the new generation of EEG systems. In this work, a 4th order OTA-C filter for EEG applications was proposed, simulated and tested experimentally with comparable measured results to those of simulation. The experimental results shown were the mean of ten different test chips results and are comparable to that of simulation. The measured frequency response showed deviations of centre frequencies of about 2% from those of simulation. The noise results showed the dominance of white noise in all frequencies of interest, in agreement with the design specifications. The figure of merit was calculated from the experimental results for the four EEG bands and showed acceptable values compared to other filters, except that reported in [6.13]. In future, the work should continue to reduce the power consumption, the supply voltage, and increase the filter order to obtain a better figure of merit than that in [6.13] which has the best value till the date of writing this thesis.
References


CHAPTER SEVEN

Conclusions and Further Work

This chapter is divided into two parts; conclusions and suggestions for further work. The 1st part constitutes a summary and discussion of the important points related to the features, design specifications, results of the biomedical circuits, and applications chosen in this work. The 2nd part outlines two suggestions recommended for future study.

7.1 Conclusions

The thesis has described study and research into electronic circuits for fields of applications characterised by its low-voltage operation and low-power consumption. These biomedical applications represent a very important research field since they are directly related with an individual’s health. This work focused on the areas of cochlear implants and EEG signals. The proposed OTA-C filters are suitable for fully implanted future cochlear implants and EEG systems. The important aspects of the cochlear implants and EEG applications and the important points related to design and results are presented as follows:

7.1.1 Cochlear Implants

The biological cochlea has the function of processing input acoustic signals. It can be thought as the frequency analysing and extraction unit in the biological auditory system. It is responsible for providing the auditory nerves with the proper stimulations. This represents the different analysed acoustic signals in terms of their frequency...
components with amplitude features. For that reason, deficiencies related with cochlea cause severe hearing problems and even profound deafness.

Amongst the hearing aids technologies, the cochlear implant is the most sophisticated one. The OTA-C filter is the key building block of the cochlear implant. The design specifications of those filters for such application can be summarised by the following

1. Low power consumption to provide long time operation.
2. Low voltage operation enabling use of low size batteries.
3. High dynamic range operation.
4. Suitable filter topology with suitable frequency response.
5. Suitable filter bank architecture.

“Suitable” in this context, relates to the trade-off between acceptable functionality and footprint. It is worth noting that for a complete cochlear implant the following specifications should be added

1. A suitable signal processing strategy related to choice of analogue, digital, or hybrid, mixed processing.
2. Flexibility to provide high performance in different environments.
3. Minimum possible cost while meeting all above specifications.

It is desirable to realise completely implanted cochlea, but further reduction in power consumption and size are required to realise this objective.
OTA-C filters for Cochlear Implants

Increasing the dynamic range is essential for such applications, so as to increase the filter ability in handling a wide range of input acoustic signals with amplitudes that may exceed 1V. This has been achieved by satisfying one or both of the two constraints represented by increasing the input linear range and decreasing the input-referred noise floor. The following topics show the important factors affecting the filter performance studied, for this case.

The OTA-C filter topologies proposed for cochlear implants should have a wide linear input range. An increase in linear range over a simple OTA has been achieved by combining both bumping MOSFETs and capacitor attenuation techniques together for the first time. This approach was shown to give a linear range increase for the proposed OTA to be ±900 mV at < 5% $THD$; about a 64 fold improvement.

As mentioned earlier, the relevant noise here consists of two types namely white and flicker. The white noise is characterised by its flat power spectrum in all frequencies of interest. The sub-threshold MOSFET current is due to the diffusion mechanism. This current is represented by the motion of the discrete charge carriers. Because of thermal fluctuations, these charge carriers have random, motions which give rise to shot-noise currents. For this reason the white noise is known as thermal noise or shot noise since the thermal noise is a two sided shot noise. The white noise per unit bandwidth is inversely proportional to MOSFET current. The flicker “$1/f$” noise on the other hand is a result of surface potential fluctuations due to oxide charge carrier trapping and release by energy states near to the MOSFET silicon-oxide interface. It is inversely proportional to MOSFET dimensions. The $1/f$ noise corner frequency, $f_c$ is proportional to MOSFET current. The reduction of $1/f$ noise is related to the increase of MOSFET area. The sizing of the OTA MOSFETs, using $g_m/I_D$ methodology, was therefore made to ensure that the white noise dominated over flicker noise using.
suitable dimensions on one hand and to ensure efficient operation on the other. The values of attenuator and output capacitors were chosen to be $C_1=0.5\text{pF}$, $C_2=7.5\text{pF}$, and $C=2\text{pF}$ respectively to set an increase of 16 fold in the linear range and a value of about $66\text{dB}$ for the dynamic range. The use of capacitor attenuators also resulted in an increase in noise voltage of a factor $\sqrt{16}$. Hence, a net increase in the filter dynamic range of 4fold was obtained using these capacitor attenuators. An additional increase of dynamic range of more than 4 fold due to the bumping MOSFETs was also obtained, with free noise cost. The net increase in dynamic range with the proposed OTA was 18dB. The performance of the filter was assessed by defining a figure of merit, $FOM$ for the filter. The $FOM$ reflects the filter performance at a specific operating voltage and power level. This value shows the filter performance represented by its dynamic range, bandwidth, and filter order; the “transition bands steepness” in terms of power consumption and supply voltage. The FOM depends linearly on power and voltage and inversely on the performance parameters. It is required to obtain a high performance using minimum power consumption and supply voltage, so a minimum $FOM$ value refers to a more efficient filter.

The $FOM$ values for the experimental results of proposed topologies 1 and 2 OTA-C filters for cochlear implants were found to be $9.13\times10^{-13}$ and $8.37\times10^{-13}$ for (100-200) Hz and (5-10k) Hz bands for topology 1. For topology 2 they were $9.15\times10^{-13}$ and $9.66\times10^{-13}$ for both frequency bands mentioned above. These values were compared to those of five other filters obtained in recent work by other researchers. The $FOM$ values obtained in this work are the lowest or “best” among other values except that of [5.14] that equals $3.4\times10^{-13}$. The filter in [5.14] used as a wearable acoustic-based breathing detector has a dynamic range of 49dB. So, this dynamic range can not provide the 60dB limit of dynamic range required for cochlear implants. In other words, the proposed OTA-C filters in this work have good figure of merit values as filters to be used in cochlear implants and suitable for such future applications. Besides, the $FOM$
values for the proposed OTA-C filters can be reduced by a factor of 9 if the supply voltage decreased from ±1.5V to 1V.

7.1.2 EEG Signals

The EEG signals represent the synchronous activity resultant of thousands to millions of neurons of the same spatial orientation. They are very important physiological signals since they reflect different activities within the brain. OTA-C filters with low voltage operation and ultra low power consumption are essential for miniaturization of devices in such applications. This leads to the realisation of lightweight and flexible devices such as wearable EEG systems that are preferred by users for applications ranging from disease diagnostics to brain-computer interfaces, BCI.

OTA-C filter for EEG Applications

For such applications, the OTA-C filters need to exhibit very low power consumption and a low input-referred noise floor. In such applications, increasing the linear range is not essential since EEG signals have very low amplitudes typically in the range (2-200) µV.

However, in such applications, a small filter input-referred noise floor is essential to be able to distinguish such low amplitude signals. Many previous designs focused on decreasing the OTA transconductance, $G_m$, to obtain such very low frequency signals. This has led to the use of complex OTA structures which in turn increase the OTA input noise floor. If EEG signals are still below the filter noise floor, the signals are amplified before filtering. The OTA proposed in this work has a very low noise floor as a result of the choice of a simple differential OTA with bumping MOSFETs that have a free noise cost. The effect of $1/f$ noise was further reduced by shifting it
outside the frequency range of the EEG signals. This was accomplished by reducing the bias current required for obtaining such frequency range to 10’s of pico-amperes. The flicker noise corner frequency therefore, becomes very small. Consequently white noise was still dominant over $1/f$ in this case, despite the operation in very small frequency bands. The values of filter capacitors were chosen to be $C=8pF$ to obtain the required low frequency EEG bands. On the other hand, this relatively high value for the output capacitors causes a reduction in the filter thermal noise. This approach served to realise the very small frequency EEG bands and to reduce the dominated white noise to a minimum.

MOSFET dimensions were chosen using the $g_m/I_D$ methodology. However, the OTA transition frequency is inversely proportional to MOSFET dimensions and was taken in account in the designs. The OTA MOSFETs dimensions were chosen as a trade-off between providing the required transition frequency whilst minimising mismatch.

Low power consumption was obtained by the use of the smallest possible bias current levels, in the pico-amperes range. Despite the need for $4^{th}$ order OTA-C filters comprising six OTAs, the power consumed was low. For EEG bands $\delta$, $\theta$, and $\alpha$, it did not exceed the pico-Watt range while that needed to provide $\beta$ band was less than 3nW.

The aforementioned $FOM$ values for the proposed OTA-C filter are $12.73\times10^{-13}$, $11.78\times10^{-13}$, $12.79\times10^{-13}$, and $13.3\times10^{-13}$ for $\delta$, $\theta$, $\alpha$, and $\beta$ bands respectively. These realised $FOM$ values represent the smallest ones compared to reported designs except the most recent design in [6.13]. That filter has the smallest $FOM$ value of $1\times10^{-13}$ in that comparison used a low voltage supply of 1V. On the other hand, the proposed filter showed better noise floor, dynamic range, and smaller area than that filter. The $FOM$ values of the proposed filter can be reduced to be the best as suggested later in the next section.
7.2 Further Work

The results obtained in this work provide encouragement to continue the research towards more efficient designs for the next generation filters for biomedical applications. The two following suggestions are proposed for further work intended to accomplish in future.

The first suggestion relates to the design and construction that could be undertaken for a completely implanted cochlea. In addition to the OTA-C filter discussed in chapter five, the other cochlear implant stages mentioned in chapter one should be explained. This requires identification of the available analogue and digital signal processing strategies. Then, the most convenient strategy can be selected. The advantages and disadvantages of whether to use analogue or digital systems and the expected advantages from combining both of them in a hybrid system should be carefully considered and studied. Some of the key issues characterising the use of analogue and digital processing are summarised below.

The analogue processing is done on the continuous physical signals obtained from the real world. The computations are made according to the physics of the computing devices such as the physical relations and interactions of active and passive devices. Such systems are sensitive to variability in the physical device parameters. This can be considered as the reason for error in such systems. The noise is mainly due to thermal fluctuations in physical devices “white noise” with some other noise type “flicker noise” due to energy states near the MOSFET gate-oxide interface. The noise is accumulated in case of using cascading approach for many stages complex configurations.

The digital processing is done on the discrete signals obtained from analogue to digital converter, ADC. Generally the continuous signals are sampled at a certain rate
then quantised to be expressed in 0 and 1 denotation. Such systems are insensitive to mismatch. The noise in such systems is due to quantisation or rounding error, particularly from the analogue to digital conversion process. It can be reduced by increasing the resolution represented by increasing number of bits.

Using physics to do computation can be powerful as in analogue computation which is more efficient but less adaptable than its digital counterpart. The multiplication process of two currents in analogue computation needs a multiplier circuit of 4 to 8 MOSFETs. In digital computation a parallel 8-bit multiply for that last example requires roughly 3000 MOSFETs. Consequently, the number of devices required for performing a computation process can be greater in digital systems than analogue in many cases. Consequently, digital circuits have typically higher area consumption than analogue circuits. Also, the power consumption is generally higher in digital circuits than their analogue counterparts. This is due to the large number of devices and the communication overhead needed for digital computations. However, the complex digital configurations are more feasible to implement than analogue ones since the round-off error does not have significant accumulation with increasing computations.

From the above considerations, it can be concluded that the analogue computation processing is more feasible than the digital one for non-complex systems. For complex systems, the digital computation processing is more feasible than analogue one. In other words, analogue computation is efficient at low-precision processing, while the digital computation is efficient at high-precision processing. Therefore, proposing a hybrid mixed signal approach may be more powerful in such applications. Such hybrid architecture is intended to exploit the advantages of both analogue and digital computations.

The second suggestion is to improve the figure of merit, $FOM$ value of the band-pass OTA-C filter for EEG applications. This can be achieved by cascading the
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Conclusions and Further Work

proposed filter with a low-pass notch filter. This will increase the roll-off characteristics on the one hand and is expected not to add high additional noise on the other. This is because the band-pass shape has small noise content. Also, the battery size can be decreased by reducing the supply voltage to 1V range instead of ±1.5V. This will help to further reduce the FOM value. So, the reduction in FOM value is expected to be the result of further reduction in the supply voltage in addition to the increase of the filter order. However, the power consumption will be increased due to addition of the low-pass notch filter stage. Fortunately, this increase in power consumption will be small due to the use of very small operating currents as well as the low supply voltage. So, it is hoped to get a best filter performance in terms of minimum power consumption and supply voltage.
Appendix A

Derivation of average power for correlated noise sources

When analysing circuits, it is necessary to add the effect of several sources of noise to get the total contribution. Superposition is used for deterministic voltage and current signals but for random signals like noise, basically the average noise power is of interest and is obtained by adding two noise signals denoted by $x_1(t)$ and $x_2(t)$ then taking the average of the resulting power as follows

$$P_{av} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} [x_1(t) + x_2(t)]^2 \, dt$$

$$P_{av} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} x_1^2(t) \, dt + \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} x_2^2(t) \, dt + \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} 2x_1(t)x_2(t) \, dt$$

$$P_{av} = P_{av1} + P_{av2} + \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} 2x_1(t)x_2(t) \, dt$$

where $P_{av1}$ and $P_{av2}$ are the average power of $x_1(t)$ and $x_2(t)$, respectively and the third term in the above equation represents the correlation term which indicates how $x_1(t)$ and $x_2(t)$ are similar to each other. The noise waveforms are usually uncorrelated if generated by independent devices which cause vanishing the third term from the last equation.
Appendix B

Detailed derivations of transfer functions of the proposed Topologies

B.1 Derivation of the transfer function of Topology 1

The nodal equations are used to get the transfer function for all the proposed filters. For the filter of figure 5.1, the nodal equations will be derived as follows

1. Node “X”

For node $X$, by apply Kirchhoff’s current law (KCL) in each node gives, $\sum$ currents around node $X=0$

\[
(V_X - V_m) sC_1 + V_X sC_2 - I_{G1} + V_X sC_A + I_{G1} = 0
\]

\[
(V_X - V_m) sC_1 + V_X sC_2 - (V_X G_{m1}) + V_X sC_A + I_{G1} = 0
\]

But $I_{G1}$ for the OTA “$G_{m1}$” = 0 and also it is the case for all other OTAs.

\[
V_X = \frac{V_m}{sC_1 (C_1 + C_2 + C_A) + G_{m1}} \tag{5.1}
\]

2. Node “Y”

For node $Y$, $\sum$ currents around node $Y=0$

\[
(V_Y - V_{out}) sC_3 + V_Y sC_4 - I_{G2} = 0
\]

\[
(V_Y - V_{out}) sC_3 + V_Y sC_4 - (V_{out} G_{m3}) + I_{G2} = 0
\]

\[
V_Y = \frac{V_{out} (sC_3 + G_{m3})}{s(C_3 + C_4)} \tag{5.2}
\]
3. For “$G_{m2}$”

\[ I_{O2} = V_{out} \left( sC_B + (V_{out} - V_Y) sC_3 - (V_X - V_Y) G_{m2} \right) \]

\[ V_{out} = \frac{V_X G_{m2} + V_Y (sC_3 - G_{m2})}{s(C_B + C_3)} \]  \hspace{1cm} (5.3)

By substituting the values of $V_X$ and $V_Y$ of equations (5.1) and (5.2) respectively in equation (5.3), gives

\[ V_{out} = \frac{V_{in} C_g m_2 (sC_3 + G_{m3}) + V_{out} (sC_3 + G_{m3}) ((sC_3 - G_{m2})}{s(C_B + C_3)} \]

\[ V_{out} = \frac{V_{in} C_g m_2}{(C_1 + C_2 + C_A) + G_{m1}} + V_{out} \frac{s^2 C_3^2 + s C_3 G_{m3} - s C_3 G_{m2} - G_{m2} G_{m3}}{s(C_B + C_3)} \]

\[ V_{out} = V_{in} \frac{C_g m_2}{(C_1 + C_2 + C_A) + G_{m1}} \]

\[ V_{out} = V_{in} \frac{s(C_B + C_3) (sC_3 + C_4) - (s^2 C_3^2 + s C_3 G_{m3} - s C_3 G_{m2} - G_{m2} G_{m3})}{s(C_3 + C_4)} \]

\[ V_{out} = V_{in} \frac{C_g m_2}{(C_1 + C_2 + C_A) + G_{m1}} \]

\[ V_{out} = V_{in} \frac{s^2 (C_B C_3 + C_B C_4 + C_3 + C_3 C_4) - (s^2 C_3^2 + s C_3 G_{m3} - s C_3 G_{m2} - G_{m2} G_{m3})}{s(C_3 + C_4)} \]

\[ V_{out} = V_{in} \frac{C_g m_2}{(C_1 + C_2 + C_A) + G_{m1}} \]
APPENDICES

Appendix B

LOW POWER ELECTRONIC CIRCUITS FOR BIOMEDICAL APPLICATIONS  Saad A. Hasan

\[ H_1(s) = \frac{V_{out}}{V_{in}} \]

\[ H_2(s) = \frac{sC_1 + G_{m1}}{sC_1 + s(C_3 + C_4) + sC_3(G_{m2} - G_{m3}) + G_{m2}G_{m3}} \]

\[ H_3(s) = \frac{V_{out}}{V_{in}} = \frac{s^2K_{Z1}}{(sK_{p3} + G_{m1})s^2K_{p2} + sK_{p1} + K_{p0}} \]  (5.4)

where

\[ K_{p3} = (C_1 + C_2 + C_A) \]

\[ K_{p2} = (C_B(C_3 + C_4) + C_3C_4) \]

\[ K_{p1} = C_3(G_{m2} - G_{m3}) \]

\[ K_{p0} = G_{m2}G_{m3} \]

\[ K_{Z1} = C_1(C_3 + C_4)G_{m2} \]

B.2 Derivation of the transfer function of Topology 2

The transfer function for this proposed filter which shown in figure 5.2 is derived as follows

1. Node “X”

For node X, \( \sum \) currents around node X=0

\[ (V_X - V_{in})sC_1 + V_X sC_2 + (V_X - V_{out})sC_3 - I_{O2} = 0 \]

\[ (V_X - V_{in})sC_1 + V_X sC_2 + (V_X - V_{out})sC_3 - (V_{out}G_{m2}) = 0 \]

\[ V_X s(C_1 + C_2 + C_3) = V_{in}C_1 + V_{out}(sC_3 + G_{m2}) \]  (5.6)

2. For “G_{m1}”

\[ I_{O1} = V_{out} sC + (V_{out} - V_X)sC_3 = -V_X G_{m1} \]

\[ V_X = V_{out} \frac{s(C + C_3)}{(sC_3 - G_{m1})} \]  (5.7)
By substituting the value of \( V_X \) of equation (5.7) in equation (5.6) yields

\[
V_{out} \frac{s(C + C_1)}{(sC_3 - G_{m1})} s(C_i + C_2 + C_3) = V_{in} sC_1 + V_{out} (sC_3 + G_{m2})
\]

\[
V_{out} \frac{s^2(C + C_3)(C_i + C_2 + C_3)}{(sC_3 - G_{m1})} = V_{in} sC_1 + V_{out} (sC_3 + G_{m2})
\]

\[
V_{out} \frac{s^2(C + C_3)(C_i + C_2 + C_3)}{(sC_3 - G_{m1})} - V_{out} (sC_3 + G_{m2}) = V_{in} sC_1
\]

\[
V_{out} \left( \frac{s^2(C + C_3)(C_i + C_2 + C_3) - (sC_3 - G_{m1})(sC_3 + G_{m2})}{(sC_3 - G_{m1})} \right) = V_{in} sC_1
\]

\[
H_2(s) = \frac{V_{out}}{V_{in}} \frac{sC_1(sC_3 - G_{m1})}{s^2(C(C_i + C_2 + C_3) + C_3(C_i + C_2)) + sC_3(G_{m1} - G_{m2}) + G_{m1}G_{m2}}
\]

\[
H_2(s) = \frac{V_{out}}{V_{in}} \frac{s^2K_{Z2} - sK_{Z1}}{s^2K_{p2} + sK_{p1} + K_{p0}}
\] (5.8)

where

\[
K_{p2} = (C(C_i + C_2 + C_3) + C_3(C_i + C_2))
\]

\[
K_{p1} = sC_3(G_{m1} - G_{m2})
\]

\[
K_{p0} = G_{m1}G_{m2}
\]

\[
K_{Z2} = C_1C_3
\]

\[
K_{Z1} = C_1G_{m1}
\]

### B.3 Derivation of the transfer function of Topology 3

The transfer function for this proposed filter which shown in figure 5.3 is derived as follows
1. **Node “X”**

For node X, \( \sum \text{currents around node } X = 0 \)

\[
(V_X - V_{in})sC_1 + V_X sC_2 + I_{G1} = 0
\]

\[
V_X = V_{in} \frac{C_1}{(C_1 + C_2)}
\]  

(5.10)

2. **For “G_{m1}”**

\[
I_{G1} = V_{out}sC_4 + (V_{out} - V_Y)sC_3 = (V_X - V_Y)G_{m1}
\]

\[
V_X G_{m1} = V_{out}s(C + C_3)(G_{m1} - sC_3)
\]  

(5.11)

3. **Node “Y”**

For node Y, \( \sum \text{currents around node } Y = 0 \)

\[
(V_Y - V_{out})sC_3 + V_Y sC_4 - I_{G2} = 0
\]

\[
(V_Y - V_{out})sC_3 + V_Y sC_4 - (V_{out} G_{m2}) = 0
\]

\[
V_Y = V_{out} \frac{(sC_3 + G_{m2})}{s(C_3 + C_4)}
\]  

(5.12)

By substituting the values of \( V_X \) and \( V_Y \) in equations (5.10) and (5.12) respectively, in equation (5.11) this gives

\[
V_{in} \frac{C_1 G_{m2}}{(C_1 + C_2)} = V_{out} \left( s(C + C_3) - \frac{(sC_3 + G_{m2})(G_{m1} - sC_3)}{s(C_3 + C_4)} \right)
\]

\[
V_{in} \frac{C_1 G_{m2}}{(C_1 + C_2)} = V_{out} \left( \frac{(s(C + C_3))(s(C_3 + C_4)) + (sC_3 + G_{m2})(G_{m1} - sC_3)}{s(C_3 + C_4)} \right)
\]
V_{in} \left( \frac{C_i G_{m2}}{C_1 + C_2} \right) = \\
V_{out} \left( \frac{s^2 \left[ C C_3 + C C_4 \right] + s C_3 \left( G_{m1} - G_{m2} \right) + G_{m1} G_{m2}}{s (C_3 + C_4)} \right) \\
H_3(s) = \frac{V_{out}}{V_{in}} = \frac{s C_1 \left( C_3 + C_4 \right) G_{m1}}{(C_1 + C_2) \cdot \left( s^2 \left[ C (C_3 + C_4) + C_3 C_4 \right] + s C_3 \left( G_{m1} - G_{m2} \right) + G_{m1} G_{m2} \right)}

\begin{align*}
H_3(s) &= \frac{V_{out}}{V_{in}} = \frac{s K_{z1}}{s^2 K_{p2} + s K_{p1} + K_{p0}} \\
\end{align*}

(5.13)

where 

\begin{align*}
K_{p2} &= (C_1 + C_2) \left( C (C_3 + C_4) + C_3 C_4 \right) \\
K_{p1} &= C_3 \left( C_1 + C_2 \right) \left( G_{m1} - G_{m2} \right) \\
K_{p0} &= (C_1 + C_2) G_{m1} G_{m2} \\
K_{z1} &= C_1 \left( C_3 + C_4 \right) G_{m1}
\end{align*}

B.4 Derivation of the transfer function of Topology 4

The transfer function for this proposed filter which shown in figure 5.4 is derived as follows

1. Node “X”

For node X, \( \Sigma \) currents around node X=0

\[ V_X = V_{in} \left( \frac{C_i}{C_1 + C_2} \right) \]  \hspace{1cm} (5.15)

\[ I_{o1} = V_{o1} s C_A + (V_{o1} - V_Y) s C_3 = (V_X - V_Z) G_{m1} \]

2. For “\( G_{m1} \)”

\[ (V_X - V_{in}) s C_1 + V_X s C_2 + I_{o1} = 0 \]

\[ V_{o1} = \frac{1}{s(C_A + C_3)} (V_X G_{m1} + V_Y s C_3 - V_Z G_{m1}) \]  \hspace{1cm} (5.16)

3. Node “Y”
For node \( Y \), \( \sum \) currents around node \( Y = 0 \)

\[
(V_Y - V_{on})sC_1 + V_YsC_4 + I_{G2} = 0
\]

\[
V_Y^2 = \frac{V_{on}}{(C_3 + C_4)} \tag{5.17}
\]

4. For “\( G_{m2} \)"

\[
I_{G2} = V_{out} sC_B + (V_{out} - V_Z)sC_5 = (V_Y - V_Z) G_{m2}
\]

\[
V_{out} = \frac{1}{s(C_B + C_5)}(V_Y(G_{m2} - V_Z(G_{m2} - sC_5)) \tag{5.18}
\]

5. Node “\( Z \)"

For node \( Z \), \( \sum \) currents around node \( Z = 0 \)

\[
(V_Z - V_{out})sC_5 + V_ZsC_6 - I_{G3} + I_{G3} = 0
\]

\[
(V_Z - V_{out})sC_5 + V_ZsC_6 - (V_{out}G_{m3}) + I_{G3} = 0
\]

\[
V_Z = V_{out} \left( \frac{sC_5 + G_{m3}}{s(C_5 + C_6)} \right) \tag{5.19}
\]

By substituting the value of \( V_X \) of equation (5.15) in equation (5.16),

\[
V_{on} = \frac{1}{s(C_A + C_3)} \left( \frac{V_{in} C^1 G_{m1}}{(C_1 + C_2)} + V_YsC_3 - V_ZG_{m1} \right) \tag{5.20}
\]

The value of \( V_{on} \) of equation (5.20) above is substituted in equation (5.17) to give

\[
V_Y = \frac{1}{s(C_A + C_3)} \left( \frac{V_{in} C_G G_{m1}}{(C_1 + C_2)} + V_YsC_3 - V_ZG_{m1} \right) \left( \frac{C_3}{(C_3 + C_4)} \right)
\]

\[
V_Y \left( 1 - \frac{sC_2^2}{(C_3 + C_4)s(C_A + C_3)} \right) = \frac{1}{s(C_A + C_3)} \left( \frac{V_{in} C_G G_{m1}}{(C_1 + C_2)} - V_ZG_{m1} \right) \left( \frac{C_3}{(C_3 + C_4)} \right)
\]
\[ V_y = \frac{C_3}{s[(C_A + C_3)(C_3 + C_4) - C_3^2]} \left( V_{in} \frac{C_1 G_{m1}}{(C_1 + C_2)} - V_{out} \frac{(sC_5 + G_{m3})G_{m1}}{s(C_5 + C_6)} \right) \]  

(5.21)

By substituting the values of \( V_y \) and \( V_Z \) of equations (5.21) and (5.19) respectively in equation (5.18), yields

\[ V_{out} = \frac{1}{s(C_B + C_5)} \left\{ \frac{C_3 G_{m2}}{s[(C_A + C_3)(C_3 + C_4) - C_3^2]} \left( V_{in} \frac{C_1 G_{m1}}{(C_1 + C_2)} - V_{out} \frac{(sC_5 + G_{m3})G_{m1}}{s(C_5 + C_6)} \right) \right\} \]

\[ = V_{out} s(C_B + C_5) \left( \frac{C_3 G_{m2}}{s[(C_A + C_3)(C_3 + C_4) - C_3^2]} \left( \frac{C_3 G_{m2} G_{m1}}{(C_A + C_3)(C_3 + C_4) - C_3^2} \right) + (G_{m2} - sC_5) \right) \]

By rearranging and simplifying terms in the above equation, the following transfer function is obtained
\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{sC_1C_3(C_5 + C_6)G_{m1}G_{m2}}{s^3\left(\left(AC_A C_3 + C_4\right) + C_3C_4\left(AC_A C_3 + C_6 + C_5C_6\right)\right)}
\]

For
\[C_1 = C_3, \ C_2 = C_4, \ C_1 = rC_2, \ C_4 = rC_3, \ \text{and} \ C_6 = rC_5\]

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{sC_3G_{m1}G_{m2}}{s^3C_3\left((C_A (1 + r)) + rC_3\right)^2 + s^2C_3\left(G_{m2} - G_{m3}\right)\left((C_A (1 + r)) + rC_3\right)}
\]

For \(a = 1 + r\)

\[
H_4(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{sC_3G_{m1}G_{m2}}{s^3C_3\left(AC_A + rC_3\right)^2 + s^2C_3\left(G_{m2} - G_{m3}\right)\left(AC_A + rC_3\right)}
\]

\[
H_4(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{sk_{Z1}}{s^3K_{p3} + s^2K_{p2} + sk_{p1} + K_{p0}} \quad (5.22)
\]

\[K_{p3} = C_3\left(AC_A + rC_3\right)^2\]

\[K_{p2} = C_3\left(G_{m2} - G_{m3}\right)\left(AC_A + rC_3\right)\]

\[K_{p1} = G_{m2}\left(C_3G_{m1} + (AC_A + rC_3)G_{m3}\right)\]

\[K_{p0} = G_{m1}G_{m2}G_{m3}\]

\[K_{Z1} = C_3G_{m1}G_{m2}\]
B.5 Obtaining the poles of the proposed Topology 4

The denominator of equation (5.22) is a 3rd order polynomial which makes the process of gating its poles more complicated than 2nd order polynomial. However, the three poles are obtained using Maple software. Two of those poles are two complex conjugate poles and a real pole all of which lie in the negative “left hand” side of the s-plane. So, the filter’s transfer function general factorised form becomes as follows

\[
H_4(s) = \frac{V_{out}}{V_{in}} = \frac{sC_3G_mG_{m2}}{(s + a) \cdot (s + b + jc) \cdot (s + b - jc)}
\]  

(5.23)

where the filter’s real and the two complex conjugate poles respectively are shown below

\[p_1 = -b_0\]
\[p_2 = -b_1 - jc\]
\[p_3 = -b_1 + jc\]

So, by using the following code in Maple 13 software, the general solution for the following 3rd order equation appears which consisting of three roots named as in software, sols [1], sols [2], and sols [3] as follows

```maple
restart; poly := Kp3 \cdot S^3 + Kp2 \cdot S^2 + Kp1 \cdot S + Kp0;
poly := Kp3 \cdot S^3 + Kp2 \cdot S^2 + Kp1 \cdot S + Kp0
> sols := solve(poly, S);
```
\[
\frac{1}{6} \frac{1}{Kp3} \left( 36 Kp1 Kp2 Kp3 - 108 Kp0 Kp3^2 - 8 Kp2^3 \\
+ 12 \sqrt{3} \left( 4 Kp1^3 Kp3 - Kp1^2 Kp2^2 - 18 Kp1 Kp2 Kp3 Kp0 \\
+ 27 Kp0^2 Kp3^2 + 4 Kp0 Kp2^3 \right)^{1/2} Kp3 \right)^{1/3} \\
- \frac{2}{3} \left( 3 Kp1 Kp3 - Kp2^2 \right) / \left( Kp3 \left( 36 Kp1 Kp2 Kp3 \\
- 108 Kp0 Kp3^2 - 8 Kp2^3 \\
+ 12 \sqrt{3} \left( 4 Kp1^3 Kp3 - Kp1^2 Kp2^2 - 18 Kp1 Kp2 Kp3 Kp0 \\
+ 27 Kp0^2 Kp3^2 + 4 Kp0 Kp2^3 \right)^{1/2} Kp3 \right)^{1/3} \right) - \frac{1}{3} \frac{Kp2}{Kp3}
\]
\[-\frac{1}{12}\frac{1}{Kp^3} \left(36Kp^3 - 108Kp0 Kp3^2 - 8Kp2^3\right) + 12\sqrt{3} \left(4Kp^3 - Kp^2 Kp2^2 - 18Kp1 Kp2 Kp3 Kp0\right) + 27Kp0^2 Kp3^2 + 4Kp0 Kp2^3\right)^{1/3}\]

\[+ \frac{1}{3} \left(3Kp1 Kp3 - Kp2^2\right) \left(36Kp1 Kp2 Kp3 - 108Kp0 Kp3^2 - 8Kp2^3\right) \left(4Kp^3 - Kp^2 Kp2^2 - 18Kp1 Kp2 Kp3 Kp0\right) + 27Kp0^2 Kp3^2 + 4Kp0 Kp2^3\right)^{1/3}\]

\[-\frac{1}{3} \left(12\sqrt{3} \left(4Kp^3 - Kp^2 Kp2^2 - 18Kp1 Kp2 Kp3 Kp0\right) + 27Kp0^2 Kp3^2 + 4Kp0 Kp2^3\right)^{1/3}\]

\[+ \frac{1}{2} \frac{1}{Kp^3} \left(36Kp1 Kp2 Kp3 - 108Kp0 Kp3^2 - 8Kp2^3\right) + 12\sqrt{3} \left(4Kp^3 - Kp^2 Kp2^2 - 18Kp1 Kp2 Kp3 Kp0\right) + 27Kp0^2 Kp3^2 + 4Kp0 Kp2^3\right)^{1/3}\]

\[+ \frac{2}{3} \left(3Kp1 Kp3 - Kp2^2\right) \left(36Kp1 Kp2 Kp3 - 108Kp0 Kp3^2 - 8Kp2^3\right) \left(4Kp^3 - Kp^2 Kp2^2 - 18Kp1 Kp2 Kp3 Kp0\right) + 27Kp0^2 Kp3^2 + 4Kp0 Kp2^3\right)^{1/3}\]
sols [3]:
\[-\frac{1}{12} \frac{1}{Kp3} \left(36 \times Kp1 \times Kp2 \times Kp3 - 108 \times Kp0 \times Kp3^2 - 8 \times Kp2^3\right)\]
\[+ 12 \sqrt{3} \left(4 \times Kp1^3 \times Kp3 - Kp1^2 \times Kp2^2 - 18 \times Kp1 \times Kp2 \times Kp3 \times Kp0\right)\]
\[+ 27 \times Kp0^2 \times Kp3^2 + 4 \times Kp0 \times Kp2^3 \right)^{1/3} Kp3^{1/3}\]
\[+ \frac{1}{3} \left(3 \times Kp1 \times Kp3 - Kp2^2\right) \left(Kp3 \left(36 \times Kp1 \times Kp2 \times Kp3\right)\right)\]
\[- 108 \times Kp0 \times Kp3^2 - 8 \times Kp2^3\]
\[+ 12 \sqrt{3} \left(4 \times Kp1^3 \times Kp3 - Kp1^2 \times Kp2^2 - 18 \times Kp1 \times Kp2 \times Kp3 \times Kp0\right)\]
\[+ 27 \times Kp0^2 \times Kp3^2 + 4 \times Kp0 \times Kp2^3 \right)^{1/3} Kp3^{1/3}\]
\[- \frac{1}{2} \times 1 \sqrt{3} \left(\frac{1}{6} \frac{1}{Kp3} \left(36 \times Kp1 \times Kp2 \times Kp3\right)\right)\]
\[- 108 \times Kp0 \times Kp3^2 - 8 \times Kp2^3\]
\[+ 12 \sqrt{3} \left(4 \times Kp1^3 \times Kp3 - Kp1^2 \times Kp2^2 - 18 \times Kp1 \times Kp2 \times Kp3 \times Kp0\right)\]
\[+ 27 \times Kp0^2 \times Kp3^2 + 4 \times Kp0 \times Kp2^3 \right)^{1/3} Kp3^{1/3}\]
\[+ \frac{2}{3} \left(3 \times Kp1 \times Kp3 - Kp2^2\right) \left(Kp3 \left(36 \times Kp1 \times Kp2 \times Kp3\right)\right)\]
\[- 108 \times Kp0 \times Kp3^2 - 8 \times Kp2^3\]
\[+ 12 \sqrt{3} \left(4 \times Kp1^3 \times Kp3 - Kp1^2 \times Kp2^2 - 18 \times Kp1 \times Kp2 \times Kp3 \times Kp0\right)\]
\[+ 27 \times Kp0^2 \times Kp3^2 + 4 \times Kp0 \times Kp2^3 \right)^{1/3} Kp3^{1/3}\]
\]

So that, the filter three poles represented by the real one, \(b_0\) and the two other complex conjugate poles, \(-b_1 \pm jc\) are as follows:

\(b_0 = \text{sol [1]}
\[-b_1 - jc = \text{sol [2]}
\[-b_1 + jc = \text{sol [3]}

\]