Programmable Topology Derivation and Analysis of Integrated Three-Port DC-DC Converters with Reduced Switches for Low-Cost Applications

Guipeng Chen, Member, IEEE, Zhufeng Jin, Yuwei Liu, Yihua Hu, Senior Member, IEEE, Jiangfeng Zhang and Xinlin Qing

Abstract—Thanks to the favorable advantage of low cost, integrated three-port dc-dc converters with reduced switches have attracted extensive attention. In order to provide more new topologies, this paper aims to propose a programmable topology derivation method, which effectively simplifies the cumbersome process of the conventional combination method. Instead of the manual connection and examination, the proposed alternative can quickly and rigorously derive multiple viable integrated three-port dc-dc topologies from a great number of possible connections with the aid of computer program. Besides, generalized analysis is also accomplished, with which performance characteristics of all derived converters are simultaneously obtained and then a comprehensive comparison can be easily conducted to select a preferred one for the practical application. Finally, an example specific application with one input and two outputs is given, with topology selection, design and experimental results demonstrated in detail.

Index Terms— Generalized Analysis, Integrated Three-Port DC-DC Converters, Programmable Topology Derivation, Reduced Switches.

I. INTRODUCTION

With the increase of different sources/loads in engineering applications, multi-port dc-dc converters are widely demanded to control power flow and regulate voltages among different ports, including photovoltaics, fuel cell, battery and auxiliary power supply [1-8]. To construct a multi-port system, employing multiple conventional single-input single-output (SISO) dc-dc converters is a feasible solution, but undesired high cost and large volume are incurred due to the large number of components. Actually, components such as magnetic elements and semiconductor devices in different power electronics converters can be multiplexed to achieve reduced cost, which have been adopted to derive a variety of integrated multi-port converters in [9-18].

In [9, 10], only one transformer with several secondary windings is demanded in the flyback converter to provide multiple outputs. And a common inductor is shared in the single-inductor multi-port converters to transfer power among multiple input and output ports in [11-15]. Therefore, magnetic components which usually account for a large proportion of converter weight and volume are effectively reduced in these multi-port converters. Nevertheless, they suffer from cross-regulation problem that load variation of one output would affect other output voltages, because the magnetic component functions as the energy storage element. Besides, the magnetic elements, semiconductor devices can also be multiplexed. In [16-18], integrated three-port dc-dc converters with reduced switches/diodes are proposed, in which only three switches/diodes instead of four are utilized to generate the required two control variables for independent power control and voltage regulation. Therefore, not only low cost is obtained, but also no cross-regulation problem exists. However, only three different types of integrated three-port topologies have been proposed in [16-18], which cannot always be the best choice for different applications. For example, the current stresses of converters in [16, 18] will increase in comparison with the conventional two separate converters, and the sum of two output voltages have to be smaller than the input voltage in the converter in [17]. Therefore, more viable topologies should be explored, and then an optimum one can be selected by engineers according to the requirements.

With the purpose of providing more new topologies, several topology derivation methods including combination [19-22], duality [23-25] and addition/replacement of cells [26-28], have been presented in the past literatures, among which the combination method attracts increasing attentions recently thanks to its systematicness. With the combination method [19-22], multiple new topologies can be obtained through combing several basic cells in different appropriate ways. For example, a family of forward converters including two-switch forward converter and interleaved series input parallel output forward converter, are obtained in [19] after combination and simplification of three forward cells. Although the theoretical idea seems to be very simple, the practical implementation process of the combination method is complicated, because there are a great number of possible connecting relationships among different cells, and their effectiveness are needed to be one-by-one manually examined to select viable ones. In
common practical applications, researchers may prefer to figuring out some viable topology configurations from all possible connections by their experience instead of examining all configurations one-by-one, and as a result, it is quite often that some preferred topologies are not found. In a word, the conventional manual topology derivation process of combination method is either complex or not precise enough.

From above, integrated three-port dc-dc converters with reduced switches are attractive in the engineering applications with low cost requirements. In order to derive more integrated three-port topologies for selection, this paper intends to use the combination method. However, the conventional manual effort of combination method would result in either complex or non-rigorous topology derivation process. Based on this, a programmable topology derivation method is proposed in this paper. It uses an algebraic array to represent the connections among converter components, transforms the electrical criteria into math relationships, and achieves all viable solutions simultaneously through computer program. With the proposed method, 10 viable integrated three-port converters with reduced switches including those proposed in [16-18, 28, 31], are quickly and rigorously derived from all possible connections. Compared with the topology synthesis in [29, 30], the transformation from the topology derivation to the mathematical problem is easier in this paper, since the state equation is eliminated and its electrical criteria are simpler. Besides, in order to conveniently select an optimum one for the practical application, generalized analysis is accomplished to simultaneously obtain performance characteristics of all proposed converters with the computer program. It can further avoid the huge one-by-one manual analysis, and then the comparison can be easily conducted. As a summary, this paper aims to explore a programmable method to conveniently provide more viable integrated three-port topologies for engineers and help to fast select the most preferred one according to the real application requirements.

The paper is organized as follows. The proposed programmable topology derivation method is introduced and employed to derive viable integrated multi-port dc-dc converters in section II. And the generalized analysis of all derived topologies is conducted in section III. In section IV, experimental verification on a specific application is taken as an example to be illustrated and finally, conclusions are drawn in section V.

II. PROGRAMMABLE TOPOLOGY DERIVATION

A. Integrated three-port circuit configuration

In the conventional three-port dc-dc system, two separate converters are typically employed to control the power flow and voltage regulation among three ports, as illustrated in Fig. 1 (a). The drive signals of the switches \( S_{1,2} \) in the converter 1 are complementary and so are those for the switches \( S_{3,4} \) in the converter 2. These drive signals are used to generate duty-cycles \( D_{1,2} \) in Fig. 1(b) which are employed to independently regulate the relationships among \( V_1 \), \( V_2 \) and \( V_3 \). However, because two separate converters are employed, the number of components is doubled, which results in undesired high cost. Actually, from Fig. 1(b), in order to obtain the two duty-cycles \( D_{1,2} \), three switches \( S_{1,3} \) are enough, instead of four. The duty-cycles \( D_{1,2} \) are respectively equal to 1-\( D_{1} \) and 1-\( D_{2} \). Therefore, by adjusting the duty-cycles \( D_{1,2} \) of switches \( S_{1,2} \), the desired \( D_{1,2} \) can be obtained. And the duty-cycle \( D_{11} \) of switch \( S_1 \) is equal to 2-\( D_{2} \) to ensure that there are always two switches in conduction. The circuit configuration of integrated three-port dc-dc converters is presented in Fig. 1(c), which retains the independent control among three ports with reduced overall cost.

From Fig. 1(c), nodes \( \{1, 2\}, \{3, 4\} \) and \( \{5, 6\} \) of \( V_1-V_3 \) can be theoretically connected to any two different nodes among \( \{a, b, c, d, e, f\} \), and thus there are \( (A_3^6)^3 = 27000 \) different possible connections in total. However, most of them cannot work because of violating the following two fundamental electrical criterions.

Criterion 1: Average voltages \( V_{1,avg} \) and \( V_{3,avg} \) of three ports must be larger than zero, and they should be independently controlled.
Criterion 2: At any switching interval, ports \( V_i/V_j/V_k \) and their combinations cannot be short-connected or parallel-connected due to the conduction of switches. Theoretically, according to above two electrical criterions, viable integrated three-port topologies can be selected from all possible connections through one-by-one manual judgement. However, the required workload is very heavy since there are too many possible connections. And with such heavy workload, some viable topologies may be undesired left out. In order to avoid these problems, a programmable alternative is proposed, with which multiple viable integrated three-port dc-dc topologies can be systematically and simply derived with only three steps.

B. Proposed programmable topology derivation

Unlike deriving topology with one-by-one manual examination in the conventional method, the proposed method can rigorously and conveniently select all viable topologies from possible connections through computer program. It only needs three steps, as illustrated in Fig. 2. Firstly, define the connecting relationships in the converter by unknowns \( x_i (i = 1, 2, \ldots 6) \) and the value of \( x_i \) represents the connecting position of ports \( V_i/V_j/V_k \). This step enables the transformation from deriving viable topologies into a mathematical problem of finding feasible solutions to \( x_i \). Secondly, the electrical criterions which must be satisfied to ensure the normal operation of converters are modeled by mathematical relations of \( x_i \) e.g. equations and inequalities. Finally, according to the mathematical relations, all solutions to \( x_i \) can be found for the problem through computer implementable algorithms and then all viable topologies can be simultaneously obtained.

To be specific, the detailed programmable topology derivation process of integrated three-port dc-dc converters from the circuit configuration in Fig. 1(c) is depicted in the following.

Firstly, turn the topology derivation process into a mathematical problem. Because each node among \( \{1, 2, 3, 4, 5, 6\} \) will connect to one node among \( \{a, b, c, d, e, f\} \), define the connecting position of node \( \hat{\circ} \) by \( x_i (i = 1, 2, \ldots 6) \). \( x_i \) is equal to 1, 2, 3, 4, 5 or 6, which respectively represents that node \( \hat{\circ} \) is connected to node \( a, b, c, d, e, \) or \( f \). Then, the problem of deriving all viable connecting relationships among nodes \( \{1, 2, 3, 4, 5, 6\} \) and nodes \( \{a, b, c, d, e, f\} \) is transformed to calculate the feasible solutions of \( x_i \) in the array \( A \) in (1).

\[
A = [x_1, x_2, x_3, x_4, x_5, x_6]
\]  

(1)

Secondly, in order to find the feasible solutions of \( x_1-6 \), list their mathematical relations according to the aforementioned fundamental electrical constraints. According to Criterion 1. (2) and (3) are respectively derived to ensure that average voltages \( V_{1,\text{avg}}-V_{3,\text{avg}} \) of three ports are larger than zero and they can be independently controlled. And from Criterion 2. (4) and (5) are respectively obtained to guarantee that ports \( V_i/V_j/V_k \) and their combinations cannot be short-connected or parallel-connected due to the conduction of switches at any time. \( V_{1,\text{avg}}-V_{3,\text{avg}} \) respectively represent the connecting voltages of \( V_1-V_3 \) in the switching interval.

\[
V_{i,\text{avg}} > 0 \quad i = 1, 2, 3
\]  

(2)
V1–V3 are independently controlled with the drive signals of switches S1–S3 in Fig. 1(b). Due to the different configurations, their performance characteristics are various and hence are preferred in different applications, such as auxiliary power supply, PV/battery hybrid system and battery cell equalizer.

### Table I

<table>
<thead>
<tr>
<th>x1</th>
<th>x2</th>
<th>x3</th>
<th>x4</th>
<th>x5</th>
<th>x6</th>
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<tr>
<td>Fig. 4 (a)</td>
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<td>6</td>
<td>1</td>
<td>4</td>
<td>2</td>
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<tr>
<td>Fig. 4 (b)</td>
<td>1</td>
<td>6</td>
<td>2</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>Fig. 4 (c)</td>
<td>1</td>
<td>6</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Fig. 4 (d)</td>
<td>1</td>
<td>6</td>
<td>2</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Fig. 4 (e)</td>
<td>1</td>
<td>4</td>
<td>2</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>Fig. 4 (f)</td>
<td>1</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Fig. 4 (g)</td>
<td>1</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Fig. 4 (h)</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>Fig. 4 (i)</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Fig. 4 (j)</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>6</td>
<td>4</td>
</tr>
</tbody>
</table>

### C. Extension to integrated N-port topologies

Apart from the integrated three-port dc-dc converters, the proposed programmable topology derivation method can also be applied to other similar integrated N-port topologies with simple modification as follows. For an integrated N-port circuit configuration, the number of elements xi in the array A in (1) is modified as 2N, and the value of each xi can be one of \{1, 2, … 2N\}. The number of voltage source in constraints (2)–(5) and the available connecting nodes in (6)–(9) are both changed to N. Then, referring to the aforementioned solving process step-by-step, viable integrated N-port topologies can be easily obtained from the similar computer code. Table II summarizes the calculation results of integrated two-port, three-port, four-port and five-port dc-dc converters, including the number of feasible topologies and the corresponding calculation time. It is noted that when N=2, the derived two-port topologies are well-known bidirectional buck/boost and buck-boost/buck-boost converters.

### Table II

<table>
<thead>
<tr>
<th>Number of ports(N)</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of feasible topologies</td>
<td>2</td>
<td>10</td>
<td>96</td>
<td>1564</td>
</tr>
<tr>
<td>Calculation time</td>
<td>1.327s</td>
<td>1.843s</td>
<td>8.477s</td>
<td>204.761s</td>
</tr>
</tbody>
</table>
III. GENERALIZED ANALYSIS

After topology derivation, performance analysis of all proposed topologies in Fig. 4 should be conducted to have a comprehensive comparison under the specific application so that a most preferred one can be selected. Although one-by-one manual evaluation of all topologies is feasible, it would be also a tedious and cumbersome work for engineers. Fortunately, because the circuit configurations of these proposed topologies are similar and only the connecting relationships of \( V_1 \sim V_3 \) are different, their performance analysis can be expressed in a generalized form with different \( x_i (i=1, 2, \ldots 6) \). Then, through a computer program, the performance characteristics of all proposed topologies including voltage/current relationship, ZVS operation and small-signal model, can also be simultaneously obtained.

A. Operational Principle

From the drive signals in Fig. 1(b), two and only two switches (or their parasitic diodes) among \( S_1 \sim S_3 \) should be in on-state at any time, to ensure that inductors \( L_1 \sim L_2 \) would not be disconnected and voltage source across \( \{a, f\} \) would not be shorted. According to the different phase relation, except for the drive signals in Fig. 1 (b) which is re-defined as DRA in Fig. 5(a), there is another drive signals DRB as shown in Fig. 5 (b). No matter with drive signal DRA or DRB, the operation of all proposed converters working in continuous conduction mode (CCM) is consisted of three different stages \((S_1, S_2, S_3)\) in a switching period, and their equivalent circuits in different stages are illustrated in Fig. 6. Because the switching process is relatively short, it is neglected. It is noted that operation with drive signal DRA and DRB are almost the same, except for the different sequence of stage \( S_1 \sim S_3 \). This difference only has an impact on the soft-switching operation of switches \( S_1 \sim S_3 \), which will be detailed analyzed afterwards.

B. Voltage Relationship

From (7), average voltages \( V_{Lavg} \sim V_{savg} \) of all proposed converters can be expressed as a function of voltage potentials \( \{V_{aavg}, V_{bavg}, V_{cavg}, V_{davg}, V_{eavg}, V_{favg}\} \) and \( x_2 \). Meanwhile, according to Fig. 1(c), the average voltages across two nodes \((a, c), (c, e) \) and \((e, f)\) are respectively equal to the average drain-to-source voltages \( \overline{V}_{a1} \sim \overline{V}_{e3} \) of switches \( S_1 \sim S_3 \), and \( V_{bavg}=V_{cavg}, V_{davg}=V_{eavg} \) can be obtained owing to the flux balance of inductors \( L_1 \sim L_2 \), which are summarized in (10).

Then, voltage relationships among \( V_{Lavg} \sim V_{savg} \) of all proposed three-port converters in Fig. 4 are easily derived in Table III from (7) and (10) by plugging in the \( x_i \) in Table I, which also could be implemented by computer program. Taking the converter in Fig. 4(a) as an example, \( x_1=1, x_2=6, x_3=4, x_4=2 \) and \( x_6=6 \) are obtained from Table I. Then, voltages of three ports are \( V_{Lavg}=V_{aavg}, V_{bavg}=V_{davg}, V_{favg}=V_{eavg}=(2-D_1)D_2D_3V_{bavg}, \) and \( V_{davg}=V_{cavg}, V_{favg}=(2-D_2)D_3V_{davg} \). From the drive signals of switches \( S_1 \sim S_3 \) in Fig. 5, there are always two switches in on-state at any time and hence \( D_1+D_2+D_3=2 \) are obtained. Then, voltage gains \( V_{2avg}/V_{1avg}=D_3, V_{3avg}/V_{1avg}=D_1 \) and \( V_{3avg}/V_{2avg}=D_3/D_1 \) can be derived. Besides, the voltage stresses \( V_{s1}, V_{s2}, V_{s3} \) of switches \( S_1 \sim S_3 \) in all proposed converter in terms of \( V_1 \sim V_3 \) are also summarized in Table III from Fig. 4.

\[
\begin{align*}
V_{a_{avg}} - V_{f_{avg}} &= \overline{V}_{a1} = (1-D_1)(V_{a_{avg}} - V_{f_{avg}}) \\
V_{c_{avg}} - V_{e_{avg}} &= \overline{V}_{c2} = (1-D_2)(V_{c_{avg}} - V_{e_{avg}}) \\
V_{c_{avg}} - V_{f_{avg}} &= \overline{V}_{c3} = (1-D_3)(V_{c_{avg}} - V_{f_{avg}}) \\
V_{b_{avg}} &= V_{c_{avg}} = V_{d_{avg}} = V_{e_{avg}}
\end{align*}
\]

where \( D_1 \sim D_3 \) are the duty-cycles of switches \( S_1 \sim S_3 \), respectively.

<table>
<thead>
<tr>
<th>TABLE III</th>
<th>VOLTAGE GAINS AND VOLTAGE STRESSES OF ALL PROPOSED CONVERTERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{2avg}/V_{1avg} )</td>
<td>( V_{3avg}/V_{1avg} )</td>
</tr>
<tr>
<td>( V_{s1,2,3} )</td>
<td></td>
</tr>
<tr>
<td>(a)</td>
<td>( D_3 )</td>
</tr>
<tr>
<td>(b)</td>
<td>( D_3 )</td>
</tr>
<tr>
<td>(c)</td>
<td>( 1-D_2 )</td>
</tr>
<tr>
<td>(d)</td>
<td>( 1-D_2 )</td>
</tr>
<tr>
<td>(e)</td>
<td>( D_3/D_1 )</td>
</tr>
<tr>
<td>(f)</td>
<td>( (1-D_3)(1-D_2) )</td>
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<tr>
<td>(g)</td>
<td>( (1-D_3)(1-D_2) )</td>
</tr>
<tr>
<td>(h)</td>
<td>( D_3/(1-D_2) )</td>
</tr>
<tr>
<td>(i)</td>
<td>( (1-D_2)(1-D_3) )</td>
</tr>
<tr>
<td>(j)</td>
<td>( 1/(1-D_2) )</td>
</tr>
</tbody>
</table>

C. Current Relationship

According to the operational principle, drain-to-source currents \( i_{L1} \sim i_{L2} \) in different stages \( S_1 \sim S_3 \) of all proposed converters are obtained in Table IV, as a function of inductor currents \( i_{L1} \sim i_{L2} \). Define \( k_i=\text{iseq}(x_i) \), \( i, j=1, 2, \ldots 6 \), which is equal to 1 if the node \( \bigcirc \) is connected to the \( j \)th node in \( \{a, b, c, \)
$d, e, f$) and is equal to 0 if not connected. Then, from Fig. 4, relationship among inductor currents $i_{L1}\sim i_{L2}$ and port currents $i_{1}\sim i_{3}$ is obtained in (11). Afterwards, the average inductor currents $I_{L1}\sim I_{L2}$ in terms of average port current $I_{1}\sim I_{3}$ of all proposed converters can be easily calculated by plugging in the corresponding $k_{th}$ through the computer program, as illustrated in Table V. Likewise, take the converter in Fig. 4(a) as an example. Because it has $x_{1}=1, x_{2}=6, x_{3}=1, x_{4}=4, x_{5}=2$ and $x_{6}=6$, $k_{1}=k_{2}=k_{3}=k_{4}=k_{5}=k_{6}=1$ can be obtained and the value of other $k_{th}$ is 0. Then according to (11), $I_{L1}=-I_{3}$ and $I_{L2}=I_{2}$ can be achieved.

$$i_{L1} = (k_{22} - k_{12})i_{1} + (k_{42} - k_{32})i_{2} + (k_{62} - k_{52})i_{3}$$
$$i_{L2} = (k_{24} - k_{14})i_{1} + (k_{44} - k_{34})i_{2} + (k_{64} - k_{54})i_{3}$$

(11)

### TABLE IV
DRAIN-TO-SOURCE CURRENTS $i_{1}\sim i_{3}$ IN DIFFERENT STAGES

<table>
<thead>
<tr>
<th>Stages</th>
<th>$i_{1}$</th>
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</tr>
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<tr>
<td>$St1$</td>
<td>$i_{1}$</td>
<td>0</td>
<td>$-i_{2}$</td>
</tr>
<tr>
<td>$St2$</td>
<td>$i_{1}+i_{2}$</td>
<td>$i_{2}$</td>
<td>0</td>
</tr>
<tr>
<td>$St3$</td>
<td>0</td>
<td>$-i_{1}$</td>
<td>$-i_{1}+i_{2}$</td>
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</table>

### TABLE V
AVERAGE INDUCTOR CURRENTS $I_{L1}\sim I_{L2}$ IN TERMS OF $i_{1}\sim i_{3}$

<table>
<thead>
<tr>
<th>Fig. 4</th>
<th>(a)</th>
<th>(b)</th>
<th>(c)</th>
<th>(d)</th>
<th>(e)</th>
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<tbody>
<tr>
<td>$I_{L1}$</td>
<td>$-I_{1}$</td>
<td>$-I_{2}$</td>
<td>$-I_{2}$</td>
<td>$-I_{1}+I_{2}$</td>
<td>$I_{1}$</td>
</tr>
<tr>
<td>$I_{L2}$</td>
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<td>$-I_{1}$</td>
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<td>$I_{2}$</td>
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<table>
<thead>
<tr>
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<th>(f)</th>
<th>(g)</th>
<th>(h)</th>
<th>(i)</th>
<th>(j)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{L1}$</td>
<td>$-I_{2}$</td>
<td>$-I_{1}$</td>
<td>$I_{1}$</td>
<td>$I_{2}$</td>
<td>$I_{1}$</td>
</tr>
<tr>
<td>$I_{L2}$</td>
<td>$I_{1}+I_{2}$</td>
<td>$I_{1}+I_{2}$</td>
<td>$-I_{1}$</td>
<td>$-I_{1}$</td>
<td>$-I_{1}$</td>
</tr>
</tbody>
</table>

D. ZVS Operation

From Table IV, drain-to-source currents $i_{1}\sim i_{3}$ in different stages $St1\sim St3$ of all proposed converters are equal to $\pm I_{1}, \pm I_{2}$ or $\pm (I_{L1}+I_{L2})$, with the neglect of ripple current. Comparing $I_{L1}, I_{L2}$ and $I_{L1}+I_{L2}$ with zero, six divided regions $R_{1}\sim R_{6}$ are obtained, as illustrated in Fig. 7. In different regions, ZVS operation of one switch among $S_{1}\sim S_{3}$ in all proposed converters can always be realized with drive signals $DRA$ or $DRB$, as shown in Fig. 8. In Fig. 8(a), drive signals $DRA$ are employed when the relationship between $I_{L1}$ and $I_{L2}$ is in region $R_{1} (I_{L1}<0, I_{L2}>0, I_{L1}+I_{L2}>0)$. According to Table IV, $i_{1}=I_{L1}$ is negative in stage $St1$ and $i_{1}=I_{L1}+I_{L2}$ is positive in stage $St2$. Therefore, current $i_{1}$ flows through the parasitic diode of switch $S_{1}$ before its turn-on, while current $i_{2}$ flows through the Mosfet channel of $S_{1}$ before its turn-off. Hence, ZVS operation of $S_{1}$ is achieved. Likewise, when $I_{L1}-I_{L2}$ are in region $R_{2} (I_{L1}>0, I_{L2}<0, I_{L1}+I_{L2}<0)$, ZVS operation of $S_{1}$ is also realized as illustrated in Fig. 8(b), but with the drive signals $DRB$ instead of $DRA$. Similarly, in regions $R_{3}$ and $R_{4}$, $S_{2}$ achieves ZVS operation with drive signals $DRA$ and $DRB$, respectively. And in region $R_{5}$ and $R_{6}$, $S_{3}$ achieves ZVS operation with drive signals $DRA$ and $DRB$, respectively. As a summary, one switch among $S_{1}\sim S_{3}$ in all proposed converters can always achieve ZVS operation over the whole current range of $I_{L1}$ and $I_{L2}$ when appropriate drive signal $DRA$ or $DRB$ is employed, contributing to reduced switching losses.

E. Small-Signal Model

From the aforementioned analysis, average drain-to-source voltages and currents of switches $S_{1}\sim S_{3}$ in all proposed converters are calculated in (12) and (13), respectively. In order to obtain small-signal linearized equation, all variables in (12) and (13) are assumed to be equal to their given quiescent values plus some superimposed small ac variations [32]. After neglecting the dc terms as well as second-order terms, their first-order ac terms are respectively derived in (14)−(15), based on which a unified small-signal model is obtained in Fig. 9. From Fig. 9, all proposed integrated three-port converters can easily derive their small-signal models through connecting nodes (1, 2, 3, 4, 5, 6) to the corresponding nodes (a, b, c, d, e, f).

$$v_{(1)}(t)_{T_{1}} = (1-d_{1}(t))v_{qf}(t)_{T_{1}}$$
$$v_{(2)}(t)_{T_{1}} = (1-d_{2}(t))v_{qf}(t)_{T_{1}}$$
$$v_{(3)}(t)_{T_{1}} = (1-d_{3}(t))v_{qf}(t)_{T_{1}}$$

(12)


\[
\begin{align*}
\langle i_1(t) \rangle_{T_c} &= d_1(t)\langle i_{i_1}(t) \rangle_{T_c} + (1 - d_1(t))\langle i_{i_2}(t) \rangle_{T_c} \\
\langle i_2(t) \rangle_{T_c} &= -(1 - d_1(t))\langle i_{i_3}(t) \rangle_{T_c} + (1 - d_3(t))\langle i_{i_4}(t) \rangle_{T_c} \\
\langle i_3(t) \rangle_{T_c} &= -(1 - d_1(t))\langle i_{i_5}(t) \rangle_{T_c} - d_3(t)\langle i_{i_4}(t) \rangle_{T_c}
\end{align*}
\]

(13)

\[
\begin{align*}
\dot{v}_{i_1}(t) &= (1 - D_s)\dot{v}_{d_1}(t) - V_{d_1}\dot{i}_{d_1}(t) \\
\dot{v}_{i_2}(t) &= (1 - D_s)\dot{v}_{d_2}(t) - V_{d_2}\dot{i}_{d_2}(t) \\
\dot{v}_{i_3}(t) &= (1 - D_s)\dot{v}_{d_3}(t) - V_{d_3}\dot{i}_{d_3}(t)
\end{align*}
\]

(14)

\[
\begin{align*}
\dot{i}_{a_1}(t) &= \dot{i}_{a_1}(t) + D_{a_1}\dot{i}_{d_1}(t) + (1 - D_{a_1})\dot{i}_{d_2}(t) \\
\dot{i}_{a_2}(t) &= \dot{i}_{a_2}(t) - (1 - D_{a_2})\dot{i}_{d_1}(t) + (1 - D_{a_2})\dot{i}_{d_3}(t) \\
\dot{i}_{a_3}(t) &= \dot{i}_{a_3}(t) - (1 - D_{a_2})\dot{i}_{d_1}(t) - D_{a_3}\dot{i}_{d_2}(t)
\end{align*}
\]

(15)

where \( \dot{i}_{a_1}(t) = I_{d_1}\dot{i}_{d_1}(t) - I_{a_2}\dot{i}_{d_3}(t) \)

Fig. 9. Unified small-signal model of all proposed three-port converters.

IV. EXPERIMENTAL VERIFICATION ON A SPECIFIC APPLICATION

After the above generalized analysis, performance characteristics of all proposed converters are obtained simultaneously. Then, according to the system parameters of the specific application, a preferred one can be easily selected out after comparison. In this section, an example application with one input \( V_{in} = 48V \), and two outputs \( V_{o1} = 36V, I_{o1,max} = 3A \), \( V_{o2} = 24V, I_{o2,max} = 2A \) will be analyzed to gain a comprehensive understanding.

A. Topology Selection and Design

Firstly, according to Table III in the voltage relationship analysis, the topology in Fig. 4(c) and (j) cannot work normally with the system parameters, because the sum of two small voltages is smaller than the large one in these two converters while \( V_{o1} + V_{o2} > V_{in} \) is required in the example application. Among the rest eight topologies, the ones in Fig. 4(a), (b) and (d) are preferred due to their relatively lower voltage stresses of switches. Secondly, according to Table V in the current relationship analysis, the average inductor currents are respectively \( I_{i_1}, I_{i_2} \) in the topologies Fig. 4 (a)–(b) while they are respectively \( I_{i_3} + I_{i_4}, I_{i_5} \) in the topology Fig. 4(d). Hence, thanks to lower average inductor current, topologies in Fig. 4 (a)–(b) will be further compared. Finally, from Table IV, the current stresses of switches are smaller in the topology Fig. 4(a) because of the opposite directions of inductor currents \( I_{i_1} - I_{i_2} \). Therefore, after the comprehensive comparison, the topology in Fig. 4(a) which can achieve relatively lower voltage/current stresses, is selected for the example application. The converter in Fig. 4(a) is re-depicted in Fig. 10(a) with port \( V_i \) as the input and ports \( V_o1-V_o3 \) as the outputs. In the example application, it is not only superior to other proposed converters in Fig. 4, but also can achieve lower cost as well as higher efficiency compared with conventional two separate buck converters in Fig. 10(b) due to the reduced switches and ZVS operation.

According to the generalized analysis, both the steady-state and dynamic characteristics of the proposed single-input dual-output (SIDO) buck converter in Fig. 10(a) can be easily obtained. The voltage gains among \( V_{in}, V_{o1} \) and \( V_{o2} \) are \( V_{o1}/V_{o2} = D_{a_1} \) and \( V_{o2}/V_{o1} = D_{a_3} \). Therefore, \( D_{a_1} \) and \( D_{a_3} \) are employed to independently control the output voltages \( V_{o1} \) and \( V_{o2} \). The duty-cycle \( D_{a_2} \) is equal to 2-\( D_{a_1} \)-\( D_{a_3} \). The average inductor currents \( I_{a_1}, I_{a_2} \) are respectively equal to output currents \( I_{o1}, -I_{o2} \). Because all switches \( S_1-S_3 \) are clamped by input voltage when they are off, their voltage stresses are equal to \( V_{in} \). Because \( V_{in} \) is relatively low, the improved switching losses of buck converter working in triangular conduction mode is limited, but the increased current stresses caused by the triangular current have an adverse effect on both the conduction losses and the power rating of switches as well as inductors, resulting in higher cost. Therefore, after comprehensive consideration of both efficiency and cost, the proposed and conventional SIDO buck converters in Fig. 10 are designed to work in the typical continuous conduction mode. Then from Table IV, the root mean square (RMS) values of drain-to-source currents \( i_{i_1} - i_{i_3} \) are calculated in (16), with the neglect of ripple current of inductors. Then, the parameters of hardware can be designed, which are summarized in Table VI.

\[
\begin{align*}
I_{i_{1,ms}}^2 &= (1 - D_{a_2})I_{i_{1,ms}}^2 + (1 - D_{a_1})(I_{a_1} + I_{a_2})^2 \\
I_{i_{2,ms}}^2 &= (1 - D_{a_3})I_{i_{2,ms}}^2 + (1 - D_{a_1})I_{i_{1,ms}}^2 \\
I_{i_{3,ms}}^2 &= (1 - D_{a_1})I_{i_{3,ms}}^2 + (1 - D_{a_3})(I_{a_3} + I_{a_2})^2
\end{align*}
\]

(16)

### TABLE VI

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage ( V_{in} )</td>
<td>48V</td>
<td>Switching Period ( T_s )</td>
<td>10\mu s</td>
</tr>
<tr>
<td>Output Voltage ( V_{o1} )</td>
<td>36V</td>
<td>Inductance ( L_1, L_2 )</td>
<td>150, 300 \mu H</td>
</tr>
<tr>
<td>Output Current ( I_{o1,max} )</td>
<td>3A</td>
<td>Capacitance ( C_1, C_2 )</td>
<td>100, 470 \mu F</td>
</tr>
<tr>
<td>Output Voltage ( V_{o2} )</td>
<td>24V</td>
<td>Switches ( S_1-S_3 )</td>
<td>IPP530N15N3</td>
</tr>
<tr>
<td>Output Current ( I_{o2,max} )</td>
<td>2A</td>
<td>Control Unit</td>
<td>TMS320FDSP2808</td>
</tr>
</tbody>
</table>

In addition, according to Fig. 9, the small-signal model of the proposed SIDO buck converter is obtained in Fig. 11. The small-signal model of the proposed SIDO buck converter is the
same as two separate buck converters connecting to a common input. Therefore, no cross-regulation problem exists in the proposed converter and good dynamic response can be achieved. The control-to-output and input-to-output transfer functions are respectively derived in (17) and (18), based on which a proportional-integral (PI) compensator can be designed and added into each control loop to improve converter performance, as illustrated in Fig. 12(a).

\[
\begin{align*}
G_{sd1} &= \frac{v_m(s)}{V_m(s)} t_{i_d(j)} = 0 = \frac{V_m}{L_C l_s^2 + L_s / R_s + 1} \\
G_{sv1} &= \frac{v_m(s)}{v_m(s)} d_{i_d(j)} = 0 = \frac{D_{11}}{L_C l_s^2 + L_s / R_s + 1} \\
G_{sd2} &= \frac{v_m(s)}{v_m(s)} d_{i_d(j)} = 0 = \frac{D_{12}}{L_C l_s^2 + L_s / R_s + 1} \\
G_{sv2} &= \frac{v_m(s)}{v_m(s)} d_{i_d(j)} = 0 = \frac{D_{13}}{L_C l_s^2 + L_s / R_s + 1}
\end{align*}
\]  

(17) 

\[
\begin{align*}
G_{sd1} &= \frac{v_m(s)}{V_m(s)} t_{i_d(j)} = 0 = \frac{V_m}{L_C l_s^2 + L_s / R_s + 1} \\
G_{sv1} &= \frac{v_m(s)}{v_m(s)} d_{i_d(j)} = 0 = \frac{D_{11}}{L_C l_s^2 + L_s / R_s + 1} \\
G_{sd2} &= \frac{v_m(s)}{v_m(s)} d_{i_d(j)} = 0 = \frac{D_{12}}{L_C l_s^2 + L_s / R_s + 1} \\
G_{sv2} &= \frac{v_m(s)}{v_m(s)} d_{i_d(j)} = 0 = \frac{D_{13}}{L_C l_s^2 + L_s / R_s + 1}
\end{align*}
\]  

(18) 

From above, the proposed integrated SIDO buck converter in Fig. 10(a) operates similarly with the conventional scheme consisting of two separate buck converters in Fig. 10(b), and their voltage gains, voltage stresses of switches, average inductor currents and small-signal models are also the same. However, the number of switches is reduced, switching losses are decreased and current stresses of switches are improved in the proposed converter, contributing to lower cost and higher efficiency.

(i) Number of switches: Only three switches \(S_1\)–\(S_3\) are employed in the proposed SIDO buck converter while four switches \(S_1\)–\(S_22\) are demanded in the conventional converter.

(ii) Switching losses: Because one switch in the proposed converter can always achieve ZVS operation, and the remaining two switches are respectively hard-switching and operating as the synchronous switch. Therefore, in comparison with the conventional two separate buck converters in which two switches are hard-switching and the other two operate as the synchronous switch, switching losses are effectively alleviated in the proposed converter.

(iii) Current stresses: The current stresses of switches \(S_1\)–\(S_22\) in Fig. 10(b) are calculated in (19). Duty-cycles \(D_{11}\) and \(D_{21}\) are respectively equal to \(D_{11}\) and \(D_{21}\). Then, combining with the current stresses of switches \(S_1\)–\(S_22\) in (16), the total RMS currents of switches in the proposed converter (Total_rms(Pro)) and in the conventional converter (Total_rms(Con)) are derived as shown in (20). With the parameters in Table VI, comparison result between the proposed (Total_rms(Pro)) and conventional (Total_rms(Con)) converter is depicted in Fig. 13. From Fig. 13, Total_rms of the proposed converter is smaller than that of the conventional one over wider load range. And smaller Total_rms achieved at rated load condition \(I_{L1}=3A, I_{L2}=2A\) also indicates that current stresses of switches are reduced in the proposed converter. In addition, at rated load condition, the square of RMS current of each switch is respectively
$I_{s, rms}^2 = 2.75$, $I_{s, rms}^2 = 4.25$, $I_{s, rms}^2 = 1.25$ for the proposed SIDO buck converter and $I_{s, rms}^2 = 6.75$, $I_{s, rms}^2 = 1.5$, $I_{s, rms}^2 = 2$, $I_{s, rms}^2 = 2$ for the conventional SIDO buck converter. Therefore, the conduction losses are distributed more equal in the proposed converter, which is also beneficial for the thermal design.

\[
\begin{align*}
I_{s1, rms} &= \sqrt{D_{s1}^2 I_{s1}^2}, \quad I_{s2, rms} = \sqrt{(1-D_{s1}) I_{s1}^2} \\
I_{s1, rms} &= -\sqrt{D_{s1}^2 I_{s2}^2} + \sqrt{(1-D_{s1}) I_{s2}^2} \\
\text{Total } \text{rms (Pro)} &= \sqrt{I_{s1, rms}^2 + I_{s2, rms}^2 + I_{s3, rms}^2} \\
\text{Total } \text{rms (Con)} &= \sqrt{I_{s1, rms}^2 + I_{s2, rms}^2 + I_{s1, rms}^2 + I_{s2, rms}^2} \tag{20}
\end{align*}
\]

B. Experimental results

Fig. 14 and Fig. 15 respectively show the steady-state waveforms of the proposed converter under condition A: $I_{o1}=3A$, $I_{o2}=2A$ and condition B: $I_{o1}=0.3A$, $I_{o2}=2A$. According to the theoretical analysis, drive signals DRA and DRB should be respectively employed for these two load conditions, as illustrated in Fig. 14(a) and Fig. 15(a). Then ZVS operation is achieved for $S_1$ under condition A as shown in Fig. 14(d), and it is achieved for $S_1$ under condition B as shown in Fig. 15(d). Besides, experimental waveforms of inductor currents $i_{L1}$-$i_{L2}$ and drain-to-source currents $i_{o1}$-$i_{o3}$ are also demonstrated in Fig. 14(b)-(c) and Fig. 15(b)-(c), which are in well coincidence with the theoretical analysis. It is noted that the spikes of drain-to-source currents $i_{o1}$-$i_{o3}$ are caused by the normal reverse recovery phenomenon of the parasitic diode of $S_2$, which operates as a synchronous switch.

Dynamic response of the proposed integrated SIDO buck converter with load variations between half and full rated load, is also shown in Fig. 16(a). Change of $I_{o1}$ mainly has an impact on $V_{o1}$ and nearly has no influence on $V_{o2}$. Similarly, when $I_{o2}$ varies, $V_{o2}$ is influenced while $V_{o1}$ almost remains unchanged. Therefore, no cross-regulation exists in the proposed converter that two output voltages $V_{o1}$ and $V_{o2}$ are independently controlled. In Fig. 17, measured efficiencies of the proposed and conventional SIDO buck converters are demonstrated. The components of conventional SIDO buck converter use the same ones in Table VI. The voltages/currents of input ($V_{in}$, $I_o$) and two outputs ($V_{o1}$, $I_{o1}$, $V_{o2}$, $I_{o2}$) are measured, and then the efficiency $\eta_{eff} = (V_{o1} I_{o1} + V_{o2} I_{o2})/V_{in} I_{o}$ is calculated. Thanks to the improved current stresses and ZVS operation of switches, higher efficiency is achieved in the proposed converter over whole load range, especially for the light load condition in which switching losses are dominant. Photo of the prototype circuit is shown in Fig. 16(b).


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